University of California, Santa Barbara

Department of Electrical & Computer Engineering

CMOS VLSI for Computer Engineering 194BB/594BB

Professor Theogarajan

Final Exam, December 4, 2009

Name: _____

This is open book and open notes exam. For all questions make reasonable approximations. Unless otherwise specified ignore body effect. All necessary formulas and values are given at the end of the exam for your convenience. GOOD LUCK!

Answer the questions in the spaces provided on the question sheets. If you run out of room for an answer, continue on the back of the page.

Question	Points	Score
1	45	
2	10	
3	45	
Total:	100	

1. Question 1: 45points

Consider the circuit shown in figure 1 which is a clock generator block used to double the clock frequency in the Pentium 4 microprocessor.

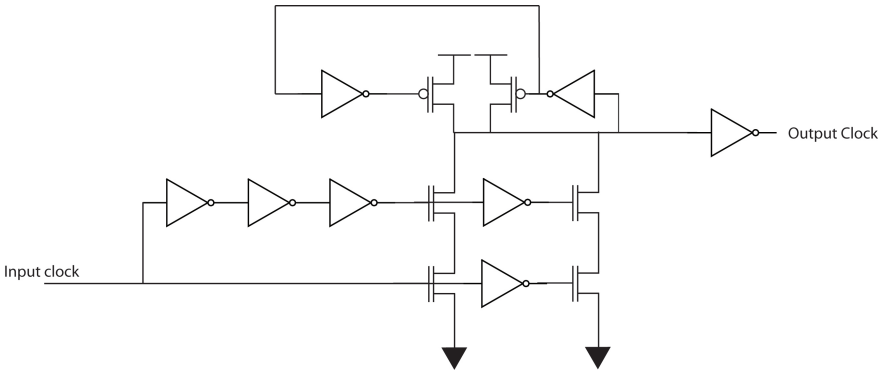

Figure 1: Question 1

(a) (7 points) How does the circuit double the clock frequqency?

(b) (8 points) Can you draw a logic-gate level version of this circuit?

(c) (10 points) Size the *original* circuit such that it can drive a 20pF load. The output clock has to have a pulse width of 180ps and the input clock frequency is 1.2GHz. Given $Req_n = 2.69k\Omega\mu m$, $Req_p = 6.51k\Omega\mu m$, $C_{dn} = 2.3fF/\mu m$, $C_{gsn} = 1.5fF/\mu m$, $C_{dp} = 2.3fF/\mu m$ and $C_{gsp} = 1.5fF/\mu m$. Make reasonable assumptions about rise and fall times.

contd...

(d) (10 points) Size your *static circuit* such that it can drive a 20pF load. The output clock has to have a pulse width of 180ps and the input clock frequency is 1.5GHz.

contd...

(e) (10 points) ***Graduate Students only:*** Calculate the power consumption for both the static and dynamic versions of the circuit.

contd...

2. Question 2: 10points

One method to save area is to employ dynamic phase 2 latches in a latch pipelined system, shown in figure 2. Answer the following questions

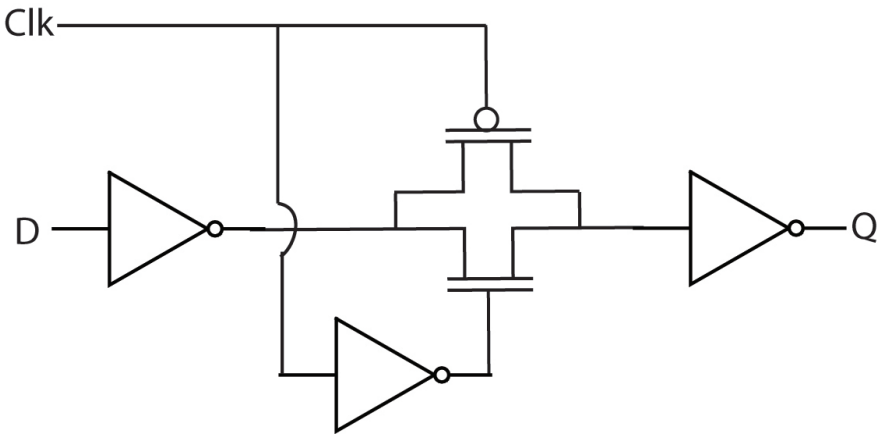

Figure 2: Question 2

(a) (5 points) Given that $V_{dd} = 1.8V$ Calculate the lowest clock frequency you can use so that the dynamic node barely discharges i.e. $< 100\mu V$ while driving a minimum sized inverter. $I_{offn} = 94pA/\mu m$, $I_{offn} = 25.2pA/\mu m$, $Req_n = 2.69k\Omega\dot{\mu}m$, $Req_p = 6.51k\Omega\dot{\mu}m$, $C_{dn} = 2.3fF/\mu m$, $C_{gsn} = 1.5fF/\mu m$, $C_{dp} = 2.3fF/\mu m$, $C_{gsp} = 1.5fF/\mu m$ and $\beta = 2.5$.

(b) (5 points) How can you ensure that the dynamic latch works at all frequencies?

3. Question 3: 45points

You are given the task to design a word-line decoder for 16K X 64 bit memory arranged as 1024 rows by 1024 bits as shown in figure 3

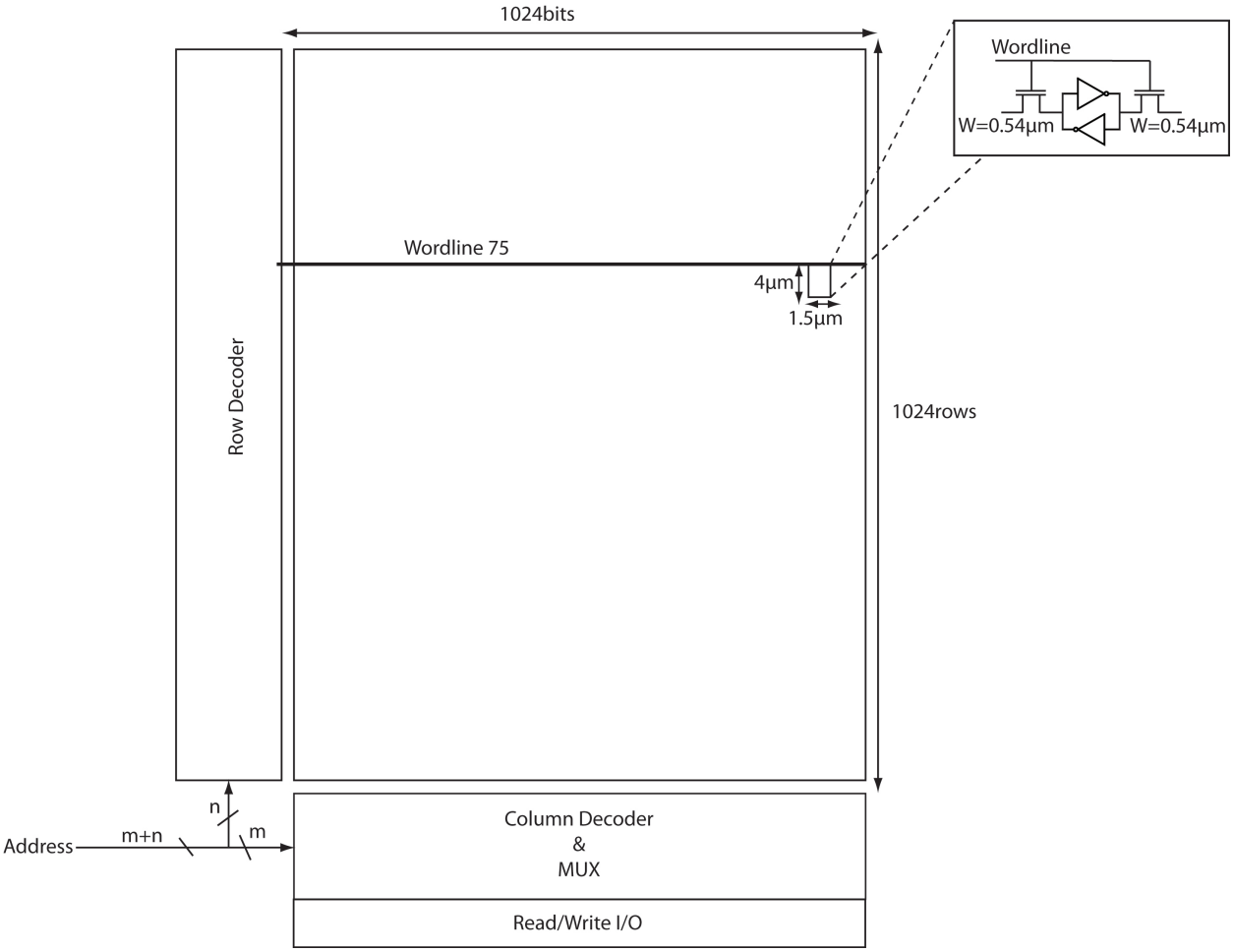

Figure 3: Circuit for Question 3

(a) (2 points) What are the values of m and n shown in figure?

(b) (3 points) Given that the wordline is routed horizontally in Metal2 with a capacitance of $0.22fF/\mu m$ and the gate capacitance is $C_{gsn} = 1.5fF/\mu m$ what is the total lumped load seen by the wordline driver?

(c) (10 points) Find the total path effort in the row address decode path assuming that the maximum load any input gate can offer is 5fF. Make sure you take the branching and logical effort into account. Assume that both *bit* and $\overline{bit}$ are available at the input.

contd...

(d) (10 points) Given that you are using static gates to implement this design and the wire resistance is $0.16\Omega/\mu m$ what is the delay from the time the clock rises and the address is presented to the decoder to the wordline going high. Given that the delay of a FO-4 inverter is 75ps and $\gamma = 1.5$, Assume that both bit and $\overline{bit}$ are available at the input.

contd...

(e) (10 points) Given that you are using domino gates to implement this design and the wire resistance is $0.16\Omega/\mu m$ what is the optimal delay from the input address to the wordline going high. Assume that both *bit* and $\overline{bit}$ are available at the input *NOTE: The input address latch is the first stage of the domino path.*

contd...

(f) (10 points) ***Graduate Students only:*** Size the precharge tree to ensure no precharge race occurs assuming a footless domino implementation.

contd...

For all problems, we are using the 0.18μm technology node. The maximum supply voltage for this technology is $V_{dd}(Max) = 1.8$ V For hand calculation you may use the following parameters

NMOS:

$$V_{tn} = 0.5V, v_{sat} = 1.6 \times 10^5 m/s, t_{ox} = 41 \times 10^{-10} m, E_{sat} = 6 \times 10^4 V/cm, C_{ox} = 8.57 fF/\mu^2, \mu = 412 cm^2/V - s$$

$$Req_n = 2.69 k\Omega/\mu m$$

PMOS:

$$V_{tp} = -0.5V, v_{sat} = 1.0 \times 10^5 m/s, t_{ox} = 41 \times 10^{-10} m, E_{sat} = 24 \times 10^4 V/cm, C_{ox} = 8.57 fF/\mu^2, \mu = 83 cm^2/V - s$$

$$Req_p = 6.51 k\Omega/\mu m$$

You may find the following equations useful

$$V_{DSsat} = \frac{(V_{GS} - V_t) E_{sat} L}{(V_{GS} - V_t) + E_{sat} L}$$

$$I_{dslin} = \mu C_{ox} \frac{W}{L} \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds}$$

$\gamma = 1.5$ for this process

For an inverter chain containing N inverters:

$$t_{pinv} = t_{po} \left(1 + \frac{f}{\gamma} \right)$$

$$F = \frac{C_L}{C_{in}}$$

$$f = \sqrt[N]{F}$$

For a logic path containing N logic gates:

$$t_{logic_gate} = t_{po} \left(p + \frac{fg}{\gamma} \right)$$

$$G = \Pi_{i=1}^{i=N} g_i$$

$$B = \Pi_{i=1}^{i=N} b_i$$

$$b_i = \frac{C_{on-path} + C_{off-path}}{C_{on-path}}$$

$$F = \Pi_{i=1}^{i=N} \frac{f_i}{b_i}$$

$$H = GBF$$

$$h = \sqrt[N]{H}$$