A Low-Voltage Fully Balanced OTA with Common Mode Feedforward and Inherent Common Mode Feedback Detector

Ahmed Nader Mohieldin Edgar Sánchez-Sinencio José Silva-Martínez

Department of Electrical Engineering, Texas A&M University, College Station, Texas 77843, USA

Abstract

A pseudo differential fully balanced CMOS OTA architecture with inherent common mode detection is proposed. Through judicious arrangement, the common-mode feedback circuit can be economically implemented. The OTA achieves a good CMRR and is suitable for low voltage operation. As an example of the applications of the proposed OTA, a 100MHz 4th order linear phase OTA-C filter is presented. The measured group delay ripple is 3%, the filter dynamic range is 45dB. It consumes 42.9mW per complex poles.

1. Introduction

In general, a fully differential structure has an improved dynamic range over its single ended counterpart. This is due to better common mode noise rejection, better distortion performance, and increased output voltage swing. One important disadvantage of fully differential structures is the need of an extra common mode feedback (CMFB) circuit. A CMFB circuit is needed for two reasons: (1) To fix the common mode voltage (V_{cm}) at different high impedance nodes. (2) to suppress the common mode signal components, on the whole band of differential operation that tends to saturate different stages.

A CMFB circuit is classically performed by means of a CMFB loop. The CMFB loop has to be designed carefully to avoid potential stability problems. This often increases the complexity of the design, the power consumption, and the silicon area used. The frequency response of the differential path is also degraded due to the added parasitic components involved in conventional CMFB schemes. In some cases and due to the system configuration, the CMFB requirements can be relaxed. For instance, if the common mode gain is sufficiently small, as would be the case of a conventional differential pair based OTA with a tail current, the CMFB bandwidth might be reduced. Its primary function will be to set the common mode voltage and it will not consume much power. Nevertheless, for good power supply rejection, a wide bandwidth CMFB is needed. In other cases, when the output is loaded by low impedance, the DC output voltage is well defined and assuming that the common mode gain is small enough, there may be no need for the CMFB circuitry as would be the case of filters built using lossy integrators [1].

In this work, a practical pseudo differential OTA is proposed. It is shown that a separate CMFB circuit can be avoided with appropriate arrangement of cascaded pseudo differential OTAs, for example in a filter. This approach takes advantage of the OTAs used for the differential mode operation to render low common mode gain without extra circuitry. The proposed OTA has inherently the common mode detector, hence the CMFB is economically realized.

2. Proposed OTA architecture

In general operational transconductance amplifiers can be divided into two main groups: Fully Differential (FD) and Pseudo Differential (PD). FD is based on a differential pair with tail current source and PD is based on two independent inverters without tail current source. Avoiding the voltage drop across the tail current source, in a PD structure, allows achieving wider linear input range and makes the architecture attractive for low voltage applications. Removing the tail current source, however, results in a poor rejection to common mode noise. Using a common mode feedforward (CMFF) technique, A_{CM} at low frequency is in the order of unity [2]. A separate transconductance is often used for common mode detection [3]. This approach adds more load to the driving stage due to the connection of two input transistors, one for the differential transconductance and the other one for the common mode transconductance, thus doubling the input capacitance. The CMFF improves the rejection to common mode signals but it is incapable to fix the DC common mode output voltage.

Figure 1 shows the circuit implementation of the proposed OTA. It can be described as a conventional three current mirror single ended OTA, without the tail current, plus the additional branches (dashed lines). Thus the OTA becomes fully balanced [4] and fully symmetric with enhanced features to be described.

2.1 Inherent common mode detection

It can be shown, using the quadratic I-V characteristics of a transistor (neglecting all short channel effects), that current (I_1+ I_2) in Figure 1 provides the information about the common mode level of the inputs as follows:

$$I_1 + I_2 = 2.\frac{K_P}{2}\left(\frac{W}{L}\right)_1\left[\left(V_{dd} - V_{icm} - |V_{TP}|\right)^2 + \frac{v_d^2}{4}\right] \qquad (1)$$

where $V_i^+ = V_{icm} + v_d/2$, and $V_i^- = V_{icm} - v_d/2$.

Note that after extracting the common mode information, the common mode current $(I_1+ I_2)/2$ is subtracted at the output nodes of the OTA, yielding (for $M_4=BM_2$):

$$I_{01} = \frac{I_2 - I_1}{2} = B\frac{K_P}{2}\left(\frac{W}{L}\right)_1\left[V_{dd} - V_{icm} - |V_{TP}|\right]v_d \quad (2)$$

$$I_{od} = I_{01} - I_{02} = B\frac{K_P}{2}\left(\frac{W}{L}\right)_1\left[V_{dd} - V_{icm} - |V_{TP}|\right]v_d = G_m v_d \quad (3)$$

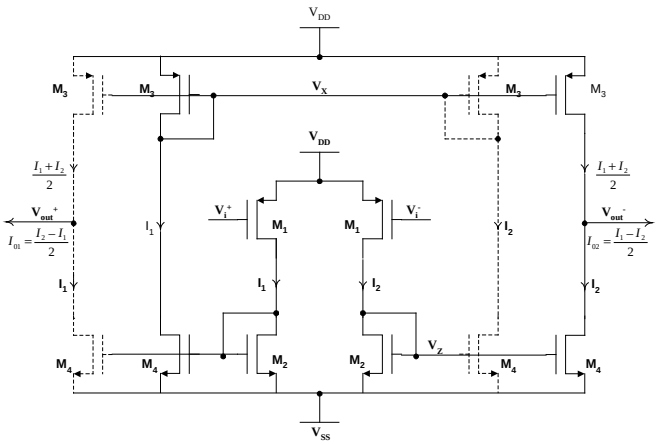

Figure 1. Proposed OTA architecure

2.2 CMFB and CMFF arrangements

Although the CMFF provides rejection to the common mode components at the output, we still need to fix the DC common mode output voltage. In the proposed OTA architecture, CMFB can be implemented by judiciously connecting at least two of the proposed OTAs. This can be achieved by adding the four transistors $M_3'=M_3$ and $M_4'=M_4$, as shown in Figure 2. The signal common mode components are suppressed by the action of the CMFF. The DC level of the output is sensed at node V_X of the next OTA, and fedback by M_3'; i_{d3}' is then compared with the proper current i_{d4}' fixing the DC output level to the required value. This arrangement has the advantage that the differential mode signals and the common mode signals share basically the same loop, and the transconductance of the CMFB loop is the same as the differential mode transconductance.

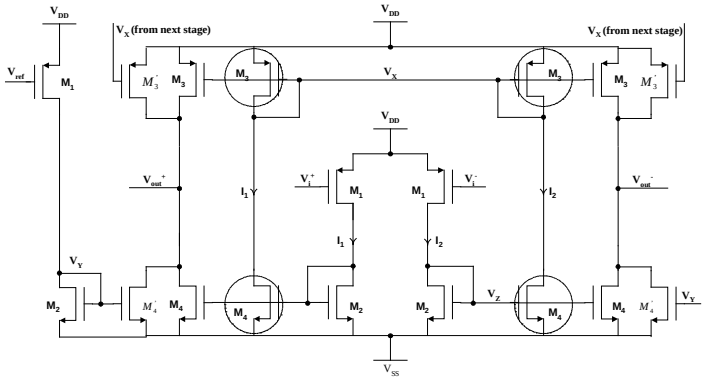

Figure 2. OTA with CMFF and CMFB ($M_4=BM_2$)

2.3 Frequency response and excess phase

The differential mode transconductance of the proposed OTA, for $M_4=M_2$, can be written as:

$$g_m(s) = \frac{i_{od}}{v_d} = g_{m1}\frac{g_{m2}}{g_{m2} + sC_Z} = \frac{g_{m1}}{1 + s/\omega_{nd1}} \quad (4)$$

where C_Z is the total parasitic capacitance at node V_Z. Thus the excess phase $\Delta\phi$ is given by:

$$\Delta\phi = -\tan^{-1}\left(\frac{\omega}{\omega_{nd1}}\right) \quad (5)$$

Note that C_Z as well as g_{m2} are functions of W_2 , thus (5) involves an iterative design procedure. L_2 can be chosen to be minimum to reduce the excess phase although it will sacrifice the DC gain.

2.4 Linearity issues

Note from (3) that the linearization of the output current depends on the cancellation of the quadratic components of the individual currents I_1 and I_2. Due to transistor mismatches, this cancellation is not perfect and some second order distortion will result. Even order harmonics can also appear, even neglecting all mismatches, due to the cross product of differential and common mode signals. Thus, the common mode signal has to be suppressed as much as possible [3].

The main nonlinearity contribution for the proposed OTA structure is due to short channel effects. For short channel devices, the effective carrier mobility (μ_{eff}) is no longer constant and is a function of both the longitudinal and transversal electric fields. Considering the degradation of mobility due to these effects and the channel length modulation effect, the drain current I of a transistor in saturation region is given by:

$$I = \frac{K_P}{2}\left(\frac{W}{L}\right)\frac{\left(V_{SG} - |V_{TP}|\right)^2}{1 + \theta\left(V_{SG} - |V_{TP}|\right)}\left[1 + \lambda V_{SD}\right] \quad (6)$$

where $K_P=\mu_{eff}C_{ox}$, $\mu_{eff}=\mu_0/(1+E/E_C)$, $E_C=v_{sat}/\mu_0$, and $\theta=1/LE_C$. L is the device electrical channel length, C_{ox} is the oxide capacitance per unit channel area, λ is the output impedance constant, μ_0 is the low-field mobility, v_{sat} is the saturation carrier drift velocity, E is the longitudinal electric field, and E_C is the critical electric field. Note that the value of θ in (6) must be modified to include the effect of the transversal electric field. The value of θ and λ have been determined for the used technology by a best fit to the simulated device characteristics, with minimum length L, to be $0.4V^{-1}$ and $0.1V^{-1}$, respectively. If a differential signal is applied, then:

$$V_{SG}-|V_{TP}|=V_{ov}+(v_d/2) \quad (7)$$

$$V_{SD}=V_{DC}-k(v_d/2) \quad (8)$$

where $V_{ov}=V_{dd}-V_{icm}-|V_{TP}|$ is the overdrive voltage, and k is the gain from the input to node V_z (see Figure 2).

Substituting (7) and (8) in (6), we have:

$$I = \frac{K_P}{2}\left(\frac{W}{L}\right)\frac{1 + \lambda V_{DC}}{1 + \theta V_{ov}}\frac{\left(V_{ov}^2 + v_d/2\right)^2}{1 + \beta(v_d/2)}\left[1 - \alpha\frac{v_d}{2}\right] \quad (9)$$

where $\beta=\theta/(1+\theta V_{ov})$, and $\alpha=k\lambda/(1+\lambda V_{DC})$.

Using taylor series expansion, with $V_d=V_{Peak}\cos(\omega t)$, yields:

$$HD_3 \cong \left| \frac{(\beta+\alpha)\left(2\beta-\beta^2 V_{ov}-\frac{1}{V_{ov}}\right)}{32\left(1-\frac{\beta+\alpha}{2}V_{ov}\right)} \right| V_{Peak}^2 \quad (10)$$

Neglecting channel length modulation effect (for k=1, $\lambda<\theta$, and $V_{DC}>V_{ov}$) and substitute the value of β in (10), yields:

$$HD_3 \cong \frac{\theta.V_{Peak}^2}{16V_{ov}(1+\theta V_{ov})^2(2+\theta V_{ov})} = \frac{\theta.V_{in\_rms}^2}{8V_{ov}(1+\theta V_{ov})^2(2+\theta V_{ov})} \quad (11)$$

A direct tradeoff between linearity and frequency response (excess phase) is observed from (11). The smaller θ is, the wider the linear range for a given HD_3. This can be accomplished by increasing the length of the channel ($\theta \ \alpha \ 1/L$) which at the same time increases the parasitic capacitances. Increasing V_{ov} also improves the linearity at the expense of power consumption.

2.5 Noise performance

The encircled transistors in Figure 2 contribute to common mode noise only due to the symmetric configuration and thus their effect can be neglected.

Consider only the integrated thermal noise power, where $V^2_n=(8KT.BW/3g_m)$, the input referred noise becomes:

$$V_{n\_rms}^2 = \frac{16KT}{3g_{m1}}.BW.\left[1+\frac{g_{m2}}{g_{m1}}+\frac{2g_{m3}}{g_{m1}B^2}+\frac{2g_{m4}}{g_{m1}B^2}\right] \quad (12)$$

where BW is the equivalent noise bandwidth.

Increasing B will reduce the noise, increase the effective transconductance and consequently g_{CMFB}, but it directly deteriorates the excess phase as C_Z increases. The accuracy of the current mirror is also less for large values of B. In this design B is chosen to be unity to maintain the ability for high frequency operation. Increasing g_{m1} will also reduce the noise, the payment is in the power consumption in this case. Using (11) and (12), the following expression for the SNR can be obtained:

$$SNR = 10\log\left[\frac{V_{in\_rms}^2}{V_{n\_rms}^2}\right] \cong 10\log\left[\frac{3.HD_3.V_{ov}(1+\theta V_{ov})(2+\theta V_{ov}).g_{m1}}{2.BW.KT.\theta\left(1+\frac{g_{m2}+2g_{m3}+2g_{m4}}{g_{m1}}\right)}\right] \quad (13)$$

For a given HD_3, the maximum input voltage, and consequently the SNR, can increased by increasing V_{OV}. The transconductance g_{m1} needs also to be maximized to reduce the noise contribution of subsequent transistors.

3. CMFB loop design considerations

The open loop gain of the CMFB, for $M_4=M_2$, is given by:

$$A_{CMFB}(s) = \frac{g_{m1}}{g_{m2}+sC_Z}.\frac{g_{m2}}{g_{m3}+sC_X}.\frac{g_{m3}}{g_o+sC_L} = \frac{G_{CMFB}(s)}{g_o+sC_L} \quad (14)$$

where C_X and C_Z is the total parasitic capacitance at node V_X and node V_Z respectively, C_L is the load capacitance, g_0 is the output conductance. A_{CMFB} should be made as high as possible at DC, and its bandwidth should be as high as the differential mode bandwidth. The CMFB loop is compensated for stability purposes by the load capacitance C_L, which is also used for differential mode operation.

The CMFB is idealy transparent to differential signals and acts at low frequencies as a resistor of value $1/g_{CMFB}$ ($g_{CMFB}=g_{m1}$ is the small signal CMFB transconductance) for common mode signals. Thus for $M_4=M_2$, the common mode gain, A_{CM}, is computed as:

$$A_{CM}(s) = \frac{g_{m1}.g_{m2}(g_0+sC_X)}{(g_{m2}+sC_Z)(g_{m3}+sC_X)[(G_{CMFB}(s)+g_0+sC_L)]} \quad (15)$$

Note that A_{CM}, at low frequency, is much less than unity; this is a result of the action of both CMFB and CMFF circuits.

4. Filter architecture

A fourth order linear phase Bessel-Thompson OTA-C filter has been implemented. The requirement is a group delay error less than 3% for frequencies up to $1.5xf_0$, where f_0=50MHz and $f_{-3dB}=2.1xf_0$. The block diagram of the filter with the required CMFB arrangement is shown in Figure 3.

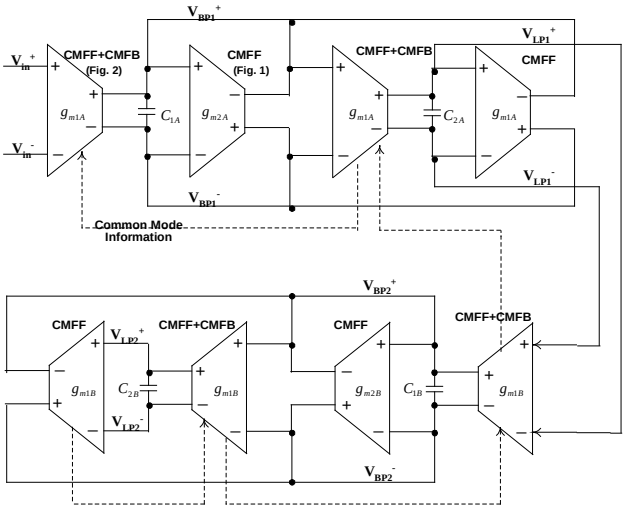

Figure 3. Filter architecture

Note that the flow of the common mode information from one stage to the other is done in a natural way. The common mode level is sensed only once per output. Similarly, the output common mode level needs to be fixed only once for any number of OTAs sharing the same output. Thus, some of the fully fledged OTAs (with CMFB and CMFF) may be replaced by ones with CMFF only as that shown in Figure 1. For instance, g_{m2A}, g_{m2B}, the last stage of the first biquad, and the last stage of the second biquad do not need to have a CMFB since their outputs are common with other OTAs which will automatically fix the output DC level of the output.

5. Measurement results

The filter has been fabricated in AMI 0.5μm CMOS process. The chip micrograph is shown in Figure 4. It

occupies a small area of 450x350 μm^2. The transconductance, and consequently the –3dB frequency of the filter, can be tuned by changing V_{icm}. This is achieved by changing the CMFB reference voltage V_{ref} (see Figure 2). Figure 5 shows the measured phase response of the filter. The group delay is shown in Figure 6. The measured group delay ripple is about 3% for frequencies up to 100 MHz. Figure 7 shows the filter output spectrum for a differential input signal of amplitude 350 mV_{pp} and frequency 30 MHz. The total in-band integrated output noise is about 700 μV_{rms}. This corresponds to 45 dB of dynamic range (DR) for 0.5% THD at 30 MHz. The measured CMRR, $PSRR^+$, and $PSRR^-$ at 10MHz is 45 dB, 26 dB, and 35 dB, respectively, and is 32 dB, 21 dB, and 28 dB, respectively, at 50MHz. The filter consumes 26 mA from a ±1.65 V power supply. Table 1 contains a summary of different filter performance parameters compared with previously reported works in [5] and [6].

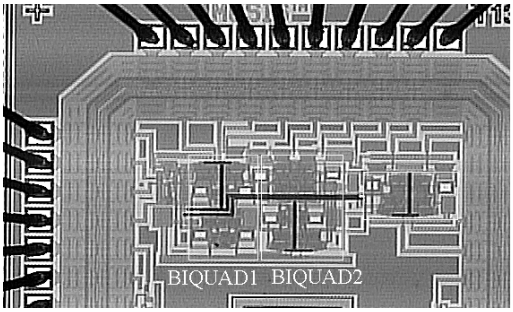

Figure 4. Chip micrograph

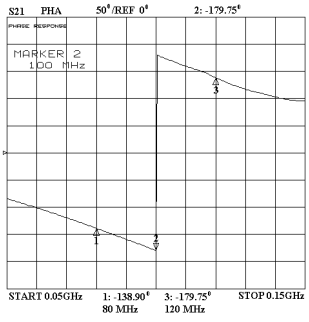

Figure 5. Phase response

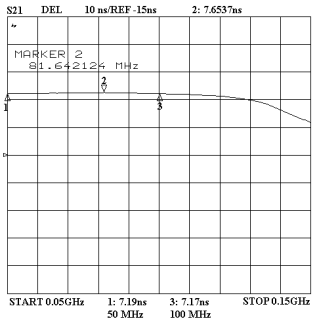

Figure 6. Group delay

6. Conclusions

A pseudo differential fully symmetric fully balanced OTA architecture has been presented. The proposed OTA features very attractive linearity properties and inherent common mode detection. It has been demonstrated that the structure made it easy to incorporate the CMFB arrangement. This is done at minimum cost of area and power consumption. The same principle can be applied to any OTA with CMFF to incorporate the detection of the common mode information of the previous stage for CMFB stabilization. A 100 MHz 4^{th} order linear phase OTA-C filter has been implemented in 0.5μm CMOS process and occupies an area of $0.16mm^2$ only. The group delay ripple is 3% for frequencies up to the –3dB frequency. Measured results assured the good performance of the proposed transconductance building block and its suitability for high frequency and low voltage operation.

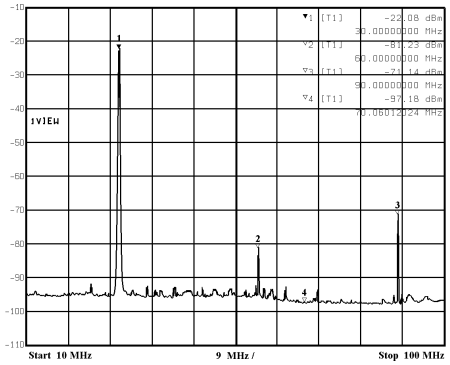

Figure 7. Spectrum for a 350mV_{pp} 30 MHz input signal

Table 1. Filter Performance Parameters

	[5]	[6]*	This Work
Filter type and order	7^{th} Order 0.05^0 Equirriple	7^{th} Order 0.05^0 Equirriple	4^{th} Order Bessel
$f_{-3\,dB}$	50 MHz	100 MHz	100 MHz
Ripple on group delay	< 2% @ $f < 1.5f_{-3dB}$	< 5% @ $f < 2f_{-3dB}$	< 3% @ $f < f_{-3dB}$
Max Input	200 mV_{p-p}	100 mV_{p-p}	350 mV_{p-p}
THD	-46 dB	-46 dB	-46 dB
Output noise	1.7 mV_{rms}	N/A	700 μV_{rms}
DR	32 dB	> 40 dB	45 dB
Power supply	3 V	3 V	3.3 V
Current drain	27 mA	40 mA	26 mA
Technology	0.72μm CMOS	0.29μm BiCMOS	0.5μm CMOS

* Include filter boost

References

[1] A. Wyszyński and R. Schaumann, "Avoiding common mode feedback in continuous-time Gm-C filters by use of lossy integrators," *IEEE International Symposium on Circuits and Systems*, vol. 5, pp.281-284, 1994.

[2] W. M. Snelgrove and A. Shoval, "A balanced 0.9 μm CMOS transconductance-C filter tunable over the VHF range," *IEEE J. Solid-State Circuits*, vol. 27, no. 30, pp.314-323, March 1992.

[3] F. Rezzi, A. Baschirotto, and R. Castello, "A 3V 12-55 MHz BiCMOS pseudo differential continuous-time filter," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp.896-903, November 1995.

[4] T. Itakura, T. Ueno, H. Tanimoto, and T. Arai, "A 2 V_{p-p} linear input range fully balanced CMOS transconductor and its application to a 2.5V 2.5MHz G_m-C LPF," *IEEE Custom Integrated Circuits*, pp.509-512, 1999.

[5] W. Dehaene, M.S.J. Steyaert, and W. Sansen, "A 50 MHz standard CMOS pulse equalizer for hard disk read channels," *IEEE J. Solid-State Circuits*, vol. 32, no. 7, pp.977-988, July 1997.

[6] N. Rao, V. Balan, and R. Contreras, "A 3V 10-100MHz continuous-time seventh order 0.05^0 equiripple linear phase filter," *IEEE J. Solid-State Circuits*, vol. 34, no. 11, pp.1676-1682, Nov. 1999.