

Exam
Digital Design and Microprocessors, ET1123
School of Computing
Blekinge Institute of Technology

Wednesday 2nd of June 2010, 9.00 – 14.00

Examiner:	Jan Carlsson
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Nr of questions:	8
Maximum score:	30
Enclosed:	Appendix “Theory from textbook, chapters 2-4” (Erik Loxbo) Appendix “The algebraic structure of finite automata’s” (Jan C) P1 Datasheet + ASCII table (Anders Nelsson)
Allowed to bring:	Textbook: “Logic and Computer Design Fundamentals”, Mano & Kime English dictionary Calculator
Grading: (Swedish)	Grade 3 requires at least 12 points Grade 4 requires at least 18 points Grade 5 requires at least 24 points
(ECTS)	Grade E requires at least 12 points Grade D requires at least 15 points Grade C requires at least 18 points Grade B requires at least 22 points Grade A requires at least 26 points

IMPORTANT:

- Write your name on every submitted paper sheet
- Write legibly
- Your solutions should be so detailed that your way of thinking is visible
- Answers only will not be enough
- Mark the questions you have finished on first page
- If any condition is missing in the question, make a plausible assumption
- The questions are not arranged by degree of difficulty
- In the design problems components of your choice may be used if not otherwise suggested

GOOD LUCK!

EXAM IN ET1123, PART A

A1.

The boolean function F is given in the following truth table:

A	B	C	F	G
0	0	0	1	1
0	0	1	0	0
0	1	0	0	x
0	1	1	0	x
1	0	0	1	1
1	0	1	1	1
1	1	0	0	0
1	1	1	1	1

- Express $F(A,B,C)$ in sum - of - minterms algebraic form
- Optimize $F(A,B,C)$ by means of a three variable map
- The function G is given by the truth table above where x indicates don't care conditions. Optimize $G(A,B,C)$ by means of a three variable map

(3p)

A2.

We have the two numbers $A = +95_{10}$ and $B = +53_{10}$ and we want to perform binary addition and subtraction in a processor where the wordlength is 8 bits. The first bit in the word is a sign-bit. Perform the following operations using 2's complement for negative numbers.

- Perform $A+B$
- Perform $A-B$
- Perform $B-A$

Indicate for each one of the three cases if the result is correct or if the result causes overflow
(3p)

A3.

Design a combinational circuit that compares two positive 2-bit binary numbers A and B to see whether $A \neq B$. (A is not equal to B) $A = A_1 A_0$ $B = B_1 B_0$

Inputs: $A_1 A_0 B_1 B_0$ Output: $F(A_1 A_0 B_1 B_0)$

Specification: $F=1$ if $A \neq B$

- Write a truth table for $F(A_1 A_0 B_1 B_0)$
- Write a K-map for F and minimize F
- Implement the circuit as a minimal AND-OR net.

(4p)

EXAM IN ET1123, PART B

B1.

(7p)

Construct a block accepter for a block consisting of 3 bits.

If, and only if, the incoming bits are "101" shall the output-signal ' $u = 1$ ', in all other cases shall the output-signal have the value ' $u = 0$ '.

The problem shall be solved by a state minimal Moore machine.

You shall take into consideration suitable methods that may result in a state assignment that result in Boolean expressions that are uncomplicated.

You shall minimize these Boolean functions.

B2.

(3p)

A very simple model of a cache memory, that is supposed to illustrate the function of a cache replacement algorithm, can only store 3 blocks in the cache memory.

For a certain test program, the CPU needs to access the following blocks:

1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.	12.
2	3	2	5	1	2	3	4	2	5	2	1

The second line in the table describe the blocks that the CPU needs to have access to, and the first line describe in what order the CPU need those blocks.

If this model-system is using LRU, least resent used, as its replacement algorithm, what will the content of the cache-model be, after the test-program has been executed?

The cache model can be described by this table:

1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.	12.

What is the hit-ratio, **H**, in this case?

If the access time for the cache-memory in this case is $t_{cache} = 2 \text{ ns}$, and the access time for the RAM memory is $t_{RAM} = 10 \text{ ns}$.

What is the total memory access time t_{tot} for this model system?

EXAM IN ET1123, PART C

C1.

The assembly code below belongs to the example processor P1.

```
init:      LDI      R2, 01h
           LDI      R3, F0h
start:     LD       R0, 81h
           AND      R2, R2
           JPZ      xyz
           LD       R0, 82h
           AND      R0, R3
           JMP      wzp
xyz:       LD       R0, 82h
           OR       R0, R3
wzp:       ST       82h, R0
           JMP      start
```

- a) Draw a flow chart diagram showing the functionality of the program. (2.5p)
- b) Describe in words what program actually is doing. (1.5p)

C2.

Give the short answers to the problems below (ONLY 2-3 sentences or a small calculation).

- a) Describe Direct Addressing Mode (in Assembler) (0.5p)
- b) Describe Indirect Addressing Mode (in Assembler) (0.5p)
- c) What are the op-codes of these three instructions in example processor P1? (0.5p)
LDI R2, FEh
ADD R3, R2
ST 82h, R3
- d) What characterizes the memory organization of a von Neuman processor? (0.5p)
- e) Assume that you have a memory of 128 Kbit. What is the minimum width of the address bus if the data bus width is 8 bits? What is the minimum address bus width if data bus width is changed to 16 bits? (0.5p)
- f) Describe the purpose of the Carry-flag in a processor. (0.5p)
- g) Describe the purpose of the PC in a processor. (0.5p)
- h) Describe the purpose of the Stack Pointer in a processor. (0.5p)

C3.

- a) Convert the binary number 11111011010b to hexadecimal and decimal values. (0.5p)
- b) Convert the hexadecimal number ACEh to binary and decimal values. (0.5p)
- c) Convert the decimal number 555d to hexadecimal and binary values. (0.5p)
- d) What is the corresponding ASCII-character (7-bit) of 52h and 0100011b?
What is the binary representation of the ASCII-characters 'g' and '='? (0.5p)