

**The schematic and the simulation results are for an analog electronic load circuit. The circuit steps through 1mA to 10mA and then starts the cycle again.**

The full circuit has a manual current sink (via a trimpot) and three stepped current sinks (1mA – 10mA, 10mA – 100mA, 100mA – 1A). This problem only relates to the 10mA and 100mA sections.

- The reference voltage is 2V.  $2V/10 \text{ steps} = 200mV$  per 1mA/10mA/100mA step.
  - The clock signal is 10 ms per step (~3 ms high and ~7 ms low), there are ten steps and then the cascaded counters reset and restart the cycle.
  - The 0.1A to 1A section is correctly functional. The first step is 100mA on the current sink ammeter, which it should be.
  - The 1mA to 10mA and the 10mA to 100mA sections have a glitch on the first step: step 1 is 300uA (or 3mA, respectively) but it should be 1mA (or 10mA).
- 

The first schematic is the actual schematic. The second schematic here is a (horrible but functional) version showing the signal and power paths when step 1 is high.

In principle I do not think the clock signals are of importance to the problem glitch. I feel the glitch is perhaps more likely related to the NMOS turning off too slowly or something along those lines; perhaps the drop from 2V to 200mV is an unrealistic expectation of the op amp and that clock design will never give it time to settle after 2V and then rise to 200mV – I have tried a load of different things to pull the NMOS drive op amp inputs to 0V or shorting them together (as in a half-done and unlikely to work chopper/AZA) so as to add step 11 and have a 0V deadtime moment between e.g. 10mA and 1mA.

As can be seen from all the shunt ammeter waveforms, 1A is correct at step 1, the other two are incorrect at step 1. The reference voltages are correct throughout the cycle, so they may not be the problem.

---

## **Pictures:**

Page 3) electronic load version 1 e schematic

Page 4) electronic load version 1 e signal path schematic (It may look like a horrible mess but I tried to make it as intuitive and quick to understand as possible.)

Page 5) 1.000A current sink ammeter (2r shunt) waveform

Page 6) 1.000A current sink reference voltages waveforms

Page 7) 0.100A current sink ammeter (20r shunt) waveform

Page 8) 0.100A current sink reference voltages waveforms

Page 9) 0.010A current sink ammeter (20r shunt) waveform

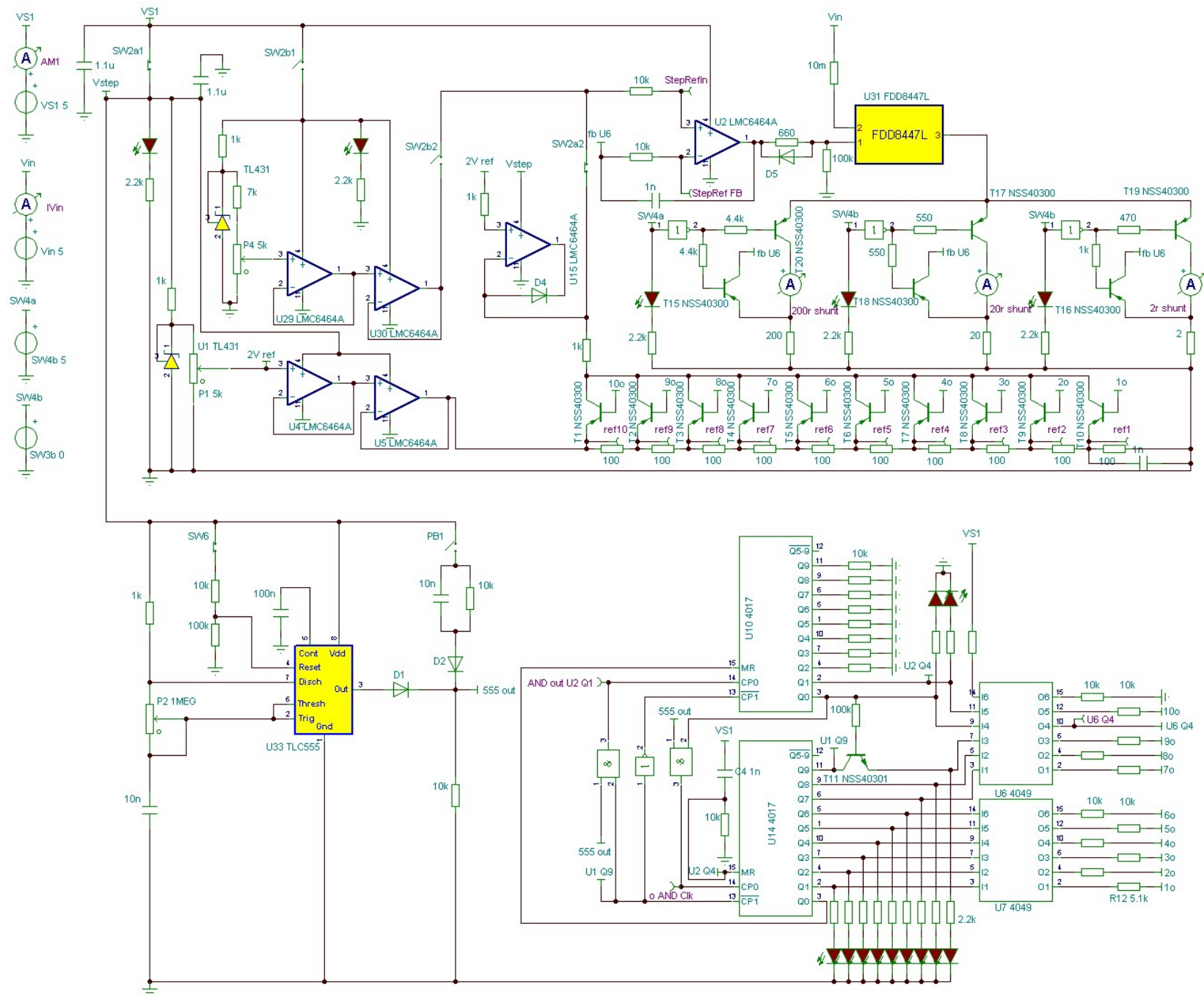
Page 10) 0.010A current sink reference voltages waveforms

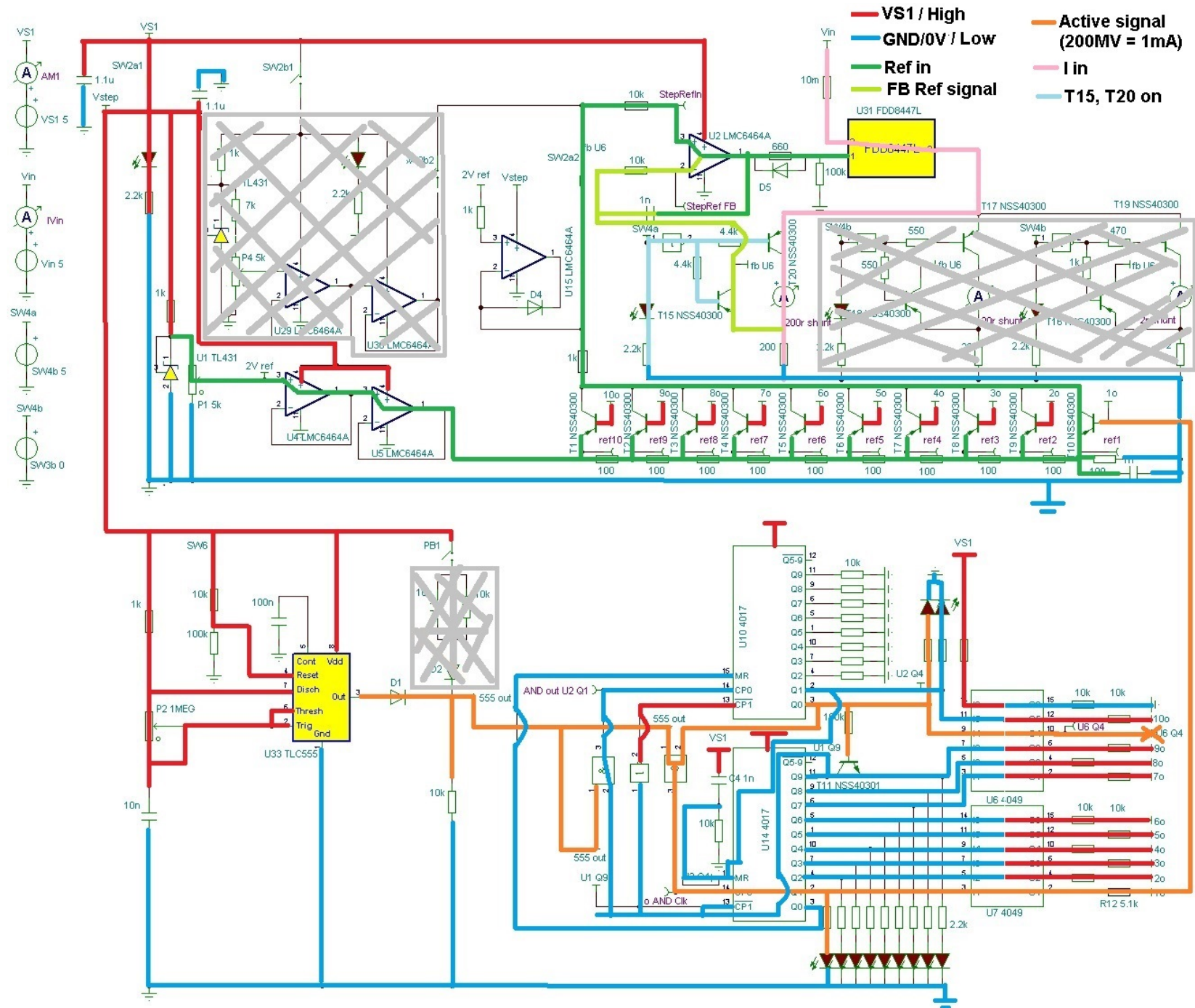
Page 11) clock signals/cascaded CD4017 signals

On the simulation results that include reference voltages:

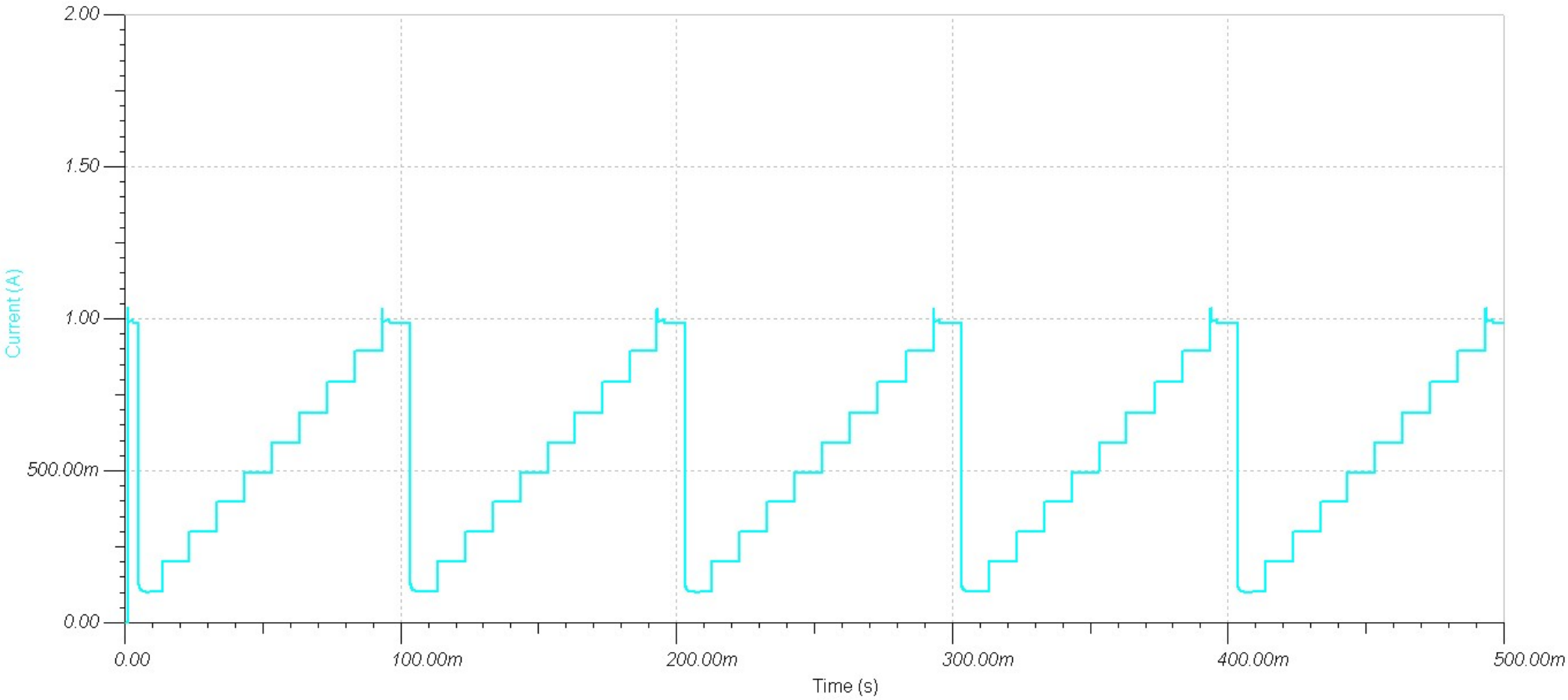
The horizontal lines are the 200mV, 400mV, etc. to 2V reference voltages on the PNP/100R junctions. The (pink) steps are the voltage steps and feedback signals seen at the U2 op amp input(s).

N.B. The current and voltage waveform ammeter diagrams read 1R, 10R, 100R – those are actually 2R, 20R, 200R – the schematic values are true/real (i.e. I'm not simulating one thing and then showing another in the schematic).

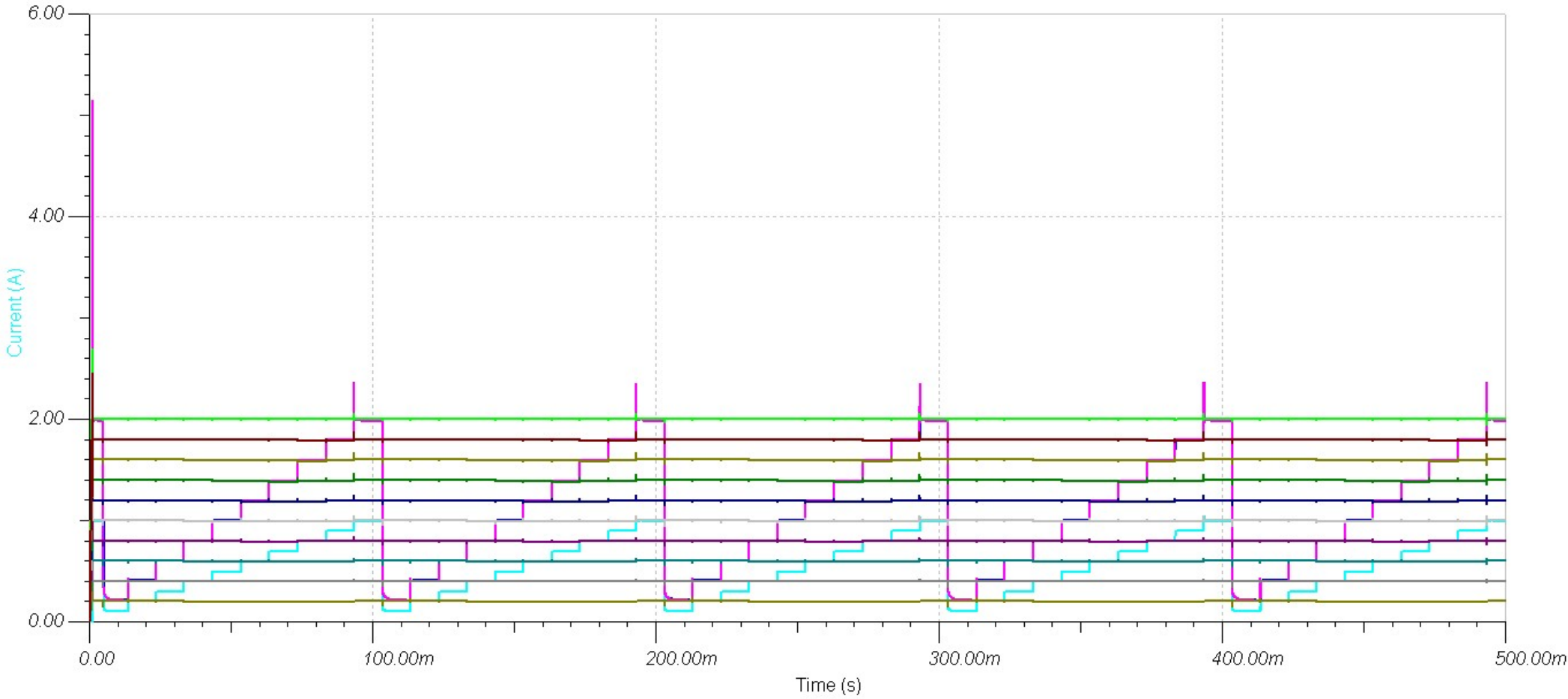




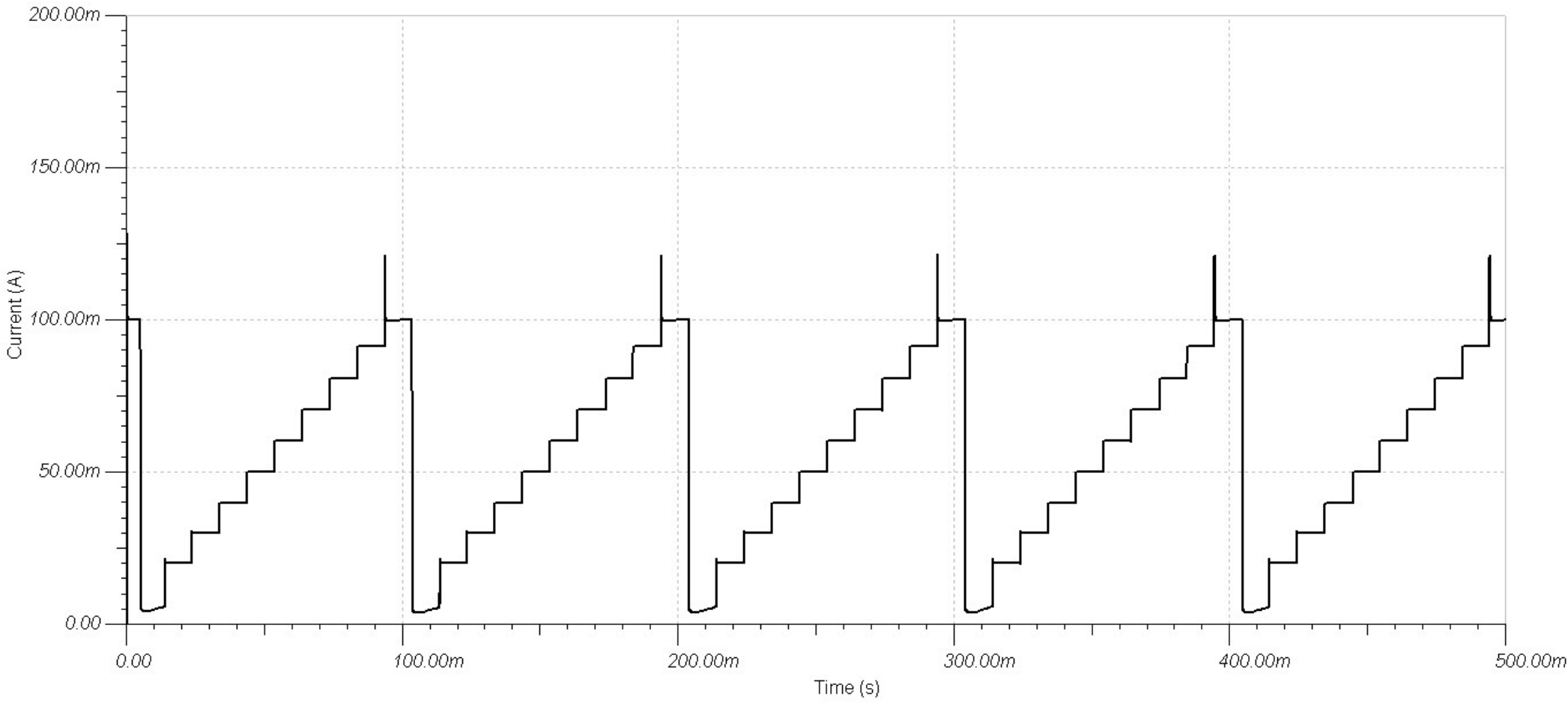
1A/2R ammeter waveforms:



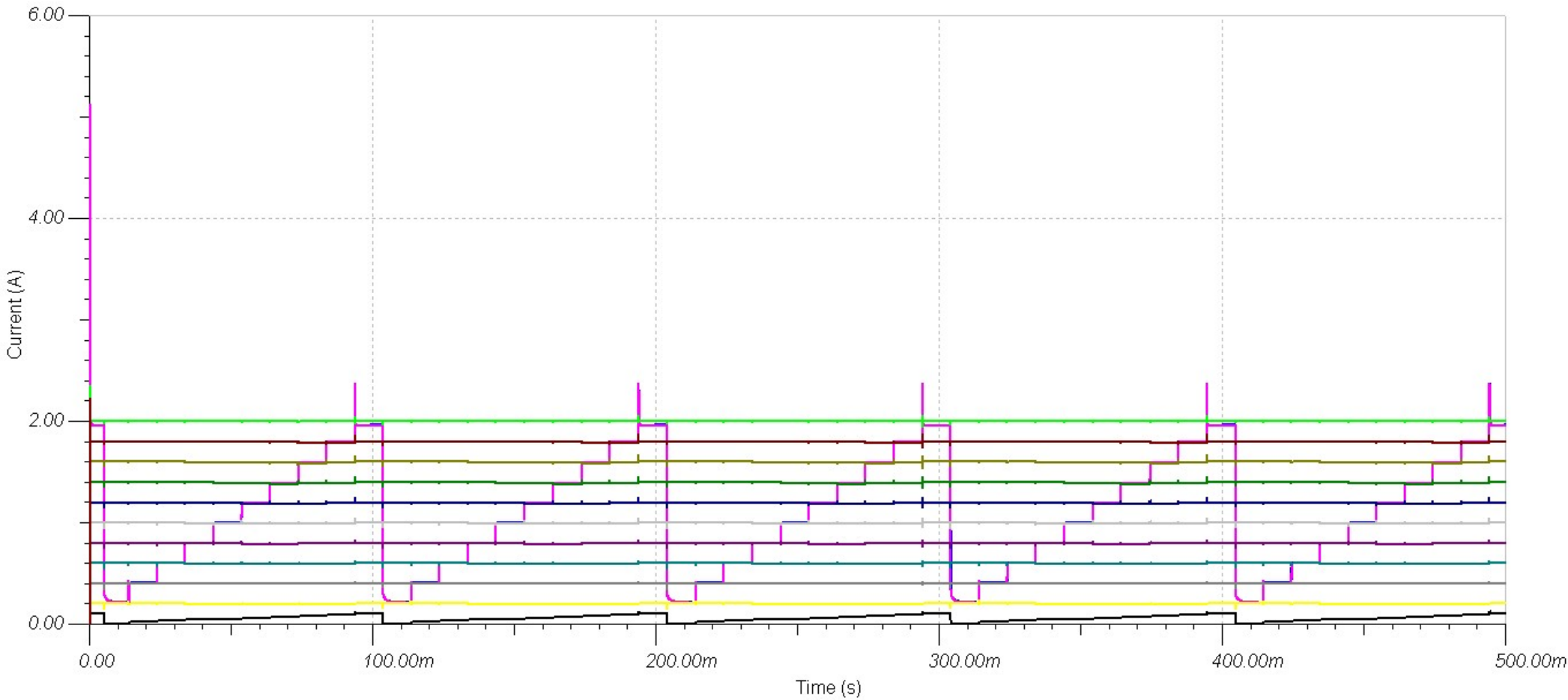
1A/2R reference voltage waveforms:



0.1A/20R ammeter waveforms:

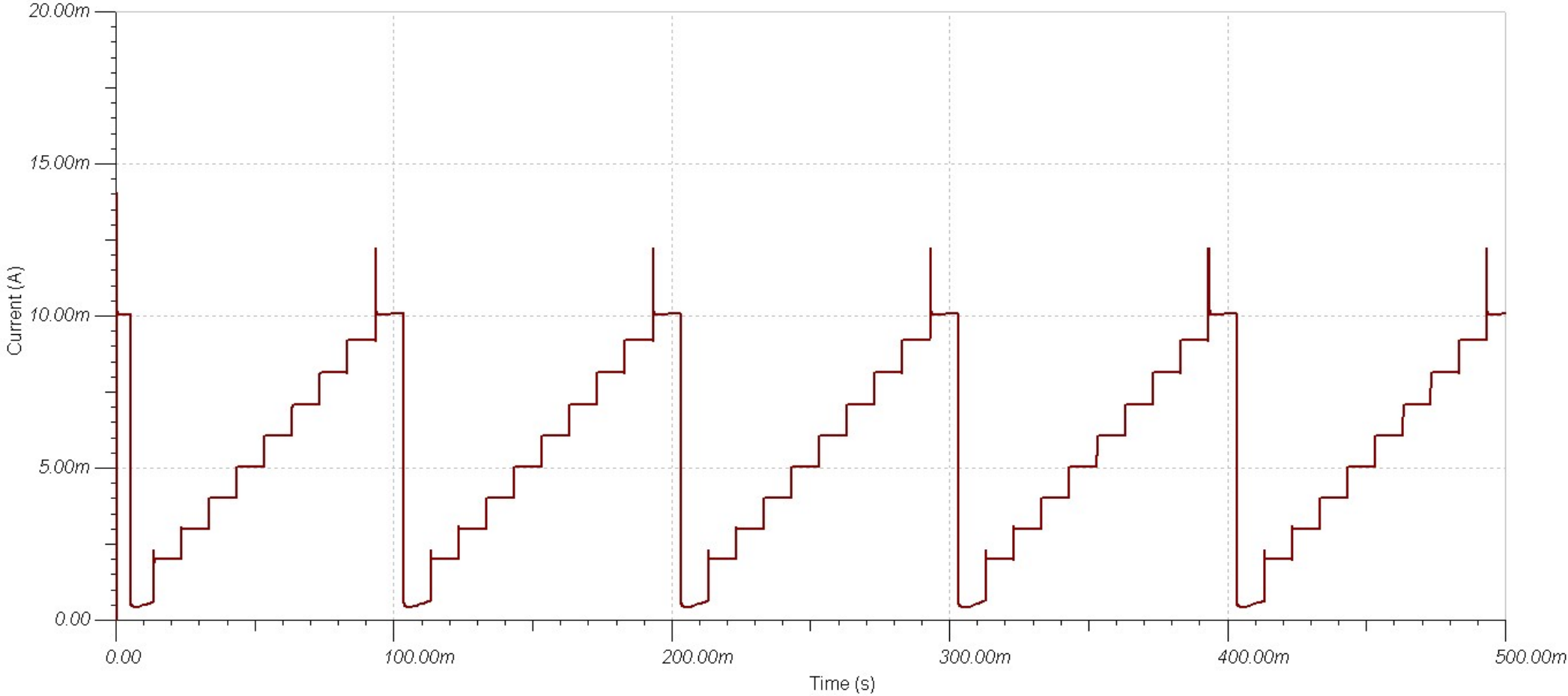


0.1A/20R reference voltage waveforms:

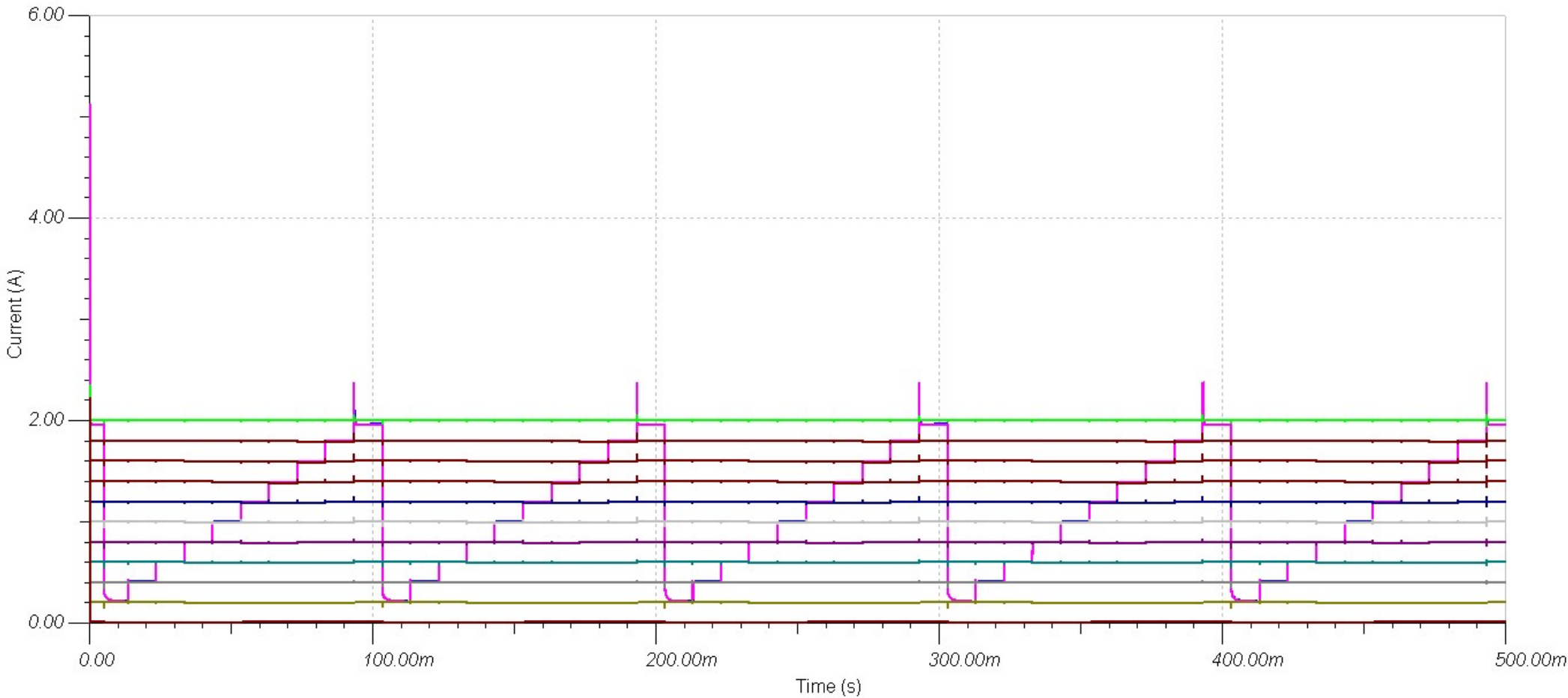




0.01A/200R ammeter waveforms:



0.01A/200R reference voltage waveforms:



Clock signals (/cascaded 4017 waveforms):

