



DESIGN OF LNA+MIXER FOR MULTI-BAND WCDMA

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Abstract

A small, low-cost, single-chip multi-band WCDMA/GSM transceiver solution is needed to address the high growth segment of 3G enabled smart phone ICs, while still keeping compatibility with widely deployed 2G GSM networks. In this thesis, an inductor-less LNA+mixer combination for multi-band WCDMA is presented. By designing the mixer for high IIP2, the inter-stage saw filter between LNA and mixer, as is normally used in WCDMA receiver designs has been eliminated, resulting in substantial cost reduction. Although mainly intended for WCDMA, the LNA+mixer combination also meets the requirements for GSM.

For the LNA design, a noise cancelation topology has been used to achieve wide-band input matching, while still providing the required low noise figure. For this configuration, tradeoffs between noise, linearity and power consumption are explored in detail. Several modifications over basic noise cancelation topology are presented, which result in a significant reduction in noise figure.

A passive mixer topology with a switching core followed by transimpedance amplifier (TIA) has been used for the mixer design. To reduce the noise contribution of the TIA, a new approach, which makes use of a current buffer between the switching core and the TIA is presented. This current buffer also allows the use of higher gate lengths and widths for the switching core transistors, which is beneficial in meeting the high IIP2 required to eliminate the inter-stage saw filter. The design of the transimpedance amplifier is also explained in detail.

The LNA+mixer combination presented in this thesis achieves a worst case total gain of 35.5dB and noise figure of 2.9dB across all WCDMA bands. S_{11} is below -15dB from 870MHz to 2.17GHz. The IIP2 at transmit frequency offset is greater than 50dBm across all WCDMA bands. Across all these bands, the worst case IIP3 at transmit frequency offset is -8.2dBm and input referred 1dB cross compression point is -20dBm. The combination of LNA and I/Q mixer consumes 25mA from 1.2V supply. The design has been carried out using IBM 65nm CMOS process technology.

Key words: multi-band, WCDMA, LNA, mixer, noise cancelation, IIP2

Preface

Completion of this project and this thesis has been an incredible one year long journey. Not only has the destination reached in this journey been very satisfactory, but the journey itself has been one filled with unforgettable memories and many learning opportunities. Along with significantly increasing my knowledge, this project has instilled in me a great deal of patience by giving me the opportunity to face and overcome many challenges.

Undoubtedly, all this would not have been possible without the support of a great number of people, of whom, I will be able to mention only a few here. First of all, I am grateful to Mr. Philippe Barré, Design Manager and Principle Engineer, Cellular Division, ST-Ericsson, for trusting me with this project as well as for sponsoring it. Philippe's support was always available whenever it was needed and I appreciate very much his explanation of the WCDMA system in order to clarify the design specifications for this project.

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It is not easy to live away from loved ones for two years. My very dear friends Amar, Vijay and Hari more than made up for the people that I missed. I treasure the superb food, great games of tennis and few but memorable trips that I shared with them. I have also been lucky to have had many more friends; my stay in Delft could not have been so enjoyable without them and I will miss them a lot.

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Chapter 1

Introduction

1.1 Motivation

Today, a wide range of technologies have been implemented for mobile wireless communication. Global System for Mobile communications (GSM) and General Packet Radio Service (GPRS) are the well established 2G technologies. Enhanced Data rates for GSM Evolution (EDGE), Wideband Code Division Multiple Access (WCDMA), and High Speed Packet Access (HSPA) are the most popular 3G technologies in current use [1]. EDGE allows improved data transmission rates, as an extension on top of standard GSM. HSPA is a collection of two mobile telephony protocols - High Speed Downlink Packet Access (HSDPA) and High Speed Uplink Packet Access (HSUPA), that extend and improve the performance of existing WCDMA protocols.

By 2012, worldwide cellular handset semiconductor revenue is forecast to reach \$32.2 billion. In 2007, WCDMA was reported to have had the largest share of this market revenue by cellular technology, and it was estimated that it would maintain this lead through 2012, with EDGE and HSPA occupying second and third positions respectively [1]. Growth has been projected to be maximum for ICs in 3G HSPA enabled smart phones, which also support GPRS/EDGE and also these ICs have been projected to command the maximum selling price. To address this high growth segment, a small, low-cost, single-chip multi-band HSPA/WCDMA/GSM/EDGE transceiver solution is needed which supports all radio bands used worldwide for these protocols.

1.2 Design objectives

In WCDMA systems, there is finite leakage from transmitter (Tx) to receiver (Rx) due to the use of Frequency Division Duplexing (see section 2.5 for more details). This Tx leakage amplified

by the LNA creates linearity issue for the mixer. In most WCDMA receiver implementations, an inter-stage Surface Acoustic Wave (SAW) filter is used between the LNA and mixer to filter out the Tx leakage. However, to enable a single chip solution, it is necessary to eliminate the inter-stage SAW filter and there have been many attempts to do this [2, 3, 4]. The IC performance reported in [2] is not sufficient to meet WCDMA requirements with 4dB loss before the LNA and Tx leakage of up to -25dBm at receiver input. In [3], a LNA with tuned LC load using high Q bond-wire inductors has been used to filter the TX leakage. In [4], a Q enhancement circuit has been used at one of the nodes of the LNA to reduce the Tx leakage. The use of tuned circuits for filtering the TX leakage makes the receiver solution narrow-band and multiple LNAs each tuned to a different band are required to satisfy multi-band requirements.

However, if the mixer can be designed for a high IIP2, then this inter-stage filter can be eliminated, without the requirement of high Q tuned circuits before the mixer. In [5], a high IIP2 mixer has been reported. However this high IIP2 has been achieved by using an inductor to tune out the parasitic capacitance at mixer switched pair common sources. This again renders the mixer narrow-band and many such mixers would have to be used in parallel to implement a multi-band solution. To facilitate a simple multi-band solution, the high IIP2 of the mixer has to be met, preferably without using any tuned circuits even in the mixer. In [1], calibration has been used to design the mixer for $IIP2 > 90dBm$.

However, in the design presented in [1], inductors have been used in the LNA in order to achieve impedance matching at input, which renders the LNA narrow band. Now, if these inductors can also be eliminated, then the entire LNA+mixer design can be made wideband. A single such LNA+mixer combination can satisfy the requirements of all WCDMA bands and GSM as well. At present, since programmable duplexers are still not available, many LNAs would still need to be used in parallel to implement a multi-band solution. However the use of the same LNA for all bands and a single mixer for all bands, greatly simplifies the design as well as significantly reduces the design time. In future, when programmable duplexers become available, a single such LNA+mixer combination can be used to implement a receiver solution, wherein any WCDMA/GSM band can be selected through software. Eliminating the need for area consuming inductors also leads to a smaller die area and hence a lower-cost receiver solution.

Therefore the two most challenging objectives of this project can be summarized as: a) to design an inductor-less LNA, that satisfies the required Noise Figure (NF) as well as provides input matching over frequencies ranging from 870MHz to 2.17GHz and b) to design the mixer for a very stringent IIP2 of 50dBm referred to the LNA input without using any tuned circuits in the mixer.

1.3 Organization of this thesis

In chapter 2, first the WCDMA system is described briefly. Then, justification for the specifications of this design is made based on the test cases described in the WCDMA standard. Finally,

individual specifications derived for LNA and mixer are given.

In the next chapter, the noise cancelation topology chosen for LNA has been analyzed in detail. A modified noise cancelation topology with a reduced noise figure is then presented. Design choices for this topology based on the initial analysis is then given. In the end, simulation results for the LNA are summarized.

Chapter 4 is devoted to the design of the mixer. A new approach to reduce noise contribution from the transimpedance amplifier used in passive mixer topology is first explained. It was found that, there is not much information available in literature regarding the design of the transimpedance amplifier. Therefore, the procedure followed in this work for the design of the transimpedance amplifier is explained in detail in this chapter. The advantages of the use of a square wave LO over a sine wave LO and the effect of LO duty cycle on gain, noise and linearity of the mixer is explored. This is followed by a section on the design approach used to meet the very stringent IIP2 specification for the mixer. Finally the mixer simulation results are given.

In the next chapter, the simulation results for LNA+mixer combination are given. In chapter 6, the layouts of LNA and mixer, along with results of post layout simulations done on these blocks are presented. The last chapter discusses the conclusions reached during this design and recommendations for future work.

In the appendix A, the analysis of negative feedback using two port network theory is explained. This analysis has been used in the design of the transimpedance amplifier.

Chapter 2

System Considerations and design specifications

2.1 Introduction

Universal Mobile Telecommunication System (UMTS) is one of the technologies standardized by the International Telecommunication Union (ITU) for 3G mobile communication systems [6]. UMTS uses Wideband Code Division Multiple Access (WCDMA) as the air interface. The LNA and mixer combination designed in this work is targeted mainly for WCDMA. Therefore, in this chapter, WCDMA system considerations important for understanding the specifications targeted in this design will be covered. Also a brief justification for these specifications, based on the system considerations will be given.

2.2 UTRA-FDD

Two technologies using UMTS have been standardized by ITU for 3G. UMTS Terrestrial Radio Access with Frequency Division Duplexing (UTRA-FDD) is the more popular one of the two (The other is UTRA Time Division Duplexing or UTRA TDD). In FDD, transmission and reception happens simultaneously but the transmit and receive channels are separated in frequency. In TDD, the transmit and receive channels can use the same frequency but are separated in time. The main characteristics of the UTRA-FDD system and the exhaustive list of different frequency bands allocated to it can be found in [7]. The three major frequency bands targeted in this design are as shown in table 2.1.

In the UTRA-FDD system, the frequency spacing between adjacent channels is 5MHz and the

Table 2.1: UTRA FDD frequency bands

Operating Band	Transmit Frequencies (MHz)	Receive Frequencies (MHz)	Tx-RX Frequency seperation (MHz)
WCDMA I	1920-1980	2110-2170	190
WCDMA II	1850-1910	1930-1990	80
WCDMA V	824-849	869-894	45

signal bandwidth is 3.84MHz (which corresponds to the chip rate as explained later).

2.3 Spread spectrum (SS) communication techniques.

SS techniques are methods by which more frequency bandwidth is used than required by the actual information rate [8]. The use of higher bandwidth has the advantage of increased resistance to interference and jamming. In Frequency Hopping Spread Spectrum (FH-SS) technique, the signal is transmitted with normal bandwidth, but with carrier frequency rapidly changing with time within a wider frequency range. Since the receiver in FH-SS system is aware of the frequency hopping sequence, the received signal can be decoded at the receiver. In Direct Sequence Spread Spectrum (DS-SS), the carrier frequency remains the same, but the signal to be transmitted is multiplied by a high bandwidth signal. This high bandwidth signal also called the 'code' is a pseudo-random sequence which appears like noise, but is completely reproducible. The bandwidth of the resulting signal is same as that of the high bandwidth signal. The process of increasing the bandwidth occupied by the signal is called spreading. In the receiver, the received signal is multiplied by this high bandwidth pseudo-random sequence to recover the original signal (This process is called despreading). The despreading in the receiver recovers the original spectrum of the desired signal. The process of DS-SS transmission and reception is illustrated in figure 2.1.

The terms 'spreading factor' and 'spreading gain' are used to describe the ratio of rate of the spreading pseudo random sequence (also called the chip rate) to the information data rate (also called the bit rate)-

$$SF = \frac{\text{chip rate}}{\text{bit rate}} \quad (2.1)$$

$$SG = 10\log_{10}SF \quad (2.2)$$

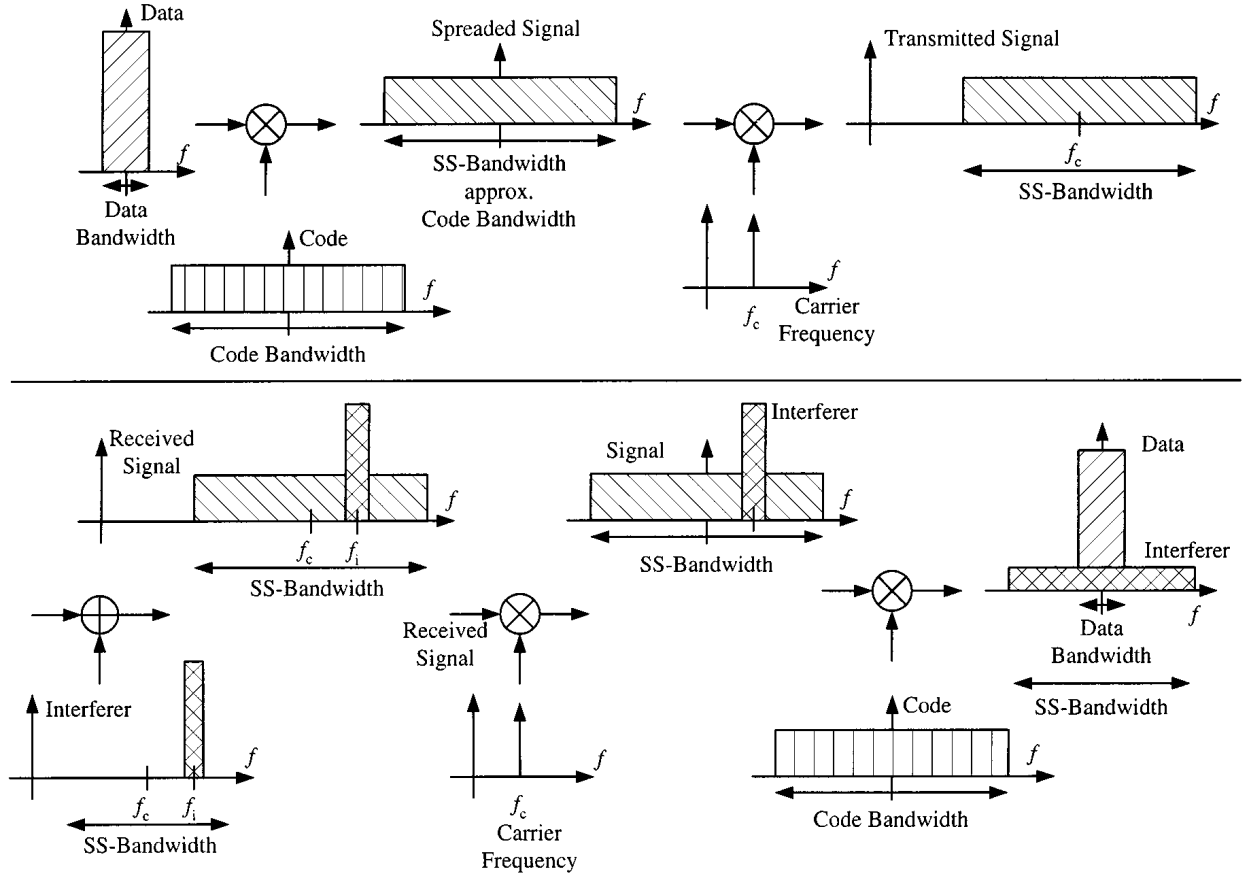


Figure 2.1: Spreading and de-spreading of signal in DS-SS technique and its resistance to narrow-band interference (image reproduced from [6])

The signal to noise ratio after despreading will be higher by a factor equal to the spreading gain compared to signal to noise ratio before despreading. This can be explained as follows. After despreading the original spectrum of the signal is recovered. Therefore the signal power which was spread over the high bandwidth of the pseudo random sequence before despreading, will occupy only its original narrow bandwidth after despreading. However, since noise will be uncorrelated to the spreading sequence, its power spectral density will not change after despreading. The noise power in signal band is therefore reduced by a factor equal to the spreading factor and hence the signal to noise ratio (expressed in dB) will increase by an amount equal to the spreading gain.

The process of spreading and despreading also increases the resistance of DS-SS communication technique to narrowband interferers. This is also shown in figure 2.1. Assuming that the interfering signal will be uncorrelated to the spreading sequence, its power will be spread over the bandwidth of the spreading sequence after despreading. Therefore the total interference power in the signal band again reduces by a factor equal to the spreading factor.

2.4 CDMA and Wideband CDMA

Multiple Access (MA) is allowing several users to share the capacity of the same physical medium. In Frequency Division Multiple Access (FDMA), each user is allotted one carrier frequency. In Time Division Multiple Access (TDMA), different users access the same carrier frequency at different times. CDMA is a multiple access technique based on the interference robustness of SS techniques. Here all users share the same carrier frequency at all the time, but each individual user is allocated a unique code. In FH-CDMA, this code is the frequency hopping sequence, while in DS-CDMA it is the multiplying sequence. UMTS uses DS-CDMA as the multiple access technique. Using orthogonal codes for spreading, several CDMA channels are multiplexed onto the same frequency channel. When the spreading codes used by different users using the same frequency channel are orthogonal, at the receiver, only the signal which was initially spread by the same pseudo random sequence as that used for despreading will be fully recovered. The signals of other users will not contribute to any power in the despread signal and hence will not result in any interference. However, it should be noted that interference from other users using the same frequency channel, will be zero, only when the spreading sequences used are perfectly orthogonal. Therefore, the choice of pseudo random spreading sequence significantly influences the overall performance of a CDMA system.

Eventhough the term CDMA is a general one and refers to the multiple access technique already explained, it is most popularly used for the IS-95 standard developed by Qualcomm for 2G systems, in which the bandwidth per channel is 1.25MHz (as compared to 5MHz in UMTS). Although there are many more differences between IS-95 and UMTS than just the bandwidth [8], the MA technique used in UMTS is called Wideband CDMA (WCDMA) to distinguish it from that used in the IS-95 standard.

2.5 General WCDMA system considerations

The UTRA-FDD system employs simultaneous transmission and reception. Therefore, a duplexer is required to provide isolation between transmitter and receiver as shown in figure 2.2. Even, in the presence of the duplexer, there is spurious leakage from transmit band (Tx) to receive band (Rx) due to close spacing of these bands as can be seen from table 2.1. Although a combination of spreading sequence allocation and data scrambling is used to minimize number of signal nulls, the envelope of the transmitted signal exhibits large amplitude variations [9]. Unless sufficient selectivity is available between transmit and receive bands, the spurious transmitter signal with large amplitude variations will cause severe dynamic range and intermodulation problems in the receive chain.

To attenuate the leakage signal from the transmitter as much as possible, it is important to have a high performance duplexer with good Tx-Rx isolation. Data regarding typical characteristics of

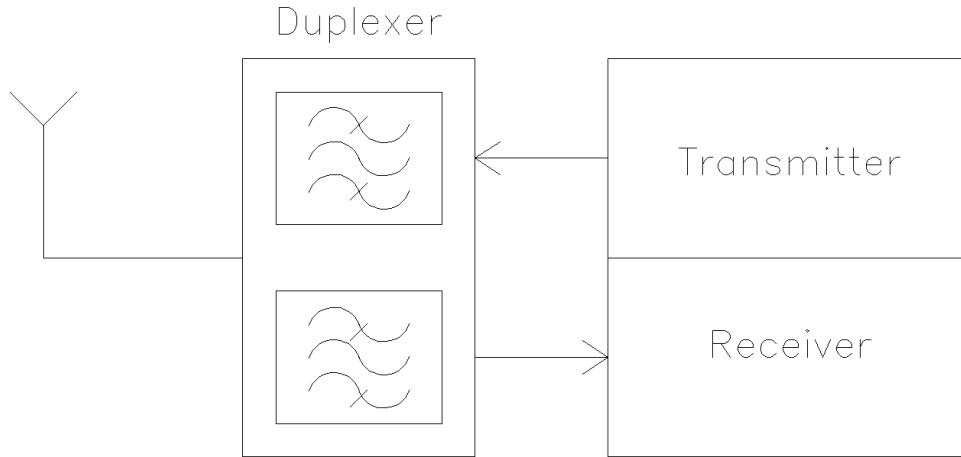


Figure 2.2: Interfacing of antenna to transceiver using duplexer in a WCDMA system

duplexer and different transmitter power classes has been compiled in table 2.2 [9, 7]. The different transmitter power classes have been defined to make the UMTS standard applicable to both hand-held as well as fixed units. For these power classes, along with nominal power, tolerance has also been specified. The tolerance for first three power classes is $\pm 1/3$ dB and for last two it is $\pm 2/2$ dB.

Table 2.2: Duplexer characteristics and transmitter power classes

Parameter	Typical values (Worst case in brackets)
Duplexer Rx path loss (dB)	3 (4)
Duplexer Tx path loss (dB)	1.5 (2.5)
Duplexer Tx-Rx isolation in Tx band (dB)	60
Transmitter power classes (dBm)	33,27,24,23,21

The power level of transmitter leakage signal at the receiver input can be calculated by taking the transmitter power class, adding the corresponding tolerance, adding the Tx path loss and subtracting the duplex filter isolation. The result is between -23.5 dBm and -34.5 dBm. Therefore, in this design a typical spurious transmitter level of -25dBm has been assumed.

2.6 UTRA-FDD test cases and WCDMA receiver specifications

Wideband CDMA is the air interface for UTRA-FDD 3G standard. The standard specifies the various test scenarios for a fixed user bit rate of 12.2kbps and the bit error rate (BER) must be

below 10^{-3} . As already mentioned before, the bandwidth for each channel is 3.84Mhz. Therefore the spreading gain (SG) given by equation 2.3 can be calculated as-

$$SG = 10 \log_{10} \left(\frac{3.84 \times 10^6}{12.2 \times 10^3} \right) = 25dB \quad (2.3)$$

The signal to noise ratio for achieving the required BER is specified in terms of the E_b/N_t ratio, where E_b is the energy per bit and N_t is the combined power spectral density of noise and interference. The required E_b/N_t ratio for BER= 10^{-3} , with some margin is [9] -

$$\frac{E_b}{N_t} = 7dB \quad (2.4)$$

In the rest of this section, important test cases described in UTRA-FDD standard [7] and the corresponding WCDMA receiver specifications to meet the requirements of these test cases will be discussed. The test cases and corresponding receiver requirements have been dealt with in detail in [9]. Of these, only the ones required for understanding the specifications for this design will be covered here.

2.6.1 Noise Figure

The noise figure (NF) of the receiver is calculated from the standard's reference sensitivity test. The sensitivity test specifies that the BER of 10^{-3} has to be met even when the power in the desired channel (P_D) at the antenna is as low as -117dBm. Using the previously mentioned E_b/N_t ratio, duplexer receive path loss and spreading gain, the maximum allowable noise power within the channel bandwidth (3.84MHz) at the receiver input can be calculated as -

$$P_N = P_D - \text{Duplexer Rx loss} - \frac{E_b}{N_t} + SG = -117dBm - 4dB - 7dB + 25dB = -103dBm \quad (2.5)$$

The required receiver noise figure can be calculated as -

$$NF = P_N - 10 \log_{10}(KT_oB) = -103dBm + 108dBm = 5dB \quad (2.6)$$

Where K is Boltzmann's constant, T_0 is the standard noise temperature 290K and B is the channel bandwidth (3.84MHz).

In the above calculation of receiver NF, we have considered only the thermal noise in the received signal and noise added by the receiver itself. However, the standard specifies that the sensitivity has to be met in the presence of maximum allowed modulated signal at the output of the transmitter. In the presence of signal at transmitter output and hence Tx leakage signal at receiver input, even LO phase noise and intermodulation components contribute to noise in the signal band. Also the noise of the transmitter in receive band after attenuation in the duplexer will add to the total noise at the input of the receiver. To account for all these noise contributions and also the noise added by the circuit blocks following the LNA and mixer, the NF for the LNA+mixer combination was decided to be 2.5dB typical and 3.5dB in the worst case.

2.6.2 Second order intercept point

Low second order distortion (even order distortion in general) is important due to the presence of strong and modulated unwanted signals at receiver input. Second order non-linearity acting on such a signal can produce spurious signals at baseband as shown in figure 2.3. Since direct down conversion architecture is used in this design, any spurious signal at baseband can affect the reception of the desired signal. Two such groups of disturbing signals are present: unwanted channels in the receive band and the transmitter leakage signal [9].

The spectral shape and bandwidth of these signals is same as that of the desired signal but the spectrum of second order product will be twice as broad as that of the desired signal. Due to the large bandwidth of the desired signal, high pass filtering can be accomplished with negligible degradation in performance. Thus, a combination of highpass and low pass filtering can be used to improve the signal power to interference power by a typical value of 6dB. however, the improvement is strongly dependent on the signal configuration of the unwanted signals and can range from 4 to 13dB [9].

Both in-band IIP2 and out-of-band IIP2 are important to ensure that the required BER is met in the presence of unwanted channels in receive band and transmitter leakage signal. However, the required in-band IIP2 is small compared to the very stringent out-of-band IIP2 to be met by a WCDMA receiver [9]. Therefore only the out-of-band IIP2 will be covered here.

The required out-of-band IIP2 is determined by the transmitter leakage level present at the receiver input. As mentioned in the previous section, the spurious components in baseband due to

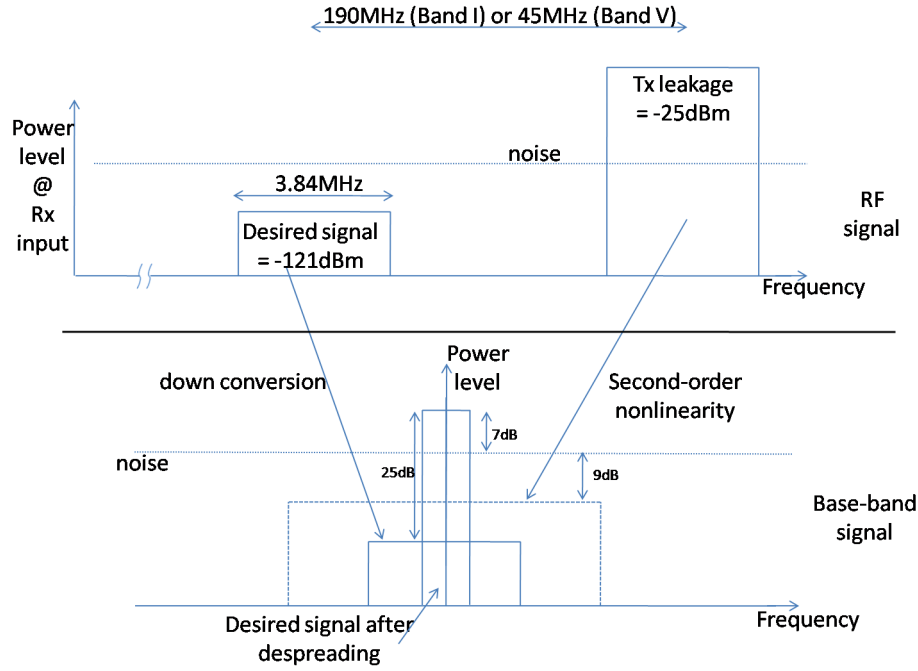


Figure 2.3: Spectrum with desired and spurious signals due to second order non-linearity

transmitter leakage should be sufficiently below the noise level at receiver input, in order to meet the receiver sensitivity at minimum desired signal power and maximum allowable signal power at transmitter output. For the spurious signals to be at least 9dB below the noise level, the required IIP2 can be determined as -

$$\begin{aligned} \text{Out of band } IIP_2 &= 2P_{Txleak} - (P_N + 6dB - 9dB) \\ &= 2(-28)dBm - (-103 + 6 - 9)dBm = 50dBm \end{aligned} \quad (2.7)$$

where P_{Txleak} has been taken to be -28dBm assuming the total transmitter leakage of -25dBm at receiver input will be split between two tones and 6dB is the improvement assumed due to highpass and lowpass filtering.

2.6.3 Third order intercept point

The third order intercept points are determined by the blocking requirements specified in the UTRA-FDD standard [7].

2.6.3.1 Out-of-band IIP3

Among the many blocking requirements, the out-of-band continuous wave blocker test sets the most stringent IIP3 requirement. If a continuous wave blocker is present at the half the spacing between Tx and Rx band, then any third order non-linearity acting on this signal and the transmit leakage signal will produce spurious components within the desired band as shown in figure 2.4

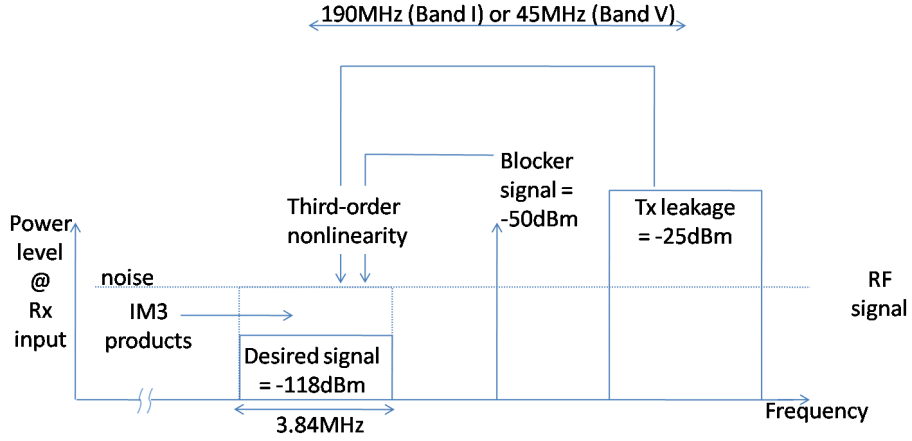


Figure 2.4: Spectrum with desired and spurious signals due to third order non-linearity

The power level of this continuous wave blocker is specified in the standard to be -44dBm at the antenna. The power level of this signal at the receiver input will depend on the attenuation at this frequency provided by the duplexer. The maximum power level of the transmit leakage signal at receiver input, as already mentioned, is -25dBm.

When the voltage levels of two signals, whose IM3 component is of interest, are different, their effective voltage level can be calculated as -

$$A_{IN,eff} = \sqrt[3]{A_1 A_2^2} \quad (2.8)$$

where $A_{IN,eff}$ is the effective voltage level, A_1 is the voltage level of the interferer farther from the desired band and A_2 is the voltage level of the interferer closer to the desired band. Therefore the effective power level of the input (when expressed in dB) can be calculated as -

$$\begin{aligned} P_{IN,eff} &= \frac{1}{3} \times (P_{Tx \text{ leak}}) + \frac{2}{3} \times (P_{blocker} - \text{attenuation in duplexer}) \\ &= \frac{1}{3} \times (-25dBm) + \frac{2}{3} \times (-44dBm - 6dB) = -41.7dBm \end{aligned} \quad (2.9)$$

where attenuation of the duplexer at half the spacing between Tx and Rx band is assumed to be 6dB (Since the duplexer loss in Rx band itself is 4dB, assumption of 6dB attenuation at half spacing between Tx and Rx bands is very pessimistic. When the attenuation is higher than this value, the required IIP3 will be lower than what is calculated in equation 2.10).

BER of 10^{-3} has to be satisfied for a minimum signal level of -114dBm for this test. Since the minimum signal level is now 3dB higher, noise will contribute to only 50% of allowed noise plus distortion power. Therefore the allowed level of spurious signal is $P_N = -103\text{dBm}$. The required IIP3 can be calculated as -

$$\begin{aligned} \text{Out of band } IIP_3 &= P_{IN,eff} - \frac{1}{2}(P_{IN,eff} - (-103\text{dBm})) \\ &= -41.7\text{dBm} - \frac{1}{2}(-41.7\text{dBm} - (-103\text{dBm})) = -11\text{dBm} \end{aligned} \quad (2.10)$$

To have some margin in the design, the out-of-band IIP3 specification for this design has been chosen to be -10dBm

2.6.3.2 In-band IIP3

In-band IIP3 is a measure of the receiver's ability to receive a WCDMA signal at its assigned channel frequency in the presence of an unwanted narrow band interferer at a frequency, which is less than the nominal channel spacing. In the UTRA-FDD standard [7], the power level of these interferers has been specified to be -56dBm at the antenna and will therefore be -60dBm at the receiver input. A BER of 10^{-3} has to be satisfied, when the signal level at the input is -107dBm (10dB higher than that specified for reference sensitivity test). Since the WCDMA channel bandwidth is 3.84MHz, which will be spread equally on either side of the local oscillator frequency (f_{LO}), the maximum signal frequency offset from f_{LO} is 1.92MHz. For measuring the In-band IIP3, two interferers at 3MHz and 4.4MHz offset from f_{LO} have been considered in this design. The IM3 component of interest will be at 1.6MHz offset from f_{LO} .

Since the BER is to be satisfied for a signal power of -107dBm (10dB higher than reference sensitivity test), the tolerable power of combined noise and interference is -93dBm (10dB higher than that calculated in equation 2.5). Due to close spacing of interferers to the desired channel, oscillator phase noise and channel selectivity will also contribute to spurious signals in the desired band in addition to third order intermodulation [9]. Allocating 30% of the total allowed noise plus distortion power to third order intermodulation component, the allowed power level of this component is -98dBm. Therefore the required in-band IIP3 can be calculated as -

$$\text{In-band } IIP_3 = -60\text{dBm} - \frac{1}{2}(-60\text{dBm} - (-98\text{dBm})) = -41\text{dBm} \quad (2.11)$$

2.6.4 Gain of LNA+Mixer combination

To reduce the noise contribution of circuit blocks following the LNA and mixer, it is necessary too have sufficient gain in the LNA+mixer combination. The gain requirement for this design was 36dB (typical) and 32dB (worst case).

2.6.5 Input referred 1dB cross compression point (ICCP1)

High power level of Tx leakage signal at receiver input can cause compression of the desired signal. Input referred 1dB cross compression point is the power level of Tx leakage signal which will reduce the gain of the receiver for the desired signal by 1dB. Since the Tx leakage can be as high as -25dBm, the required ICCP1 for this design is chosen to be -25dBm.

2.6.6 Power consumption

The target power consumption for this design was 30mW from 1.2V supply.

2.7 Individual specifications for LNA and mixer

In this design, the LNA has been designed to behave like a transconductance and the mixer accepts current as input, while generating a voltage at its output. Since it is inconvenient to report mixer input referred specifications as currents and LNA input referred specifications as voltages, the specifications for both these circuit blocks have been referred to the LNA input. The specifications for the mixer can be referred to LNA input by assuming the LNA to be ideal and consider only the linear gain of the LNA. The targeted specifications for LNA and mixer in this design are as shown in table 2.3. The specification for in-band IIP3 has not been included in this table, because this specification is much less stringent compared to the specification for out-of-band IIP3. Therefore in-band IIP3 should easily be satisfied once out-of-band IIP3 is met.

To arrive at the individual specifications for noise figure, if the noise figure of the mixer is referred to the LNA input, then the following equation can be used -

Table 2.3: Summary of specifications for LNA+mixer along with targeted individual specifications (worst case values are given in brackets for some specifications)

Specification	Value for LNA+mixer combination	value for LNA	value for mixer (referred to LNA input)
Noise Figure (dB)	2.5 (3.5)	2.05 (2.7)	0.73 (1.4)
IIP2(@Tx offset) (dBm)	50		50
Out-of-band IIP3 (dBm)	-10	-7	-7
Gain (dB)	36 (32)		
ICCP1 (dBm)	-25		
Power consumption (mW)	30		

$$NF_{tot} = NF_1 + NF_2 - 1 \quad (2.12)$$

Where NF_{tot} is the noise factor for the cascade of two stages, NF_1 is the noise factor of the first stage (LNA), NF_2 is the noise factor of the second stage (mixer) referred to the input of first stage. The noise figure can then be calculated as $noise\ figure = 10\log_{10}(noise\ factor)$

For calculation of individual IIP3 specifications, the following equation has been used [10] -

$$\frac{1}{A_{IIP3,tot}^2} = \frac{1}{A_{IIP3,1}^2} + \frac{G_{v1}^2}{A_{IIP3,2}^2} \quad (2.13)$$

Where $A_{IIP3,tot}^2$ is the IIP3 (in absolute voltage and not dBm) for the cascade of two stages, $A_{IIP3,1}^2$ is the IIP3 of first stage, $A_{IIP3,2}^2$ is the IIP3 of the second stage and G_{v1} is the linear voltage gain in first stage. Again, since the mixer IIP3 has been referred to LNA input, G_{v1} has been taken as 1.

Due to the use of fully differential LNA in this design along with ac-coupling between LNA and mixer, the effective IIP2 of the LNA will be very high. Therefore in this design, the IIP2 of the LNA+mixer combination will be limited by the IIP2 of the mixer and thus the IIP2 specification for the combination directly determines the IIP2 specification for the mixer.

Chapter 3

Low Noise Amplifier

3.1 Introduction

An inductor-less wide-band LNA for multi-band WCDMA has been designed in this thesis work. In this chapter, first a brief justification is given for the choice of LNA topology. Important properties of this topology, namely the noise cancelation topology are explained in section 3.3. In the same section the different possible implementations of this topology and the implementation chosen for this design are mentioned. In the next section, the requirements to meet input matching are given. In section 3.5, the various design trade offs are elaborated upon for the noise cancelation topology. The actual design of the LNA, along with several modifications carried out on the basic topology to reduce noise figure and power consumption are highlighted in section 3.6. In the final section the simulation results for the LNA are presented.

3.2 Choice of LNA topology

The high sensitivity required in modern integrated receivers sets stringent requirements on the LNA. LNAs need to have sufficient gain to reduce the impact of noise contributions of the following circuit blocks, low noise figure ($< 3dB$), adequate linearity and input impedance matching. The aim of this design was also to satisfy these requirements over multiple WCDMA bands. Therefore these requirements had to be satisfied across frequencies ranging from 870MHz to 2.17GHz. A stretch goal was to aim for inductor-less design.

Common wide-band inductor-less CMOS low noise amplifiers have been reviewed in [11] in order to highlight their noise figure limitations. In this paper, a limited form of noise-cancelation presented in [12], has been generalized. Also, in this paper, a LNA using noise cancelation technique

has been presented, which has $NF < 2.4dB$ over frequencies ranging from 150MHz to 2GHz, $s_{11} < -10dB$ and $s_{21} = 13.7dB$ from 10-1600MHz and IIP3=0dBm, thus demonstrating that very stringent LNA requirements can be met over a very wide frequency range, using the noise cancellation technique. Therefore the noise cancellation topology has been chosen for the LNA in this design.

The complete schematic of the differential LNA is as shown in figure 3.1.

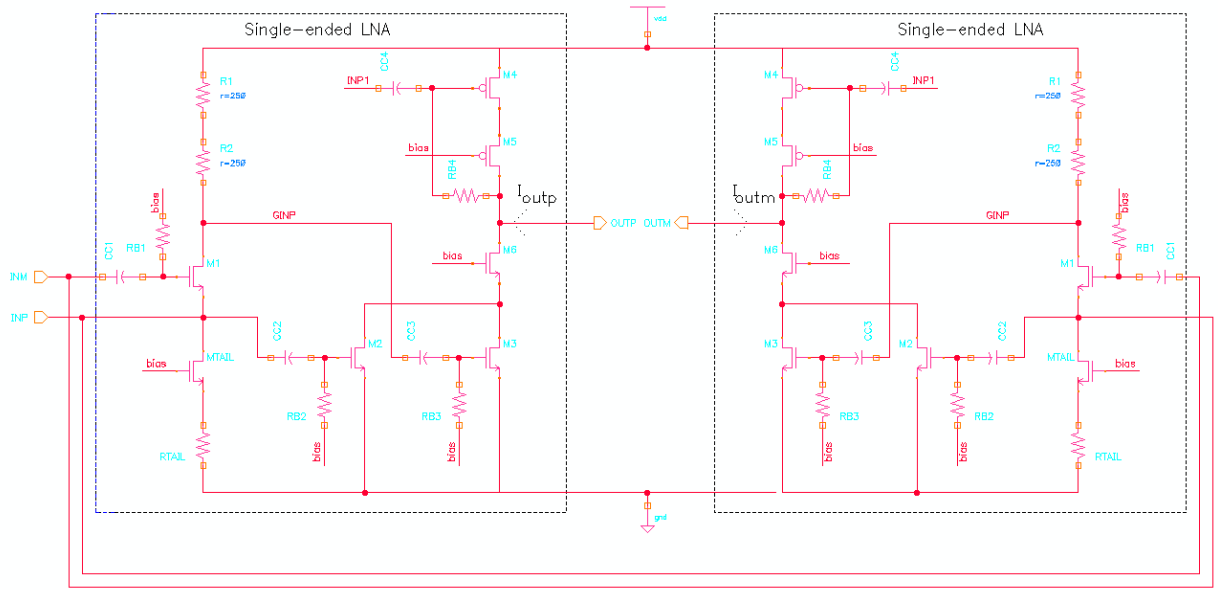


Figure 3.1: Complete schematic of the differential LNA (biasing not shown)

3.3 Noise cancellation topology

3.3.1 Principle of noise cancellation

Using the noise cancellation technique, the noise of the transistor used for active input impedance matching can be canceled. To understand this, let us consider the schematic shown in figure 3.2(a). The looking-in impedance at node INP is $Z_{in} \approx \frac{1}{g_{m1}}$, where g_{m1} is the transconductance of M1. By choosing $g_{m1} = \frac{1}{R_s}$, the input impedance of this circuit can be matched to the source impedance. Now, let the instantaneous direction of the noise current of M1, which can be modeled as a current source $I_{n,M1}$ between the drain and source terminals, be as shown in figure 3.2(a). We can see that the noise voltage at nodes INP and OUTP due to $I_{n,M1}$ will be fully correlated but opposite

in polarity. In addition, the noise voltage at node OUTP will be a gained up version of the noise voltage at node INP by a factor $\frac{R_1}{Z_{in}}$.

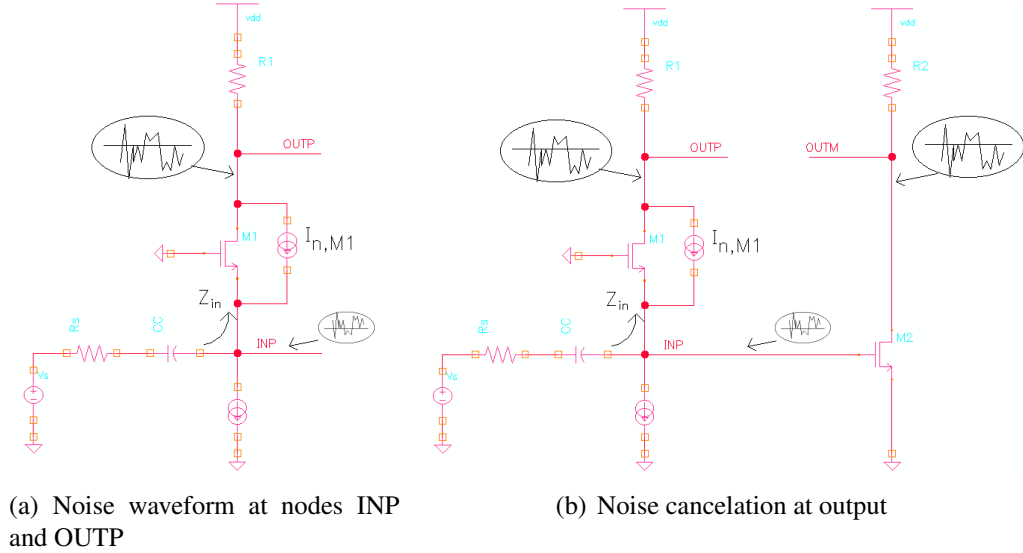


Figure 3.2: Noise cancellation principle

Now if a common source stage is added to the circuit as shown in figure 3.2(b) and if gain of this stage satisfies the condition

$$|G_{CS}| = g_{m2}R_2 = \frac{R_1}{Z_{in}} \quad (3.1)$$

then the noise voltages at node OUTP and OUTM due to $I_{n,M1}$ will be equal in magnitude and of the same polarity. If the output is taken differentially across the terminals OUTP and OUTM, then the noise due to M1 does not appear in the output and can therefore be considered to be canceled.

3.3.2 An added benefit: cancelation of distortion of matching transistor

In addition to noise of M1, any distortion introduced by M1 is also canceled at the output. This has been explained very well in [14]. The analysis in [14] is included here for completeness. Let us consider the noise cancellation topology redrawn with relevant details as in figure 3.3.

Non-linear behavior of M1 can be modeled by a drain-to-source current i_{ds} , which depends non-linearly on v_{gs} and v_{ds} of M1. Therefore signal source voltage V_s causes a non-linear drain-to-

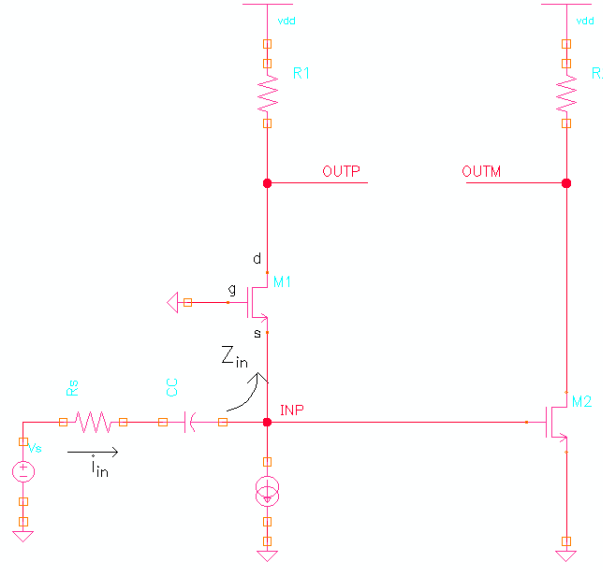


Figure 3.3: Distortion cancelation of M1

source current i_{ds} in M1 which, flowing through the linear source resistance R_s produces a non-linear voltage at node INP which can be written using Taylor expansion as -

$$v_{INP} = \alpha_1 v_s + \alpha_2 v_s^2 + \alpha_3 v_s^3 + \dots = \alpha_1 v_s + v_{NL} \quad (3.2)$$

where $\alpha's$ represent the Taylor coefficients and v_{NL} represents all the non-linear terms. The coupling capacitance CC at input has been assumed to be large enough to act as a short at the frequency of the input signal. The voltage at node OUTP can be written as -

$$V_{OUTP} = i_{in} R_1 = \frac{v_s - v_{INP}}{R_s} R_1 = ((1 - \alpha_1) v_s - v_{NL}) \frac{R_1}{R_s} \quad (3.3)$$

The voltage at node OUTM can be written as -

$$V_{OUTM} = -g_{m2} R_2 v_{INP} = -\frac{R_1}{Z_{in}} v_{INP} = (-\alpha_1 v_s - v_{NL}) \frac{R_1}{R_s} \quad (3.4)$$

where equation 3.1 and $Z_{in} = R_s$ have been used.

Now, if the output is sensed differentially between the nodes OUTP and OUTM, then the output voltage can be written as -

$$V_{OUT,diff} = V_{OUTP} - V_{OUTM} = v_s \frac{R_1}{R_s} \quad (3.5)$$

From equation 3.5, we can see that any non-linear current introduced by M1 also gets canceled at the output. Since the condition for cancelation of distortion of M1 is same as that for cancelation of noise of M1 and for input impedance matching, simultaneous noise and distortion cancelation can be obtained along with input impedance matching.

3.3.3 Comparison of noise cancelation topologies

The noise cancelation topology shown in figure 3.2(b) can be generalized into a model as shown in figure 3.4 [11]. The model consists of an amplifier stage to provide source impedance matching $Z_{in} = R_s$, another amplifier stage sensing the voltage and noise across the input source and a network for combining the output of these two stages, such that noise of the matching transistor is canceled, while signal contributions from these two stages add up. The noise cancelation topology shown in figure 3.2(b) has been redrawn in figure 3.5 with the functional blocks highlighted. The process of sensing the output differentially between the nodes OUTP and OUTM serves the function of the combining network.

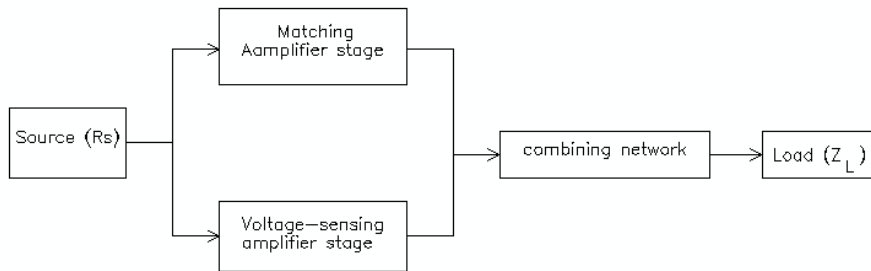


Figure 3.4: Generalized model for noise cancelation topologies

On the basis of this model, several possible topologies for noise cancelation of the matching transistor have been proposed in [15]. Since, the distortion of the matching transistor is canceled as

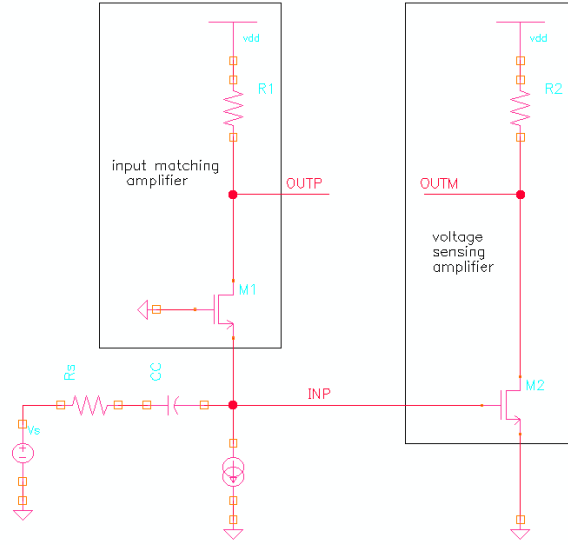


Figure 3.5: Functional blocks corresponding to the generalized noise cancellation model

mentioned in the previous section, the distortion performance of these topologies is decided by the common source stages used for voltage sensing and combining functions. It will be shown in section 3.5.2 that, the load impedance of common source stage has to be small in order to obtain good IIP3. With low load impedance for the common source stage, the overall voltage gain that can be obtained from the LNA will be low. Without adequate voltage gain these topologies are not well suited for providing a voltage output from the LNA. However, these stages are well suited for providing a current output with good linearity and hence can act as good transconductance stages. But, all the topologies proposed in [15] are for providing a voltage output from the LNA and hence were not considered suitable for meeting the LNA requirements of this design. Even in the topology shown in figure 3.5, noise of M1 is canceled only when the voltage at nodes OUTP and OUTM are sensed differentially and not when the drain currents of M1 and M2 are sensed differentially. With voltage being sensed at the output of the common source stage, a LNA designed using this topology will also suffer from low IIP3 and was not considered suitable for this design.

A new topology has been proposed in [16]. This is as shown in figure 3.6.

The condition for cancelation of M1 noise in this topology is-

$$\frac{g_{m2}}{g_{m3}} = \frac{R_1}{Z_{in}} = g_{m1}R_1 = A_{v1} \quad (3.6)$$

where $A_{v1} = g_{m1}R_1$ is also the gain in the input arm. Even this topology has been proposed to provide a voltage output. However, it can be easily modified as shown in figure 3.7 to provide

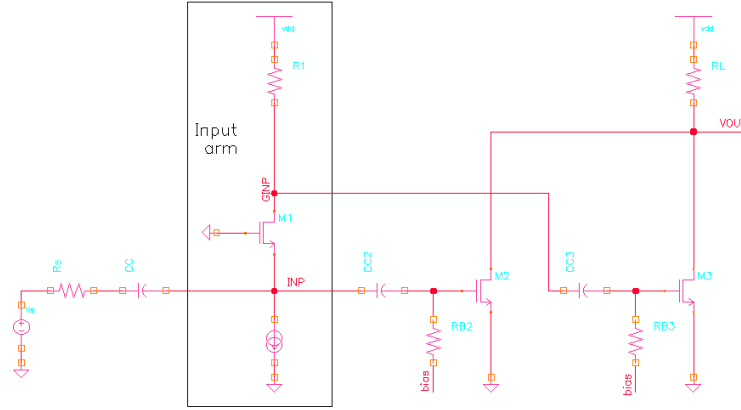


Figure 3.6: A new LNA topology employing noise cancellation

a current output. In figure 3.7, the load resistance R_L has been replaced with a high impedance represented by a current source. A current output can now be taken from this LNA, when the input impedance of the succeeding stage is low, as is the case in this design, where the mixer provides a low input impedance.

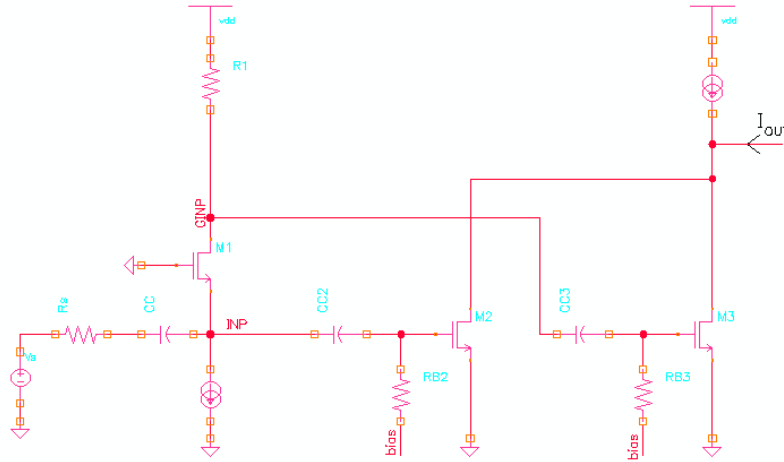


Figure 3.7: Modification of the new LNA topology to provide current output

The topology shown in figure 3.7 has been used for the design of the LNA in this work. Two such LNAs have been used to implement a differential input, differential output LNA. The LNA which has been designed to act as a transconductance, is followed by a mixer which accepts current as input. As can be seen from figure 3.1, several modifications have been done to the basic noise cancellation topology shown in figure 3.7. These were done to reduce noise figure and power consumption of the LNA. These will be explained in section 3.6.

3.4 Achieving input matching

For the input network, 2nH of inductance has been considered in series with the input terminals of the LNA to account for bond-wire inductance. Looking into the input terminals of the LNA, through the bond-wire inductors, the LNA has been matched to a differential port impedance of 100Ω as shown in figure 3.8.

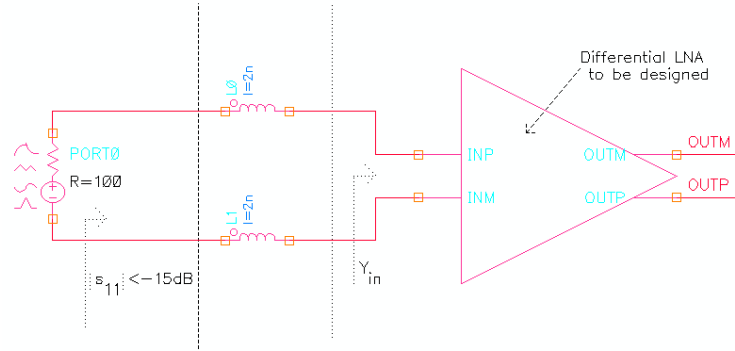
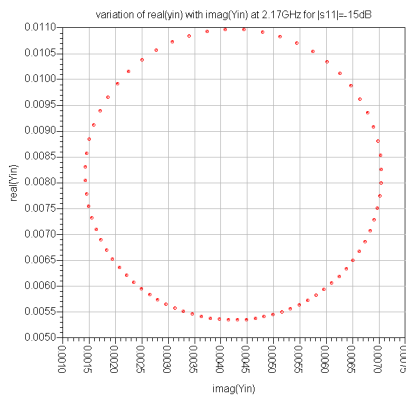
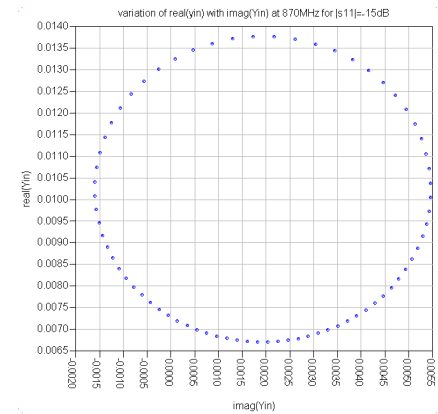


Figure 3.8: Circuit schematic considered for input matching

To ensure good matching, it was aimed to have $|s_{11}| < -15dB$. To achieve this condition, it is necessary to find the Y_{in} , which can satisfy this condition. Therefore, all possible combinations of $\text{real}(Y_{in})$ and $\text{imag}(Y_{in})$ which can satisfy the condition $|s_{11}| = -15dB$ were generated at both the maximum and minimum frequencies of operation of the LNA (2.17GHz and 870MHz). These are shown in figures 3.9(a) and 3.9(b).



(a) Variation of $\text{real}(Y_{in})$ with $\text{imag}(Y_{in})$ at 2.17GHz for $|s_{11}| = -15dB$



(b) Variation of $\text{real}(Y_{in})$ with $\text{imag}(Y_{in})$ at 870MHz for $|s_{11}| = -15dB$

Figure 3.9: Required Y_{in} for input matching

If the combination $(\text{imag}(Y_{in}), \text{real}(Y_{in}))$ lies within these circles, then $|s_{11}| < -15\text{dB}$. Since many combinations of $\text{real}(Y_{in})$ and $\text{imag}(Y_{in})$ are possible, which can satisfy the condition of input matching, one of these can be chosen which best satisfies the other requirements of the LNA such as noise figure, linearity and power consumption. The actual choice is explained in section 3.6.

3.5 Trade offs between noise figure, linearity and power consumption

3.5.1 Effect of gain in the input arm

Consider the simplified schematic of single ended noise cancellation topology as shown in figure 3.10.

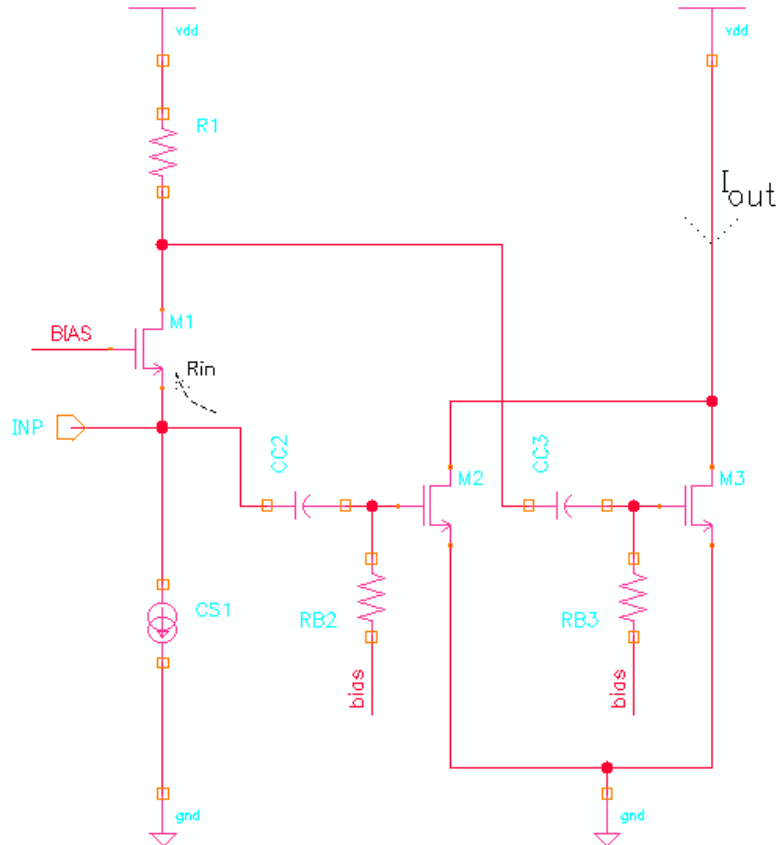


Figure 3.10: Simplified topology of LNA using noise cancellation scheme

The PSD of noise current at the output can be written as-

$$I_{n,out}^2 = KTR_s(g_{m2} + A_{v1}g_{m3})^2 + I_{n,cs1}(R_{in}||R_s)^2(g_{m2} + A_{v1}g_{m3})^2 + 4KTR_1g_{m3}^2 + 4KT\gamma\alpha g_{m2} + 4KT\gamma\alpha g_{m3} \quad (3.7)$$

where g_{m2} and g_{m3} are transconductance of M2 and M3, $I_{n,cs1}$ is the noise of current source CS1 (which can be modeled as a current source in parallel with CS1), γ is the MOSFET noise parameter and $\alpha = \frac{g_m}{g_{d0}}$, with g_{d0} being the drain conductance when $v_{ds} = 0$. The coupling capacitors have been assumed to act as shorts at frequency of the input signal. The noise contribution of bias resistors RB_1 and RB_2 has been assumed to be negligible. Also only the channel thermal noise of M2 and M3 has been considered (Other noise sources of M2 and M3 will be negligible at frequencies of interest in this design, where max frequency of operation is 2.17GHz and F_T of transistors is about 70GHz). The transconductance of the LNA is -

$$G_{LNA} = g_{m2} + A_{v1}g_{m3} \quad (3.8)$$

From equation 3.7, it can be seen that, if A_{v1} is increased by increasing R_1 and if g_{m3} is reduced by the same factor by which A_{v1} is increased, then the noise contribution of R_1 reduces, while the transconductance of the LNA remains the same.

However this degrades the distortion performance of the LNA, which is explained as follows. Let the input signal be v_{in} . The first and higher order terms in the output current can be written as-

$$i_{out} = g_{m2}v_{in} + \frac{g'_{m2}}{2!}v_{in}^2 + \frac{g''_{m2}}{3!}v_{in}^3 + \dots + g_{m3}(A_{v1}v_{in}) + \frac{g'_{m3}}{2!}(A_{v1}v_{in})^2 + \frac{g''_{m3}}{3!}(A_{v1}v_{in})^3 + \dots \quad (3.9)$$

where g'_m and g''_m refer to the first and second derivatives of g_m .

If A_{v1} is increased by a factor of ζ ($\zeta > 1$) by increasing R_1 and g_{m3} is reduced to g_{m3}/ζ , to keep G_{LNA} constant, then the first and higher order terms in the output current are -

$$\begin{aligned}
 i_{out} = & g_{m2}v_{in} + \frac{g'_{m2}}{2!}v_{in}^2 + \frac{g''_{m2}}{3!}v_{in}^3 + \dots \\
 & + \frac{g_{m3}}{\zeta}(\zeta A_{v1}v_{in}) + \frac{g'_{m3}}{2!\zeta}(\zeta A_{v1}v_{in})^2 + \frac{g''_{m3}}{3!\zeta}(\zeta A_{v1}v_{in})^3 + \dots
 \end{aligned} \tag{3.10}$$

To compare the distortion in the two cases, let us consider the ratio of third order term to first order term in equations 3.9 and 3.10. While in equation 3.9, the ratio is -

$$\frac{g''_{m3}(A_{v1}v_{in})^3 + g''_{m2}v_{in}^3}{3!(g_{m3}(A_{v1}v_{in}) + g_{m2}v_{in})} \tag{3.11}$$

in equation 3.10, the ratio is -

$$\frac{\frac{g''_{m3}}{\zeta}(\zeta A_{v1}v_{in})^3 + g''_{m2}v_{in}^3}{3!\left(\frac{g_{m3}}{\zeta}(\zeta A_{v1}v_{in}) + g_{m2}v_{in}\right)} \tag{3.12}$$

Observing that the denominator is same in both the ratios, we can see that the distortion is higher in the case when the gain in the input arm is increased by a factor ζ , with $\zeta > 1$. Thus having higher gain in the input arm reduces the noise figure of the LNA, but degrades the distortion performance of the LNA.

3.5.2 Optimum bias point for linearity, Noise figure and low power consumption

As described in section 3.3.2, the distortion of the matching transistor is also canceled in this LNA topology. Therefore, in the simplified topology shown in figure 3.10, the distortion is determined by transistors M2 and M3. With the use of a differential LNA topology, IM2 products are greatly suppressed. Hence, the biasing of M2 and M3 needs to be optimized for maximizing IIP3, which is decided mainly by g'_m and g''_m .

Figure 3.11 shows the variation of g_m , g'_m and g''_m with V_{GS} of a MOSFET, for an arbitrarily chosen transistor size of $2(2.6\mu/0.08\mu)$ and a fixed drain to source voltage. From the figure 3.11, we can

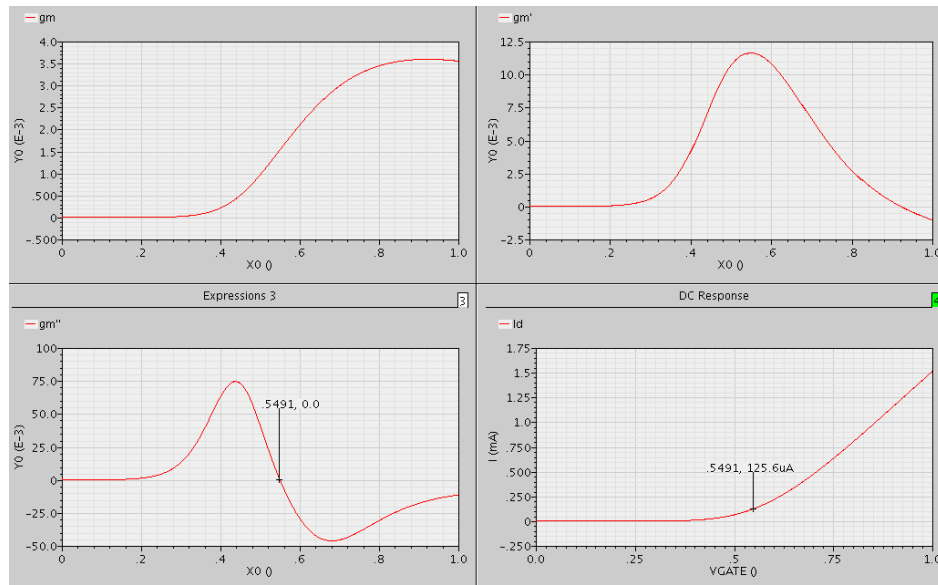


Figure 3.11: Variation of g_m , g'_m and g''_m of a MOSFET with V_{GS}

see that there is a bias point where g''_m is zero. This is the bias point for maximum IIP3. (IIP3 will still not be ∞ at this bias point, since even higher order terms in equation 3.9 can result in third order inter-modulation products).

Figure 3.12 shows the variation of IIP3 measured in the drain current, as a function of bias current for the same transistor.

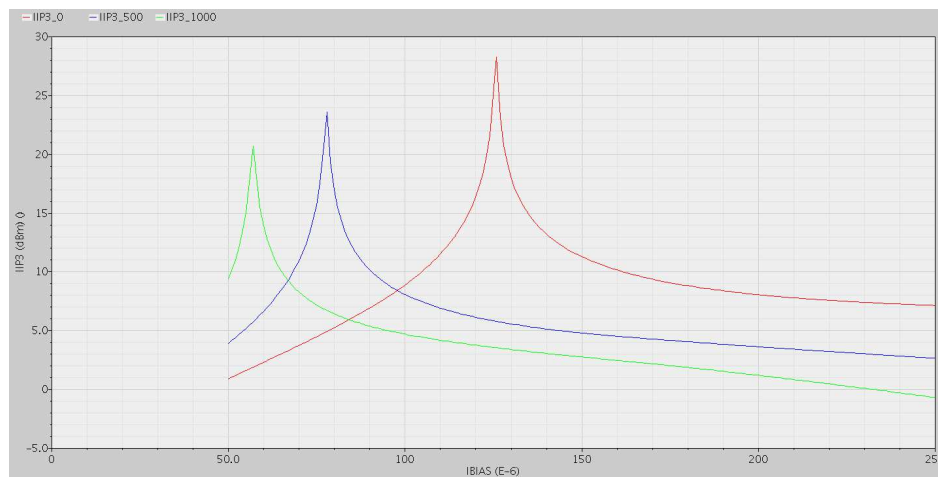


Figure 3.12: Variation of IIP3 vs. bias current for different load impedances

The traces 'IIP3_0', 'IIP3_500' and 'IIP3_1000' represent this variation for impedance of 0Ω , 500Ω and $1k\Omega$ respectively at the drain. We can see that, when the impedance at drain is zero, IIP3 is

maximum at a bias current of 125uA, which as we can see from figure 3.11, is also the point where g_m'' is zero. However, with higher load impedance at the drain, not only does the entire IIP3 vs. bias current curve shift down, but also the maximum IIP3 point moves towards lower bias current value.

Figure 3.13 shows the variation of IIP3 as a function of bias current for the same impedance levels as in figure 3.12, but with cascoding. We can see, that the curves for 0Ω and 500Ω load impedances almost overlap, which means that the IIP3 is no longer sensitive to loading if the load impedance is maintained low. However, for higher load impedance (e.g. 1000Ω) we can see that the IIP3 degrades even with cascoding.

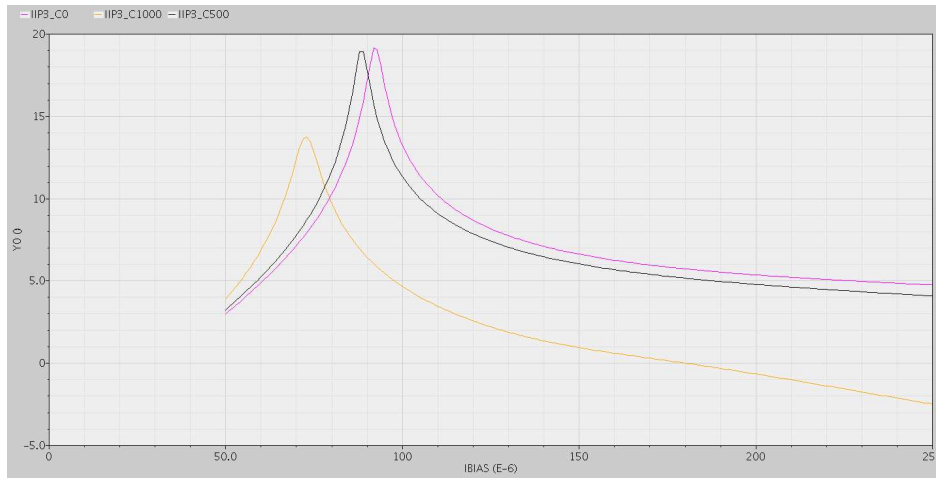


Figure 3.13: Variation of IIP3 vs. bias with cascoding for different load impedances

If the bias point for transistors M1 and M2 is to be chosen only from the point of maximizing IIP3, then the bias point where IIP3 reaches maximum in figure 3.13 is the optimum one. However this bias point is not the optimum, when NF and power consumption of the LNA are also considered. This can be explained as follows. Using the expression for output noise current given in equation 3.7, the noise factor (NF) of the simplified LNA topology shown in figure 3.10 can be written as -

$$NF = \frac{KTR_s(g_{m2} + A_{v1}g_{m3})^2 + I_{n,cs1}(R_{in} || R_s)^2(g_{m2} + A_{v1}g_{m3})^2 + 4KTR_1g_{m3}^2 + 4KT\gamma\alpha g_{m2} + 4KT\gamma\alpha g_{m3}}{KTR_s(g_{m2} + A_{v1}g_{m3})^2} \quad (3.13)$$

From equation 3.13, we can see that increasing g_{m2} and g_{m3} reduces the noise factor, since the noise contribution of M2 and M3 is directly proportional to these transconductances, while the noise contribution of the source resistance R_s is proportional to square of these transconductances.

Also as explained in section 3.4, in order to keep $|s_{11}|$ lower than -15dB, there is a fixed maximum capacitance that can be tolerated at the input of the LNA. To get maximum g_m , for this fixed input capacitance, the bias point of M2 and M3 has to be chosen where F_T of these transistors is maximum. Figure 3.14 shows the variation of F_T with bias current.

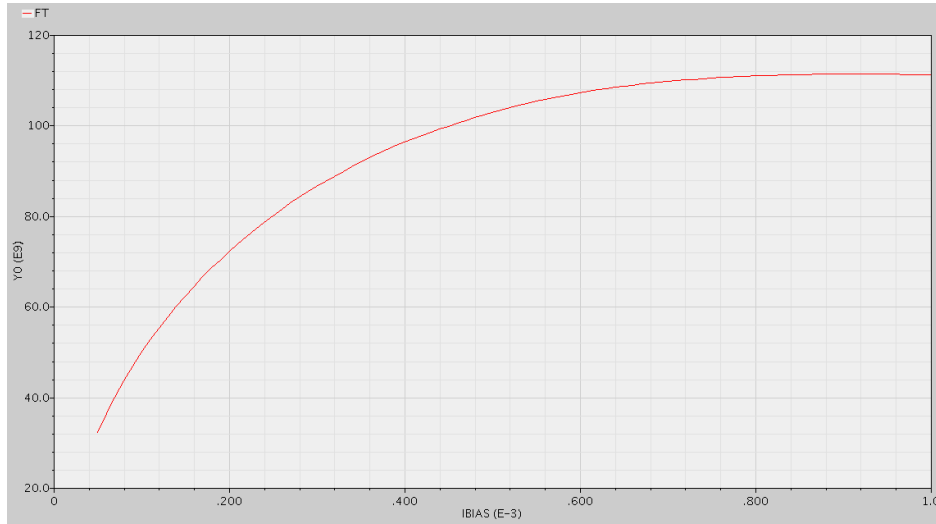


Figure 3.14: Variation of F_T with bias current

If there is no limit on power consumption, then to maximize F_T , bias point can be chosen where F_T just begins to saturate (which is about 800uA for transistor of size $2(2.6\mu/0.08\mu)$). However, this is not the optimum bias point for low power consumption, because increase in F_T for a given increase in bias current is high at low bias currents and decreases rapidly for increasing bias current. The choice of the bias point for transistors M2 and M3 and other transistors used in the final topology, taking into account the tradeoffs between noise, linearity and power consumption is explained in section 3.6.

3.6 Design of the LNA

As explained in section 3.5.2, it is necessary to use cascoding for transistors M2 and M3 to reduce the sensitivity of LNA IIP3 to load impedance. Also it is important to maintain a low load impedance. Since, the mixer, which follows the LNA, has been designed for current input, the required low impedance at signal frequency is provided by the mixer. However, it was found from simulations, that low impedance at DC is also essential to maintain good IIP3 performance. This is ensured by the load for the common source stage consisting of transistors M4, M5, resistor RB4 and capacitance CC4 as shown in figure 3.15. The load also provides a high input impedance at signal frequency, thus ensuring that the LNA behaves as a transconductance stage.

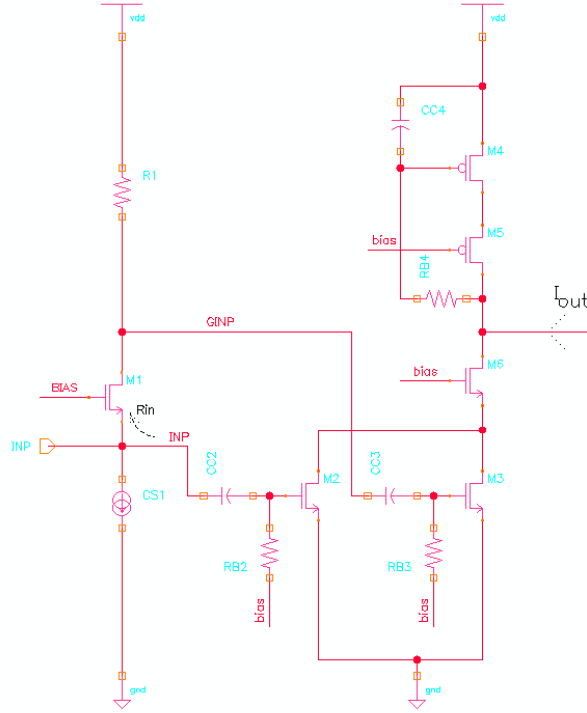


Figure 3.15: Noise cancellation topology for LNA with cascoding in output arm and load optimized for IIP3

3.6.1 Improvements to reduce noise factor

Instead of having an ac ground at the gate of M4, it is possible to split M4 into two transistors M42 and M43 and feed signals INP and GINP at the gates of these transistors as shown in figure 3.16. This will increase the effective transconductance from nodes INP and GINP to I_{out} and hence reduce the noise factor of the LNA, while still providing low impedance for the cascode near DC. If the ratio of transconductances of M42 and M43 is maintained the same as $g_{m2} : g_{m3} = A_{v1}$, then condition for noise and distortion cancelation of M1, as mentioned in section 3.3 is still satisfied. This can be done by choosing the same (W/L) ratio for each of the fingers in M42 and M43 and keeping the ratio of the fingers same as desired transconductance ratio.

Since capacitive loading at nodes GINP and INP is mainly due to transistors M3, M43 and M2, M42 respectively, the capacitances at these nodes will be in the ratio $1 : A_{v1}$. Now resistances at these nodes will be in the ratio $\frac{R_1}{R_{in} \parallel R_s} = \frac{A_{v1} R_{in}}{R_{in} \parallel R_s} \approx \frac{A_{v1} R_{in}}{R_{in}/2} = 2A_{v1}$. Therefore the bandwidth at node GINP will be approximately half the bandwidth at node INP and will limit overall bandwidth of the circuit. However, instead of splitting M4 into two transistors, the required transconductance from GINP to I_{out} can be implemented using only NMOS transistor M3 and the required transconductance from INP to I_{out} implemented as combination of NMOS transistor M2 and PMOS transistor

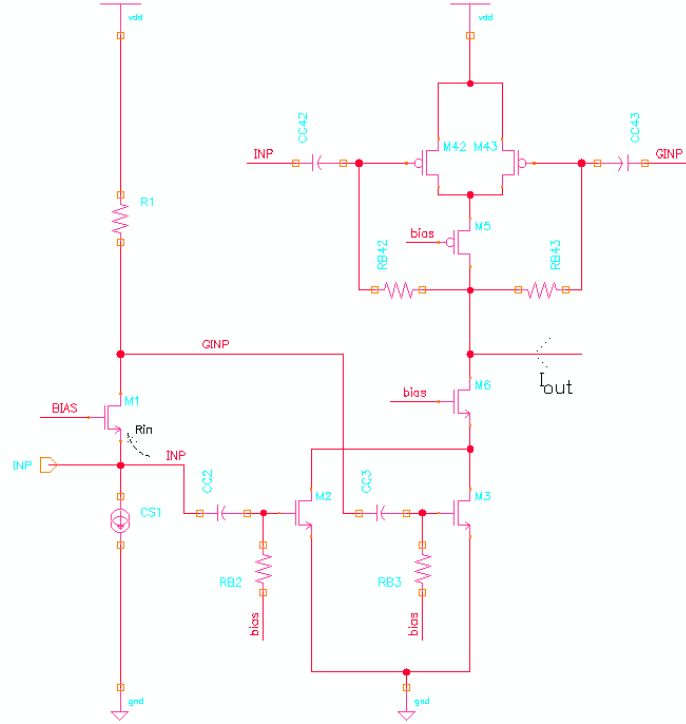


Figure 3.16: Improved noise cancellation topology for LNA with signal being fed to PMOS load

M4 as shown in figure 3.17. The condition to be satisfied by the transconductances of M2, M3 and M4 for noise and distortion cancellation of M1 is-

$$\frac{g_{m2} + g_{m4}}{g_{m3}} = A_{v1} \quad (3.14)$$

Now, for a given A_{v1} , the number fingers and W/L ratio of M4 can be chosen such that equation 3.14 is satisfied as well as the capacitances at nodes GINP and INP are in the ratio $1 : 2A_{v1}$. This ratio is exactly inverse of the ratio of the resistances at these nodes. Therefore the bandwidth at these nodes will now be equal. Also the absolute capacitance at node GINP will be reduced because of loading due to only NMOS transistor M3. Thus, not only do the bandwidth at nodes INP and GINP become same, but the bandwidth at these nodes, and hence the overall bandwidth of the circuit also increases. For this topology, the equation for the noise factor of the LNA will have to be modified as -

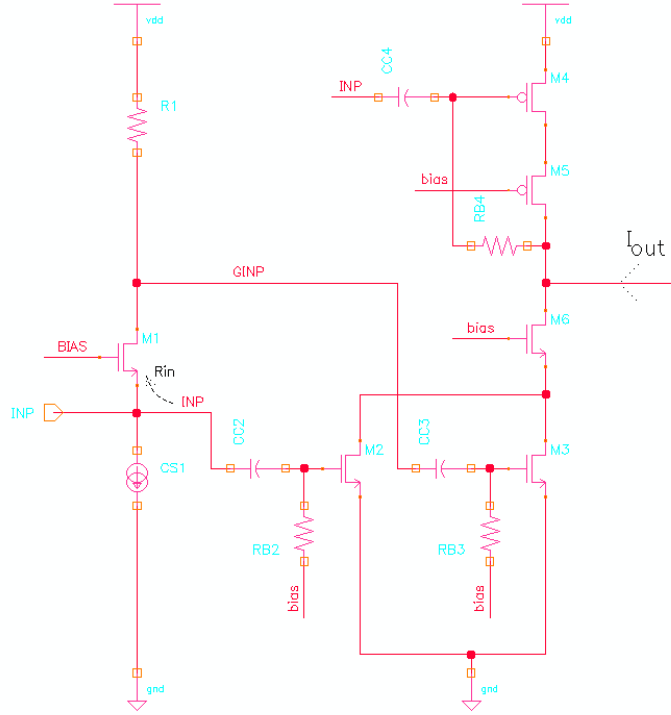


Figure 3.17: Improved noise cancelation topology optimized for bandwidth

$$NF = \frac{KTR_s(G_{LNA})^2 + I_{n,cs1}(R_{in}||R_s)^2(G_{LNA})^2 + 4KTR_1g_{m3}^2 + 4KT\gamma\alpha g_{m2} + 4KT\gamma\alpha g_{m3} + 4KT\gamma\alpha g_{m4}}{KTR_s(G_{LNA})^2} \quad (3.15)$$

where $G_{LNA} = g_{m2} + g_{m4} + A_{v1}g_{m3}$.

3.6.2 Cross-coupling of input to further reduce noise factor

Since the noise of the matching transistor M1 is canceled, the noise contributors in the input arm are the resistor R_1 and the current source CS1. The value of resistor R_1 is decided by the required gain A_{v1} in the input arm as well the allowable dc voltage drop across the resistor. For a given dc voltage drop, lower the bias current in the input arm, higher can be the value of R_1 . Although increasing the value of R_1 increases its noise contribution to the output noise current, the gain A_{v1} in the input arm and hence the total transconductance of the LNA also increases. This leads to overall lower noise factor for the LNA, as can be seen from equation 3.15.

To reduce the noise contribution of current source CS1, resistive degeneration has been used. Higher the degeneration resistance, lower will be the noise contribution of the current source. However, the maximum value of the degeneration resistance that can be used, is also limited by the dc voltage drop across the resistor. Therefore, lower bias current in the input arm helps to lower even the noise contribution of the current source.

Since the LNA is being designed for a differential input signal, cross-coupling of input can be used in each of the single ended LNAs [13]. This is as shown in figure 3.18.

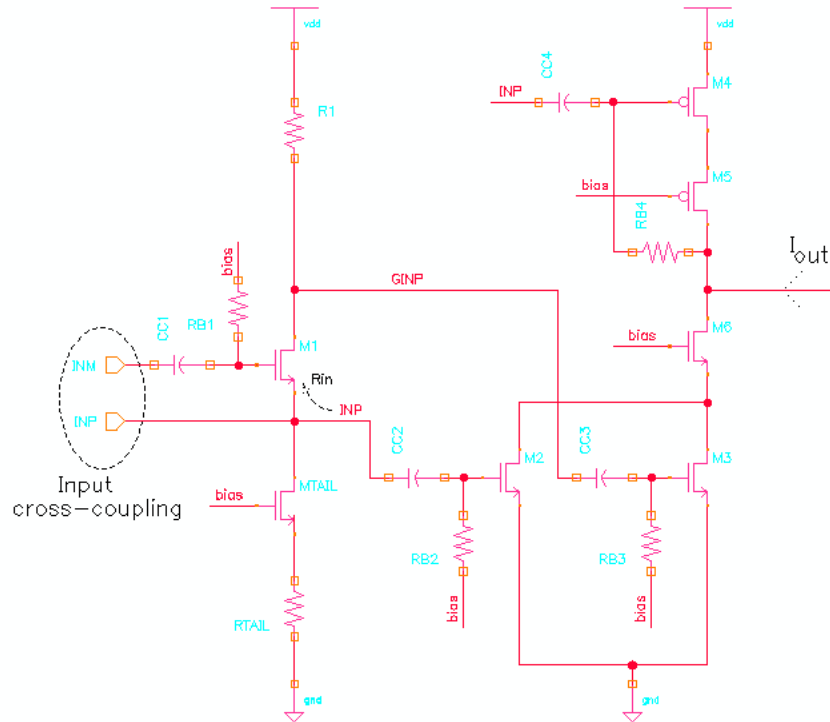


Figure 3.18: Improved noise cancelation topology with input cross coupling

Cross-coupling of the input doubles the effective signal voltage across the gate-source terminals of M1 and hence doubles its g_m for the same bias current. Therefore, for same g_{m1} as in the topology of figure 3.17, the bias current in the input arm can be reduced. This will reduce the noise factor of the LNA as mentioned before.

3.6.3 Choice of bias current in the output arm of the LNA

The capacitance at node INP is mainly decided by the input capacitance of the output arm of the LNA (C_{gs} and C_{gd} of transistors M2, M3 and M4 in figure 3.18). From equation 3.15, we can see that increasing g_{m2} , g_{m3} and g_{m4} leads to lower noise factor for the LNA. Therefore, in order to

make these transconductances as high as possible, first, the capacitance at node INP and hence $\text{imag}(Y_{in})$ has to be chosen to be the maximum that still satisfies the input matching condition. Then, for this fixed maximum capacitance, high g_m can be obtained by choosing the bias point where F_T is high. However, it was also explained in section 3.5.2, that the optimum bias points of common source stage for IIP3 and high F_T are not the same. Since the noise factor is a more critical specification in this design, higher priority has been given for noise factor, by choosing the bias current for M2, M3 and M4 where F_T is high. To keep F_T reasonably high, while still meeting the power consumption specification for the LNA, the current density for M2 and M3 was chosen to be 200uA for unit finger size of $2(2.6\mu/0.08\mu)$. The current density for M4 was chosen to be 200uA for unit finger size of $2(5.2\mu/0.08\mu)$. The number of fingers of M2, M3 and M4 were then increased, maintaining their ratio to satisfy the condition in equation 3.14, till the total capacitance at node INP reached the maximum that can satisfy the input matching condition. In this way, the transconductances g_{m2} , g_{m3} and g_{m4} were maximized, while simultaneously satisfying the condition for input matching.

3.6.4 Choice of voltage gain and bias current in the input arm of the LNA

It was explained in section 3.5.1 that, higher gain in the input arm will lower the IIP3 of the LNA. In order to decide the maximum gain that can be implemented in the input arm, it is necessary to quantify the IIP3 degradation due to this gain. In figure 3.13, the IIP3 performance of a simple common source stage with cascode has been plotted. To compute the degradation in IIP3, with respect to that of cascoded common source stage, let us consider the circuit shown in figure 3.19 (If we assume that the IIP3 performance of cascoded PMOS common source stage is similar to that of a NMOS stage, then g_{m2} used in subsequent analysis can be considered the sum of g_m of M2 and M4).

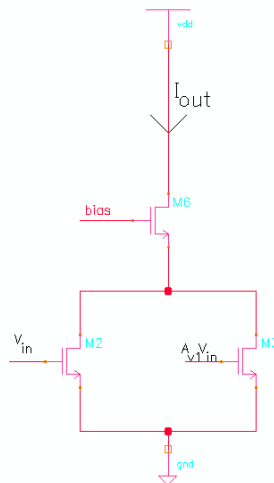


Figure 3.19: Circuit used for analysing IIP3 degradation due to gain in input arm

The condition to be satisfied for noise and distortion cancellation of M1 is $g_{m3} = \frac{g_{m2}}{A_{v1}}$. In a manner similar to that of equation 3.9, the output current can now be written as -

$$i_{out} = g_{m2}v_{in} + \frac{g'_{m2}}{2!}v_{in}^2 + \frac{g''_{m2}}{3!}v_{in}^3 + \dots$$

$$+ \frac{g_{m2}}{A_{v1}}(A_{v1}v_{in}) + \frac{g'_{m2}}{2!A_{v1}}(A_{v1}v_{in})^2 + \frac{g''_{m2}}{3!A_{v1}}(A_{v1}v_{in})^3 + \dots \quad (3.16)$$

where g_{m3} , g'_{m3} and g''_{m3} have been replaced by $\frac{g_{m2}}{A_{v1}}$, $\frac{g'_{m2}}{A_{v1}}$ and $\frac{g''_{m2}}{A_{v1}}$ respectively.

The ratio of first order terms to third order terms of v_{in} is -

$$\frac{\text{1st order terms}}{\text{3rd order terms}} = \frac{2g_{m2} \times 3!}{(1 + (A_{v1})^2)g''_{m2}} \quad (3.17)$$

For the simple cascoded common source stage, this ratio is $\frac{3! \times g_{m2}}{g''_{m2}}$ (This can also be confirmed by substituting $A_{v1} = 1$ in equation 3.17).

Since IIP3 depends on square-root of the ratio of first order terms to third order terms [10], the IIP3 for simple cascoded stage can be written as-

$$A_{IIP3,CCS} \propto \sqrt{\frac{3! \times g_{m2}}{g''_{m2}}} \quad (3.18)$$

where $A_{IIP3,CCS}$ is the IIP3 of the cascoded common source stage expressed in absolute voltage. Similarly, the IIP3 for the circuit shown in figure 3.19 can be written as-

$$A_{IIP3,LNA} \propto \sqrt{\frac{2g_{m2} \times 3!}{(1 + (A_{v1})^2)g''_{m2}}} \quad (3.19)$$

Therefore, with respect to the IIP3 of the cascoded common source stage, the IIP3 of the LNA (in dBm) can be written as -

$$IIP3_{LNA} = IIP3_{CCS} - \frac{1}{2} \times 20 * \log_{10} \left(\frac{1 + (A_{v1})^2}{2} \right) \quad (3.20)$$

where $IIP3_{CCS}$ is the IIP3 of cascoded common source stage plotted in figure 3.13 and $IIP3_{LNA}$ is the desired IIP3 of the LNA. From chapter 2, the targeted IIP3 for the LNA in this design is -7dBm. From figure 3.13, the IIP3 at bias current of 200uA is about 5dBm. If A_{v1} is chosen to be 4, then, from equation 3.20, the expected LNA IIP3 is about -4.3dBm, which leaves some margin over the desired specification. Therefore it was decided to implement a voltage gain of 4 (12dB) in the input arm. To obtain a gain of 4, R_1 in figure 3.18 was chosen to be $4 \times R_{in,SE}$, where $R_{in,SE}$ is the single ended looking in impedance of the LNA. From figure 3.9(a), the desired $\text{real}(Y_{in})$ for maximum $\text{imag}(Y_{in})$ is $\approx 8mS$, from which desired $R_{in,SE} = \frac{1}{2 \times \text{real}(Y_{in})} = 62.5\Omega$. Therefore R_1 was chosen to be 250Ω . (As can be seen from figure 3.9, maximum $\text{imag}(Y_{in})$ at 2.17MHz results in less than maximum allowed $\text{imag}(Y_{in})$ at 870MHz. Therefore if $\text{real}(Y_{in})$ is chosen to satisfy the requirement of $|s_{11}| < -15dB$ at 2.17GHz, the this requirement is satisfied at 870MHz also.)

Now, the real part of the input admittance looking into node INP can be written as -

$$g_{in} = \frac{R_1 + r_{ds1}}{1 + g_{m1}r_{ds1}} \quad (3.21)$$

where g_{m1} and r_{ds1} are the effective transconductance (taking into account cross-coupling of input) and output impedance of M1 respectively. The bias current in the input arm and size of M1 were chosen to get the required g_{m1} and r_{ds1} to make $g_{in} = 2 \times \text{real}(Y_{in}) = 2 \times 8mS = 16mS$.

3.6.5 A new method to reduce the noise contribution due to R_1

Modification to the noise cancelation topology, to reduce the noise contribution of resistance R_1 is shown in figure 3.20. As can be seen the value of R_1 has been doubled. This increases the voltage gain from INP to GINP, from 4 to 8. Capacitive division by a factor of 1/2 is used to reduce this gain back to 4 at the gate of M3. This is implemented by choosing the value of CC3 to be equal to the capacitance looking into the gate of M3.

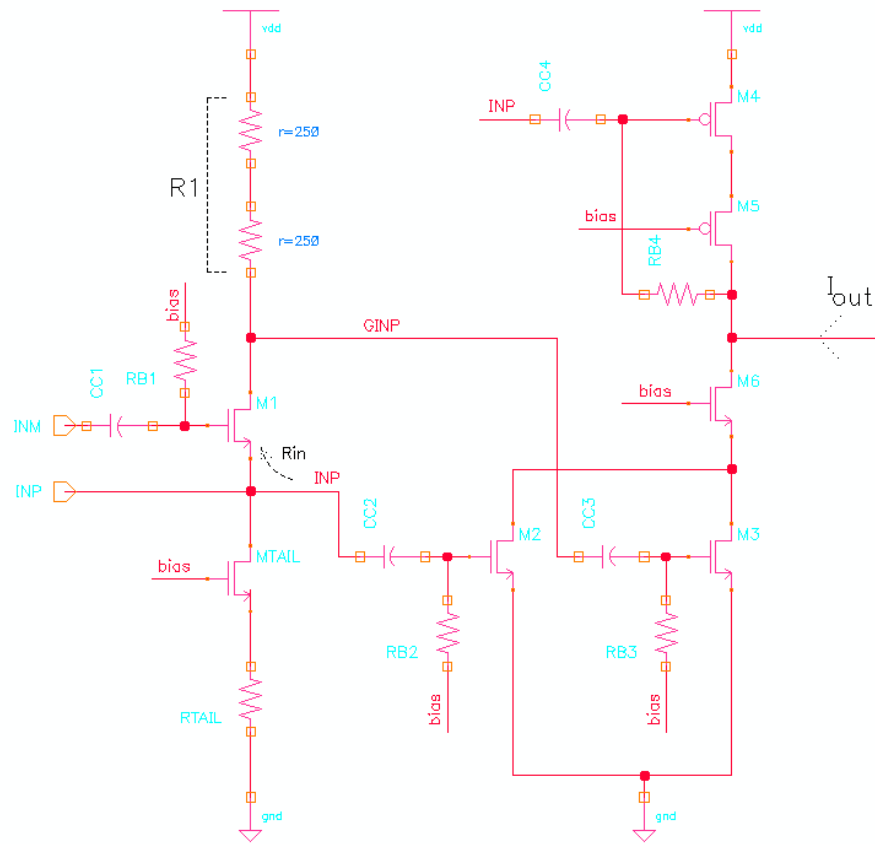


Figure 3.20: Modification to reduce the noise contribution of R_1

Since the gain of signal at the gate of M3 does not change, the IIP3 performance of the LNA is not affected. However, the noise contribution of R_1 to output current is reduced. This can be explained as follows. In the topology shown in figure 3.18, the noise contribution of R_1 is -

$$I_{nout,R1}^2 = 4KTR_1g_{m3}^2 \quad (3.22)$$

In the new topology, the noise contribution is -

$$I_{nout,R1}^2 = 4KT(2R_1) \times \left(\frac{1}{2}\right)^2 g_{m3}^2 \quad (3.23)$$

where the factor $(\frac{1}{2})^2$ is due to capacitive division. From equations 3.22 and 3.23, we can see that noise contribution of R_1 is reduced by a factor of $\frac{1}{2}$.

The topology shown in figure 3.20 is the final topology used in this design for implementing each of the single-ended LNAs shown in figure 3.1.

3.7 Simulation results

Nominal, fast and slow process corners were considered for simulations. Also temperatures 0°C , 27°C and 100°C have been considered. To reduce the total number of possible combinations of process corners and temperature, following combinations were chosen - nominal 25, fast 100, fast 0, slow 100 and slow 0. Also simulations have been done only in Band I (2.12GHz) and Band V (880 MHz). The performance in Band II (1.96GHz) is expected to be close to that of Band I. The test bench used for simulating the LNA is as shown in figure 3.21.

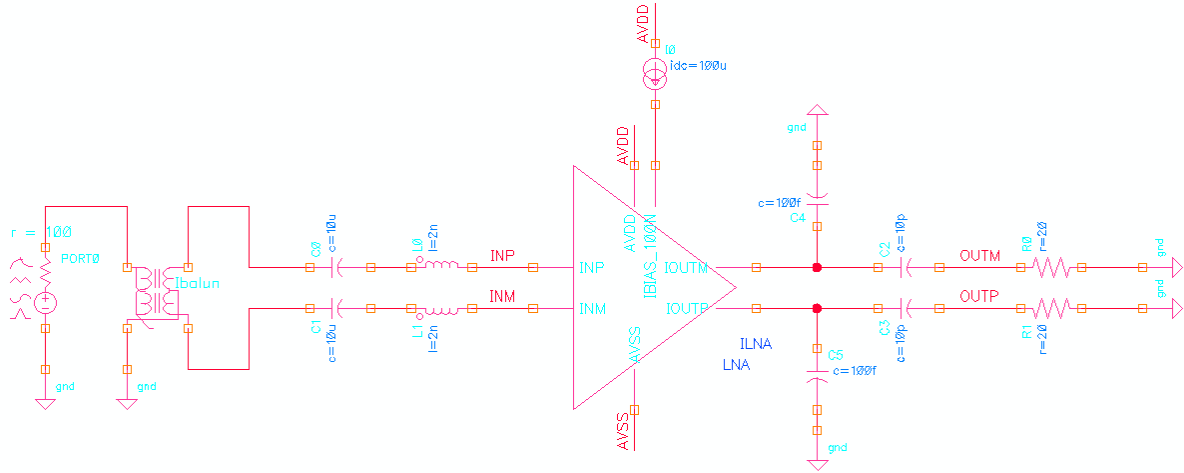


Figure 3.21: Test bench used for simulating the LNA

3.7.1 Power Consumption

The LNA consumes 11.5mA from 1.2V supply. Each of the single-ended LNAs use 4.8mA each. 1.9mA is used for biasing.

3.7.2 Transconductance

The LNA transconductance was measured as the ratio of the differential current flowing through resistors R0 and R1 to the equivalent voltage with respect to 100Ω corresponding to the input power. The transconductance in Band I and Band V in different simulation corners are as shown in table 3.1.

Table 3.1: Transconductance of LNA (mS)

Band	Nominal $25^{\circ}C$	Fast $0^{\circ}C$	Fast $100^{\circ}C$	Slow $0^{\circ}C$	Slow $100^{\circ}C$
I	189.4	208.6	182.8	185.4	154.3
V	205.8	224.7	198.3	202.7	170.6

3.7.3 Input matching

LNA s_{11} with respect to 100Ω impedance in nominal $25^{\circ}C$ corner is as shown in figure 3.22. The s_{11} in Band I and Band V in different simulation corners are as shown in table 3.2.

Table 3.2: s_{11} (dB) of LNA with respect to 100Ω impedance

Band	Nominal $25^{\circ}C$	Fast $0^{\circ}C$	Fast $100^{\circ}C$	Slow $0^{\circ}C$	Slow $100^{\circ}C$
I	-21.9	-22.3	-21.5	-21.4	-19.7
V	-17.9	-19.6	-16.3	-18.6	-15.0

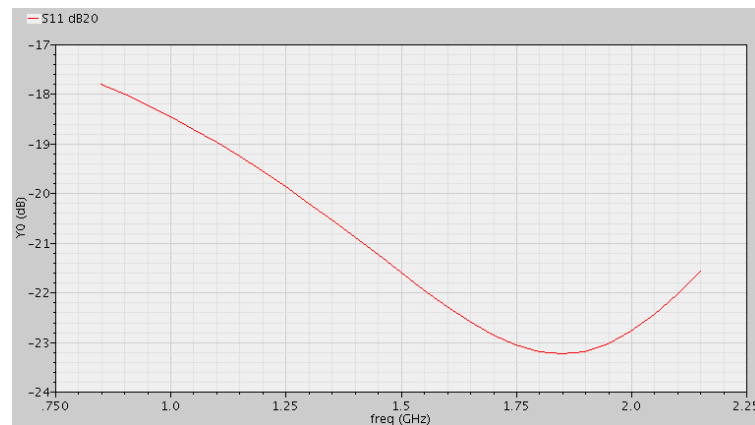


Figure 3.22: s_{11} of the LNA with respect to 100Ω impedance in nominal $25^{\circ}C$ corner

3.7.4 Noise Figure

The variation of noise figure of the LNA with frequency in nominal 25°C corner is as shown in figure 3.23. The noise figure in Band I and Band V in different simulation corners is as shown in table 3.3.

Table 3.3: Noise figure (dB) of LNA (Specification: 2.05dB (typical), 2.7dB (worst case))

Band	Nominal 25°C	Fast 0°C	Fast 100°C	Slow 0°C	Slow 100°C
I	2.23	2.06	2.62	2.10	2.71
V	2.16	1.99	2.58	2.03	2.67

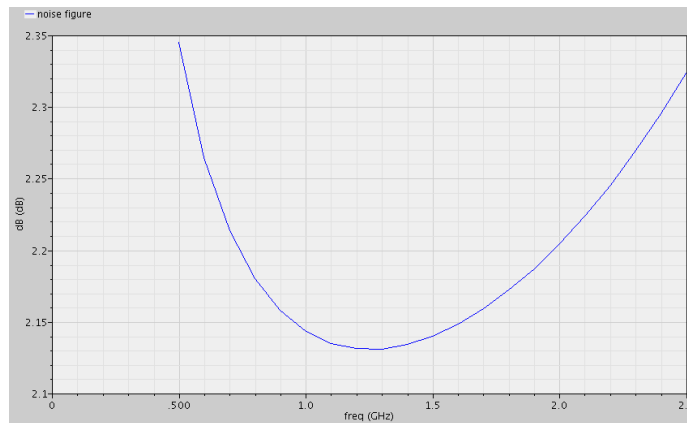


Figure 3.23: Noise figure of LNA in nominal 25°C corner

3.7.5 IIP2

Since the LNA has been implemented using a differential topology, ideally there should be no intermodulation components due to second order distortion. However, due to random mismatch between devices, small amount of IM2 components will be present at the output of the LNA. After mixing with the LO in the mixer, the sum frequency components will produce frequency components far from the desired signal band and hence will get filtered. Ideally, even the difference frequency components will get up-converted to LO frequency and should not affect the reception of the desired signal. However, due to finite RF to IF isolation in the mixer, the difference frequency components can leak to the mixer output and appear at baseband. Therefore IIP2 of the LNA, measured in terms of the spurious difference frequency component appearing at the LNA output, is of interest. Since, the difference frequency components lie close to DC, they will be attenuated by the ac-coupling between LNA and mixer, before appearing at mixer input.

Monte Carlo simulations were done to check the effective IIP2 performance of the LNA (including the IIP2 improvement due to attenuation of the difference frequency components by ac-coupling between LNA and mixer). The histogram of IIP2 in Band I is as shown in figure 3.24.

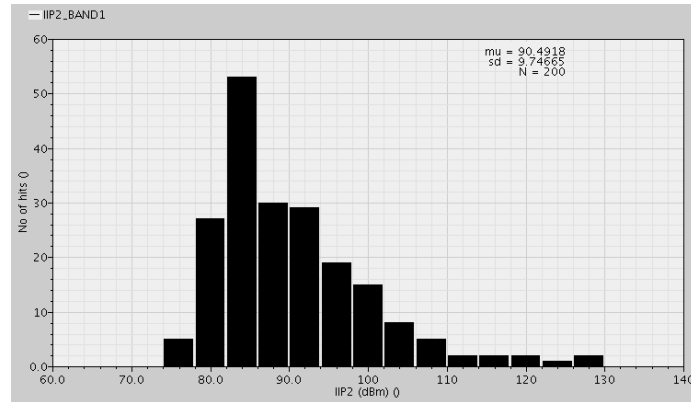


Figure 3.24: Histogram of LNA IIP2 in Band I

As can be seen from the figure the mean and standard deviation are 90.5dBm and 9.75dBm respectively for 200 Monte Carlo simulation iterations. However, while the lower limit for IIP2 is set by the maximum possible mismatch, there is no upper limit, since in the ideal case of no mismatch, the IIP2 is infinity. Therefore, as can also be seen from figure 3.24, the distribution of IIP2 is not Gaussian and therefore mean and standard deviation are not the right parameters to estimate the worst case IIP2. A good estimate can however be obtained from the lowest IIP2 obtained, which is about 74dBm.

The histogram of IIP2 in Band V is as shown in figure 3.25. The lowest IIP2 obtained in this case is 76dBm. Since the IIP2 specification for the LNA+mixer combination is 50dBm, we can see that IIP2 performance of the LNA will not be a limitation in achieving this specification.

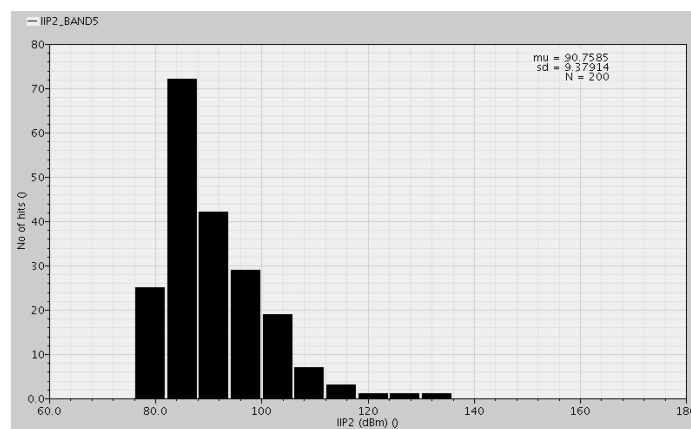


Figure 3.25: Histogram of LNA IIP2 in Band V

3.7.6 Out-of-band IIP3

Leakage from transmitter is the largest source of interference in WCDMA. In addition to this leakage, if there is any interfering signal at half the frequency separation between transmit and receive bands or at twice this separation, third order intermodulation can produce spurious components within the desired band. The out-of-band IIP3 performance is used to quantify the extent of performance degradation that can be caused by this interference.

In Band I, the frequency separation between transmit and receive bands is 190MHz (45MHz in Band V). To measure out-of-band IIP3 in Band I, two tones at offset frequency of 189MHz and 95MHz (43MHz and 22MHz in Band V), from LO frequency (2.12GHz in Band I and 880MHz in Band V) with power levels of -25dBm and -50dBm respectively were used as the input. Since the tone nearer to the desired band has higher influence on the third order spurious component, the effective input power level can be calculated as $\frac{1}{3} \times (-25) + \frac{2}{3} \times (-50) = -41.7\text{dBm}$. The spectrum of the output in nominal 25°C corner is shown in figure 3.26. Similar to the calculation of effective input power level, the effective voltage level of these tones at the output can be calculated as $\frac{1}{3} \times (-15.4) + \frac{2}{3} \times (-40.6) = -32.2\text{dB}$. The IM3 component of interest is one at 2.119GHz (879MHz in Band V). We can see that the voltage level of the IM3 component is -105.8dB. The IIP3 can now be calculated as $-41.7 + \frac{1}{2} \times (-32.2 - (-105.8)) = -4.9\text{dBm}$. Out-of-band IIP3 in Bands I and V in different simulation corners is as shown in table 3.4.

Table 3.4: Out-of-band IIP3 (dBm) of LNA (Specification: -7dBm)

Band	Nominal 25°C	Fast 0°C	Fast 100°C	Slow 0°C	Slow 100°C
I	-4.9	-4.5	-1.5	-5.8	-4.9
V	-5.6	-5.7	-6.7	-5.8	-6.1

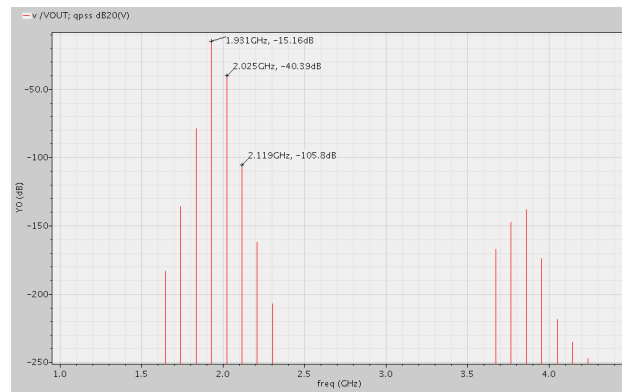


Figure 3.26: Spectrum to calculate out-of-band IIP3 of LNA (nominal 25°C corner)

Chapter 4

Mixer

4.1 Introduction

In this chapter the design and simulation results of a low noise and high IIP2 mixer is presented. Passive mixers result in low $1/f$ noise [17, 1, 18], making them an ideal choice for direct down conversion architecture. The required mixer IIP2 of 50dBm (referred to LNA input) is a very stringent specification in this design. It has been shown in [17], that passive mixers can also achieve a high IIP2. Therefore a passive mixer was chosen for this design.

In the next section, a new approach to reduce the noise of a passive mixer, by reducing the noise contribution of the transimpedance amplifier (TIA), is presented. This is followed by a detailed explanation of the design of the transimpedance amplifier itself. Effect of local oscillator (LO) waveform on gain, noise and linearity of the mixer is then explored followed by a brief explanation of the circuit used to generate the desired LO waveform. Design choices, which enabled the design of this mixer for high IIP2 are explained in the following section. Simulation results for the mixer are provided at the end of this chapter.

4.2 Passive mixer topology

The mixer topology used in this design is a modification of the conventional passive mixer topology consisting of a switching core with current input and current output, followed by a TIA. The conventional passive mixer topology is as shown in figure 4.1. The TIA is used to convert the current output from the switching core into a voltage. This topology also results in a low mixer input impedance, which is a requirement for meeting the linearity requirements of the LNA that has been selected for this design.

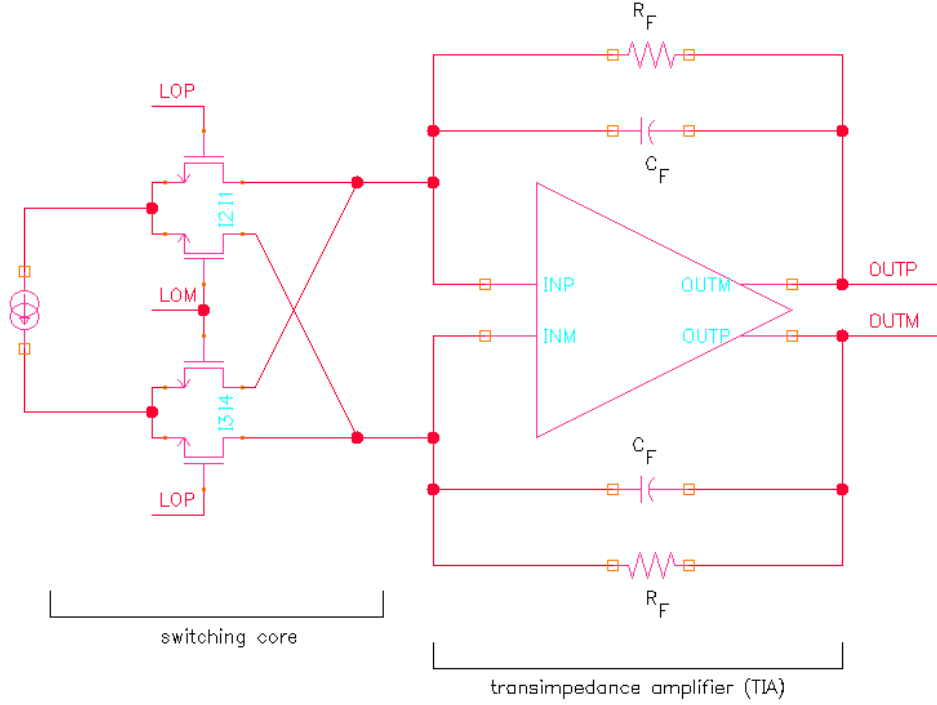


Figure 4.1: Schematic of conventional passive mixer

However, as will be shown next, the contribution of TIA to overall mixer noise is high in this topology.

4.2.1 Noise contribution of TIA in conventional passive mixer topology

As shown in [19], the NF of conventional passive mixer is high because of the high contribution of the TIA to overall mixer noise. let us now consider the conventional passive mixer topology shown again in figure 4.2, but now with more relevant details.

Let R_{MIX} be the impedance looking into the switching core as seen from terminals V_{GP} and V_{GM} . Considering only the noise of the opamp, the noise at the output of the TIA, $V_{no_TIA}^2$, is given by-

$$V_{no_TIA}^2 = \left(1 + \frac{R_F}{R_{MIX}/2}\right)^2 \cdot V_{ni_TIA}^2 \quad (4.1)$$

where $V_{ni_TIA}^2$ is the input referred noise of the opamp (Only voltage noise is considered, since the maximum frequency of the input signal to the TIA is 2MHz and the input impedance of the

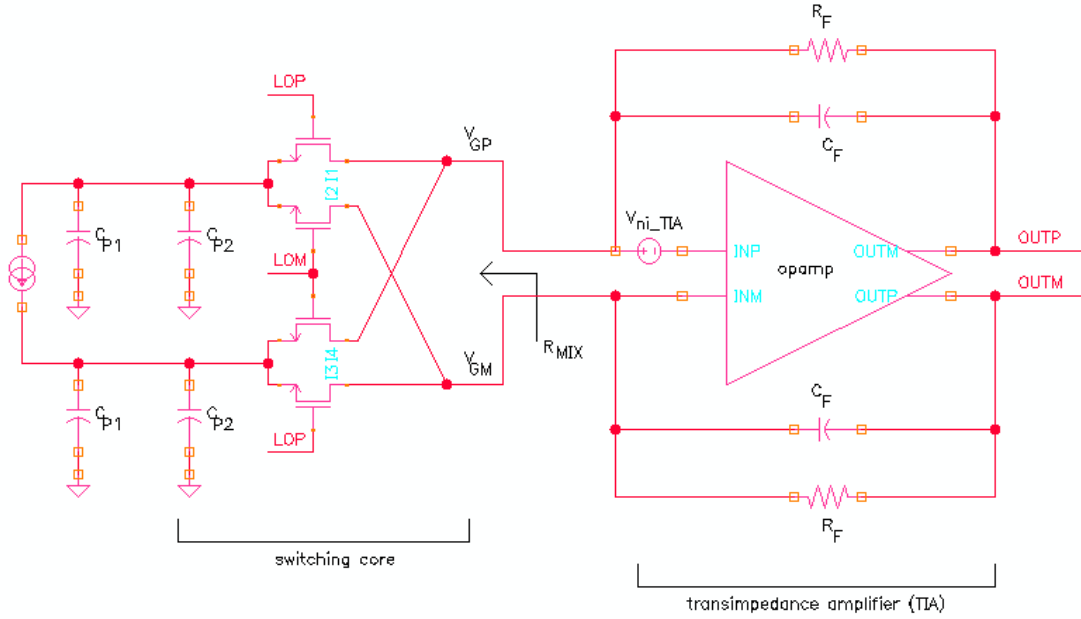


Figure 4.2: Noise contribution of TIA in conventional passive mixer

opamp will be high in this frequency range. When the input impedance of the opamp is high, the equivalent current noise at the input of the opamp can be neglected). $R_{MIX}/2$ is the impedance seen from each of the terminals V_{GP} and V_{GM} to ground and R_F is the feedback resistance. As can be seen from equation 4.1, R_{MIX} has to be as large as possible for TIA noise to be low. However the higher bound for R_{MIX} is determined by the operating frequency and the equivalent impedance offered by parasitic capacitances C_{P1} and C_{P2} due to their switching between the nodes V_{GP} and V_{GM} [19]. C_{p1} is the capacitance due to the switching core and C_{p2} is the output capacitance of the LNA. In [17], a series resistance has been added before the switching core to increase R_{MIX} . However this increases the input impedance of the mixer and affects the linearity of the LNA. A new approach to reduce noise contribution of TIA is presented in the next section.

4.2.2 A new approach to reduce noise contribution of the TIA

A current buffer can be used between the switching core and the TIA to reduce the noise contribution of the TIA. A current buffer has low input impedance and high output impedance. The low input impedance of the current buffer will help to keep the input impedance of the mixer low. High output impedance of the current buffer, increases the source impedance for the TIA and hence reduces the TIA noise contribution. However, the current buffer adds noise of its own, which should be kept low.

4.2.2.1 Current buffer

The schematic of the current buffer used in this design is as shown in figure 4.3. Common gate configuration has been used to implement the current buffer. Transistors TPLOADP and TPLOADM in combination with RPLOADP and RPLOADM act as current sources. Similarly transistors TNTAILP and TNTAILM in combination with RNTAILP and RNTAILM also act as current sources. The dominant noise contributors in the current buffer are these current sources. Resistive degeneration has been used to reduce the noise due to these current sources.

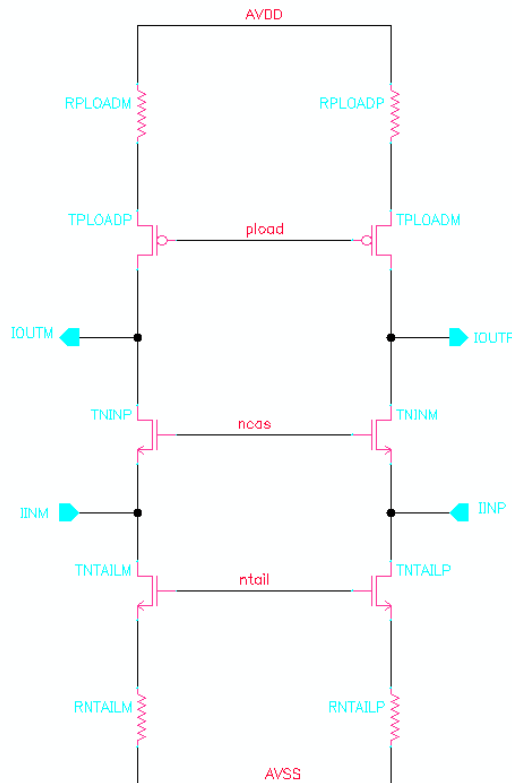


Figure 4.3: Schematic of current buffer

The effectiveness of the current buffer in reducing the noise contribution of the TIA can be seen in figure 4.4, where noise factor of the mixer (referred to LNA input) is compared with and without current buffer. It can be seen that noise factor reduction is significant at low frequencies. This is explained as follows: The size of the transistors in the opamp used to implement the TIA cannot be made very large, to keep the TIA circuit stable. So when no current buffer is used, the noise of the TIA is the dominant contributor to total mixer noise, in which the large $1/f$ noise of the TIA further dominates. When current buffer is used, the noise contribution of the TIA to total mixer noise is significantly reduced. However, the current buffer will add noise of its own. Since the current buffer is not part of a feedback loop, the sizes of transistors used in the current buffer can be made large to reduce their $1/f$ noise contribution. Thus the total $1/f$ noise due to current buffer and TIA

is much less when current buffer is used, when compared to the $1/f$ noise of the TIA alone, when no current buffer is used.

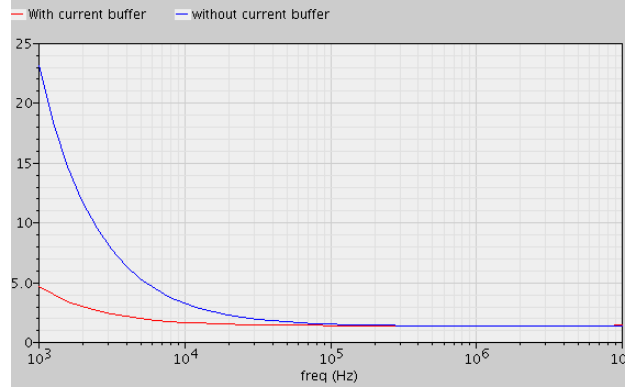


Figure 4.4: Comparison of noise factor of the mixer (referred to LNA input) with and without current buffer

At higher frequencies ($>100\text{KHz}$), the noise factor is almost the same with and without current buffer. This is due to the thermal noise contribution of the current buffer. The thermal noise contribution of the current buffer can be reduced only by increasing the degeneration resistances of the current sources or by reducing the DC bias current. The DC bias current has been chosen to guarantee the linearity requirements of the mixer in this design. The value of degeneration resistances is limited by the supply voltage. In designs using higher supply voltage, the noise reduction due to the use of current buffer will be more significant.

4.2.3 Complete schematic of the mixer

The complete schematic of the mixer is as shown in figure 4.5. The function of additional capacitors and level shifter shown in the schematic will be explained later in this chapter.

4.3 Design of the transimpedance amplifier

4.3.1 General considerations

The transimpedance amplifier (TIA) is used to convert the output current of the current buffer into voltage. The TIA should have low input impedance to minimize signal loss in the current buffer-TIA interface. Feedback topology shown in figure 4.6 has been used to implement the TIA.

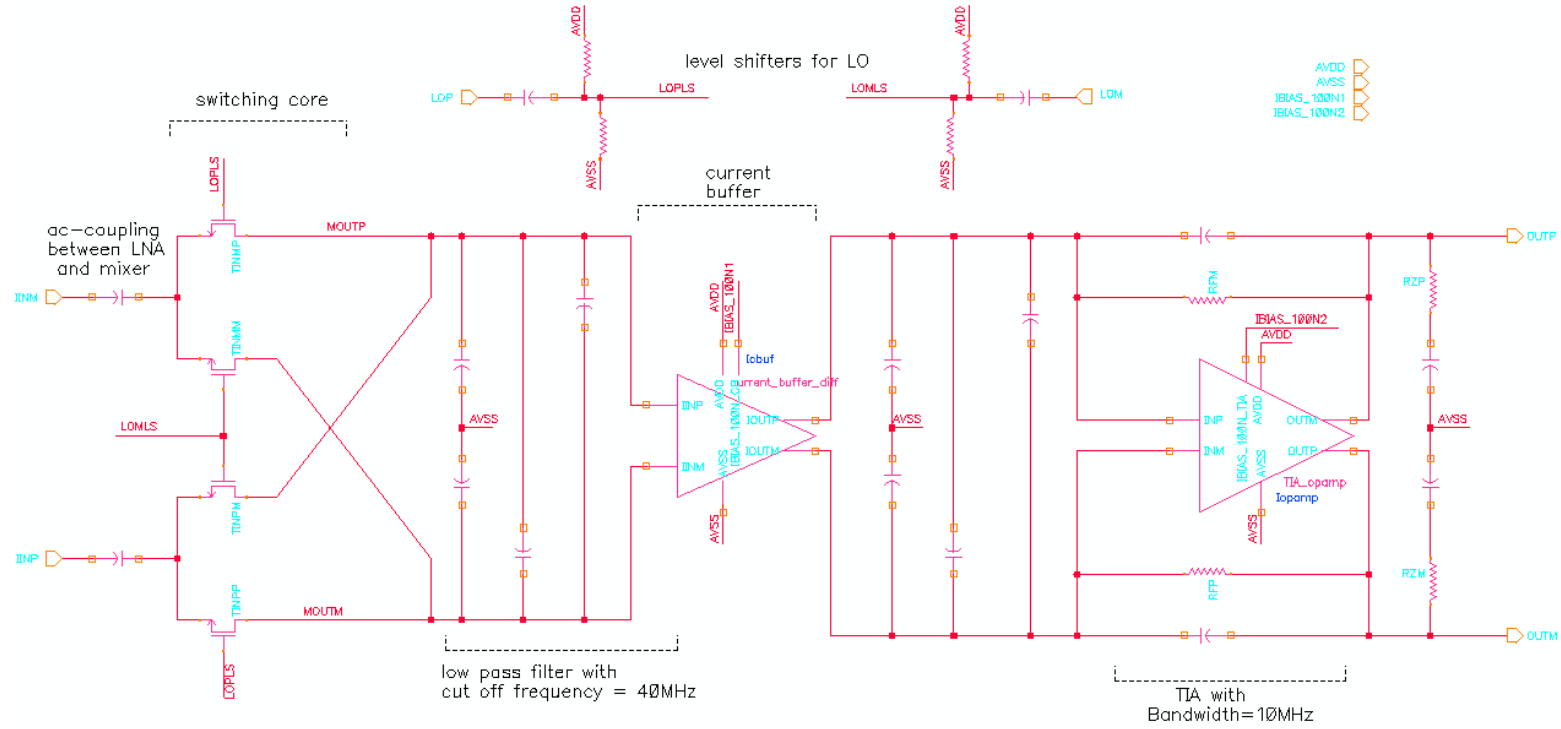


Figure 4.5: Complete schematic of the mixer (including level shifters for LO)

Assuming an ideal opamp, ideal current source drive and no loading at the output, the transfer function of this circuit is -

$$\frac{V_{out}}{I_{in}} = \frac{OUTP - OUTM}{I_{in}} = \frac{2R_F}{1 + sR_FC_F} \quad (4.2)$$

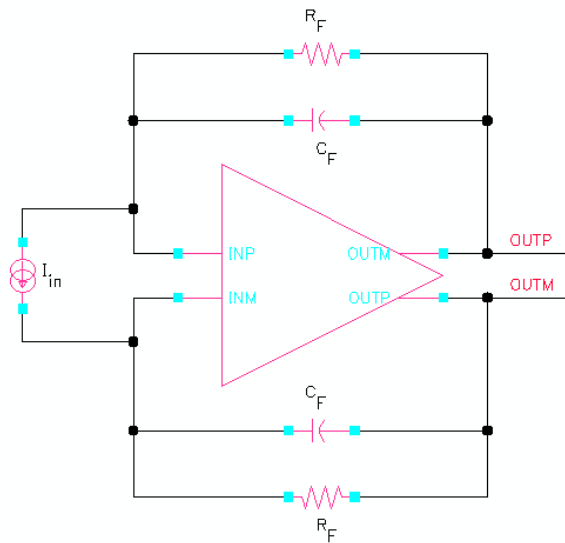


Figure 4.6: Feedback topology used to implement the TIA

As expected, the bandwidth of the TIA is decided by the time constant of the feedback network, when the opamp is ideal and when there is no additional loading at the input and output of the TIA.

As explained in chapter 2, a major source of interference in WCDMA is the leakage from the transmitter. While the power level of the desired input signal can be as low as -117dBm, the power level of the leakage signal from the transmitter at the input of the receiver can be as high as -25dBm. Since this high leakage signal can have severely limit the linearity of the receiver, it is important to filter these interfering signals as much as possible and as early in the receive chain as possible. The effectiveness of filtering depends on the separation between the transmit and receive bands. The separation between transmit and receive frequency bands can be as low as 45MHz (Band V). The LNA has been designed for frequencies from 800MHz to 2.2GHz to cover all WCDMA bands. Hence the filtering of the leakage signal from the transmitter cannot be carried out in the LNA. However, if this leakage signal is not filtered before the mixer output, then it can severely limit the gain that can be implemented in the LNA+mixer combination, since the voltage swing at the output of the mixer is limited. Also it can severely limit the linearity of the mixer. Therefore along with filtering the signal as much as possible before the TIA, the bandwidth of the TIA also has to be chosen just enough to have a flat response within the frequency band of the desired signal

and attenuate the interfering signals. The frequency band of the desired input signal is limited to 2MHz. However the TIA has to be designed for a higher bandwidth to maintain gain flatness and low phase delay in the desired frequency band. In this design the bandwidth of the TIA is chosen to be 10MHz.

4.3.2 Design of the TIA opamp

To maximize the gain that can be achieved in the transceiver, the TIA has to be designed for highest possible output swing. Common source topology was therefore chosen for the output stage of the TIA opamp. Without cascoding, the gain that can be achieved from a common source stage is small. Therefore a two-stage configuration was chosen for the opamp.

4.3.2.1 Pole zero analysis of TIA loop gain

The small-signal equivalent circuit of the TIA including the two-stage opamp is as shown in figure 4.7.

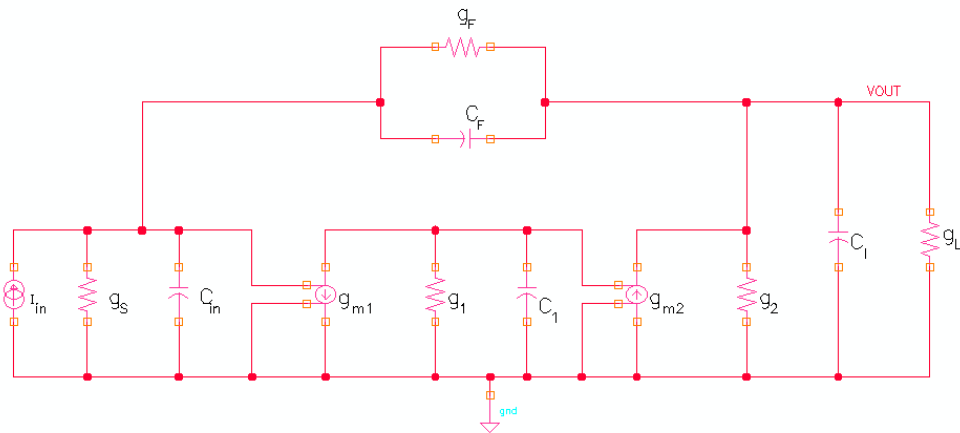


Figure 4.7: Small signal equivalent circuit of the TIA

g_{m1} and g_{m2} are the transconductances of first and second common source stages respectively. g_1 and g_2 are the respective output conductances. C_1 is the parasitic capacitance at the output of first stage. C_l is the total capacitance at the output of the TIA (including the additionally added capacitance for stability and parasitic output capacitance of the second stage). C_{in} is the total capacitance at the input of the TIA (including additionally added capacitance for stability and the parasitic output capacitance of the current buffer). g_s is the output conductance of the current buffer. g_L is the load to be driven by the mixer. g_F and C_F are the conductance and capacitance of the feedback network.

As explained in detail in appendix A, the loop gain of the circuit in figure 4.7 is best written in terms of the two-port y-parameters of the source, feedback network, opamp and load as -

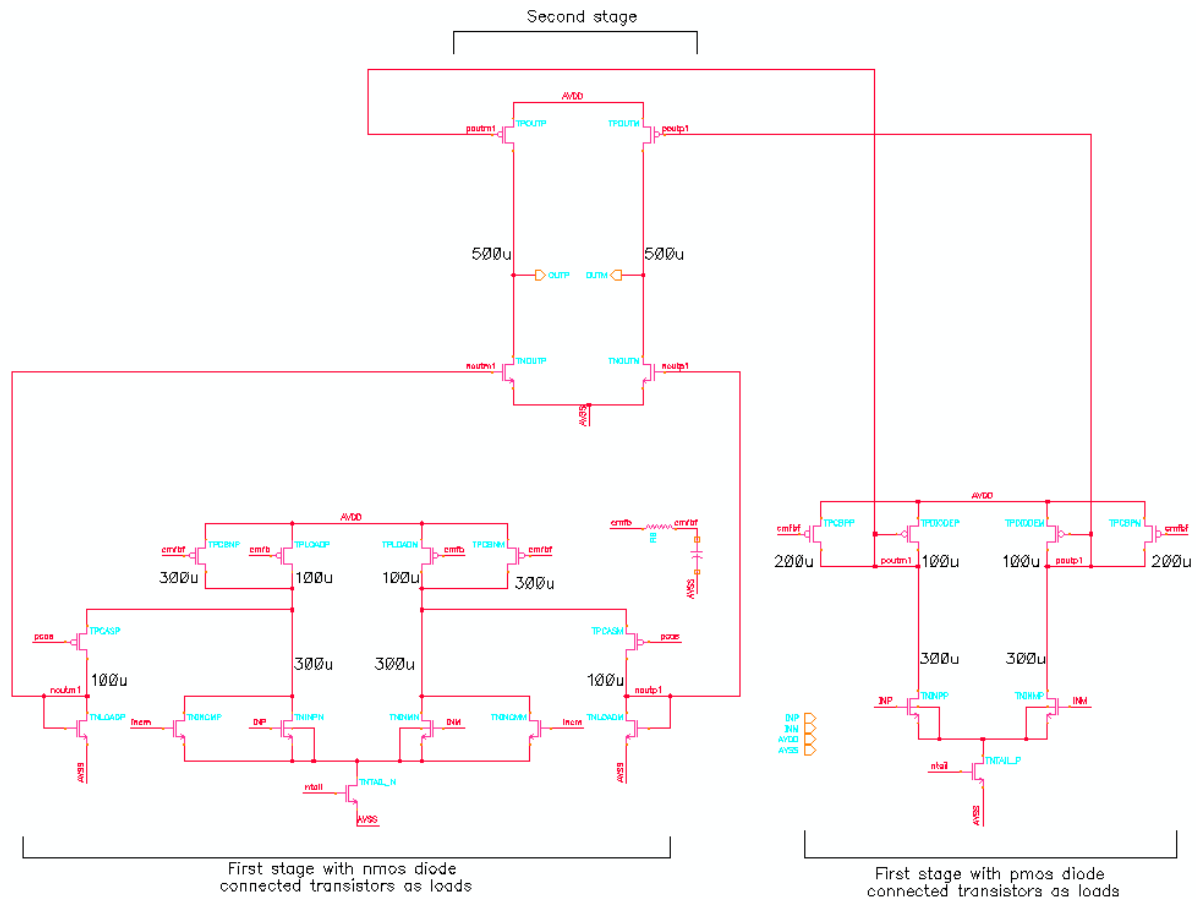
$$G_{loop} = \frac{(y_{FA} + y_{FF}) \times (y_{RA} + y_{RF})}{(y_{IA} + y_{IF} + y_{IS}) \times (y_{OA} + y_{OF} + y_{OL})} \quad (4.3)$$

where Y_I is the input admittance, Y_O is output admittance, Y_F is the feedforward transmission coefficient and Y_R is the reverse transmission coefficient. The second letter in the subscript refers to either the opamp(A), feedback network(F), source(S) or Load(L). In terms of the small signal parameters, the loop gain can be written as -

$$G_{loop} = - \frac{\left(\frac{g_{m1}g_{m2}}{g_1 + sC_1} - (g_f + sC_f) \right) (g_f + sC_f)}{(g_f + sC_f + g_s + sC_{in})(g_2 + sC_2 + g_f + sC_f + g_l + sC_l)} \quad (4.4)$$

we can see that there are 3 poles - one at the input (p_{in}), one at output (p_{out}) and one due to parasitic capacitance at the output of the first stage (p_1). When considering the 3 zeros, the position of one is directly related to the time constant of the feedback network (z_F). The other two zeros depend on g_{m1} , g_{m2} , p_1 and z_F . Of these two zeros, one will be in right half of s-plane (z_{rhp}) and other one in the left (z_{lhp}). Also the z_{rhp} occurs at a lower frequency compared to z_{lhp} . Thus this pair of zeros gives phase delay in addition to that due to the poles. To have a good phase margin, this pair of zeros has to be kept sufficiently outside the unity gain bandwidth(UGB) of the TIA. It was seen from MATLAB simulations, that the absolute value of z_{rhp} is close to p_1 . Therefore to keep z_{rhp} and z_{lhp} away from UGB, even p_1 has to be kept outside the UGB. Hence p_1 cannot be one of the dominant poles.

The input impedance looking into the TIA is the input impedance without feedback divided by the loop gain. In order to have a constant and low input impedance through out the desired signal band, the dominant poles of the loop gain have to be kept sufficiently away from the desired signal band. Since the bandwidth of the desired signal is 2MHz, the first dominant pole has been chosen to be at about 5MHz. The zero due to the feedback network (z_F) which is at about 10Mhz is used to approximately cancel the second dominant pole. These dominant poles are located at the input and output of the TIA respectively (p_{in} and p_{out}) and additional capacitors have been added at the input and output to set these poles to the desired frequency. Since the voltage swing at the output of the TIA is much higher than at the input, higher capacitance at the output of the TIA can only be supported by having a sufficiently high current in the output (second) stage of the TIA opamp. So to keep the total capacitance at the output and hence current requirement in the output stage as low as possible, the first dominant pole was chosen to be at the input of the TIA and second dominant pole at the output.



4.3.2.3 Checking loop gain and phase margin in simulation

The expression for loop gain of the TIA topology used in this design is as shown in equation 4.4. The two zeros in the loop gain z_{rhp} and z_{lhp} are due to feedforward transmission through the feedback network. If the simulation for loop gain is done by breaking the loop at the input of the TIA, then there is no longer any feedforward transmission through the feedback network and the effect of these two zeros will not be seen in the simulated transfer function. Therefore the feedforward transmission through the feedback network has to be carefully taken into account while computing the loop gain by breaking the loop. This can be done as shown in figure 4.9.

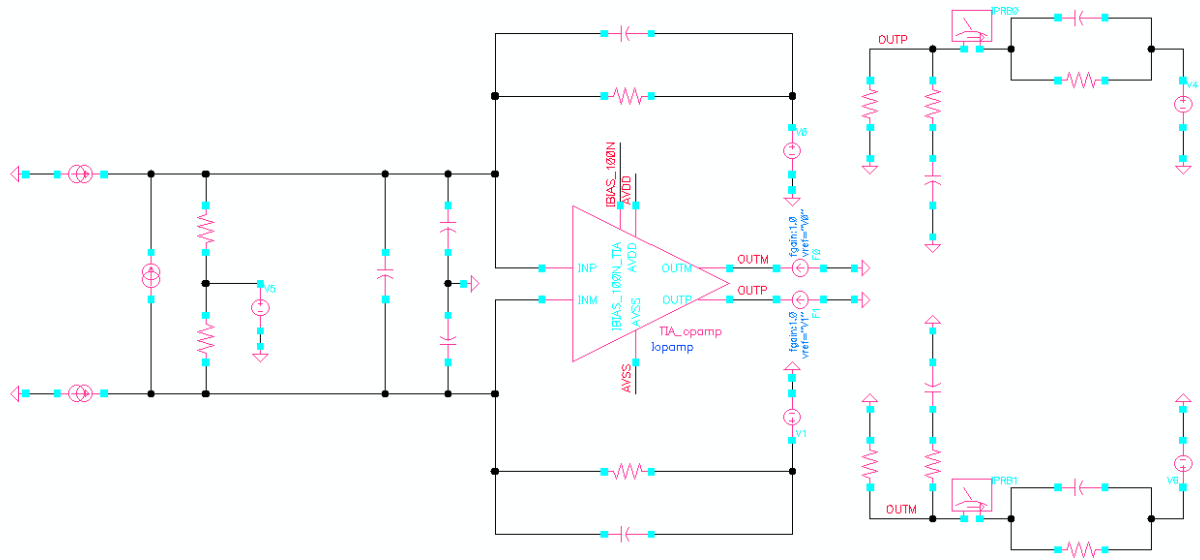


Figure 4.9: Schematic for simulation of loop gain of the TIA

Feedforward transmission through the feedback network is taken into account by duplicating the feedback network at the input of the TIA and measuring the current flowing through it using voltage sources V0 and V1. This current is then fed into the output nodes of the amplifier by using current controlled current sources F0 and F1. The bode plot of loop gain is as shown in figure 4.10. The loop gain at low frequency is 26dB and phase margin is 68.5° . The UGB of the opamp is 103.8MHz.

4.3.3 Complete schematic of TIA

The overall schematic of the TIA is as shown in figure 4.11. The resistor $R_z = 100\Omega$ has been placed in series with capacitor $C_l = 5p$ at the output of the TIA for common-mode stability as

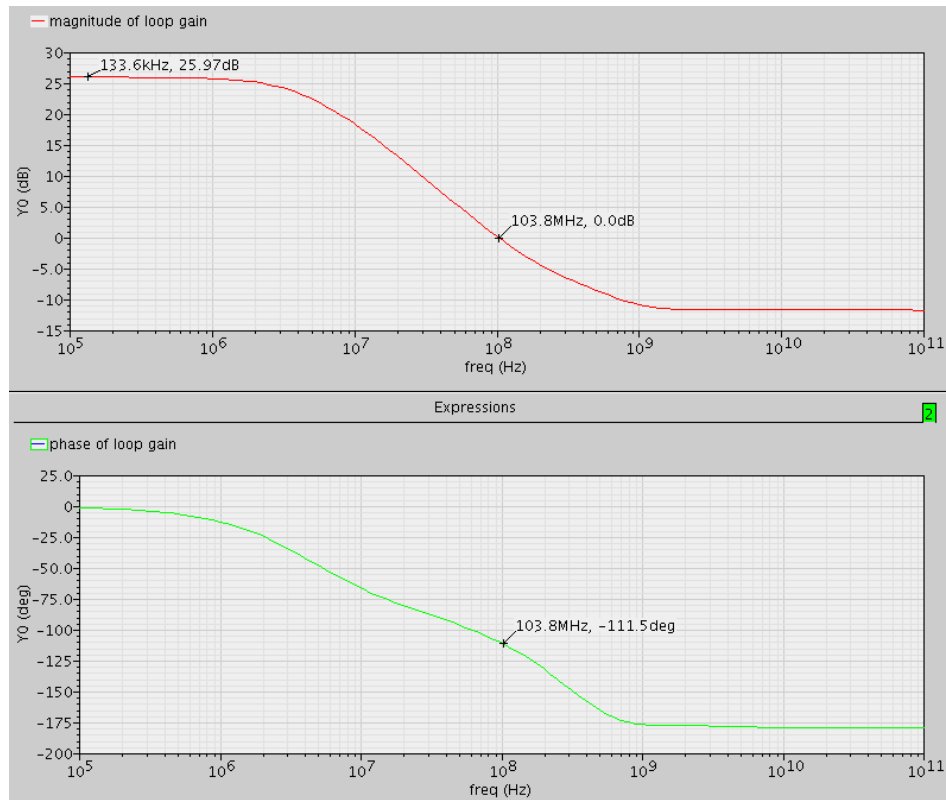


Figure 4.10: Bode Plot for computing the phase margin of the TIA

explained later. Presence of R_z introduces another pole and zero to the transfer function. However this pole and the zero lie so much outside the UGB, that they do not affect the differential mode stability of the TIA.

The initial specification for the single-ended output load of the TIA was 250Ω . However it was found during the design phase, that for the TIA topology shown in figure 4.6, the preferred loading is with a significantly higher load (A load of $5k\Omega$ has been chosen in this design). So it was decided to add a buffer after the TIA to drive a load of 250Ω , a situation, which is more optimum than designing the TIA itself to drive the low impedance load directly. This can be explained as follows: With a output load of $5k\Omega$, the effective resistance to ground at the output node is $R_F \parallel \frac{1}{g_2} \parallel \frac{1}{g_l} \approx 1k\Omega$. The total capacitance at that node is $C_l + C_F = 15pF$. Also as explained before, for stability, the pole at the output of the TIA (p_{out}) has to be lower or equal in frequency to the zero due to feedback network (z_F). If the output load is 250Ω , the capacitance at this node will have to be four times higher to obtain the same pole as that with output load of $1k\Omega$. Both the first and second stages of the TIA opamp will have to be scaled by approximately a factor of 5 to support this capacitance. Therefore, instead of burning this additional power in the TIA opamp, it will be more optimum to have a buffer after the TIA to drive the low load impedance of 250Ω . Also this buffer can be absorbed into the low pass filter, which usually follows the LNA and the mixer.

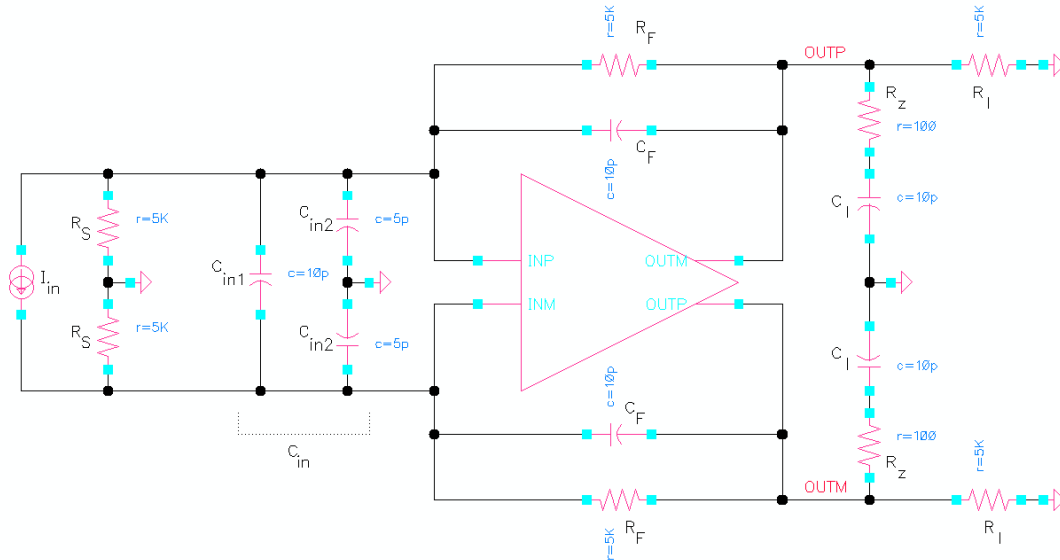


Figure 4.11: Overall schematic of the TIA with additional capacitors at the input and output.

4.3.4 Common-mode stability

A common-mode feedback loop has been used to set the output common-mode voltage. This is as shown in figure 4.12.

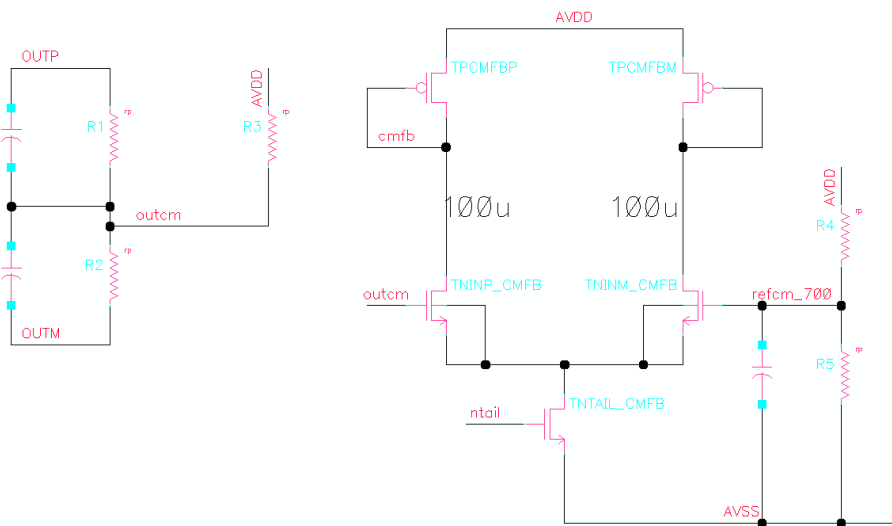


Figure 4.12: Common mode feedback loop for setting the output common-mode voltage of the TIA

The output common-mode voltage 'outcm' is measured using a resistive divider between OUTP and OUTM. Nominally this voltage will be set to 0.6V (half the supply voltage). To provide a higher input common-mode voltage for the cmfb amplifier, an additional resistor from supply is connected to 'outcm' node. With this, the common-mode voltage is raised to 0.7V. This is then compared to a reference level of 0.7V also derived from the supply using another resistive divider. The difference voltage is fed as the input to the cmfb amplifier and the output taken from the 'cmfb' node is used to adjust the currents in the TIA opamp as shown in figure 4.8.

For common-mode signals, referring to figure 4.11, $(C_F \parallel R_F)$ in series with $(C_{in2} \parallel R_s)$ appears as load at the output of the amplifier in addition to R_z in series with C_l . The pole at the input of the TIA does not appear in the expression of the loop gain for common-mode signals. The pole at the output of the amplifier is almost at the same location as that for differential mode signals ($\approx 10MHz$) and becomes the dominant pole, while the pole at the output of the first stage remains the non-dominant pole. None of the zeros in equation 4.4 appear in the expression of the loop gain for common-mode signals. Since the dominant pole for common-mode signals ($\approx 10MHz$) is at twice the frequency as that for differential mode ($\approx 5MHz$) and dc gain for common-mode signals is almost the same as that for differential mode signals, the UGB for common-mode signals will be twice as that for differential mode signals. However the position of non-dominant pole remains the same as in differential mode. This will degrade the phase margin of the common-mode feedback loop. Therefore a low-pass filter (with a cut off frequency of 3MHz) has been added as shown in figure 4.8 to kill the gain of the common-mode feedback loop at high frequencies. Also a resistance R_z has been added in series with C_l to introduce a zero. The low-pass filter and the added zero keep the negative feedback loop formed by the TIA opamp and the cmfb amplifier stable.

Analyzing the common-mode stability of the TIA is not a straight forward task since there are 2 feedback loops. One is the negative feedback loop through the cmfb amplifier and the other is the positive feedback loop formed by the TIA opamp and the feedback network consisting of R_F and C_F . Therefore the common-mode stability was ensured by checking the response of the TIA to a common-mode step voltage at the input. It should also be noted that the loop gain of the positive feedback loop will be low due to degeneration by the tail current source for common-mode signals in the first stage of the TIA opamp.

It can also be seen from figure 4.11, that if during startup, the output common-mode voltage of the TIA opamp is zero, then the positive common-mode feedback loop formed by the TIA opamp and the feedback network can sustain the output common-mode voltage at zero. This will happen even with the presence of negative feedback through the cmfb amplifier, because the input transistors will be off and there is no path for the tail current to flow. Therefore a startup circuit consisting of two NMOS transistors with their gates connected to a fixed 'incm' voltage has been added in parallel to the input transistors in the first stage of the TIA opamp. These transistors provide an alternate path for the tail current to flow, even when the input transistors are off, thus enabling the negative feedback through cmfb amplifier to function and restore the output common-mode voltage to the desired value. During the normal operation, these two transistors are off and do not affect the functionality of the circuit.

4.4 Choice of Local Oscillator (LO) waveform

4.4.1 sine wave versus square wave

Consider one of the single-ended output currents of the LNA. This current is fed to two transistors each in the I-mixer and Q-mixer as shown in figure 4.13. Ideally, in each mixer, at any given time, one of the two transistors should be completely on, while the other should be completely off. However, in reality, depending on the LO signal, there can be some overlap time, when either both transistors are on or both transistors are off. The transistors turn on when the LO voltage exceeds the sum of V_T and input common-mode voltage (V_{incm}) of the current buffer (input common-mode voltage of the TIA when no current buffer is used). If the LO common-mode is higher than this sum, then there is ON overlap between the two transistors. If the LO common-mode voltage is less than the sum, there is OFF overlap [19].

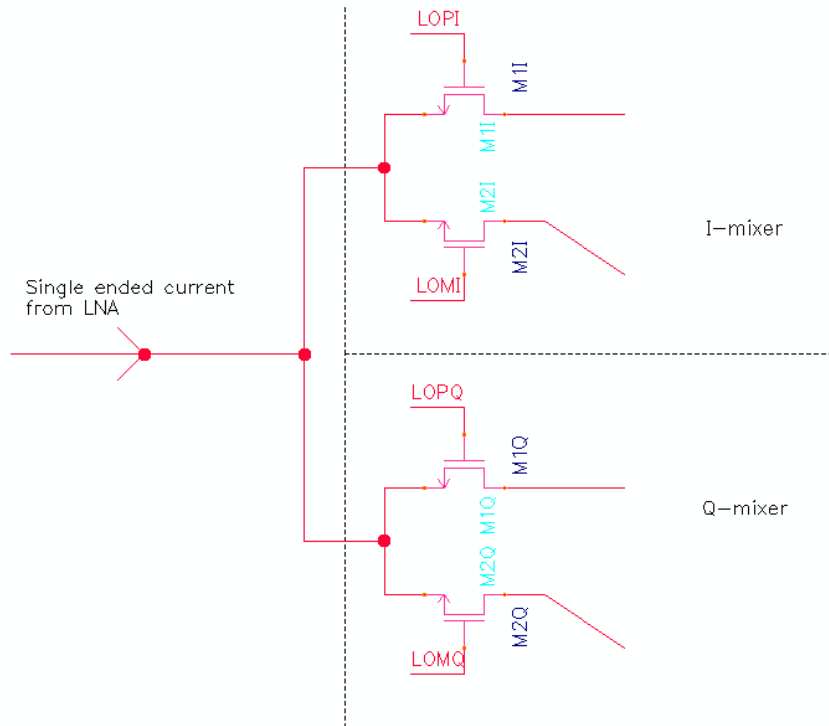


Figure 4.13: Current splitting in I and Q mixers

During ON overlap, in the absence of current buffer, there is an increase in TIA noise contribution, due to shorting of the input terminals of the TIA through the switching core transistors [19]. To analyze the effect of ON overlap in the presence of current buffer, let us consider the simplified representation of the I/Q mixer as shown in figure 4.14. Only the switching core and the current buffer have been shown in each of the mixers. The current sources in the current buffer have been

represented by symbols for current source for simplicity.

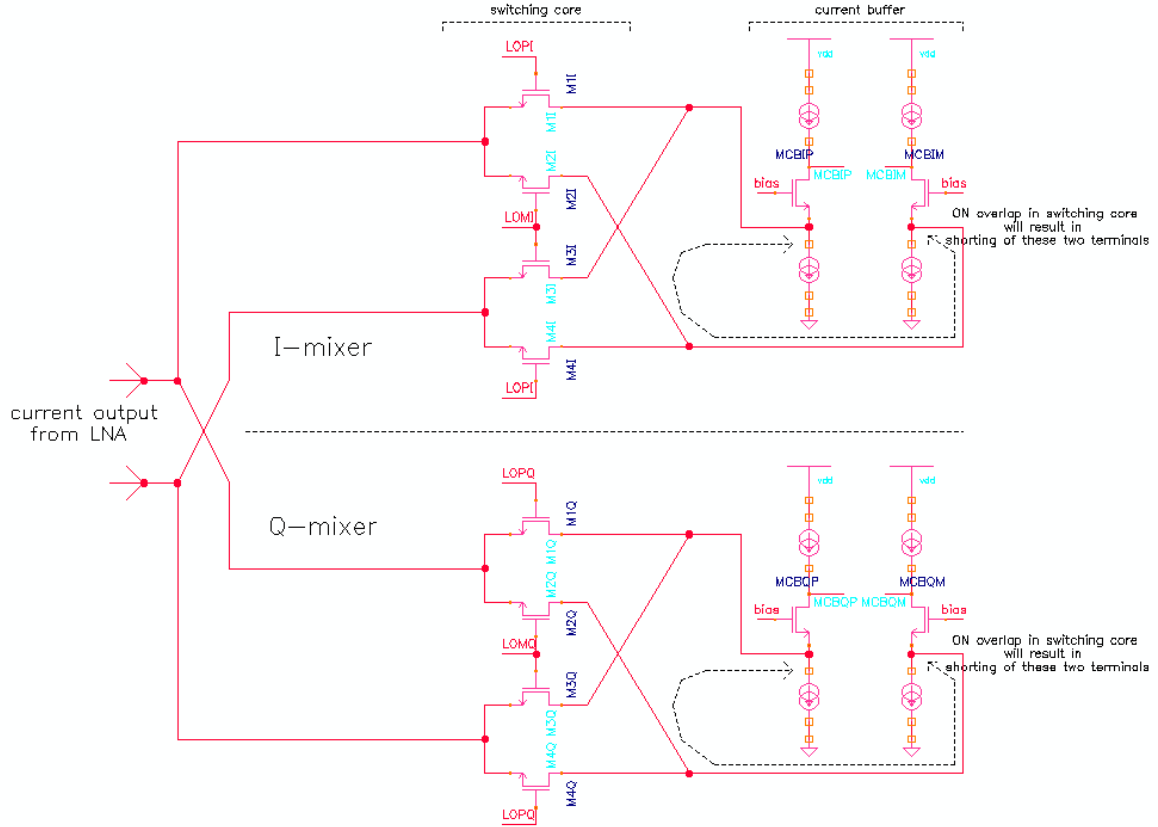


Figure 4.14: Increase in mixer noise due to ON overlap between transistors in switching core

As can be seen from the figure, in the presence of current buffer, ON overlap will result in shorting of the source terminals of the two input transistors of the current buffer. During normal operation, as explained in section 4.2.2, the dominant noise contributors in the current buffer are the degenerated current sources. However, when source terminals of the input transistors are shorted through switching core, even the input transistors (MCBIP, MCBIM in I-mixer and MCBQP, MCBQM in Q-mixer) contribute to noise, resulting in overall increase in mixer noise. Hence, when sinusoidal LO signal is used, care has to be taken to ensure that the common-mode level of the LO is less than $V_T + V_{incm}$. However if the common-mode level of LO is too low compared to $V_T + V_{incm}$, then the ON time of the transistors reduces, resulting in reduction of the gain of the mixer. Therefore the optimum condition is when the LO common-mode is only slightly lower than $V_T + V_{incm}$. However, it is not easy to ensure this condition since V_T varies with process corner and temperature.

Use of square wave LO signal reduces this problem to some extent since the ON overlap is now decided only by the rise and fall times, which can be made very small. Also, with a small amount of additional circuitry, the LO signals can be made non-overlapping with slightly less than 50% duty cycle. With this the noise increase due to ON overlap can be completely eliminated. Therefore

square wave LO signals have been preferred in this design.

4.4.2 Effect of LO duty cycle on mixer gain

It is possible to get close to 3dB improvement in gain of a current driven passive I/Q mixer combination, when 25% duty cycle LO signals are used as compared to 50% duty-cycle LO [1]. This is explained in brief here. Figures 4.15(a) and 4.15(b) show LO waveforms with 50% duty-cycle and 25% duty-cycle respectively. The instants when respective transistors shown in figure 4.13 are on is also shown in figures 4.15(a) and 4.15(b).

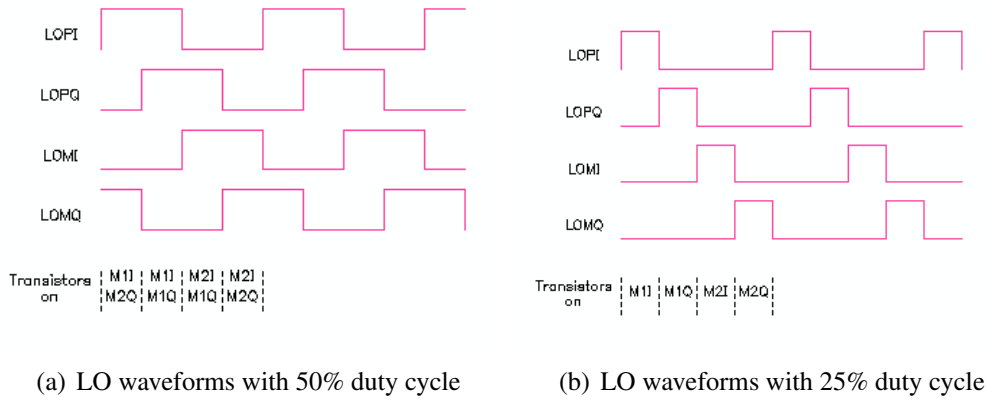


Figure 4.15: Comparison of LO waveforms with 50% and 25% duty cycle

With 50% duty cycle LO, the current from LNA always splits equally between the I and Q mixers since, at any given instant one transistor is on in both these mixers. The current entering each of the mixers is effectively multiplied by a pulse train of 1,-1 repeating every LO cycle. This pulse train can be represented using Fourier series as -

$$F_{50\%}(t) = \frac{4}{\pi} \left[\cos \omega_{LO} t - \frac{1}{3} \cos 3 \omega_{LO} t + \frac{1}{5} \cos 5 \omega_{LO} t - \dots \right] \quad (4.5)$$

Therefore the magnitude of the desired difference frequency current signal can be written as -

$$I_{IF} = \frac{2}{\pi} [\cos \omega_{LO} t] \times \frac{I_{LNA}}{2} \quad (4.6)$$

where the factor $\frac{2}{\pi}$, instead of $\frac{4}{\pi}$, accounts for equal splitting of the signal current from the LNA into sum and difference frequencies after mixing with the LO, I_{LNA} is the output current of the LNA and $\frac{I_{LNA}}{2}$ accounts for equal splitting of this current between the I and Q mixers.

Now with 25% duty cycle LO, we can see that only one of the four transistors shown in figure 4.13 is on at any given time. So the entire output current from the LNA flows through this transistor. This current is effective multiplied by the pulse train 1,0,-1,0 repeating every LO cycle. This pulse train can be represented using Fourier series as -

$$F_{25\%}(t) = \frac{2\sqrt{2}}{\pi} [\cos\omega_{LO}t + \frac{1}{3}\cos3\omega_{LO}t - \frac{1}{5}\cos5\omega_{LO}t + \dots] \quad (4.7)$$

Therefore the magnitude of the desired difference frequency current signal can be written as -

$$I_{IF} = \frac{\sqrt{2}}{\pi} [\cos\omega_{LO}t] \times I_{LNA} \quad (4.8)$$

Comparing equations 4.6 and 4.8 we can see that theoretically 3dB higher gain can be achieved when 25% duty cycle LO is used. However due to non-zero rise and fall times of the clock, the actual improvement in gain will be slightly smaller than 3dB. Nevertheless, the higher gain that can be achieved with 25% duty cycle LO helps to reduce the NF of the mixer. Therefore 25% duty cycle LO has been chosen for this design. Also a level shifter as shown in figure 4.5 is used to level shift the clocks from 0V - 1.2V levels to 0.5V - 1.5V levels. Since the input common-mode voltage of the current buffer is 0.5V, level shifting increases $V_{GS} - V_T$ for the switches and hence reduces their ON resistance. Since 1.5V transistors have been used in the switching core, the high level for the clocks has been limited to 1.5V.

4.4.3 Additional advantages of 25% duty cycle LO

In addition to the close to 3dB improvement in gain as explained in previous section, there are a few more advantages of using 25% duty cycle LO. They are:

1. When 50% duty cycle LO is used, at any given time, the LNA output node is connected to two ON transistors, one in each of the I and Q mixers. Referring to figure 4.14, this leads to shorting of the source terminal of one of the input transistors in the current buffer of I mixer

with the source terminal of one of the input transistors in the current buffer of Q mixer. This increases the overall noise of each of these mixers in the same manner as explained in section 4.4.1. When 25% duty cycle LO is used, the LNA output node is connected to only one ON transistor at a time and this problem no longer exists.

2. It was found in simulations that when both I and Q mixers are connected to the LNA and 50% duty cycle LO is used, the voltage at the output of the each of the mixers drops by about 12dB, when compared to the voltage when only one of the mixers is connected. This is 6dB higher than expected drop in voltage due to equal splitting of the LNA current between the two mixers. Although this problem was traced to lack of isolation between the two mixers, not much time was spent on identifying the root cause. However, when 25% duty cycle LO is used, at any given time the LNA current flows into only one of the mixers. Thus the mixers are isolated in time and this problem is not seen.
3. Parasitic capacitance at the input of the switching core degrades the IIP2 of the mixer in the presence of mismatch in the switching core [20]. When 25% duty cycle LO is used, only one of the four transistors shown in figure 4.13 is ON at any given time. This reduces the capacitance at the input of the switching core, when compared to using 50% duty cycle LO, during which two transistors will be ON at any given time. The reduction in capacitance in turn improves the IIP2 of the mixer [1].

4.5 25% duty cycle LO generation

A clock generation circuit has been designed that uses a sinusoidal signal at two times the LO frequency ($2f_{LO}$) and generates four non-overlapping clocks at f_{LO} of approximately 25% duty cycle each. The complete schematic is as shown in figure 4.16. The input sine wave is first fed to a Schmitt trigger to generate a square wave. The Schmitt trigger also helps to reject any noise in the input sine wave and generate a clean square wave signal. The schematic of the Schmitt trigger is as shown in figure 4.17. The output of the Schmitt trigger is shown in figure 4.18.

The buffered output of the Schmitt trigger is then fed to a non-overlapping clock generator. The schematic of the non-overlapping clock generator is as shown in figure 4.19. This circuit accepts a square wave as input and generates two non-overlapping clocks as shown in figure 4.18. The output of the Schmitt trigger is also fed to a divide by 2 circuit implemented using D-flip flop configured in toggle mode. The outputs of the divide by 2 circuit and the non-overlapping clock generator are then combined using logic gates to generate 4 non-overlapping clocks at approximately 25% duty cycle as shown in figure 4.20

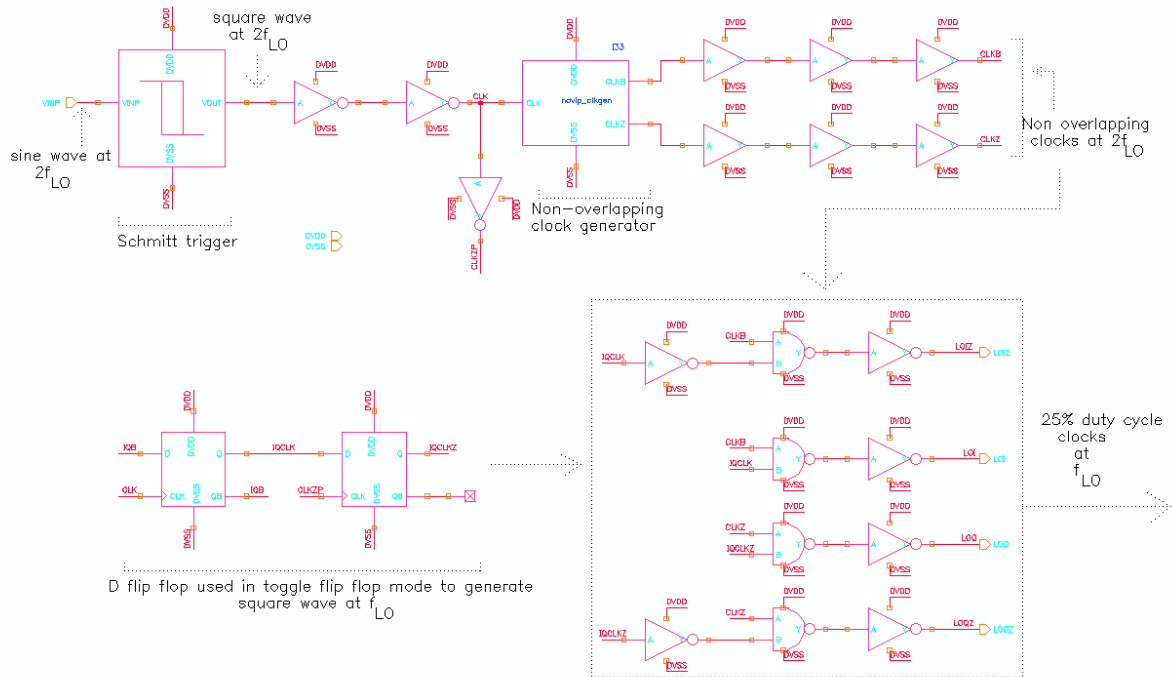


Figure 4.16: Schematic of clock generation circuit

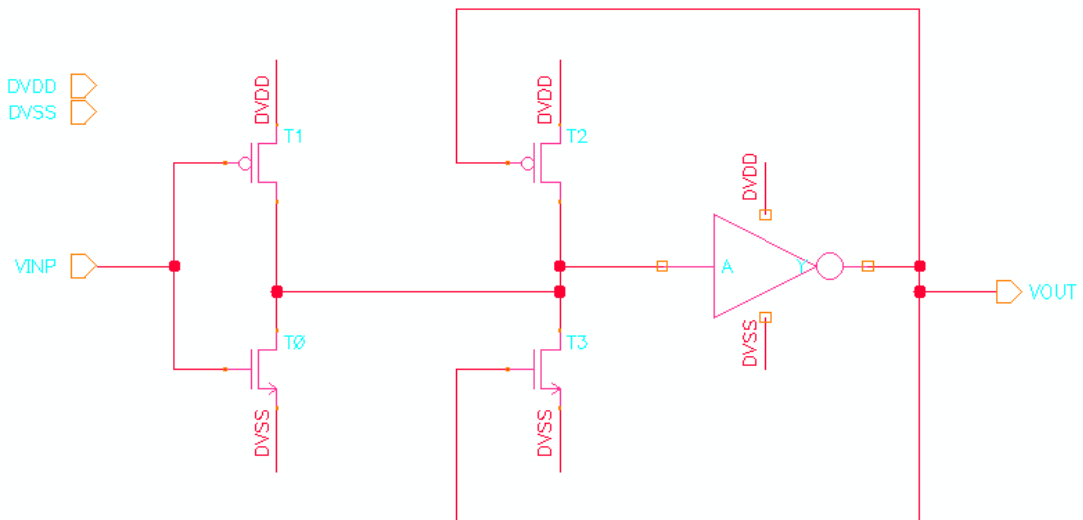


Figure 4.17: Schmitt trigger schematic

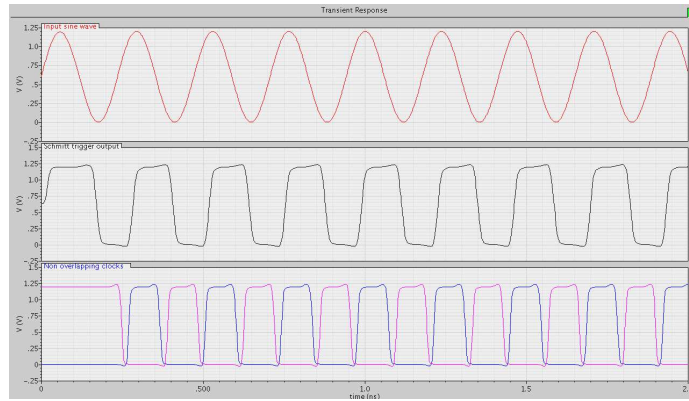


Figure 4.18: Waveforms at the input of Schmitt trigger, output of Schmitt trigger and output of non-overlapping clock generator respectively

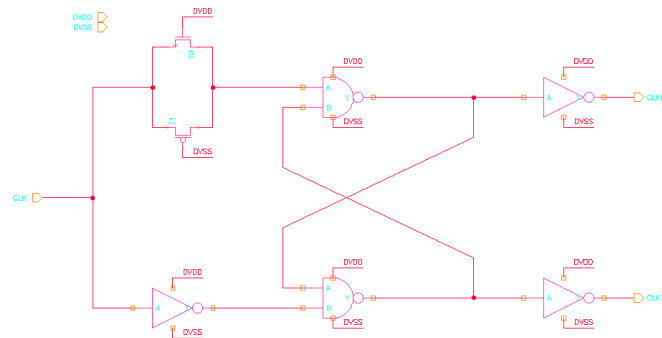


Figure 4.19: Non-overlapping clock generation circuit

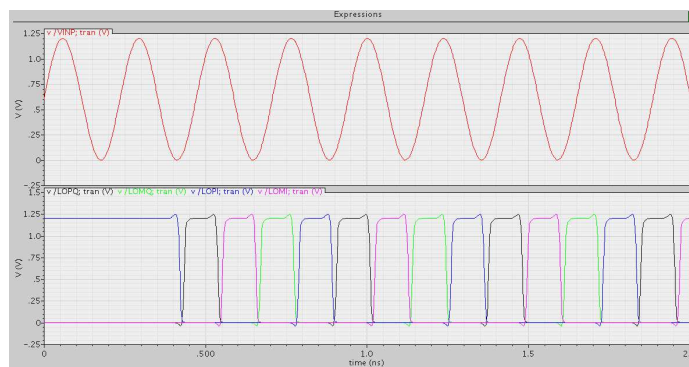


Figure 4.20: Final outputs of the clock generation circuit (four non-overlapping clocks of approximately 25% duty cycle generated from single input sinewave at $(2f_{LO})$)

4.6 Design of the mixer to meet the stringent IIP2 requirement

As explained in chapter 2, the IIP2 requirement of the transceiver at transmit frequency offset is minimum of 50dBm. This is a very stringent requirement. To meet this requirement both the LNA and the mixer have been designed to be fully differential. In the ideal case, there is no second order distortion from a fully differential circuit and hence infinite IIP2 can be obtained. However, in reality, random mismatch between devices will determine the IIP2 that can be obtained. Since, direct down conversion architecture is used in this design, only the low frequency components produced by second order distortion are of interest. Also, since ac coupling is used between the LNA and mixer, the low frequency components produced in the LNA are highly attenuated. The IIP2 of the LNA+mixer combination is thus mainly determined by the mismatch in the mixer alone.

It has been shown in [21], that passive mixers can achieve a much higher IIP2 than active mixers. Therefore using a passive mixer has been one of the critical design choices, which enabled the design of this mixer for the required high IIP2.

In [18], it has been shown, that square wave LO, reduces the RF-to-IF leakage due to mismatches in the switching core, when compared to sinewave LO. This in turn reduces the leakage to the mixer output, of any low-frequency IM2 component present in the mixer input. During this design, it was also seen that square wave LO improves the IIP2 in the presence of mismatch, even when only the non-linearity of the switching core transistors is considered (i.e when an ideal and linear model is used for the LNA). This can be explained as follows: During the time when the switching core transistors are in the transition region between completely OFF and completely ON states, the effect of mismatch between them on mixer IIP2 is higher than when the transistors are completely ON. When a sinewave LO is used, the switching core transistors spend more time in the transition state than when a square wave LO is used. Therefore square wave LO results in higher IIP2, even when the IM2 distortion is mainly from the non-linearity of the switching core transistors itself.

Non-equal duty cycle of LO waveforms can also degrade the IIP2 of the mixer. In this design, the two square wave LO signals used in each of the mixers are intended to be of approximately 25% duty cycle each and separated in time by one half of LO period. A sinusoidal signal at twice the LO frequency is used as input signal to generate these square wave LO signals. Therefore the two LO signals are generated from the same phase of the input sinewave signal but in alternate periods. The duty cycle of the two LO signals will therefore always be same, even if the two pulses generated in each period of the input sinewave by the combination of Schmitt-trigger and non-overlapping clock generator are not of equal duty cycle. This non-ideality can only make the duty cycle of both the LO signals different from 25%, but will still keep the duty cycle of these two signals the same.

Random mismatch between devices can be reduced only by using large gate lengths and hence large gate widths for the transistors in all the circuit blocks of the mixer namely switching core, current buffer and TIA opamp. However as explained in section 4.2, increasing the size of transistors in the switching core will increase the parasitic capacitance C_{p2} due to the switching core. Without current buffer, this reduces the effective resistance looking into the switching core and

hence increases the noise contribution of the TIA. However, in the presence of the current buffer this capacitance will have no effect on the TIA noise contribution and hence the sizes of transistors used in the switching core can be increased to improve their matching. The size will only be limited by the switching speed that is required and also the maximum power that can be dissipated in the clock buffers (LO buffer) used for driving the switching core.

Increasing the sizes of transistors in the current buffer not only improves the matching but also provides two more advantages. Mixer noise at low frequencies is dominated by the flicker noise of the current sources used in the current buffer as explained in section 4.2.2. Increasing the sizes of transistors in the current buffer helps to reduce this flicker noise. Also using larger lengths for transistors in the current buffer increases the output impedance and hence increases the impedance looking into the current buffer-switching core combination. This reduces the noise amplification of the TIA as explained in section 4.2.2.

However, in the TIA opamp, increasing the sizes of transistors increases the parasitic capacitance at the output of the first stage. This brings the pole associated with this node closer to the origin and reduces the stability of the TIA as explained in section 4.3.2.1. Therefore the dc gain in the TIA opamp has to be kept low to keep the UGB much lower compared to the frequency of the pole.

The complete schematic of each of the I and Q mixers is shown in figure 4.5. Additional capacitors added after the switching core provide a bypass path for high frequency current components produced after mixing. With a cut-off frequency of 40MHz, about 4dB of attenuation is also provided at transmit frequency offset in Band V (45MHz). Further attenuation of these components is provided by the capacitors added at the input of the TIA and by the transfer function of the TIA itself where the bandwidth is limited to 10MHz. These filtering operations are also critical to obtain the high IIP2 required in this design. In Band I, with transmit frequency offset of 190MHz, the attenuation at this frequency is higher and hence the IIP2 obtained is much better than the required specification of 50dBm.

The mismatch simulation done to measure the IIP2 of the mixer is explained in section 4.7.5. Care has also been taken in layout to ensure matching of critical transistors by ensuring same environment around the transistors to be matched. Dummy transistors have also been used in layout, wherever required to ensure matching.

4.7 Mixer simulation results

Nominal, fast and slow process corners were considered for simulations. Also temperatures 0°C, 27°C and 100°C have been considered. To reduce the total number of possible combinations of process corners and temperature, following combinations were chosen - nominal 25, fast 100, fast 0, slow 100 and slow 0. Monte Carlo simulations done for estimating IIP2 due to device mismatch also take into account process corner variations. Many simulation iterations have to be

done to get an estimate of IIP2 due to mismatch. Since each set of iterations take a very long time, IIP2 simulation has been done only at 25°C . Also simulations have been done only in Band I (2.12GHz) and Band V (880 MHz). The performance in Band II (1.96GHz) is expected to be close to that of Band I.

The mixer used in this design takes current as input and provides voltage as output. However the performance of most of the mixers reported in literature is for voltage input and voltage output (In designs using switching core with current input and current output, a transconductance is usually added before the switching core. In this design, however, the LNA provides current output and can be directly interfaced with the mixer. Also the performance of the mixer depends on the source impedance provided by the LNA. Therefore, for accuracy, in all the simulations for the mixer, an ideal model for the LNA has been used. The components used for the ideal model match the transconductance and output impedance of the LNA. Also for ease of reporting of the results and for ease of comparison with results reported in literature, all results are reported referred back to LNA input.

The test bench used for simulating the mixer is as shown in figure 4.21.

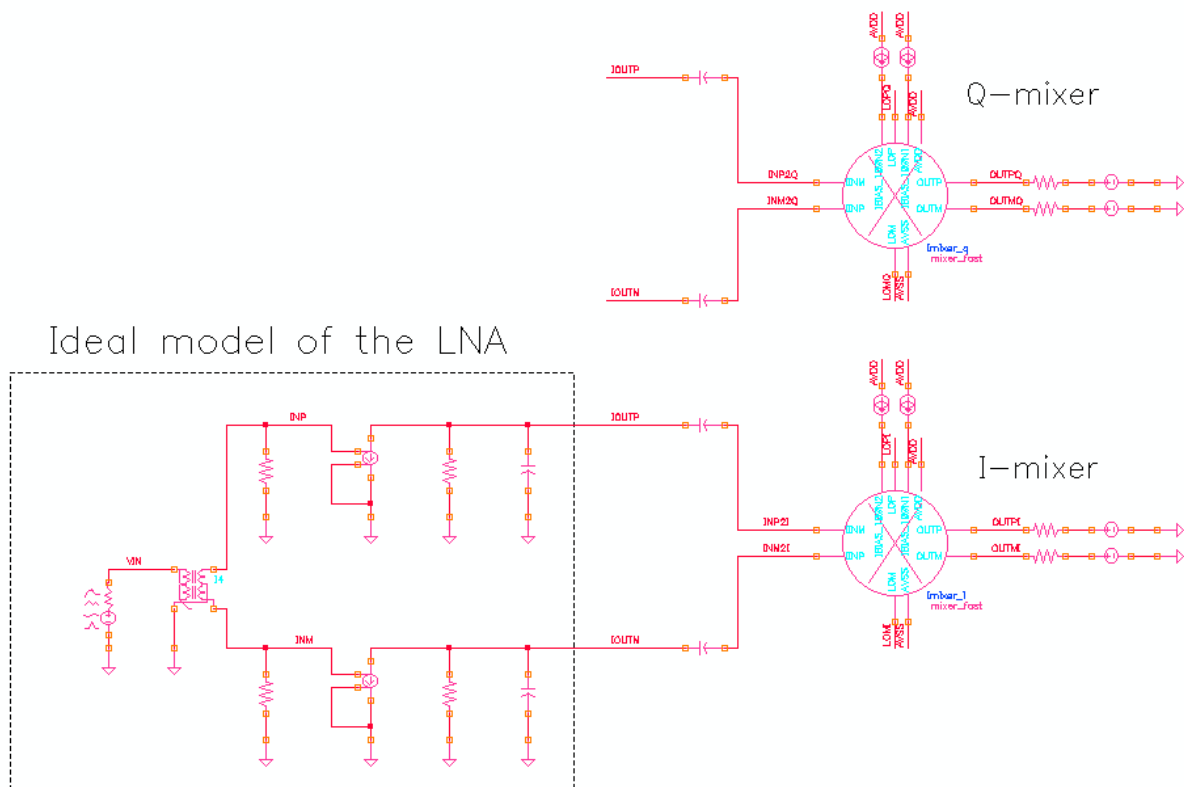


Figure 4.21: Test bench used for simulating the mixer

4.7.1 Power consumption

Each of the I/Q mixers consume 6mA current from 1.2V supply. The main circuits consume only 4.75mA, with 2mA being consumed in the current buffer and remaining in the TIA. The remaining 1.25mA of current is used for biasing in the current buffer and the TIA.

4.7.2 Gain

To check the gain of the LNA+Mixer combination, a single tone of -32dBm w.r.t. 100Ω (-39dB in terms of voltage) is used as input. This power level was chosen for the input signal, since it results in maximum tolerable voltage swing at the output of the mixer. The frequency of the single tone is 2.121GHz for Band I and 881MHz for Band V. The LO frequency for Band I is 2.12GHz and 880MHz for Band V. The spectrum of the output in Band I for nominal 25°C is as shown in figure 4.22. This shows that the gain of the combination is 35.51dB. The gains for Band I and Band V for different simulation corners are as shown in table 4.1

Table 4.1: Gain of LNA(ideal)+mixer combination (dB)

Band	Nominal 25°C	Fast 0°C	Fast 100°C	Slow 0°C	Slow 100°C
I	35.51	35.86	35.05	35.61	34.71
V	36.72	36.95	36.38	36.80	36.18

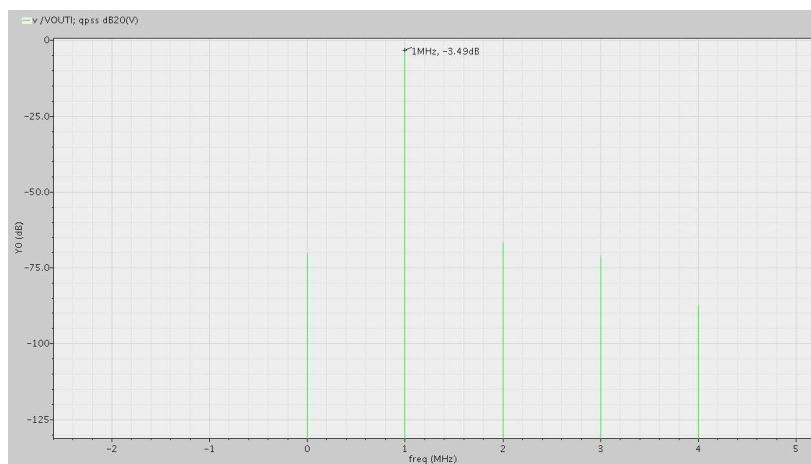


Figure 4.22: Spectrum used for computing the gain of LNA(Ideal)+mixer combination in Band I (nominal 25°C)

4.7.3 Noise Figure

Usually a combination of high-pass and low-pass filtering is done after the mixer. High-pass filtering is used to remove any DC. Therefore the lower cutoff frequency for measuring noise has been chosen to be 1kHz in this design. Also the maximum frequency occupied by the desired signal is 2MHz. Since the average noise over the entire frequency band is of interest, the average noise factor (NF_{avg}) is computed as follows -

$$NF_{avg} = \frac{\int_{1KHz}^{2MHz} \text{spot noise factor}}{2MHz} \quad (4.9)$$

The noise figure is then computed as $NF_{dB} = 10\log_{10}NF_{avg}$. The spot noise factor of the mixer from 1KHz to 2Mhz in Band I at nominal $25^{\circ}C$ is as shown in figure 4.23. The NF_{dB} in Bands I and V at different simulation corners are as shown in table 4.2.

Table 4.2: Average Noise Figure(dB) of mixer referred to LNA input

Band	Nominal $25^{\circ}C$	Fast $0^{\circ}C$	Fast $100^{\circ}C$	Slow $0^{\circ}C$	Slow $100^{\circ}C$
I	1.33	1.29	1.50	1.28	1.50
V	1.22	1.20	1.32	1.18	1.31

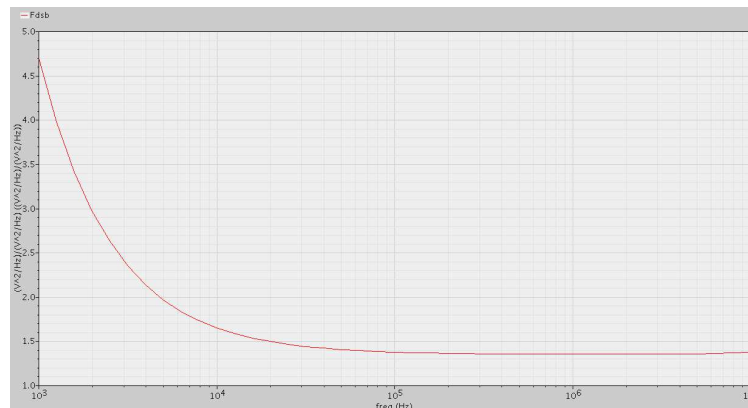


Figure 4.23: Spot noise Factor of the mixer in Band I (nominal $25^{\circ}C$)

4.7.4 Out-of-band IIP3

As mentioned in section 4.3.1, leakage from transmitter is the largest source of interference in WCDMA. In addition to this leakage, if there is any interfering signal at half the frequency sepa-

ration between transmit and receive bands, third order intermodulation can produce spurious components within the desired band. Out-of-band IIP3 is used to quantify the extent of performance degradation that can be caused by this interference.

In Band I, the frequency separation between transmit and receive bands is 190MHz (45Mhz in Band V). To measure out-of-band IIP3 in Band I, two tones at frequency offsets of 189MHz and 90MHz (43MHz and 22MHz in Band V) from LO frequency, with power levels of -25dBm and -50dBm respectively were used as the input. Since the tone nearer to the desired band has higher influence on the third order spurious component, the effective input power level can be calculated as $\frac{1}{3} \times (-25) + \frac{2}{3} \times (-50) = -41.7dBm$ w.r.t to 100Ω. Equivalent voltage level is -48.7dB. The spectrum of the output is shown in figure 4.24. We can see that the voltage level of the spurious 1MHz signal is -101.5dB. Referred to input (with a gain of 35.5dB) the level of spurious signal is -137dB. The IIP3 can now be calculated as $-41.7 + \frac{1}{2} \times (-48.7 - (-137)) = 2.46dBm$. Out-of-band IIP3 in Bands I and V in different simulation corners is as shown in table 4.3. As can be seen from table 4.3, IIP3 is higher in Band1. This is because, the frequency separation between transmit and receive bands is higher in Band I and hence the interfering signals experience higher filtering compared to the interfering signals in Band V.

Table 4.3: Out-of-band IIP3 (dBm) of mixer (referred to LNA input)

Band	Nominal 25°C	Fast 0°C	Fast 100°C	Slow 0°C	Slow 100°C
I	2.46	2.77	3.56	2.06	2.63
V	-5.19	-5.27	-4.4	-5.68	-4.58

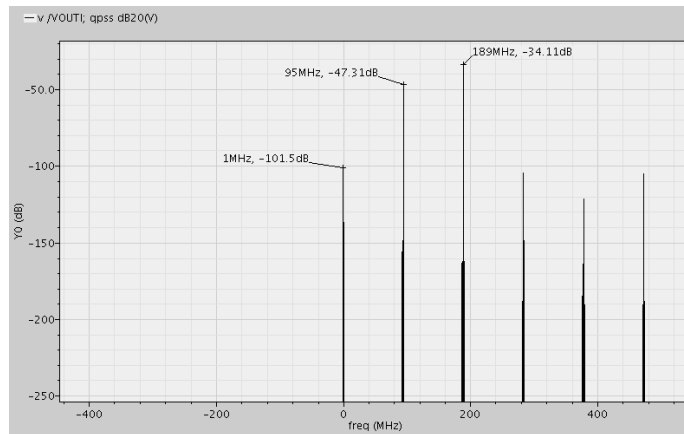


Figure 4.24: Spectrum used to compute out-of-band IIP3 of the mixer in Band I (nominal 25°C)

4.7.5 IIP2

As explained in section 4.6, the IIP2 of the receiver is mainly determined by the IIP2 of the mixer. Also the IIP2 of the mixer is mainly determined by random mismatch between the devices. Monte Carlo simulations were done to estimate the IIP2 of the mixer due to mismatch. Since IIP2 of the mixer is most important at transmit frequency offset, two tones at offsets of 45MHz & 44MHz in Band V (190MHz & 189MHz in Band I), at -28dBm power level each were used as the input. In Band I, due to large offset from desired frequency band, these tones undergo large attenuation and hence the mixer IIP2 (refer to LNA input) obtained is much better than the required specification of 50dBm as shown in figure 4.25. The simulation results for Band V is as shown in figure 4.26. Since each of these simulations takes a very long time, only ten Monte Carlo simulations were run each for BAND I as well as BAND V. In each iteration the IIP2 obtained for I and Q channel are independent. Therefore the results are effectively for 20 iterations. We can see that in all iterations the IIP2 is higher than 50dBm.

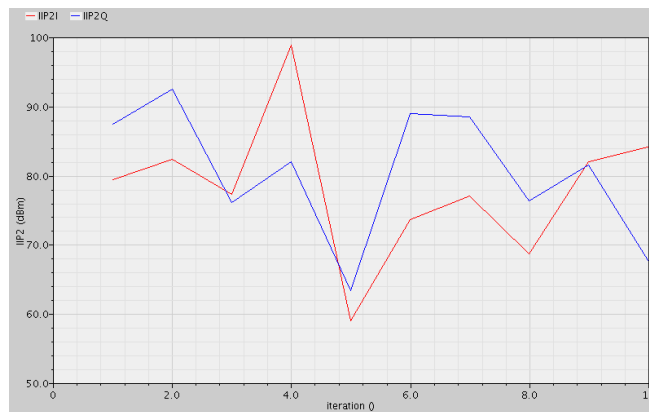


Figure 4.25: IIP2 (referred to LNA input) of the mixer in Band I obtained in different monte carlo iterations (25°C)

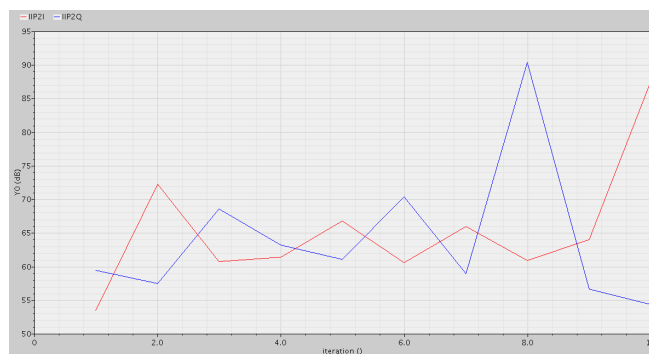


Figure 4.26: IIP2 (referred to LNA input) of the mixer in Band V obtained in different monte carlo iterations (25°C)

Chapter 5

LNA+Mixer simulation results and performance comparison

In chapter 2, the specifications targeted in this project for LNA+mixer were given. The design of and simulation results for the LNA and mixer were covered in chapters 3 and 4 respectively. In this chapter the simulation results for the LNA+mixer combination will be given. Comparison of the performance of this design with some of the designs published in the recent past is given at the end of this chapter.

The complete schematic of the differential LNA and I/Q mixer combination along with the clock generation circuit is as shown in figure 5.1. The schematic of the LNA was shown in figure 3.1. The schematics of each of the I/Q mixers and the clock generation circuit were shown in figures 4.5 and 4.16 respectively.

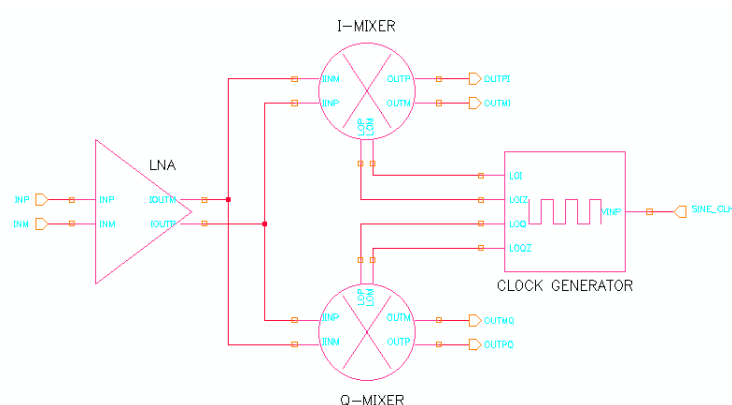


Figure 5.1: Complete schematic of differential LNA and I/Q mixer combination along with clock generation circuit

5.1 LNA+mixer simulation results

Just like in the case of individual simulation results for LNA and mixer, nominal, fast and slow process corners were considered for simulation of the LNA+mixer combination. Also temperatures 0°C , 27°C and 100°C have been considered. To reduce the total number of possible combinations of process corners and temperature, following combinations were chosen: nominal 25, fast 100, fast 0, slow 100 and slow 0. Simulations have been done only in Band I (2.12GHz) and Band V (880 MHz). The performance in Band II (1.96GHz) is expected to be close to that of Band I. Monte Carlo simulations were done for estimating IIP2 due to device mismatch. Many simulation iterations have to be done to get an estimate of IIP2 due to mismatch. Since each set of iterations take a very long time, IIP2 simulation has been done only at 25°C (Monte Carlo simulations automatically take into account process corner variations). In the following sections, the simulation results for each of the specifications for the LNA+mixer combination will be covered in detail.

5.1.1 Gain (specification: 36dB typical, 32dB worst case)

To check the gain of the LNA+Mixer combination, a single tone of -32dBm w.r.t. 100Ω (-39dB in terms of voltage) is used as input. This power level for the input signal, results in maximum tolerable voltage swing at mixer output. The frequency of the single tone is 2.121GHz for Band I and 881MHz for Band V. The LO frequency for Band I is 2.12GHz and 880MHz for Band V. The spectrum of output in Band I for nominal 25°C is as shown in figure 5.2. We can see that the voltage level of 1MHz signal at the output is -3.53dB. From this, the gain of the LNA+mixer combination can be calculated to be 35.47dB. The gains for Band I and Band V for different simulation corners are as shown in table 5.1

Table 5.1: Gain of LNA+mixer combination (dB)

Band	Nominal 25°C	Fast 0°C	Fast 100°C	Slow 0°C	Slow 100°C
I	35.47	36.66	34.61	35.45	33.76
V	37.21	38.22	36.39	37.25	35.14

5.1.2 Input matching (specification: $s_{11} < -15\text{dB}$)

As mentioned in chapter 3, 2nH of inductance has been considered in series with each of the LNA inputs to model bondwire inductance. The variation from 800MHz to 2.2GHz of s_{11} with respect to 100Ω impedance in nominal 25°C corner is as shown in figure 5.3. The s_{11} in Band I (2.12GHz) and Band V (880MHz) in different simulation corners is as shown in table 5.2.

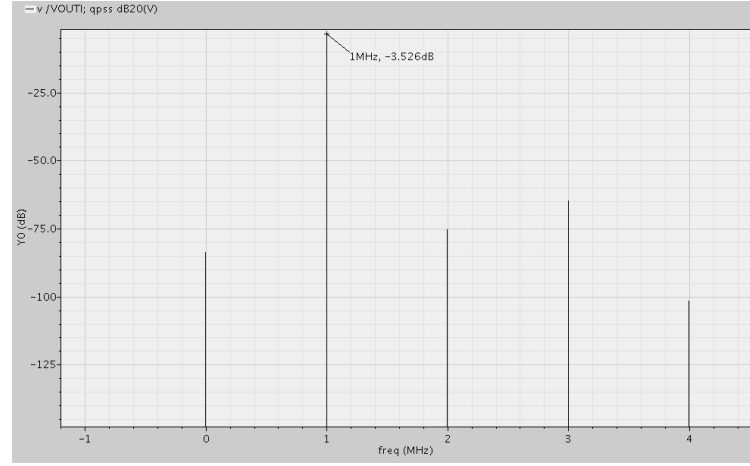


Figure 5.2: Spectrum used for computing the gain of LNA+mixer combination (nominal 25°C)

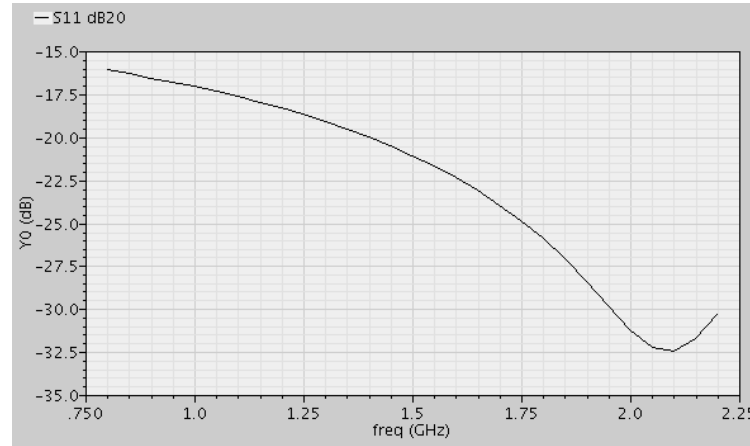


Figure 5.3: s_{11} with respect to 100Ω impedance in nominal 25°C corner

5.1.3 Noise Figure (specification: 2.5dB typical, 3.5dB worst case)

As explained in section 4.7.3, the average noise over the frequency band from 1KHz to 2MHz is of interest in this design. The average noise factor (NF_{avg}) is computed as follows -

$$NF_{avg} = \frac{\int_{1KHz}^{2MHz} \text{spot noise factor}}{2MHz} \quad (5.1)$$

The noise figure is then computed as $NF_{dB} = 10 \log_{10} NF_{avg}$. The spot noise factor of the LNA+mixer combination from 1KHz to 2Mhz in Band I at nominal 25°C is as shown in figure 5.4.

Table 5.2: s_{11} (dB) of LNA with respect to 100Ω impedance

Band	Nominal 25°C	Fast 0°C	Fast 100°C	Slow 0°C	Slow 100°C
I	-32.17	-36.61	-30.06	-30.79	-22.78
V	-16.46	-16.71	-18.04	-16.28	-15.48

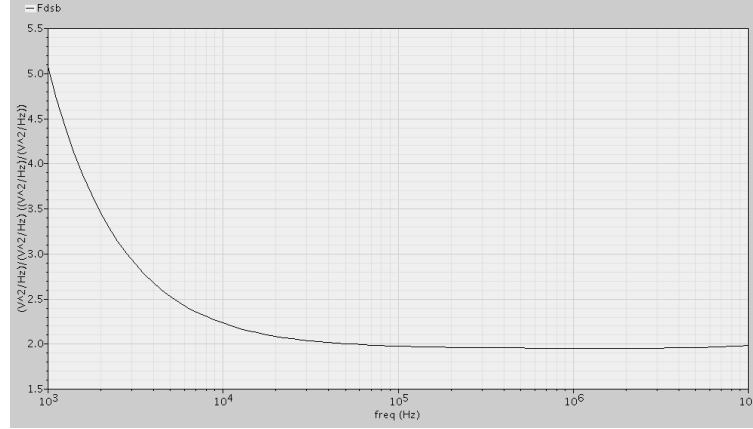


Figure 5.4: Noise Factor of the LNA+mixer in Band I (nominal 25°C)

The NF_{dB} in Bands I and V at different simulation corners are as shown in table 5.3.

Table 5.3: Average Noise Figure(dB) of LNA+mixer

Band	Nominal 25°C	Fast 0°C	Fast 100°C	Slow 0°C	Slow 100°C
I	2.92	2.65	3.46	2.75	3.48
V	2.93	2.71	3.46	2.75	3.57

5.1.4 Out-of-band IIP3 (specification : -10dBm @ Tx frequency offset)

As mentioned in section 2.5, in WCDMA, there is finite leakage from transmitter present at receiver input. This is the largest source of interference in WCDMA. In addition to this leakage, if there is any interfering signal at half the frequency separation between transmit and receive bands, third order intermodulation can produce spurious components within the desired band. Out-of-band IIP3 is used to quantify the extent of performance degradation that can be caused by this interference.

In Band I, the frequency separation between transmit and receive bands is 190MHz (45Mhz in Band V). To measure out-of-band IIP3 in Band I, two tones at frequency offsets of 189MHz and 90MHz (43MHz and 22MHz in Band V) from LO frequency, with power levels of -25dBm and

-50dBm respectively were used as the input. Since the tone nearer to the desired band has higher influence on the third order spurious component, the effective input power level can be calculated as $\frac{1}{3} \times (-25) + \frac{2}{3} \times (-50) = -41.7\text{dBm}$ w.r.t to 100Ω . Equivalent voltage level is -48.7dB. The spectrum of the output is shown in figure 5.5. We can see that the voltage level of the spurious 1MHz signal is -86.75dB. Referred to input (with a gain of 35.47dB) the level of spurious signal is -122.22dB. The IIP3 can now be calculated as $-41.7 + \frac{1}{2} \times (-48.7 - (-122.22)) = -4.94\text{dBm}$. Out-of-band IIP3 in Bands I and V in different simulation corners is as shown in table 5.4. As can be seen from table 5.4, IIP3 is higher in Band I. This is because, the frequency separation between transmit and receive bands is higher in Band I and hence the interfering signals experience higher filtering compared to the interfering signals in Band V.

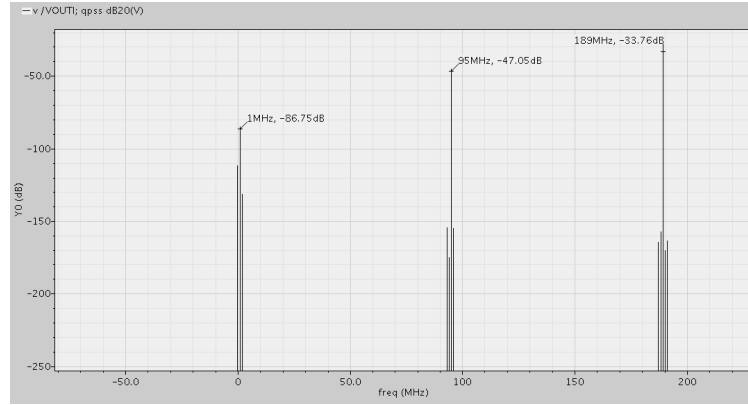


Figure 5.5: Spectrum used to compute out-of-band IIP3 of the LNA+mixer combination in Band I (nominal 25°C)

Table 5.4: Out-of-band IIP3 (dBm) of LNA+mixer combination

Band	Nominal 25°C	Fast 0°C	Fast 100°C	Slow 0°C	Slow 100°C
I	-4.94	-5.35	-3.83	-5.61	-4.86
V	-7.71	-8.09	-7.26	-8.22	-7.07

5.1.5 IIP2 (specification: minimum 50dBm @ Tx frequency offset)

IIP2 of the LNA+mixer combination is determined by random mismatch, mainly in the mixer. Monte Carlo simulations were done to estimate the IIP2 due to mismatch. Since IIP2 is most important at transmit frequency offset, two tones at offsets of 45MHz & 44MHz in Band V (190MHz & 189MHz in Band I), at -28dBm power level each were used as the input. IIP2 obtained during different iterations for Band I and Band V are as shown in figures 5.6 and 5.7 respectively. For both Band I and Band V, twenty Monte Carlo iterations were run. In each iteration the IIP2 obtained for I and Q channel are independent. Therefore the results are effectively for 40 iterations. We can see

that in Band I, the IIP2 obtained is much better than the required specification of 50dBm. This is due to the higher offset of the input tones from the desired frequency band, because of which they are filtered to a larger extent in the mixer.

Even in Band V, the IIP2 is equal to or higher than the required specification of 50dBm in all iterations. However, just from these results, it is not possible to say with certainty that the minimum IIP2 will be 50dBm, since the results are effectively only for 40 iterations. But, we can conclude that the probability of IIP2 being less than 50dBm is less than 2.5%.

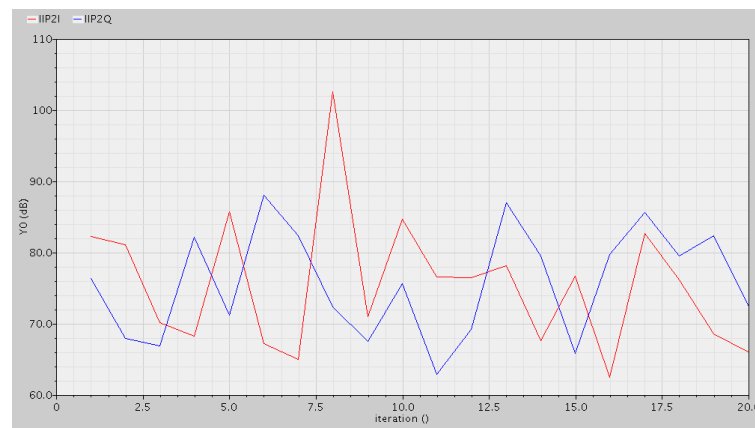


Figure 5.6: IIP2 of the LNA+mixer combination in Band I obtained in different monte carlo iterations (25°C)

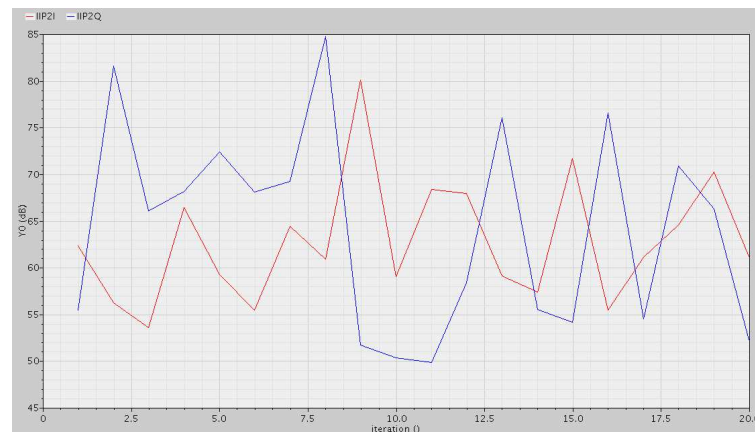


Figure 5.7: IIP2 of the LNA+mixer combination in Band V obtained in different monte carlo iterations (25°C)

5.1.6 Input referred 1dB cross compression point (specification: -25dBm)

Input referred 1dB cross compression point (ICCP1) is the power level of Tx leakage signal which will reduce the gain of the receiver for the desired signal by 1dB. This is a measure of the compression of desired signal caused by the high power level of Tx leakage signal at receiver input. Since the Tx leakage can be as high as -25dBm, the required ICCP1 for this design is -25dBm. To simulate for ICCP1, two tones, one at offset of 1MHz from f_{LO} and other transmit frequency offset (190MHz in Band I and 45MHz in Band V) were used. The power level of 1MHz offset tone was fixed at -55dBm. The power level of other tone was increased till a reduction in gain of 1dB for 1MHz offset tone was seen at the output. The variation of the voltage level of 1MHz tone at output, with different power levels of Tx leakage signal at input is shown in figure 5.8 and 5.9 for Band I and Band V respectively. From these figures we can see that ICCP1 is -20dBm in Band V and -13.6dBm in Band I. Again, higher ICCP1 in Band I is due to larger offset of Tx band from Rx band.

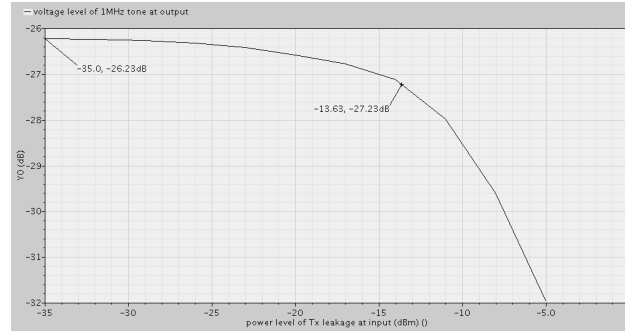


Figure 5.8: Variation of voltage level of 1MHz offset tone at output, with varying power levels of Tx leakage signal at input (Band I)

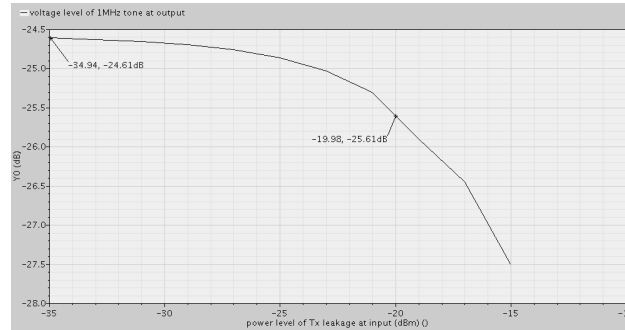


Figure 5.9: Variation of voltage level of 1MHz offset tone at output, with varying power levels of Tx leakage signal at input (Band V)

5.1.7 Power consumption (Specification: 25mA from 1.2V supply)

The total power consumption (excluding LO power) is 24.5mA from 1.2V supply. The current consumption in the differential LNA is 10mA and each of the I/Q mixers use 5mA each. Remaining current is used in the bias circuits.

5.2 performance comparison

In table 5.5, the results obtained in this work have been compared with recently published results for WCDMA receiver front-ends. Only those receiver front-ends which do not require inter-stage SAW filter between LNA and mixer have been chosen for comparison. Also only those specifications, for which data is available for comparison, have been include in the table. However, it should be noted that published results are measured ones, while those reported here are from simulations.

Table 5.5: Performance comparison of LNA+mixer with recently published results for WCDMA receiver front-ends

	This work	[1] JSSC 2009	[2] RFIC 2005	[3] RFIC 2006	[4] ISSCC 2008
Multi-band	Yes	No	No	No	No
NF (dB)	2.9	2.2	4.9	2.9	2.8
IIP2 @ Tx offset					
Band I (dBm)	> 60	> 90	38.8	63	> 65
Band V (dBm)	> 50				
Out-of-band IIP3					
Band I (dBm)	-4.9	-1	-7.4	-7	-2
Band V (dBm)	-7.7				
Power (mW)	29.4 ¹	22.7	83.7 ²	75 ²	101.5 ²
Process	65nm CMOS	90nm CMOS	0.35u SiGe	90nm CMOS	0.18um CMOS
Supply voltage	1.2V	1.5V	2.7V	1.4V/2.4V	2.9V

¹ The main circuits consume only 25mW. The remaining is used for biasing, which can be further optimised.

² For complete front-end including LNA, mixer, baseband filter and programmable gain amplifier.

Some fields in the above table have been left blank because either data is not available or it is inconclusive. The criterion for considering a design to be 'multi-band' has been whether a single

LNA+mixer combination presented in the design can work across all WCDMA bands. As emphasised in chapter 1, this criterion is very important in order to realize a low cost, small die size, software programmable receive chain for multi-band WCDMA. Though not explicitly mentioned, it has been assumed that the LNA presented in [1] does not satisfy the requirement of multi-band as explained above, since inductive degeneration has been used at the source terminal of input transistors, to achieve impedance match at the input. By this method, only narrow band impedance match at the input can be obtained, whereas for satisfying multi-band requirement for WCDMA, a bandwidth ranging from 870MHz to 2.17GHz is required.

Chapter 6

Layout

In this chapter, first the layouts of the LNA and mixer are shown. In the next section, results of the post-layout simulations will be compared to simulation results from schematics.

6.1 Layouts

6.1.1 LNA

The layout of the LNA is as shown in figure 6.1. Referring to figure 3.20, the main transistors which contribute to noise in the LNA are MTAIL, M2, M3 and M4. Therefore care was taken in layout to minimize the routing resistance at the gate terminals of these transistors as much as possible. Any parasitic capacitance at the gate terminals of M2, M3 and M4 will reduce the signal appearing at these nodes, which in turn will lead to a reduction in the overall transconductance of the LNA, and hence an increase in NF of the LNA. So care was taken in layout to minimize the routing capacitance at these nodes, by avoiding routing in lower metal levels. However, the finite routing capacitance at the gate of M3 increased the signal attenuation from GINP to gate of M3 from the intended value of $1/2$. This would result not only in imperfect cancelation of the noise and distortion of M1, but also to a reduction in transconductance of the LNA. Both these will increase the NF of the LNA. Therefore the value of CC3 was increased to make it equal to total capacitance at gate of M3, including the routing capacitance. With this the attenuation from GINP to gate of M3 was restored back to the intended value of $1/2$.

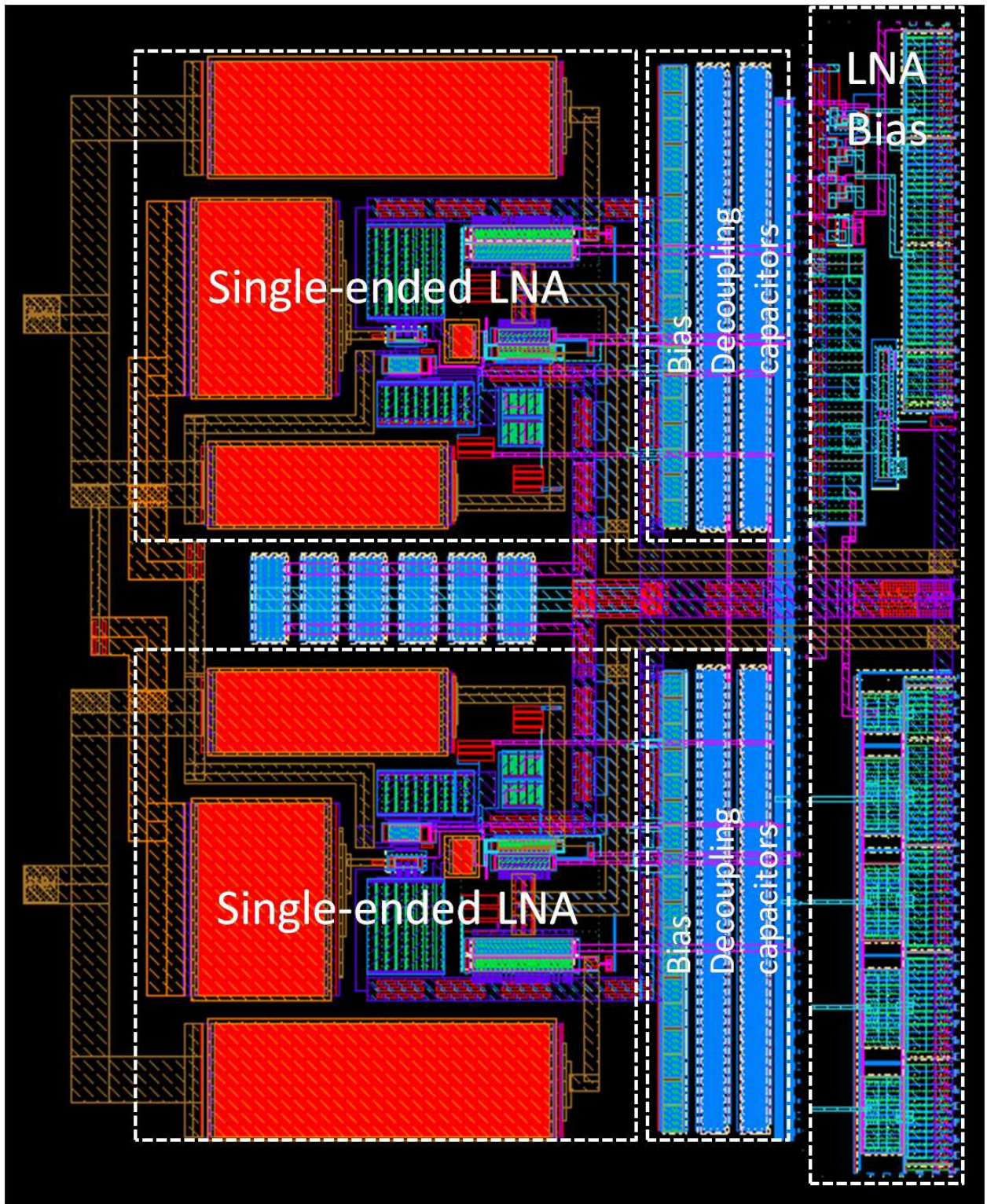


Figure 6.1: Layout of differential LNA

6.1.2 Mixer

The layout of the mixer is as shown in figure 6.2. Care has been taken to minimize parasitic coupling between RF, LO and IF ports. Also, since matching is critical in the mixer to obtain high IIP2, dummy transistors have been added where ever required to ensure matching of two transistors by the making the environment for these transistors as identical as possible.

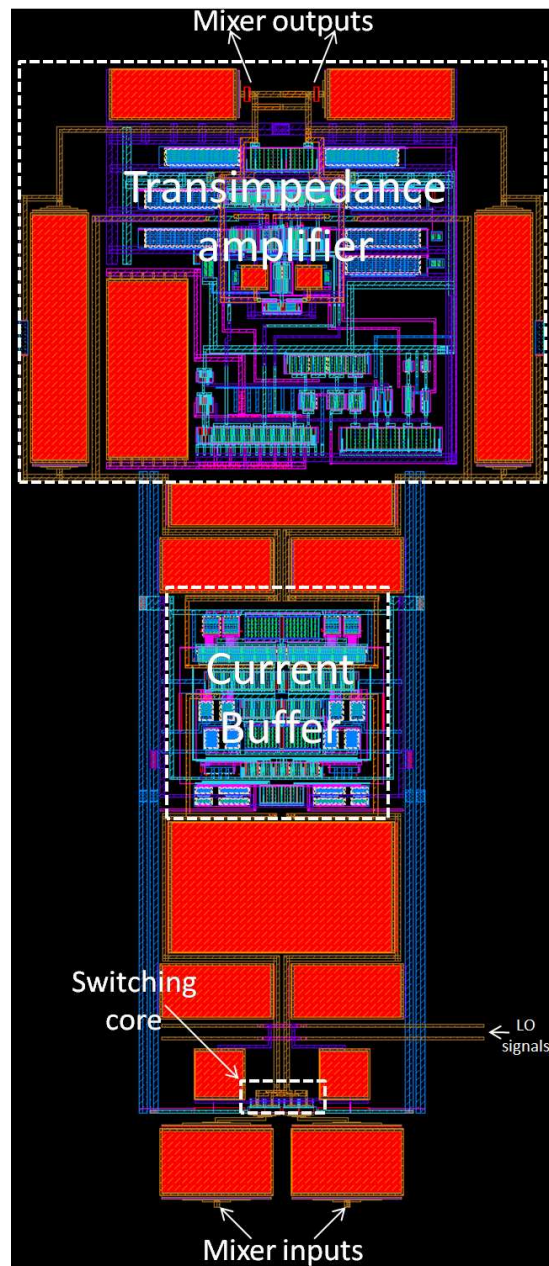


Figure 6.2: Layout of each of I/Q mixer

6.1.3 Top level

The layout of the complete design was not yet complete at the time of writing this thesis. Therefore it has not been shown here.

6.2 Post-layout simulation results

6.2.1 LNA

Simulations were done on the netlist extracted from layout by including parasitic routing resistance and capacitance. Due to the large size of the netlist, simulations take a very long time. Therefore only important simulations were done in nominal process corner and 25°C for comparison with schematic simulation results.

The test-bench used for simulation is same as that shown in figure 3.21. The LNA transconductance in Band I (2.12GHz) was found to be 170mS as compared to 189mS obtained from schematic simulations. This reduction is mainly due to parasitic capacitance at the gate terminals of M2, M3 and M4.

The comparison of NF obtained from post layout simulations with that of schematic is as shown in figure 6.3. The slight increase in NF is mainly due to the decrease in transconductance of the LNA.

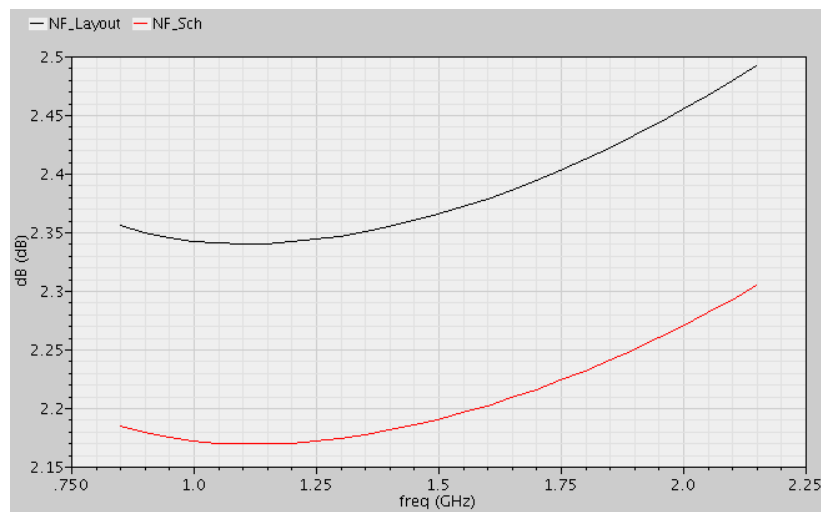


Figure 6.3: Comparison of NF of LNA obtained from post layout simulations with that of the schematic

The comparison of s_{11} is as shown in figure 6.4. Again the slight increase in s_{11} is due to increase in total capacitance at the input of the LNA due to parasitic routing capacitance.

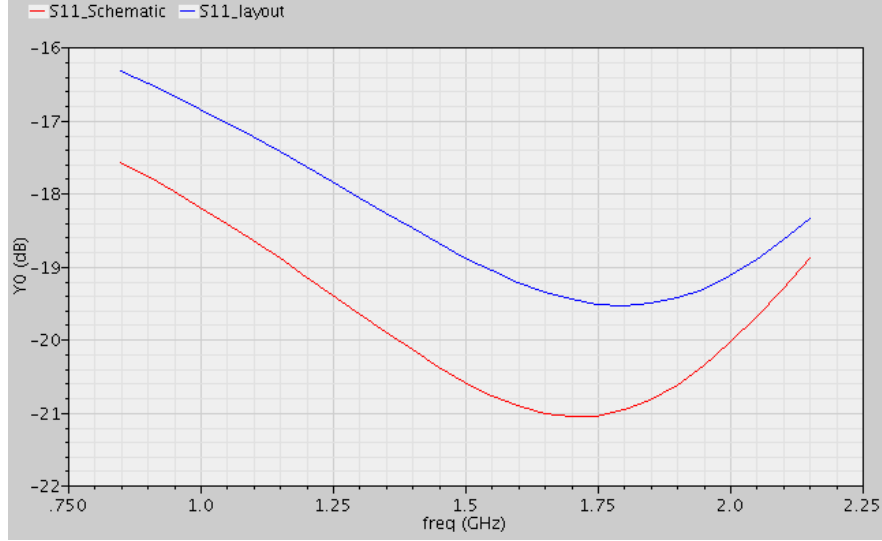


Figure 6.4: Comparison of s_{11} of LNA obtained from post layout simulations with that of schematic

Out-of-band IIP3 of the LNA was simulated in the same manner as that mentioned in section 3.7.6. The spectrum at the output in Band I is as shown in figure 6.5. Using the procedure mentioned in section 3.7.6, the out-of-band IIP3 of the LNA in Band I can be calculated to be -4.7dBm. This is very close to that obtained from schematic simulations, which is -4.9dBm.

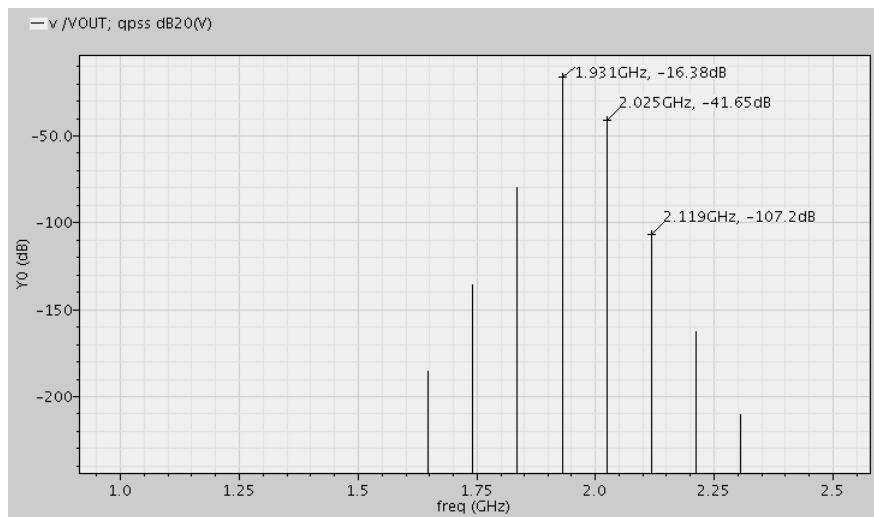


Figure 6.5: Spectrum obtained from post layout simulation for calculation of out-of-band IIP3 of LNA in Band I

6.2.2 Mixer

Mixer simulations were done using the same test bench as shown in figure 4.21 by using an ideal model for the LNA. Also, the simulations were done only in nominal process corner and 25°C temperature, using the same input signal settings as explained in section 4.7 of chapter 4. In the simulations for noise and gain of the mixer, both parasitic routing resistance and capacitance were included. However, for IIP2 and IIP3 simulations, only the parasitic routing capacitance was included, since simulation times for IIP2 and IIP3 became very large when parasitic routing resistance was also included. Also simulations for gain, IIP2 and IIP3 were done using looser tolerance settings in the simulator compared to those used in schematic simulations to reduce simulation time.

The spectrum obtained during the simulation of mixer gain in Band I, is as shown in figure 6.6. From the figure we can see that the voltage level of the 1MHz signal at the output is -2.78dB. From this, the gain of the LNA(ideal)+mixer combination can be calculated to be 36.22dB. This is very close to that obtained from schematic simulations, which is 35.5dB. The slightly higher gain could be due to the looser tolerance settings used in the simulator.

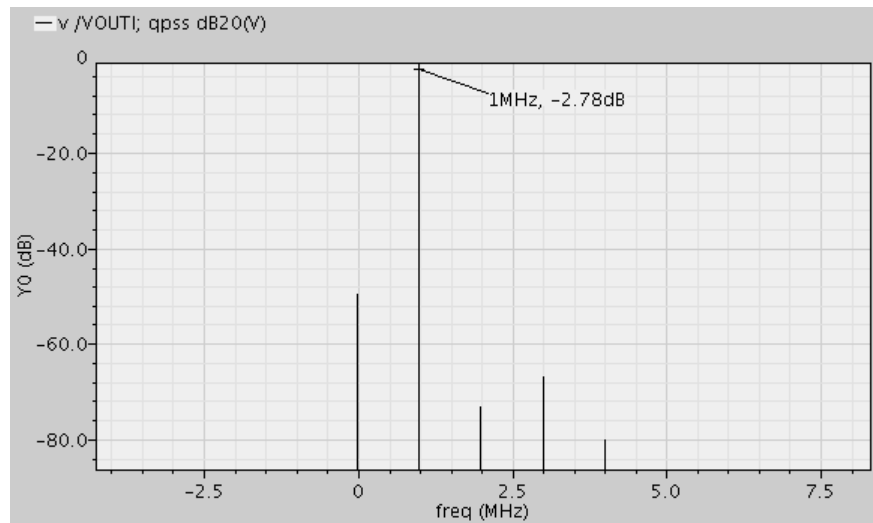


Figure 6.6: Spectrum obtained from post layout simulation for calculation of the gain of LNA(ideal)+mixer combination in Band I

The comparison of mixer noise figure is as shown in figure 6.7. The average noise figure in 1kHz to 2MHz frequency range is 1.41dB, which is very close to that obtained from schematics, which is 1.33dB.

Estimation of mixer IIP2, from mismatch simulations using the post layout netlist would take a very long time and have not been done. However, it is important to ensure that there is no unintended systematic mismatch in layout, which can degrade the IIP2. Therefore IIP2 simulation

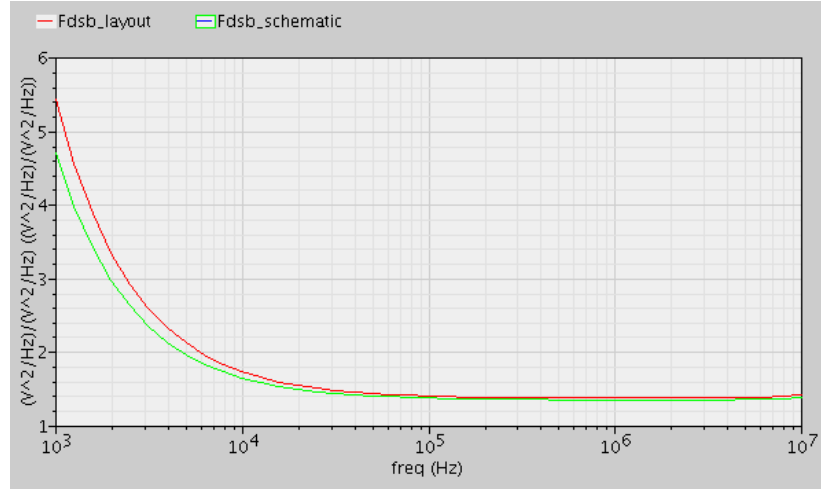


Figure 6.7: Comparison of mixer noise figure in Band I obtained from post layout simulations with that of schematic

was done on post-layout netlist including the parasitic routing capacitance, but without enabling random mismatch between devices. As explained in section 4.7.5, the IIP2 obtained in Band I, is higher than the IIP2 obtained in Band V. Therefore IIP2 simulation on post layout netlist was done for Band V. The spectrum obtained at output is as shown in figure 6.8.

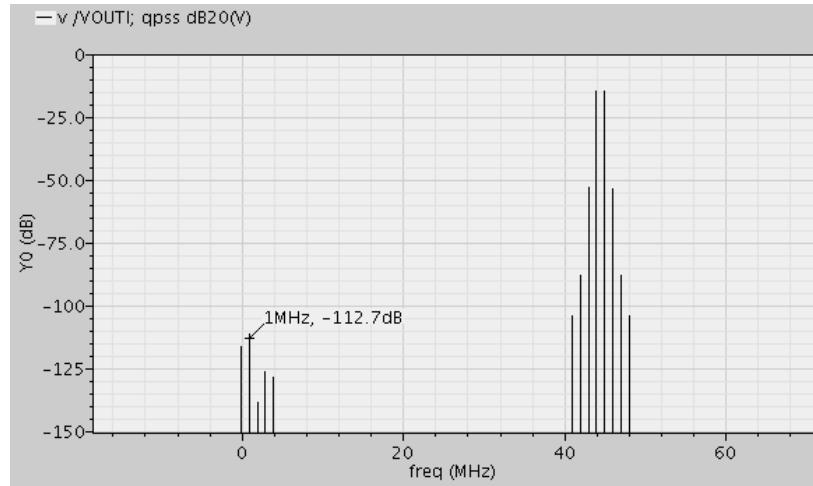


Figure 6.8: Spectrum obtained from post layout simulation for calculation of mixer IIP2 in Band V

The voltage level of 1MHz signal at the output is -112.7dB. Referring back to the input with a gain of 36dB, the voltage level of 1MHz signal at the input is -148.7dB. Noting that voltage level of a signal with power of -28dBm with respect to 100Ω is -35dB, the IIP2 can be calculated to be $-28 + (-35 - (-148.7)) = 85.7dB$. The IIP2 obtained here is limited both by simulation accuracy

as well any slight systematic mismatch that may be present in the layout. However, since the IIP2 with mismatch is expected to be around 50dBm, the final IIP2 will still be limited by random mismatch between devices.

Finally, the IIP3 of the mixer was also checked in Band V. The spectrum at the mixer output is as shown in figure 6.9. The IIP3 obtained is -3.7dBm, which is 1.5dB higher than that obtained from schematic, which is -5.2dBm. The higher value could again be due to the looser tolerance setting in the simulator.

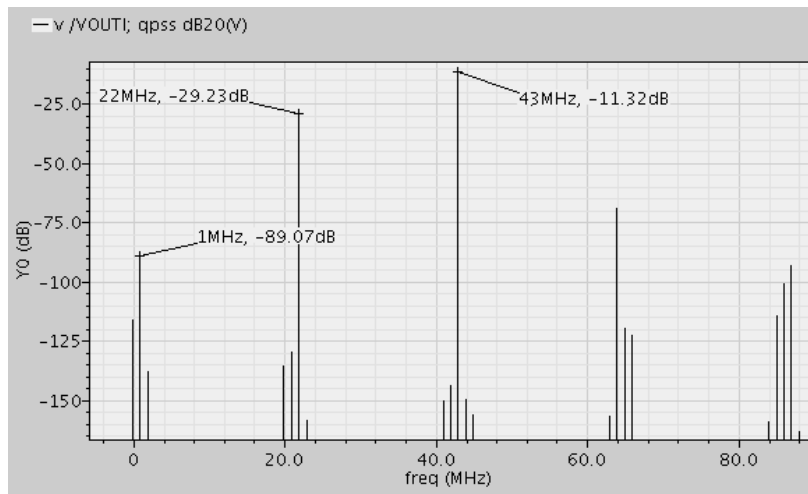


Figure 6.9: Spectrum obtained from post layout simulation for calculation of mixer IIP3 in Band V

Chapter 7

Conclusions and future work

An inductor-less multi-band LNA+mixer combination mainly intended for WCDMA has been designed in this work using IBM 65nm process technology. The main contributions and innovations in this work are:

1. The trade-offs between noise, linearity and power consumption have been analyzed in detail for noise-cancelation LNA topology
2. Modifications to the basic noise cancelation topology have been proposed for lower NF.
3. In most passive mixer implementations, a transimpedance amplifier (TIA) is used after the switching core to convert the current output from the switching core into a voltage. Not much information is available in literature about the design of the TIA. In this thesis, the design of the TIA, using a two stage operational amplifier has been explained in detail.
4. A new approach of adding a current buffer between the switching core and the TIA, to reduce the overall input referred noise of the mixer has been proposed.
5. Advantages of using 25% duty cycle LO on mixer gain, noise and linearity have been explored in detail.

7.1 Conclusions

The main conclusions in this thesis can be summarized as follows:

7.1.1 LNA

1. Noise cancelation topology can be used to meet the very stringent LNA requirements as mentioned in chapter 3, over a wide frequency range. Therefore this is a good starting choice in the search for a LNA which can meet the requirements for WCDMA over multiple bands.
2. As shown in chapter 3, IIP3 of common source stage, without cascode is very sensitive to load impedance. When cascoding is used, although the sensitivity to load impedance is reduced, it is still desirable to have low load impedance for optimum IIP3 performance. Since, the noise cancelation topology uses common source stage as the amplification stage, it is more suited for providing current output (wherein input impedance of following stage will be low) than a voltage output (wherein input impedance of following stage will have to be high).
3. The noise figure of the LNA using noise cancelation topology can be lowered by increasing the transconductance in the amplifying stage. However, for impedance matching at the input, without using any additional network for matching except the bondwire inductance, there is a maximum capacitance that can be tolerated at the input of the LNA. The maximum transconductance in the amplifying stage is limited by this maximum capacitance that can be tolerated. Therefore for low noise figure the bias current density for the amplifying stage has to be chosen where transistor F_T is maximum. However, this bias point is not the optimum one for low power consumption. Therefore, as is common in all analog circuits, there is a trade-off between noise figure and power consumption.
4. The requirement on bias current density in the amplifying stage, for high IIP3 and high transistor F_T are contradictory to each other. Therefore a compromise has to be made on one of the specifications, depending upon which specification is more important for the design. In this design higher priority has been given to obtain a high F_T to lower the noise figure of the LNA.

7.1.2 Mixer

1. Passive mixer topology is an ideal choice for the mixer to obtain high IIP2.
2. As shown in chapter 4, a current buffer can be used between the switching core and the TIA to lower the contribution of the TIA to mixer noise and also lower the total input referred noise of the mixer at the same time.
3. When fully differential circuits are used to implement a mixer, the mixer IIP2 is determined solely by random mismatch. To reduce this random mismatch large gate widths and lengths have to be used for all transistors used in the design of the mixer. When the TIA directly follows the switching core, increasing the width and length of the transistors used for the switching core, increases the contribution of the TIA to mixer noise, since the contribution

of TIA to mixer noise is directly dependent on the parasitic capacitance at the input of the switching core. A current buffer added between the switching core and the TIA, removes this dependence and hence enables the design of the mixer for high IIP2.

4. When sine wave LO signal is used in the mixer, depending on the common mode voltage of the LO signal, there is a possibility of the two outputs of the switching core getting shorted for a short period of time during every LO cycle. This can lead to an increase in mixer noise as explained in chapter 4. By using square wave non-overlapping clocks as LO signals, this issue can be avoided.
5. In [1], it has been pointed out that, when square wave LO is used, using 25% duty cycle for LO signals can result in theoretical improvement of 3dB in the gain of the mixer. In the same paper, it has also been explained that using 25% duty cycle LO can help to reduce mixer noise figure and also improve mixer IIP2. During this design one more advantage of using 25% duty cycle LO was observed : It was found in simulations that when both I and Q mixer are connected to the LNA and 50% duty cycle LO is used, the voltage at the output of the each of the mixers drops by about 12dB, when compared to the voltage when only of the mixers is connected. This is 6dB higher than expected drop in voltage due to equal splitting of the LNA current between the two mixers. Although this problem was traced to lack of isolation between the two mixers, not much time was spent on identifying the root cause. However, when 25% duty cycle LO is used, at any given time the LNA current flows into only one of the mixers. Thus the mixers are isolated in time and this problem is not seen.

7.2 Recommendations for future work

The design and simulation results, presented in this thesis are only a first step in realizing a true multi-band receiver solution for WCDMA/GSM. Based on these results and the conclusions reached in this work, recommendations for further improvement are as follows:

1. A noise figure of 2.9dB has been achieved in this design. However, a noise figure of 2.5dB or lower for LNA+mixer combination is desirable. So techniques to further reduce the noise figure of both the LNA as well as the mixer need to be explored, without compromising on other performance specifications. It is worth exploring for example, to check if the noise contribution of the current source at the input of the LNA (implemented using MTAIL and RTAIL in figure 3.20) can be eliminated by implementing a single current source for both the single-ended LNAs and making the noise of this current source appear as common mode noise at the outputs of the two LNAs. This can result in reduction of the noise figure of the differential LNA from 2.23dB to 1.78dB in Band I.
2. IIP3 was a more relaxed specification in this design than noise figure and IIP2 specifications. As explained in chapter 4, adding a current buffer between the switching core and the TIA

helps to reduce the NF of the mixer as well as improve the IIP2 of the mixer. However, the effect of the current buffer on mixer IIP3 has not been studied in detail in this design and needs to be done.

3. The transimpedance amplifier in this design requires a high impedance load to be present at its output. Therefore a voltage buffer is required after this LNA+mixer combination to drive a low impedance load. A modified transimpedance amplifier scheme may be possible where in a low impedance load at the output can be tolerated without significant increase in power consumption. Such a scheme might result in lower power consumption when compared to total power consumption of the TIA and the following voltage buffer.

Appendix A

Analysis of negative feedback using two port network theory

A.1 Introduction

Feedback is defined as the returning of a fraction of the output signal of a system to its input. Figure A.1 shows the block diagram of a general feedback system. Here $G(s)$ is the transfer function of the feedforward network and $H(s)$ is the transfer function of the feedback network. Now since $E(s) = X(s) - Y(s)H(s)$,

$$Y(s) = G(s) \times (X(s) - Y(s)H(s)) \quad (\text{A.1})$$

Therefore,

$$\frac{Y(s)}{X(s)} = \frac{G(s)}{1 + G(s)H(s)} \quad (\text{A.2})$$

$G(s)$ is called the open loop transfer function or open-loop gain and $Y(s)/X(s)$ is called the close loop transfer function or close loop gain. $-G(s)H(s)$ is called the loop gain and is obtained by making the input zero, breaking the loop at some point, inserting a test signal and calculating the gain around the loop as shown in figure A.2. $1 + G(s)H(s)$ is called the return difference.

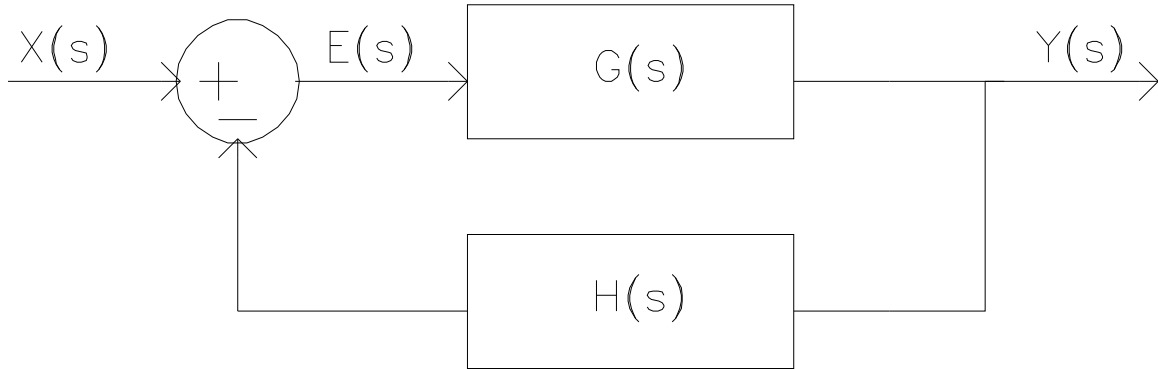


Figure A.1: Block diagram of general feedback system

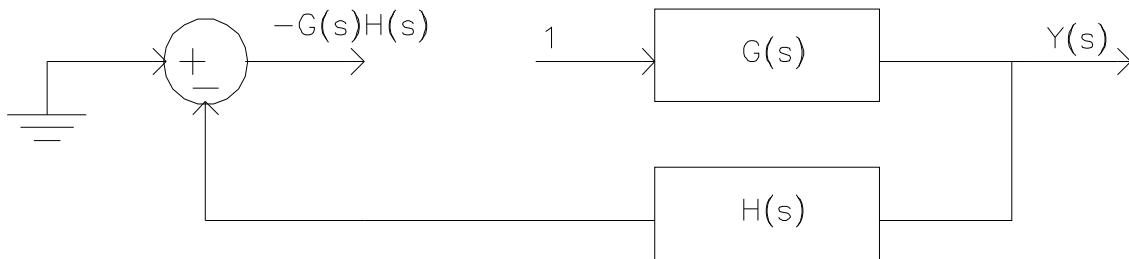


Figure A.2: Calculation of loop gain

If $-G(s)H(s)$ is positive, then it is called positive feedback. Here the fraction of the output returned to the input increases the effective input. If $-G(s)H(s)$ is negative, then it is called negative feedback. Here the fraction of the output returned to the input decreases the effective input. In most feedback circuits used in the design of amplifiers, $G(s)$ represents an operational amplifier with gain A and $H(s)$ is a frequency independent quantity β which is represented as shown in figure A.3.

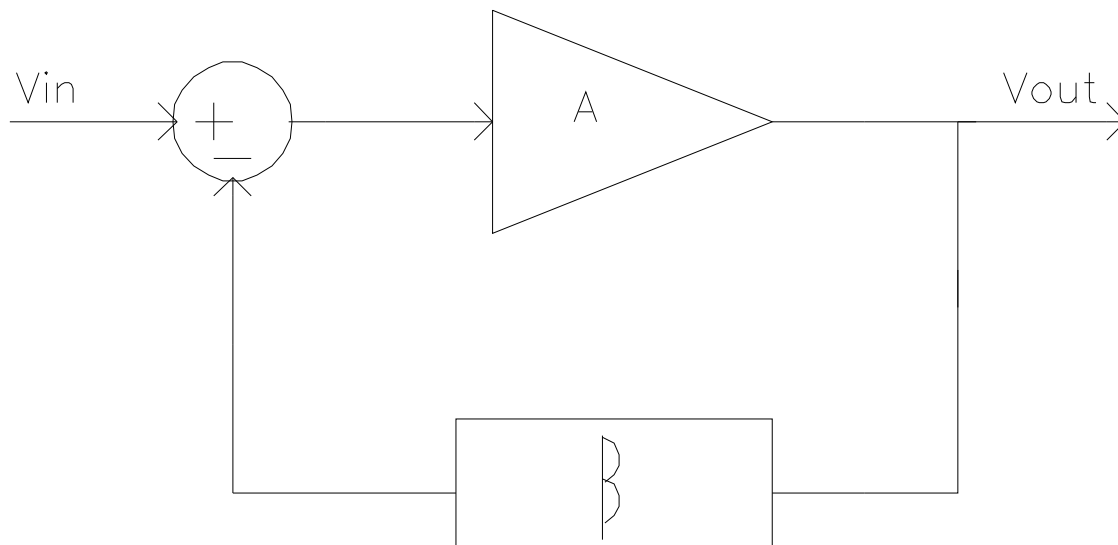


Figure A.3: Common feedback system

A.2 Analysis of feedback using 2-port networks

A two port network can be analyzed in terms of any of y , z , h or g parameters. Depending on the type of amplifier (voltage, current, transimpedance or transconductance) being designed, one of these parameters is more suitable for the analysis. If the two port parameters for the feedforward and feedback networks are chosen such that the independent variables are common to both these networks at the input and output (for e.g. when voltage is sensed at the output and a corresponding current is fed back to the input, then voltage at the output and voltage at the input are common to both the feedforward and feedback networks), then the two port parameters of the composite network can be written as the sum of the two port parameters of the individual networks.

Let the two port matrix of the feedforward network (usually an opamp) be

$$P_A = \begin{bmatrix} p_{IA} & p_{RA} \\ p_{FA} & p_{OA} \end{bmatrix} \quad (\text{A.3})$$

and that of the feedback network be

$$P_F = \begin{bmatrix} p_{IF} & p_{RF} \\ p_{FF} & p_{OF} \end{bmatrix} \quad (\text{A.4})$$

The two port matrix of the composite network can now be written as -

$$P = \begin{bmatrix} p_{IA} + p_{IF} & p_{RA} + p_{RF} \\ p_{FA} + p_{FF} & p_{OA} + p_{OF} \end{bmatrix} \quad (\text{A.5})$$

When the two port parameters are chosen such that the two port matrix of the composite network is obtained as sum of the two port matrices of the feedforward and feedback network, the composite network actually represents an amplifier for which the appropriate two-port matrix will be obtained by interchanging the independent and dependent variables. (For e.g. In a transimpedance amplifier, the two port matrix of the composite network can be written as sum of y-matrices of the feedforward and feedback networks. However, z-matrix is the appropriate two port matrix for a transimpedance amplifier)

So the two port matrix actually representing the feedback network will be the inverse of the composite matrix and is given by

$$P^{-1} = \begin{bmatrix} \frac{p_{OA} + p_{OF}}{\Delta P} & \frac{-(p_{RA} + p_{RF})}{\Delta P} \\ \frac{-(p_{FA} + p_{FF})}{\Delta P} & \frac{p_{IA} + p_{IF}}{\Delta P} \end{bmatrix} \quad (\text{A.6})$$

where

$$\Delta P = (p_{IA} + p_{IF}) \times (p_{OA} + p_{OF}) - (p_{RA} + p_{RF}) \times (p_{FA} + p_{FF}) \quad (\text{A.7})$$

ΔP can also be written as

$$\Delta P = (p_{IA} + p_{IF}) \times (p_{OA} + p_{OF}) \times \left(1 - \frac{(p_{RA} + p_{RF}) \times (p_{FA} + p_{FF})}{(p_{IA} + p_{IF}) \times (p_{OA} + p_{OF})}\right) \quad (\text{A.8})$$

Now it can be recognised that the loop-gain is

$$G_{loop} = \frac{(p_{RA} + p_{RF}) \times (p_{FA} + p_{FF})}{(p_{IA} + p_{IF}) \times (p_{OA} + p_{OF})} \quad (\text{A.9})$$

So ΔP can also be written as

$$\Delta P = (p_{IA} + p_{IF}) \times (p_{OA} + p_{OF}) \times (1 - G_{loop}) \quad (\text{A.10})$$

Here if G_{loop} is negative, then the feedback is negative, else it is positive.

Now the two port matrix representing the feedback network is given by

$$P^{-1} = \begin{bmatrix} \frac{1}{(p_{IA} + p_{IF}) \times (1 - G_{loop})} & \frac{-(p_{RA} + p_{RF})}{(p_{IA} + p_{IF}) \times (p_{OA} + p_{OF}) \times (1 - G_{loop})} \\ \frac{-(p_{FA} + p_{FF})}{(p_{IA} + p_{IF}) \times (p_{OA} + p_{OF}) \times (1 - G_{loop})} & \frac{1}{(p_{OA} + p_{OF}) \times (1 - G_{loop})} \end{bmatrix} \quad (\text{A.11})$$

If the corresponding source and load parameters are p_{IS} and p_{OL} respectively then,

$$G_{loop} = \frac{(p_{RA} + p_{RF}) \times (p_{FA} + p_{FF})}{(p_{IA} + p_{IF} + p_{IS}) \times (p_{OA} + p_{OF} + p_{OL})} \quad (\text{A.12})$$

$$P^{-1} = \begin{bmatrix} \frac{1}{(p_{IA} + p_{IF} + p_{IS}) \times (1 - G_{loop})} & \frac{-(p_{RA} + p_{RF})}{(p_{IA} + p_{IF} + p_{IS}) \times (p_{OA} + p_{OF} + p_{OL}) \times (1 - G_{loop})} \\ \frac{-(p_{FA} + p_{FF})}{(p_{IA} + p_{IF} + p_{IS}) \times (p_{OA} + p_{OF} + p_{OL}) \times (1 - G_{loop})} & \frac{1}{(p_{OA} + p_{OF} + p_{OL}) \times (1 - G_{loop})} \end{bmatrix} \quad (\text{A.13})$$

A.3 voltage-current feedback or y-feedback

Here the output voltage is sensed and a proportionate current is fed back to the input. Thus the feedback network will be in parallel with the feedforward network both at the input as well as at the output as shown in figure A.4. Because the feedback network is in parallel with the feedforward network, both at the input as well as at the output, intuitively we can say that this feedback should reduce both the input as well as the output impedances. Hence an amplifier with voltage current feedback can act as good current controlled voltage source or transimpedance amplifier.

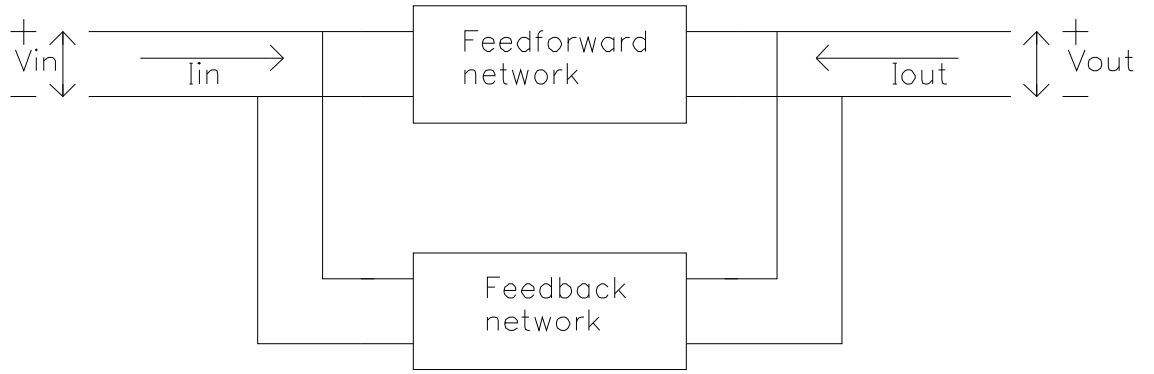


Figure A.4: Block diagram of y-feedback

Here the voltage is common to both the feedforward as well as feedback networks both at the input as well as at the output. Hence the composite matrix has to be written in term of y-parameters, with input and output voltage being independent as given below -

$$\begin{bmatrix} i_I \\ i_O \end{bmatrix} = P \cdot \begin{bmatrix} v_I \\ v_O \end{bmatrix} = \begin{bmatrix} (y_{IA} + y_{IF}) & (y_{RA} + y_{RF}) \\ (y_{FA} + y_{FF}) & (y_{OA} + y_{OF}) \end{bmatrix} \cdot \begin{bmatrix} v_I \\ v_O \end{bmatrix} \quad (\text{A.14})$$

But this network needs to be ideally represented in terms of z-parameters since this feedback is used to obtain a good current controlled voltage source. The z-parameter matrix P^{-1} for the composite network in terms of y-parameters of the individual networks is

$$\begin{bmatrix} v_I \\ v_O \end{bmatrix} = P^{-1} \cdot \begin{bmatrix} i_I \\ i_O \end{bmatrix} = \begin{bmatrix} z_I & z_R \\ z_F & z_O \end{bmatrix} \begin{bmatrix} i_I \\ i_O \end{bmatrix} \quad (\text{A.15})$$

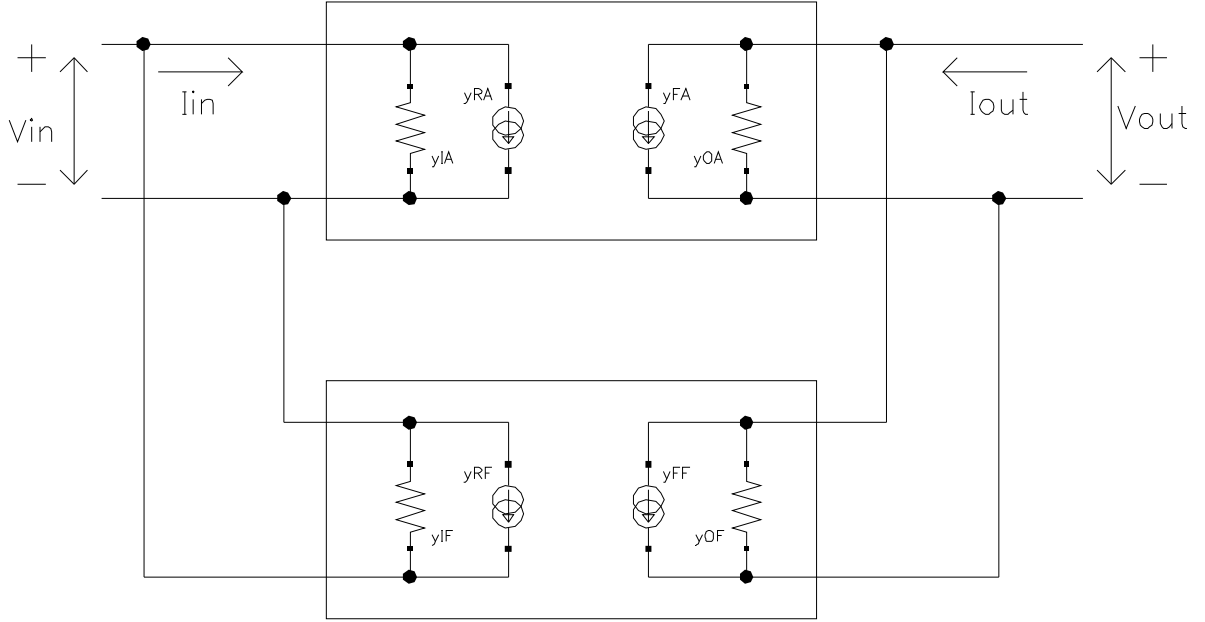


Figure A.5: Representation of voltage-current feedback network in terms of y-parameters.

$$P^{-1} = \begin{bmatrix} \frac{1}{(y_{IA} + y_{IF}) \times (1 - G_{loop})} & \frac{-y_{RF}}{(y_{IA} + y_{IF}) \times (y_{OA} + y_{OF}) \times (1 - G_{loop})} \\ \frac{-y_{FA}}{(y_{IA} + y_{IF}) \times (y_{OA} + y_{OF}) \times (1 - G_{loop})} & \frac{1}{(y_{OA} + y_{OF}) \times (1 - G_{loop})} \end{bmatrix} \quad (A.16)$$

and the loop gain G_{loop} is

$$G_{loop} = \frac{(y_{FA} + y_{FF}) \times (y_{RF} + y_{RF})}{(y_{IA} + y_{IF}) \times (y_{OA} + y_{OF})} \quad (A.17)$$

Taking into account source and load admittances, the loop gain is

$$G_{loop} = \frac{(y_{FA} + y_{FF}) \times (y_{RF} + y_{RF})}{(y_{IA} + y_{IF} + y_{IS}) \times (y_{OA} + y_{OF} + y_{OL})} \quad (A.18)$$

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