Overview of Xilinx Virtex II Pro

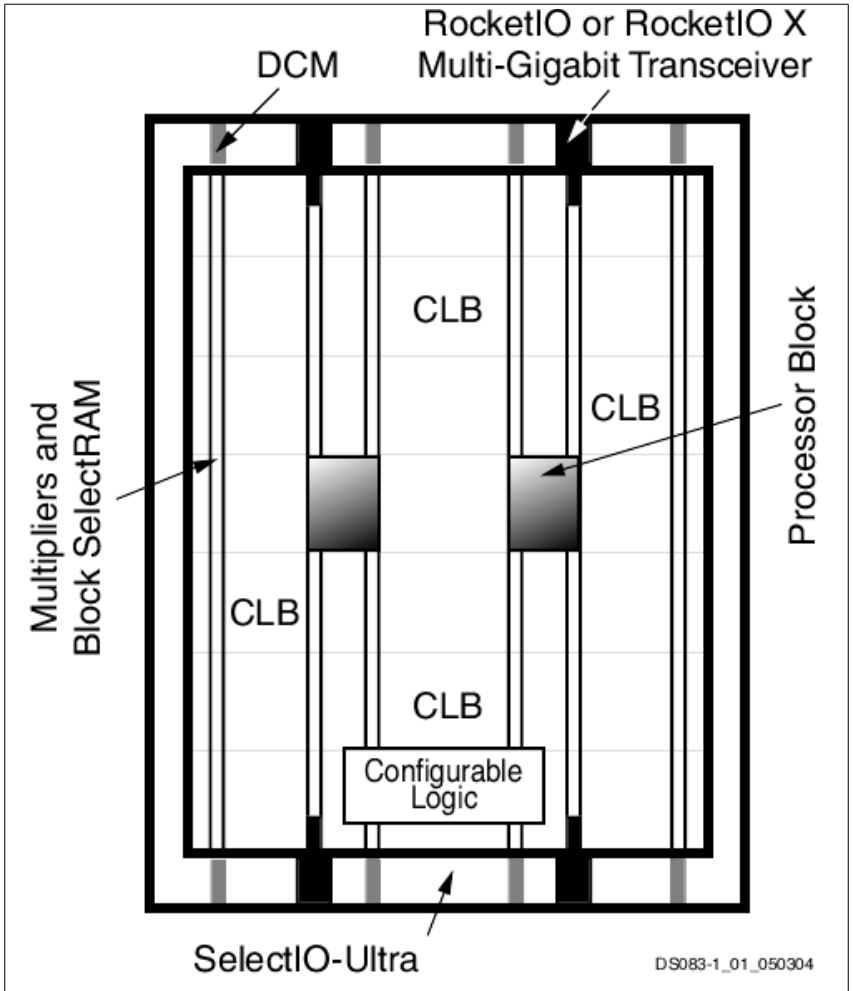


Figure 1: **Virtex-II Pro Generic Architecture Overview**

Acronyms

lots of TLAs...

- ***CLB*** — Configurable Logic Block
- ***IOB*** — Input/Output Block
- ***LUT*** — Look-Up Table
- ***SRL16*** — Shift Register and Look-up (16 bits)
- ***TBUF*** — Three-state Buffer

CLB Interface

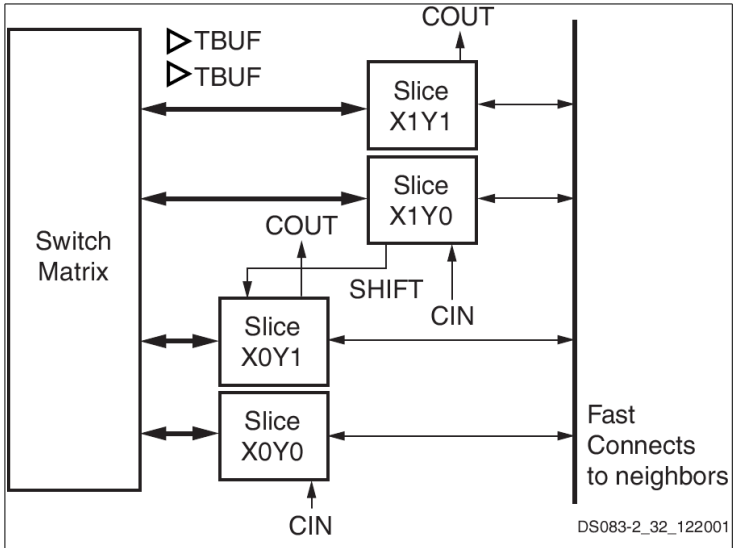


Figure 32: **Virtex-II Pro CLB Element**

One CLB is composed of

- four slices
- some fast carry-chain routing
- two three-state buffers

Overview of a Slice

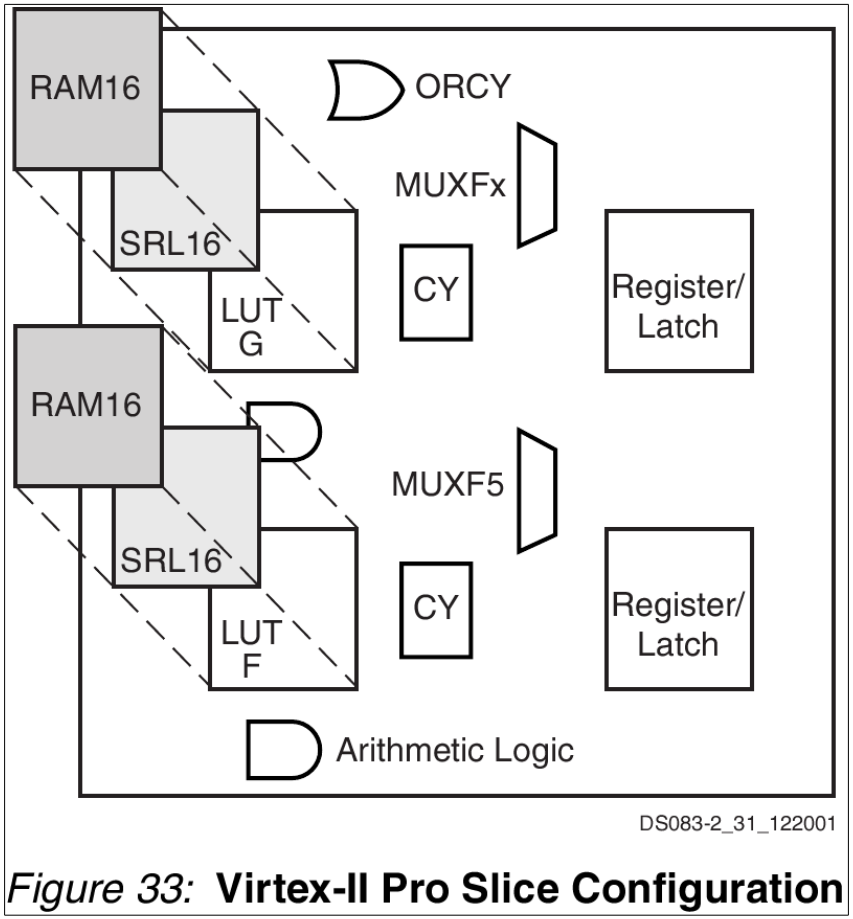
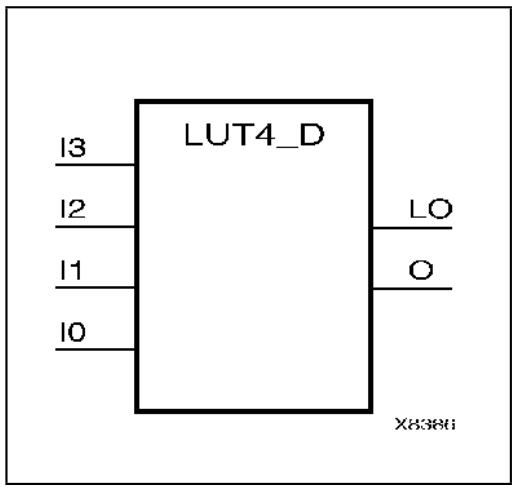


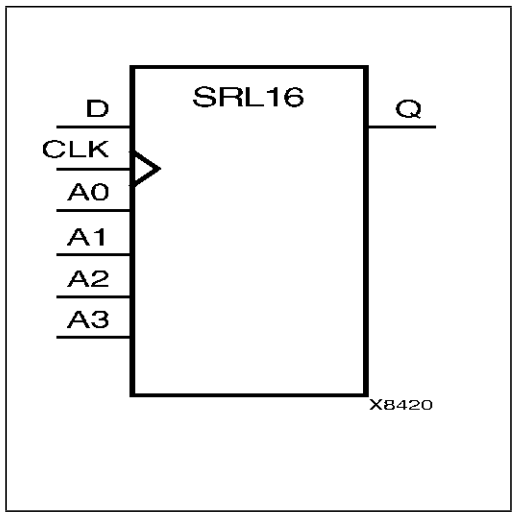
Figure 33: **Virtex-II Pro Slice Configuration**

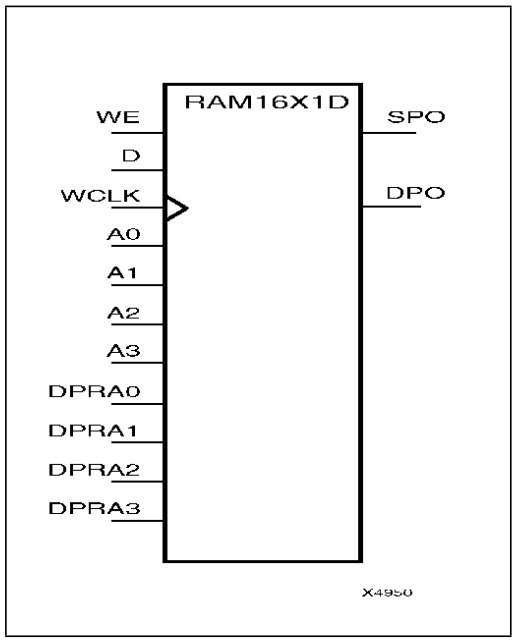
LUT4_D/SRL16/RAM16

- the Look-Up Table can be configured to do multiple functions
  - as a LUT, it is a function generator
    (NOTE: normally, one let's the VHDL synthesis tool translate normal Boolean operators into LUTs)
  - as a SRL, the block forms a 16-bit shift register; however the output can be set to "read" from any bit so it is effectively 1- to 16-bit shift register
  - as a RAM, the block can behave as a 16-bit deep by 1-bit wide static dual ported RAM
- which function it configured to do depends on what primitive shows up in the netlist

LUT4_D/SRL16/RAM16 Schematic



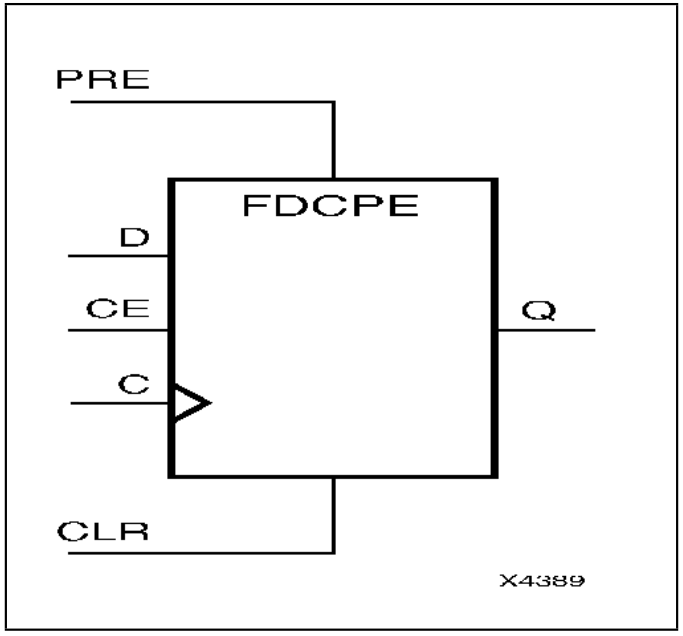




Register/Latch Block

- register/latch block is configured based on what primitive shows up in the netlist
- for example: `FDCPE` is a single D-type flip-flop with clock enable and asynchronous clear and pre-set
  - `D` — (in) data
  - `CLK` — (in) clock
  - `CE` — (in) chip enable
  - `CLR` — (in) clear (force `Q` low)
  - `PRE` — (in) preset (force `Q` high)
  - `Q` — (out) output

FDCPE Schematic Symbol



FDCPE in VHDL

```
-- FDCPE: Single Data Rate D Flip-Flop with Asynchronous Clear, Set and
--        Clock Enable (posedge clk).  All families.
-- Xilinx HDL Libraries Guide, version 9.1i

FDCPE_inst : FDCPE
generic map (
   INIT => '0') -- Initial value of register ('0' or '1')
port map (
   Q => Q,       -- Data output
   C => C,       -- Clock input
   CE => CE,     -- Clock enable input
   CLR => CLR,   -- Asynchronous clear input
   D => D,       -- Data input
   PRE => PRE    -- Asynchronous set input
);

-- End of FDCPE_inst instantiation
```

Slice Details (Top-Half)

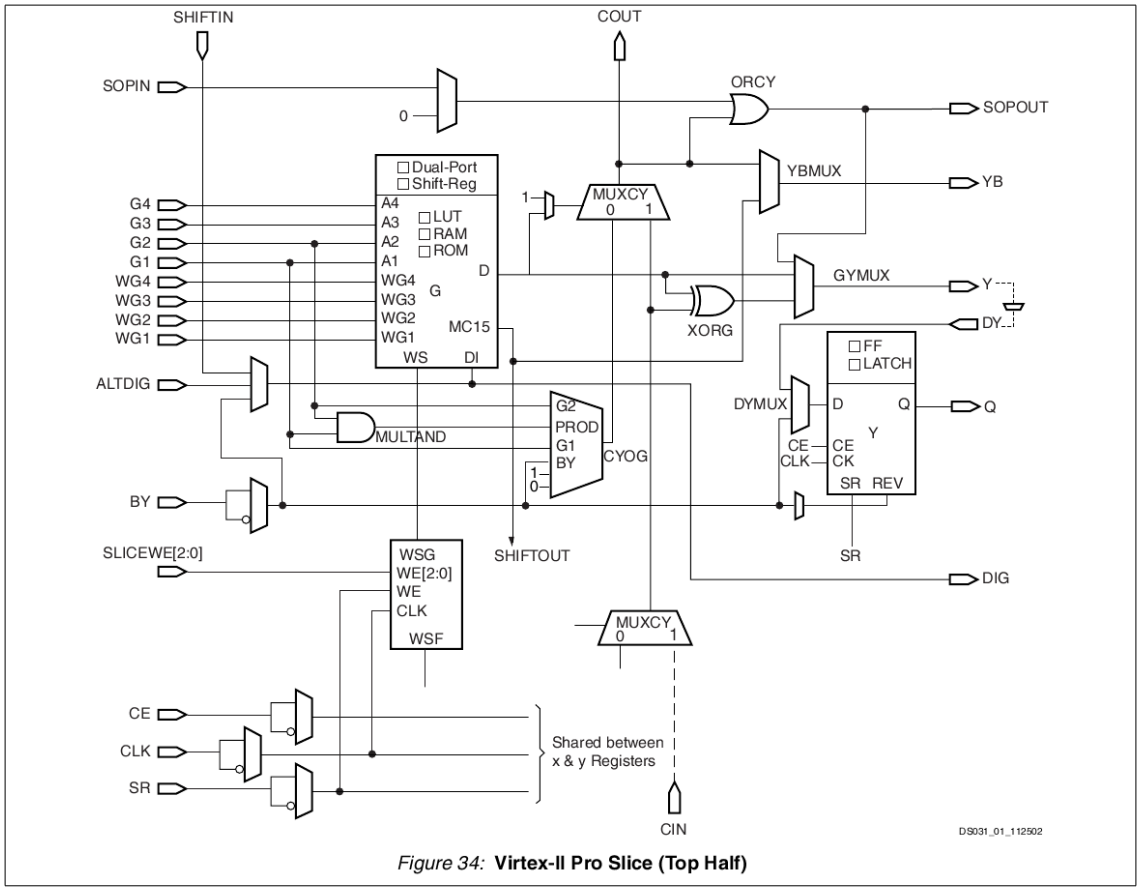


Figure 34: **Virtex-II Pro Slice (Top Half)**

Flip-Flops in Slice

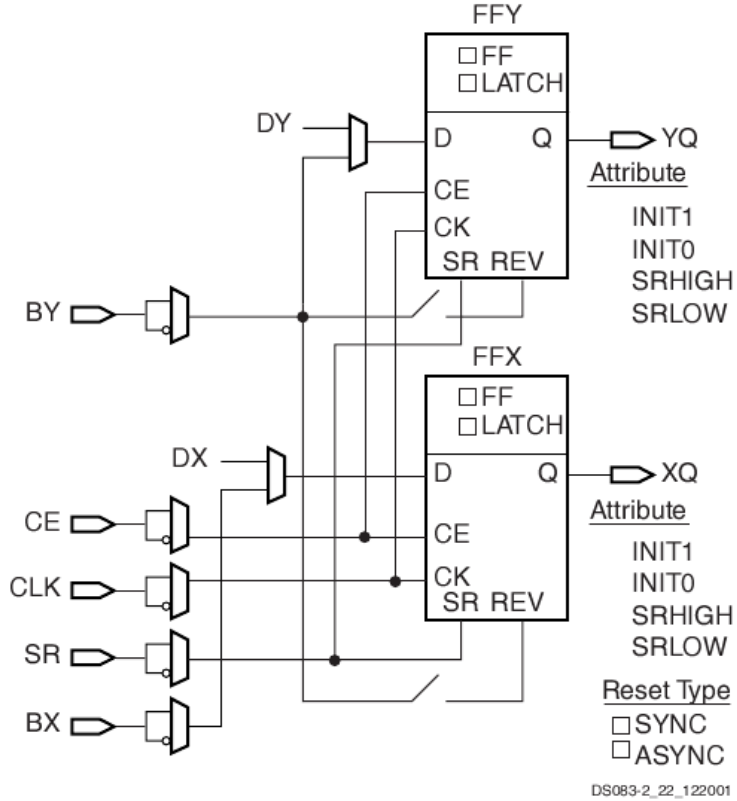


Figure 35: **Register / Latch Configuration in a Slice**

Tri-State Gates

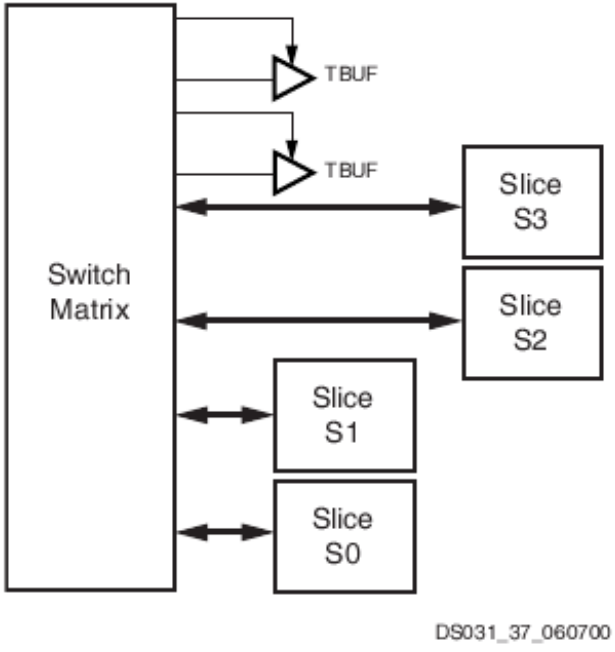


Figure 45: **Virtex-II Pro 3-State Buffers**

I/O Blocks Interface

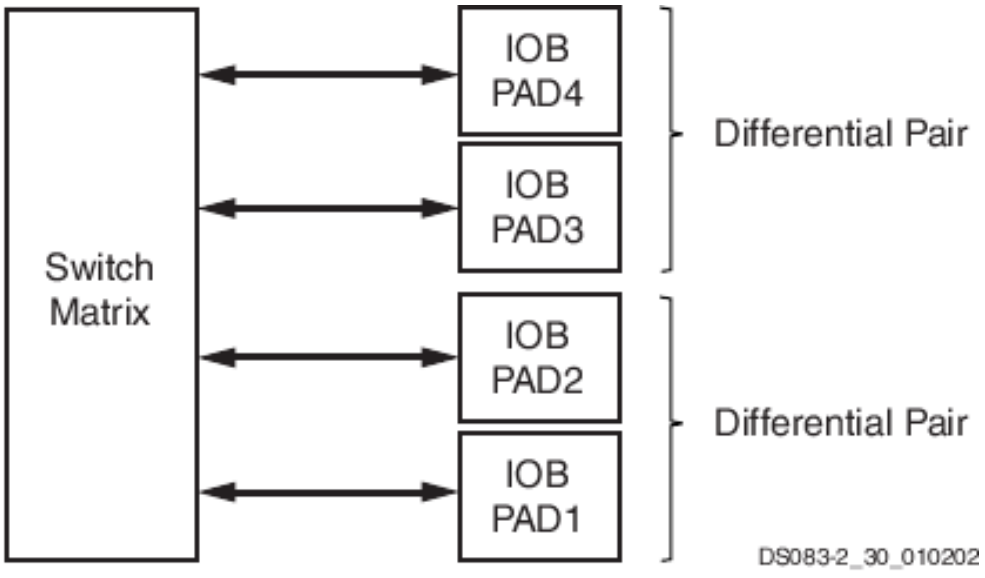


Figure 18: **Virtex-II Pro Input/Output Tile**

Note: Differential I/Os must use the same clock.

I/O Blocks Details

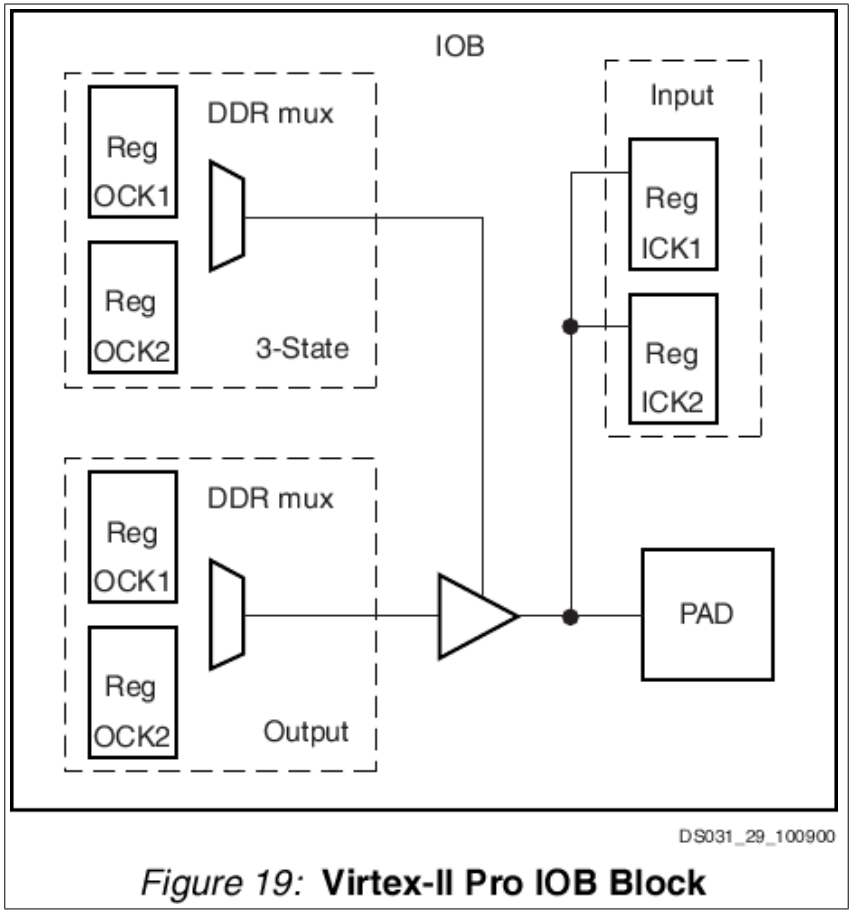


Figure 19: **Virtex-II Pro IOB Block**

I/O Banks

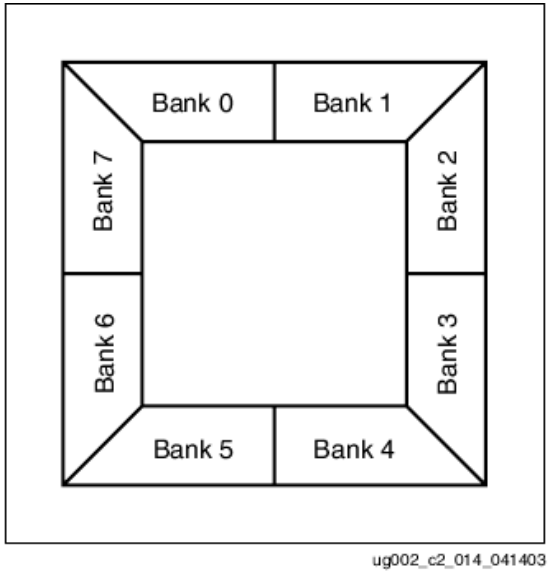


Figure 24: **I/O Banks: Wire-Bond Packages (FG) Top View**

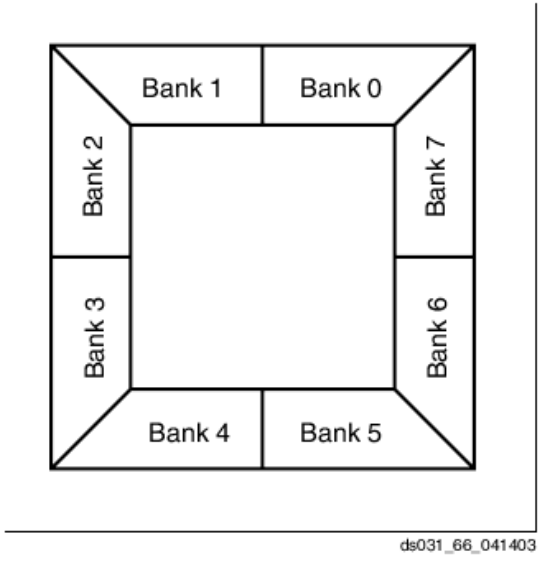


Figure 25: **I/O Banks: Flip-Chip Packages (FF) Top View**

Routing Resources

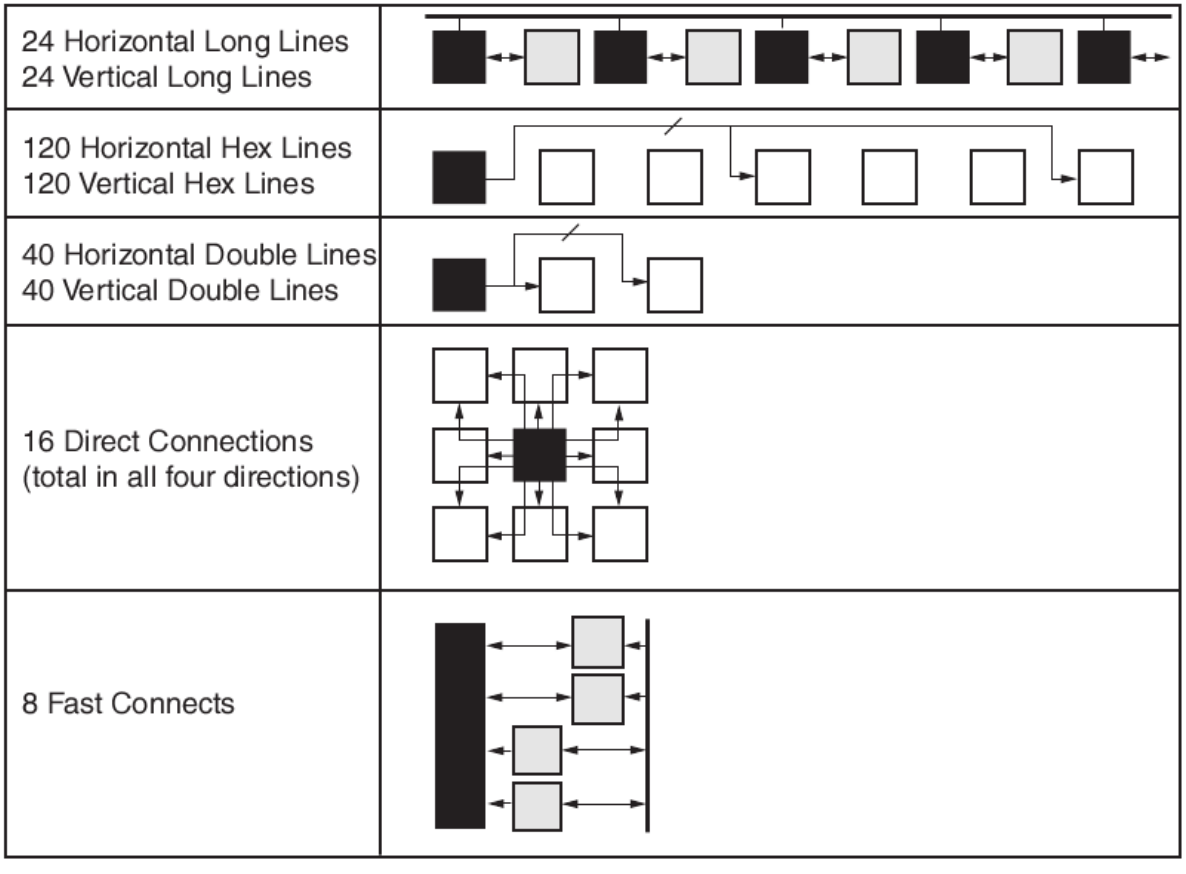


Figure 64: **Hierarchical Routing Resources**

PowerPC Core

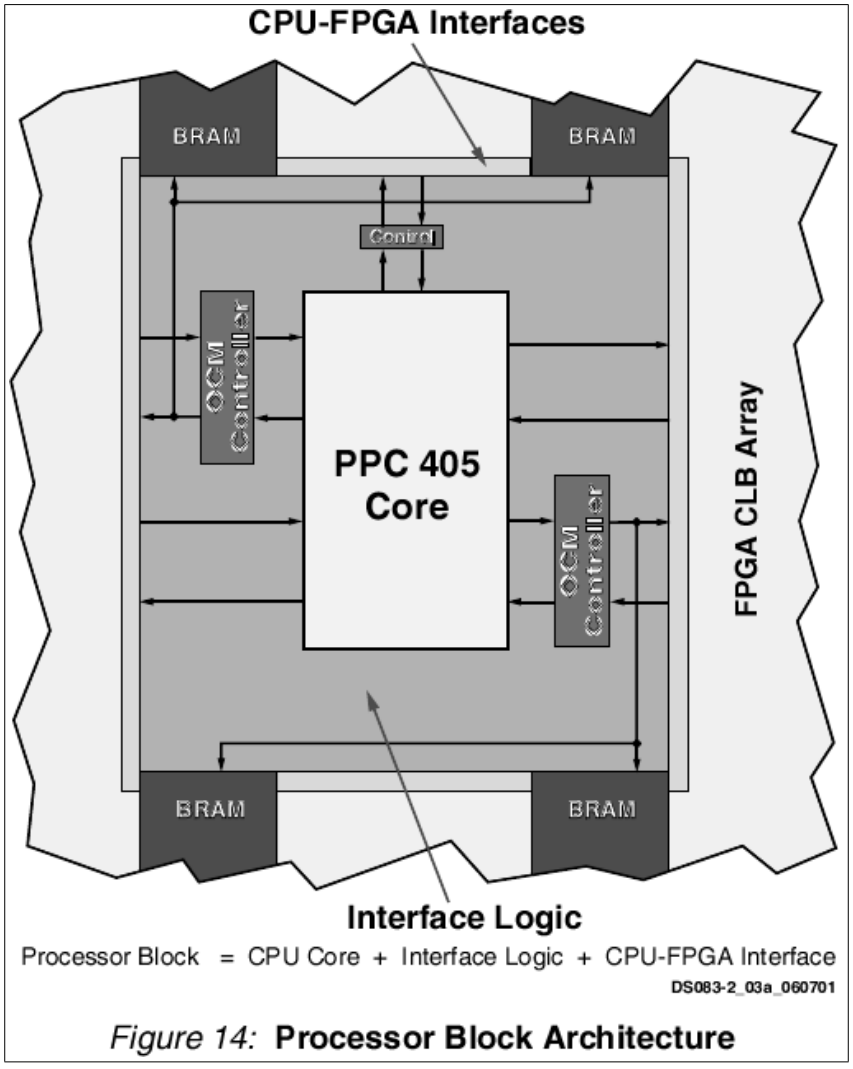


Figure 14: **Processor Block Architecture**

Block SelectRAM+ (Dual-Port Example)

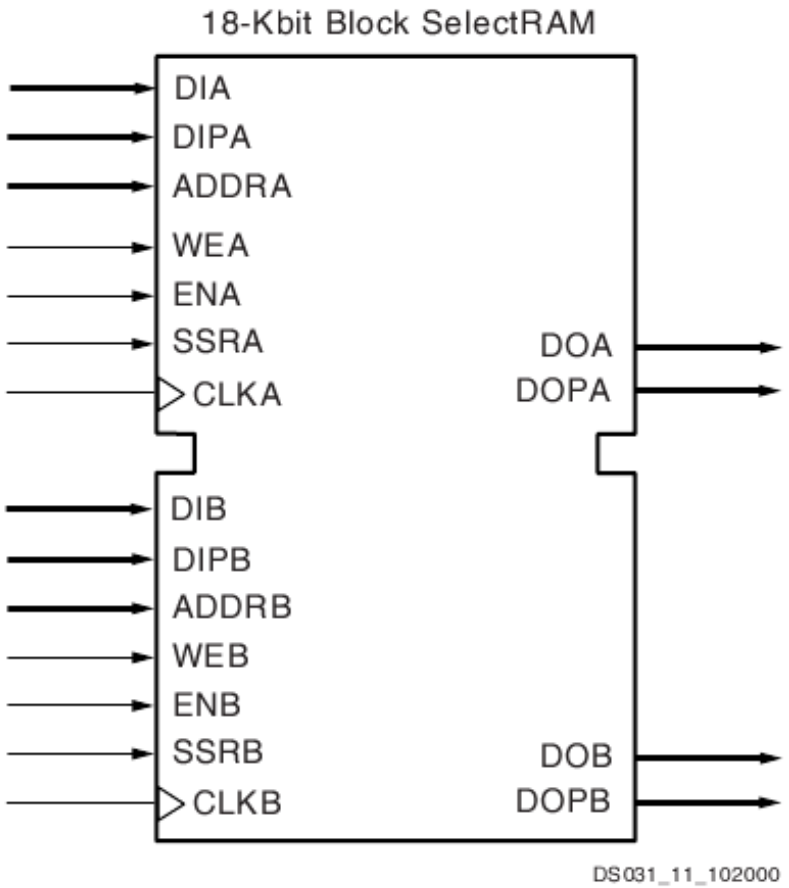


Figure 48: **18 Kb Block SelectRAM+ in Dual-Port Mode**

Block SelectRAM+ (Configuration Options)

Table 22: **Dual-Port Mode Configurations**

Port A	16K x 1	16K x 1	16K x 1	16K x 1	16K x 1	16K x 1
Port B	16K x 1	8K x 2	4K x 4	2K x 9	1K x 18	512 x 36
Port A	8K x 2	8K x 2	8K x 2	8K x 2	8K x 2	
Port B	8K x 2	4K x 4	2K x 9	1K x 18	512 x 36	
Port A	4K x 4	4K x 4	4K x 4	4K x 4		
Port B	4K x 4	2K x 9	1K x 18	512 x 36		
Port A	2K x 9	2K x 9	2K x 9			
Port B	2K x 9	1K x 18	512 x 36			
Port A	1K x 18	1K x 18				
Port B	1K x 18	512 x 36				
Port A	512 x 36					
Port B	512 x 36					

Column Layout of IC

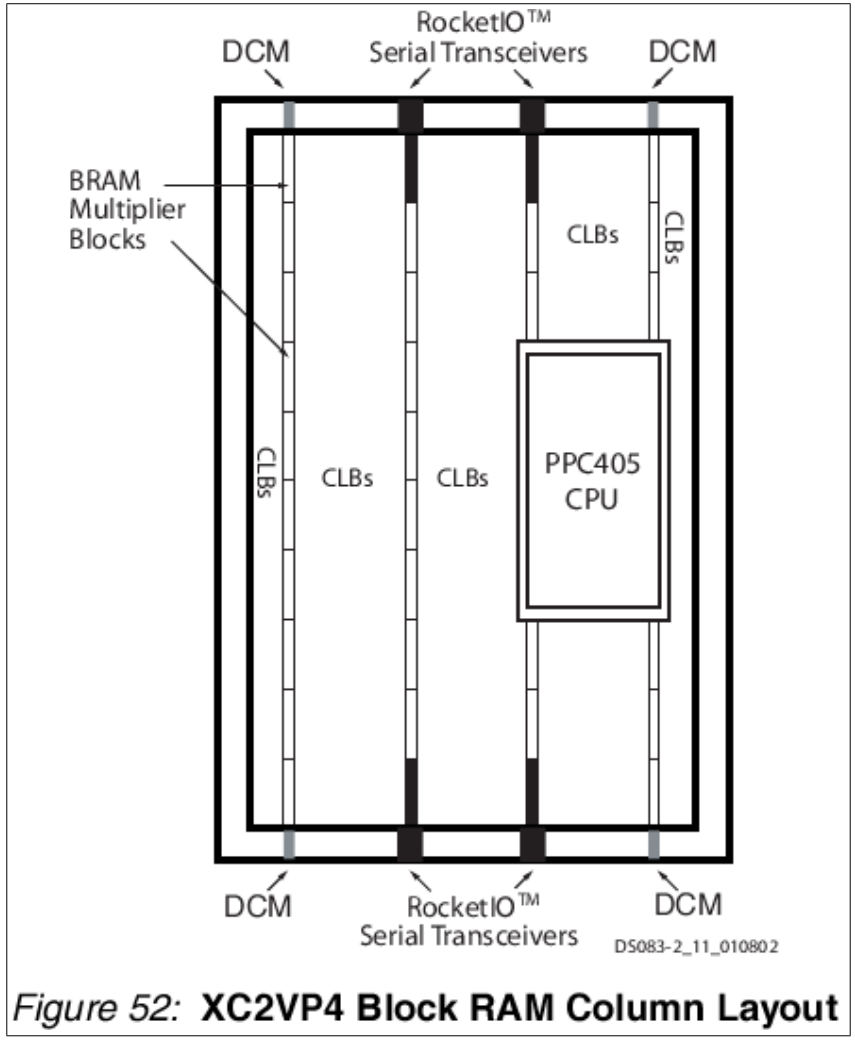


Figure 52: **XC2VP4 Block RAM Column Layout**

Block SelectRAM+ and Multipliers

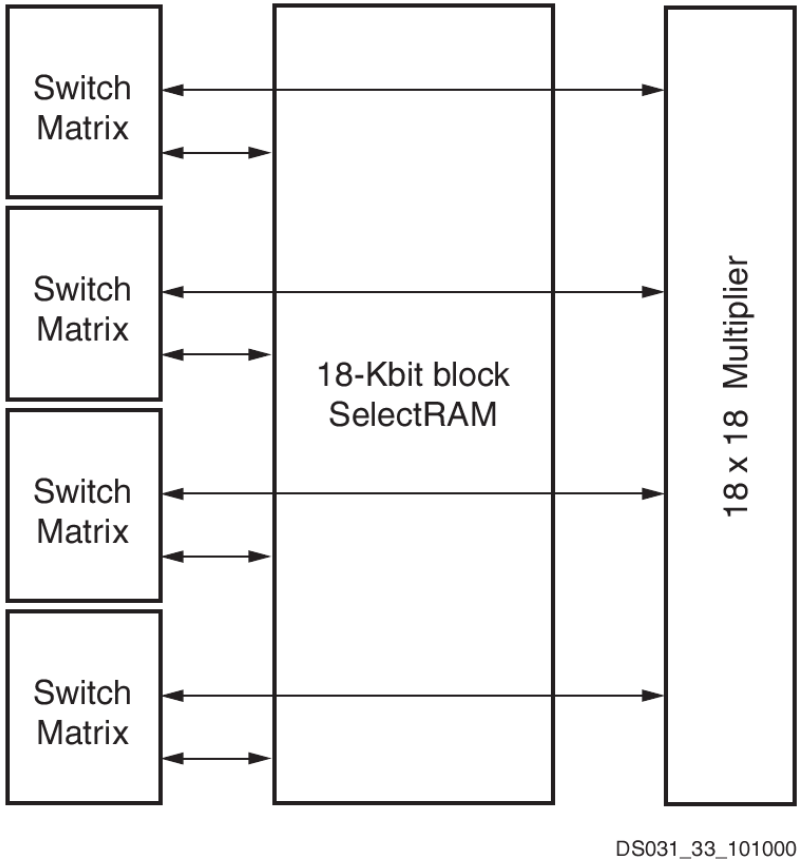


Figure 53: **SelectRAM+ and Multiplier Blocks**

Multi-Gigabit Transciever

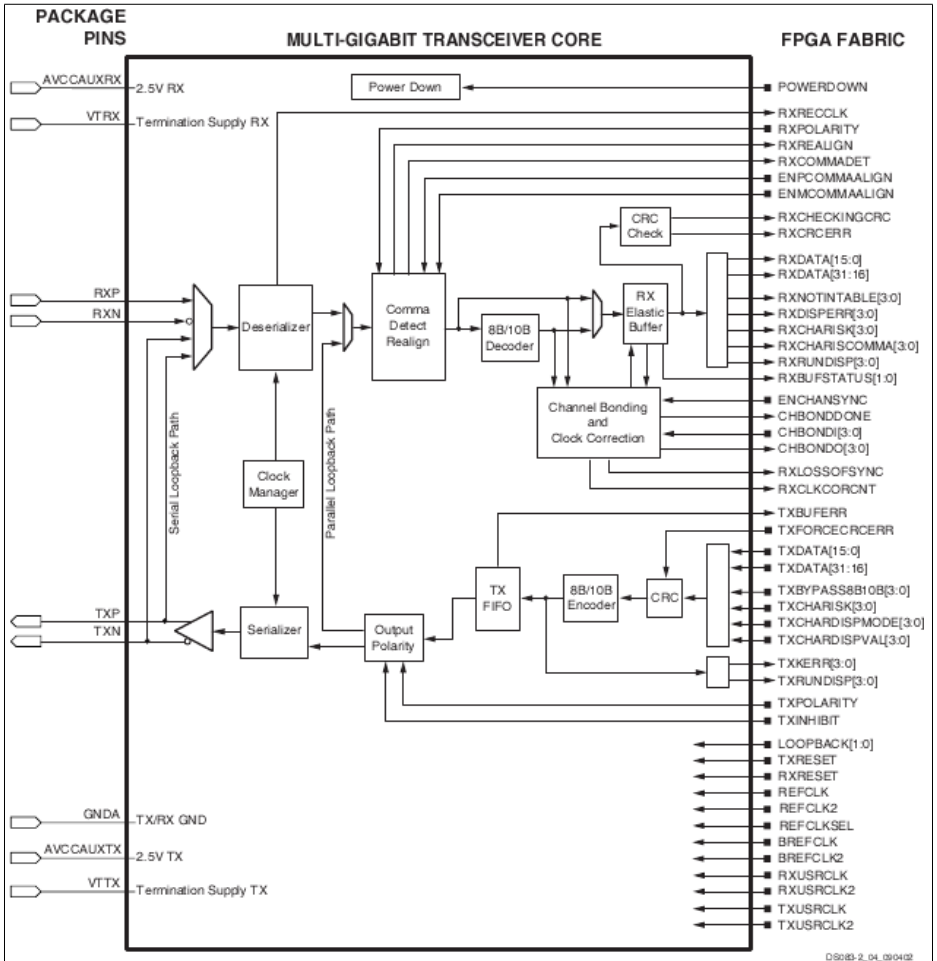


Figure 10: **RocketIO Transceiver Block Diagram**

Available Chip Sizes

Table 19: **Logic Resources in One CLB**

Slices	LUTs	Flip-Flops	MULT_ANDs	Arithmetic & Carry-Chains	SOP Chains	Distributed SelectRAM+	Shift Registers	TBUF
4	8	8	8	2	2	128 bits	128 bits	2

Table 20: **Virtex-II Pro Logic Resources Available in All CLBs**

Device	CLB Array: Row x Column	Number of Slices	Number of LUTs	Max Distributed SelectRAM or Shift Register (bits)	Number of Flip-Flops	Number of Carry-Chains(1)	Number of SOP Chains(1)
XC2VP2	16 x 22	1,408	2,816	45,056	2,816	44	32
XC2VP4	40 x 22	3,008	6,016	96,256	6,016	44	80
XC2VP7	40 x 34	4,928	9,856	157,696	9,856	68	80
XC2VP20	56 x 46	9,280	18,560	296,960	18,560	92	112
XC2VPX20	56 x 46	9,792	19,584	313,334	18,560	92	112
XC2VP30	80 x 46	13,696	27,392	438,272	27,392	92	160
XC2VP40	88 x 58	19,392	38,784	620,544	38,784	116	176
XC2VP50	88 x 70	23,616	47,232	755,712	47,232	140	176
XC2VP70	104 x 82	33,088	66,176	1,058,816	66,176	164	208
XC2VPX70	104 x 82	33,088	66,176	1,058,816	66,176	164	208
XC2VP100	120 x 94	44,096	88,192	1,411,072	88,192	188	240

Notes:
1. The carry-chains and SOP chains can be split or cascaded.