Guide to Verifying Saturation Operation
A Cadence Help Document

Overview

In order for most analog circuits to work properly all transistors need to be biased in the saturation (active) region. When designing circuits, it is important to verify this throughout the simulation process. Locating transistors that are not properly biased in saturation is a useful way of debugging a circuit and can help explain unexpected results.

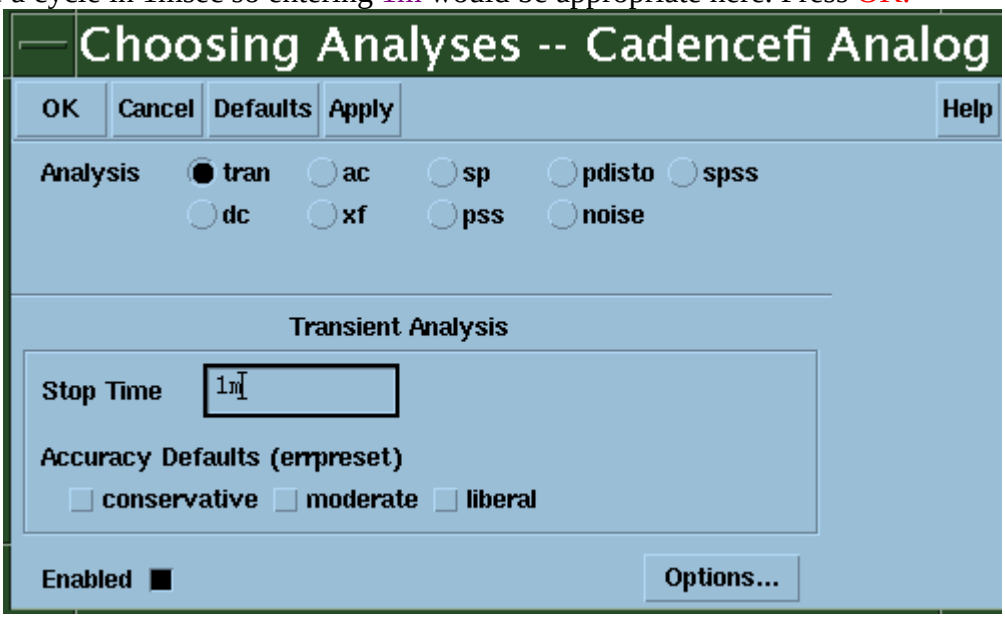
Most simulators provide a way to observe the operating point conditions of a circuit. These values form the initial conditions when the simulator solves the equations that model a circuit. In most simulators, these operating point conditions are associated with a transient analysis.

Setup

- With the schematic of your circuit complete, add the appropriate DC bias sources (power supply, input voltages/currents, etc.).
    - ECE418 op amp design: provide a VDD source and a Vmid source at the inputs
- Add a sinusoidal voltage source to the input. typical values for this source would be 100mV amplitude and 1kHz frequency. If this same source will be used for AC analysis, set the AC magnitude to 1V.
    - ECE418 op amp design: simulate the open loop configuration with the transient source applied to the positive input, much like the circuit for measuring Vos, gain, gain bandwidth, and phase margin.

Procedure

- In the Cadence Analog Design Environment window, select Analyses => Choose
- In the Choosing Analysis window, choose tran as analysis type to select a transient (verse time) analysis and enter a Stop Time appropriate for the input signal. For example, a 1kHz input will complete a cycle in 1msec so entering 1m would be appropriate here. Press OK.



- Select the output and input nodes as the outputs to be plotted and run the simulation (select Simulation => Run). Transient analysis waveform will appear in a new window.
- Observer the output waveform. For the values mentioned above, you should see one phase of the sine wave input and the output response. This plot itself can generally provide much valuable information about the circuit and whether or not it is operating properly.
- To verify each transistor is operating in saturation, in the Cadence Analog Design Environment window, select Tools => Results Browser
- In the Results Browser window, go to psf/ => Run1 => finalTimeOP-info. Check each transistor one at a time to verify saturation operation
    - either, observe vds, vgs, vth, and vdsat (vdsat = vgs-vth, vth = threshold voltage) determine if saturation conditions are met
    - or, verify each transistor is operating in **region** 2, which is saturation
- If any transistors are out of the saturation region (Vds less than Vdsat) adjust W/L or Id to get a lower Vdsat or to increase the Vds of that transistor. A Vdsat around 200mV to 500mV is a typical/reasonable result.