Design and Implement of BPSK Modulator and Demodulator Based on Modern DSP Technology

Wenmiao Song ,Jingying Zhang, Qiongqiong Yao
Dept. of Electronic & Communication Engineering
North China Electric Power University
Baoding, China
jingying1957@163.com

***Abstract*—This paper presents a method to design BPSK modulator and demodulator. The method makes use of modern DSP technology which uses the tool of DSP Builder of American Altera Co. The direct digital synthesis (DDS) principle is briefly presented and used to design orthogonal cosine signal module. In demodulator, we use the low pass FIR filtering IP core to filter high frequency component. The BPSK modem is ultimately implemented on the FPGA device. This design uses MATLAB/Simulink, DSP Builder 7.2, ModelSim 6.1g and Quartus Ⅱ 7.2 to simulate and realize directly BPSK modulator and demodulator based on FPGA, using DSP Builder to substitute the VHDL programming, has the organic integration in modeling and hardware implementation on the same work bench. The method can greatly improve the developing efficiency, shorten developing period and reduce costs. The practice has proved the accuracy and validity of the method.**

Keywords-BPSK; DDS; IP core; FIR; DSP Builde

I. INTRODUCTION

DDS is a new technology of Frequency Synthesis. It develops the third generation of Frequency Synthesis Technology after Direct Frequency Synthesis and Indirect Frequency Synthesis, and breaks through the theory of the former two methods of Frequency Synthesis. Reference [1] pointed that the technique of DDS is gaining popularity as a method of generating sinusoidal signals and modulated signals in digital systems.

Modern DSP technology is that the EDA design technology is used to develop DSP on FPGA chip. DSP Builder is a DSP-oriented system level design tool developed by American Altera Co. It appears as a toolbox in Simulink of MATLAB. What the designer needs is to fulfill the harmonic checking algorithms and processing procedure in simulation of MATLAB by DSP Builder. Reference [2] has verified that if the file passes the examination and can be compiled, then it can be downloaded to FPGA. As a result, the FPGA performs the corresponding functions according to the downloaded orders. The complicated software programming process is omitted. So the developing speed is quickly, and developing speed is fasten, and developing period and costs are lowered.

II. THE PRINCIPLE OF DDS

In the simplest case a Direct Digital Synthesis is constructed by a ROM with many samples of a sine wave stored in it (sine look-up table, LUT) and it was introduced in [3]. Fig.1 shows the block diagram of a DDS system. The DDS produces sinusoidal signals at a given frequency by digital integration of a higher clock frequency. The Phase Accumulator stage accepts the so called Frequency Setting Word (FSW) which determines the phase step. Once set, this digital word determines the sine wave frequency to be produced. The phase accumulator then continuously produces in the output proper binary words indicating the instantaneous phase to the table look-up function. In other words the phase accumulator is used to "calculate" the successive addresses of the sine look-up table which generates a digital sine-wave output. In this way the samples are swept in a controlled manner i.e. with a step depending on the Frequency Setting Word. The DDS translates the resulting phase to a sinusoidal waveform via the look-up table, and converts the digital representation of the sine-wave to analog form using a Digital-to-Analog Converter followed by a low pass filter (LPF).

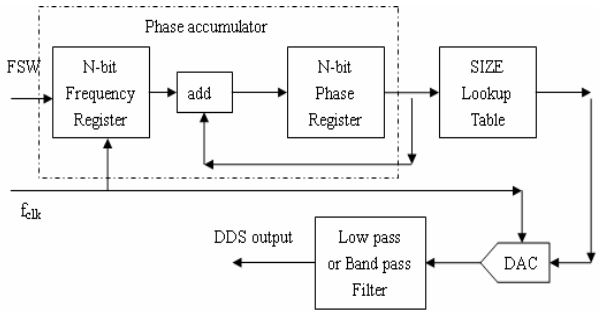

Figure 1. Block diagram of a DDS system

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The digital part of the DDS, i.e. the phase accumulator and the LUT, is usually called a Numerically Controlled Oscillator (NCO).The frequency of the output signal for a M-bit system is determined by the following equation:

$$f_o = \frac{K \times f_{clk}}{2^M} \tag{1}$$

Where K is the FSW, M is the number of bits that the phase accumulator can handle and f_{clk} is the generator clock frequency in HZ.

III. SYSTEM DESIGN AND IMPLEMENT BASED ON MODERN DSP TECHNOLOGY

In our design, we use model-based design tools like Simulink with the libraries of DSP Builder. The DSP Builder uses model design to produce and synthesize HDL code, which can then be integrated with other hardware design files within a synthesis tool, like the Quartus II development environment, and this method has been introduced in [4]. In the present, we design DDS and fir filter using DSP Builder libraries to implement BPSK modem and the resulting blocks were integrated in Quartus II system.

A. The DDS model based on DSP Builder

According to the basic principles of DDS, DDS model is built in the Matlab/ Simulink software by using FPGA and DSP development tools, DSP Builder. The orthogonal signals generator application model based on DDS technology is built by Quartus II software. The configuration of DDS subsystem is shown in Fig.2, which is the DDS model based on DSP Builder. There are three inputs, such as a 32-bit frequency control words (Freq word), a 16-bit phase control words (Phase word) and a 10-bit amplitude control words (Amp), there are two outputs of 10-bit Output2 and Output3, there are two Parallel Adder Subtractors, phase accumulator and phase modulators, and a LUT for the sine ROM look-up table is also adopted in the DDS subsystem.

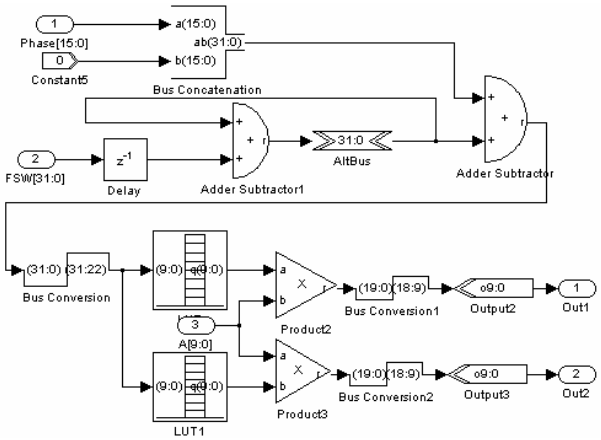

Figure 2. The DDS subsystem based on DSP Builder

B. The model design of BPSK modem

Based on the principle of BPSK modulator-demodulator, the architecture is built with some basic modules in DSP Builder and it can be seen in Fig.3.

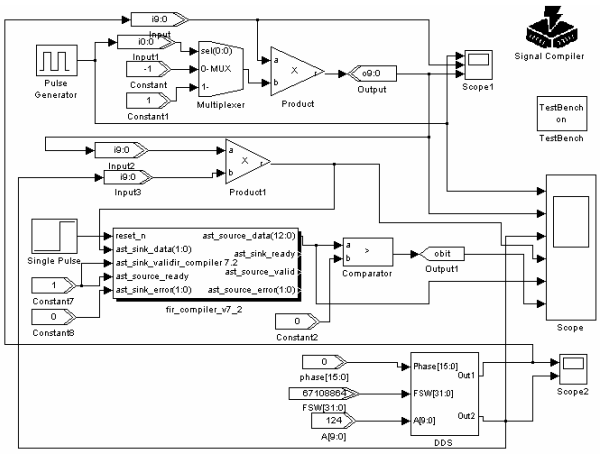

Figure 3. The architecture of BPSK modem

In Fig.3, two same sine carriers are generated from DDS. Pulse Generator is used to simulate pulse source signal for the modulator and the output is binary sequence; Multiplexer realizes the conversion of code type; the other are I/O ports. The binary pulse is input from Input1 and multiplied with sine carrier, the result is output from Output. The modulated signal multiply with sine wave, then the fir_compiler_v7.2 filter the high frequency parts, and the demodulated signal can be obtain from Output1 after Comparator. The BPSK modem is compiled in the Simulink development environment of MATLAB software. Setting correlation parameter of model, the VHDL language of BPSK modem is generated by DSP Builder Signal Compiler tool.

IV. SIMULATION RESULTS AND ANALYSIS

Here we adopt the DSP Builder tool to carry out the algorithms system level design. It is a DSP development tool that interfaces the MathWorks system-level DSP tool Simulink with Quartus II development software. Once we complete the algorithmic modeling, simulation and system integration in MATLAB and Simulink, the DSP Builder can automatically generate HDL files which are at the register transfer level (RTL).The RTL level simulation is performed by the ModelSim simulator where we can verify that the RTL simulation results match the Simulink simulation results (system level).The FPGA implementation and test is achieved using Quartus II and the Cyclone II EP2C5F256C6 DSP development board.

Fig.4 shows the simulation result of DDS in Simulink. Two same of sine wave are output from DDS. The LUT sin wave or cosine wave look-up table is described by the formula, 511*sin([0:2*pi/2^10:2*pi]). The word length of phase modulator, M, is equal to 32, f_{clk} is 65536HZ, and f_0 is 1024HZ. The phase control words the frequency control word, K, and the amplitude

control words are set as 0, 67108864 and 124, respectively.

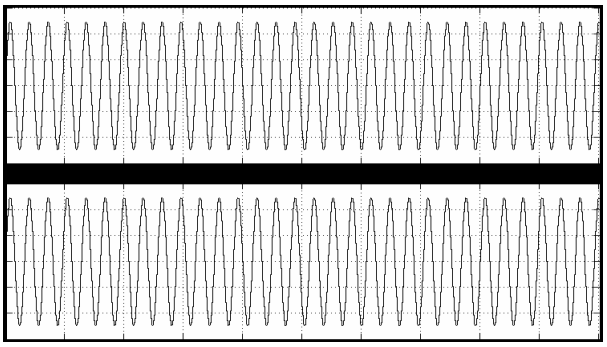

Figure 4. The outputs of DDS

The results of BPSK modem can be seen in Fig.5.

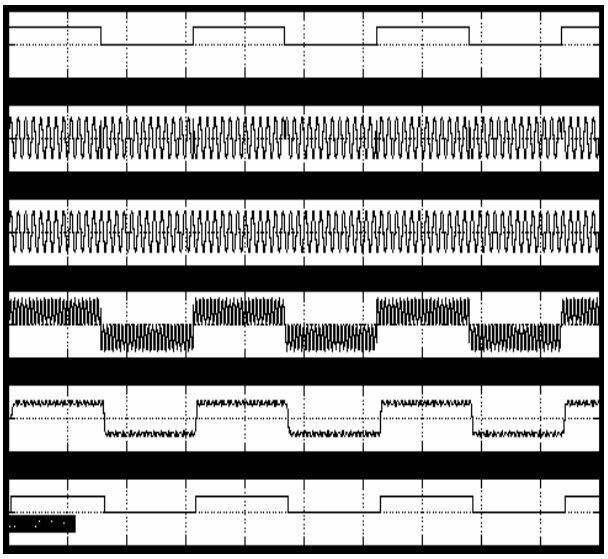

Figure 5. The results of BPSK modem

The RTL simulation result is shown in Fig.6 and Fig.7 shows simulation waveforms under Quartus II 7.2.

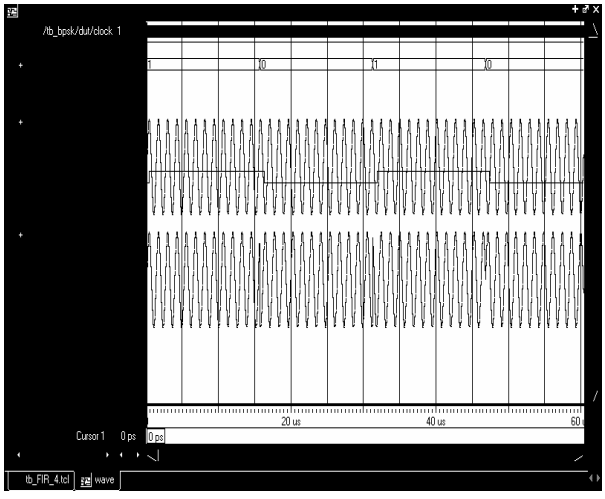

Figure 6. The output cave in ModelSim

In Fig.5, the first is binary pulse signal, the second is modulated data, the third is modulator and demodulator carrier, the forth is output from Product1, the fifth is signal from FIR IP core, the last is output after Comparator. Fig.5 shows that the demodulator result is in agreement with input pulse signal, and we obtain the same result from ModelSim simulator by Fig.6. So the architecture of BPSK modem can implement the function that we want. The method has the organic integration in modeling and hardware implementation on the same work bench

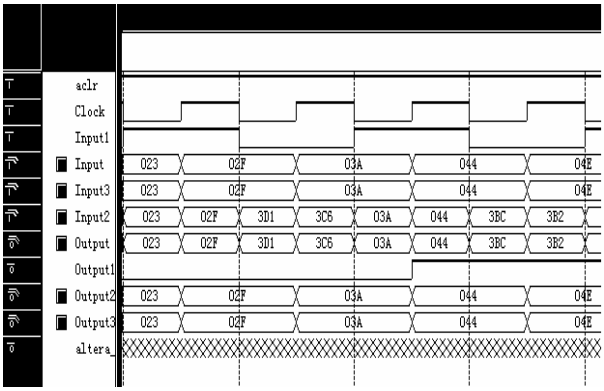

Figure 7. Simulation waveforms under Quartus II

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