Integrated Balanced Sampling Circuit for Ultra-Wideband Communications and Radar Systems

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***Abstract*—A balanced sampling circuit realized using step recovery and Schottky diodes on coplanar waveguide, coplanar strips, and slotlines is presented for ultra-wideband communications and radar applications. An efficient design was implemented to achieve improved performance. The impulse generator, providing signal for the sampling gate, was designed with a new LO feeding structure. The fabricated circuit shows 16–19 dB conversion loss without amplifier and 1–4 dB conversion gain with amplifier across 9-GHz RF bandwidth with 500-MHz sampling frequency.**

***Index Terms*—Impulse generator, radar, sampling circuit, sampling mixer, ultra-wideband (UWB).**

I. Introduction

RECENTLY, ultra-wideband (UWB) communications and radar systems, operating up to 10 GHz, have received significant attention for various applications such as low interference, high data rate, short-range communications [1], and unexploded ordance and mine detection [2]. Sampling circuit is one of the most important components in these systems. Especially, low-cost, compact and simple sampling structures are needed for reducing the cost, size and complexity of UWB communications and radar systems. A sampling circuit operating beyond 50 GHz has been reported using microwave monolithic integrated circuit (MMIC)-based nonlinear transmission lines [3], which is attractive for millimeter-wave applications such as network analyzers and digitizing oscilloscopes. MIC-based sampling circuits have also been developed below 20 GHz and are suitable for UWB systems [4]–[6]. The sampler presented in [4] operates to 18 GHz. However, it uses double-sided circuitry, has relatively high conversion loss, around 36–42 dB, and requires high LO level. The sampler reported in [5] is uniplanar and has a conversion gain of 15 dB (with amplifier). However, it operates only to 3 GHz. The other sampler [6] has a conversion loss of 9 dB over a bandwidth of 6 GHz and uses a transformer balun implemented with ferrite ring, which is not planar. Some analyses were also reported for sampler [7], [8].

Practically, it is relatively difficult to design a sampler with wide bandwidth and high conversion efficiency using the hybrid MIC technology. To achieve such a component, one needs to carefully design the circuit considering important sampler design and operating factors based on extensive theoretical analysis. In this paper, we report on the development of a new balanced sampler using hybrid MIC with improved performance for UWB communications and radar applications. The sampler operates over a 9-GHz bandwidth, much wider than that reported in [5] and with a conversion loss of 16–19 dB, much lower than the sampler presented in [4]. It also needs only 12 dBm of driving LO signal as compared to 20-dBm LO reported in [4]. Uniplanar structure is used for simplicity and low cost. A modified LO-RF coupling structure to the sampling diodes is used to minimize the distortion of the LO pulse signal and, eventually, maximize the circuit performance. A simple and effective LO feeding structure is designed to integrate the internal pulse generator, based on shunt-mode step recovery diode (SRD), with the sampling circuit.

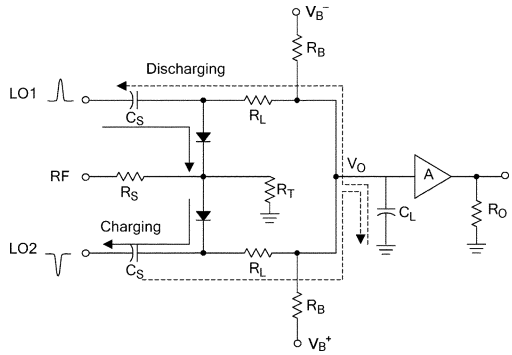

Fig. 1. Balanced sampling circuit.

II. Circuit Analysis

To determine the important circuit parameter values and the factors needed to be considered in the design, extensive time-domain transient signal analysis of the balanced sampling circuit, shown in Fig. 1, has been performed. Important facts about conversion efficiency and bandwidth of the circuit follows.

1) The sampling diode is ON during the LO pulse, but the diode's effective ON duration can be reduced by using a high barrier diode, which results in increased bandwidth.
2) For proper operation, the diode should be OFF when the pulse is off. If RF signal level is greater than the diode contact potential, the diode can be turn-on in any time-interval. To obtain large dynamic range for the circuit, high barrier diode or reverse bias is required.

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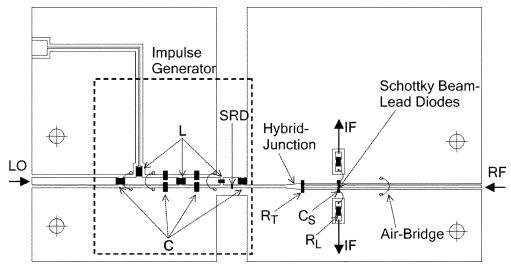

Fig. 2. Actual sampler layout.

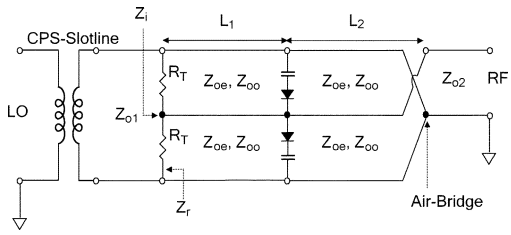

Fig. 3. Equivalent circuit model of the designed sampler.

3) High barrier diode or reverse bias would result in reduction of conversion efficiency for limited LO pulse amplitude.
4) Sampling capacitance $C_{\rm S}$ is determined by the required charging time constant for given LO pulse rising time. $C_{\rm S}$ should be small enough to have sufficient charging voltage.
5) The load resistance $R_{\rm L}$ should be large enough to obtain high conversion efficiency.

III. Circuit Design

Fig. 2 shows the overall layout of the sampling circuit with actual placement of the circuit components, including the impulse generator and LO feeding structure. The hybrid junction needed to provide the in-phase and 180° out-of-phase to the sampling diodes for the RF signal and LO pulse, respectively, is similar to that used in [5]. However, in this sampling circuit, we modified the coupled-slotline coupling structure to sampling diodes for the LO and RF signals and optimized it to reduce the distortion and multiple reflections of the LO pulse and hence improve the sampler performance. We also implement a new LO feeding structure to facilitate the integration of the impulse generator with the sampling circuitry and design the shunt-mode impulse generator as described in Section IV.

Fig. 3 shows the equivalent circuit model of the sampling circuit shown in Fig. 2. In Fig. 3, $R_{\rm T} = 100\ \Omega$ is used for RF termination. The air-bridge is used to decouple the LO pulse from the RF port. This air-bridge provides narrower LO pulse to sampling diodes if the distance L_2 is properly designed. To minimize pulse width without loss of amplitude, L_2 is such that round-trip time of the pulse is half of the generated pulse width.

The characteristic impedance of the feeding slotline, $Z_{\rm o1}$, should be equal to the input impedance at the slotline hybrid junction, $Z_{\rm i}$. For the even-mode LO pulse signal

$$Z_{\rm o1} = Z_{\rm i} = 2(R_{\rm T} \| Z_{\rm oe}) \tag{1}$$

where $Z_{\rm oe}$, the even-mode characteristic impedance of the coupled slotlines, is chosen as 55 Ω based on the physical size of the Schottky beam-lead diode. Therefore, $Z_{\rm o1} = 71\ \Omega$ according to (1). This impedance is also proper for the load impedance of the pulse generator. Another important thing we have to consider in this design is possible multiple reflections of the LO pulse between $R_{\rm T}$ and the air-bridge. To reduce these reflections, matching must be achieved at the hybrid junction. In Fig. 3, $Z_{\rm r}$ represents the impedance looking into $R_{\rm T}$ from the coupled slotlines. For a perfect matching condition, it is

$$Z_{\rm r} = (Z_{\rm o1} + (R_{\rm T} \| Z_{\rm oe})) \| R_{\rm T} = Z_{\rm oe}. \tag{2}$$

From (2), the desired characteristic impedance for $Z_{\rm o1}$ is

$$Z_{\rm o1} = R_{\rm T} Z_{\rm oe} \left(\frac{1}{R_{\rm T} - Z_{\rm oe}} - \frac{1}{R_{\rm T} + Z_{\rm oe}} \right) \tag{3}$$

which is equal to 86.7 Ω. This result shows that the previously designed value of 71 Ω for $Z_{\rm o1}$ can provide good matching condition for the reflected pulse signal and hence reducing unwanted multiple reflections on the coupled slotlines.

The location of the sampling diodes is also important for minimizing the LO pulse distortion. Since it is impossible to remove the reflection of the pulse from $R_{\rm T}$ completely, there would be a small reflection of the pulse to the diodes. To avoid this distortion effect, the sampling diodes are located a distance L_1 apart from $R_{\rm T}$, and L_1 should be the same as L_2.

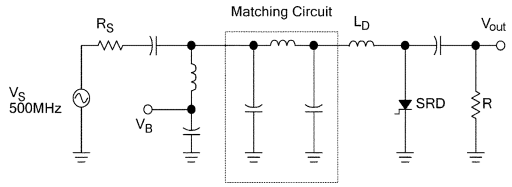

Fig. 4. Shunt-mode SRD impulse generator.

IV. Design of the Pulse Generator

The bandwidth of the sampling circuit is determined by the gating pulse width applied to the sampling diodes. Therefore, generation of a short-duration pulse is the most important thing for obtaining wide bandwidth. As we described in Section II, the actual gating time can be reduced from the generated pulse by using high barrier diodes or reverse-biasing the diodes. Furthermore, as shown in Section III, using air-bridge can further reduce the gating time. The pulse amplitude is also important. A large pulse-amplitude can transfer more charge to the sampling capacitors so as to improve the conversion efficiency. A large pulse amplitude driving high barrier diodes or diodes with more reverse biasing also improves the dynamic range of the circuit.

In sampling circuits, a step pulse is usually used to turn on and off the diodes. However, if an impulse is used, the resulting gating pulse composing of incident and reflected ones can have narrower pulse width than that using step pulse. Therefore, an impulse generator is designed and used for our sampling circuit.

The impulse generator employs a SRD and is based on a shunt-mode configuration [9] as shown in Fig. 4. The shunt mode is the most power efficient configuration for SRD impulse generators. The desired output pulse width is set to 100 ps and the damping factor is 0.67 to obtain $L_{\rm D} = 2$ nH and $R = 70\ \Omega$. The design is done to have the same R value as the input impedance at the slotline hybrid junction to satisfy the matching

condition at the junction. The SRD used is a beam-lead SRD, MMDB-30-B11 from Metelics, which has a junction capacitance of 0.25 pF, transition time of 35 ps, and minority carrier lifetime of 5 ns. The frequency of LO driving source signal, 500 MHz, is used and is greater than the inverse of the minority carrier lifetime to minimize loss of output pulse power.

Fig. 2 shows the layout of the impulse generator part and the LO feeding to the diodes via slotline, showing the placement of the SRD and other components. The 500 MHz sinusoidal LO driving signal is fed via CPW and used to generate the impulse by means of the SRD connected in a shunt mode, which is then guided to the sampling diodes via slotline, necessitating the use of a CPW-slotline transition. However, a conventional CPW-slotline transition cannot be used here because of the shunt-connected SRD and series-connected blocking capacitor. Therefore, we have designed a new transition structure for this application as shown in Fig. 2. The transition is actually composed of 2 transitions. One is CPW-to-CPS and the other is CPS-to-slotline. Using this simple structure, we can obtain a smooth transition from CPW to slotline while the circuit components are properly placed.

V. Fabrication and Measurement Results

The entire sampling circuit including the pulse generator and IF circuit is fabricated on a single circuit board of 3 × 2 in using RT/Duroid RO3010 substrate having a relative dielectric constant of 10.2 and a thickness of 50 mil. The sampling diode is a beam-lead Schottky diode with high barrier junction, MSS-50 146-B10B provided by Metelics. The high barrier Schottky diode is selected to facilitate wide bandwidth for the sampling circuit without bias. The contact potential of the diode is 0.5 V. Diode parameter values are used to calculate the sampling capacitance C_{S} and discharging resistance R_{L} (see Section I). The IF circuit consists of a single-ended noninverting op-amp circuit and biasing circuit for sampling diodes.

The measured return loss at the LO driving port is 30 dB for a driving frequency of 500 MHz and for a SRD bias of 0.6 V. For the RF port, the measured return loss is in the range of 7–25 dB for 1–10 GHz frequency range.

Fig. 5 shows the measured LO pulse signal propagating through one slot of the coupled slotlines where a diode is mounted. The half-amplitude pulse width is about 100 ps. The pulse amplitude is about 0.6 V, so that we may use 0.5-V high barrier diode. This pulse signal is generated from a 12-dBm input driving signal. As indicated in Fig. 5, if we apply proper reverse bias voltage to the sampling diodes, 50-ps gating time can be obtained. Using the approximate bandwidth calculation formula, $\mathrm{BW(GHz)} \approx 350/\mathrm{Gating\ Duration\ (ps)}$, we expect that this circuit may have more than 7-GHz bandwidth using a 50-ps gating pulse.

Fig. 6 shows the measured conversion loss of the sampling circuit without the video amplifier. The driving LO power is 12 dBm. As can be seen, for a 3-dB RF bandwidth of 9 GHz, the conversion loss is from 16 to 19 dB. The measured output IF signal is 2 MHz. With an amplifier of about 20-dB gain, the sampling circuit displays a conversion gain from around 1 to 4 dB across the 9-GHz bandwidth. The measured 1-dB compression input power is about 8.5 dBm.

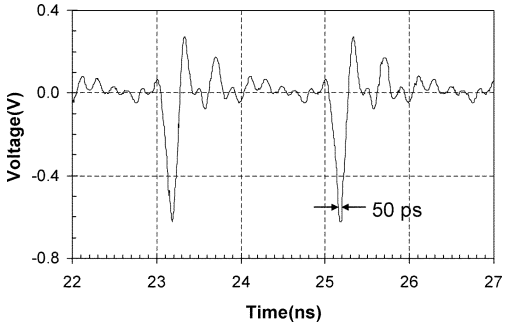

Fig. 5. Measured LO pulse signal at one of the sampling diodes.

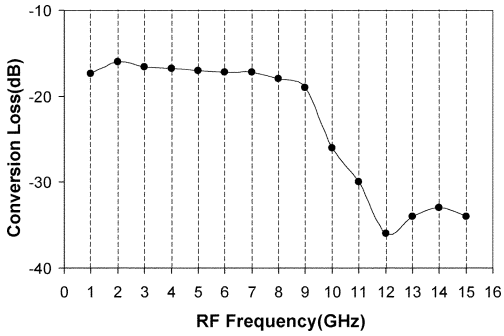

Fig. 6. Measured conversion loss of the sampling circuit.

VI. Conclusion

A new integrated balanced sampling circuit including impulse generator and IF amplifier has been developed using SRD, Schottky diodes, CPW, CPS and slotlines. The circuit displays a conversion loss from 16 to 19 dB (without amplifier) and a conversion gain from 1 to 4 dB (with amplifier) for a 9-GHz RF bandwidth. The circuit is simple to fabricate and low cost, and is intended for UWB communications and radar systems. Design information described in this paper should be valuable for other sampler development.

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