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# Differential Amplifier Input Impedance and Blackman's Impedance Relation

CLAUDE S. LINDQUIST

***Abstract*—Recently the input impedance of a differential amplifier was derived and discussed. This correspondence derives similar results using a different approach, namely, Blackman's impedance relation, and generalizes earlier observations. The results provide an alternative active *RC* realization of a bilinear *RL* impedance. Various all-pass networks are also analyzed.**

A recent letter derived and described the input impedance of a differential amplifier and presented an illustrative example [1]. This correspondence derives the input impedance using another approach, namely, Blackman's impedance relation, and proceeds to generalize and apply the results. It provides an alternative active $RC$ realization for bilinear $RL$ impedances. The input impedance of several recent all-pass networks are also derived and are discussed to illustrate these results.

To begin, consider the differential amplifier embedded in external circuitry, as shown in Fig. 1. The differential amplifier is shown inside the dotted lines; the inverting port voltage is $V_c$ and the noninverting port voltage is $V_d$. A simplified amplifier model is used that neglects the cross-coupling between inputs and the reverse transmission from the output to either input. Also, the forward channel gains are assumed to be equal in magnitude. The input impedances are $Z_{i1}$ and $Z_{i2}$ and the output impedance is $Z_o$. The forward gain is $A$. This model is adequate for the discussion here. We intend to extend the model to include common-mode effects in the near future. Following the condition of [1, eq. (9)] where the open-circuit voltage $E_b$ is linearly related to $E_a$, the noninverting voltage port is driven from a voltage source $K(s)E_a$ through the voltage divider consisting of $Z_2$ and $Z_3$. In the equations that follow, $K(s)$ is simply expressed as $K$.

The input impedance $Z_b$ of the noninverting channel equals $E_b/I_b$ and can be written immediately as

$$Z_b = Z_2 + Z_3 \| Z_{i2} = Z_2 + \frac{Z_3 Z_{i2}}{Z_3 + Z_{i2}}. \tag{1}$$

Under the condition that $Z_{i2} \gg Z_3$, which is usually the case,

$$Z_b = Z_2 + Z_3. \tag{2}$$

The input impedance $Z_a$ of the inverting channel was derived in [1] from basic network equations. $Z_a$ is given by (8) and is a function of $Z_1$, $Z_2$, $Z_3$, and $K$ under limiting gain $A$ conditions. We will derive the input impedance utilizing Blackman's impedance relation as an alternative approach. It is particularly illuminating to those familiar with feedback network theory.

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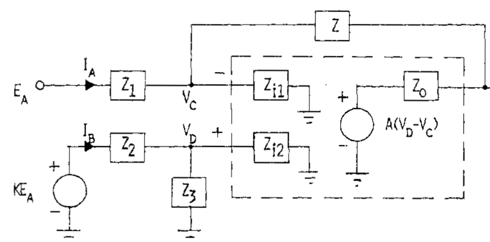



Fig. 1. Differential amplifier embedded in external circuitry.

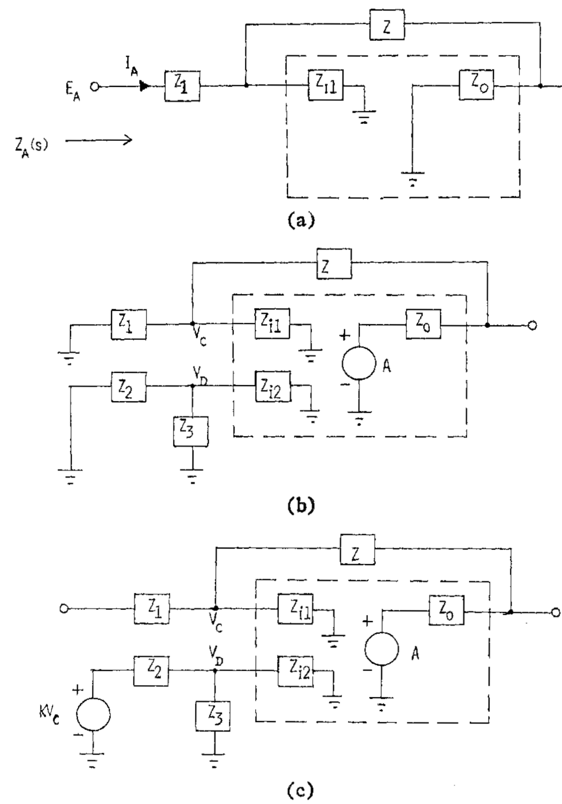



Fig. 2. Calculation of $Z_a(0)$, $T_s$, and $T_\infty$ terms in Blackman's impedance relation. (a) Input impedance of system in reference state. (b) Calculation of short-circuit return ratio $T_s$. (c) Calculation of open-circuit return ratio $T_\infty$.

Blackman's impedance relation states [2], [3]

$$Z(k) = Z(0)\,\frac{1 + T_s}{1 + T_\infty} \tag{3}$$

where $Z(k)$ and $Z(0)$ are driving-point impedances of the port of interest when the system is in its normal and reference states ($k = 0$), respectively; $T_s$ and $T_\infty$ are the system return ratios for coupling $k$ under short-circuit and open-circuit port conditions, respectively.

Let us choose the voltage source $A(V_d - V_c)$ as the source of interest having strength $A$. Setting $A = 0$, the driving-point impedance $Z_a(0)$ for the system in the reference state shown in Fig. 2(a) is

$$Z_a(0) = Z_1 + Z_{i1} \| (Z + Z_o). \tag{4}$$

The short-circuit return ratio $T_s$ is readily determined by replacing the dependent voltage source by an independent voltage source having strength $A$, shorting the input port, and calculating $T_s$ which equals $-(V_d - V_c)$ under these conditions. Thus from Fig. 2(b)

$$T_s = -(V_d - V_c)\Big|_{\substack{E_a=0\\ \text{thus } E_b=0}} = V_c\Big|_{E_a=0=E_b} = A\,\frac{Z_1 \| Z_{i1}}{Z + Z_o + Z_1 \| Z_{i1}}. \tag{5}$$

The open-circuit return ratio $T_\infty$ is obtained by instead open-

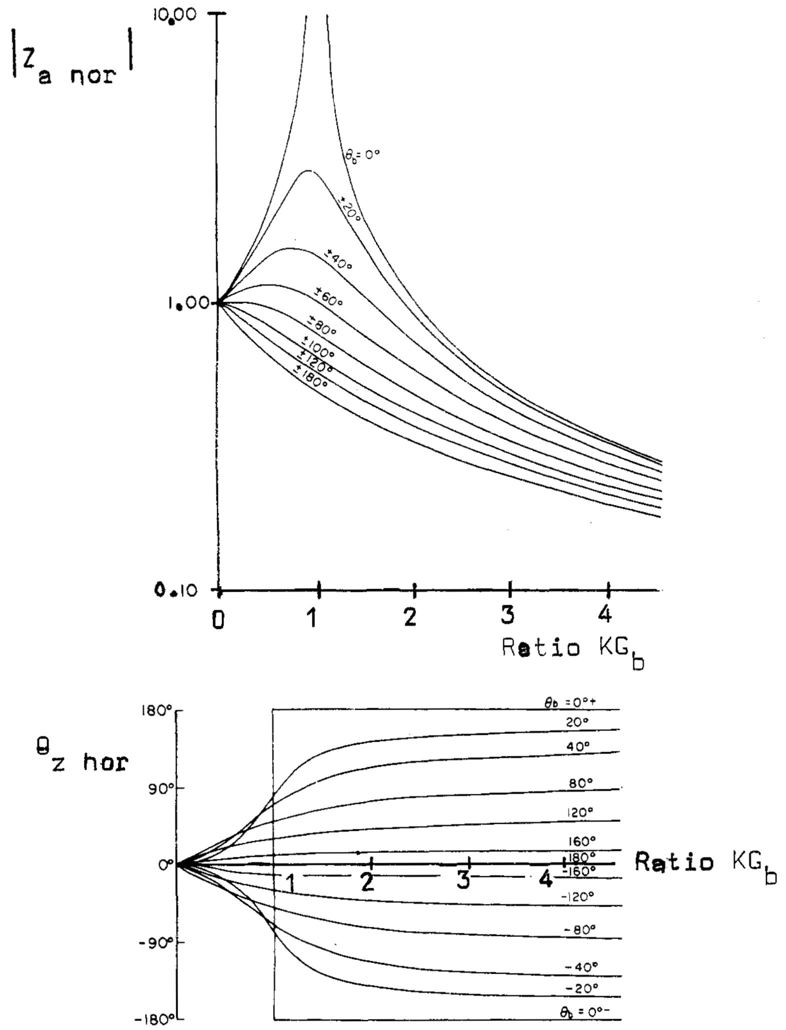



Fig. 3. Magnitude and phase of $Z_{a\,\mathrm{nor}}$ as a function of $KG_b$.

circuiting the input port and calculating $-(V_d - V_c)$ which equals $T_\infty$ under these conditions. Therefore, from Fig. 2(c)

$$T_\infty = -(V_d - V_c)\Big|_{I_a=0} = V_c\left(1 - K\frac{Z_3\|Z_{i2}}{Z_2 + Z_3\|Z_{i2}}\right)$$
$$= A\frac{Z_{i1}}{Z_{i1} + Z + Z_o}\left(1 - K\frac{Z_3\|Z_{i2}}{Z_2 + Z_3\|Z_{i2}}\right). \quad (6)$$

Substituting (4), (5), and (6) into (3) gives the general input impedance $Z_a(A)$ expression. Under limiting impedance conditions for the differential amplifier where $Z_{i1}\to\infty$, $Z_{i2}\to\infty$, and $Z_o\to 0$, we find that

$$Z_a(A) = (Z_1 + Z)\frac{1 + A\dfrac{Z_1}{Z + Z_1}}{1 + A\left(1 - K\dfrac{Z_3}{Z_2 + Z_3}\right)} \quad (7)$$

which is identical to [1, eq. (10)]. Under the limiting condition on differential amplifier gain that $A\to\infty$, (7) reduces to

$$Z_a \triangleq Z_a(\infty) = \frac{Z_1}{1 - K\dfrac{Z_3}{Z_2 + Z_3}} = \frac{Z_1}{1 - KG_b} \quad (8)$$

where $G_b = Z_3/(Z_2 + Z_3)$ is the voltage gain of the input (impedance) divider to the noninverting channel for $Z_{i2}\to\infty$. This is equivalent to [1, eq. (11)] in rearranged form. It is a particularly useful factoring since the output voltage of the differential amplifier network can be written as

$$E_o = \frac{Z_3}{Z_2 + Z_3}\left(1 + \frac{Z}{Z_1}\right)E_b - \frac{Z}{Z_1}E_a$$
$$= G_b(1 + G_a)E_b - G_aE_a \quad (9)$$

where $-G_a = -Z/Z_1$ is the gain of the inverting channel (for $Z_{i1}$, $A\to\infty$, and $Z_o\to 0$). Therefore, for $E_b = KE_a$, the overall system gain $G(s)$ is

$$G(s) = \frac{E_o}{E_a} = KG_b(1 + G_a) - G_a. \quad (10)$$

If we normalize the input impedance expression of (8) by $Z_1$, we obtain

$$Z_{a\,\mathrm{nor}} \triangleq \frac{Z_a}{Z_1} = \frac{1}{1 - KG_b} \quad (11)$$

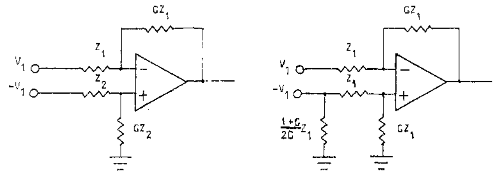
so that $Z_a = Z_1$ when $KG_b = 0$. Thus under nonzero $KG_b$ conditions, $Z_1$ must be denormalized by $1/(1 - KG_b)$. In sinusoidal steady state, this denormalization factor can be obtained directly from [1, Fig. 4(a), (b)] by simply redefining $K$ given by [1, eq. (14)] and $Z_a$ by [1, eq. (15)]. Expressing

$$KG_b = |KG_b|\,e^{j\theta_b} \quad (12)$$

and

$$Z_{a\,\mathrm{nor}} = 1/(1 - KG_b) = |Z_{a\,\mathrm{nor}}|\,e^{j\theta_{z\,\mathrm{nor}}} \quad (13)$$

in (11) and relabeling [1, Fig. 4], the normalized input impedance to channel $a$ is shown in Fig. 3. The input impedance is infinite when $KG_b = 1$.



(a) (b)

Fig. 4. Operational amplifier network for converting balanced outputs into unbalanced outputs.

The ratio $R$ of the input impedances of channels $b$ and $a$ from (2) and (8) is

$$R \triangleq \frac{Z_b}{Z_a} = \frac{Z_2+Z_3}{Z_1}(1-KG_b) = \frac{Z_2+Z_3}{Z_1}\left(1-K\frac{Z_3}{Z_2+Z_3}\right). \quad (14)$$

For the channels to be matched, $R=1$. Thus rearranging (14) gives the condition on the coupling coefficient $K$ for matching of the input impedances of the two channels as

$$K_{\text{match}} = 1+\frac{Z_2-Z_1}{Z_3}. \quad (15)$$

In the example of [1, Fig. 3]

$$K_{\text{match}} = 1+\frac{1K-1K}{10K} = 1 \quad (16)$$

so that simply connecting the inputs together leads to matched channel input impedances of 11 kΩ. The total input impedance to both channels is therefore 5.5 kΩ. Equation (14) shows that for $K=1$, the two channels are impedance matched (to $Z_2+Z_3$) only when $Z_1=Z_2$. This becomes obvious after recalling $V_c=V_d$ for infinite gain operational amplifiers and $E_a=E_b$ since $k=1$ (see Fig. 1). Thus $I_a=I_b$ only when $Z_1=Z_2$, in which case $Z_a=Z_b$.

The total input impedance $Z_{\text{in}}$ of the differential amplifier network is

$$Z_{\text{in}} = \frac{Z_aZ_b}{Z_a+Z_b} = (Z_2+Z_3)\frac{Z_1}{Z_1+Z_2+Z_3(1-K)}$$
$$= Z_1\left[1-K\frac{1-Z_1/Z_3}{1+Z_2/Z_3}\right]^{-1}. \quad (17)$$

Note that $Z_{\text{in}}$ is independent of the feedback impedance $Z$. When the inputs to each channel are connected together so $K=1$,

$$Z_{\text{in}}(K=1) = Z_1\frac{Z_2+Z_3}{Z_1+Z_2} = Z_1\frac{1+\dfrac{Z_3}{Z_2}}{1+\dfrac{Z_1}{Z_2}}. \quad (18)$$

Equations (17) and (18) form the basis for an interesting driving-point impedance synthesis method. It can be used, for instance, to provide an alternative method for realizing a bilinear $RL$ impedance to that in [4] and [5]. For example, setting $Z_1=R$, $Z_2=1/sC$, and $Z_3=aR$, the total input impedance $Z_{\text{in}}$ of the network is

$$Z_{\text{in}}(K=1) = R\frac{1+asRC}{1+sRC}. \quad (19)$$

For $a>1$, the input impedance is inductive. Drawing the Bode magnitude approximation for $Z_{\text{in}}$ shows that the equivalent inductance value is $aR^2C$ H in the frequency range $1/aRC<\omega<1/RC$. For $a<1$, the input impedance is capacitive over a limited frequency range.

Another application area of these results are operational amplifier systems that convert balanced systems into unbalanced systems. Balanced systems are symmetrical with respect to ground so $K=-1$. Since these outputs must remain balanced with respect to impressed loads, then $Z_a=Z_b$. Another constraint that channel gains be equal and opposite requires that $G_b=G_a/(1+G_a)$ from (10). Thus if the channel gains required are $G$ (noninverting channel) and $-G$ (inverting channel), respectively, the channel gain constraint requires $Z=GZ_1$ and $Z_3=GZ_2$ from (10), as shown in Fig. 4(a). The input impedances are then

$$Z_a = \frac{1+G}{1+2G}Z_1 \quad (20)$$

$$Z_b = (1+G)Z_2 \quad (21)$$

from (8) and (2), respectively. Requiring $Z_a=Z_b$ for equal loading requires

$$Z_1 = Z_2(1+2G). \quad (22)$$

Since large gain $G$ requires $Z_1\approx 2GZ_2$ and $Z\approx 2G^2Z_2$, the feedback impedance $Z$ may become excessively large. In such cases, it is more practical to add a shunt impedance $Z_s$ to the input of the noninverting channel to reduce $Z_b$ to the desired level. Equating $Z_b\|Z_s$ to $Z_a$ and rearranging results in the design equation

$$\frac{1}{Z_s} = \frac{1}{(1+G)Z_1}\left[1-\frac{Z_1}{Z_2}+2G\right]. \quad (23)$$

A convenient choice is to make $Z_1=Z_2$ which requires that $Z_s=Z_1(1+G)/2G$. The resulting network is shown in Fig. 4(b). An additional constraint that is sometimes desirable requires matching of the input impedances presented to the operational amplifier itself. This minimizes the voltage offsets due to nonzero offset currents. Assuming that the voltage sources $\pm V_1$ have output impedances $Z_o$, then the impedance presented to the inverting terminal of the operational amplifier is $(Z_o+Z_1)\|GZ_1$, while that presented to the noninverting terminal is $(Z_o+Z_2)\|GZ_2$ [see Fig. 4(a)]. Impedance matching requires $Z_1=Z_2$ which cannot be satisfied under the equal loading requirement of (22). The problem is simply overconstrained and more degrees of freedom must be introduced if a solution is to exist. This will not be pursued here.

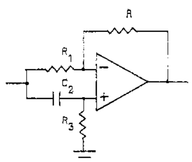
All-pass networks having the equivalent topology of Fig. 1 can also be readily analyzed using these results [6], [7]. These considerations can be directly generalized for other topologies. Consider the all-pass networks of Fig. 5. For the network of Fig. 5(a), the input impedance $Z_a$ of the inverting channel, using (8), is

$$Z_a = R_1\frac{1}{1-G_b} = R_1\frac{1}{1-\dfrac{sR_3C_2}{1+sR_3C_2}} = R_1(1+sR_3C_2). \quad (24)$$

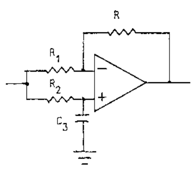
The equivalent circuit of this input appears to be a resistance of $R_1$ Ω in series with an inductance of $R_1C_2R_3$ H. We found experimentally that $Z_a=20.2$ kΩ$+jw17$ H when theoretically $Z_a=20$ kΩ $+jw15.3$ H for an all-pass network having $R_1=R=20$ kΩ, $C_2=0.09$ μF, and $R_3=8.5$ kΩ using an LM101 operational amplifier. The total input impedance $Z_{\text{in}}$ is $R_1(1+sR_3C)/(1+sR_1C)$ so that this network can be used to obtain the bilinear $RL$ impedance discussed in (19) for $R_3>R_1$.

For the network of Fig. 5(b),

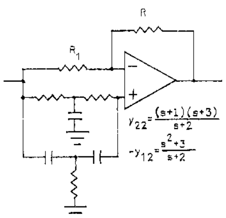
$$Z_a = R_1\frac{1}{1-\dfrac{1}{1+sR_2C_3}} = R_1\left(1+\frac{1}{sR_2C_3}\right) \quad (25)$$




(a)




(b)




(c)

Fig. 5. Recent all-pass networks [7].

so that the input appears to be a resistance of $R_1$ Ω in series with a capacitance of $C_3R_2/R_1$ F. Experimentally, $Z_a = 20.2$ kΩ$-j/w$ $0.0348 \times 10^{-6}$ F when theoretically $Z_a = 20$ kΩ$-j/w$ $0.038 \times 10^{-6}$ F, interchanging the $R$ and $C$ position of Fig. 4(a). The total input impedance $Z_{in}$ is $(1+sC_3R_2)/sC(1+R_2/R_1)$.

In passing we note that the input impedance $Z_a$ of the network of Fig. 5(c) is

$$Z_a = R_1 \frac{1}{1 + \dfrac{y_{21}}{y_{22}}} = R_1 \frac{1}{1 - \dfrac{s^2+3}{s+2} \dfrac{(s+2)}{(s+1)(s+3)}}$$

$$= R_1 \frac{(s+1)(s+3)}{4s}. \tag{26}$$

These all-pass networks provide excellent application and verification of the results developed in [1] and in this correspondence. The results provide insight into impedance matching problems. The results also provide the basis for an active $RC$ realization of a driving-point impedance.

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# Fast Neutron Tolerance of GaAs JFET's Operating in the Hot Electron Range

A. F. BEHLE AND R. ZULEEG

***Abstract*—Carrier removal and mobility degradation in epitaxially grown n-type GaAs, due to exposure to fast neutrons, is reported. The variations in carrier concentrations and mobilities are utilized to predict the transconductance degradation of GaAs JFET's as a function of neutron fluence. Experimental results up to a fluence of $8 \times 10^{15}$ n/cm² are reported and correlated with theory.**

A theoretical analysis and preliminary data for the effects of fast neutron irradiation on the electrical parameters of n-channel, GaAs JFET's operating under hot electron conditions have been reported previously by McNichols and Zuleeg [1].

The purpose of this correspondence is to report further experimental data confirming the improved neutron tolerance expected for these devices. In addition, data for neutron effects in n-type, GaAs epitaxial layers are presented.

In order to fully assess the effects of fast neutron irradiation on GaAs JFET's, pre- and post-irradiation Hall effect measurements were performed to determine the effects of neutron irradiation on the basic starting material of n-type epitaxial GaAs layers on chromium doped, semi-insulating substrates. Fig. 1 presents data for the carrier removal rate $(-dN/d\Phi)$ and the degradation parameters $a$ and $b$ as a function of initial carrier concentration for epitaxial GaAs layers greater than 1 μm thick. The degradation parameters $a$ and $b$ are defined in [1] and predict the post- to pre-irradiation carrier concentration $N$ and mobility $\mu$ as a function of neutron fluence $\Phi$ from the relations

$$N = N_0(1 - a\Phi) \tag{1}$$

$$\frac{1}{\mu} = \frac{1}{\mu_0}(1 + b\Phi). \tag{2}$$

These data correlate well with data for bulk n-type GaAs published by McNichols and Ginell [2]. The straight lines in Fig. 1 are obtained by the method of least squares, and are numerically represented by [2]

$$a = 7.2 \times 10^{-4} N^{-0.77}\ (\mathrm{cm}^2) \tag{3}$$

$$b = 7.8 \times 10^{-6} N^{-0.64}\ (\mathrm{cm}^2). \tag{4}$$

When epitaxial films thinner than 1 μm were investigated, it was not possible to extract meaningful information from pre- and post-irradiation Hall measurements due to space-charge redistribution effects of significant magnitudes occurring at the substrate–epitaxial layer interface.

The GaAs JFET's (Fig. 2) used in this study were fabricated on n-type layers 1–2 μm thick with carrier concentrations in the range of $10^{15}$–$10^{17}$ cm$^{-3}$ on chromium doped, semi-insulating substrates. The gate, with a length of 5 μm, is zinc diffused across a mesa formed by etching through the epitaxial layer. Source, drain, and gate contacts are alloyed AuGe. The maximum frequency of oscillations for the devices is about 6 GHz.

The data for the normalized transconductance degradation of the JFET's as a function of channel doping for a neutron fluence of $2 \times 10^{15}$ n/cm² is presented in Fig. 3 for all transistor lots tested under the program. Each lot was composed of a minimum of ten devices. It is evident that the average value and the standard deviation range of normalized transconductance degradation of device lots doped with $2 \times 10^{15}$, $2 \times 10^{16}$, $5 \times 10^{16}$, and $1 \times 10^{17}$ cm$^{-3}$ are predicted by the theory for $z \gg 1$, where by definition [3]

$$z = \frac{\mu V_0}{v_m L} \tag{5}$$

and where $\mu$ is the low-field drift mobility, $V_0$ is the device pinchoff voltage, $v_m$ is the carrier saturation drift velocity, and $L$ is the gate

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