# PCB Design for EMI/EMC Compliance

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WEMPEC Seminar

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# References

*Unless noted otherwise, everything is from the 1st two references*


- *PCB Design Techniques for EMC and Signal Integrity* Short Course, 27-29 June, UW–Madison, Mark Montrose, Instructor
- *Printed Circuit Board Design Techniques for EMC Compliance*, Mark Montrose, 1996 IEEE Press
- *Electronic Manufacturing*, Sheldon Kohen and Michael Rose, 1982 Reston Publishing Company
- *Linear Design Seminar*, Analog Devices, October 1987
- *Electronic Manufacturing Processes*, Thomas Landers, William Brown, Earnest Fant, Eric Malstrom and Neil Schmitt, 1994 Prentice Hall
- *Electronics Assembly Handbook*, Keith Brindly, 1990 Newnes

# Presentation Overview

- Definitions
- PC Board Materials & Construction
- EMC Fundamentals
- EMI Suppression
- Signal Integrity
- Bypassing & Decoupling
- Trace Routing
- ESD Protection

# Definitions

- *Printed Circuit Board (PCB)* Also known as a Printed Wire Board (PWB). A device used to mechanically hold components while providing electrical interconnection via a transmission line. It consists of one or more layers of an insulating material and one or more layers of a conductive foil.
- *land* The part of a PCB trace allocated for the connection to a component.
- *via* A hole in the PCB with conductive plating on the inside and which connects to one or more condutive layers.
- *Through-hole Technology (THT)* “Standard” leaded components which are mounted by inserting the leads into vias and then filling the vias and surrounding land/pad with solder.
- *Surface-mount Technology (SMT)* Leadless components which are soldered directly onto the lands located on the surface of the PCB.

- *Electromagnetic Compatibility (EMC)* The capability of electical and electronic systems, equipment, and devices to operate in their intended electromagnetic environment within a defined margin of safety, and at design levels of performance, without suffering or causing unacceptable degradation as a result of electromagnetic interference. (ANSI C64.14-1992)
- *Electromagnetic Interference (EMI)* The process where disruptive electromagnetic energy is transmitted from one electronic device to another via radiated or conducted paths.
  - *Radiated Emissions* The component of RF (roughly 10kHz to 100GHz) energy transmitted through a medium, usually free space (air), as an electromagnetic field.
  - *Conducted Emissions* The component of RF energy transmitted as a propagating wave generally through a wire or interconnect cable. LCI (Line conducted interference) refers to RF energy in the power cord.
- *Susceptibility* The measure of a device's ability to be disrupted or damaged by EMI exposure.

- *Immunity* The measure of a device's ability to withstand EMI exposure and still operating at a designated level.
  - *Electrostatic Discharge (ESD)* A transfer of electric charge between bodies of different electrostatic potential in proximity or through direct contact.
  - *Radiated Immunity* The ability to withstand electromagnetic energy which is propagated through free space.
  - *Conducted Immunity* The ablity to withstand electromagnetic energy which is enters through external cables and connections (power or signal).
- *Containment* Keeping RF energy inside of an enclosure by providing a metal shield or plastic housing with RF conductive paint. Similarily, external RF energy can be kept out.
- *Suppression* Design techniques which reduce or eliminate RF energy from entering or leaving without using a secondard method like a shield or metal chassis.

# Board Materials and Construction

- The base material or core
- Copper Layers
- 2-Layer boards
- Multilayer boards
- Types of Traces
- Transmission Line Calculations

# Core Materials

The most common material is a fiberglass resin called FR-4.

| Material | $\epsilon_r'$ | CTE ppm/$^oC$ | Loss Tangent ($\delta$) | Cost per sq. ft. |
|---|---|---|---|---|
| FR-4 glass | 4.1-4.8 | +250 | 0.02-0.03 | $2.5 |
| GTEK | 3.5-4.3 | +250 | 0.012 | $3.5 |
| woven glass/ceramic loaded | 3.38 | +40 | 0.0027 | $9.50 |
| PTFE/ceramic (Teflon) | 2.94 | 0 | 0.0012 | $100.00 |

# Copper Layers

The conductive layer of a PCB is usually a sheet of copper which has been etched to form the circuit traces. The copper sheet's nominal thickness is designated by the weight of 1 square foot of copper of the nominal thickness.

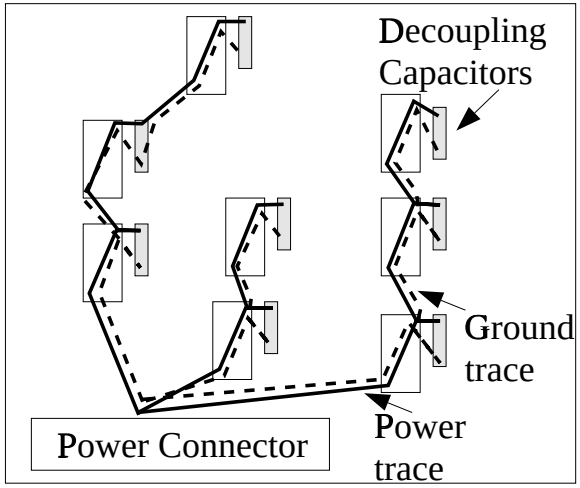
Copper Thicknesses*

| Weight (oz) | Thickness (in) | Weight (oz) | Thickness (in) |
|---|---|---|---|
| 1/8 | 0.00017 | 4 | 0.0056 |
| 1/4 | 0.00035 | 5 | 0.0070 |
| 1/2 | 0.0007 | 6 | 0.0084 |
| 1 | 0.0014 | 7 | 0.0098 |
| 2 | 0.0028 | 10 | 0.0140 |
| 3 | 0.0042 | 14 | 0.0196 |

**Electronic Manufacturing*

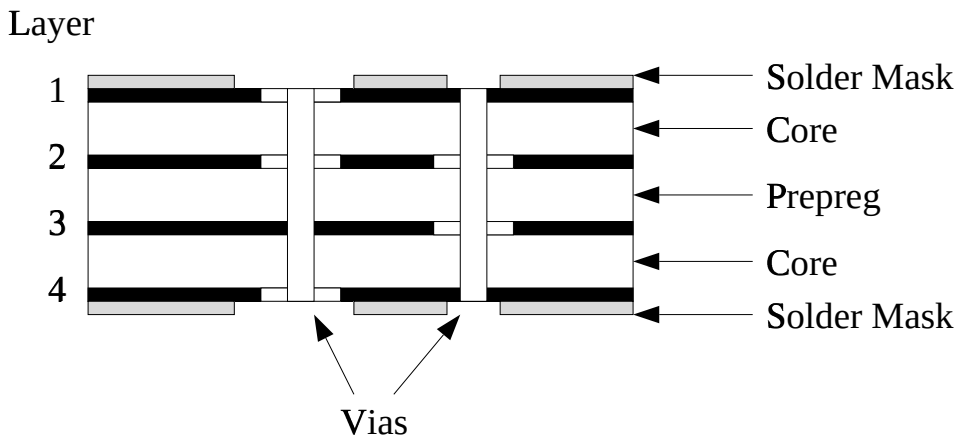
# 2-layer Boards

- Route power traces *radially* from the power supply
- Route power and ground traces parallel to each other
- Signal flow should parallel the ground paths.
- Don’t create current loops by tieing different branches together.



# Multilayer Boards

Multilayer boards are formed by etching several double-sided boards and then gluing them together with a material called *prepreg.* The thickness and material for both the core and the prepreg can be specified and controlled. *Vias* are holes which are electroplated after drilling and connect the different layers.



# Types of Traces

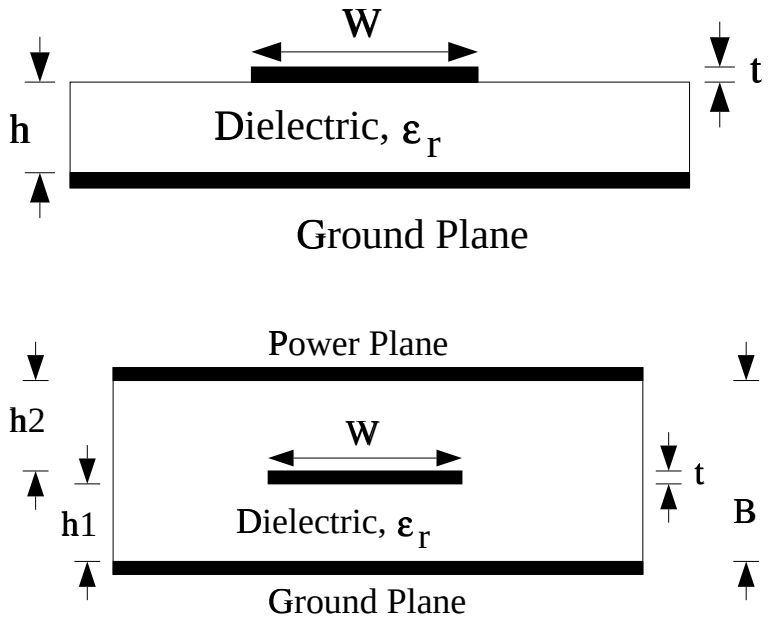
There are two basic types of trace topology: Microstrip and Stripline.

- Microstrip

  Faster signals possible due to lower capacitive coupling, but greater radiated RF

- Stripline

  Greatly reduced RF emissions, but slower signals



# Impedance & Delay Calculations

- Microstrip†

$$
\begin{aligned}
Z_0 &= \left(\frac{87}{\sqrt{\epsilon'_r + 1.414}}\right) \ln\left(\frac{5.98h}{0.8W + t}\right) \\
t_{pd} &= 85\sqrt{0.475\epsilon'_r + 0.67} \qquad \text{(ps/in)} \\
C_0 &= \frac{0.67(\epsilon'_r + 1.414)}{\ln\left(\frac{5.98h}{0.8W+t}\right)} \qquad \text{(pF/in)} \\
L_0 &= Z_0^2 C_0 = 5071.23 \ln\left(\frac{5.98H}{0.8W + t}\right) \qquad \text{(pH/in)}
\end{aligned}
$$

†see also *Lines and Electromagnetic Fields for Engineers* in the WEMPEC Library

- Stripline‡

$$
\begin{aligned}
Z_0 &= \left(\frac{60}{\sqrt{\epsilon_r'}}\right) \ln\left[\frac{4h}{0.67\pi W\left(0.8+\frac{t}{W}\right)}\right] \\
t_{pd} &= 85\sqrt{\epsilon_r'} \quad \text{(ps/in)} \\
C_0 &= \frac{1.41\epsilon_r'}{\ln\left(\frac{3.81h}{0.8W+t}\right)} \quad \text{(pF/in)} \\
L_0 &= Z_0^2 C_0 \quad \text{(pH/in)}
\end{aligned}
$$

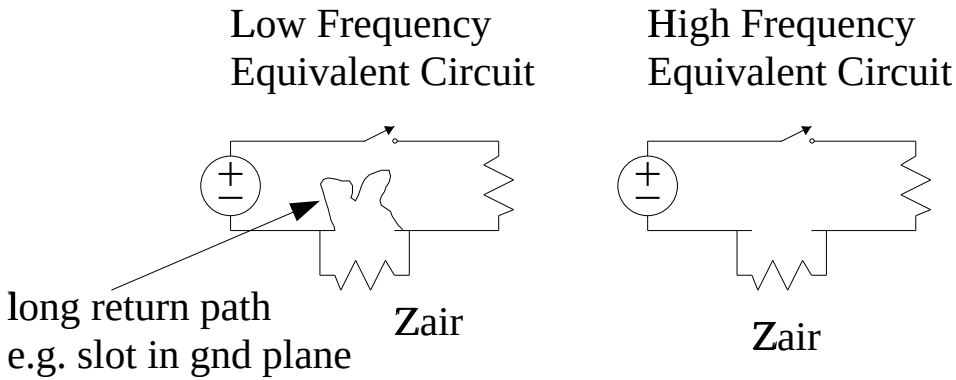
‡see also *Lines and Electromagnetic Fields for Engineers* in the WEMPEC Library

# EMC Fundamentals

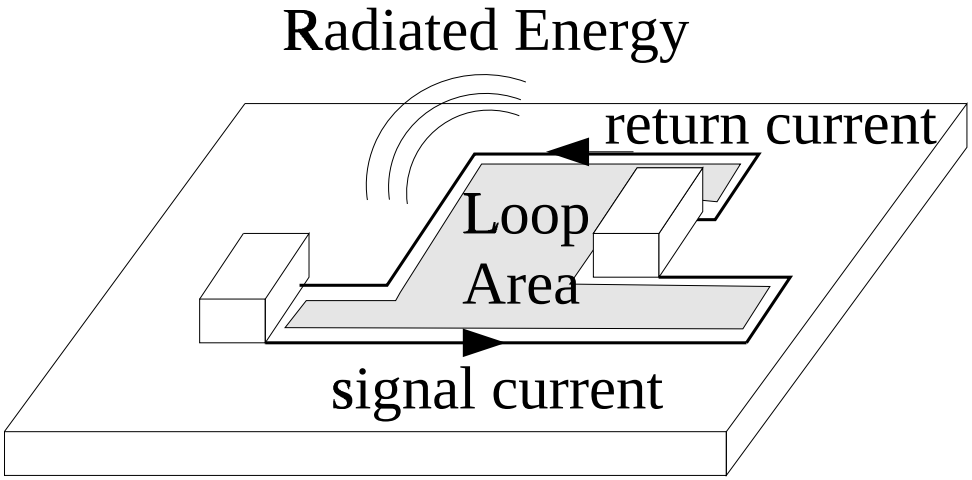
- The coupling path is frequency dependent
  - High frequencies are radiated
  - Low frequencies are conducted
  - The boundary is typically about 30 MHz
- There are 5 aspects to EMC when finding the problem
  - Frequency - Where in the spectrum is the problem observed?
  - Amplitude - How strong is the energy source?
  - Time - Is it continuous or intermittent with operation?
  - Impedance - What is the $Z$ of the source and receiver?
  - Dimensions - What are the physical dimensions of the device which will allow emissions? (RF currents will leave through openings which are fractions of a wavelength!)

# How PCB's Radiate RF Energy

- Digital signals with fast rise/fall times contain very high frequency components even for low clock frequencies! $F_{max} = \frac{1}{\pi t_r}$
- The RF currents from the switching choose the low impedance path
- The $Z_0$ of air is about 377Ω.
- Discontinuities in the RF return path $Z_{PCB}^{RF} \gg 377\Omega$
- RF current leaves the board in favor of the air = EMI



# Radiated Emissions

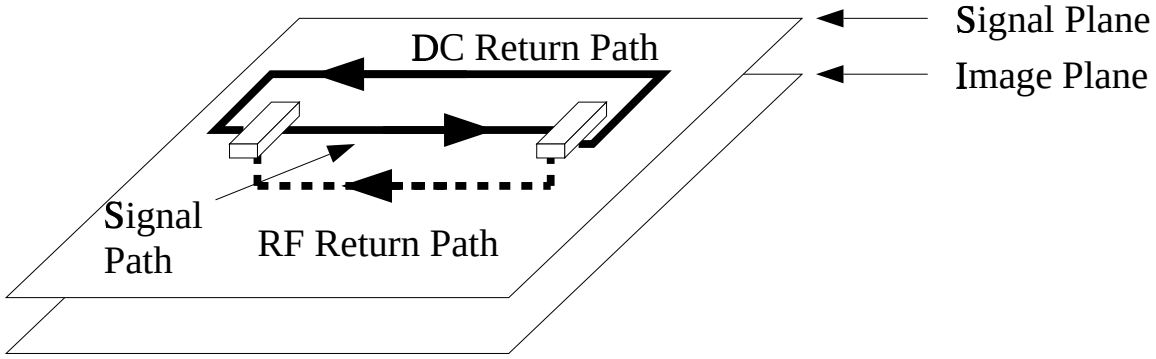


# EMI Suppresion

- Image Planes
- The 20-H Rule
- System Level Grounding
- Partitioning

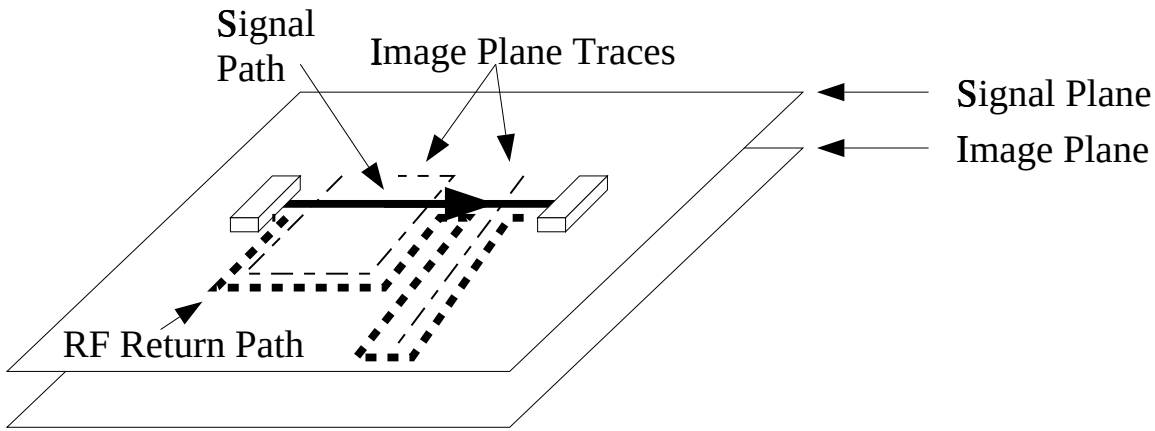
# Image Planes

An image plane is a layer of copper (either a voltage or a ground plane) which physically adjacent to the signal routing plane. The image plane provides a low impedance path for the RF currents and reduces the EMI emissions since the RF currents use the plane instead of the air.



# Image Plane Violations

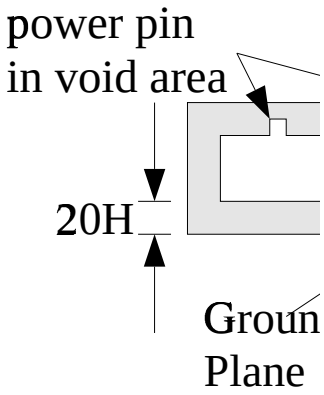
Routing traces in the image plane will create slots in the RF return path and create a large loop area and potential EMI!!



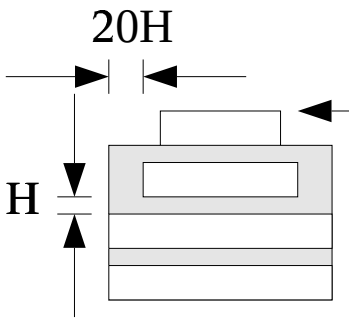
# The 20-H Rule

- RF currents fringing between the power and ground planes at the edge of the board can result in RF emissions.
- Reducing the size of the power plane with respect to the ground plane will reduce these emissions.
- This increases the intrinsic self-resonant frequency of the PCB.
- The ground plane should exceed the power plane by $20 \cdot H$ where $H$ is the total thickness between the power and ground planes
- 20-H provides for approximately a 70% reduction of the fringing flux and changing to 100-H will provide about a 98% reduction.

# The 20-H Rule in Action




Board top view




Board side view

If a power pin needs to be located near the edge of the board, then it is ok for the plane to extend into the 20-H void to surround the pin.

# System Level Grounding

There are three main system grounding methods

- Single-Point Grounding
  - Either Series or Parallel
  - Best for frequencies below 1 MHz
  - Has the largest amount of ground loop currents
- Multi-point Grounding
  - Preferred for frequencies above 1 MHz.
  - Minimizes loop currents and ground impedance of planes.
  - Lead Lengths must be kept extremely short
  - Provides for maximum EMI suppression at the PCB level

- Hybrid
  - A mixture of both Single-Point and Multi-Point Grounding in the same system.
- Ground loops cause RF energy to be radiated when high inductance returns are provided.
- Note: Do not count on mounting screws to provide low inductance connections. They are highly inductive and can act as helical antennae at high frequencies (100 MHz-1 GHz)!! (Use conductive gaskets in addition to the screws.)
- In a Multi-point ground system, the distance between the screws should not exceed $\lambda/20$ of the highest edge rate on the PCB.

# Partitioning

Partioning consists of breaking a board up into functional areas with respect to the bandwidth of the functional block. Grounding connections are made around the perimeter of each functional block using spring finger, screws, gaskets, etc, provided that the method has a sufficiently low inductance between the ground plane and the chassis ground.

# Signal Integrity

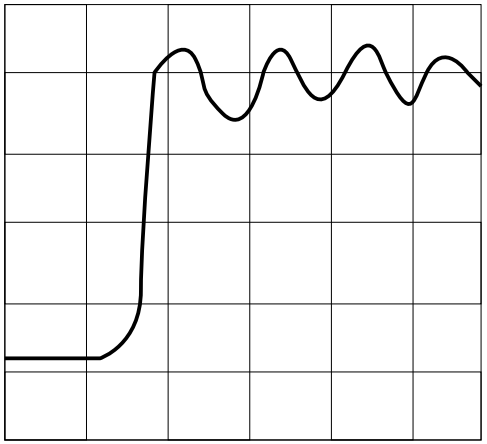
- Ringing and Reflection
- Cross-Talk
- Power and Ground Bounce

# Ringing and Reflection

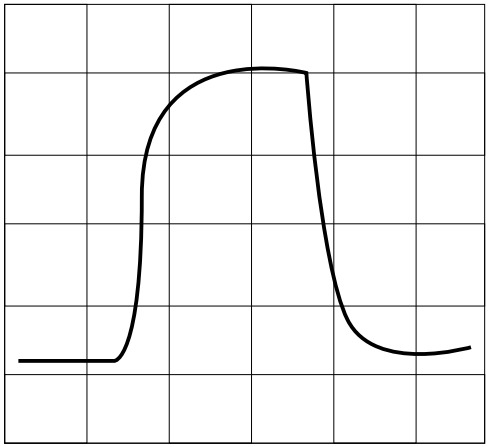
Transmission line properties which occur between the source and load. Possible causes:

- Changes in trace width
- Improperly matched termination networks
- Lack of terminations
- T-stubs, branched or bifurcated traces
- Varying loads and logic families
- Large power plane discontinuities
- Connectior transitions
- Changes in trace impedance

# Signal Distortion



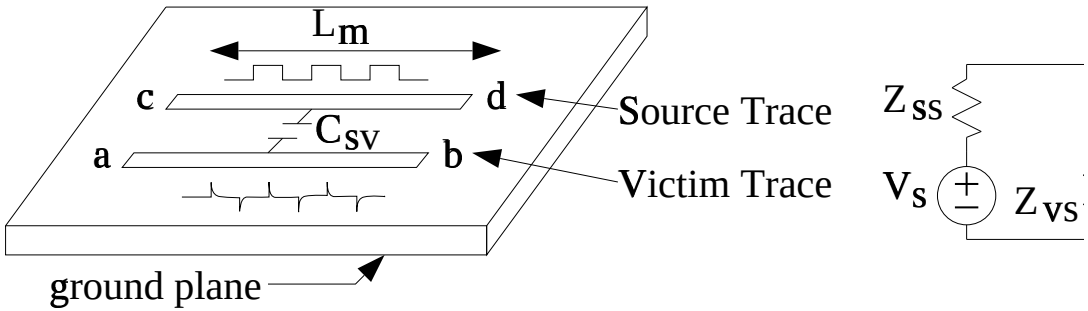
Ringing means reflections (due to excessive inductance)



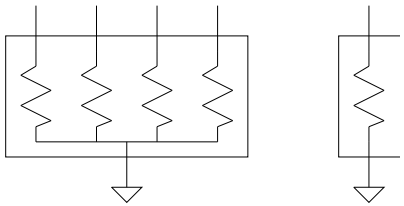
Rounding is due to excessive capacitance or trace resistance

- Ringing is minimized by proper terminations (*e.g.* series R)
- Rounding means the net is overdamped. Don’t forget about the shunt capacitance of the trace as well as the load capacitance.

# Cross-Talk (aka Board-level EMI!)




- cross-talk requires a 3-wire circuit!
- Terminating resistors with a common pin susceptible!



# Preventing Cross-Talk

First, note the following observations:

- Decreasing the trace seperation increases the mutual capacitance $C_m$ and the cross-talk.
- With parallel traces, longer parallel lengths increase the mutual inductance $L_m$ and the cross-talk.
- Decreasing the rise time of the signal, increases the cross-talk.

Some Solutions are:

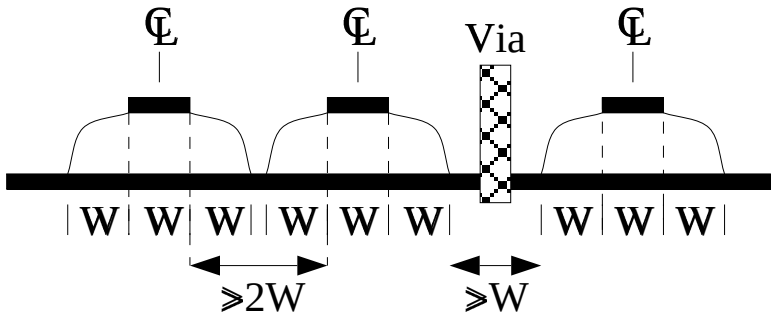
1. Group and locate logic devices according to functionality.
2. Minimize routed distance between components
3. Minimize parallel routed trace lengths

4. Locate components away from I/O interconnects and *other areas susceptible to data corruption.*
5. Provide proper terminations on impedance controlled traces or routed traces rich in harmonic energy
6. Avoid routing traces parallel to each other. Provide sufficient seperation between traces to minimize inductive coupling (The 3 W Rule) or use *guard traces.*
7. Route adjacent signal layers orthogonal to reduce capacitive coupling between the layers.
8. Reduce signal-to-ground reference distance seperation
9. Reduce trace impedance and/or signal drive level
10. Isolate signal layers which must be routed in the same axis with a solid planar structure.

# The 3-W Rule[§]

This rule for trace seperation will reduce the cross-talk flux by approximately 70%. (For a 98% reduction, change the 3 to 10.)

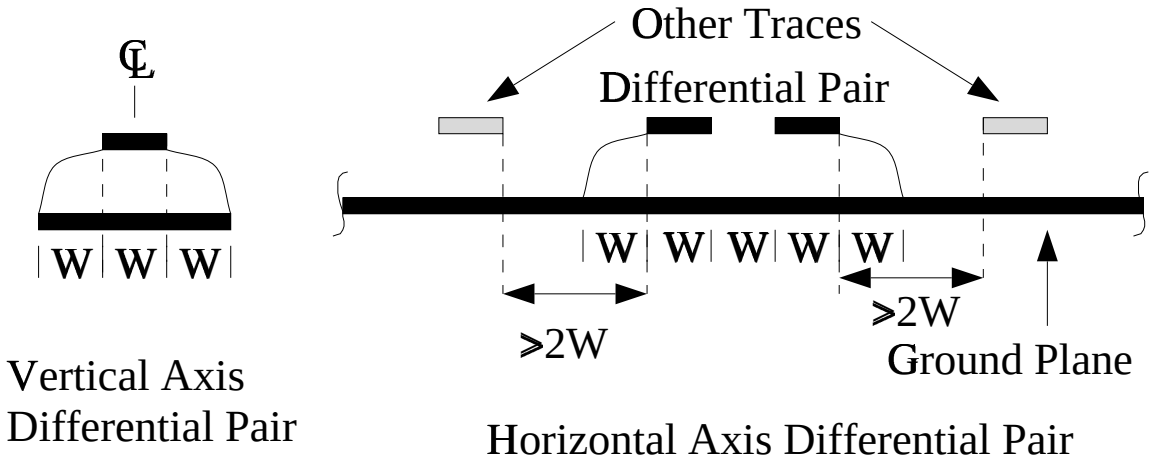
> The distance of seperation between traces must be three times the width of the traces, measured center-line to center-line.




Note that the traces near the edge of the plane need to be $>$ 1W from the edge!

[§]First described by W. Michael King

# For Differential Pair Traces




Vertical Axis
Differential Pair

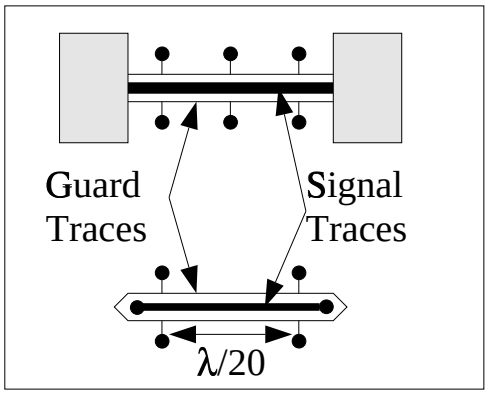
Horizontal Axis Differential Pair

# Guard/Shunt Traces

- Guard traces surround the high-threat traces (clocks, periodic signals, differential pairs, *etc.*) and are connected to the ground plane. *They are very useful in 2-layer boards.*
  - The guard trace should be *smallest, tolerable manufacturable spacing* from the signal.
  - The guard trace is connected to ground.
  - If a ground plane is available, make ground connections no farther than $\lambda/20$¶ apart.
- Shunt traces are traces located immediately above a high-threat trace and follow the trace along the entire route. They are best used in multi-layer (6 or more) boards.

¶$\lambda = \frac{1}{10 f_{max}}$

# Guard & Shunt Trace Examples




Guard Trace

Shunt Trace

# Power and Ground Bounce

- Ground bounce is caused by the simultaneous switching of drivers in an IC package and may cause functionality as well as EMI concerns. Ground bounce presents a situation where the ground reference system is not at a constant 0 V reference value.
- Be sure to provide a seperate ground connection for each ground pin directly to the ground plane. *Connecting two ground terminals together with a trace to a single via defeats the purpose of having independent ground leads on the device package!*
- Also, choose component packaging carefully: use devices with a ground reference in the center of the device to reduce the $L_{gnd}$ (4nH vs 15nH). Surface mount devices are preferred over through-hole packages for this reason.

# Bypassing and Decoupling

- Capacitor Usage and Resonance
- Parallel Capactitors
- Placement

# Types of capacitor usage

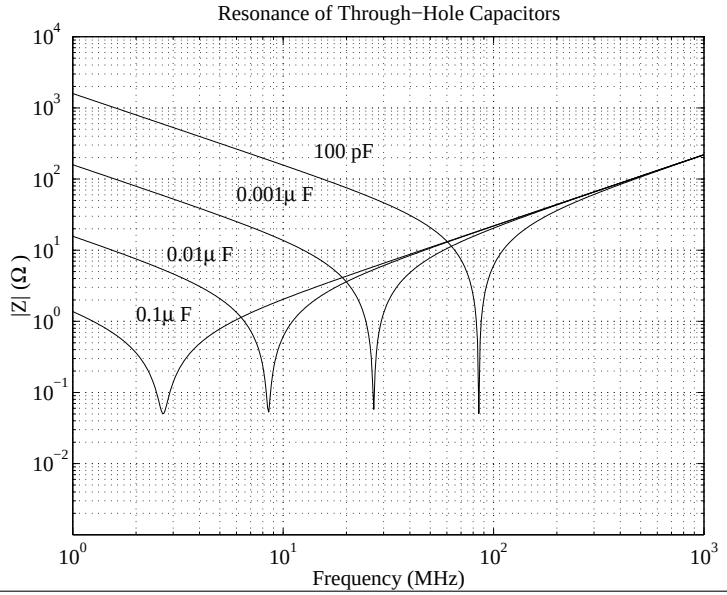
There are three primary uses for capacitors:

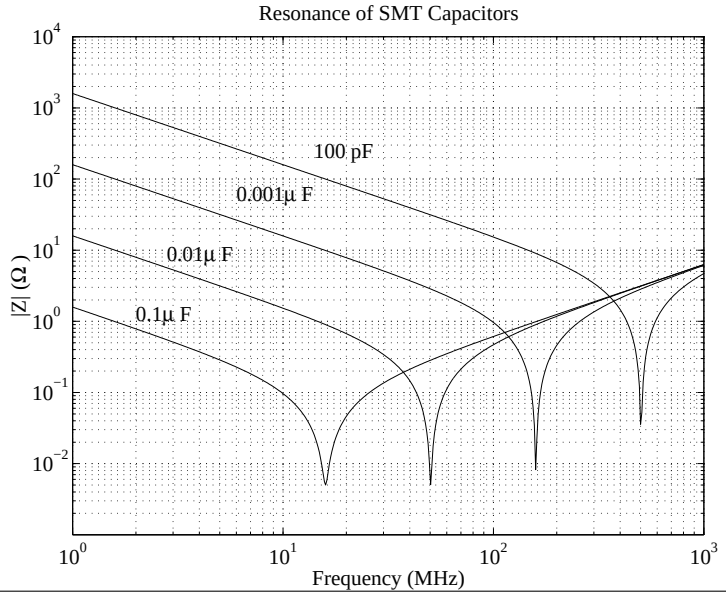
1. *Bulk* Used to maintain constant DC voltage and currents when all signal pins switch. Also prevents power drop out due to $dI/dt$ current surges from the components.
2. *Bypassing* Removes unwanted common-mode RF noise from components or cables by placing an AC-short to ground. This keeps the unwanted energy from entering a protected area as well as limiting the bandwidth. Bypassing is also used to divert RF energy from one area to another.
3. *Decoupling* Removes RF energy injected into the power planes from high frequency components consuming power at the device's switching speed. They also provide a small amount of energy to function as localized bulk capacitors.

# Resonance Effects

Remember, the capacitors really have an ESL and ESR.

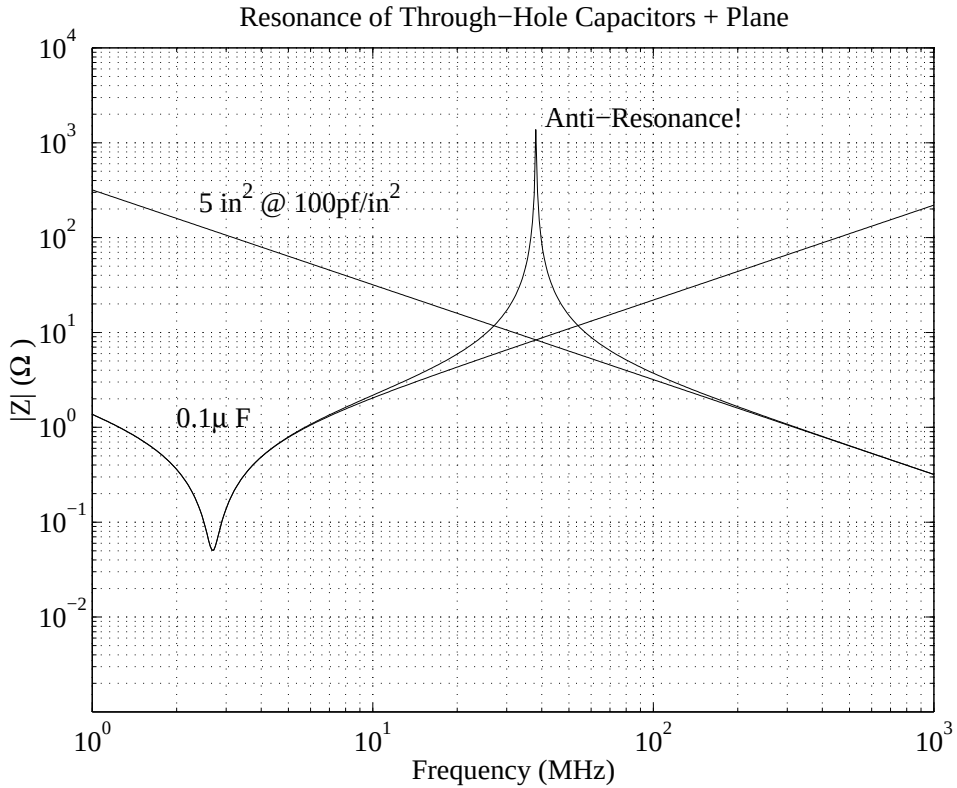
- Through-hole: ESL≈35nH and ESR≈50mΩ
- Surface Mount: ESL≈1nH and ESR≈5mΩ



# Parallel Capacitors

Remember that the power planes form a capacitor.



# Tips on Paralleling Capacitors

- Parallel capacitors of the same value will increase the net capacitance and reduce the ESL and ESR. The reduction of the ESL and ESR is the most important property. Improvements of 6dB have been observed (replacing one capacitor with multiple smaller ones).
- Be careful to remember that the values will be different and anti-resonance will occur.
- Choose values such that the anti-resonance will not occur at a harmonic of a generated signal (either a switching *or* transition frequency).
- See *Printed Circuit Board Design Techniques for EMC Compliance*, pg. 55 for capacitor value design procedure. (Giri's book)

# Capacitor Placement

Key idea is to reduce path inductance

- location location location
- the location of the components is limited by mechanical contstraints
- SMT parts can be closer than THT parts
- trace inductance will be 3-10x larger than plane inductance
- each via adds 1-3 nH of inductance

# Trace Routing

- Keep signal traces AWAY from high frequency devices, *e.g.* clocks.
- Do *NOT* use auto routers since they typically choose the *worst* possible layout for EMI/EMC concerns...
- Remember the 3-W rule
- Remember the 20-H rule
- Use isolation (moats) in conjunction with the partitioning

# Isolation/Moating

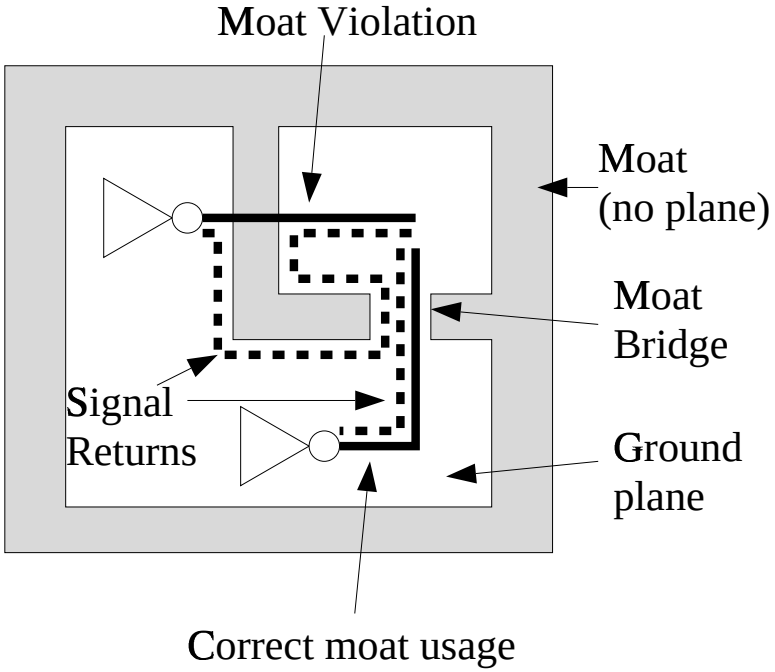
Intentionally introducing breaks in the power and/or ground planes.

**WHY???**

Consider the following:

# Moat Violations

*Moat violations will virtually always generate lots of EMI, even if the violating trace is "quiet."*



# Bridging Moats

- Make the bridge wide enough for just the required traces (observing 3W)
- Use a ferrite to provide filtering in the *power* trace, but do not put one in the ground traces.
- If a violation *must* occur, place a bypass capacitor across the moat as close to the violation as possible. (capacitor is connected ground to ground).
  - choose for proper filtering bandwith (RF return current)
  - Peak surge voltage capability for ESD protection

# ESD Protection

- Provide good shielding with the chassis and connectors
- Provide good grounding connections; wire braid with a 5:1 width:height aspect ratio is good (Solder wick works nicely!).
- Avoid pigtail wiring harnesses. (they make good RF antennae!)
- Filling un-used signal plane with a ground fill helps prevent ESD, not EMI.
- Guard Bands

# Guard Bands

- Different from guard, shunt or groung traces
- Prevents ESD damage from handling of PCB
- A *NON*-continuous trace around the edge of the PCB on both the top and bottom layers (introduce some moats to prevent ground loops!).
- Should not be covered with the soldermask and should frequently be connected to the ground reference with vias.

# A Guard Band