

DESIGN OF AN EDUCATIONAL PURPOSE MULTIFUNCTIONAL DC/DC  
CONVERTER BOARD

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CONVERTER BOARD**

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## **ABSTRACT**

### **DESIGN OF AN EDUCATIONAL PURPOSE MULTIFUNCTIONAL DC/DC CONVERTER BOARD**

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In this thesis a multifunctional DC/DC converter board will be developed for utilization as an educational experiment set in the switched-mode power conversion laboratory of power electronic courses. The board has a generic power-pole structure allowing for easy configuration of various power converter topologies and includes buck, boost, buck-boost, flyback, and forward converter topologies. All the converters can be operated in the open-loop control mode with a switching frequency range of 30-100 kHz and a maximum output power of 20 W. Also the buck converter can be operated in voltage mode control and the buck-boost converter can be operated in peak-current-mode control for the purpose of demonstrating the closed loop control performance of DC/DC converters. The designed board allows for experimentation on the DC/DC converters to observe the macroscopic (steady-state/dynamic, PWM cycle and low frequency) and microscopic (switching dynamic) behavior of the converters. In the experiments both such characteristics can be clearly observed such that students at basic learning level (involving only the macroscopic behavior), and students at advanced learning level (additionally involving the parasitic effects) can benefit from the experiments. The thesis reviews

the switch mode conversion principles, gives the board design and proceeds with the experiments illustrating the capabilities of the experimental system.

Keywords: Switch-mode power supply, SMPS, DC/DC converter, buck, boost, buck-boost, isolated converter, voltage mode, peak current mode, educational board.

## ÖZ

### EĞİTİM AMAÇLI, ÇOK İŞLEVİLİ DC/DC DÖNÜŞTÜRÜCÜ DEVRESİNİN TASARIMI

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Bu tezde, güç elektroniği derslerinin anahtarlama modlu güç dönüştürücüleri laboratuvarında kullanmak amacıyla, çok fonksiyonlu DA/DA dönüştürücü kartı geliştirilmiştir. Kartın genel, güç-kutup yapısı, üç tanesi yalıtımsız iki tanesi yalıtımlı olmak üzere beş adet DA/DA dönüştürücü temel devresinin tek kart üzerinde uygulanabilmesini mümkün kılmaktadır. Tüm dönüştürücüler açık çevrim olarak, 30-100 kHz frekans aralığında, maksimum 20 W güçte çalıştırılabilmektedir. Bunun yanında, DA/DA dönüştürücülerin kapalı çevrim performanslarını gösterebilmek amacıyla, gerilim düşüren dönüştürücünün gerilim modu denetimi, gerilim yükselten-düşüren dönüştürücünün tepe akım modu denetimi uygulanmıştır. Tasarlanan kart, DA/DA dönüştürücü karakteristiklerinin küçük ölçekli (kalıcı durum dinamiği, darbe genişliği modülasyonu döngüsü ve düşük frekans) ve büyük ölçekli (anahtarlama dinamiği) olarak gözlemlenmesine olanak sağlamaktadır. Deneylerde her iki karakteristik de açıkça gözlemlenebilir olacak ve gerek temel öğrenme seviyesindeki öğrencilerin (yalnızca küçük ölçekli davranışlar kapsanarak), gerekse ileri seviyedeki öğrencilerin (ek olarak büyük ölçekli davranışlar da kapsanarak) deneylerden faydalanması sağlanacaktır. Tezde temel anahtarlama modu

dönüştürücü prensipleri gözden geçirilmiş, kartın tasarımı sunulmuş ve deneysel sonuçlar ortaya konarak deney sisteminin kapasitesi gösterilmiştir.

Anahtar Kelimeler: Anahtarlama-modlu güç kaynağı, AMGK, DA/DA dönüştürücü, indirici, yükseltici, indirici-yükseltici, yalıtımlı dönüştürücü, gerilim modu, tepe akım modu.

*To My Mother, Müjde*  
*To My Aunt, Yurdagül*  
*And To My Uncle, Hazim*



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# TABLE OF CONTENTS

PLAGIARISM.....	iii
ABSTRACT.....	iv
ÖZ.....	vi
DEDICATION.....	viii
ACKNOWLEDGEMENTS.....	ix
TABLE OF CONTENTS.....	x
LIST OF FIGURES.....	xiii
LIST OF TABLES.....	xx
CHAPTER	
1. INTRODUCTION.....	1
1.1 An Overview of Power Electronics.....	1
1.2 Power Electronics Education.....	5
1.3 An Introduction to the Switch-Mode DC/DC Power Conversion Technology.....	7
1.4 Switch-Mode Power Conversion Education.....	11
1.5 Scope and Organization of the Thesis.....	16
2. SWITCH-MODE DC/DC CONVERTER BASICS.....	20
2.1 Introduction.....	20
2.2 DC/DC Converter Topologies and Operation.....	23
2.2.1 Non-Isolated Topologies in CCM.....	23
2.2.2 Isolated Topologies in CCM.....	29
2.2.3 DC/DC Converters in Discontinuous Conduction Mode.....	34
2.3 Modeling and Small-Signal Transfer Functions of DC/DC Converters...37	
2.3.1 State-Space Averaging.....	38

2.3.2 Circuit Averaging.....	43
2.3.3 Obtaining and Understanding Converter Transfer Functions.....	50
2.4 Control of DC/DC Converters.....	55
2.4.1 Effects of Negative Feedback on Converter Transfer Functions....	56
2.4.2 Stability.....	57
2.4.3 Compensator Design Using Direct Duty Ratio Pulse-Width Modulator.....	60
2.4.3.1 Compensator Design in Theory.....	61
2.4.3.2 Compensator Design in Practice.....	64
2.4.4 Voltage Feed-Forward Control.....	68
2.4.5 Current Mode Control.....	69
3. SWITCH-MODE HARDWARE DESIGN.....	75
3.1 Introduction.....	75
3.2 Switch Basics and Switch Selection Criteria in SMPS Applications.....	76
3.2.1 The Uncontrolled Switch: The Power Diode.....	76
3.2.2 The Controlled Switch:The Power MOSFET.....	78
3.2.3 Switching Characteristics of a Power MOSFET- Diode Pair.....	79
3.3 Passive Components of SMPS.....	86
3.3.1 Capacitor Basics.....	86
3.3.2 Magnetic Components.....	93
3.4 Snubber Circuits.....	101
3.5 PCB Design Considerations.....	105
4. POWER-POLE BOARD.....	110
4.1 Introduction.....	110
4.2 Hardware Description.....	111
4.2.1 PWM Controller and Gate Drive Circuitry.....	114
4.2.2 Error Detection and Protection Circuitry.....	116
4.2.3 Hall Effect Sensors and Measurement Circuitry.....	118
4.2.4 The Linear Power Supply for the Power-Pole Board.....	120
4.3 Applications on Power-Pole Board.....	121

4.3.1 Topological Relations.....	121
4.3.2 Buck Converter Results.....	123
4.3.3 Boost Converter Results.....	129
4.3.4 Buck-Boost Converter Results.....	133
4.3.5 Flyback Converter Results.....	138
4.3.6 Forward Converter Results.....	145
4.3.7 Voltage Mode Control Results.....	148
4.3.8 Peak Current Control Results.....	159
 5. CONCLUSIONS.....	 163
 REFERENCES.....	 166
 APPENDICES.....	 171
 A. Power Pole Board Visual Explanation.....	 171
B. Power Pole Board Schematic.....	174
C. PCB and Layout of Power Pole Board.....	175
D. Real Appearance Schematic, PCB, and PCB Layout of Linear Power Supply.....	177

## LIST OF FIGURES

### FIGURES

1.1 Generic block diagram of a power electronics system.....	2
1.2 Multidisciplinary structure of power electronics.....	4
1.3 The basic linear power supply circuit diagram.....	8
1.4 Schematic diagram of a generic switch-mode power supply.....	10
2.1 The simplest form of a switching DC/DC converter: (a) circuit diagram; (b) Output voltage waveform.....	21
2.2 General classification of popular switch-mode DC/DC converter topologies..	22
2.3 The step-down (buck) converter: (a) circuit diagram; (b) inductor voltage and current waveforms.....	26
2.4 Boost converter basic circuit diagram.....	26
2.5 The basic circuit diagram of the buck-boost converter.....	27
2.6 Two additional popular non-isolated topologies: (a) Cuk converter; (b) SEPIC converter.....	29
2.7 The Flyback converter circuit diagram.....	30
2.8 Forward converter circuit diagram.....	31
2.9 Advanced isolated converter topologies: (a) two-switch forward converter; (b) push-pull converter; (c) half-bridge converter; (d) full-bridge converter...	33
2.10 Critical conduction mode of inductor current.....	34
2.11 The buck converter inductor voltage and current waveform for DCM.....	36
2.12 Boost converter model: (a) Switch network replaced with dependent sources; (b) controlled switch voltage waveform; (c) averaged model.....	45
2.13 Linearized circuit for line input disturbances.....	46
2.14 Linearized circuit model: (a) DC components; (b) small-signal AC components.....	46
2.15 Circuit model for line input variations with terminal parameters scaled.....	47

2.16 Equivalent circuit model for line input variations-to-output.....	47
2.17 Circuit to model the effects of duty cycle variations.....	48
2.18 Small-signal linearized model for duty cycle variations .....	49
2.19 Duty cycle variation circuit model: (a) model with independent sources distinguished and terminal parameters scaled; (b) the combined model.....	49
2.20 Generic block diagram of a voltage regulator system.....	55
2.21 Representation of gain and phase margins on bode plot.....	59
2.22 Representation of gain and phase margins on polar plot: (a) positive gain and phase margins; (b) negative gain and phase margins.....	59
2.23 Gain and phase plots of a lead compensator transfer function.....	61
2.24 Gain and phase plots of a lag compensator transfer function.....	63
2.25 Gain and phase plots of a lead-lag compensator.....	63
2.26 Circuit diagram of type I compensator.....	65
2.27 Type II compensator: (a) circuit diagram; (b) bode plot.....	66
2.28 Type III compensator: (a) circuit diagram; (b) bode plot.....	67
2.29 Voltage feed-forward control waveforms.....	68
2.30 Current mode control circuitry of a buck-boost converter.....	70
2.31 Slope compensation of peak current control.....	71
2.32 Two-port equivalent circuit of basic non-isolated converters.....	73
3.1 The reverse recovery current of a diode (10V/div, 10V/div, 50 $\mu$ s/div).....	77
3.2 The inductive switching concept: (a) basic circuit diagram; (b) the switching waveforms.....	79
3.3 MOSFET drain-source voltage (top, 20V/div) and gate-source voltage (bottom, 10V/div) with $R_{gate}=0$ : (a) macroscopic view for $R_{LOAD}=10\Omega$ ; (b) macroscopic view for $R_{LOAD}=40\Omega$ ; (c) detailed view during MOSFET turn-on for $R_{LOAD}=10\Omega$ ; (d) detailed view during MOSFET turn-off for $R_{LOAD}=10\Omega$ .....	82
3.4 MOSFET drain-source voltage (top, 20V/div) and gate-source voltage (bottom, 10V/div) for $R_{LOAD}=10\Omega$ : (a) $R_{gate}=39\Omega$ ; (b) $R_{gate}=100\Omega$ .....	82
3.5 MOSFET drain-source voltage (top, 20V/div) and gate-source voltage (bottom, 10V/div) for $R_{LOAD}=10\Omega$ , $R_{gate}=100\Omega$ : (a) during MOSFET turn- on; (b) during MOSFET turn-off.....	83

3.6 Direct drive from the PWM output.....	84
3.7 High side gate drive circuit using isolated DC/DC converter.....	85
3.8 The impedance curve of an ideal capacitor.....	88
3.9 Capacitor equivalent model.....	89
3.10 Impedance curve of a real capacitor.....	90
3.11 Impedance curve of two different capacitors connected in parallel.....	92
3.12 Impedance curve of same capacitors connected in parallel.....	93
3.13 Transformer cross section: (a) one leg gapped; (b) all legs gapped.....	97
3.14 Magnetic equivalent circuit of a three gapped core.....	98
3.15 Flyback topology with RCD snubber network.....	103
3.16 PCB routing examples: (a) bad routing; (b) correct routing.....	106
3.17 Connection of power traces: (a) wrong single trace connection; (b) correct star connection.....	107
3.18 Ground and power planes on a PCB.....	108
3.19 Current loops in a boost converter.....	108
4.1 Generic block diagram of power-pole board.....	111
4.2 The real PCB appearances of forward converter magnetic board, flyback converter magnetic board and non-isolated converters' magnetic board.....	112
4.3 Power-pole board view with hardware blocks illustration.....	113
4.4 Gate drive circuitry.....	114
4.5 UC3824 based PWM controller circuit.....	116
4.6 Overvoltage detection circuit.....	117
4.7. The current measurement circuitry using LA25-NP.....	110
4.8 Buck converter model with two voltage source.....	121
4.9. The topological relation of buck and boost converters.....	122
4.10 The topological relation of buck-boost converter.....	123
4.11 The connection diagram of power pole board for buck converter.....	124
4.12 Inductor current ripple (bottom, 400mA/div ) for different duty cycles(top, 20V/div): (a) D=10%; (b) D=30%; (c) D=50%; (d) D=80%.....	125
4.13 The output voltage ripple(bottom, 200mV/div) for different duty cycles (20V/div): (a) at 30% duty cycle; (b) at 50% duty cycle.....	126

4.14 The output voltage ripple during switching transients: (a) during MOSFET turn-on; (b) during MOSFET turn-off (scale: 200mV/div).....	126
4.15 MOSFET drain-source voltage (top, 20V/div) and inductor current (bottom, 400mA/div) DCM operation of buck converter: (a) very beginning of the operation $R_{LOAD}=48\Omega$ ; (b) the load is increased to $R_{LOAD}=65\Omega$ .....	127
4.16 The inductor current ripple(bottom, 400mA/div) at 50% duty cycle(top, 20V/div) (a) at 65 kHz; (b) at 30 kHz.....	127
4.17 MOSFET drain-source voltage(top, 20V/div), inductor current(bottom, 400mA/div for (a) and (b), 1A/div for (c) and (d)) at DCM operation: (a) at 65 kHz the beginning of DCM $R_{LOAD}=40\Omega$ ; (b) at 65 kHz $R_{LOAD}=85\Omega$ ; (c) at 30 kHz the beginning of DCM $R_{LOAD}=13\Omega$ ; (d) at 30 kHz $R_{LOAD}=23\Omega$ .....	128
4.18 Duty cycle output voltage relation of buck converter.....	129
4.19 The connection diagram of power pole board for the boost converter.....	130
4.20 Boost converter inductor current ripple (bottom, 400mA/div) at different duty cycles (top, 5V/div): at 10%; (b) at 30%; (c) at 50%; (d) at 80%.....	131
4.21 Boost converter output voltage ripple (bottom, 200mV/div) for different duty cycles (top 5V/div): (a) at 20% duty cycle; (b) at 50% duty cycle.....	131
4.22 The MOSFET drain-source voltage (top, 20V/div) and the inductor current (bottom, 1A/div) for DCM at 30 kHz: (a) at 57 $\Omega$ ; (b) at 80 $\Omega$ .....	132
4.23 The oscillation of switch voltage (20V/div) and the inductor current (1A/div) in DCM.....	133
4.24 The duty cycle and output voltage relation for boost converter.....	133
4.25 The connection diagram of power pole board for the buck-boost converter .....	134
4.26 The inductor current ripple (bottom, 400mA/div ) of buck-boost converter for different duty cycles (top, 10V/div for (a), 20V/div for (b)): (a) for 40% duty cycle; (b) for 60% duty cycle.....	135
4.27 MOSFET gate-source voltage and inductor current discontinuity at low duty cycles: (a) 10% duty cycle; (b) 20% duty cycle (scales 10V/div, 200mV/div) .....	135
4.28 The buck-boost converter simulation: (a) circuit diagram; (b) inductor current ripple waveform (top) and output voltage ripple waveform(bottom) at 50%	



duty cycle.....	136
4.29 Buck-boost converter waveforms for 70% duty cycle; (a): duty cycle (top, 20V/div) and output voltage ripple (bottom, 200mV/div), (b) inductor current ripple (top, 1A/div) and output voltage ripple (bottom, 200mV/div).....	137
4.30 MOSFET drain-source voltage (top, 10V/div) and inductor current (bottom, 400mA/div) at DCM of buck-boost converter for 95Ω load resistance: (a) at 100 kHz; (b) at 65 kHz.....	137
4.31. The DC input to output voltage characterization of buck boost converter..	138
4.32 The connection diagram of power pole board for flyback converter.....	139
4.33 EE25E core dimensions.....	139
4.34 The primary (top, 20V/div) and the secondary (bottom, 20V/div) voltage waveforms of flyback converter: (a) at 30% duty cycle; (b) at 50% duty cycle.....	141
4.35 Primary (top, 20V/div) and secondary (bottom, 20V/div) voltage waveforms with output diode snubber: (a) at 30% duty cycle; (b) at 50% duty cycle...	142
4.36 Primary voltage (top, 20V/div) and the output current (bottom, 400mA/div for (a), 1A/div for (b)) of flyback converter: (a) at 30% duty cycle; (b) at 50% duty cycle.....	142
4.37 Primary voltage (top, 20V/div) and primary current (bottom, 400mA/div for (a), 1A/div for (b)) waveforms: (a) at 30% duty cycle; (b) at 60 % duty cycle .....	143
4.38 MOSFET drain-source voltage at the flyback operation (20V/div): (a) for 5μs/div; (b) for 100ns/div.....	144
4.39 DC voltage transfer characteristic of the flyback converter.....	144
4.40 The connection diagram of power pole board for forward converter.....	145
4.41 The primary voltage (top, 10V/div for (a) and 20V/div for (b)) and the secondary voltage of forward converter (bottom, 20V/div): (a) at 20 % duty cycle; (b) at 40% duty cycle.....	146
4.42 The primary voltage (top, 10V/div for (a) and 20V/div for (b)) and the secondary voltage (bottom, 20V/div) waveforms with one of the output diodes snubbed: (a) at 20% duty cycle; (b) at 40% duty cycle.....	147

4.43 Primary voltage (top, 10V/div) and inductor current (400mA/div): (a) at 20% duty cycle; (b) 40% duty cycle.....	147
4.44 DC voltage transfer characteristic of forward converter.....	148
4.45 Bode diagram of the uncompensated loop gain.....	151
4.46 Bode diagram of the Bode diagram of the quantity $T/(1+T)$ .....	151
4.47 Bode plot of the compensator.....	153
4.48 Bode plot of the compensated loop.....	154
4.49 Bode plot of the quantity $T_c/(1+T_c)$ .....	154
4.50 Type-II controller for the voltage mode control.....	155
4.51 The switched-load pulses (top, 5V/div) and output voltage (bottom, 500mV/div for (a), 200mV/div for (b)) waveforms at open-loop operation: (a) at normal mode of the scope; (b) at averaging mode of the scope.....	156
4.52 The switched-load pulses (top, 5V/div) and output voltage (bottom, 500mV/div for (a), 200mV/div for (b)) waveforms at closed-loop operation: (a) at normal mode of the scope (b) at averaging mode of the scope.....	157
4.53 Output voltage in closed-loop control with smaller time division.....	157
4.54 The switched-load pulses (top, 5V/div) and the output voltage (bottom, 2V/div for (a), 500mV/div for (b)) responses at light load: (a) open-loop response (b) closed-loop response.....	158
4.55 The output voltage with small time division.....	158
4.56 Inductor current (bottom, 1A/div) and duty cycle signal (gate-source voltage, top, 20V/div) at peak current control: (a) at minimum duty cycle; (b) at maximum stable duty cycle.....	159
4.57 The subharmonic oscillations of duty cycle (top, 20V/div) and inductor current (bottom, 1A/div) at peak current control: (a) current reference closer to the sub limit 50%; (b) excessive value of current reference.....	160
4.58 Duty cycle (top, 20V/div) and the inductor current (bottom, 2A/div) for the slope compensation step of the peak current mode control: (a) at 50% duty cycle; (b) at 64% duty cycle.....	161
4.59 The type-II controller for the voltage loop of peak current mode control...	161
4.60 Inductor current (bottom, 1A/div) and output voltage (top, 1V/div) waveforms: (a) open-loop response; (b) closed-loop response.....	162

A-1 Power-pole board.....	173
B-1 Power-pole board schematic.....	174
C-1 Top copper layer of power-pole board.....	175
C-2 Bottom copper layer of power-pole board.....	175
C-3 Power-pole board layout.....	176
C-4 Pads and vias of power-pole board.....	176
D-1 Real appearance of linear power supply.....	177
D-2 Bottom copper layer of linear power supply.....	178
D-3 Schematic diagram of linear power supply.....	179
D-4 PCB layout of linear power supply.....	180
D-5 Pads and vias of linear power supply.....	180

## LIST OF TABLES

TABLES.....	
1.1 Power electronics courses offered in some universities of Türkiye.....	15
2.1 Voltage conversion ratios of the basic non-isolated converters in DCM.....	37
2.2 The parameters of the basic non-isolated converter transfer functions according to the equations (2.51) and (2.52).....	52
2.3 The parameter changes of the basic non-isolated converter transfer functions, with ESR according to (2.53) and (2.54).....	54
3.1 Recommended core types for low power flyback converter design [46].....	95
4.1 Buck converter parameters for controller design.....	149
4.2 Compensator pole, zero, and crossover frequency values.....	150
4.3 Type-II compensator component values.....	152

# **CHAPTER 1**

## **INTRODUCTION**

### **1.1 An Overview of Power Electronics**

Power electronics is a common part of the everyday life. For example, an engineer in a factory during a manufacturing process uses a motor drive for the conveyors, a medical doctor in a hospital uses an X-ray machine which draws energy from the utility grid, a taxi driver drives a car that utilizes power electronics circuits to deliver energy from the battery, or a person needs to dry his/her hair uses a hair dryer that makes use of the power electronics solutions in modern life. As implied in the examples, power electronics is used in quite various applications in our lives. This is due to the fact that different load types require different types of power supply while there exist only two types of electrical energy source which are the utility grid and/or a battery.

In broad terms, the task of power electronics is to process and control the flow of electric energy in a form that is optimally suited for user loads [1]. The generic block diagram of a typical power electronics system is shown in Figure 1.1. The power electronics circuit accepts the input power and processes it according to the load requirements. A controller inspects the responses of the load in order to see whether the predetermined specifications are met or not. The controller, which produces the

correcting signals for the power electronic unit by inspecting the errors of the output, is also an analog or a digital electronic circuit with sensors and/or active/passive components. These are the basic required elements of a power electronic system to condition the electrical energy.

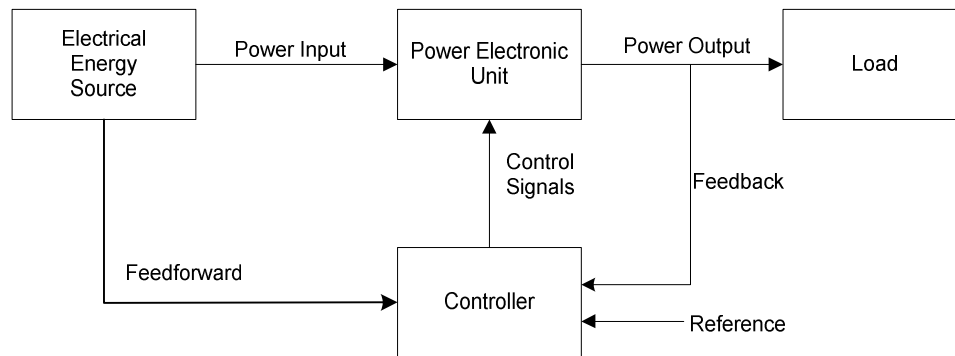


Figure 1.1 Generic block diagram of a power electronics system.

As the energy sources of the world have been decreasing over the years, efficient energy conversion has become one of the most important issues. This fact verifies the importance of the power electronics area, since it enables the efficient conversion of energy by using the year by year improving power converter topologies.

Undoubtedly, the invention of the transistor in 1948 by Bardeen, Brattain, and Shockley at the Bell Telephone Laboratory is one of the most important inventions of the history. It can also be regarded as the starting point for the improvement of power electronics as it is for the other branches of the electrical engineering. More specifically, the beginning of power electronics can be accepted as the introduction of the first commercial thyristor by the General Electric Company in 1957 [2]. Since then, various power electronic switches have been invented for different types of

applications, such as triacs, Gate Turn-Off thyristors (GTO), power Bipolar Junction Transistors (BJT), power Metal-Oxide-Semiconductor Field Effect Transistors (MOSFET), and the Insulated Gate Bipolar Transistors (IGBT). In the early times of power electronics, the thyristorized line frequency converters and their commutation problems were common. The introduction of GTO seemed to bring a practical solution but still needed high reverse current for turn-off. However, when the power BJT, MOSFET, and IGBT appeared, the era of fully-controlled, high speed switches and converters was initiated. This so called “the switch-mode power conversion technology” is today the dominant power electronic energy conversion technology. As the switch-mode power conversion technology matured, fast switches suitable for this technology have been invented in parallel to it. However, along with performance advantages such as increased energy efficiency, compactness, and controllability, faster switching has brought its own problems.

Modern switch-mode power electronics converters demand more and more speed. On the one hand, fast turning on and off devices enables reduction in component size and ensures compact solutions. On the other hand, the fast switching phenomena comes along with more problems of conducted and radiated Electromagnetic Interference (EMI). Both the components in the same circuit and the peripheral circuits connected to the same grid are affected by EMI. Failure of analog controllers, microprocessors, and all other integrated circuits (IC) may occur because of EMI. This has brought out the requirement for proper filtering and printed circuit board (PCB) design for the reduction of interference. All of the discussion up to this stage, point out one thing: The multidisciplinary nature of power electronics.

A power electronic converter aims to condition the energy and converts it from one type to another. The DC voltage/current being one form and AC voltage/current representing another form, the aim of a power converter is to convert the energy from

DC to DC (DC/DC), DC to AC (DC/AC), etc. Thus, the power converter designer needs to know the conversion type that will affect the converter topology selection process. Then, knowledge of power switches is required along with the knowledge of topological theory to design the converter using these switches and to overcome the problems they create. Therefore, a designer also needs some solid-state physics knowledge. Along with the basic topology, the circuit may need some behavioral improvements on the operation. This cure requires basic circuit theory knowledge. The output voltage/current of the system should be constant under some specific load or supply condition changes. Then the output voltage/current has to be regulated and its stability must be ensured. As a result, a designer needs some control theory knowledge. It is possible to control the power electronic system digitally by a microcontroller. Then, signal processing and microcontroller knowledge is needed. In some cases, the application may require galvanic isolation. Then, the designer will have to face the transformer design problem, which requires basic magnetics knowledge. As explained above and illustrated in Figure 1.2, power electronics overlaps with many fields of electrical, mechanical, thermal, and material engineering disciplines.

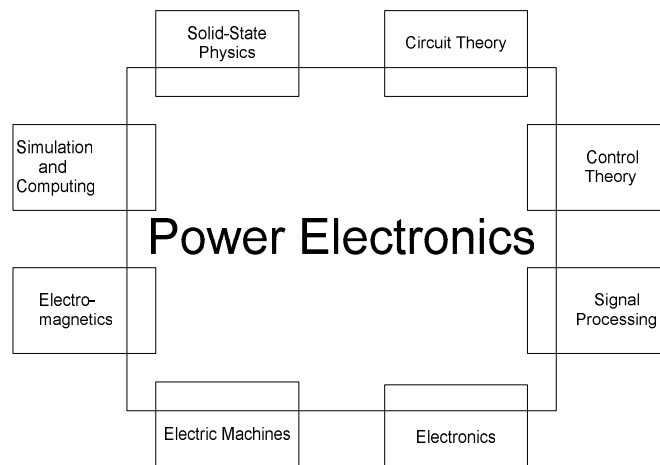


Figure 1.2 Multidisciplinary structure of power electronics.



The multidisciplinary structure of power electronics does not only involve an engineer and a designer. It also involves an educator. Since the tasks to achieve a power converter design are multidisciplinary, the task of teaching power electronics courses turns out to be difficult as well. The rapid change in the direction of power electronics technology causes the universities to lag in the education of newer technologies. For that reason, starting in the 1990's some workshops, meetings have been arranged around the world to discuss the power electronics education [3]-[7]. In these meetings, the roadmap for power electronics has been predicted; new power electronics curriculum and laboratory topics were brainstormed. People both from the academics and industry were involved with these issues, and the needs of industry were also taken into consideration.

## **1.2 Power Electronics Education**

Power electronics curriculum and the topics to be taught are the first and maybe the most important subjects of discussion regarding power electronic education. The course topics should be compatible with the needs of industry and also the content of the curriculum is an important factor in attracting the students' attention to the area. In the USA, the workshop that was organized in 1996 by the University of Central Florida proposes some clear ideas for power electronics education. The proposal on the curriculum is based on a two lecture power electronics course: One is at undergraduate and the other is at graduate level. Related and supporting courses are also specified in the workshop. According to that workshop, time spared to discussing the basics (diode circuits, magnetics, power flow, etc.) should be decreased; the part on rectifiers is the most boring part, so it should be gone through very fast, and the math should be skipped. In order to attract attention, the first power electronics course should start with the switch-mode DC/DC converters which form the basis for today's popular trend of

modern power electronics topic known as SMPS (Switch-Mode Power Supply) [5]. Another interesting idea is to switch the power electronics course to the electronics curriculum which is applied at Virginia Tech [5], [8]. The main reason behind this change is that many students identify themselves as electronics engineering students rather than power engineering students. By this way, the interest in and the subscription to power electronics lectures could be increased.

The reformation in power electronics education is not peculiar to the universities in the USA. In Europe, for example Aalborg University in Denmark is pursuing the project-based and the problem-based learning rather than the classical theory-based learning structure. Swiss Federal Institute of Technology Zurich and Fachhochschule Darmstadt in Germany have developed web-based interactive power electronics courses. In Asia, Huazhong University of Science and Technology (China) has introduced a new series of power electronics courses. Utsunomiya University in Japan and Huazhong University in China also have developed web-based power electronics courses [3]. As a corollary, the importance of the power electronics area is recognized all over the world because of decreasing energy sources; and the education programs are all being innovated to increase the number of high quality engineers in this field.

Complementary to the lecture and internet based innovations in the education area is the modernization of laboratory facilities and the experiments carried out on the laboratory hours. A comprehensive power electronics laboratory and its required experiments are explained and detailed in the addendums of [9] available on the associated website [10]. The multidisciplinary structure of power electronics dictates a practice-based learning to gain physical insight to the systems under discussion beyond the theoretical approach.

As universities and institutes are attempting to keep up with requirements of industry in terms of the modern power electronics by improving both their theoretical and practical learning environments, one thing comes into prominence when their methods and curricula are examined. The DC/DC switch-mode converter topics are starting to take more percentage of time. When the two power electronics course outlines proposed in [5] are examined it is clear that in the first course, the DC/DC converters chapter is one of the largest chapters and the second course completely covers the DC/DC converter advanced topics such as the small-signal modeling, controller design, soft-switching and power factor correction (PFC) issues. Also in [11], nine chapters out of fifteen are directly related with the switch-mode technology. This is based on the growing industry of switch-mode power converter technology and hence on meeting the growing needs in this field.

### **1.3 An Introduction to the Switch-Mode DC/DC Power Conversion Technology**

Switch-mode DC/DC converters are high-frequency switching power circuits, in which the semiconductor devices switch at a rate that is quite fast compared to the variation of the input and output waveforms [12]. Switch-mode DC/DC converters are used almost everywhere. Motor drive applications and modern power supply (SMPS) applications are the two most popular areas of usage for these converters. Especially the growing demand on computers and the size reduction which can be observed in LCD TVs has caused the switch-mode power supplies to be very popular in usage and hence an interesting topic of research. The question is “why do we prefer switch-mode supplies rather than any other solutions?” There can be an easy way to adjust a DC voltage by using a simple voltage divider which is implemented by two resistors. The only advantage of this method is its simplicity. But a voltage divider is an inefficient device

for DC/DC conversion. It also cannot provide a higher voltage level on the output than its input voltage level. It can be useful for voltage sensing where little current is drawn from the output, but it cannot be useful for power conversion due to its very low energy efficiency [9].

Another rival for the switch-mode power converter technology is the linear power supply technology. The linear power supply schematic is shown in Figure 1.3. A linear power supply uses the linear region of a switch (BJT) to adjust the output voltage level. By adjusting the base current of the switch via the controller command, the output voltage can be regulated to the desired value, which has to be less than the input voltage in any normal operational case of the circuit. No boosting is available. The only series element on the way from input to output is the switch as seen in Figure 1.3.

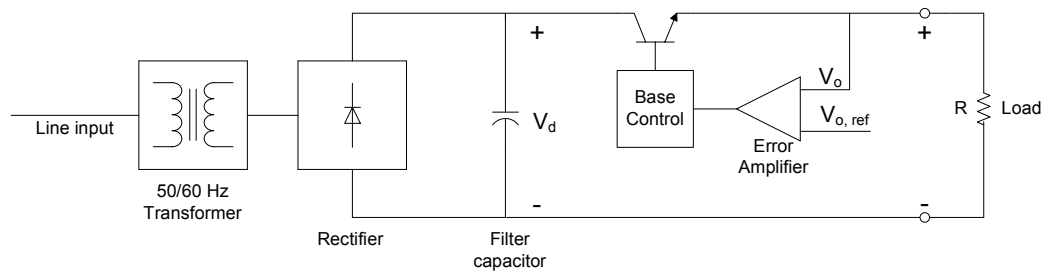


Figure 1.3 The basic linear power supply circuit diagram.

The difference between input and output voltages of the linear regulator is dissipated on the switch by multiplying the current through it. The dissipation comes out as heat. That means, the more the difference between two voltage levels occurs, the less the converter efficiency will be. Generally, the efficiency of linear converters can not be higher than 60%. This is the first but unfortunately not the last drawback of the linear technology. The power dissipation causes heatsink problem which may occupy

significant space on the PCB. However, the most important factor that determines the size of a linear power supply is the 50/60Hz line frequency transformer. These transformers can be very large and heavy because of the large amount of flux circulating through their core. Linear supplies surely have some advantages. The first advantage is the structural simplicity. When a linear regulator chip is used, designing a power supply is a quite simple process which may require only one or two filter elements. Since a linear supply does not involve any switching phenomena, it operates at the line frequency. The highest frequency a linear supply may be submitted to is a second, third, or maybe sixth harmonic component caused by a single phase or a three phase rectifier. That means it has no noise and EMI problem. It can be claimed that this is the best feature of a linear supply.

On the other hand, there exists the high frequency switch-mode power converter technology making high efficiency power conversion possible in a range from watts up to megawatts [13]. The switch-mode technology based different topologies of DC/DC converters allow all kinds of voltage/current conversion. One can obtain a lower voltage at the output by a step-down (buck) converter topology; or a higher voltage level with a step-up (boost) converter topology. Both higher and lower voltage levels in the same converter can be obtained by utilizing a step-up-down (buck-boost) converter. These are the basic non-isolated topologies and all the other topologies can be derived by modifying these converter topologies.

Electrical isolation does not bring a serious size problem in switch-mode power supplies compared to the linear supplies. The transformer can be placed at the high-frequency switching stage of the converter instead of the low frequency AC rectification stage. High switching frequency means small switching period, which creates small volt-seconds hence small amount of flux according to Faraday's Law. A small core volume will be enough to obtain a specific flux density when the amount of

flux in the core is small. Roughly that's the main idea behind the basic isolated topologies; flyback and forward converters.

The generic high frequency DC/DC power supply circuit is illustrated as blocks in Figure 1.4. The high frequency transformer on the power stage can be removed to

model a non-isolated system. Up to now, the advantages of the switch-mode have been discussed. However, whether the topology is isolated or not, there are some new problems introduced because of the fast switching phenomena in switch-mode converters. As seen in Figure 1.4, there is an input EMI filter to prevent the conducted EMI and coupling with the other circuits in the periphery. The parasitic elements introduced by the Printed Circuit Board (PCB) that are normally ignored in low frequency applications start to appear when the switching frequency is raised over a few tens of kilohertz level. The fast turn-on and turn-off times of the switches and the trapped energy in the transformer cores during the switching periods cause several problems that require a cure, such as snubbers. In that respect, the interdisciplinary structure of power electronics in switch-mode design must be taken into consideration as well. The education of switch-mode has a tendency to become confusing and complicated when not supported with the auxiliary topics well. Hence, the education on SMPS technology is one of the most important topics for the power electronics lecturers in power engineering departments. Some practical difficulties hide behind the theoretical simplicity of switch-mode design. Therefore, the educators emphasize the importance of practice-oriented education for SMPS and especially the commonality of the SMPS topologies. In the USA, this tendency on topological relation based SMPS education becomes dominant in recent years [14], [15].

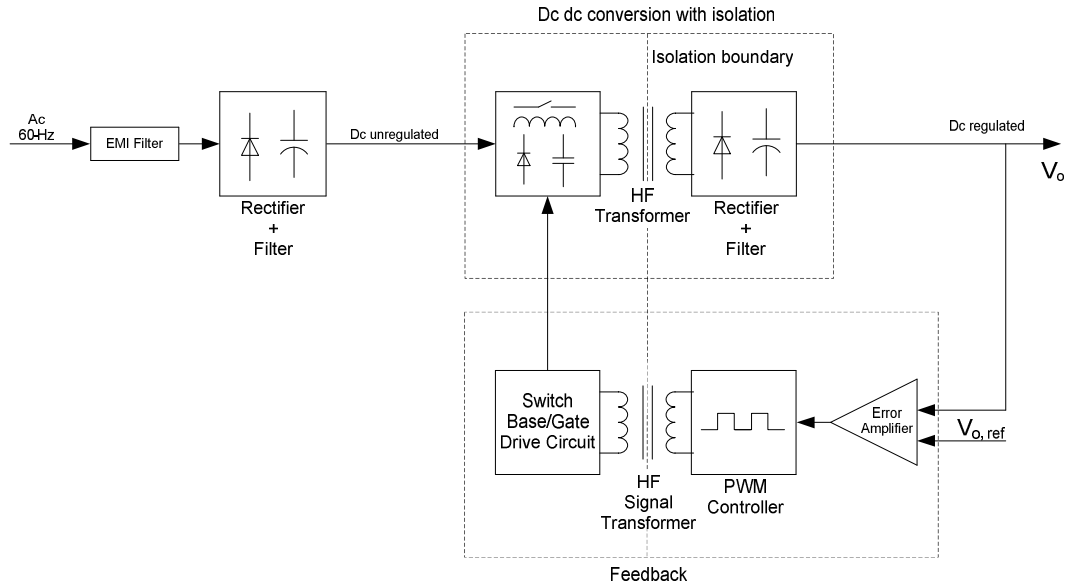


Figure 1.4 Schematic diagram of a generic switch-mode power supply.

## 1.4 Switch-Mode Power Conversion Education

The theoretical basis of operation of switch-mode converter topologies, which will be further explained in the next chapter, offers no complexity when compared to the typical rectifier circuits. Since the number of components in a circuit is not large and their behavior is assumed to be the ideal in theory, the voltage transfer equations can easily be derived and the buck and boost functions can be easily explained. However, in practice it may not be easy as connecting four diodes to the AC utility and observing the fully rectified waveform. Therefore, teaching the high frequency principles should be certainly based on a practical aspect to increase the comprehension of the students [16]. This may require project-based teaching approach or may involve experimental work with at least some laboratory sessions supported with a basic design project at the end of the sessions.

For establishing depth in understanding switch-mode power conversion, using ready-made commercial power electronics training sets may be a solution as well. Some of such products offer computer-based experimentation as in [17]; the measurements are observed from a software-based scope on the PC. The main drawback of the system in [17] is the closed-architecture structure. The converters are designed using LM2578 IC which is not penetrable. Since the discrete elements are inside the IC, it is not possible to observe any diode current or switch voltage. Only outputs can be viewed via the software-based scope. There are some other commercial products as in [18] and in [19]. In order to develop a complete power electronics set, all of these companies manufacture and offer modular-designed laboratory equipments in closed or semi-open architectures, which require long cablings for connections and hence increase the parasitic components in high frequency. This feature limits the highest possible frequency of operation. These modular designs do not support learning the concept of topological relation as well, since each topology is manufactured as different boards. These educational sets can be successful and satisfactory if they are used in right places. The main usage for these products can be in technical high schools and maybe in undergraduate education at very basic level (for example, only steady-state performance investigation), but not in an education of a senior student in a power electronics curriculum where the emphasis on second order effects (parasitics) is placed. As a corollary it can be claimed that these simple educational sets do not offer a solution for a deeper education about the SMPS topologies.

The universities in Europe or in the USA have established their own methods by developing their own solutions about the laboratory equipments to teach the switch-mode power converters because of some specific reasons. Commercially available switch-mode power supplies use voltages that are too high for the safety of the students in an experiment. Due to the construction techniques used in many commercial power supplies, it is very difficult to observe currents flowing in components of interest [20].



The converters in [20] which is designed to use in the University of Glasgow have power ratings about 10-20W to comply with safety rules. Another example is the buck and boost converter experiments carried out in the University of Reading UK. The experiments are explained and illustrated in [16]. Both converters are realized by using the commercial SG3524 PWM controller chip and completely carrying an open-architectural design. Another design with the SG3524 is used in University of Arkansas in USA. First, the buck converter is operated in the open-loop mode and the gate signals are obtained by a function generator [21]. In the second experiment of buck converter, the system is designed by using SG3524 IC and the close-loop operation is examined. When the operating frequency of the converters is observed, it is seen that the buck converter in [21] operates at 1 kHz and buck converter in [20] operates at about 3-5 kHz which are quite low for today's SMPS frequencies. The system in [16] can reach higher frequencies for the buck converter experiment as up to 75 kHz. However, the boost converter can be implemented in the range of 25 kHz. All these circuits have one common point. To build a converter which is penetrable for the student study, unfortunately the weakness they own is the same: The lack of topological relations. A student surely will have the chance to see the real converter waveforms by carrying out some experiments on these buck and boost converters on individual converter boards. However, this solution does not give a chance to a student to see how the converter topologies are related to each other.

In Türkiye, some universities which have power electronics course in their undergraduate curriculum are shown in Table 1.1. All of the courses are taken from the websites of the departments in June 2008. Some departments also offer power electronics courses under “drive” names. These courses are not included in the table, and only courses named as “power electronics” or “industrial electronics” are included. In the websites, there is no additional information whether the elective courses are being offered regularly or not. They are described only as elective (E). Core elective

(CE) courses of Middle East Technical University are offered regularly in every fall and spring terms, respectively.

The theoretical concept of the switch-mode power conversion is lectured adequately in the universities in Türkiye as tabulated in Table 1.1. Some experiments are carried out in the laboratory facilities about the switch-mode topics covered in the courses as well. Some courses offer design studies to the students to increase the practical hours spared on the switch-mode power conversion study. However, the circuits used in the laboratories are discrete circuits (unique to each converter type). The lecturers generally develop one circuit for each topology, which can be enough to discover the basics of converters but discards the topological connections/relations among converters. The topological aspect is one of the most important subjects that must be gained in a switch-mode power conversion learning process. The buck converter topology is the most important topology in the switch-mode power conversion world. Most of the converters can be derived using the buck converter. Topological point of view is the required philosophy to see these relations between the converters. A buck converter can be viewed as a boost converter when its input and output terminals are replaced. When the buck and boost converters cascaded, buck-boost topology can be derived. All the buck-boost derived converters have topological connections and can be obtained by different cascade connections. This point of view may bring a different perspective to the designer while making a converter design even while developing a controller strategy. Therefore, a reconfigurable but single hardware can be a useful tool to teach the topological aspect of the switch-mode conversion. A circuit that can make possible the transformation of the buck converter into a boost converter only by changing a few connections will provide a better vision about topological relation rather than the single circuit for each topology approach. These issues must be considered when establishing a switch-mode power conversion teaching laboratory.

Table 1.1 Power electronics courses offered in some universities of Türkiye

M: Must Course , E: Elective Course, CE: Core Elective Course

University and Program		Power Electronics Courses Offered	Type of Course	Theory Hours	Lab. Hours
Gazi University	Electrical Branch	Power Electronics I	M	3	2
		Power Electronics II	M	3	2
	Electronics Branch	Industrial Electronics	M	3	2
Hacettepe University	Electrical Branch	Power Electronics	E	3	0
		Power Electronics Lab	E	3	0
	Electronics Branch	Power Electronics	E	0	2
		Power Electronics Lab	E	0	2
Istanbul Technical University	Electronics and Telecommunication Engineering	Industrial Electronics	E	3	0
	Electrical Engineering	Power Elec. Circuits	M	3	0
		Power Elec. Lab.	M	0	2
		Ind. App. of P.E I	E	3	0
		Ind. App. of P.E II	E	3	0
	Control Engineering	Power Elec. Circuits	M	3	0
		Power Elec. Lab.	M	0	2
		Ind. App. of P.E I	E	3	0
		Ind. App. of P.E II	E	3	0
Middle East Technical University	Energy Area	Static Power Conversion I	E	3	2
		Static Power Conversion II	E	3	0
Yıldız Technical University	Common	Power Electronics	M	3	0
		Ind. App. of P.E I	M	3	2
	Electric Machinery and Power Electronics Branch	Design of P. E. Circuits	E	3	0
		Analysis of P.E. Circuits	E	3	0
		Ind. App. of P.E II	E	3	0
		Control of P. E Circuits via Microcontrollers	E	3	0
		Power Elec. Lab.	E	0	2
		Control and Protection Circuits in P.E.	E	3	0

In addition to the topological relations, in an educational switch mode power converter board, the influence of the parasitic components of the circuit must be brought out to the front stage such that the student can see the relation between each important parasitic component and the affected measured signal. For example, the parasitic inductances and capacitances under fast switching result in significant high frequency noise and stresses in the converter. Decoupling capacitors, snubbers and involved EMI filters are effective elements to suppress such noise and stresses on the converter. Introduction of such elements in the circuits and showing the behavior with and without these elements is important and should be included in an educational board.

In addition to the two issues discussed in the former two paragraphs, the basic attributes of the converters should be easily and accurately measurable such that the converter basic behavior is well observed and its characteristics are efficiently extracted via experiments. This thesis involves the design and implementation of such an SMPS educational kit. The following section discusses the content and contribution of the thesis.

### **1.5 Scope and Organization of the Thesis**

While designing a converter, there are many issues that must be considered together such as passive component selection, power semiconductor switch selection, PCB design, magnetic design, and controller design. Significant amount of technical literature is available as commercial books on power electronics or SMPS design, in the form of papers and journals on the IEEE website, and as product datasheets and application notes in the website of many chip or component manufacturers. In the power electronics literature, typically, each document covers a specific subject and as a result the remaining subjects become weak or totally missing because of the irrelevance to the topic under discussion.

The main purpose of the thesis is to develop a reconfigurable hardware for a switch-mode education laboratory and to fill the training system gap at METU and more broadly in Türkiye by sharing all the sources of the implementation. This equipment will be supported with the educational approach about the DC/DC converter design. Hence another important purpose of this thesis is to gather all the topics stated in this section under a single source not only in a theoretical basis but also including the experiences gained during design and implementation process. The topics that are covered will be explained in a manner that the noncritical materials will be discarded such that the students confusion will be avoided. However, while maintaining this, keeping the main ideas strict and avoiding superficiality about the topics are other main concerns.

All the topics explained in the thesis are based on the implementation of the educational-purpose multifunctional DC/DC converter board which is originally designed by Ned Mohan [22]. The purpose of that design is to set up a switch-mode laboratory to use in University of Minnesota. Although this power-pole board is available as a commercial product, the source about the circuit schematic is open and it can be adopted and implemented by anyone for any other uses. The board has been used as laboratory equipment in different universities as well [15], [23].

The power-pole board consists of a main board with some plug-in daughter boards for control purposes and magnetics boards for implementation of different types of converters. The power-pole board should not be considered as a commercial power supply board. It is not a power supply but a DC/DC converter stage of an SMPS instead. It does not include EMI filters at the input or output. For the practical use of students, the board is designed to be quite large which is again violating the general commercial power supply design rule because of its EMI and efficiency issues.

The most important feature of the board is enabling the comprehension of topological relations by allowing the implementation of five different topologies. Three basic non-isolated topologies and two basic isolated topologies can be implemented on the board via reconfigurable hardware design. These converters are buck, boost, buck-boost, flyback, and forward converters. Therefore, in some sections of the thesis, an undergraduate power electronics student attempting to learn the operation of these basic DC/DC converters is targeted. However, some other sections of the thesis are more suitable for a higher-level student (perhaps, a graduate student who has just started research about DC/DC converter design). Consequently, the contents of the thesis are shaped around the main idea of two different-level students. These attributes of the designed board and established experiments differ from the design of Ned Mohan as the original design mainly focuses on the prime characteristics targeted for teaching the basic behavior.

The main contribution of the thesis to the experimental setup is the ability of inspection of the first and second-order parasitic effects which can be faced as a problem in any switch-mode design experience. The output voltage ripples caused by the capacitor ESR, the stray inductance and the capacitances introduced by the PCB, the device capacitances can be examined and studied through the experiments.

In the next chapter, the theory of the basic topologies of DC/DC converters is explained. The volt-second balance principle, conduction modes, and the general equations around a DC operating point are presented. Modeling and control principles are also covered in this chapter. Hence the first section of this chapter is for a senior student maybe but the modeling and the control sections are more suitable for a graduate student.

In Chapter 3 the hardware design is examined. The basic characteristics and properties of inductors, capacitors, and switches, and the approaches to the design and selection of these components are explained. The elements cause deviation from the ideal component behaviors called as parasitics, are inspected. Since the design of the magnetic parts is another concern of this thesis, the basic design of flyback and forward converter transformers will take place in this chapter. One of the most important components of the switch mode power converter hardware is the PCB. The basic PCB design rules for power electronics circuits are also discussed in this chapter along with the effects of parasitics introduced by the PCB.

Chapter 4 is allocated for the power-pole board and includes the explanations of board design and the experimental results. The implementations on the power-pole board are presented in this chapter as well. The resulting waveforms of the given topologies and control methods are revealed throughout the chapter.

Chapter 5 is the conclusion chapter. A general overview about the thesis and some further work that can be carried out are included in that chapter.

## **CHAPTER 2**

### **SWITCH-MODE DC/DC CONVERTER BASICS**

#### **2.1 Introduction**

Switch-mode DC/DC converters are the fundamental elements of the SMPSs where the DC voltage/current is processed from one level to another level. The converters can be cascaded and one stage can even supply the other stage's voltage requirements in some power supply applications. Various types of DC/DC converter topologies are available for different types of applications.

The simplest form of a switch-mode DC/DC converter is illustrated in Figure 2.1. In the figure, the switch alternates between on and off states continuously and chops the input DC voltage as shown in the waveform of the referred figure. The duty cycle, which is the ratio of switch conduction time to whole switching period, determines the average output voltage. But the square wave output voltage contains high frequency harmonics. Since in the given case the load is resistive the same harmonic content exists in the input current as well. The converter draws square wave currents and the sharp rising, falling edges cause radiated and conducted EMI problems. Another problem of this basic switching topology is that it can only step down the voltage level. Voltage boosting is not possible. That means the topology needs some modifications, such as inclusion of some filter elements and additional switches. By adding an inductor in series, the high frequency components of the current can be filtered out; a capacitor connected in parallel with the load can



supply a low impedance path to the remaining high frequency components of the current and maintain a smooth output voltage. The topologies can be changed by applying different modifications to this primitive converter topology.

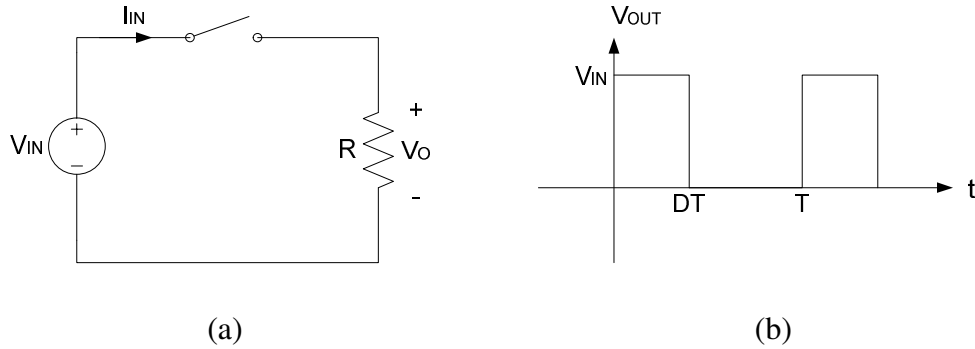


Figure 2.1 The simplest form of a switch-mode DC/DC converter: (a) circuit diagram; (b) output voltage waveform.

The general classification of switch-mode DC/DC converters is based on the presence of the galvanic isolation [1]. Using that idea, the most popular topologies of two general classes of DC/DC converters are listed in Figure 2.2. The step-up (boost) and step-down (buck) converters are the two basic topologies and all other topologies can be derived from these two converters [24]. In fact, the step-up converter can be viewed as a down converter, depending on the point of view in terms of input and output terminals. In this chapter the basic topologies of DC/DC converters will be examined.

The referred “basic topologies” term includes buck, boost, buck-boost converters and two basic isolated converters known as flyback and forward converters. The DC voltage transfer characteristics of these converters will be derived using volt-seconds balance rule which will be introduced through the section as well. All these characteristics will be derived in the continuous conduction mode (CCM) of the converters. A further step is the discussion of the discontinuous conduction mode

(DCM) of operation of these basic topologies. Explaining the DCM behavior of the converters completes the DC (steady-state) analysis of the topologies.

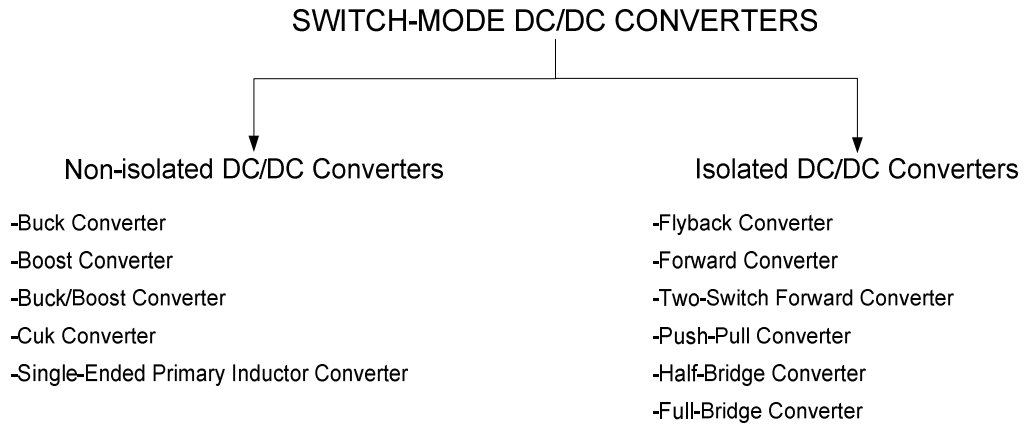


Figure 2.2 General classification of popular switch-mode DC/DC converter topologies.

Along with the DC analysis, the AC analysis of the converters should also be examined for the control purposes. Therefore, the second part of the thesis is allocated for the modeling of the converters to obtain the small-signal transfer functions. The modeling process will provide the physical interpretation of the AC variations caused by the different phenomena in the converter. Two basic modeling approaches, known as state-space averaging and circuit averaging in the literature, will be introduced to obtain the linear converter models. These models will lead the way to the converter transfer functions to design a controller.

The last section is the application of control theory to the DC/DC converters. The effects of negative feedback, stability considerations, and compensator design issues are covered in that part. Voltage feedback and voltage feedforward control methods are also explained in this section. The section is concluded with the introduction of peak current mode control both in theory and practice.

## **2.2 DC/DC Converter Topologies and Operation**

In this part of the thesis, the converter topologies and the principles that the DC/DC conversion is based on, will be examined. The operation of a DC/DC converter can be examined under two different conditions depending on the inductor current continuity. If the inductor current never falls to zero in any period during the converter operation, then the converter is said to be operating in the continuous conduction mode (CCM). Otherwise the operational mode is named as the discontinuous conduction mode (DCM).

### **2.2.1 Non-Isolated Topologies in CCM**

In Figure 2.2, five basic non-isolated converters were listed. These converters employ one controllable switch (MOSFET or IGBT in general) and one uncontrollable switch (diode) with different switch network and filtering configurations. To be studied first, and maybe considered as the most important topology, is the step-down or so called “buck” converter topology which is shown in Figure 2.3(a). The buck converter, as the name indicates bucks or steps-down the voltage level that is applied as input. The converter operation starts with the controlled switch conduction period. This controlled switch is typically and generally a MOSFET. While the MOSFET is conducting, the complementary diode will be reverse-biased with the input voltage level, hence it will be off. In this mode of the circuit, the current flows through the inductor and is delivered to the output capacitor and load. In this state, the inductor is connected between the input voltage source and the load. That means inductor voltage will be the difference between

input voltage and output voltage across its terminals. Since this converter steps down the voltage, the input voltage is greater than the output voltage and hence the difference will be positive which means this is the energy storage mode for the

inductor. When the MOSFET is turned-off, the diode will be on since the inductor current is nonzero and cannot change instantaneously. Starting that moment, the diode freewheels the energy stored in the passive elements to provide the continuity of the energy that is delivered to output. Now the inductor is directly connected to the output but it is biased with negative polarity which means inductor is releasing its stored energy to the capacitor and the load. In this condition, the inductor current is expected to decrease since its energy is delivered to the output. Figure 2.3(b) shows the inductor voltage and current waveforms.

At steady-state, the average value of the inductor current will not change over one switching period. It rises to its peak at the end of mode-1 and returns to the initial value (the value it started to rise) at the end of the freewheeling mode (mode-2). Therefore, the average of the stored energy in the inductor, and hence average flux does not change in one switching period. In other words, the average flux change through one switching period is zero. According to the Faraday's law, the total flux is directly proportional to the total volt-seconds that is applied to the inductor. As a corollary, it can be stated that at steady-state, the total volt-seconds of an inductor over one switching period is zero and this volt-second principle is the way to find an expression between the input and the output voltage. Applying the volt-second balance rule to the inductor of the buck converter the following result can be obtained.

$$DT_s(V_{IN} - V_O) + (1 - D)T_s(-V_O) = 0 \quad (2.1)$$

$$\frac{V_O}{V_{IN}} = D \quad (2.2)$$

Here  $D$  is the duty cycle which is introduced in Section 2.1 and  $T_s$  is the switching period. The capacitor correspondence of the volt-second balance is the ampere-second balance. At steady-state, as the inductors do not carry DC voltages, a capacitor does not allow DC current to flow. Hence at steady-state, the total charge

increase of a capacitor in one switching period is zero according to the principle of capacitor charge balance (ampere-seconds balance).

As a conclusion, in the buck converter, the input voltage source is processed by a switch network which is at the input side of the converter and is filtered by a second order low pass filter. The inductor filters some part of the current harmonics, but not all of them. The capacitor provides a low-impedance path for the remaining high frequency harmonics and hence the load can get smooth voltage and more smooth current. In fact, the current through the capacitor is the AC component of the inductor current and the DC component is delivered to the load.

The second basic topology is the step-up or so called “boost” topology which can be derived from the buck converter by using the principle of duality. If a converter is a buck type when one looks from the input to the output, then it is a boost converter from output to the input point of view. The basic circuit diagram of the boost converter is shown in Figure 2.4.

In the boost converter, the filter inductor is at the input side. This time the controllable switch is in the low side and hence an easier gate drive is possible since the source of the MOSFET is connected to the circuit ground. The first mode of the circuit operation starts with the switch turn on again. The inductor is directly connected to the input source and stores energy in this mode. The diode breaks the connection of the input source with the output and the load is supplied from the output capacitor. When the switch turns off, the inductor current commutates to diode, the inductor releases its stored energy through the diode. By applying inductor volt-second rule the input to output relationship can be found as follows:

$$\frac{V_o}{V_{IN}} = \frac{1}{1-D} \quad (2.3)$$

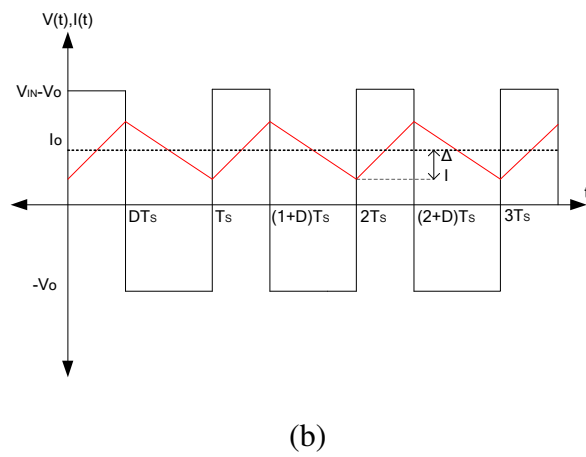
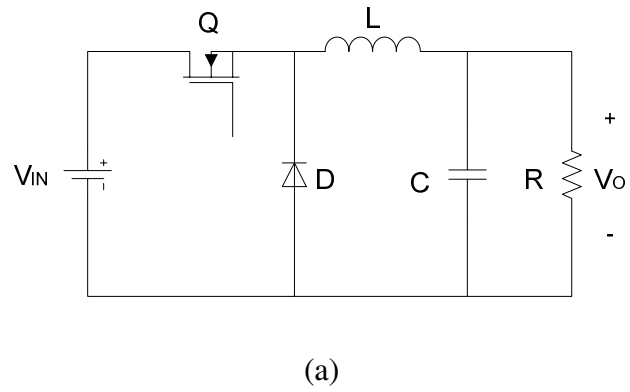


Figure 2.3 The step-down (buck) converter: (a) circuit diagram; (b) inductor voltage, and current waveforms.

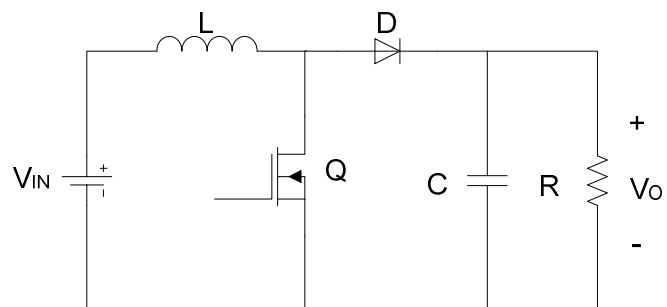


Figure 2.4 Boost converter basic circuit diagram.

The buck-boost converter which is referred as an indirect converter in [9], [12] is shown in Figure 2.5.

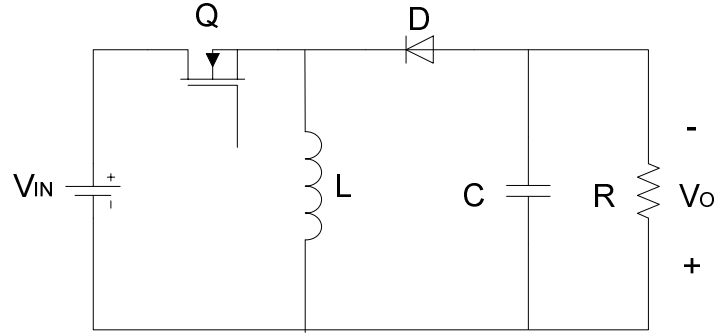


Figure 2.5 The basic circuit diagram of the buck-boost converter.

During the switch conduction time ( $DT_s$ ) the inductor receives energy from the input source and the reverse-biased diode disconnects the source from the load. In this mode the load energy is supplied by the output capacitor as in the boost converter case. When the switch turns off, the diode becomes forward biased and takes the inductor current on and the stored energy in the inductor is delivered to the load. Since the inductor current is in reverse direction, the load also receives the

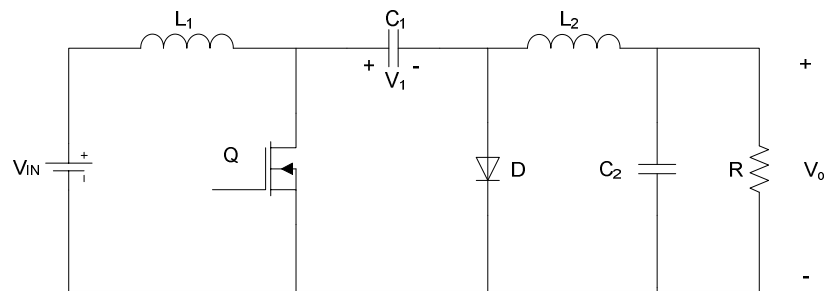
output current in the reverse direction, unlike the formerly introduced converters. Therefore, the output voltage of the buck-boost converter will have reverse polarity in comparison to its input. Again, the voltage conversion ratio can be obtained as in (2.4) by applying the volt-second balance rule.

$$\frac{V_O}{V_{IN}} = \frac{D}{1-D} \quad (2.4)$$

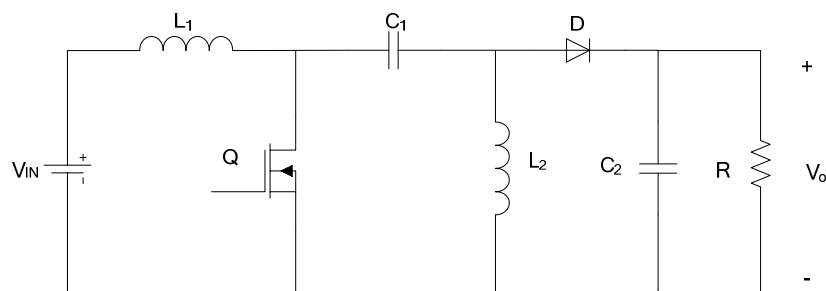
It is obvious from the converter operation that the input and output are never directly connected to each other. In mode-1 the output takes energy from the capacitor and in mode-2, inductor delivers energy to the output. There is no direct DC path between the input and the output. That's the reason why the buck-boost

converter is classified as an indirect converter, unlike the buck and boost converters which are direct converters.

The basic non-isolated topologies have been presented up to this point. Figure 2.6(a) and (b) show the other two important non-isolated indirect converters, the Cuk converter and single-ended primary inductor converter (SEPIC), respectively. Both converters are buck-boost derived topologies. The importance of Cuk converter is the presence of the inductors both at the input and at the output of the converter. These inductors provide non-pulsating current in both sides of the circuit. But the load voltage polarity is still reversed. The SEPIC converter solves the reverse voltage polarity problem of the former indirect topologies and that's the main reason of its preference in any buck-boost application.



(a)



(b)

Figure 2.6 Two additional popular non-isolated topologies: (a) Cuk converter; (b) SEPIC converter.



### 2.2.2 Isolated Topologies in CCM

Isolated topologies utilize a high frequency transformer in their circuitry and they are derived from the basic non-isolated topologies. These converters have a wide power range of application from a few watts to hundreds of kilowatts [24]. The most popular topologies of DC/DC converters will be introduced in this section.

The first isolated topology to be introduced is the flyback converter shown in Figure 2.7. The flyback converter can be obtained by replacing the inductor of the buck-boost converter with a transformer and reversing the polarity of the secondary side with respect to primary. This polarity reversal changes the polarity of the diode and capacitor as well; thus solves the problem of the negative load voltage polarity of the buck-boost converter.

The transformer of the flyback converter topology is not a conventional transformer. A transformer is generally used to transfer energy. It is not a desired situation for a transformer to store energy inside the core. The stored energy means leakage in any transformer. But as the literature name implies, “flyback transformer” is specific for a flyback converter and it stores energy in one mode of operation and then transfers it to the output side in the other mode. It is also named as coupled-inductor to refer both the energy storage and transferring duties.

The operation of the flyback converter starts with the turning on of the controlled switch which is placed at the lower side of the circuit to simplify the gate drive circuit. The primary terminals are connected to the input source and energy is stored in the primary inductor in this mode of operation. This input voltage level will also be observed in the secondary side with reverse polarity and as scaled with the turns ratio of the transformer. The reverse polarity of the voltage, reverse biases the diode and load energy requirement is supplied by the output capacitor. When the switch turns off, the magnetic field collapses and the voltage reverses causing the diode turn on. The transformer secondary transfers the stored energy to the load.

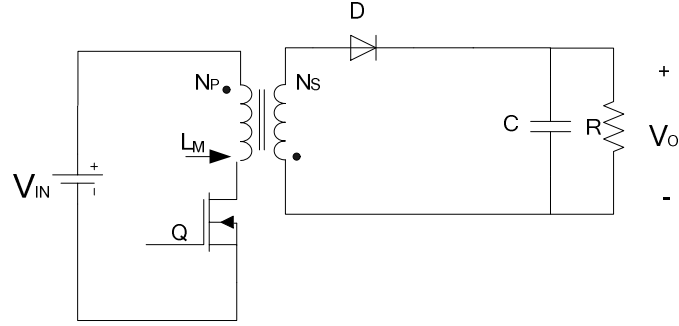


Figure 2.7 The flyback converter basic circuit diagram.

The voltage transfer ratio of the flyback converter can be found as in (2.5) by applying the volt-second balance principle to the magnetizing inductor of the transformer. The currents of both primary and secondary windings are always discontinuous. The operating mode of the flyback controller is determined by the magnetization current. For that reason, the DCM is sometimes referred as complete demagnetization mode in flyback converters. The detailed modeling of this situation can be found in [1], [13].

$$\frac{V_O}{V_{IN}} = \frac{N_s}{N_p} \frac{D}{1-D} \quad (2.5)$$

Since the applied primary voltage is always positive, the flux in the core is always in the same direction. That means the flyback converter operation always takes place in the first quadrant of the core B-H curve which points the under-utilization of the core. For that reason the flyback converter is only used up to a few hundred watts power rating.

The forward converter which is a buck derived topology is illustrated in Figure 2.8. It is clear in the figure that the secondary circuit resembles a buck converter with a replaced D1 diode instead of a controlled switch. The topology is a buck converter with a transformer used to transfer energy and to provide isolation. A forward

converter transformer has an additional winding except from primary and secondary windings. This winding is referred as tertiary winding [9], demagnetization winding [1], or catch winding and works as the secondary winding of a flyback transformer to reset the core. When the switch is conducting, primary terminals see the DC source with positive polarity. In this case D1 is forward biased. D2 and D3 diodes are reverse-biased. When the switch turns off, the energy stored in the magnetizing inductance of the primary winding is transferred to the demagnetizing branch and forward biases D3. In this mode, output current continuity is provided by the output inductor and capacitor currents which circulate through D2 becoming forward biased with the switch turn off.

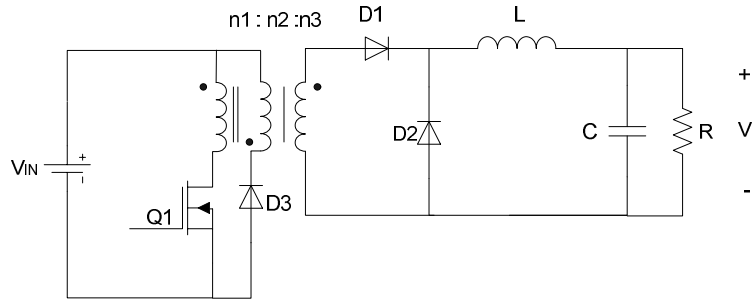


Figure 2.8 Forward converter circuit diagram.

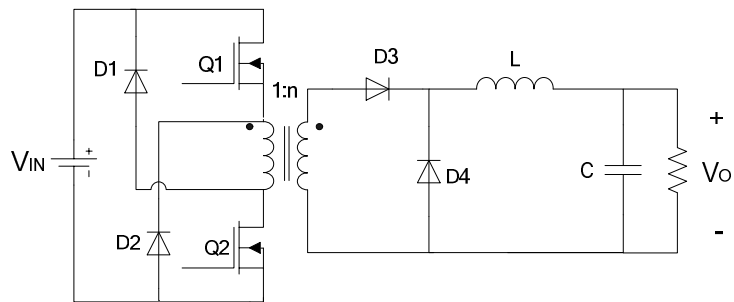
The voltage transfer ratio expression can be derived by the volt-second balance rule applied to the output inductor as in (2.6).

$$\frac{V_o}{V_{IN}} = \frac{N_s}{N_p} D \quad (2.6)$$

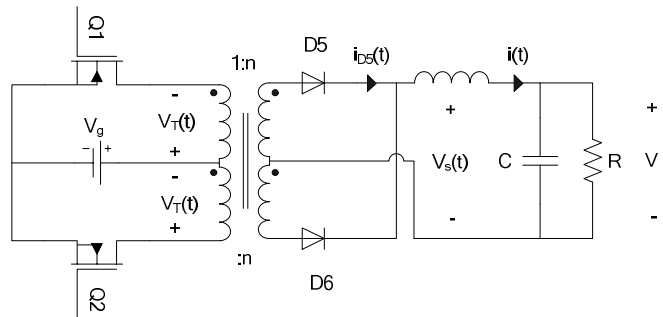
Since the demagnetization of the magnetizing current requires some specific time period determined by the primary and tertiary winding turns ratio, the duty cycle of the forward converter is restricted in conjunction with this ratio as well. The magnetizing inductance of transformer operates in discontinuous mode in conjunction with diode D3. The output inductor in conjunction with D2 can operate both in continuous or discontinuous mode. Since the converter is a buck derived

topology, the output current has a non-pulsating behavior. That makes the forward converter suitable for high output current applications as well [13].

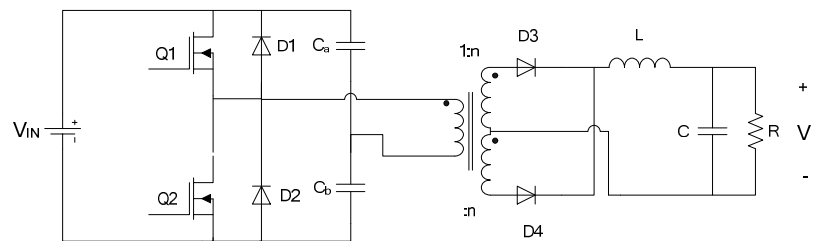
The two basic isolated topologies have been discussed up to this point. As listed in Figure 2.2, there are four more converters under the classification of isolated topologies. These converters are the two-switch forward converter, push-pull converter, half-bridge and full-bridge converters and shown in Figure 2.9(a), (b), (c), and (d), respectively.



(a)



(b)



(c)

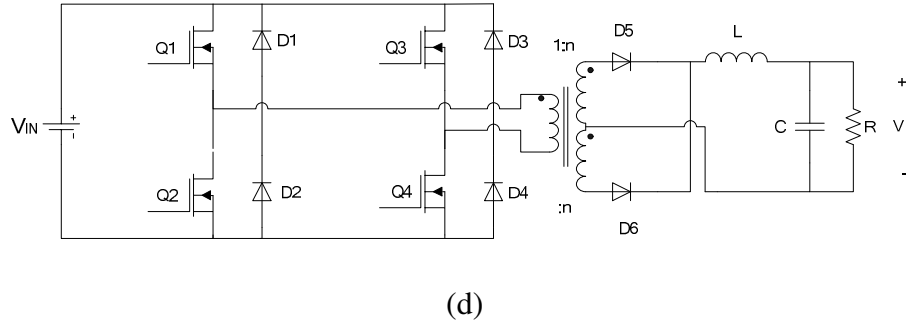


Figure 2.9 Advanced isolated converter topologies: (a) two-switch forward converter; (b) push-pull converter; (c) half-bridge converter; (d) full-bridge converter.

The two-switch forward converter implements two active switches operating simultaneously and anti-parallel diodes to provide demagnetization. For that reason the tertiary winding can be removed from the transformer. Other three topologies basically depend on the push-pull philosophy. The push-pull converter achieves demagnetization by implementing two active switches and a center-tapped transformer in both the primary and secondary sides. One switch applies positive voltage to the primary in the first switching period during  $DT_s$  (pushing the flux), the other switch applies negative voltage in the next switching period in the same  $DT_s$  duration (pulling the flux). The two switching period completes the energy transfer period and the core utilization is better than the other single quadrant utilizing converters. The half –bridge converter shown in Figure 2.9(c), uses two equal series capacitors to divide the input voltage equally and two switches to apply the positive and negative voltages to the primary terminals with respect to the common point of the capacitors. The push-pull idea is the same and is completed in two switching periods. The full-bridge converter is used in high-power applications. When two capacitors of the half-bridge converter are replaced by another half-bridge leg, the full-bridge converter is obtained. The push-pull idea remains the same and the secondary side circuit operations are the same in all three push-pull based converters. Further explanations on the subject can be found in [1], [12] and [13].

### 2.2.3 DC/DC Converters in Discontinuous Conduction Mode

If the inductor current in any DC/DC converter, decreases to zero before the next switching instant is reached, there will be a time gap between transitions from mode-2 to mode-1 where neither switches carry any current. A third circuit mode arises after mode 2. Any converter operating in this mode is said to be operating in the discontinuous conduction mode (DCM). DCM arises when the switching ripple in an inductor current or capacitor voltage is large enough to cause the polarity of the applied switch current or voltage to reverse [13]. DCM generally occurs in high inductor current ripples meaning low inductor values in conjunction with the light loads meaning low average current value. In this section, the DCM operation will be explained and the results will be presented with the derivation of the buck converter results only.

The inductor current at the boundary of CCM and DCM which can be called as critical conduction mode is shown in Figure 2.10. This is the critical mode because, if the current ripple becomes larger or if the load current becomes smaller than these presented values the system goes into DCM. In the critical mode the circuit is still inside the CCM of operation.

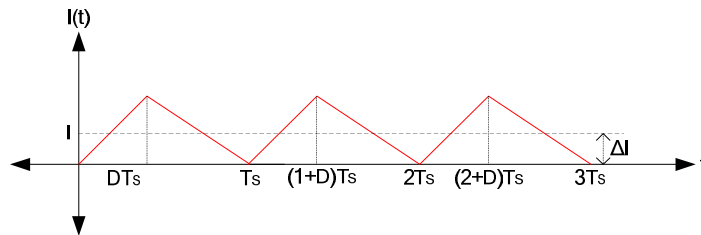


Figure 2.10 Critical conduction mode of inductor current.

As seen in Figure 2.10, the average inductor current value  $I$  (which is equal to the DC load current of a buck converter) is equal to half of the inductor current ripple referred as  $\Delta I$ . Thus, a DCM criterion can be defined by using these two current

expressions. Whenever the average current value  $I$  is larger than  $\Delta I$ , the system operates in CCM. But, if average current value  $I$  is reduced below the  $\Delta I$  value the system goes into DCM.

$$I > \Delta I \rightarrow \text{CCM}$$

$$I < \Delta I \rightarrow \text{DCM} \quad (2.7)$$

By calculating the DC and the ripple value of the inductor current of any converter, one can easily find an expression for DCM condition. Applying this rule to the buck converter, the condition to operate in DCM is found as follows.

$$\frac{2L}{RT_s} < (1-D) \quad (2.8)$$

$$K < K_{cr}(D) \quad \text{for DCM} \quad (2.9)$$

where

$$K = \frac{2L}{RT_s} \quad (2.10)$$

$$K_{cr}(D) = (1-D) \quad (2.11)$$

In the expressions above  $K$  is a circuit dependent variable.  $K_{cr}(D)$  is a topology dependent variable. It can be calculated whether a buck converter will operate in CCM or DCM at any duty cycle or not, by using the expressions derived. Further results of other converters are available in [13] and are tabulated at the end of this section in Table 2.1.

For DCM, the discontinuous inductor voltage and current waveforms are shown in Figure 2.11. The first two modes of the circuit are the same as the two modes of CCM operation. During  $D_1T_s$  the transistor conducts, during  $D_2T_s$  the diode conducts, and during  $(1-D_1-D_2)T_s$  neither the transistor nor the diode conducts. In

mode 3 the load current is provided by the output capacitor. In order to find an expression for the voltage conversion ratio the inductor volt-second balance rule can be applied to the filter inductor.

$$D_1 T_s (V_{IN} - V_O) + D_2 T_s (-V_O) + (1 - D_1 - D_2) T_s (0) = 0$$

$$V_O = V_{IN} \frac{D_1}{D_1 + D_2} \quad (2.12)$$

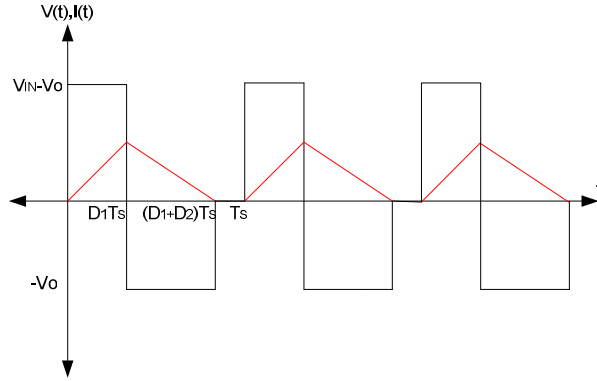


Figure 2.11 The buck converter inductor voltage and current waveform for DCM.

In equation (2.12)  $D_1$  corresponds to the duty cycle of the transistor which we previously referred as “D” in CCM. But, the diode duty cycle  $D_2$  is an unknown parameter. Hence, another equation is needed to complete the calculations. The second equation can be derived using the capacitor ampere-seconds balance rule or capacitor charge balance rule. By using the capacitor ampere-seconds balance rule and integrating the current one can obtain the following inductor current expression.

$$I = \frac{V_{IN} - V_O}{L} \frac{(D_1 + D_2) D_1}{2} T_s \quad (2.13)$$

Using (2.12) and (2.13) one can obtain the input and output voltage relation of (2.14) for the buck converter in DCM.



$$\frac{V_O}{V_{IN}} = \frac{2}{1 + \sqrt{1 + \frac{4K}{D_1^2}}} \quad (2.14)$$

where  $K$  is as defined in equation (2.10). For the derivation steps refer to reference [13]. With the same approach the results for the conversion ratios can be obtained for other converters. The results are tabulated for the non-isolated converters in

table 2.1. The same principles are valid for discontinuous modes of the basic isolated converters. In the flyback converter, both sides of the transformer are already discontinuous. Therefore the calculations for DCM are processed on the magnetizing inductance of the flyback transformer. For the forward converter, the transformer winding currents are discontinuous as well, but DCM is determined according to the filter inductor current. Further explanations on DCM can be found in [13].

Table 2.1 Voltage conversion ratios of the basic non-isolated converters in DCM.

Converter	DCM Conversion Ratio	$K_{cr}(D)$
Buck	$\frac{2}{1 + \sqrt{1 + 4K/D^2}}$	$1-D$
Boost	$\frac{1 + \sqrt{1 + 4D^2/K}}{2}$	$D(1-D)^2$
Buck-Boost	$-D/\sqrt{K}$	$(1-D)^2$

### 2.3 Modeling and Small-Signal Transfer Functions of DC/DC Converters

The output voltages of DC power supplies are regulated to be within a specified tolerance band in response to changes in the output load and the input line voltages [1]. Therefore, SMPS systems always include a closed-loop controller generally

with negative feedback. One of the duties of the power supply designer is to design a closed-loop controller (compensator, regulator) that corrects the errors in the output voltage according to a reference input.

To design an error amplifier for a closed-loop system, the linear dynamic model of the converter is needed. The nonlinear converter circuits must be modeled to obtain

the linear mathematical representation of the system. Basically, modeling is the representation of physical phenomena by mathematical means [13]. The modeling replaces the nonlinear converter circuit with the linear time invariant converter model. The obtained model includes the dominant behavior of the system and some complex phenomena are excluded. For example, a buck converter gate drive signals are modulated in a few tens of kilohertz and maybe hundreds of kilohertz. However, the dominant behavior of the output voltage is different because of the second order low-pass filter at the output stage which has much bigger time constant than the modulator. Hence, one can neglect the high switching frequency component as ignoring its effect on the converter control behavior.

There are two main modeling methods reported in the literature: State-space averaging and circuit averaging. In this section, these two modeling approaches will be discussed.

### **2.3.1 State-Space Averaging**

State-space averaging is a formal method for averaging. The method is based on the state-space representation of the converter modes. State vectors are described and the equations can be written in a compact matrix form. The variables which are related with the energy storage of the converter are the state variables of the converter. The state-space representation of a system is as follows:

$$K \frac{dx(t)}{dt} = Ax(t) + Bu(t) \quad (2.15)$$

$$y(t) = Cx(t) + Eu(t) \quad (2.16)$$

$x(t)$  is the state vector,  $y(t)$  is the output vector, and  $u(t)$  is the input vector which represents the independent inputs of the system.  $K$  is an  $n \times n$  diagonal matrix where  $n$  is the number of energy storage components; capacitors and inductors for an electrical system.

Now the state-space averaged model of a buck converter will be derived. The state variables of a buck converter are the capacitor voltage and inductor current.

$$x(t) = \begin{bmatrix} v_o(t) \\ i_L(t) \end{bmatrix} \quad (2.17)$$

The output vector can be any variable in the circuit that is intended to be calculated. Here input current  $i(t)$  is chosen for the output vector. Hence  $i(t)$  is chosen as the only output vector,

$$y(t) = [i(t)] \quad (2.18)$$

The only independent input to the system is the input voltage source. Therefore the input vector is  $1 \times 1$  matrix consists of the input voltage source.

$$u(t) = [v_{IN}(t)] \quad (2.19)$$

State-space representations of mode 1 equations are:

$$\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix} \begin{bmatrix} \frac{di_L(t)}{dt} \\ \frac{dv_o(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -1 \\ 1 & -1/R \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \end{bmatrix} [v_{IN}(t)] \quad (2.20)$$

where

$$K = \begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix} \quad (2.21.a)$$

$$A_1 = \begin{bmatrix} 0 & -1 \\ 1 & -1/R \end{bmatrix} \quad (2.21.b)$$

$$B_1 = \begin{bmatrix} 1 \\ 0 \end{bmatrix} \quad (2.21.c)$$

$$\dot{i}(t) = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix} + \begin{bmatrix} 0 \end{bmatrix} v_{IN}(t) \quad (2.22)$$

where

$$C_1 = \begin{bmatrix} 1 & 0 \end{bmatrix} \quad (2.23.a)$$

$$E_1 = \begin{bmatrix} 0 \end{bmatrix} \quad (2.23.b)$$

State-space representations of mode 2 equations are:

$$\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix} \begin{bmatrix} \frac{di_L(t)}{dt} \\ \frac{dv_o(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -1 \\ 1 & -1/R \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_g(t) \quad (2.24)$$

where

$$K = \begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix} \quad (2.25.a)$$

$$A_2 = \begin{bmatrix} 0 & -1 \\ 1 & -1/R \end{bmatrix} \quad (2.25.b)$$

$$B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \quad (2.25.c)$$

$$[i(t)] = \begin{bmatrix} 0 & 0 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix} + [0] [v_g(t)] \quad (2.26)$$

where

$$C_2 = \begin{bmatrix} 0 & 0 \end{bmatrix} \quad (2.27.a)$$

$$E_2 = \begin{bmatrix} 0 \end{bmatrix} \quad (2.27.b)$$

The state-space averaged model is given as

$$0 = AX + BU \quad (2.28)$$

$$Y = CX + EU \quad (2.29)$$

where

$$A = DA_1 + (1-D)A_2 \quad (2.30.a)$$

$$B = DB_1 + (1-D)B_2 \quad (2.30.b)$$

$$C = DC_1 + (1-D)C_2 \quad (2.30.c)$$

$$E = DE_1 + (1-D)E_2 \quad (2.30.d)$$

Using equations of (2.30) A, B, C, and E matrices can be obtained as follows:

$$A = \begin{bmatrix} 0 & -1 \\ 1 & -1/R \end{bmatrix} \quad (2.31.a)$$

$$B = \begin{bmatrix} D \\ 0 \end{bmatrix} \quad (2.31.b)$$

$$C = \begin{bmatrix} D & 0 \end{bmatrix} \quad (2.31.c)$$

$$E = \begin{bmatrix} 0 \end{bmatrix} \quad (2.31.d)$$

The converter equations in equilibrium point are:

$$0=AX+BU=\begin{bmatrix} 0 & -1 \\ 1 & -1/R \end{bmatrix}\begin{bmatrix} I_L \\ V_o \end{bmatrix} + \begin{bmatrix} D \\ 0 \end{bmatrix}[V_{IN}] \quad (2.32)$$

$$Y=CX+EU \quad (2.33)$$

$$I=\begin{bmatrix} D & 0 \end{bmatrix}\begin{bmatrix} I_L \\ V_o \end{bmatrix} + \begin{bmatrix} 0 \end{bmatrix}[V_{IN}] \quad (2.34)$$

It is obvious that, the equations of (2.32) to (2.34) coincide with the DC operating point expressions of buck converter which are derived in section 2.2.1. After deriving the DC equations and obtaining the DC model, one needs to find the small-signal AC model equations to obtain the transfer function. The equations for an averaged system are given as:

$$K \frac{d\hat{x}(t)}{dt} = A \hat{x}(t) + B \hat{u}(t) + \{(A_1 - A_2)X + (B_1 - B_2)U\}\hat{d}(t) \quad (2.35.a)$$

$$\hat{y}(t) = C \hat{x}(t) + E \hat{u}(t) + \{(C_1 - C_2)X + (E_1 - E_2)U\}\hat{d}(t) \quad (2.35.b)$$

Using the above equation set, the small signal model for the buck converter can be obtained. The results are given below.

$$L \frac{d\hat{i}_L(t)}{dt} = -\hat{v}_o(t) + D \hat{v}_{IN}(t) + V_{IN} \hat{d}(t) \quad (2.36)$$

$$C \frac{d\hat{v}_o(t)}{dt} = \hat{i}_L(t) - \frac{\hat{v}_o(t)}{R} \quad (2.37)$$

$$\hat{i}(t) = D \hat{i}_L(t) - I_L \hat{d}(t) \quad (2.38)$$

where the “ $\hat{x}(t)$ ” notation defines the small signal AC variations of the corresponding variable around the “X” DC operating point. By using these

equations, a small-signal equivalent circuit can be constructed which is detailed in [13]. Thus, obtaining the transfer function which follows the modeling process can be carried out using the circuit model as well as it can be derived directly using the model equations.

Another critical point about the state-space averaging is the CCM of the converters can be modeled only. Since the method averages the converter state equations instead of converter waveforms, the discontinuity period of DCM cannot be predicted by the introduced equations unless additional work is carried out. Therefore, in such cases state-space averaging is not suitable and it is more practical to model the DCM operation and the resonant converters using the circuit averaging method.

### **2.3.2 The Circuit Averaging Method**

The circuit averaging method was developed historically earlier than the state-space averaging method and described in [25]. Circuit averaging is a more general method with respect to the state-space averaging concept as well. The method performs manipulations and calculations directly on the circuit, instead of making them on the converter equations.

The main idea of the circuit averaging method is obtaining a time invariant network by replacing the switches by dependent voltage and current sources [13]. When a time-invariant network is obtained, the averaging and linearization operations can be performed on the dependent sources' waveforms. In the following, the circuit averaging steps will be explained by applying them on an ideal boost converter. The boost converter circuit diagram was shown in Figure 2.4. The first aim is to obtain a time invariant network by replacing the switches with dependent sources which provide equivalent waveforms with the switches. In mode 1 of the converter, the MOSFET conducts; hence there is no voltage drop on the switch since the

components are assumed as ideal. In mode 2, the diode turns on and the switch is off. Hence the drain of the MOSFET is connected to the positive output terminal through diode. The MOSFET source terminal has already been connected to the circuit ground. The total voltage seen by the MOSFET is the output voltage  $V_O$  and only in the interval of  $(1-d)$ . That means one can replace the MOSFET with a dependent voltage source whose waveform can be described as  $\{1-d(t)\}V_O(t)$ . On the other hand, in mode-1 the diode does not conduct any current and in mode-2, it

turns on and connects the input and the output circuits. That means diode carries the input current to the output during the  $(1-d)$  interval. Hence the diode can be replaced with a dependent current source whose value is  $\{1-d(t)\}i(t)$ . The corresponding equivalent circuit is shown in Figure 2.12(a).

With the above described steps, the time-invariant network is reached but the circuit is still discontinuous. By averaging the waveforms in one switching period, one can obtain a continuous equivalent of the waveforms and hence a network which discards analytic difficulty of discontinuous waveforms. The averaging definition is given as:

$$\langle x(t) \rangle = \frac{1}{T_s} \int_t^{t+T_s} x(t) dt \quad (2.39)$$

The effect of averaging is approximately that of a low-pass filter with cut-off frequency  $\omega = 2\pi/T_s$  [25]. The result of averaging step is illustrated on the waveform in Figure 2.12(b). The dependent current source modeling the diode has the same waveform with the dependent voltage source. Now the converter waveforms were averaged and the system has become continuous which brings simplicity in calculations. The averaged model of the circuit is shown in Figure 2.12(c). The  $\langle x(t) \rangle$  notation on circuit models implies averaged waveforms.



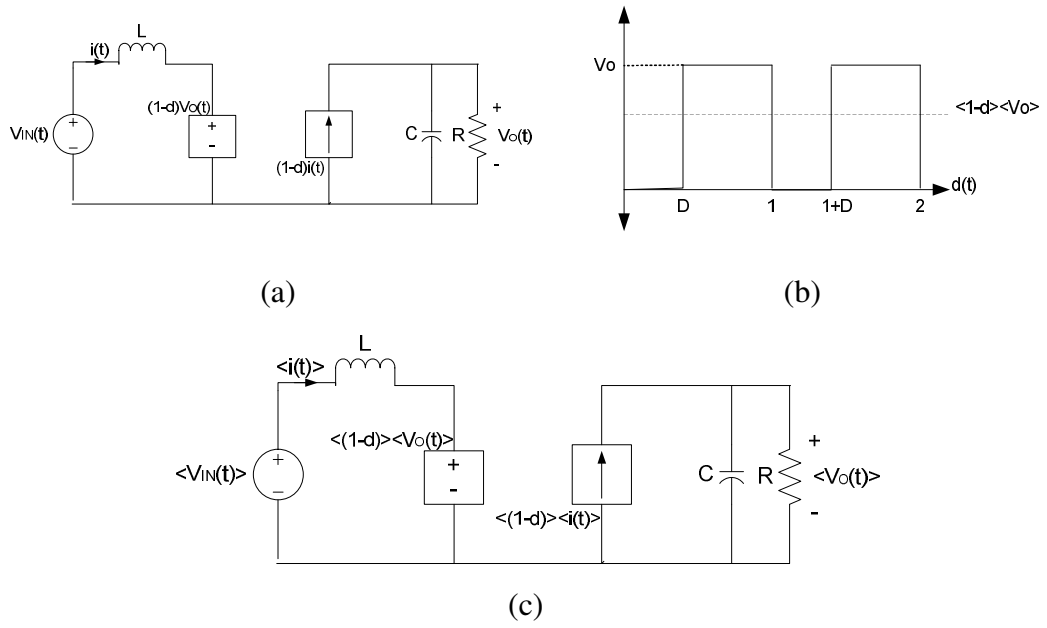


Figure 2.12 Boost converter model: (a) switch network replaced with dependent sources; (b) controlled switch voltage waveform; (c) averaged model.

Now the circuit of Figure 2.12(c) is time invariant and averaged but, still including the multiplication of time varying functions, therefore the system is still nonlinear. The converter has two independent inputs. One is the input voltage source  $v_{IN}(t)$ , the other is the control input  $d(t)$ . After that point, the converter can be linearized by treating one input as a constant and the other input as a disturbance under investigation. First, the duty cycle function  $d(t)$  is assumed to be constant as the DC operating value  $D$ . Now the circuit in Figure 2.12(c) becomes the circuit of Figure 2.13. There is no multiplication of two time varying functions anymore. The system is linearized. The averaged functions with notation  $<x>$  are assumed to comprise two components; a quiescent DC value (denoted by capital letters) and a superimposed AC variation (denoted by lower case letters with cap) around this DC point. Since the system is linear, DC inputs can be related with DC outputs and AC inputs can be related with the AC outputs as shown in Figure 2.14(a) and (b) respectively.

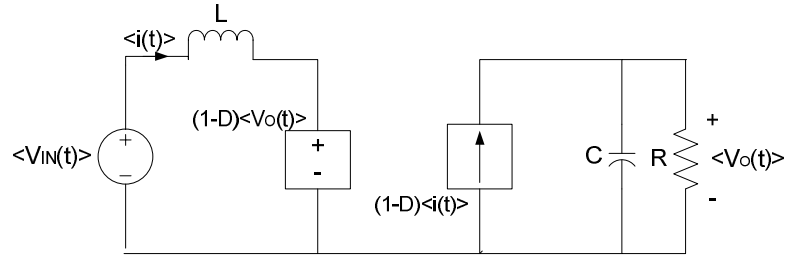


Figure 2.13 Linearized circuit for line input disturbances.

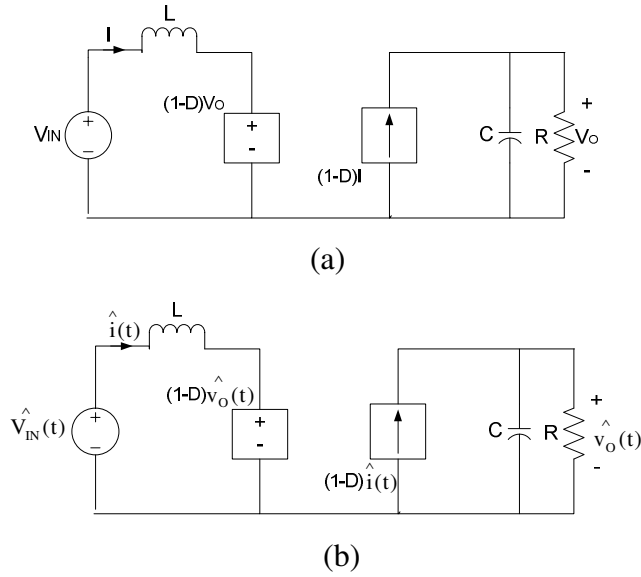


Figure 2.14 Linearized circuit model: (a) DC components; (b) small-signal AC components.

Figure 2.14 (a) shows that the results of the DC circuit coincide with the DC equations derived earlier. Now the circuit of Figure 2.14 (b) is under investigation. The circuit only includes the small-signal AC variations in the system. If the two sides of the circuit can be combined, then a complete equivalent circuit modeling the input disturbance to output can be obtained. In order to connect these separate terminals together, the voltages across both terminals and the current through the terminals must be equal. Circuit of Figure 2.14 (b) can be transformed to the desired condition by applying simple manipulations to the circuit. First, the terminal voltages can be equated by dividing all the sources and the impedances at the left

hand side of the circuit by  $(1-D)$ . This will cause the terminal voltage to be equal to the output voltage while keeping the current circulating around the loop constant. A similar manipulation in the right hand side loop can be carried out to equate the currents. If all the impedances in that loop is scaled with  $(1-D)$ , the current is scaled to the desired value while the output voltage remaining constant. The new form of the circuit is shown in Figure 2.15. It is clearly seen on the circuit that the voltages and the currents of both terminals are the same; hence, the two terminals can be combined by removing the dependent sources. The final circuit is shown in Figure 2.16.

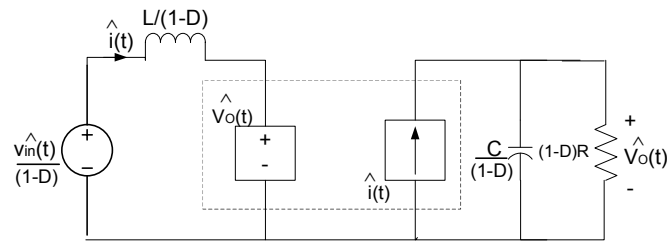


Figure 2.15 Circuit model for line input variations with terminal parameters scaled.

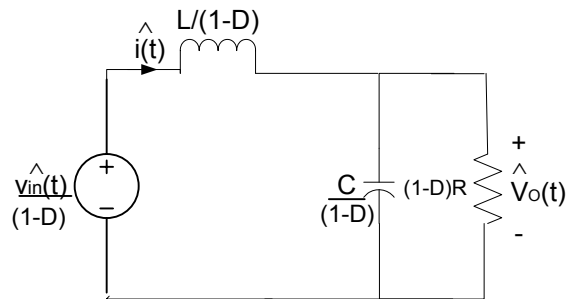


Figure 2.16 Equivalent circuit model for line input variations-to-output.

After setting the duty cycle to the constant value  $D$ , the responses to input variations have been analyzed and the equivalent circuit in Figure 2.16 is obtained. This time responses to control input variations will be investigated by assuming the input

voltage source of Figure 2.12(c) is constant DC value  $V_{IN}$ . The equivalent circuit in Figure 2.12(c) now is reduced to the circuit shown in Figure 2.17. The converter model in Figure 2.17 is still nonlinear because of the  $\langle v_o(t) \rangle \langle d(t) \rangle$  multiplication, since both multipliers are time varying functions. Hence linearization is required in the circuit. Now, the averaged values shown in  $\langle x \rangle$  notation are assumed to contain two components one being the quiescent DC value, and the other being the small AC variation.

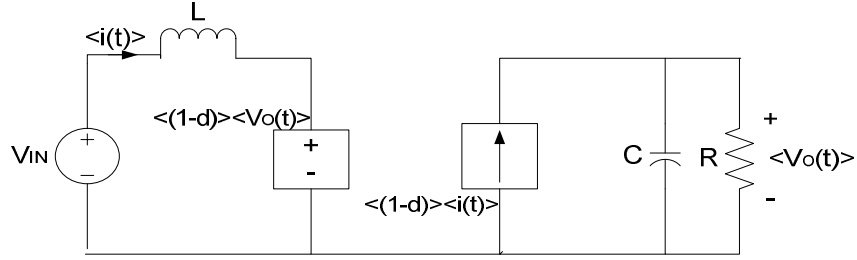


Figure 2.17 Circuit to model the effects of duty cycle variations.

$$\langle v(t) \rangle = V + \hat{v}(t) \quad (2.40)$$

$$\langle d(t) \rangle = D + \hat{d}(t) \quad (2.41)$$

$$\langle i(t) \rangle = I + \hat{i}(t) \quad (2.42)$$

where

$$\hat{v} \ll V, \hat{d} \ll D, \text{ and } \hat{i} \ll I \quad (2.43)$$

$$\langle v(t) \rangle \langle d(t) \rangle = DV + \hat{d}(t)V + D\hat{v}(t) + \hat{v}(t)\hat{d}(t) \quad (2.44)$$

According to the conditions stated in (2.40) to (2.42) the  $\hat{v}(t)\hat{d}(t)$  multiplication becomes negligibly small and can be neglected. the same condition is valid for the  $\langle i(t) \rangle \langle d(t) \rangle$  multiplication. The new small-signal linearized form (nonlinear and DC terms discarded) of the circuit is shown in Figure 2.18.

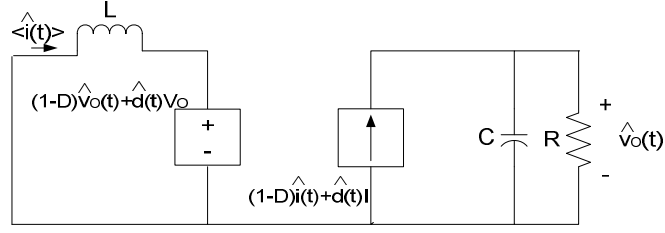


Figure 2.18 Small-signal linearized model for duty cycle variations.

The circuit still needs some manipulations to reach the final form. Since  $d(t)$  represents the independent control input variation,  $d(t)V$  should be modeled with an independent voltage source. Using same approach  $d(t)I$  should be modeled with an independent current source. Since  $v(t)$  and  $i(t)$  are the circuit dependent functions  $Dv(t)$  and  $Di(t)$  should be still dependent sources. Finally, if the required scaling is performed on the circuit, the final form becomes as in Figure 2.19 (a) and the terminals can be combined as shown in 2.19 (b). Using these equivalent circuits, input disturbance-to-output and control-to-output transfer functions can be obtained by simple circuit analysis which will be explained in further sections.

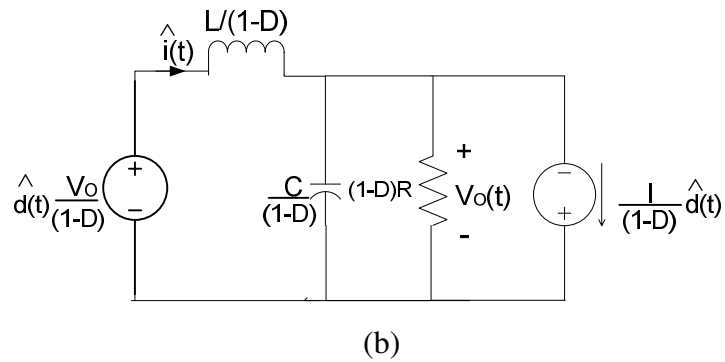
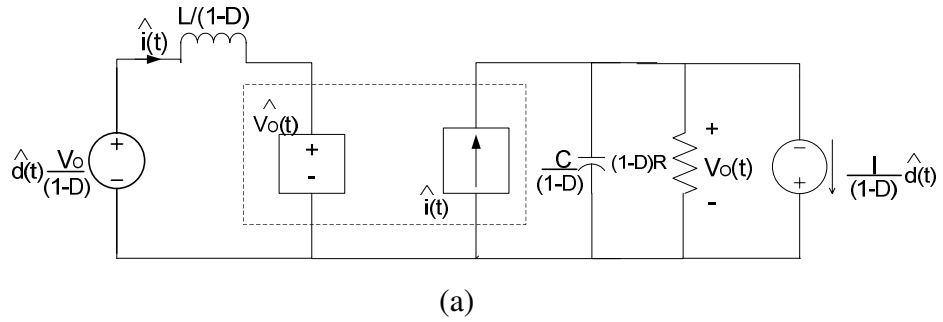


Figure 2.19 Duty cycle variation circuit model: (a) model with independent sources distinguished and terminal parameters scaled; (b) the combined model.

### 2.3.3 Obtaining and Understanding Converter Transfer Functions

In the previous sections two types of modeling have been introduced. The state-space averaging method revealed some equations while circuit averaging revealed some circuit models. In this section the transfer functions of the converters will be derived using the results of both averaging methods. Three equations of buck converter obtained at the end of the state-space averaging method are rewritten here using the Laplace domain expression instead of time domain equations.

$$Ls\hat{i}_L(s) = -\hat{v}_O(s) + D\hat{v}_{IN}(s) + V_{IN}\hat{d}(s) \quad (2.45.a)$$

$$Cs\hat{v}_O(s) = \hat{i}_L(s) - \frac{\hat{v}_O(s)}{R} \quad (2.45.b)$$

$$\hat{i}(s) = D\hat{i}_L(s) - I_L\hat{d}(s) \quad (2.45.c)$$

The control-to-output transfer function  $G_{vd}(s)$  can be obtained by setting the line variations ( $\hat{v}_{IN}(s)$ ) of equation (2.45.a) to zero. The result is given as:

$$G_{vd}(s) = \frac{\hat{v}_O(s)}{\hat{d}(s)} = \frac{V_{IN}}{1 + s\frac{L}{R} + s^2LC} \quad (2.46)$$

By setting the control input variations to zero, line-to-output transfer function  $G_{vi}(s)$  can be obtained using same steps.

$$G_{vi}(s) = \frac{\hat{v}_O(s)}{\hat{v}_{IN}(s)} = \frac{D}{1 + s\frac{L}{R} + s^2LC} \quad (2.47)$$

Both the line-to-output and the control-to-output transfer functions of the ideal buck converter are obtained using the results of state-space averaging. Now the transfer

function of the boost converter will be obtained using the resultant circuit models of circuit averaging.

In the circuit averaging method, two different circuits have been obtained to model both the line-to-output and control-to-output disturbances in Figures 2.16 and 2.19(b) respectively. Hence, the last step is the basic circuit analysis. It is clear in Figure 2.16 that the parallel connected resistor and capacitor are in series with inductor and the circuit can be treated as a voltage divider.

$$\hat{v}_O(s) = \frac{\hat{v}_{IN}(s) \left( \frac{1}{sC} // R \right)}{1-D \left( \frac{sL}{1-D} + \left( \frac{1}{sC} // R \right) \right)} \quad (2.48)$$

$$G_{vi}(s) = \frac{\hat{v}_O(s)}{\hat{v}_{IN}(s)} = \frac{1}{1-D} \frac{1}{1+s \frac{L}{(1-D)^2 R} + s^2 \frac{LC}{(1-D)^2}} \quad (2.49)$$

By applying the same analysis to the circuit of Figure 2.19 (b), the control-to output transfer function can be obtained. However, the derivation of control-to-output transfer function may require some additional work since the circuit model includes two independent sources. To obtain the transfer function the superposition theorem must be applied.

$$G_{vd}(s) = \frac{\hat{v}_O(s)}{\hat{d}(s)} = \frac{1 - \frac{sL}{(1-D)^2 R}}{1 + s \frac{L}{R} + s^2 LC} \quad (2.50)$$

The control-to-output transfer function of the boost converter differs at one point. A right half plane zero exists in the transfer function which introduces additional phase lag and hence makes the control of the boost converter difficult with respect to the buck derived topologies. The general forms of line-to-output and control-to-

output transfer functions are of the form (2.51) and (2.52), respectively. The parameters of the transfer functions of three basic converters are shown in Table 2.2.

$$G_{vi}(s) = G_{i0} \frac{1}{1 + \frac{s}{Q\omega_o} + \left(\frac{s}{\omega_o}\right)^2} \quad (2.51)$$

$$G_{vd}(s) = G_{d0} \frac{1 - \frac{s}{\omega_z}}{1 + \frac{s}{Q\omega_o} + \left(\frac{s}{\omega_o}\right)^2} \quad (2.52)$$

Table 2.2 The parameters of the basic non-isolated converter transfer functions according to the equations (2.51) and (2.52).

	$G_{i0}$	$G_{d0}$	$\omega_o$	$Q$	$\omega_z$
Buck	$D$	$\frac{V}{D}$	$\frac{1}{\sqrt{LC}}$	$R\sqrt{\frac{C}{L}}$	$\infty$
Boost	$\frac{1}{1-D}$	$\frac{V}{1-D}$	$\frac{(1-D)}{\sqrt{LC}}$	$(1-D)R\sqrt{\frac{C}{L}}$	$\frac{(1-D)^2 R}{L}$
Buck-boost	$\frac{D}{1-D}$	$\frac{V}{D(1-D)}$	$\frac{(1-D)}{\sqrt{LC}}$	$(1-D)R\sqrt{\frac{C}{L}}$	$\frac{(1-D)^2 R}{DL}$

The given converter transfer functions have similar forms. The denominators of the transfer functions correspond to the second order low-pass filter characteristics of the converters. In the buck converter transfer function, the result is straightforward since the output stage of the buck converter is directly a second order filter. Since the filter elements are distinguished by the switches in boost and buck-boost converters, the filter characteristics are also changed. In these two converters the frequency of the quadratic poles is multiplied by the factor (1-D) with respect to the buck converter pole frequency. Since D is defined between 0 and 1, (1-D) is always between 0 and 1 as well. That means boost and buck-boost converters have lower



open-loop pole frequency than buck converter of the same parameter values and hence, will be expected to exhibit a slower dynamic response in open-loop operation according to these ideal transfer functions.

Another difference is the right half plane zeroes of the boost and buck boost converters. A positive zero owns the gain characteristics of a negative zero, and the phase characteristics of negative pole. Based on this data it is clear that positive zero introduces additional phase lag and reduces the phase margin. Reduced phase margin threatens both the relative and absolute stability. The positive zero arises because the energy change in the state vectors occurs in opposite direction in any mode. Therefore, additional time is needed for the inductor to recondition the capacitor to the desired energy level. For example, when the duty cycle is increased in a boost converter (which means higher output voltage is intended) more time is spared by the circuit to store energy in the inductor, to increase the inductor energy to the required level (mode 1). Less time is spared to send the inductor energy to the load (mode 2). Since the inductor current cannot change rapidly, the desired energy level cannot be reached instantaneously. At the instant the duty cycle increase occurs, the inductor provides the same amount of current but in a smaller time interval caused by the decrease in  $(1-D)$ . Therefore, load will get less energy until the inductor energy level reaches the required energy level. This causes the load voltage to decrease temporarily. When the inductor recharges the capacitor to new energy level the output voltage will settle to its new value. This positive zero behavior, decreases the controllability of boost derived converters which will be discussed in the next section.

The transfer functions given in (2.51) and (2.52) are given for the ideal case since the converter circuits have been modeled with the assumption of ideal components. Before going on to the control section one critical point must be discussed: The equivalent series resistance (ESR) of the output capacitor. The ESR of the capacitor modifies the transfer function parameters given in the Table 2.2 and introduces an additional zero to all transfer functions which have to be considered in controller

design. The general forms of transfer functions are given in equations (2.53), (2.54) Table 2.3 shows the modifications in the transfer function parameters of three basic topologies, when the ESR is included. Since the DC gains are the same with the transfer function without ESR, DC gain parameters are removed from Table 2.3.

$$G_{vi}(s) = G_{i0} \frac{1 + \frac{s}{w_z}}{1 + \frac{s}{Qw_o} + (\frac{s}{w_o})^2} \quad (2.53)$$

$$G_{vd}(s) = G_{d0} \frac{(1 - \frac{s}{w_{zp}})(1 + \frac{s}{w_z})}{1 + \frac{s}{Qw_o} + (\frac{s}{w_o})^2} \quad (2.54)$$

Table 2.3 shows the modifications of converter transfer functions caused by the capacitor ESR. The most important effect of the capacitor ESR on a converter transfer function is the zero introduced at frequency  $w=1/CR_{ESR}$ . The ESR zero improves the relative stability of the system by improving the phase angle around the crossover frequency (phase margin).

Table 2.3 The parameter changes of the basic non-isolated converter transfer functions, with ESR according to (2.53) and (2.54).

	$w_o$	$Q$	$w_{zp}$	$w_z$
Buck	$\frac{1}{\sqrt{LC(1 + \frac{R_{ESR}}{R})}}$	$\frac{\sqrt{LC(1 + \frac{R_{ESR}}{R})}}{(CR_{ESR} + \frac{L}{R})}$	$\infty$	$\frac{1}{CR_{ESR}}$
Boost	$\frac{(1-D)}{\sqrt{LC(1 + \frac{R_{ESR}}{R})}}$	$\frac{\sqrt{LC(1 + \frac{R_{ESR}}{R})}}{(1-D)(CR_{ESR} + \frac{L}{(1-D)^2 R})}$	$\frac{(1-D)^2 R}{L}$	$\frac{1}{CR_{ESR}}$
Buck-boost	$\frac{(1-D)}{\sqrt{LC(1 + \frac{R_{ESR}}{R})}}$	$\frac{\sqrt{LC(1 + \frac{R_{ESR}}{R})}}{(1-D)(CR_{ESR} + \frac{L}{(1-D)^2 R})}$	$\frac{(1-D)^2 R}{DL}$	$\frac{1}{CR_{ESR}}$

## 2.4 Control of DC/DC Converters

In all switching converters, the output voltage  $v(t)$  is a function of the input line voltage  $v_{IN}(t)$ , the duty cycle  $d(t)$ , and the load current  $i_{load}(t)$ , beside the converter circuit element values [13]. Therefore the disturbances in these parameters induce variations in load voltage. However, in a DC/DC converter a constant voltage is desired in spite of the variations in these functions. A voltage regulator is utilized to provide DC regulation and to obtain reasonable transient response against the disturbances. A voltage regulator system is illustrated as a generic block diagram in Figure 2.20 [13].

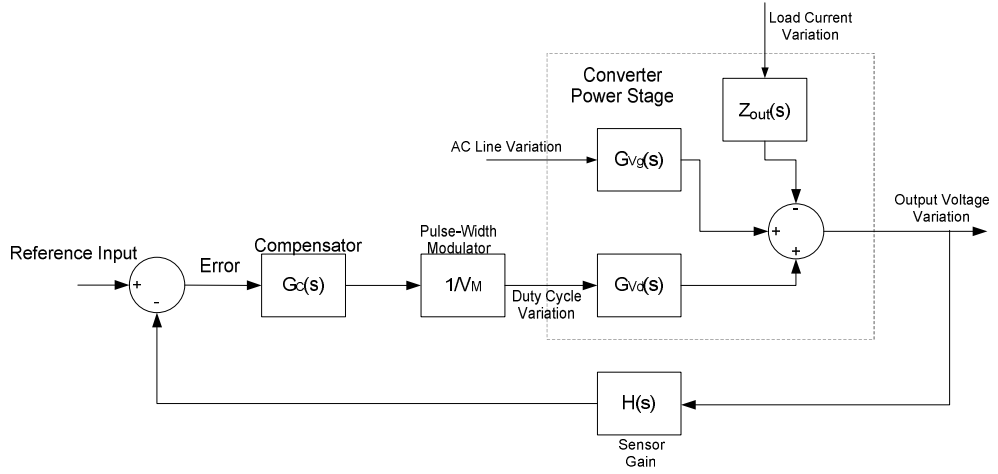


Figure 2.20 Generic block diagram of a voltage regulator system.

The converter power stage is modeled as three blocks: Control-to-output transfer function block, line-to-output transfer function block, and output impedance block.

$$\hat{v}(s) = G_{vd}(s)\hat{d}(s) + G_{vi}(s)\hat{v}_{IN}(s) - Z_{out}(s)\hat{i}_{load}(s) \quad (2.55)$$

The two transfer functions have been introduced in previous sections. The converter equivalent circuit reveals that output impedance is the impedance seen from the output terminals when the disturbances are set to zero.

$$Z_{out}(s) = sL_e + (R // 1/sC) \quad (2.56)$$

The open-loop power stage models of the converters will be complete after adding the effects of load current disturbances are included. Closing the feedback loop will alter the transfer functions from all disturbances to the output in a positive way.

However, closing the loop may create an unstable system although the open-loop transfer functions are stable. For that reason, closing the feedback loop requires stability analysis. Hence, the effects of feedback on the transfer functions and on stability will be examined respectively. These sections will be followed by the compensator design.

#### 2.4.1 Effects of Negative Feedback on Converter Transfer Functions

When the feedback loop is closed, the transfer functions are altered by the loop gain. If all the forward path gains are represented as  $G(s)$  and the feedback path gains are represented as  $H(s)$  the closed-loop transfer function will be

$$X(s) = \frac{G(s)}{1 + G(s)H(s)} \quad (2.57)$$

$G(s)H(s)$  is the overall loop gain since it includes the multiplication of the gains both in the forward and feedback path and will be represented as  $T(s)$  from this point. If the rule is applied to the converter functions the following result will be obtained.

$$\hat{v}(s) = \frac{G_{vd}G_C/V_M}{1 + HG_{vd}G_C/V_M} \hat{v}_{ref}(s) + \frac{G_{vi}}{1 + HG_{vd}G_C/V_M} \hat{v}_{IN}(s) - \frac{Z_{out}}{1 + HG_{vd}G_C/V_M} i_{load}(s) \quad (2.58)$$

The overall loop gain defined previously is given as:

$$T = G_{vd} G_C H / V_M \quad (2.59)$$

Substituting equation (2.59) into (2.58) the following result can be obtained.

$$\hat{v} = \frac{1}{H} \frac{T}{1+T} \hat{v}_{ref} + \frac{G_{vi}}{1+T} \hat{v}_{IN} - \frac{Z_{out}}{1+T} \hat{i}_{load} \quad (2.60)$$

It is obvious that the disturbances are reduced with a ratio of  $1/(1+T)$ . If the loop gain,  $T(s)$  becomes large enough, then the expression  $1/(1+T)$  yields  $1/T$ . This means that the feedback attenuates the disturbances with the reciprocal of loop gain. Large loop gain means less disturbance effect on the output and is useful for reference input as well. When the loop gain is large enough, the expression on the reference input  $T/(1+T)$  yields 1. This provides that the output will be independent of the changes in the forward path gains.

In most of the cases altering the sensor gain  $H(s)$  or modulator gain  $V_M$  may not be possible for the designer. The overall loop gain compensation is achieved by the compensator transfer function gains. However, increasing transfer function gains may lead to the instability of the system. For that reason a stability analysis is also required in the overall feedback system.

## 2.4.2 Stability

It is a well-known fact that a system containing right half-plane pole exhibits an unstable behavior. Even if the open-loop transfer function of a converter does not include any positive poles, closing the feedback loop may introduce positive poles to the system. That means the stability of a closed-loop system can directly be investigated on the closed-loop transfer function. However, as a practical solution,

there are methods to predict the closed-loop behavior of a system from its open-loop poles. At this point it is critical to know that the system to be controlled is whether a minimum-phase or a non-minimum phase system.

If a system does not contain any right half plane poles or zeros in its open-loop transfer function, this type of system is said to be a minimum-phase system. The stability of a minimum-phase system can be ensured easily by the bode analysis, applying gain and phase margins criteria. For a non-minimum phase system the more general Nyquist Stability Theorem and polar plot should be used for stability analysis.

For the stability of a negative feedback minimum-phase system, the additional phase lag introduced by the loop elements must not exceed  $180^\circ$ . In other words, for stability, positive gain should not be applied to the frequency components in a system that has the phase angle over  $180^\circ$ . These two statements basically constitute the phase and gain margin concept. Phase margin is the additional phase lag to bring the phase angle to  $-180^\circ$  at the frequency where the open-loop gain is equal to 1 (0dB)(gain crossover frequency). Gain margin is the amount of gain below 0dB at the frequency where the phase angle crosses  $-180^\circ$  (phase crossover frequency). The phase margin and gain margin of the system are shown on a bode plot in Figure 2.21.

Positive gain and phase margins ensure the stability of a non-minimum phase system. However, gain and phase margin criteria on the Bode plot are the special cases of the Nyquist Stability Theorem for minimum-phase systems. As previously mentioned the stability analysis of a non-minimum phase system must be carried out on the Nyquist plot which is a more general method. The Nyquist Stability Theorem states that, if there is  $Z$  positive zeros and  $P$  positive poles of an open-loop transfer function of a system, the polar plot of this system must encircle the  $-1+j0$  point  $Z-P$  times in clockwise direction to ensure closed-loop stability [26]. Figure 2.22 (a) and (b) shows a part from the polar plots of a minimum-phase system and a

non-minimum phase system respectively. Gain margin and phase margins are also defined on the polar plot. Figure 2.22 (a) reveals that, the polar plot of the minimum-phase system does not encircle  $-1+j0$  point. In this case, for stability of closed-loop system there must be no right half plane poles of open loop transfer function [26]. Since a minimum-phase system is defined as a system with no positive poles or zeros, that condition is satisfied. Figure 2.22 (a) shows that the phase and gain margins are positive and will remain positive until the polar plot encircles  $-1+j0$  point. Hence, it can be generalized that a minimum phase system is stable if the open-loop transfer function has positive phase and gain margins; and that can be determined on bode plot easily.

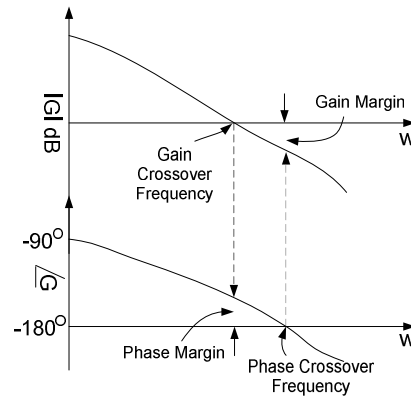


Figure 2.21 Representation of gain and phase margins on the bode plot.

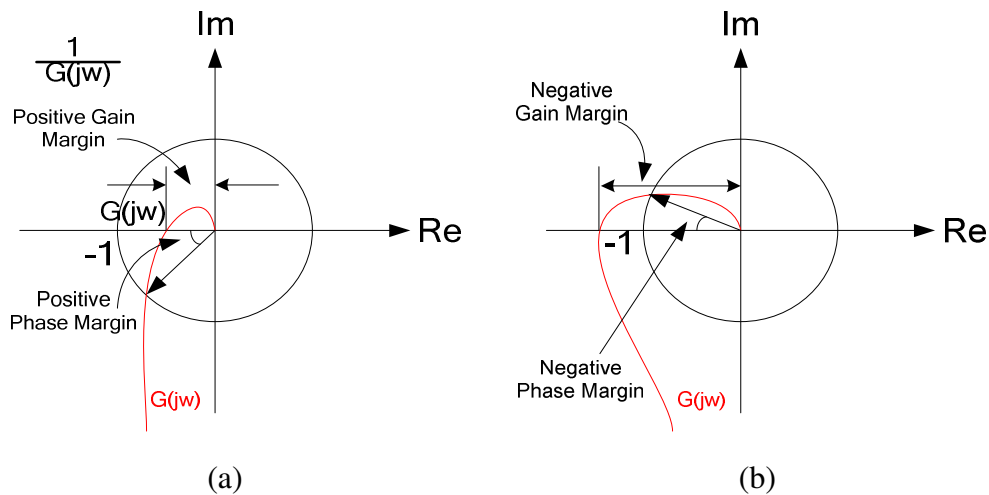


Figure 2.22 Representation of gain and phase margins on polar plot: (a) positive gain and phase margins; (b) negative gain and phase margins.

In Figure 2.22 (b), it is obvious that, polar plot of the non-minimum phase system somewhat encircles  $-1+j0$  point. Since a non-minimum phase system transfer function includes positive poles and/or zeroes, to ensure stability  $-1+j0$  point must be encircled. In this case the gain margin and phase margins may become negative as seen on Figure 2.22 (b). This fact verifies that a non-minimum phase system, despite its gain and phase margins are both negative, can be stable. But this cannot be determined by simple gain and phase margin criteria on the bode plot. That's the main reason why a non-minimum phase system transfer function must be inspected on a polar plot in the aspect of stability.

As a conclusion, if a DC/DC converter has a minimum-phase transfer function, any stability determination for analysis or design purpose can be carried out on the bode plots using gain and phase margin criteria. However, since a stable non-minimum phase system may have negative gain and phase margin, determination on the stability must be carried out on polar plots using the Nyquist Stability Theorem. More information is available in [26] on Nyquist Stability Criterion.

### **2.4.3 Compensator Design Using Direct Duty Ratio Pulse-Width Modulator**

The most common compensator design method is the direct duty ratio control method which is also known as voltage-mode control. In this type of application the output voltage is sensed and fed back to a comparator with the  $H(s)$  sensor gain block to calculate the error. The error signal passes through the error amplifier (compensator) and the control voltage is obtained as an output. The control voltage is fed through the modulator to obtain the gate pulses. In the closed-loop system of Figure 2.20, all these blocks are defined except the  $G_C(s)$  compensator block. The compensation block is designed to meet specifications set by the design goals such as rejection of disturbances, reasonable transient response, and ringing. A general compensation strategy is well-defined in [1] as three statements: The gain at low frequencies should be high to minimize steady-state errors; the crossover frequency



should be high enough for a quick response to the transients and low enough to reject the switching frequency and its harmonics; the phase margin of the system should be in a range of 45°-60° to prevent excess overshoot and ringing. The proper compensation type and network can be chosen to meet these specifications.

### 2.4.3.1 Compensator Design in Theory

The compensator types can be divided into three categories: A lead compensator, a lag compensator and a lead-lag compensator.

A lead compensator is used to improve phase margin [13]. A low frequency zero is added to lead the phase near crossover frequency. The transfer function of the lead compensator is given as

$$G_C(s) = G_{c0} \frac{(1 + \frac{s}{w_z})}{(1 + \frac{s}{w_p})} \quad (2.61)$$

The bode diagrams and the transfer function of the lead compensator is given in Figure 2.23.

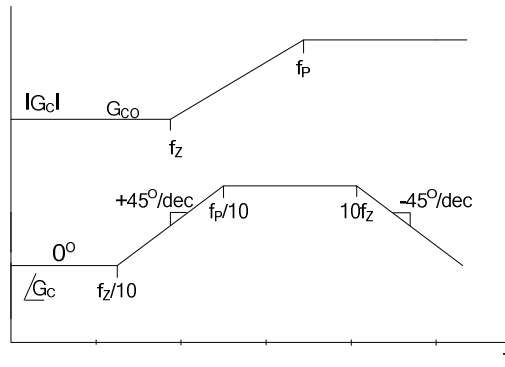


Figure 2.23 Gain and phase plots of a lead compensator transfer function.

The frequency at which the maximum phase lead occurs is the geometric mean of the pole and zero frequency.

$$f_{\phi \max} = \sqrt{f_p f_z} \quad (2.62)$$

The relation between the pole-zero frequencies and introduced phase lead is given as

$$\frac{f_p}{f_z} = \frac{1 + \sin \phi}{1 - \sin \phi} \quad (2.63)$$

The DC gain of the compensator  $G_{C0}$  can be chosen in a way to change the crossover frequency to the desired value or to keep it constant in the existing value. A lead compensator design can be initiated by choosing the desired crossover frequency and desired phase lead at that frequency. By using (2.62) and (2.63) the pole and zero frequencies can be determined. And the DC gain can be selected to bring the chosen frequency to the 0dB crossover level. However a lead compensator is generally used together with a lag compensator rather than to be used as a single compensator.

A lag compensator bode diagram is shown in Figure 2.24. It is clear on the bode diagram that the lag compensator has a pole at zero frequency which introduces a high low-frequency gain to the system. Lag compensator is generally used to solve the steady-state error problem. One drawback of this compensator is a  $90^\circ$  phase lag introduced and this problem is solved by placing a zero at about one decade below the expected crossover frequency to improve the phase angle. The transfer function of this compensator is given as

$$G_C(s) = G_{C0} \left(1 + \frac{w_z}{s}\right) \quad (2.64)$$

Transfer function reveals that the lag compensator is a proportional-integral (PI) controller. The last type of compensator is a combination of the previous two compensator types called as lead-lag compensator. The compensator transfer function is given in equation (2.65). The bode diagram for the transfer function is shown in Figure 2.25.

$$G_C(s) = G_{C0} \frac{(1 + \frac{w_{Z1}}{s})(1 + \frac{s}{w_{Z2}})}{(1 + \frac{s}{w_{P1}})(1 + \frac{s}{w_{P2}})} \quad (2.65)$$

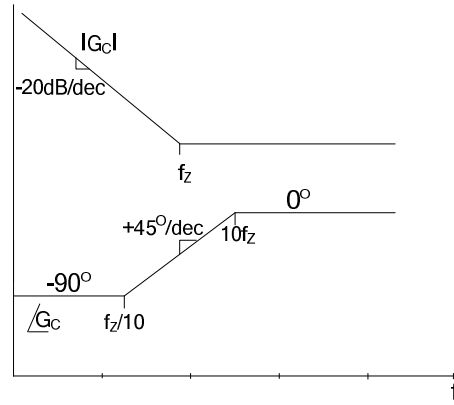


Figure 2.24 Gain and phase plots of a lag compensator transfer function.

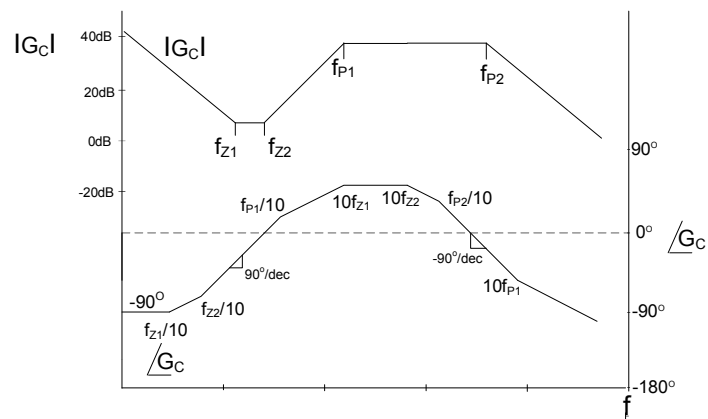


Figure 2.25 Gain and phase plots of a lead-lag compensator.

The lag-lead compensator combines the advantages of the lead and lag compensator. The pole at zero frequency regulates the steady-state error as in the lag compensator example. The first zero is placed to improve the phase angle from  $-90^\circ$  to  $0^\circ$ . To improve the phase margin, another zero is introduced in the system which is close to the frequency of the first zero. The two poles are placed after the crossover frequency to provide the required gain margin and the required attenuation at the switching frequency. In some cases two zeroes and two high frequency poles may be placed to same frequencies separately. Then the compensator transfer function becomes

$$G_c(s) = G_{c0} \frac{(1 + \frac{s}{w_z})^2}{s(1 + \frac{s}{w_p})^2} \quad (2.66)$$

The bode plot of this transfer function will highly resemble the plot of Figure 2.25. The flat portions of the gain characteristic will disappear between the two zero frequencies and two pole frequencies.

#### 2.4.3.2 Compensator Design in Practice

In the theoretical part, the compensators have been classified according to their effects on phase angle and the theoretical idea of design is introduced. These conceptual designs can be used in simulations but the realization as an electrical circuit may be confusing. Hence in this part, three types of compensators which are implemented via operational amplifiers are will be introduced. The philosophy gained in the theoretical part is valid in this part but the representation will be more practical.

The circuit shown in Figure 2.26 is called the Type-I compensator. The compensator is a single pole compensator and has a dominant behavior of an

integral controller. The compensator DC gain is  $R_2/R_1$  and the pole frequency is  $1/R_2C$ . This type of compensation has high low-frequency gain hence is useful for compensating steady state-error. However, since the single pole structure reduces the gain crossover frequency, this compensator may exhibit a slow transient response.

$$G_C(s) = -\frac{R_2}{R_1} \frac{1}{1+sR_2C} \quad (2.67)$$

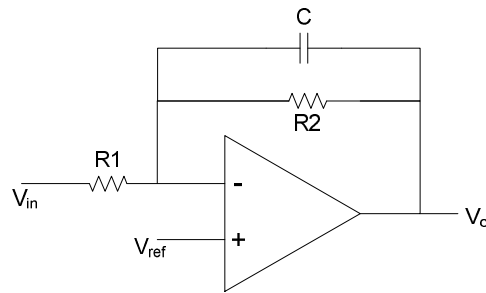


Figure 2.26 Circuit diagram of Type-I compensator.

Type-II compensator circuit and the bode plot are illustrated in Figure 2.27. As the bode plot implies, Type-II compensator is a 2-pole 1-zero system. One of the poles is at zero frequency and improves the low-frequency gain. The frequencies of pole zero pair can be chosen as in the lead compensator design by considering the frequency at which the maximum phase boost is intended. While choosing the pole frequency, the high frequency attenuation should be considered as well. The transfer function of Type-II network is given as

$$G_C(s) = -\frac{1}{R_1C_1} \frac{s + \frac{1}{R_2C_2}}{s(s + \frac{C_1 + C_2}{R_2C_1C_2})} \quad (2.68)$$

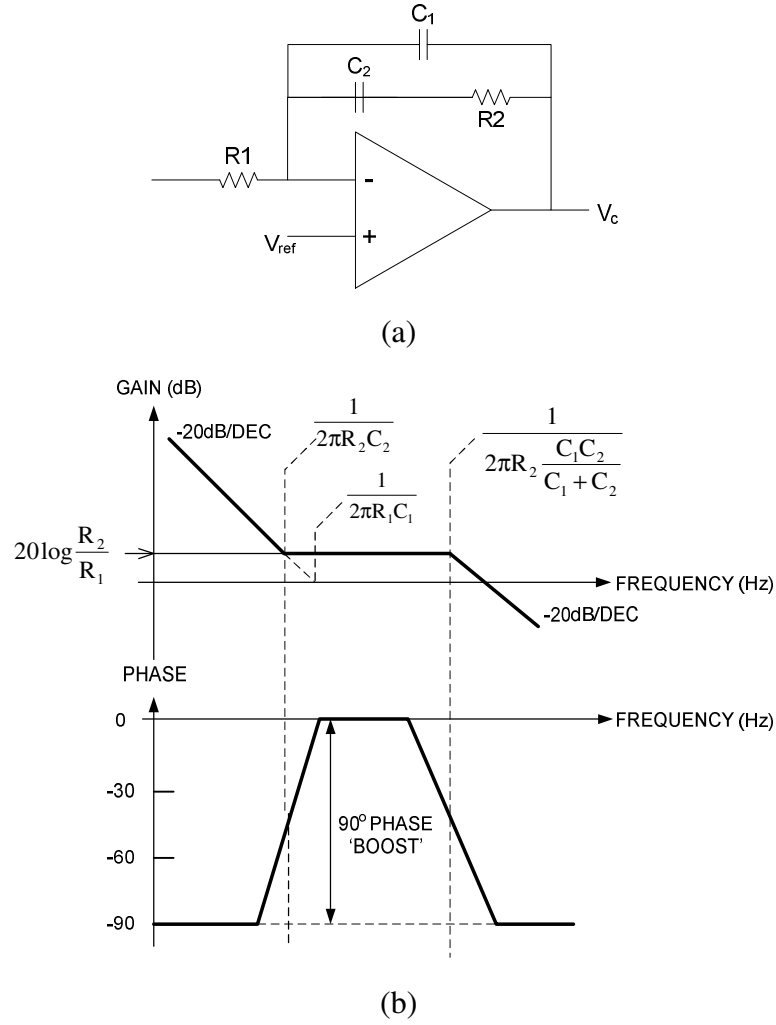


Figure 2.27 Type-II compensator: (a) circuit diagram; (b) bode plot.

The last general type of compensator is the Type-III compensator with 3 poles and 2 zeroes. Type-II system does not have a phase-leading property. It can only boost the phase up to  $0^\circ$  from  $-90^\circ$  which is caused by its zero-frequency pole. However, Type-III network can provide  $180^\circ$  phase boost theoretically starting from  $-90^\circ$  up to  $90^\circ$ . The circuit diagram and bode plot are given in Figure 2.28. The transfer function of a Type-III network is given as

$$G_C(s) = -\frac{R_1 + R_3}{R_1 R_3 C_1} \frac{(s + \frac{1}{R_2 C_2})(s + \frac{1}{(R_1 + R_3)C_3})}{s(s + \frac{C_1 + C_2}{R_2 C_1 C_2})(s + \frac{1}{R_3 C_3})} \quad (2.69)$$

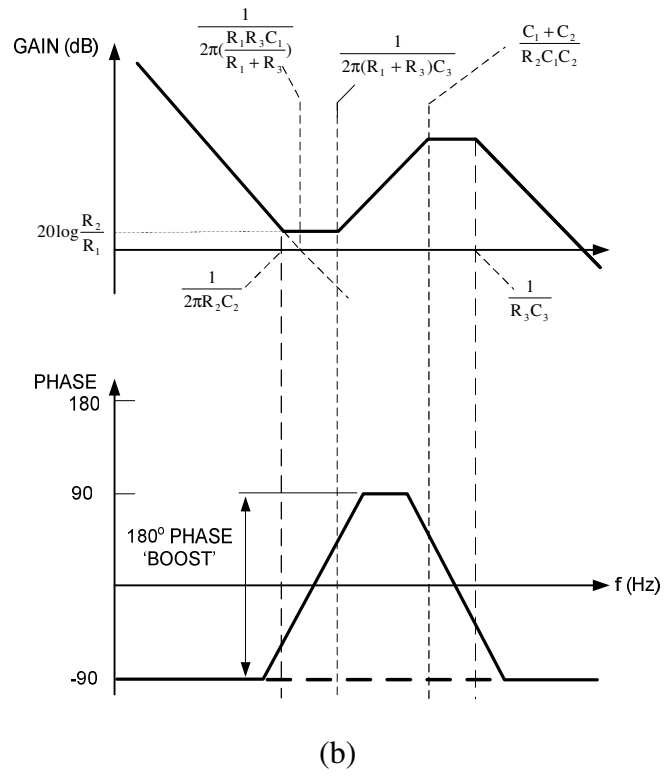
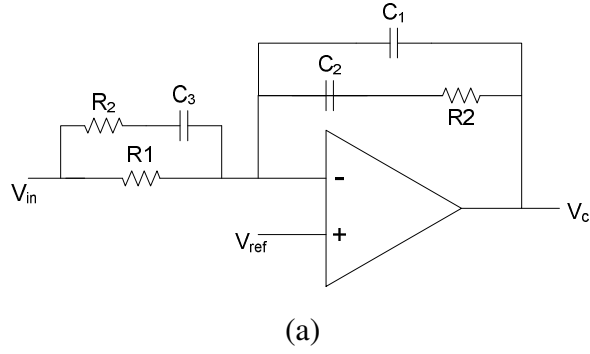


Figure 2.28 Type-III compensator: (a) circuit diagram; (b) bode plot.

Type-III transfer function resembles the lag-lead compensator introduced in the theoretical part. In all types of compensators a starting point is required to evaluate the component values. Generally the  $R_1$  resistor is taken as a value and starting this point other components are calculated according to the chosen pole and zero frequencies and/or the chosen compensator gain values. More information can be found on calculating the component values in [1], [27], and [28].

#### 2.4.4 Voltage Feed-Forward Control

In the direct duty ratio PWM control, the duty cycle is obtained by comparing the control voltage by a modulating ramp waveform which has constant amplitude. As previously mentioned the control voltage is obtained by amplifying the error signal which is the difference between the sensed output voltage and the reference input. Hence, in order to update the duty cycle in any input voltage change, the system has to wait until the input voltage change, alters the output. In that condition the response time is generally limited by the second order low-pass filter time constant.

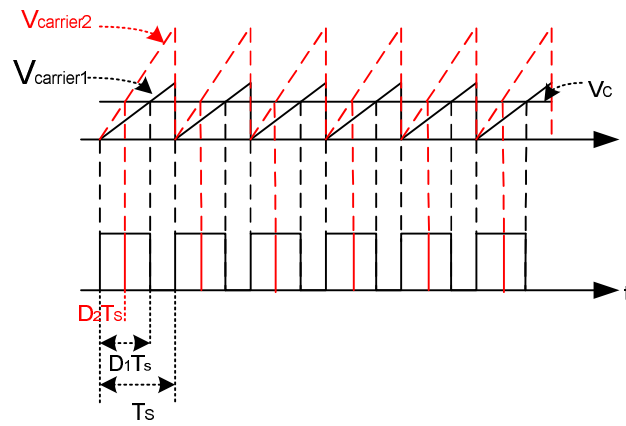


Figure 2.29 Voltage feed-forward control waveforms.



In voltage feed-forward control method, input voltage is feed to the PWM controller IC. The amplitude of the ramp waveform is altered as directly proportional to the input voltage level. Figure 2.29 illustrates the condition. When the input voltage level increases, the amplitude of the waveform is increased as well, which causes the duty cycle to decrease or vice versa. This control method provides fast responses to the input voltage changes, since the correction signal is not produced by the compensator which senses the changes of output and hence, is limited to the low-pass filter bandwidth.

#### **2.4.5 Current Mode Control**

Voltage-mode control which is referred as direct duty ratio control is a very common control method, since the sources on single-loop compensator design rules are wide and application of single-loop design is quite easy. However, in some cases voltage feedback may not be adequate alone to provide the desired system performance. Especially converters having non-minimum phase transfer functions require an inner current loop. This type of control is referred as current-mode control.

In current mode control, instead of controlling the duty cycle directly, the control voltage controls the average or peak values of the inductor current depending on the control strategy which are the two main types of inductor current control strategy: Peak Current Control and Average Current Control. The peak current control method will be discussed in this section.

In the peak current control strategy, the inductor current is sensed and the inductor current ramp is used to create the gate pulses. The outer voltage loop provides the control voltage from the output of compensator which is compared with the inductor current ramp. When the current reaches the pre-determined peak value, the switch is turned-off. Different control strategies can be applied to the system to turn

the switch off. Constant frequency control is possible and offers simplicity in the magnetic design aspect. In this strategy, the switch is turned-off when the inductor current ramp intersects the control voltage and the switch is turned on by a constant frequency clock. Another strategy is variable frequency with constant off time. The switch turn off strategy is the same with the constant frequency method. However, in this application the switch off time is constant which causes the variable frequency structure. The circuit diagram of the peak current controlled buck-boost converter is shown in.

The constant frequency peak current controller has a significant problem inherent. The controller becomes unstable whenever the duty cycle becomes greater than 0.5. Whenever the duty cycle exceeds 0.5, the system exhibits so-called sub-harmonic oscillations [29]. These oscillations can be damped using an external ramp waveform. The method is known as slope compensation. The slope of the external ramp waveform determines the maximum duty cycle and by selecting a proper slope, the current mode controller can be stabilized in the whole  $0 < D < 1$  interval. The slope compensation process is shown in Figure 2.31. Detailed explanation on slope compensation can be found in [13].

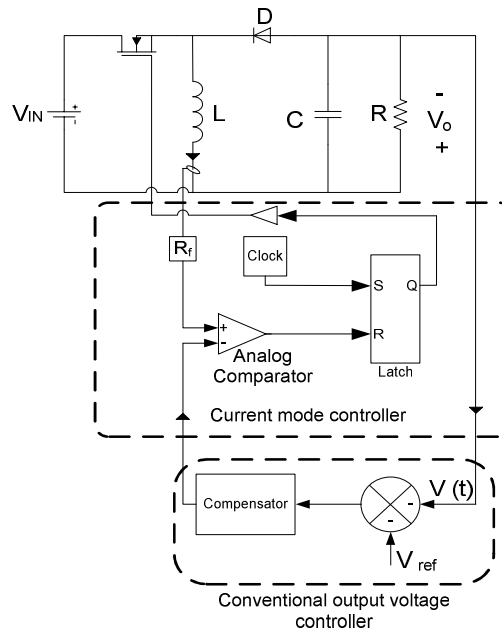


Figure 2.30 Current mode control circuitry of a buck- boost controller.

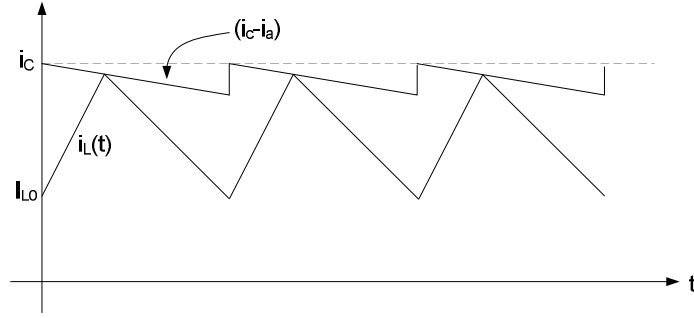


Figure 2.31 Slope compensation of peak current mode control.

After introducing and stabilizing the inner current loop, the circuit requires the outer voltage loop which will provide the reference input for the current controller. In order to design the outer loop compensator, the small-signal AC model of the converter with the current controller is needed. A simple model for the current controller will be introduced here to reveal the effect of current controller on the converter system. However, further modeling issues on converters with current controller are beyond the scope of the thesis. The small signal model equations of the buck-boost converter are given below in both time domain and s-domain.

$$L \frac{d\hat{i}_L(t)}{dt} = D \hat{v}_{IN}(t) + (1-D) \hat{v}_O(t) + (V_{IN} - V_O) \hat{d}(t) \quad (2.70)$$

$$C \frac{d\hat{v}_O(t)}{dt} = -(1-D) \hat{i}_L(t) - \frac{\hat{v}_O(t)}{R} + I_L \hat{d}(t) \quad (2.71)$$

$$\hat{i}(t) = D \hat{i}_L(t) + I_L \hat{d}(t) \quad (2.72)$$

These time domain expressions can be obtained using state-space averaging method. When the laplace transformation is applied to the equations the result is

$$L s \hat{i}_L(s) = D \hat{v}_{IN}(s) + (1-D) \hat{v}_O(s) + (V_{IN} - V_O) \hat{d}(s) \quad (2.73)$$

$$C s \hat{v}_O(s) = -(1-D) \hat{i}_L(s) - \frac{\hat{v}_O(s)}{R} + I_L \hat{d}(s) \quad (2.74)$$

$$\hat{i}(s) = D\hat{i}_L(s) + I_L \hat{d}(s) \quad (2.75)$$

The assumption of this modeling process is based on the small inductor current ripple. For small current ripple, the inductor current ( $i_L(t)$ ) can be assumed to be equal to the reference current of the controller ( $i_C(t)$ ) as illustrated in Figure 2.32. Therefore, under this assumption it can be claimed that

$$i_L(s) \approx i_C(s) \quad (2.76)$$

Then, the substitution can be applied to the equation of (2.73)

$$Ls\hat{i}_C(s) = D\hat{v}_{IN}(s) + (1-D)\hat{v}_O(s) + (V_{IN} - V_O)\hat{d}(s) \quad (2.77)$$

the solution yields

$$\hat{d}(s) = \frac{Ls\hat{i}_C(s) + D\hat{v}_{IN}(s) + (1-D)\hat{v}_O(s)}{(V_{IN} - V_O)} \quad (2.78)$$

This equation reveals the variation of duty cycle according to the variations in controller reference current, input voltage and output voltage. By substituting (2.78) in (2.74) and (2.75) one can get the following two terminal equations.

$$Cs\hat{v}_O(s) = \left\{ s \frac{LD}{(1-D)R} - (1-D) \right\} \hat{i}_C(s) - \left\{ \frac{D}{R} + \frac{1}{R} \right\} \hat{v}_O(s) + \left\{ \frac{D^2}{(1-D)R} \right\} \hat{v}_{IN}(s) \quad (2.79)$$

$$\hat{i}(s) = \left\{ s \frac{LD}{(1-D)R} + D \right\} \hat{i}_C(s) - \frac{D}{R} \hat{v}_O(s) - \left\{ \frac{D^2}{(1-D)R} \right\} \hat{v}_{IN}(s) \quad (2.80)$$

Two-port equivalent circuit of non-isolated converters is shown in Figure 2.32. The parameters for the converters are given in Table 2.3.

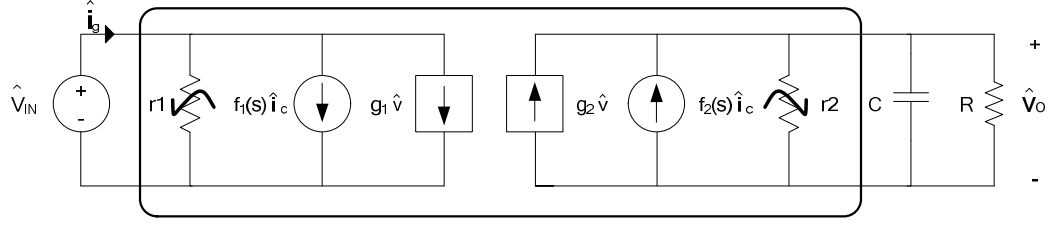


Figure 2.32 Two-port equivalent circuit of basic non-isolated converters.

The control-to-output, line-to-output transfer functions and the output impedance of the system can be found by setting the required variations to zero.

$$G_{vc}(s) = \frac{\hat{v}_o(s)}{\hat{i}_c(s)} = f_2(r_2 // R // \frac{1}{sC}) = -\left(R \frac{1-D}{1+D}\right) \frac{(1-s \frac{DL}{(1-D)^2 R})}{(1+s \frac{RC}{1+D})} \quad (2.81)$$

$$G_{vi}(s) = \frac{\hat{v}_o(s)}{\hat{v}_{IN}(s)} = g_2(r_2 // R // \frac{1}{sC}) = -\left(\frac{D^2}{1-D^2}\right) \frac{1}{(1+s \frac{RC}{1+D})} \quad (2.82)$$

$$Z_{out}(s) = r_2 // R // \frac{1}{sC} = \frac{R}{1+D} \frac{1}{(1+s \frac{RC}{1+D})} \quad (2.83)$$

With the simple model approximation, the current controller reduced the order of converter transfer function by 1. While the open-loop transfer function exhibits a quadratic pole response, the converter with current controller has only one pole. This simplifies the voltage loop compensator design of the system. However, the current controller has no effect on the frequency of right half-plane zero hence the compensator design still has to be considered according to the positive zero. However, more accurate models exist in literature and are introduced in [13], [30], [31].

The current mode control issue is the last concept to be introduced in chapter 2. The DC operating characteristics of the DC/DC converters have been derived by using the inductor volt-second balance concept. Before deriving the converter transfer

functions, the two basic AC modeling approaches have been introduced. Using these modeling methods the converter transfer functions have been derived. The application of the classical control theory has led the way to the control strategies such as voltage mode and current mode control at the end of the chapter. The theoretical part forms the conceptual design part of any DC/DC converter however the physical implementation of the circuit on a PCB requires some additional experience. The next chapter will provide some information about these practical issues as component selection and PCB layout.

## **CHAPTER 3**

### **SWITCH-MODE CONVERTER HARDWARE DESIGN**

#### **3.1 Introduction**

In the previous section the theoretical basis of the switch-mode power conversion was established. The basic approaches for analyzing the converter topologies both in DC and AC conditions were introduced. The volt-seconds and ampere-seconds concepts for the DC operation and the averaging methods for small-signal AC linearization have been mentioned completing the section with the control theory. Although the ESR of the capacitance has been discussed with the effects on the converter transfer function, most of these analyses were based on an ideal device assumption. However, in the case of a hardware implementation of any DC/DC converter, the parasitic effects introduced by the real components may not be clearly understood by an inexperienced designer. Hence, this chapter is allocated to provide a simple guide for the hardware design considerations.

The basics about the switches used in SMPS applications, the capacitor types, the design of the magnetic components, and the snubbers will be covered in this chapter. Beside the topological components and their requirements, the PCB design and the parasitics introduced by the PCB will also be introduced in a section to complete the chapter.

### **3.2 Switch Basics and Switch Selection Criteria in SMPS Applications**

In each topology introduced in chapter 2, at least one controlled (MOSFET) and one uncontrolled switches (diode) are used. These switches commutate the current among themselves and the structures of these devices affect the overall converter unit but more significantly the switching performance of the circuit. The switching characteristics and gate drive requirements of the MOSFETs; switching problems caused by the diodes will be explained and the basic philosophy to select the switches suitable for SMPS applications will become clearer at the end of switch section.

In the hardware implementation of the thesis, MOSFET is used as the controlled switch. Therefore, along with the power diode which is an uncontrolled switch, the power MOSFET will be introduced during the section. An IGBT can be used as the controlled switch as well, which has a pin-to-pin compatibility in many cases with a power MOSFET. For that reason IGBT is also included in specific points.

#### **3.2.1 The Uncontrolled Switch: The Power Diode**

The diodes used in the power applications are different from the standard low power diodes in structure. The well-known p-n junction of the standard diodes are modified by doping an additional  $n^-$  layer between the heavily doped p and n layers to make them suitable for the high voltage, high power applications.

The diode characteristic appears as three different regions: The cut-off region, forward conducting region and reverse conducting region. The diode is in the cut-off region until the anode-cathode voltage reaches the forward voltage drop  $V_F$  level. In the forward conducting region, the diode behaves linearly and the conduction loss is determined by the on resistance beside the forward voltage drop. The reverse conducting region which results with the complete deterioration of the



diode is the unwanted region for normal operation. Hence, the maximum reverse voltage is one of the diode selection criteria. In the aspect of conduction losses, the forward voltage drop and on resistance are the critical selection criteria.

One of the most important phenomenons of the diode is the reverse recovery process. Since most of the diodes are minority carrier devices, when the turn-off occurs these minority carriers should be cleared away from the junction to complete the turn off process. This causes a reverse current flow through the diode at the end of the turn off process and takes additional time to complete turn off of device. The standard diodes which are also referred as general purpose diodes have too long a reverse recovery time for a fast switching SMPS application. An example of a reverse recovery current is shown in Figure 3.1.

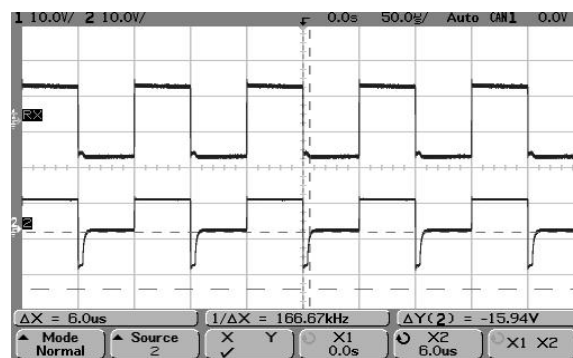


Figure 3.1 The reverse recovery current of a diode (10V/div, 10V/div, 50 $\mu$ s/div).

The measurement in this experiment does not aim to characterize the high current behavior of any device. The measurement is taken at the signal level of 10 kHz to demonstrate the reverse recovery behavior. The first channel (upper signal) shows the applied voltage. The diode recovery current (lower signal) is obtained across resistor terminals connected in series with the diode. As seen in the Figure 3.1 the reverse recovery time is at microseconds level which is enough for a line frequency application but not for a high-speed application.

### 3.2.2 The Controlled Switch: The Power MOSFET

Power MOSFETs with appreciable on-state current-carrying capability and off-state blocking voltage suitable for power electronic applications have been available since the early 1980s [1]. Replacing the older technology BJTs, they are the most popular switches for low power and fast-switching applications.

First of all, a MOSFET is a voltage-driven majority carrier device unlike the BJT which is a current-driven minority carrier device. The excess carrier charge removal requirement of a BJT is the reason that a BJT cannot be switched as fast as a MOSFET. Another advantage of the MOSFETs is its positive temperature coefficient structure. This structure enables the paralleling of MOSFETs which is not possible for BJTs which have negative temperature coefficient on state resistance.

The main difference between the power MOSFET and the MOSFETs used in small signal electronic (analog or digital) circuits is its  $n^-$  layer as in the power diodes which are lightly doped to increase the breakdown voltage and bring the MOSFETs to a suitable structure for power applications. The breakdown voltage, often referred as maximum drain-to-source voltage or drain-to-source breakdown voltage in datasheets, is the maximum voltage that a MOSFET can hold in its off-state. In the on state, the voltage drop rating of the MOSFET is generally standardized by the on-resistance generally referred as “static drain-to-source on-resistance” in datasheets. These factors can be counted as the two important factors in selecting a power MOSFET. The breakdown voltage determines the maximum voltage that a MOSFET should be subjected to. Since the on-resistance is the indicator of the conduction losses of the MOSFET, together with the switching losses, it determines the total power dissipation of a MOSFET and hence the heatsink requirements. More information can be found on these and other MOSFET parameters in [32].

Significant care should be given to the device capacitances of a MOSFET. These capacitances arise because of the isolated gate structure of the MOSFET and these capacitances determines the switching behavior and gate drive requirements of a switching MOSFET-diode pair in a power electronic circuit.

### 3.2.3 The Switching Characteristics of a Power MOSFET- Diode Pair

All DC/DC power converters have a MOSFET/IGBT-diode inductive switching pair and understanding the dynamics of this switch network is critical to proper design and obtaining a good switching performance. The switching performance of the switch network is generally determined by the device parasitic capacitances and parasitic inductances. Consider the switching cell of Figure 3.2.(a). The circuit includes an inductor at the output side. Removing the inductor, a resistive switching network can be obtained. In this condition there will be no element that forces the circuit for the continuity of the current and that provides a less problematic switching action. The existence of the inductor forces the current in one direction and causes the current commutation event among the switches in each switching period which appears as a device stress problem. The dynamic switching waveform is shown in Figure 3.2.(b).

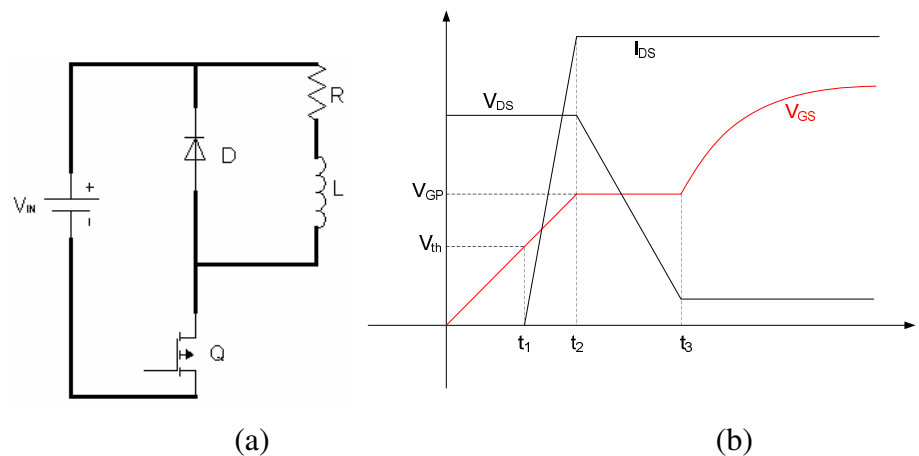


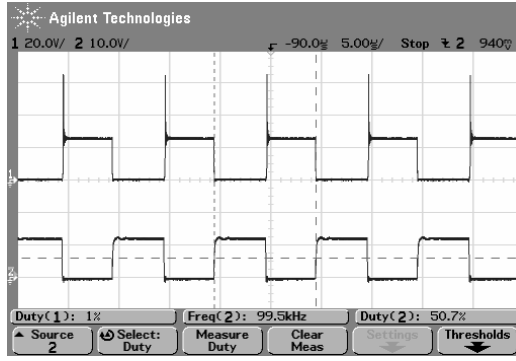
Figure 3.2 The inductive switching concept: (a) basic circuit diagram; (b) the switching waveforms.

Before the switching instant, the MOSFET has been holding the full input voltage as drain-source voltage  $V_{DS}$ . When the voltage is applied to the gate, the gate-source capacitance  $C_{GS}$  starts to charge and gate-source voltage  $V_{GS}$  increases almost linearly. The drain current starts to rise when  $V_{GS}$  reaches to the MOSFET threshold voltage while  $V_{DS}$  is decreasing  $V_{GS}$  remains constant and this interval is called as Miller Plateau arising from the Miller capacitance effect. This plateau voltage  $V_{GP}$  is the minimum required gate-source voltage to accomplish switching at that specific condition [33]. When  $V_{DS}$  reaches the  $I_{DS} \times R_{on}$  (means current commutation is completed) level,  $V_{GS}$  starts to increase again until the applied gate supply voltage is reached. The device capacitances are defined in the datasheets of the switches as input ( $C_{iss}$ ), output ( $C_{oss}$ ), and reverse transfer ( $C_{rss}$ ) capacitors and somewhat can be related to the terminal capacitances. However, designing a gate drive using only the capacitance values and RC time constant calculations may not provide the adequate switching performance since the gate-drain capacitance  $C_{GD}$  (also known as the Miller capacitance) is the non-linear function of voltage [33]. Instead of the capacitances, the total gate charge requirements should be taken into consideration and the required current should be calculated to achieve the desired switching time using the total gate charge data. Gate voltage and required gate current are no more unknown parameters. Using these data an approximate gate resistance  $R_G$  can be chosen. High  $R_G$  value results in low gate current and more time to supply required gate charge. Low  $R_G$  value may cause oscillations at the gate voltage because of the parasitic inductances of the circuit. Now the real switching waveforms and the effects of gate resistance will be presented using the device characterization board.

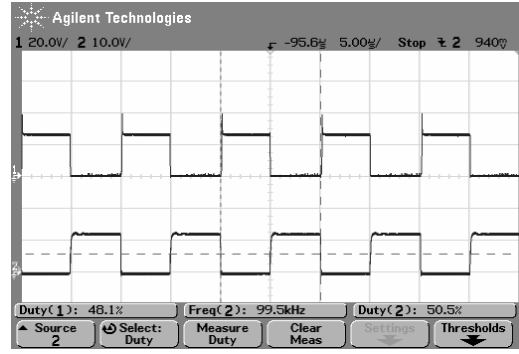
The waveforms of Figure 3.3 to Figure 3.5 are recorded for 24V input with 220 $\mu$ H series inductance to the load resistance. All the upper waveforms are the drain-to-source voltages, and the lower waveforms are gate-to-source voltages. It is seen on Figure 3.3 (a) and (b) that when the load resistance is increased the amplitude of the voltage peak decreases at the switch turn-off transient. This proves that the peak at the turn-off instant of the MOSFET is due to load and PCB impedances. The

characteristic impedance generally appears as an inductive behavior which causes  $Ldi/dt$  spikes. Another important phenomenon of the switching cell is the Miller plateau. Since the gate resistance is zero (for the demonstration shown in Figure 3.3), the switch turns on rapidly and the Miller plateau is observed for a very short time period. Finally, at the switch turn-off in Figure 3.3 (d), some high frequency oscillations are observed. This is caused by the, MOSFET output capacitor and the PCB parasitic inductance again. Thinking the oscillation source as the load inductor will not be a true approach because the Figure 3.4.(d) shows that the oscillation frequency is about 25 MHz. A 220 $\mu$ H inductor needs a capacitance value lower than picofarad levels to cause a 25 MHz oscillation which is generally not the capacitance value of a typical MOSFET. More specifically an IRF540 MOSFET is used and it has 870pF input, 125 pF output capacitance. Assuming a few tens of nanoHenries of PCB trace inductance results in a few hundreds of picofarads of capacitance. That is a reasonable value for the given IRF540 MOSFET capacitance.

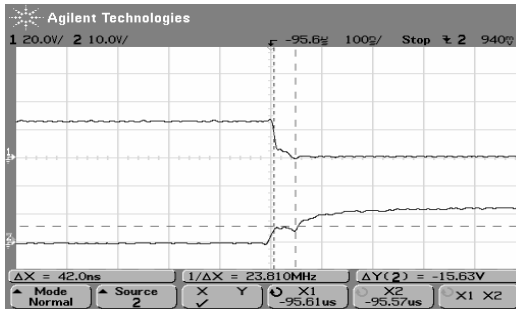
Now, Figure 3.4 (a) and (b) illustrates the general view of the MOSFET switching waveforms for 39 $\Omega$  and 100 $\Omega$  gate resistances respectively with 10 $\Omega$   $R_{LOAD}$ . Figure 3.3, 3.4 (a), and 3.4 (b) shows that, as the gate resistance increases (gate current decreases), the switching time increases since it takes more and more time for the gate drive circuit to supply the required gate charge for switch turn on. The increased gate resistance causes a slower switching action and shows the Miller plateau. Figure 3.5 shows the turn-on and turn-off times for the 100 $\Omega$  gate resistance case. It is clearly seen on the figure that the Miller plateau (which eventually corresponds to drain-to source capacitance charging or discharging time) is increased to 230ns level from 42ns which is observed in Figure 3.3 when no gate resistance is used.



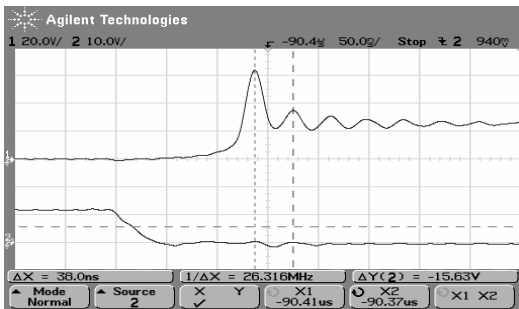
(a)



(b)

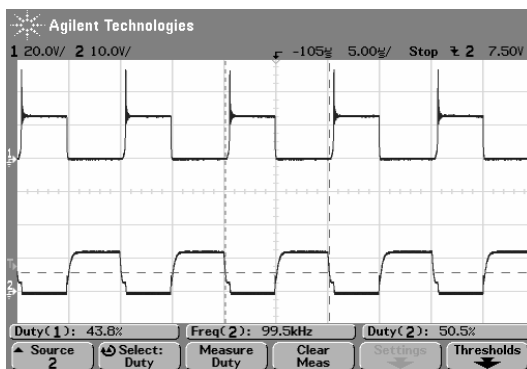


(c)

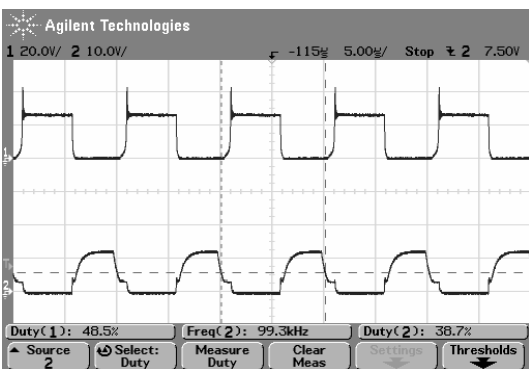


(d)

Figure 3.3. MOSFET drain-source voltage (top, 20V/div) and gate-source voltage (bottom, 10V/div) with  $R_{gate}=0$ : (a) macroscopic view for  $R_{LOAD}=10\Omega$  (5 $\mu$ s/div); (b) macroscopic view for  $R_{LOAD}=40\Omega$  (5 $\mu$ s/div); (c) detailed view during MOSFET turn-on for  $R_{LOAD}=10\Omega$  (100ns/div); (d) detailed view during MOSFET turn-off for  $R_{LOAD}=10\Omega$  (50ns/div).



(a)



(b)

Figure 3.4 MOSFET drain-source voltage (top, 20V/div) and gate-source voltage (bottom, 10V/div) for  $R_{LOAD}=10\Omega$  (5 $\mu$ s/div): (a)  $R_{gate}=39\Omega$ ; (b)  $R_{gate}=100\Omega$ .

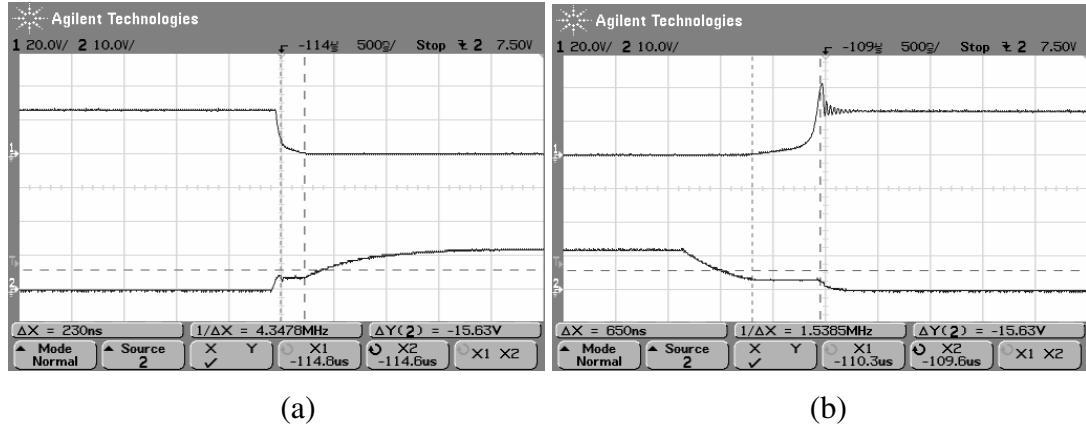


Figure 3.5 MOSFET drain-source voltage (top, 20V/div) and gate-source voltage (bottom, 10V/div) for  $R_{LOAD}=10\Omega$ ,  $R_{gate}=100\Omega$  (500ns/div for both waveforms):

(a) during MOSFET turn-on; (b) during MOSFET turn-off.

Waveforms obtained from device characterization board showed the real dynamics of the MOSFET voltages and currents. The effect of gate resistance and the simple calculation to choose the resistance value is discussed. Detailed information can be found in [32]-[34]. Now, a few points about the gate drive circuit design will be discussed.

A practical method for driving a MOSFET gate is the direct drive from the PWM controller output which is shown in Figure 3.6. The method is a practical and a quick solution however, brings some problems along. To drive a switch with this method, the circuit layout should be considered carefully because the stray inductances on the ground return path may cause ringing in the gate drive [35]. Another drawback of this circuit is the inadequate drive current capability of PWM controllers. Therefore, sometimes an additional gate drive IC is necessary to provide higher current. Despite the drawbacks stated this method can be a good solution if the MOSFET is in the low-side (MOSFET source grounded) and not switching high currents.

If the MOSFET is in the high-side of the circuit or in other words if the source terminal is floating, the gate drive circuitry requires isolation. The first method to isolate the gate drive circuit from the ground is to use an optocoupler. Most optocouplers require a separate supply grounded to the source on the receiving end of the optical link and a booster stage at the output [36]. Another solution is using a pulse transformer to drive the MOSFET in the high side. However, they can provide a limited duty cycle between 0.30-0.65. Choosing a p-channel MOSFET instead of an n-channel can bring the simplicity for a high-side driver. Since a p-channel MOSFET requires negative gate-source voltage to turn on, the simple inverted direct PWM controller drive method can be used as in the low side n-channel case, if the voltage rating is appropriate. However in a p-channel MOSFET the majority carriers are holes and since the holes have lower mobility than the electrons the on-resistance is higher than any n-channel MOSFET having same device ratings [37]. They also have higher device capacitances and threshold voltages. Hence an n-channel MOSFET has more advantages in aspect of both switching and conduction losses.

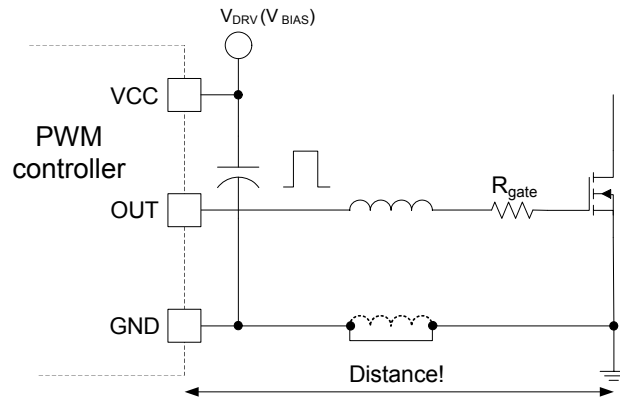


Figure 3.6 Direct gate driving from the PWM output.

The last method proposed for the high side driver that implements an n-channel MOSFET is to use an isolated DC/DC converter chip by a high side gate driver IC.



A PWM controller or a timer can create the pulses and the gate driver IC receives the pulses as input. Some commercial gate driver ICs have external pins to detect floating voltage level as the offset level and has an additional input for the floating voltage supply. A DC/DC converter is utilized to apply an isolated DC to the floating input supply. The circuit diagram is shown on Figure 3.7.

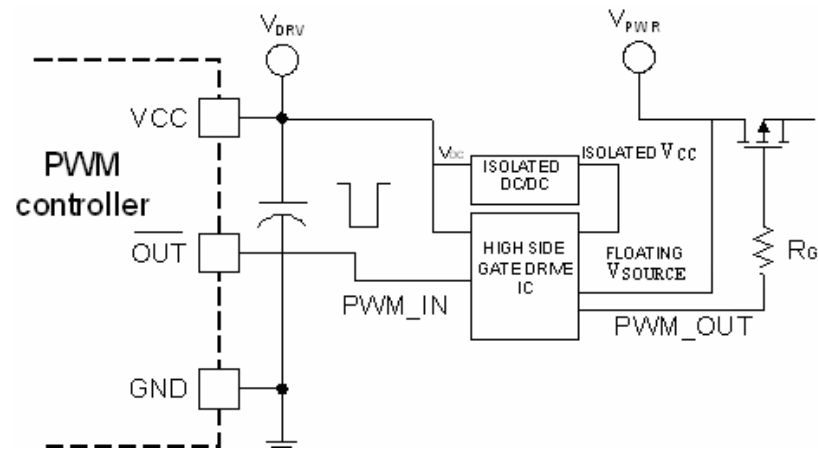


Figure 3.7 High side gate drive circuit using isolated DC/DC converter.

The high-side gate driver accepts the gate floating voltage as the base voltage and adds the output voltage of DC/DC converter on to the floating voltage. This type of high-side drivers can also be used as the low side drivers. Additional information on gate drive circuits can be found on [35]-[38].

Up to this point, the diode and the MOSFET is chosen and the requirements and types of the drive circuits are discussed. The passive components such as capacitors, inductors, and transformers will be discussed in the following section.

### 3.3 Passive Components of an SMPS

Passive component selection and/or design is one of the most important topics of SMPS design. Capacitor selection is one of the most confusing process because there are many different types of capacitors available. Although the inductor and transformer design considerations are quite straightforward processes, the effects of them on the efficiency, noise, and EMI can be difficult to comprehend because of the abstract structure of these phenomena. Hence, this section is allocated for the basics of the passive components.

#### 3.3.1 Capacitor Basics

Capacitors are devices formed by two conducting materials separated by a non-conducting medium. Therefore, the capacitors are classified according to the conducting and non-conducting materials used in their manufacturing or directly by the manufacturing process' itself.

The capacitance of a capacitor depends on the area and the distance of the conductors with the electrical permittivity (dielectric constant) of the insulator material as given below.

$$C = \epsilon \frac{A}{d} \quad (3.1)$$

As (3.1) states, for a larger capacitance, larger conductor surface or smaller distance is required. However, these factors do not bring an absolute degree of freedom to the capacitor design because of the physical limitations of manufacturing process. Therefore, a large variety of dielectric materials are used in capacitor production such as, glass, paper, plastic, mica, and ceramic. These capacitors are named with their dielectric materials. In [9], capacitors are divided into three major types: Simple dielectric capacitors, electrolytic capacitors, and double-layer capacitors.

Simple dielectric capacitors are the most basic type, formed directly with parallel plates and an insulator [9]. Electrolytic capacitors use a metal usually aluminum or tantalum as an electrode and the electrode is oxidized to obtain the non-conducting medium. The second electrode can be either a solid or liquid electrolyte. These are one of the most popular types of capacitors. Double-layer capacitors are newer technology capacitors and can provide large capacitance in small volumes hence sometimes referred as supercapacitors. From these classes and types, electrolytic, ceramic and metal-film capacitors are popular in SMPS applications.

While choosing a capacitor in an SMPS application, the first thing to determine is the function of the capacitor in the circuit. The question “What is the duty of the capacitor in the circuit?” is crucial. Will it provide energy storage for low frequency ripple rejection, or will it be used for high frequency decoupling for an IC? Along with the answers of these questions, the voltage and the current that the capacitor will be submitted to is another concern of the designer.

For the low frequency ripple rejection in the output of an SMPS, large values of aluminum electrolytic capacitors are used. The capacitor terminal law is given by the following formula.

$$i(t) = C \frac{dV(t)}{dt} \quad (3.2)$$

It is obvious that for a specific amount of current, the lower the voltage ripple becomes, as the capacitance  $C$  is increased. Therefore in the output, an SMPS requires a high capacitance such as tens or hundreds of microfarads ( $\mu F$ ). Electrolytic capacitors are one of the high density capacitors in terms of capacitance per volume. Although the ideal formula of (3.2) indicates the fact that lower ripple will be obtained by increasing the capacitance, the parasitic components of the capacitors will be a serious problem as the size gets larger. Discussing the effects of these parasitics on decoupling basics may provide a clearer comprehension. For that

reason the decoupling basics will be discussed and the corollary obtained will be applied to the output electrolytic capacitors as well.

The sharp rising and falling edges of a current waveform cause noise and EMI problems in an SMPS. The noise coupled to the digital and/or analog parts may result in unexpected responses from these devices. Hence, the designer should neutralize the effects of these high speed signals by decoupling them from the ICs or other components in the circuit via the decoupling/by-pass capacitors. The duty of a decoupling capacitor is to create a low impedance path to the ground for the undesired high frequency currents to flow. The impedance of a capacitor is calculated as

$$Z = \frac{1}{\omega C} \quad (3.3)$$

According to this ideal equation the impedance curve of a capacitor is expected as a straight line as in Figure 3.8.

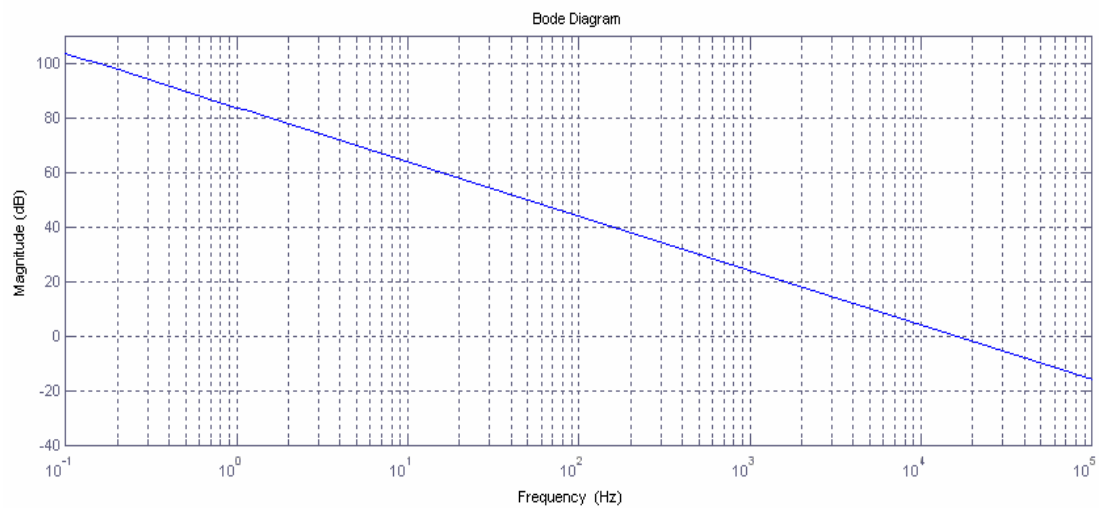


Figure 3.8 The impedance curve of an ideal capacitor.

The curve in Figure 3.8 is a bode-diagram; the base impedance is taken as 1  $\Omega$  and the capacitance value is taken as 10  $\mu\text{F}$ . If any capacitor behaves as in the curve in

Figure 3.8, the decoupling capacitor selection process would be a simple process. However, this ideal case is never valid in the real world and a practical capacitor can never be treated as only a pure capacitor. The contact resistances, the lead inductances, and other parasitic components cause the capacitor to be non-ideal. This non-ideality should be modeled and considered for the right selection of the capacitor. There are different models for the real capacitors depending on the type of the capacitor. The generally adopted model for a real capacitor is shown in Figure 3.9.



Figure 3.9 Capacitor equivalent model.

It is seen on the figure that, the capacitor has an equivalent series resistor and inductor components. These components are basically caused by the connection lead's themselves and by the points where the electrodes contact with the leads inside the capacitor. The impedance in equation (3.3) needs to be modified and the more accurate impedance formula which includes the parasitic effects is given as

$$Z = \sqrt{ESR^2 + (X_L^2 - X_C^2)} \quad (3.4)$$

where  $X_C$  is given as in (3.3) and  $X_L$  is given as

$$X_L = \omega L \quad (3.5)$$

Since the values of these components are too small, the effects of them were neglected in the era prior to the switch mode power electronics where the applications had low frequency. The high impedance of a capacitor in low

frequency dominates and the effects of these parasitics are negligible. Therefore, the impedance curve can be approached as in Figure 3.8. However these parasitics change the impedance curve as in Figure 3.10 at higher frequencies. The curve is obtained by assuming a 10 $\mu$ F capacitor with a 25 milliohm ESR and 10nH ESL. It is obvious that for a low frequency application, for example line frequency or even higher up to kHz level, the capacitor behaves as a capacitor. The impedance continues to decrease with increasing frequency.

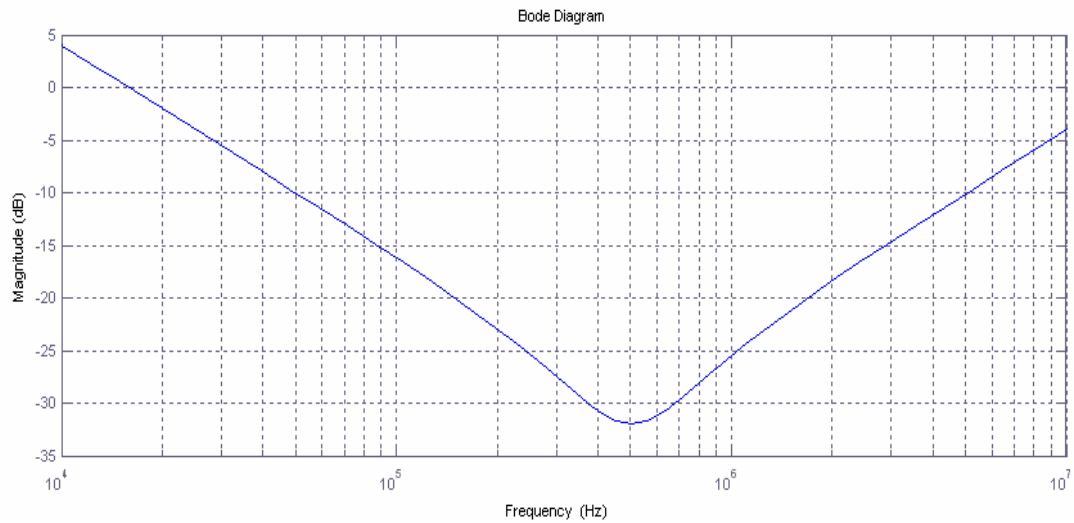


Figure 3.10 Impedance curve of a real capacitor.

However, after a valley at the 500 kHz point, the impedance starts to increase with increasing frequency which is the characteristic of an inductor, not of a capacitor. Thus, it can be claimed that after a resonance point the capacitor becomes an inductor; and near the resonance point the impedance is determined by the ESR of the capacitor. Therefore for a successful decoupling, the frequency to be decoupled should correspond to a frequency below or around the capacitor self resonance. Decreasing the ESR and ESL will take the capacitor closer to the ideal case. Hence, decoupling capacitors should be placed as close as possible to the associated pin of IC to eliminate the effects of PCB trace resistance and inductance. To eliminate the

capacitor lead inductance radial type capacitors can be selected rather than the axial types. The radial type capacitors are more suitable in high frequency applications because the through-hole structure of the PCB minimizes the length of the capacitor leads while connecting it to the circuit.

In aspect of capacitor types, for the decoupling of the ICs, the ceramic or multi-layer ceramic type capacitors can be preferred. Because, only the ceramic capacitors have extremely low ESR value that is needed to reduce the ripple voltage amplitude [39]. However, ceramic capacitors can only be found up to a few tens of nanofarads and at hundred-volt levels. Therefore, these capacitors cannot be used to reduce spikes at high voltage levels and also can not meet the requirements for higher capacitance values in low voltage levels. For higher capacitor or higher voltage requirements polyester or polypropylene film capacitors are preferred. Tantalum capacitors can also be used for decoupling up to hundred kHz levels; however, since they are polarized capacitors they can only be used in components which have a DC value that is greater than its peak AC value.

Now these principles can be applied to the output capacitor selection process. Suppose the curve of Figure 3.10 is an output capacitor curve. That means it shows the amount of output voltage swing in a specific frequency and current. Hence, for a designer, the values of the parasitic resistance and inductance are now constraints to design the output side and to choose the output capacitor. Aluminum electrolytic capacitors are used at the output side for the high capacitance requirement. However, since the size of these capacitors can be large, the parasitics of the device can also be large causing the voltage spikes and high ripples occur in the output voltage. For that reason, along with the low frequency large-valued capacitance, a high frequency small-valued capacitance is paralleled to decouple the high frequency components. At this point two questions arise: What happens, if more than one high-frequency capacitor is paralleled to decouple different frequencies in circuit? What happens if more than one same decoupling capacitor is paralleled at the output?

Paralleling more than one high frequency capacitor may cause some problems. While two different frequencies are decoupled by the self resonances of each capacitor, some frequency components between the resonance frequencies may be amplified. Figure 3.11 shows the response of two different capacitors paralleled. A 1 $\mu$ F capacitor with 10 m $\Omega$  ESR and 5nH inductor is paralleled to the former capacitor. It is clear that, depending on each of the capacitor, there are two resonance points at 500 kHz and just above 2 MHz. However an anti-resonance point exists at above 1 MHz. Therefore two capacitors having closer frequency responses should not be placed parallel. The optimum solution is to use aluminum electrolytic for low frequency with a high frequency ceramic or film capacitor depending on the application.

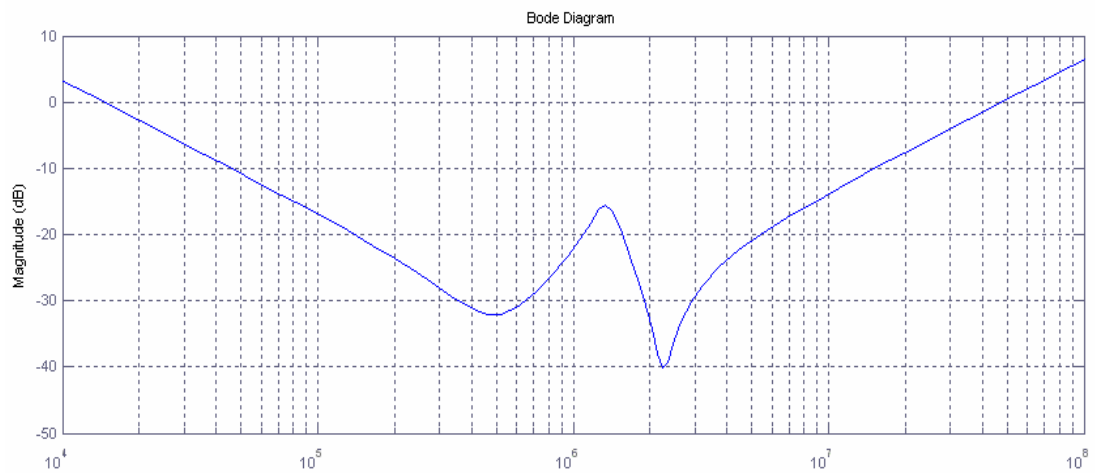


Figure 3.11 Impedance curve of two different capacitors connected in parallel.

Placing more than one identical capacitor may work positively. Figure 3.12 shows the impedance of one, two and four identical capacitors connected in parallel. In the figure Z1 shows the curve of the single capacitor, Z2, two capacitors paralleled, and Z4 shows four capacitors paralleled.



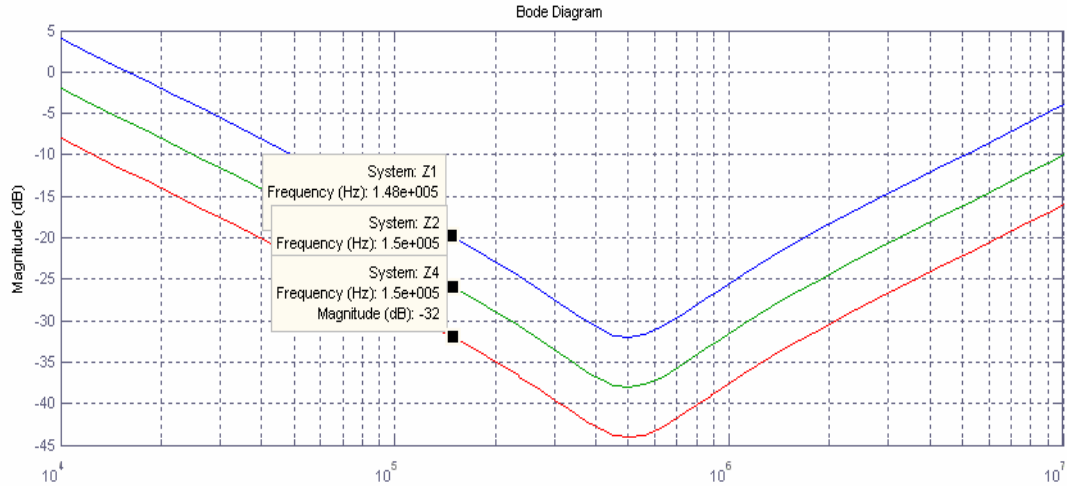


Figure 3.12 Impedance curve of same capacitors connected in parallel.

It is clear in Figure 3.12 that the identical capacitors keep the resonance frequency identical since the total capacitance value is multiplied by  $n$  (number of parallel capacitors) while the total inductor value is divided by  $n$  in parallel connection. ESR also decreases in the same way as the ESL. Therefore, the impedance of the combination is decreased as the number of parallel components increases. Real component curves and more information can be found on [39]-[43].

### 3.3.2 Magnetic Components

Yet another types of passive components used in SMPSs are the magnetic components which can be classified as energy storage components (inductors) or energy transfer components (transformers). The magnetic component in the flyback converter performs both functions. Although the design philosophy between these components may differ in some ways, the magnetic principles are the same and well-known concepts such as Faraday's Law and Ampere's Law. In this section the practical magnetic design will be discussed briefly. The sources on magnetic design may offer complex formulas and involved parameters in these formulas which are

sometimes difficult to comprehend and apply. The main purpose here is to introduce an introduction-level practical design to comprehend the basic magnetic design concepts. When the designer becomes somewhat experienced at the end of the design and gains some physical insight about the phenomena, the first primitive design can be improved using the advanced resources on magnetic design. Since the scope of the thesis includes the flyback and forward converters, the general concepts discussed in this section are related to magnetic circuits involving these converter types.

The components of a magnetic component are basically a magnetic core and copper wire for the windings. Hence the type of core material and the way the copper wires are wound carry significance in the performance of magnetic component. The type of the core material is determined by the application and mainly by the frequency. In the low frequency applications the general limitation of the core depends on the saturation. At low frequency transformers, silicon steel laminations are preferred because of their high flux density and low cost. However, they have relatively low resistivity which causes eddy currents and that's why these cores are manufactured in laminated structure. By this way the eddy current circulation is limited to a small area. In SMPS applications design approaches are different because of the high frequency switching.

Powdered metal cores and ferrite cores are the preferred materials in SMPS applications. Distributed air gap powdered metal cores have energy storage capability in their distributed air gap between the metal powder particles. Therefore these types of cores are suitable in applications where a magnetic component is utilized to store energy.

The most popular material type used in SMPSs is ferrite. Ferrites are ceramic materials made by sintering a mixture of iron oxide with oxides or carbonates of either manganese and zinc or nickel and zinc [44]. They can be both used in a transformer application or in an inductor application by adding a discrete air gap.

They offer low magnetic flux density limit ( $B_{SAT}$ ) generally 0.3 T. However, in high frequency applications  $B_{SAT}$  is not a real limitation [44]. The main limitation in high frequency is the core loss caused by hysteresis loss or eddy currents. The advantage of ferrite cores at this point is the high resistivity of the material which limits these eddy currents.

The ferrite cores can be found in different shapes and sizes. The dimensional and design data on all of these cores can be found in [45]. Generally EE, ETD, EFD, U, and RM/PM type ferrite cores are recommended for flyback and forward converters [46].

Given the magnetic circuit external specifications, the first step of the magnetic design is to select the core type and core size. As the core material, the ferrite core is the point of interest because ferrite cores are commonly used in flyback and forward topologies. In selection of the core dimension, there is no certain formulation that determines directly the core size. The empirical formulation called area product is used which is introduced in [44], [45], and [47]. However, core power handling does not scale linearly with area product or with core volume. Because the surface area dissipating heat does not increase in proportion to the volume producing heat [47]. Most manufacturers' no longer provide area-product information but use their own methodology to estimate power handling capability for a given core size [47]. The recommended core types in low power flyback design are tabulated in Table 3.1.

Table 3.1 Recommended core types for low power flyback converter design [46].

Output Power Level	Recommended Core Type
0 to 10W	EFD15, EF12.6, EF16, EE8.3, EE13, EE16, EE19
10W to 20W	EFD17, EFD20, EF20, EE13, EE19, EE22
20W to 30W	EFD20, EFD25, EE13, SEE16

After selecting the core type, the flyback transformer can be designed by using simple magnetic equations. The inputs of the design are the electrical values determined by the converter circuit such as turns ratio, primary/secondary voltage, current, and inductance values. The output of the design process should be the size of the air gap and the number of turns that will not saturate the core and provide the required inductance value. Hence, at this point of design, the air gap structure should be determined to continue the design process.

A single air gap can be placed to the center lag of the core which the bobbin is placed around. This will minimize the external field and hence the radiation and fringing losses. When the single gap structure is used, it should be considered that all of the magnetic energy is stored on this gap. Therefore, to provide the required inductance value the size of the single gap may be large which causes some increase in the fringing fields. In this situation to obtain more accuracy the air gap area correction (by employing a fringing coefficient) can be applied while calculating the reluctance. The air gap area correction details can be found in [44].

Another choice is gapping all legs of the core. This is more practical and economical since the two halves of the core are separated by a non-magnetic material which can even be an ordinary paper material for non-critical applications. In this case, the gap size is smaller because the single gap is distributed to three legs. In general, it is preferred to place the bobbin to the gapped leg to decrease the fringing field and radiation [44]. However, in this case it is not possible since all the legs are gapped. What is not possible? Since the bobbin placed in the center leg, the outer leg gaps may radiate EMI. The practical solution for that problem is to wind a shorted copper strip just around the core. The strip should be placed as co-axial with the turns and just at the gap level to prevent the radiation from the gaps. The shorted copper strip can also be grounded if required to carry the induced currents to the ground. Figure 3.13 (a) and (b) show the single and multi gap configurations.

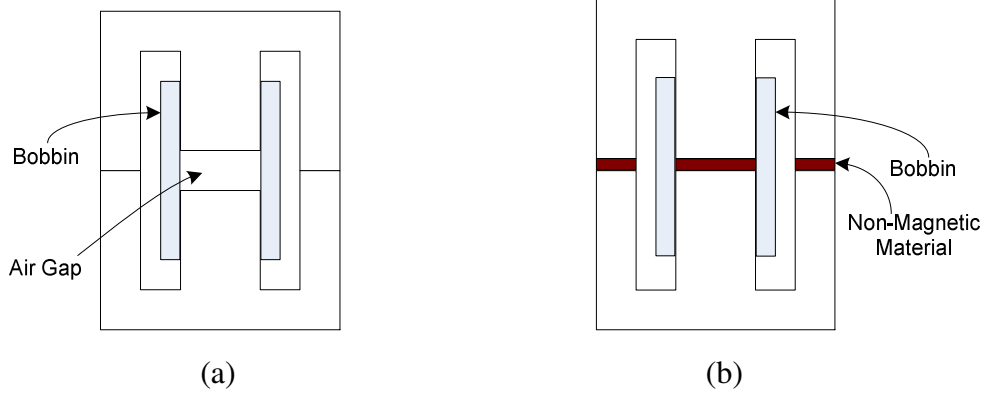


Figure 3.13 Transformer cross section: (a) one leg gapped; (b) all legs gapped.

After choosing the air-gap type, the calculations can be performed to find the number of primary turns ( $N_p$ ) and the gap size ( $l_g$ ). The number of primary turns can be calculated using the total flux linkage equation.

$$L\Delta I = N\Delta\phi \quad (3.6)$$

$$N_p = \frac{L_p \Delta I_{MAX}}{A_c \Delta B_{MAX}} \quad (3.7)$$

where  $L_p$  is the primary inductance,  $A_c$  is the core cross section,  $\Delta I_{MAX}$  and  $\Delta B_{MAX}$  are the maximum changes (peak to peak ripple at steady-state) in current and flux density during one switching period.

After finding the number of primary turns, the air gap size ( $l_g$ ) can be obtained using inductance formula of (3.8).

$$L_p = \frac{N_p^2}{R} \quad (3.8)$$

where  $R$  is the total core reluctance given by

$$R = \frac{l}{\mu A} \quad (3.9)$$

In an inductor or flyback transformer design the energy stored by the core material is negligible since most of the energy is stored in the non-magnetic gap (air gap). Therefore, the reluctance of the core can be neglected and the total reluctance can be taken as the gap reluctance. Hence, in the reluctance formula,  $l$  is the air gap length  $l_g$ ,  $A$  is the air gap area (may be taken as core cross sectional area or corrected gap area), and  $\mu$  is the permeability of free space ( $\mu_o$  here)  $4\pi \times 10^{-7}$ .

At this point there is one difference between one gapped and three gapped configuration. In one-gapped case, an air gap length of  $l_g$  results in a reluctance value as explained in previous paragraph. However, an  $l_g$  gap in three legs will end up with different reluctance result. The magnetic circuit can be drawn and an equivalent reluctance can be calculated. Figure 3.14 shows the magnetic circuit of the flyback transformer shown in Figure 3.13 (b).

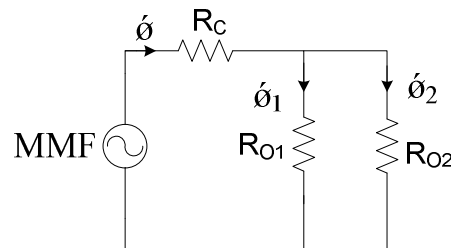


Figure 3.14 Magnetic equivalent circuit of a three gapped core.

$R_C$ ,  $R_{O1}$ , and  $R_{O2}$  are the reluctances of center leg and the outer legs respectively. Since all the legs have the same air gap, by calculating the equivalent reluctance of this magnetic circuit, the total reluctance caused by an air gap length of  $l_g$  can be calculated.

In summary for the flyback converter, first, the core material and the core type are selected. Then, the primary number of turns is calculated using the known circuit

parameters such as  $L_P$  and  $\Delta I_{MAX}$ .  $\Delta B_{MAX}$  is a design parameter and selected by the designer. The maximum B value of the ferrite materials are about 0.3-0.4 T. However, in high frequency, if the flux (hence flux density) change is large, the core losses may increase. Therefore, to keep the losses in a reasonable level maximum flux density can be applied about 0.15T in high frequency applications. This value may seem quite low however, as the saturation does not bring a limitation at high frequencies.

The forward converter magnetic design is simpler than the flyback transformer design because the forward converter topology involves a simple high frequency transformer. However, all forward mode converters need core resetting in their transformers since they have no flyback period for energy transfer. Hence an external flyback effect should be implemented by the designer. At this point, the amount of the stored energy in the core that is released is significant because it determines the transformer structure. If an RCD snubber circuit is implemented, the transformer can be designed with two windings; or, a tertiary winding can be implemented to return the energy to the supply which is a more efficient method. However, a third winding in the transformer is required in this case, which may bring complexity to the design of the transformer. The latter approach will be covered in this part.

The forward converter transformer design principles are not much different from the flyback transformer. However, a specified inductor value is not available in this application since the transformer should transfer as much energy as possible. Hence, as a design specification, the designer should determine the  $B_{MAX}$  value which is a point of trade-off. If  $B_{MAX}$  is kept too low, the number of turns hence the core size will increase. If  $B_{MAX}$  becomes too high, the losses will increase although the transformer size becomes smaller [48]. The  $B_{MAX}$  value can be selected around 0.15T as in the flyback case.

Other inputs for the design are the turn ratios between, primary-secondary and primary-tertiary windings according to the application. Turns ratio between primary and secondary determines the output voltage level. Primary to tertiary turns ratio determines the maximum allowable duty cycle, depending on the reset function.

$$D_{MAX} = \frac{1}{1 + \frac{N_3}{N_1}} \quad (3.10)$$

Choosing the  $N_3/N_1$  ratio high will cause a slower resetting action, hence results with a smaller  $D_{MAX}$ . Choosing it low may cause excessive voltage levels appear on primary and also on switch. Therefore, this selection also affects the switch selection process; or in other words, a pre-selected switch may also limit this turns ratio determination. This is a trade-off point as well. A designer can increase  $D_{MAX}$  by decreasing  $N_3/N_1$  ratio and can increase  $N_2/N_1$  to reach the desired output level. Or with a higher  $D_{MAX}$ ,  $N_2/N_1$  may be decreased. After selecting the turns ratios and  $B_{MAX}$ , the primary turns number  $N_1$  can be calculated by employing Faraday's Law.

$$V(t) = N \frac{d\phi}{dt} \quad (3.11)$$

$$N_1 = \frac{V_{IN} D_{MAX}}{f_s B_{MAX} A_C} \quad (3.12)$$

The secondary and the tertiary winding number of turns can be calculated using the turn ratios. After finishing the introduction of theoretical design concepts, some practical aspects can be discussed. In a flyback converter, to obtain a good coupling between primary and secondary, the wires should be wound tightly and coaxially. This will provide the proper magnetic flux alignment and reduces the leakage flux. In a multi layer design, the primary terminal which will be connected to the switch can be selected as the bottom terminal to provide self shielding [49]. To reduce the risk of interlayer voltage breakdown due to insulation failure, layer to layer



insulation must be improved and the interlayer capacitance should be decreased by placing polyester film tape [49]. This will also help the alignment of the upper layer to be smooth. Some details on winding techniques can be found in [50]. Another problem of the flyback transformer is the leakage inductance which may interact with the switch capacitances and causes voltage spikes or oscillations. In the complete demagnetization mode of the flyback converter, the energy transfer ends before the (1-D) period ends, hence this time the charged capacitors of switches (diode or MOSFET) may resonate with the magnetizing inductance which will be observed as a lower frequency oscillation in comparison to the leakage case. In order to prevent these oscillations or to damp them rapidly a snubber network is required which will be discussed in the next section. It should be mentioned, in some operating modes, such resonant modes can be utilized to the benefit of the converter as soft switching condition may occur for the transistor.

Another snubber requirement exists in the forward converter topology. One option to reset the core is to use a snubber circuit which causes the converter inefficiency. Therefore, the reset winding techniques have been proposed and adopted, however the tertiary winding is not a complete solution. The leakage inductances of the windings also store some energy that can not be transferred and should be dissipated. For this reason, a forward converter with reset winding may also require a snubber but this time a smaller amount of energy (the energy that can not be transferred by reset winding) will be dissipated on. Hence the efficiency is still better than the snubber with no reset winding case. The following section will explain the basics of snubbers.

### **3.4 Snubber Circuits**

Snubbers are small networks of parts in the power switching circuits whose function is to control the effects of circuit reactances [50]. Snubber circuits reduce the stresses by limiting the voltages, currents during the switching transients and

limiting the rate of rise of voltages and currents as well. As a result, the voltage spikes on switches are reduced and the circuit performance and reliability is enhanced. Snubber circuits also reduce EMI with the rate of rise limiting property. First classification of snubbers can be based on whether the components of snubber circuits are active or passive. Hence the snubbers are named in the same way as active snubbers or passive snubbers. In flyback and forward converters, passive snubbers are generally used because of their simplicity.

Passive snubbers can be classified as dissipative and non-dissipative snubbers. If the energy absorbed by the snubber is dissipated on the snubber resistor then the snubber is called as dissipative; if the energy is somewhat returned back to the source capacitor than the snubber is said to be non-dissipative. The snubbers can also be classified according to the direction of energy flow as polarized or non-polarized snubbers. Since the main concern here is the basic flyback and forward converter design, dissipative type of passive snubbers will be discussed.

One of the most popular snubber types is the basic RC type snubber which is composed of a resistor and a capacitor connected in series. The configuration is connected in parallel to the switching device under stress. RC type snubbers are used for damping and reducing the rate of rise of voltage however the main application of the RC snubber is damping [51]. The capacitance of the snubber capacitor must be larger than the resonant circuit capacitor in order to damp the oscillations. The resistance value in the snubber must be close to the characteristic impedance of the parasitic resonance [51], which is given by

$$Z = \sqrt{\frac{L}{C}} \quad (3.13)$$

L and C represent the parasitic inductance and capacitance values respectively. An experimental methodology is offered in [51] to calculate the RC values in the snubber. First, the frequency of the resonance is determined without snubber and

after that a capacitor is placed in parallel to the device. The designer can alter the capacitance value up or down until obtaining the half of the previously observed resonance frequency. Considering the parasitic inductance is constant, the total capacitance should be at least 4 times greater from the original value to obtain the half of the resonance frequency depending on the formulation of resonance frequency given below.

$$f = \frac{1}{2\pi\sqrt{LC}} \quad (3.14)$$

When half of the original resonance frequency is obtained the external capacitance value is the 3 times larger of the parasitic resonance circuit capacitance. By this way the approximate value of the parasitic capacitance can be obtained which leads the designer to calculate the parasitic inductance value using (3.14). After finding both the L and C values, the characteristic impedance can be calculated according to (3.13). This value gives the value of the snubber resistor, and a suitable capacitor value can be chosen since the parasitic capacitance value is no more an unknown parameter.

The main type that is used with the flyback and forward converters are resistor-capacitor-diode or RCD snubbers. These snubbers can be used for both rate of rise control or clamping purpose. However, in forward and flyback converters it is generally used as the clamping snubber. The clamping snubber network is shown with a flyback topology in Figure 3.15.

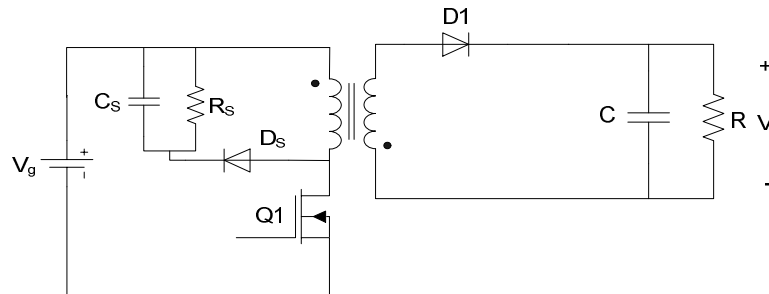


Figure 3.15 Flyback topology with RCD snubber network.

This snubber network can not be used for the rate of rise control since there is a direct DC path through  $D_S$  and  $R_S$ . For the clamping purpose the RC time constant of the snubber should be higher than the switching period  $T_S$  [51], [52]. In order to calculate the  $R_S$ ,  $C_S$  values, the amount of stored energy should be estimated in the leakage inductance which requires the data of leakage inductance value. The leakage inductance may be obtained via a short circuit test however; it will be difficult to carry out a short circuit test in high frequency transformers because of the interlayer and interwinding capacitances. A good estimation of the leakage inductance for a carefully wound transformer is 3% of the magnetizing inductance. Some tolerance may be added for the design safety considerations. By using this value the stored energy can be calculated as

$$W = \frac{1}{2} L_{\text{leakage}} I^2 \quad (3.15)$$

$I$ , is the peak current at the turn-off instant. The amount of power that will be dissipated on the snubber can be calculated after obtaining the energy.

$$P = W f_s \quad (3.16)$$

The total voltage across the switch during off state of the switch is the sum of the input voltage and the voltage across the snubber terminals. Hence the designer can select a safe voltage level for the switch and calculate the snubber clamp voltage level.

$$V_R = V_{\text{SWITCH}} - V_{\text{IN}} \quad (3.17)$$

$V_R$  is the voltage across the snubber terminals. Now, after obtaining the power dissipated on resistor and the voltage across the resistor, it is possible to obtain a  $R_S$  value using the simple power formulation.

$$R_s = \frac{V_R^2}{P} \quad (3.18)$$

The value of the snubber capacitor can be calculated by choosing an RC time constant that is much larger than the  $T_s$  switching period. The capacitor type should be a low ESL capacitor again since a resonance is possible with the junction capacitance of the snubber diode. [52] offers an additional RC network, with the traditional RCD snubber to damp the oscillation caused by the diode reverse recovery. Since the diode will turn-on and turn-off in every switching period, it should be selected as a fast recovery diode as well. A schottky diode can also be used.

### 3.5 PCB Design Considerations

One of the most challenging parts of the hardware design is the PCB design part in high frequency converter design. As the frequency increases, the parasitic components of PCB start to dominate the parasitics of other components. PCB traces are considered as an inductor and the nanohenries per cm calculations need to be carried out. The PCB traces which are close to each others or the layers of a multilayer PCB exhibit capacitive behavior because of the increasing frequency again. These parasitics require an optimization to limit the EMI of a system to minimize the noise. A commercial product is also responsible to fulfill the requirements of Electromagnetic Compatibility (EMC) standards. In this section the basic PCB design strategy and some critical points will be discussed. By aiming a designer making first PCB design, the basic definitions will be introduced first.

The rules on high frequency design such as grounding, component placing, and routing are generally common in all types of applications however, some points may differ in a power electronic circuit design because the PCB traces conduct higher current and voltage with respect to an electronic circuit. At this point the

basic routing rules of a PCB will be introduced and the critical points of component placement in the SMPS applications will be discussed.

In all high frequency PCB designs, the parasitic resistances, capacitances, and the inductances of the traces are crucial. Hence the traces, especially traces carrying high currents or high  $di/dt$  currents, should be as short as possible and wide to decrease the parasitic inductance and resistance. The longer the PCB trace is the more EMI radiation will happen. Therefore the more traces will be coupled by this radiated EMI causing the increase of conducted EMI as well. While routing, the traces should be used as  $45^\circ$  and should progress by twisting along the board instead of going directly point to point [53], [54].

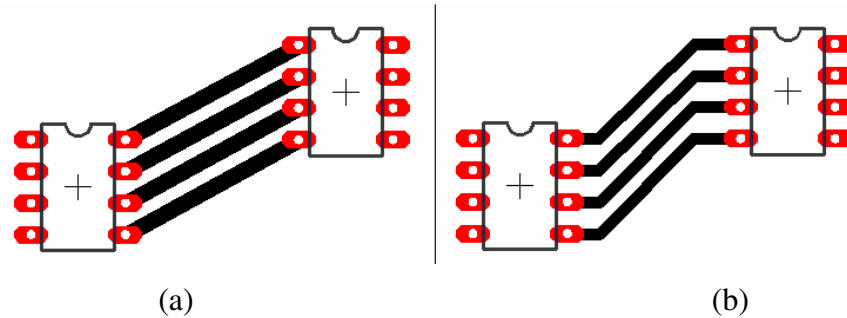


Figure 3.16 PCB routing examples: (a) bad routing; (b) correct routing.

Power and ground traces are other critical traces hence need special care while routing. The basic rule for power routing is not making a loop and distributing them from one point known as the star connection method. If a power trace is connected to one pad of an IC and out of this pad to the associated pad of another IC, the noise caused by any IC affects all other ICs since the current paths of the all ICs are common by a single trace. Therefore the ground and power connections should be carried from one point and delivered separately to the ICs instead of a one single way. The wrong and the correct methods are shown in Figure 3.17.

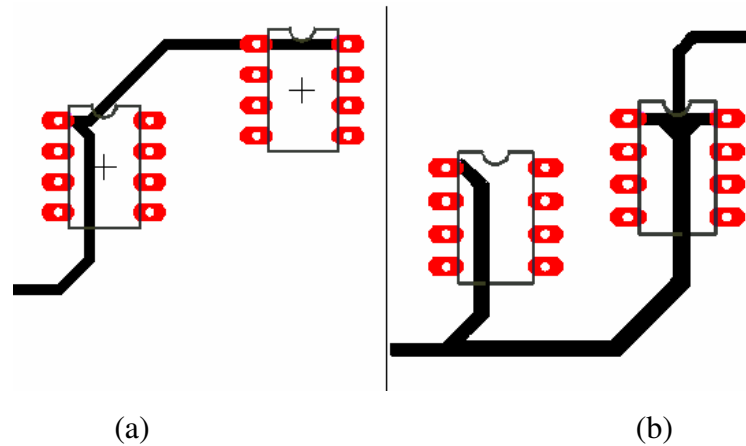


Figure 3.17 Connection of power traces: (a) wrong single trace connection; (b) correct star connection.

The main idea of the grounding is the same as the power tracing along the board. For reduced noise and EMI, the separate ground planes are recommended in the PCB design. The ground planes will provide low inductance return paths for the current hence decreases the voltage peaks caused by the current transients. Ground planes may also perform the shielding action for radiated EMI. Therefore it is recommended to use as much copper as possible. The critical point here is to make hardware partitioning. The components that serve to the different function in the circuit should be connected to the separate ground plane. For instance the power stage and the control stage of a circuit should have different ground planes; or digital parts and analog parts should have separate ground planes. These separate planes should be connected to the main ground at only one point to prevent the ground loop problem as in the power routing case. An example of grounding via ground planes is shown in Figure 3.18.

In a single layer design, the ground planes provide a low inductance path for the return current hence the traces carrying high  $di/dt$  currents should be as short as possible to minimize the area it embraces [55]. The high  $di/dt$  paths of a boost

converter are shown in Figure 3.19 on a generic boost converter schematic. The components on the specified paths should be placed close to keep the trace lengths at minimum on a PCB.

When a double-sided or a multi-layer design is considered the ground or power planes should be placed carefully because of the high  $dv/dt$  components and traces on the PCB. Since the wide copper areas will result as higher parasitic capacitance values, the high  $dv/dt$  signals will cause higher current spikes in wider copper planes. Both the high  $di/dt$  and high  $dv/dt$  concepts are important for conducted and the radiated EMI issues. An important clue can be twisting the all critical PCB traces to obtain the mutual cancellation of magnetic fields [55].

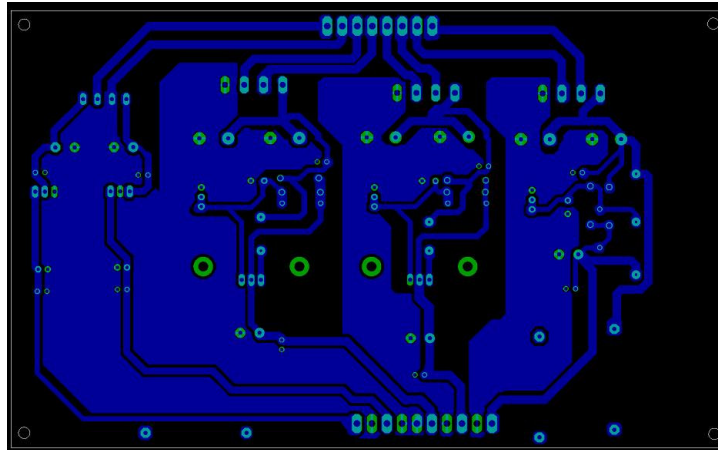


Figure 3.18 Ground planes on a PCB.

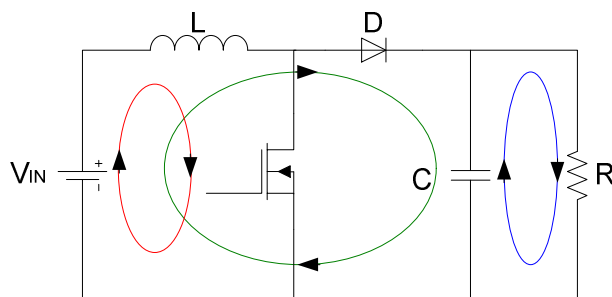


Figure 3.19 Current loops in a boost converter.



The loops are antennas, which radiate EMI to the devices around them [52]. Therefore, while considering the component placement, the tendency of placement should be in a way that minimizes these high  $di/dt$  current loops. The placement of power stage components must be compact to reduce these loop areas. The other parts of the circuit such as analog controller chips and the components of control circuitry can be placed to the far side of the PCB, especially far from the high frequency transformer in an isolated application to discard the effects of field caused by the transformer. Keeping the low and high frequency side circuit components separate will provide the separation of these signals and hence reduces the noise coupling.

Mentioning the current loops on SMPSs completes the hardware design chapter. Through the chapter, the basic component selection processes were discussed and the diode-MOSFET switching characteristics were examined. The importance of diode reverse-recovery process is explained. Passive component selection was another main concern of the chapter. The results of the non-ideality of the capacitor caused by the parasitic elements called as ESR and ESL were discussed and the frequency response for the capacitors were inspected. In the magnetic component side, the transformer and the inductor design approaches were discussed. The magnetic principles utilized for design process, were explained to prevent the confusion caused by the equations given in suppliers' technical documents. The chapter is finalized with the basic PCB and layout design approach. The topics such as correct routing and the layout rules for EMI optimization were covered in that last section.

## **CHAPTER 4**

### **THE POWER-POLE BOARD**

#### **4.1. Introduction**

The idea of implementing the previously discussed basic DC/DC converters in a single board to provide a better understanding of the topological relations requires reconfigurable hardware. The main feature of the power-pole board is the reconfigurable power-pole structure consisting of two MOSFETs and two diodes [56]. The drive circuits are also implemented on the board and a PWM controller is utilized to provide the PWM signals in variable duty cycle and frequency. The PWM signals obtained using the controller can be carried to the gate driver of either the upper or the lower MOSFET via small mechanical switches. The current sensing gate driver ICs provide overcurrent protection and shut down the gate pulses in case of an overcurrent condition. Three basic non-isolated and two basic isolated topologies can be implemented by configuring the power pole and changing the magnetic components which are designed as separate plug-in magnetics boards. These topologies are the buck, boost, buck-boost, flyback, and forward converters. There is also small-signal analysis pin available on the board for small signal injection and determining the frequency response of the board. Obtaining this response, a student can design a controller to demonstrate closed-loop operation. The daughter boards are available for voltage/current mode control and required output pins are available on the board to connect it to the daughter boards.

## 4.2 Hardware Description

The generic block diagram of the power-pole board is shown in Figure 4.1. The upper and lower switches can be connected by using their end terminals. The input current and the current of magnetic device are measured using two hall-effect sensors (manufactured by LEM). Both terminals of the power-pole board have a 680 $\mu$ F aluminum electrolytic capacitor and a 10 $\mu$ F tantalum electrolytic capacitor connected in parallel.

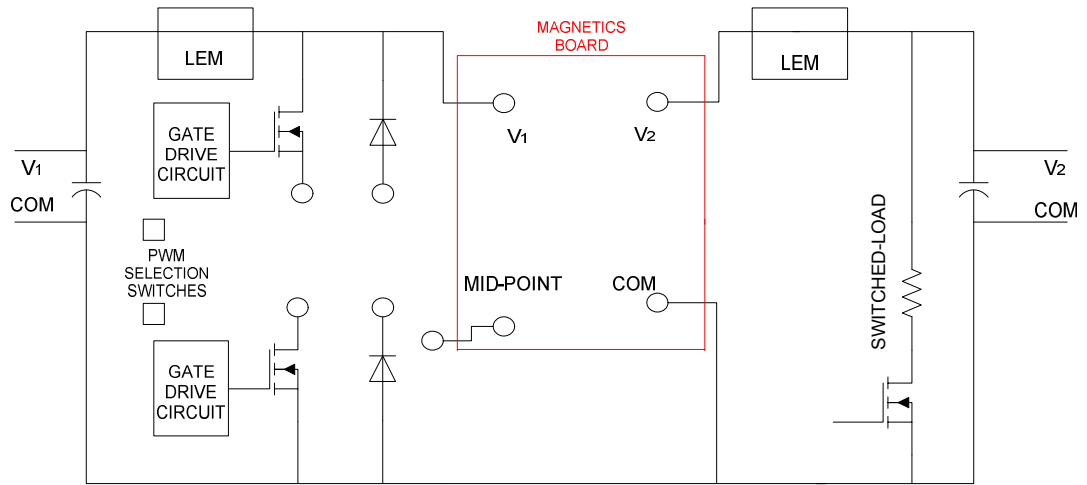


Figure 4.1 Generic block diagram of the power-pole board.

Connecting the required end terminals of the switches and using the proper magnetic board, the converters mentioned earlier can be implemented on the power-pole board. For example, to implement a buck converter, the  $V_1$  terminal is selected for input since the magnetic component (inductor) is at the  $V_2$  terminal side on the Power-pole board which will be the output for the buck converter. An upper MOSFET and lower diode are required for a buck converter. By connecting the end terminals of the upper MOSFET and lower diode, and connecting their common point to the mid-point terminal, a proper switch configuration is provided. The inductor is placed to the magnetic board side and the buck converter is obtained. For the boost converter, the dual of the buck converter can be considered. Hence,

the  $V_2$  terminal is input this time. The same inductor board is used and the switch configuration involves the lower MOSFET and upper diode this time.

There are three magnetic boards required to implement these five converters. The buck, boost, and buck-boost converters require only an inductor as a magnetic component. However the isolated topologies require transformers designed suitably for their operation. The manufactured magnetic circuits with their PCB mounted appearances are shown in Figure 4.2.

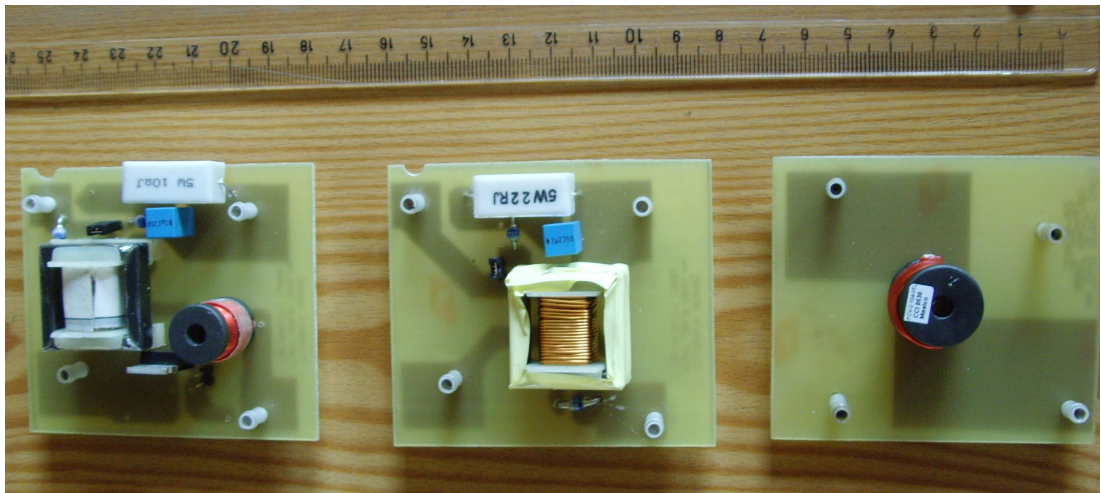


Figure 4.2 From left to right, the forward converter magnetic board, flyback converter magnetic board, and non-isolated converters' magnetic board.

The power-pole board also contains a switched-load configuration. An externally connected load is switched at about 10Hz. The switched-load is used to observe the load disturbance dynamics in the closed-loop applications. Figure 4.3 shows the complete view of the power-pole board with the hardware block interpretation. A detailed explanation of power-pole board can be found in Appendix-A

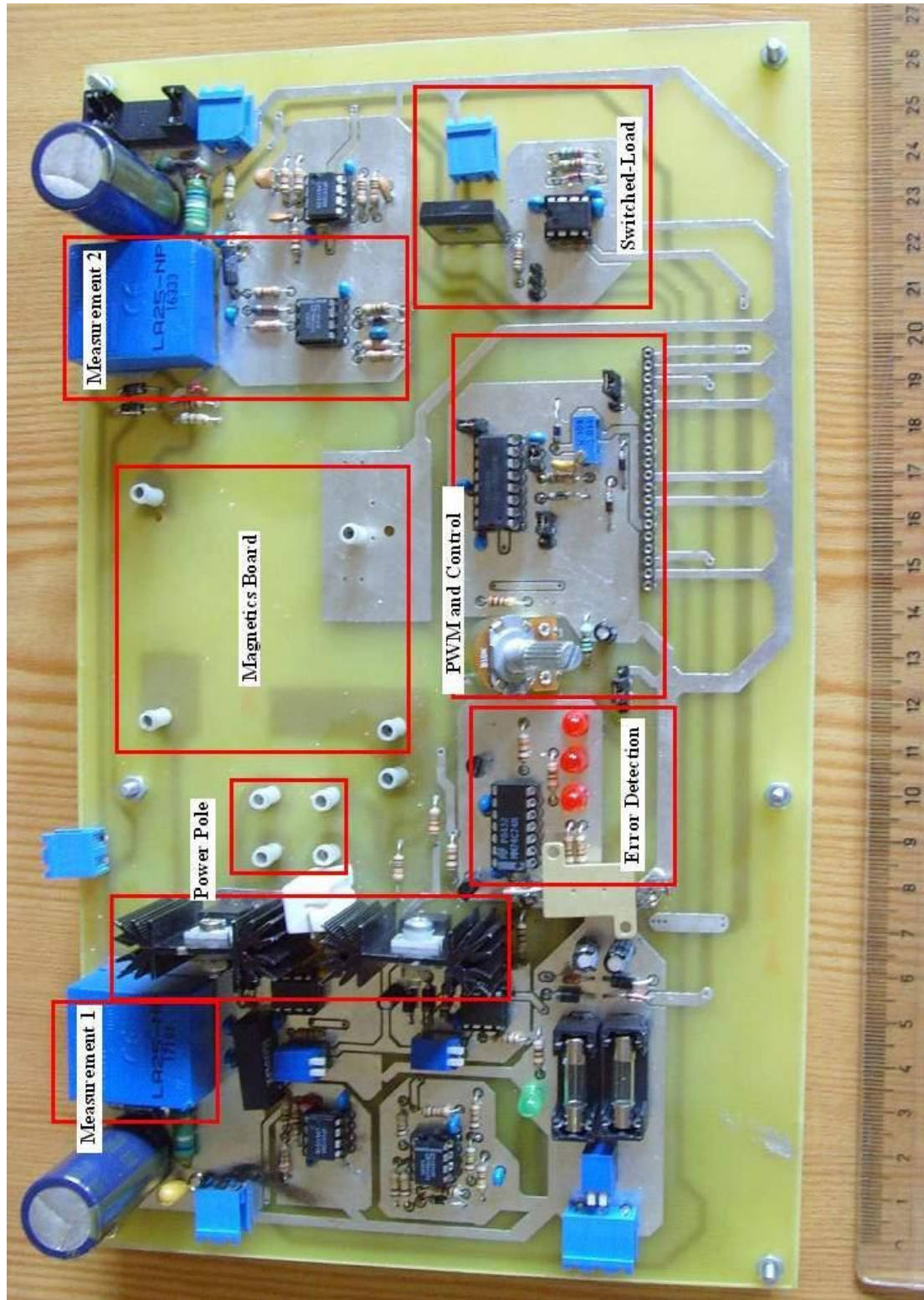


Figure 4.3 Power-pole board view with hardware blocks illustration.

### 4.2.1 The PWM Controller and Gate Drive Circuitry

To meet the isolated gate drive requirement of the high side MOSFET and to obtain high gate drive current, an IR2125 high side gate driver IC is used which has high output current capability. The IC also provides current sensing and cycle-by-cycle shut down in case of an overcurrent error. The upper side drive circuit is shown in Figure 4.4. The lower side drive circuit is the same with the upper gate drive circuit except the isolated DC/DC converter module which is used in high side drivers to guarantee a higher gate voltage than the floating MOSFET source terminal voltage.

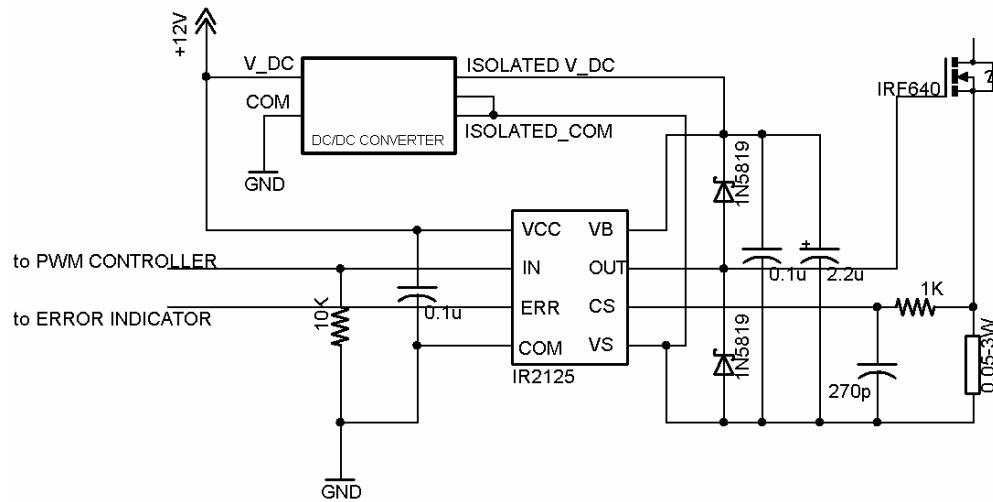


Figure 4.4 Gate drive circuitry.

An additional gate resistor has not been used in the design to obtain maximum gate current and minimum gate capacitance charge time. Since there is no damper (resistor) on the path, the IC should be placed as close as possible to the gate and the PCB trace must be wide to reduce stray inductances.

The PWM pulses are obtained by Texas Instruments' UC3824 PWM controller IC. Using a 10 k $\Omega$  potentiometer, the PWM duty cycle can be varied from 0 to 0.96.

The controller IC also provides variable frequency via a 100 k $\Omega$  trimmer potentiometer. With the help of the internal error amplifier of the PWM controller, it is possible to build a closed-loop control both in voltage and current modes.

The PWM controller IC offers an RC input. Hence it is possible to obtain a ramp by using appropriate resistor and capacitor values. Connecting the 100k $\Omega$  trimpot in series with a 10 k $\Omega$  resistor to the RT input and a 1nF capacitor to the CT input, a variable frequency range from 100kHz down to 30 kHz can be obtained. Pins 1, 2, and 3 of UC3824 are the terminals of inverting, non-inverting, and the output pins of an error amplifier respectively. The error amplifier is internal and can be configured for both open-loop and closed-loop operation. Pin 16 of the IC provides 5.1V DC reference voltage to be utilized in the control circuit applications such as obtaining the reference voltage. The DC voltage is scaled via a voltage divider which is realized with 10 k $\Omega$  pot; and is compared with the ramp waveform. This comparison operation is processed internally in the controller IC between the ramp waveform and the output voltage level of the error amplifier. For that reason the scaled 5.1V DC voltage of pin 16 is supplied to the non-inverting input of the error amplifier and a voltage follower configuration is used in the open-loop mode. The inverting and non-inverting inputs, and the output pins of the error amplifier can also be configured via two jumpers. In the closed-loop control mode all three terminals are brought to the daughter board connection pins separately for compensator design purposes. 5.1V zener diodes are placed to both inputs and the output of the error amplifier to prevent the saturation of the compensator in the closed-loop modes. The PWM controller circuitry is shown in Figure 4.5. As seen in Figure 4.5, the jumpers let the designer configure the error amplifier pins for open-loop or closed-loop mode. In the closed-loop mode the reference voltage can be applied using 10k $\Omega$  pot or the pins can also be configured to enable the use of an external voltage supply for reference voltage input. The PWM output is fed to the gate drive ICs through a 2.2K $\Omega$  and 10K $\Omega$  voltage divider resistors. Two mechanical switches are placed to select whether the PWM signals will be received by the upper or the lower MOSFET's gate driver.

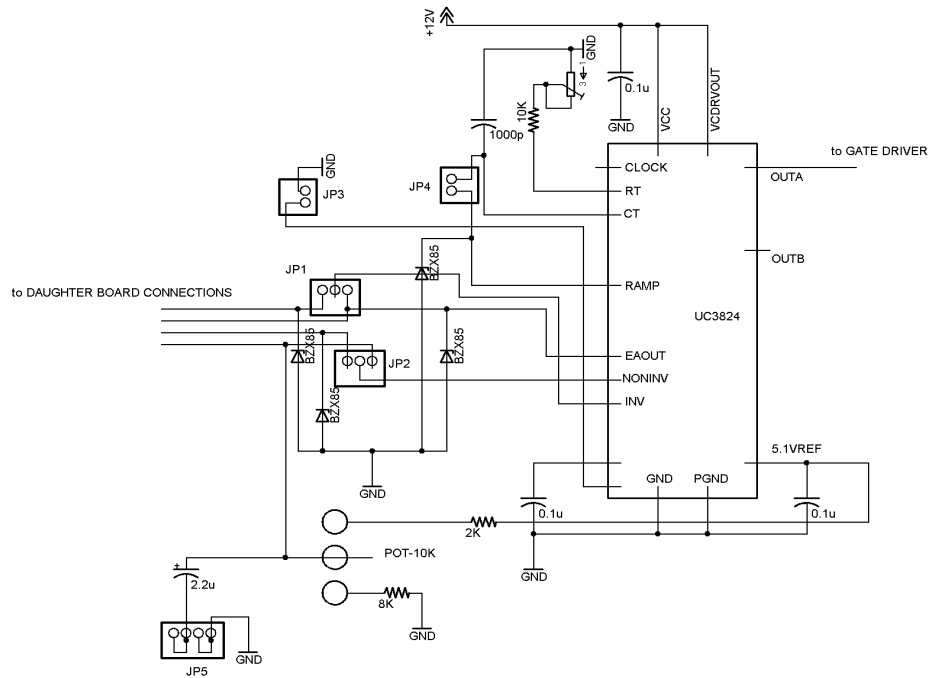


Figure 4.5 UC3824 based PWM controller circuitry.

#### 4.2.2 Error Detection and Protection Circuitry

The power pole board is protected against the possible overcurrent and overvoltage conditions by means of both simple fuses and electronic circuitry. The electronic power input ( $\pm 12\text{V}$ ) is supplied to the circuit through a 250mA fuse to protect the analog ICs. The power output is also protected with a 3A fuse against the short circuit possibility of the load.

Along with the fuse protection in the electronic side of the circuit, the power side of the circuit is protected by utilizing an electronic protection circuitry. When this circuit is activated due to a fault, the PWM output of the controller IC is disconnected from the input of the gate driver IC by turning on a BJT transistor that grounds the PWM signal.



Overvoltage protection is realized by carrying both the input voltage and the output voltage level via two diodes as shown in Figure 4.6. In that connection the diode on the path of higher voltage will be on and this higher voltage level (whether input or output) is scaled to its one tenth using a voltage divider. This voltage is theoretically compared to the 4.5V which is obtained by scaling of 12V using a 39K and 65K. Whenever the voltage exceeds 4.5V level, the overvoltage circuit protection is activated, the PWM signal is grounded, overvoltage and fault LEDs are on. Since the one tenth of the sensed voltage is compared with 4.5V the circuit will activate the overvoltage protection in case the input or the output voltage exceeds 45 volts.

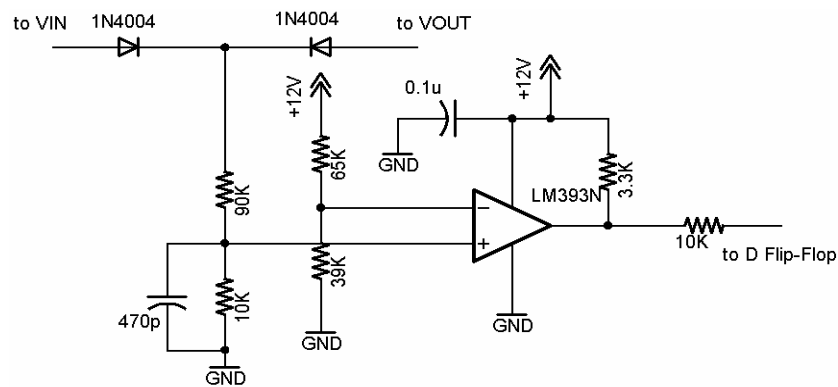


Figure 4.6 Overvoltage detection circuit.

Overcurrent protection is realized by the IR2125 gate driver ICs. When the current sense pin of the IC reaches 230mV threshold voltage, the IC detects an overcurrent condition and starts to charge the capacitor between the ERR pin and the ground with a constant charge current. When the ERR pin voltage exceeds 1.8V, the ERR pin is pulled-up to  $V_{CC}$  level indicating the error. The capacitor of ERR pin and the series resistor that the CS pin reads the voltage is crucial here. The over current level is determined by the series resistor. For example a 100m $\Omega$  resistor will set the overcurrent level to 2.3A (230mV/100m $\Omega$ ). The capacitor of the ERR pin

determines the time that the error voltage level(1.8V) is reached since the ERR pins provides constant current. The details can be found in [38].

The voltage levels that the overvoltage and the overcurrent fault conditions create are processed by the LM393 comparators and 74C74 data flip-flops and the resulting fault indicator LEDs are turned on. There are three LEDs indicating overcurrent, overvoltage and fault conditions. The fault LED is activated both in the overvoltage and overcurrent conditions. The power should be turned off and on again to remove the fault conditions and bring the circuit to the normal operation mode.

#### **4.2.3 Hall Effect Sensors and Measurement Circuitry**

Measuring the current is difficult in comparison with the voltage measurement. Since the voltage measurement is realized using high impedance probes, generally it does not effect the operation of any circuit. However current measurement requires a series connection of the measurement device (resistor) which is generally impossible for PCBs; or a small-valued resistor is connected in series and the current is measured by transforming it to the resistor voltage. Adding a series resistor may reduce the efficiency of the circuit and increases the parasitic inductance and decreasing the resistance value may reduce the SNR hence the intended signal may not be observed because of the switching noises.

One of the most practical ways to measure a current is to use Hall-effect sensors. In this work, the LA25-NP sensor manufacture of LEM is used in the circuit to measure the current. This sensor provides an isolated measurement hence improves the reliability and safety. The sensor has 5 input and output pins for the current to be measured. By series and parallel connection configurations 1 to 5 turns can be obtained. The measurement output provides current scaled to its 1/1000. In the connection in Figure 4.7, there are 2 turns in the device. First the current passes

through shorted three inputs to the three outputs. These outputs are connected to other two inputs and current passes through the device one more time which makes two turns in the device. Hence the measurement pin will output  $2/1000$  of the current passing through the circuit. This current is scaled on a  $250\Omega$  resistor to make possible the observation on the scope as a voltage waveform. For example, if 1A of current passes through the circuit the sensor output will scale it to 2mA. 2mA flowing through  $250\Omega$  results 0.5V. That means 1A of current will be observed as 0.5V of voltage in the oscilloscope.

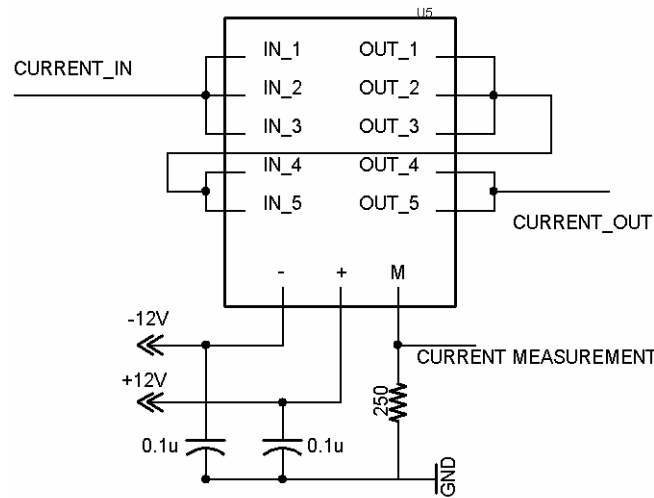


Figure 4.7. The current measurement circuitry using LA25-NP.

The measured input and output currents are brought out to the daughter board connection pins for control purposes. The voltages on the  $250\Omega$  precision resistors are scaled to twice of their values. Hence when the currents are observed from the pinheaders they will be seen by their actual values. The output voltage is also scaled and brought out to the daughter board connection pins. The scale factor is  $1/5$ . That means the voltage feedback gain  $H(s)$  is  $1/5$ , in aspect of controller design. This scaling is done to obtain the voltage level that is suitable to compare it with the ramp signal level produced by the UC3824 PWM controller.

#### **4.2.4 The Linear Power Supply for the Power-Pole Board**

In the previous parts of hardware description section, the different functions of the power-pole board such as gate drive circuitry, measurement parts, and error detection and protection have been introduced. All these parts of the system includes different ICs. For example, the measurement circuitry includes operational amplifier ICs to scale the measured signals. The high side gate-drive circuitry includes isolated DC/DC converter for MOSFET with the floating source. Error detection circuits employ operational amplifiers as comparators. All these ICs require power as either positive or negative level voltages to execute their duties. Along with the IC supplies, the experiments of the power-pole board require different levels of voltages at higher current ratings in comparison to the IC supplies. To meet all these requirements a linear DC power supply is designed with five different output voltage levels.

The power-pole board ICs require negative and/or positive 12V level. Since the ICs do not draw much current these requirements are met using conventional 7812-7912 positive and negative output voltage linear regulators. For experimental power inputs the LM338 chip which is an adjustable linear regulator is used. The complete schematic of the circuit is presented in Appendix B; and the PCB layout data is presented in Appendix D.

Designing a switching power supply using an adjustable switch-mode IC could save some space with respect to the linear supply. However there would be an additional noise source other than the main converter in the switch-mode power supply case. Mixing the noises of two circuits may result in predicting wrong results about the second order effects of the main converter. To obtain clearer ideas about the second order effects caused by the main converter, a linear power supply which does not generate high frequency noise is preferred.

### 4.3 Applications on Power-Pole Board

The power-pole board is based on the transitive relations between the topologies. As previously explained in section 4.1, five basic topologies can be implemented using the power-pole board. All of these topologies can be derived from buck converter topology by following the step by step procedure. For that reason to provide a better understanding of the power-pole board first, the topological relations between the converters will be examined in this section. After that the applications on the power-pole board will be explained and the resulting waveforms will be presented. The simulation results will also be used whenever they are considered to be useful.

#### 4.3.1 Topological Relations

In a DC/DC converter the load and the output capacitor can be modeled as a voltage source. Considering the basic non-isolated topologies and the single output isolated topologies, it can be claimed that a basic topology requires two voltage source. Using this approach the buck converter topology is redrawn again in Figure 4.8.

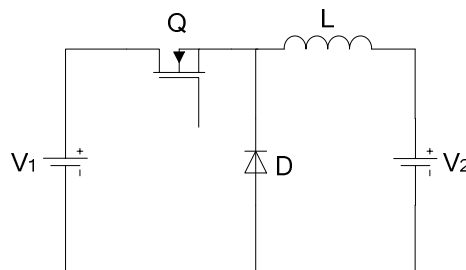


Figure 4.8 Buck converter model with two voltage source.

Modeling the output voltage source as a dependent source may be a more appropriate representation; however the purpose here is to clarify the topological

resemblances not to obtain a circuit model. Since this is a buck converter, the input voltage must be higher than the output voltage ( $V_1 > V_2$ ). Now, when the power flow is reversed, that means  $V_2$  is input and  $V_1$  is output, then the circuit operates in a way that the lower voltage at the input is stepped up to a higher level at the output. The boost converter is obtained. For easier control purpose, the controlled switch can be taken to the input side which requires a low side drive circuitry. Now it is clear that buck and boost converters share the same topology with different direction of power flow. Figure 4.8 is redrawn in Figure 4.9 revealing the topological relation.

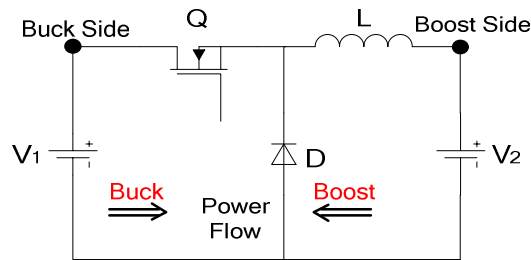


Figure 4.9. The topological relation of buck and boost converters.

As seen in Figure 4.9, if the power flow is from high voltage side to low voltage side, the topology is a buck converter, otherwise it is a boost converter. The buck and boost input terminals are also marked and named in Figure 4.9. Along with the boost converter, buck-boost converter can also be obtained using same topology. It is originally derived cascading the buck and boost converters and removing the redundant elements. However, the same topology is obtained by following this method. To obtain the buck-boost converter, simply the input voltage is connected between buck and boost terminals to control both bucking and boosting functions as shown in Figure 4.10.

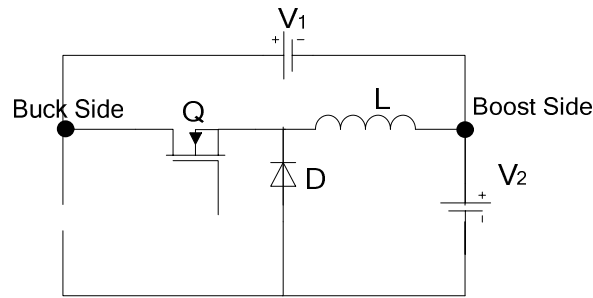


Figure 4.10 The topological relation of buck-boost converter.

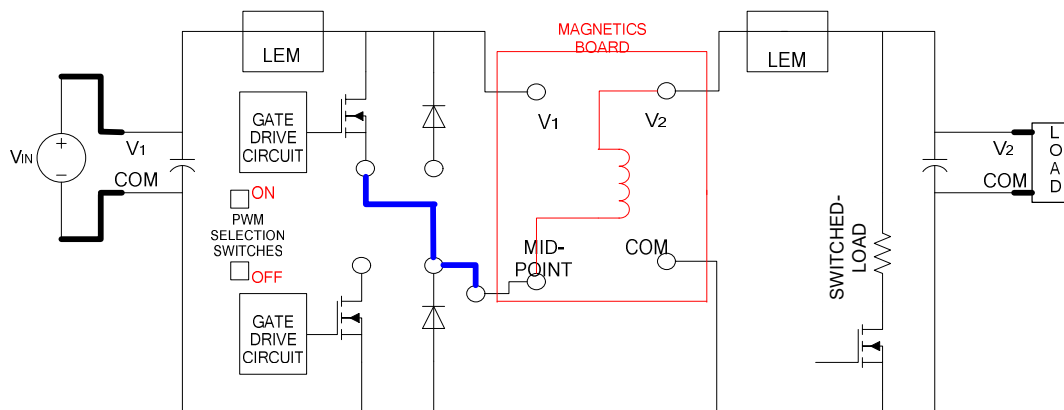
The three non-isolated topologies are derived. Now the flyback converter which is a buck-boost derived converter; and the forward converter which is again a buck derived converter will be introduced.

The secondary side of a forward converter is the same with a buck converter if the secondary windings are considered as a voltage source. When the voltage source and the output side is distinguished by a transformer, the buck converter becomes forward converter. MOSFET is taken to the low side again for gate drive simplicity and another diode takes the duty of the MOSFET in the output side.

The flyback converter is derived from buck-boost converter by replacing the inductor by a flyback transformer. MOSFET is again carried to the low side of the primary circuit for gate requirements. The secondary polarity is reversed to overcome the negative polarity problem of buck-boost converter.

### 4.3.2 Buck Converter Results

Buck converter includes a high side MOSFET and low side diode as the switch. The magnetic element of the boost converter is an inductor. Therefore, the inductor board will be used as the magnetic board. The power-pole board connection is shown in Figure 4.11.



The upper mechanical switch is turned on to deliver the PWM signal to the high-side gate drive IC. The frequency is adjusted to 100 kHz by using the trimpot of the PWM controller. The input voltage is 15V and the load resistor is 10 $\Omega$ . The inductor and the output capacitor values are 100 $\mu$ H and 680 $\mu$ F. The first measurements are taken at 100 kHz of switching frequency. However, before presenting the measurement results as waveforms, discussing the measurement conditions will be useful. The scope used for the measurements were an Agilent 54624A mixed signal 4 channel 100MHz oscilloscope. The bandwidth of the differential probe was 25MHz however, the differential probe is only used for the measurements of terminals having floating voltages. Ground referenced measurements were always taken using the original Agilent probe. The inductor currents were measured as voltages sensed by the LEM Hall-effect sensors. The bandwidth for these sensors is 200 kHz. Hence, the accuracy of the measurements should be evaluated according to these measurement conditions. Now the measured waveforms can be presented. The first measured waveforms is one of the important features of a DC/DC converter: The inductor current ripple. At four different duty cycle values, the inductor current ripple measurements are shown in Figure 4.12.



The measurements prove the non-linearity of the inductor current against duty cycle. The current ripple does not increase linearly with the increase of duty cycle. In the buck converter maximum inductor current ripple is obtained at 50% duty cycle [1].

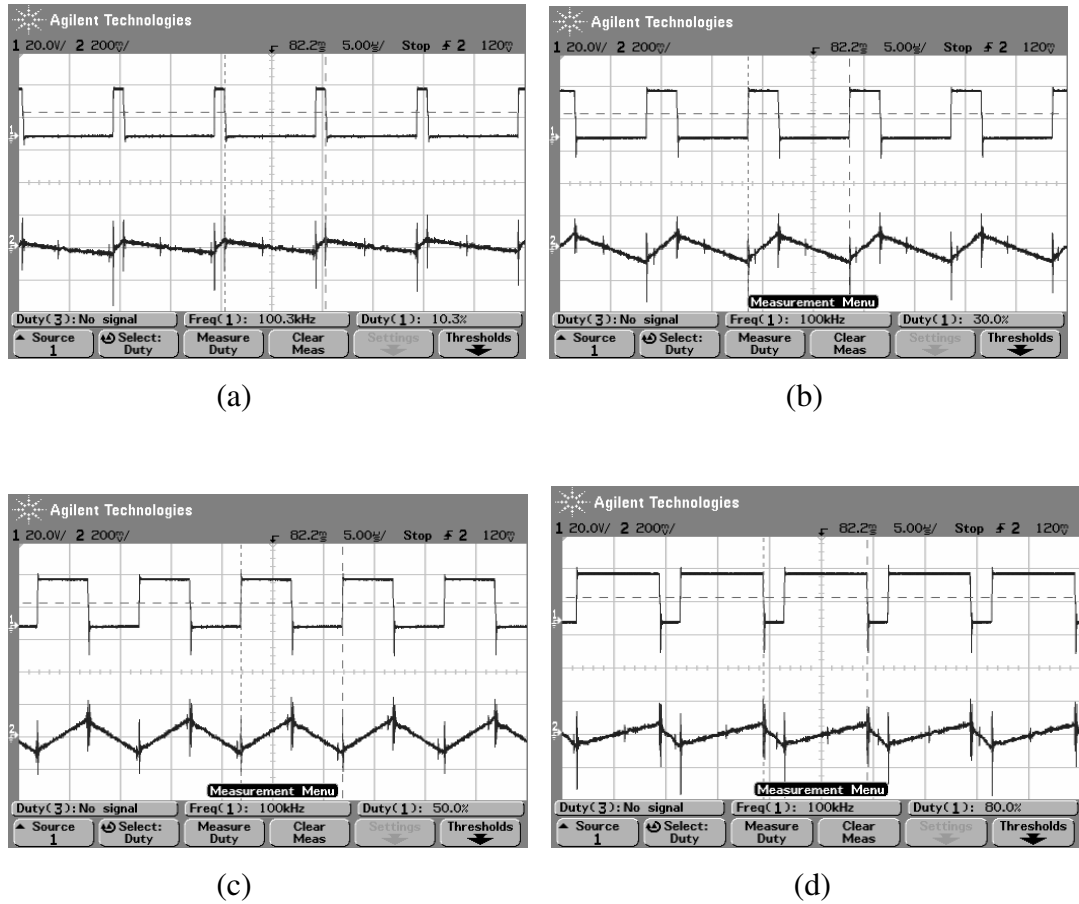


Figure 4.12 Inductor current ripple (bottom, 400mA/div ) for different duty cycles(top, 20V/div): (a) D=10%; (b) D=30%; (c) D=50%; (d) D=80%.

The output voltage ripple is quite related with inductor current ripple. The measurements on output voltage ripple are shown in Figure 4.13.

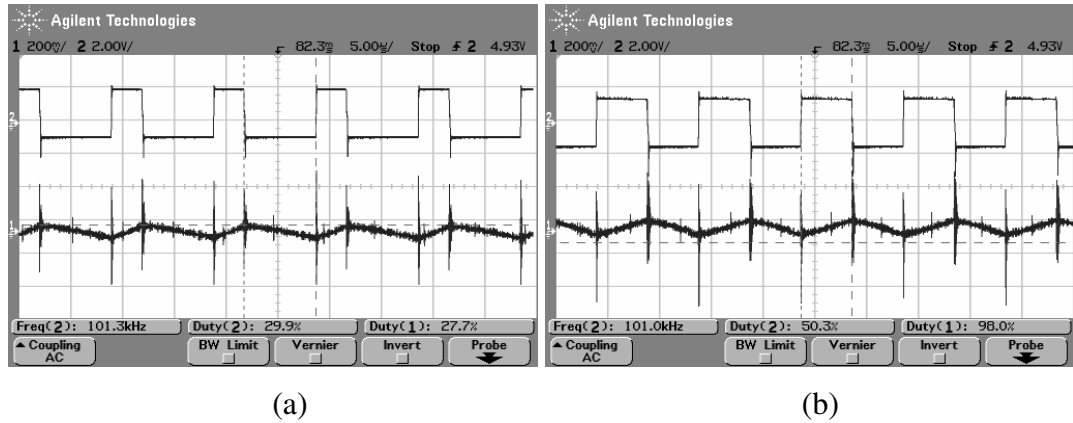


Figure 4.13 The output voltage ripple(bottom, 200mV/div) for different duty cycles (20V/div): (a) at 30% duty cycle; (b) at 50% duty cycle.

The switching dynamics are shown in Figure 4.14, both at MOSFET and diode turn-ons. This proves the relation of the output voltage ripple with the AC component of the inductor current. The AC component is amplified by the ESR of the capacitor and appears as the voltage ripple.

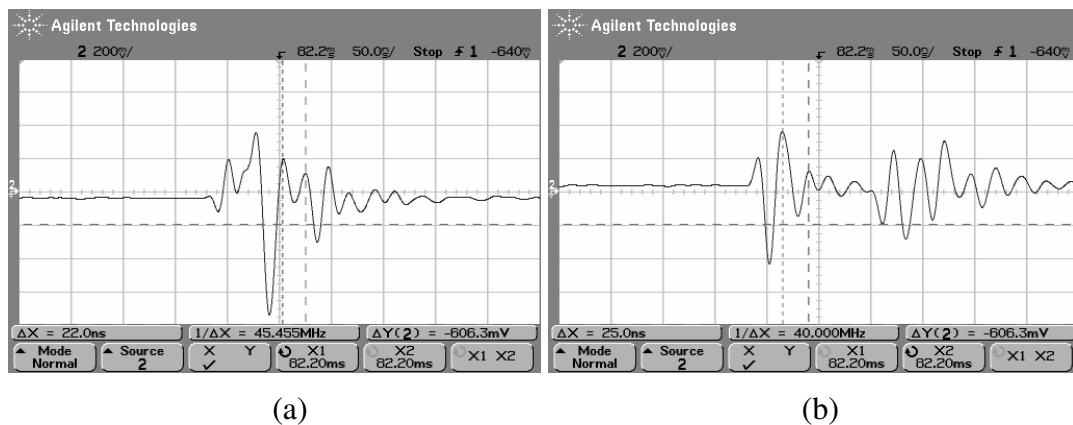


Figure 4.14 The output voltage ripple during switching transients: (a) during MOSFET turn-on; (b) during MOSFET turn-off (scale: 200mV/div).

The DCM waveforms of the buck converter are shown in Figure 4.15. In the figure, the inductor current ripple and drain-source voltage of MOSFET is examined.

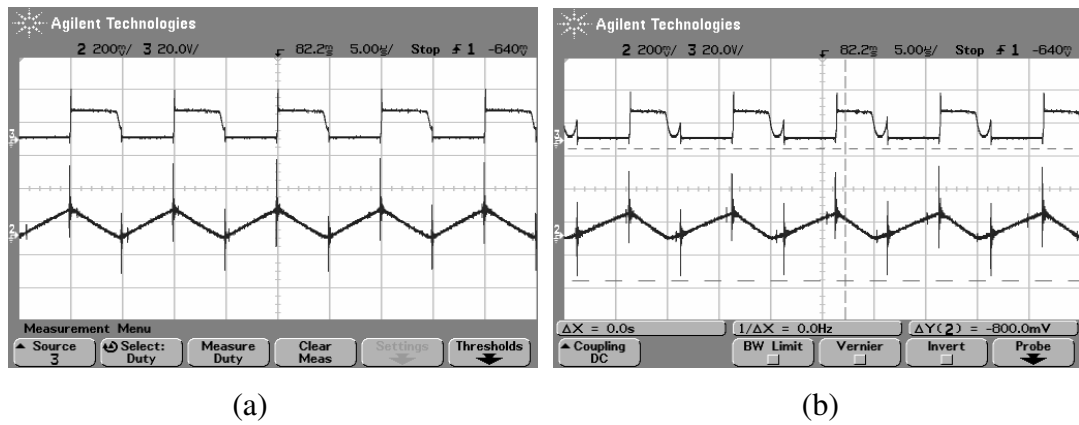


Figure 4.15 MOSFET drain-source voltage (top, 20V/div) and inductor current (bottom, 400mA/div) DCM operation of buck converter: (a) very beginning of the operation  $R_{LOAD}=48\Omega$ ; (b) the load is increased to  $R_{LOAD}=65\Omega$ .

To see the effects of the frequency on the inductor current ripple as the switching frequency is decreased to 65 kHz and to 30 kHz. The resulting inductor current at 50% duty cycle is shown in Figure 4.16.

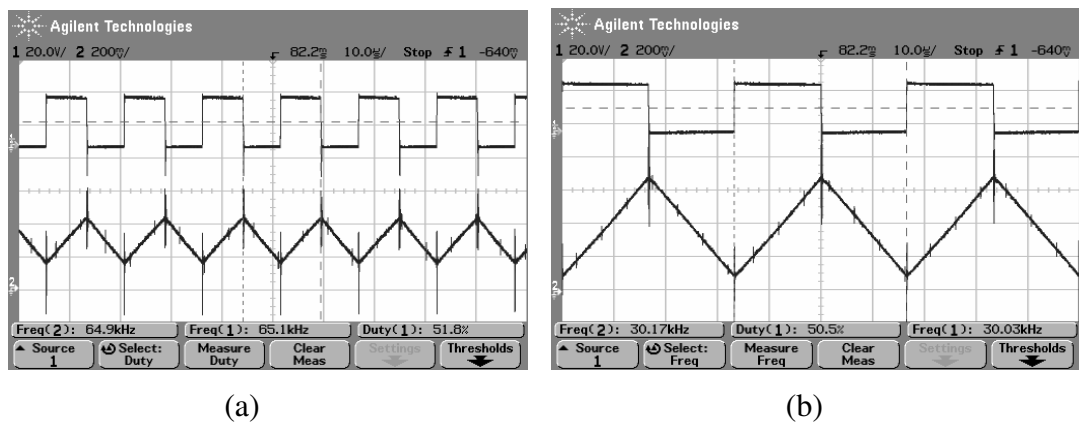


Figure 4.16 The inductor current ripple(bottom, 400mA/div) at 50% duty cycle(top, 20V/div) (a) at 65 kHz; (b) at 30 kHz.

It can be observed that as the frequency is decreased the inductor current ripple increases. After that point the load is increased at 65 kHz and 30 kHz to observe the DCM operation at this frequency. The result is shown as switch voltage and inductor current in Figure 4.17.

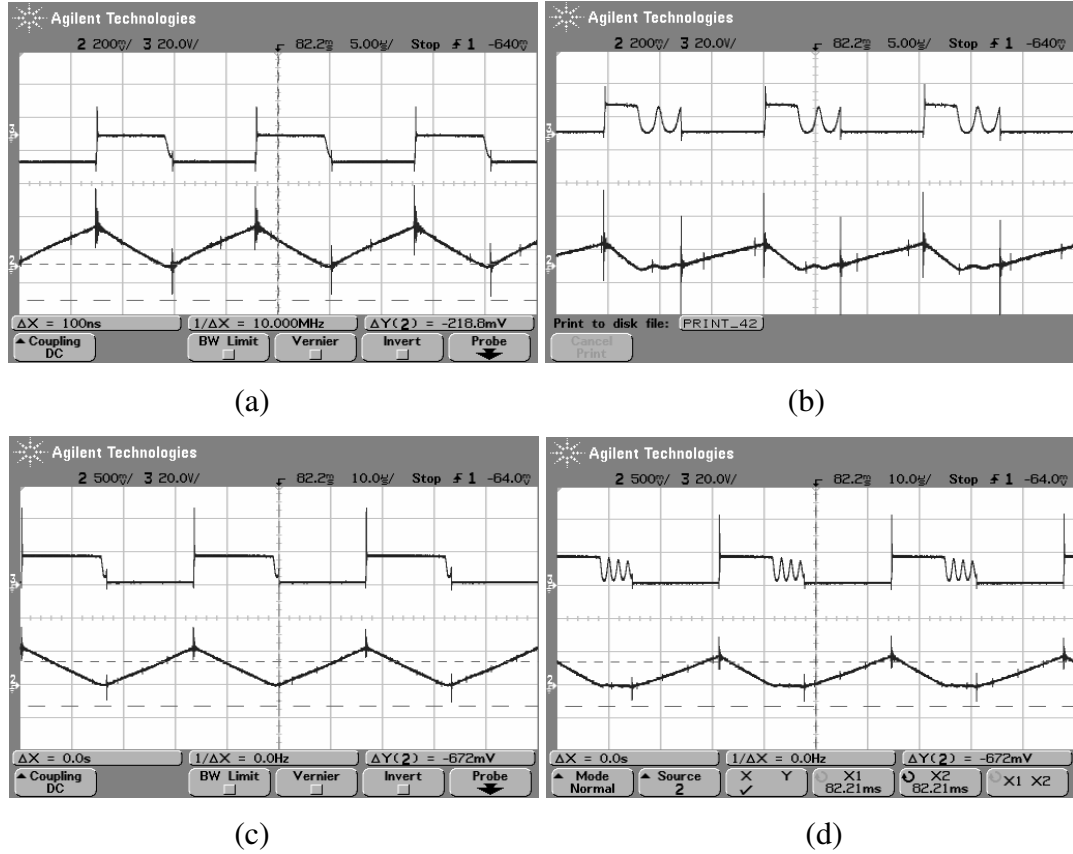


Figure 4.17. MOSFET drain-source voltage(top, 20V/div), inductor current(bottom, 400mA/div for (a) and (b), 1A/div for (c) and (d)) at DCM operation: (a) at 65 kHz the beginning of DCM  $R_{LOAD}=40\Omega$ ; (b) at 65 kHz  $R_{LOAD}=85\Omega$ ; (c) at 30 kHz the beginning of DCM  $R_{LOAD}=13\Omega$ ; (d) at 30 kHz  $R_{LOAD}=23\Omega$ .

It is clear that, since the current ripple is increased as the frequency decreases, the converter goes into DCM in lower load resistance values at lower frequencies. At the end of the buck section, the output voltage is recorded for different duty cycles with a step of 0.1. The theoretical and practical results are shown in Figure 4.18 in a graphical representation.

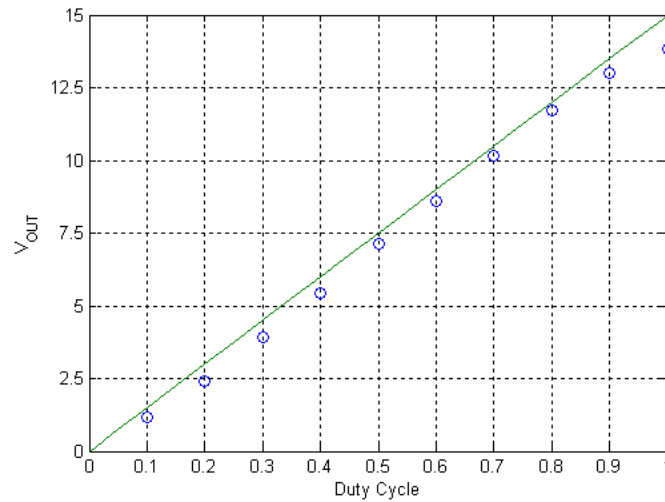


Figure 4.18 Duty cycle output voltage relation of buck converter.

The line represents the theoretical results, and the measurements are shown point by point. It is clear that the linear DC transfer characteristic of buck converter is provided however, there is some offset between theoretical and practical values. The offset is caused by the non-idealities of the components but mostly by the MOSFET and diode on-state voltage drops.

### 4.3.3 Boost Converter Results

As explained in section 4.3.1, boost converter is the dual of the buck converter. Hence, the connection of the buck converter will be reversed to obtain the boost converter. The connection diagram of the boost converter is shown in Figure 4.19.

The input voltage is 10V and the load resistor is adjusted as  $50\Omega$ . This time the lower PWM switch is set to on state to deliver the PWM signal to the lower gate drive. The inductor current ripple duty cycle relation is crucial in boost converter as well. As in the buck converter stage the maximum current ripple occurs at 50% duty cycle. The results on inductor current at different duty cycles are shown in

Figure 4.20. The waveforms of Figure 4.20 verify that the maximum inductor current ripple occurs at 50% duty cycle.

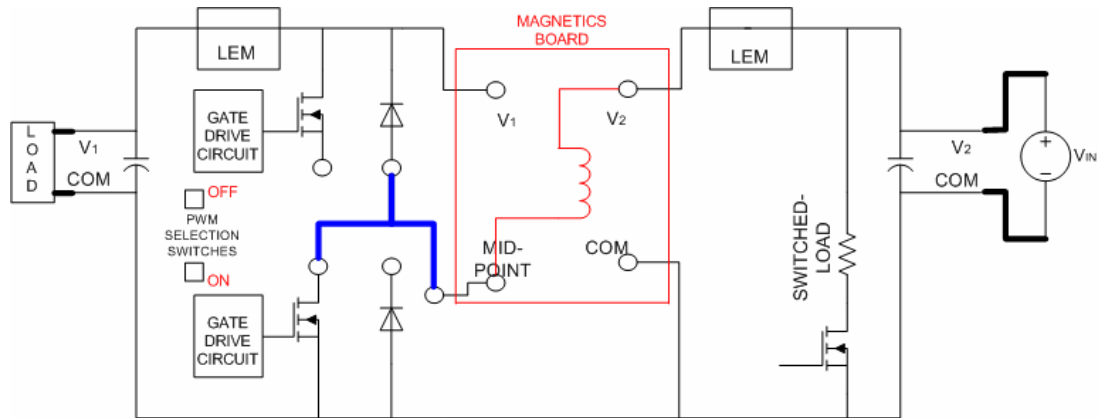
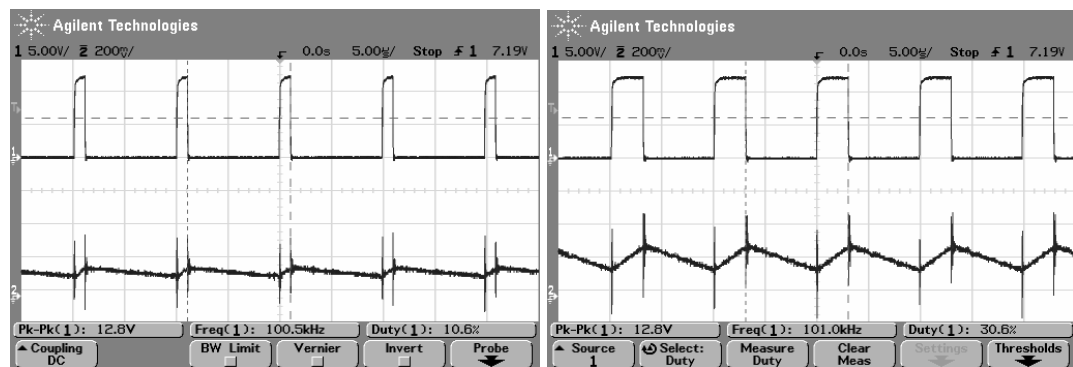


Figure 4.19 The connection diagram of power-pole board for the boost converter.

When the results are compared to the buck converter, it can be seen that the frequency of oscillation at diode turn-on at the buck converter is closer to the frequency of oscillation at MOSFET turn-on at the boost converter and vice versa. This can be another proof of that; the oscillations are caused by the PCB parasitics of power-pole board. At the buck converter topology the diode is the low side switch, and at the boost converter MOSFET is the low side switch. Since in the power-pole configuration, the path for the low-side switches are the same, the parasitic components are the same for buck diode turn-on and boost MOSFET turn-on. The output voltage ripple of boost converter is shown in Figure 4.21.



(a)

(b)

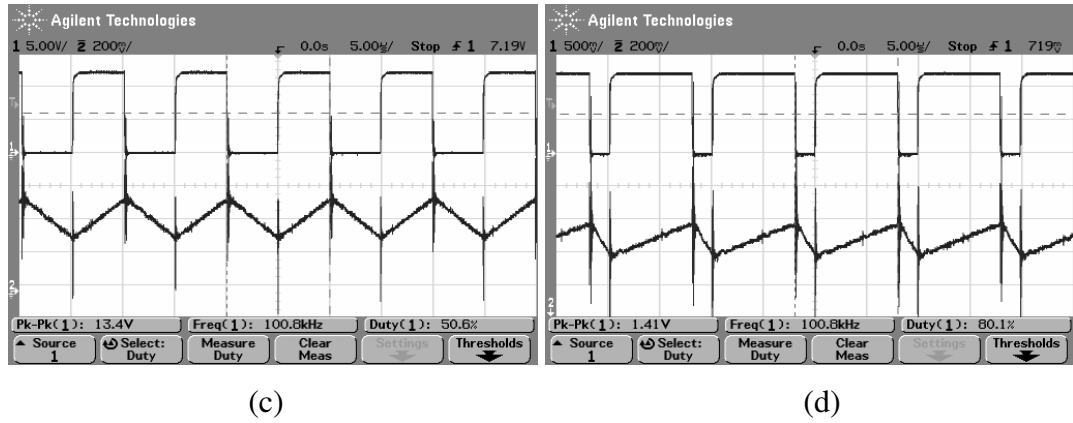


Figure 4.20 Boost converter inductor current ripple (bottom, 400mA/div) at different duty cycles (top, 5V/div): (a) at 10%; (b) at 30%; (c) at 50%; (d) at 80%.

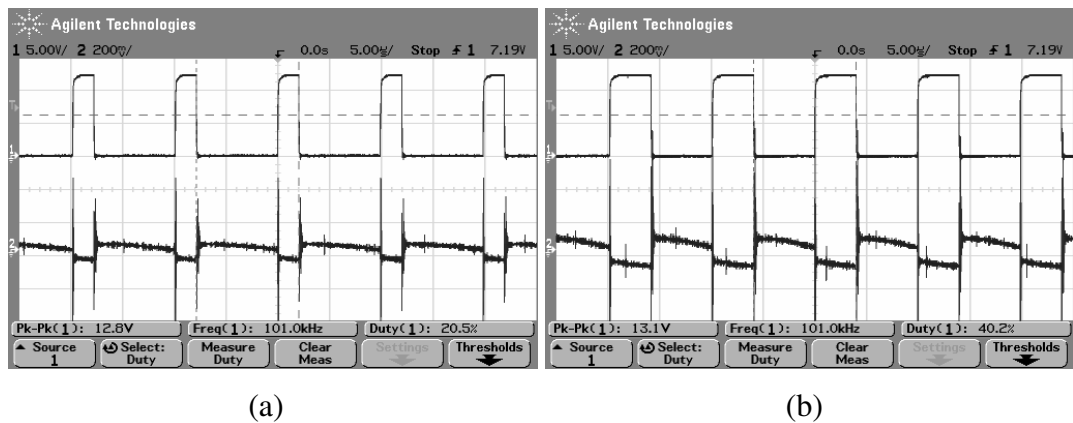


Figure 4.21 Boost converter output voltage ripple (bottom, 200mV/div) for different duty cycles (top 5V/div): (a) at 20% duty cycle; (b) at 50% duty cycle.

In the buck converter the output voltage ripple was directly a function of inductor current ripple since the inductor is at the output side and never disconnected from the load. In the boost converter, when the inductor is storing energy in mode-1 the output current is provided by the output capacitor. Thus, the decreasing waveform of output capacitor is observed at the output in mode-1.

In the boost converter circuit, the DCM mode can not be observed at 100 kHz at the maximum available load resistor value used in the experiments which is 100 $\Omega$ . For that reason the discontinuous conduction mode is observed by decreasing the frequency to 30 kHz. The DCM waveforms at 30 kHz are shown in Figure 4.22. In the figure the inductor current and MOSFET voltage are presented. A more detailed representation for DCM is shown in Figure 4.23. The oscillation seen in the Figure 4.23 has a low frequency in comparison to switching dynamics. This relatively low frequency component is due to MOSFET capacitance and stray capacitances of PCB resonating with the main inductor of the circuit. As the final step different output voltage measurements are taken to compose a representation on duty cycle to output voltage. The result is shown in Figure 4.24. It is clearly seen in the figure that the theoretical output voltage levels are not possible and boost converter can not step up the voltage until 100% duty cycle. After a specific point the output voltage starts to decrease because of the losses caused by the excessive currents. The losses can be caused by the resistor of the inductor and in the semiconductors of the converter.

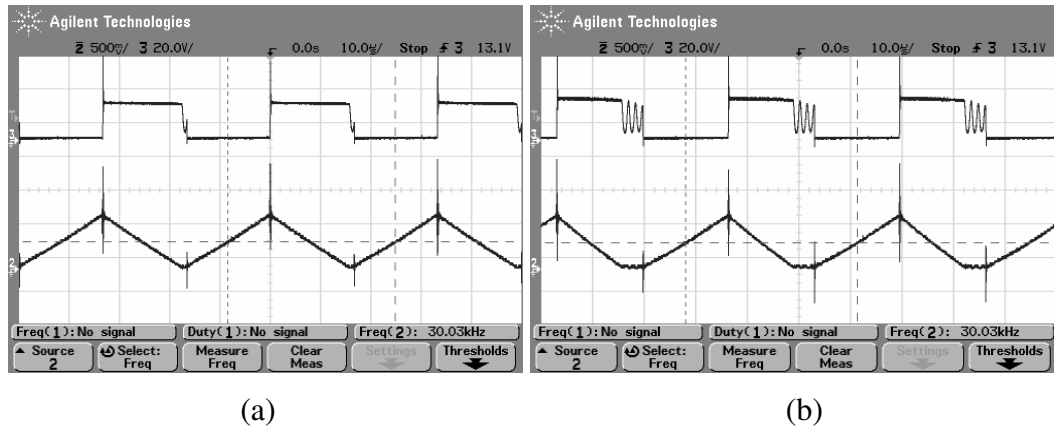


Figure 4.22 The MOSFET drain-source voltage (top, 20V/div) and the inductor current (bottom, 1A/div) for DCM at 30 kHz: (a) at 57 $\Omega$ ; (b) at 80 $\Omega$ .



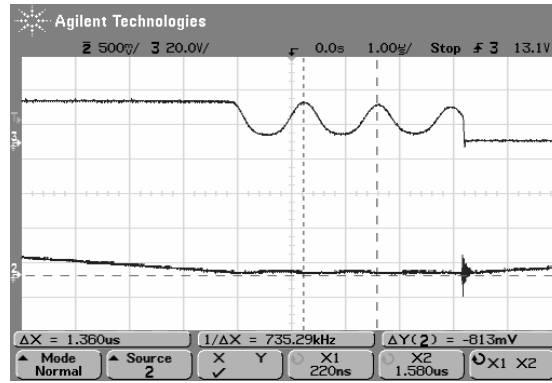


Figure 4.23 The oscillation of switch voltage (20V/div) and the inductor current (1A/div) in DCM.

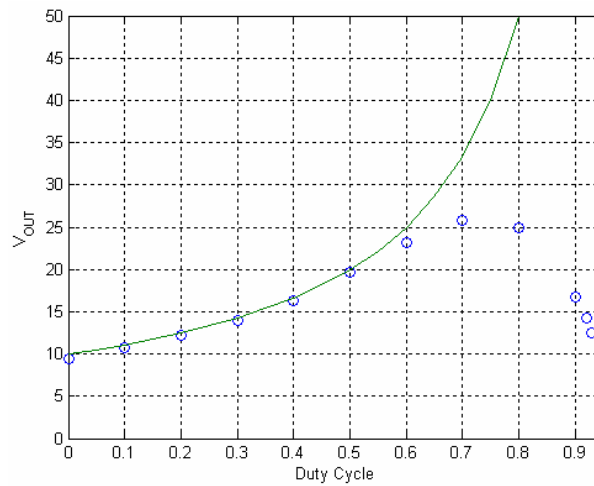


Figure 4.24 The duty cycle and output voltage relation for boost converter.

#### 4.3.4 Buck-Boost Converter Results

In the buck-boost converter, the connection on power-pole board is different from the other 4 topologies. As presented earlier, the two positive terminals of the power-pole board should be connected to each other. The magnetic board is the same inductor board again. The connection diagram is shown in Figure 4.25.

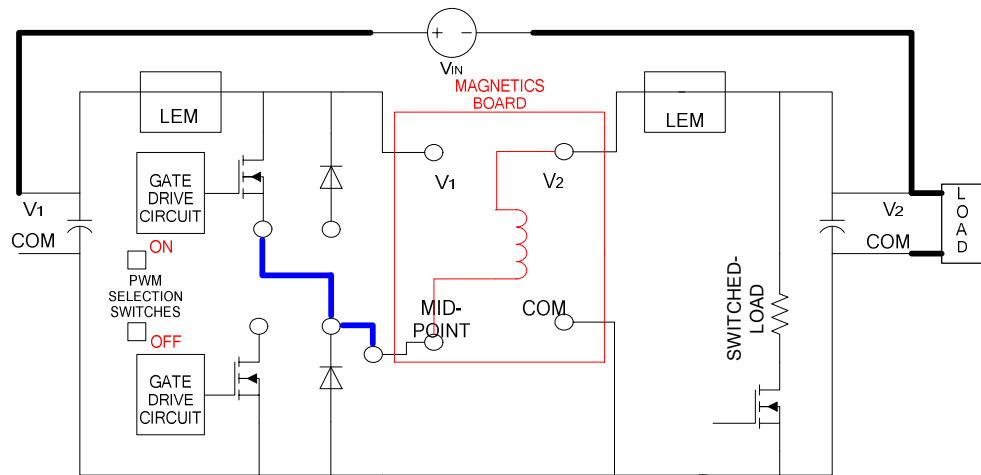
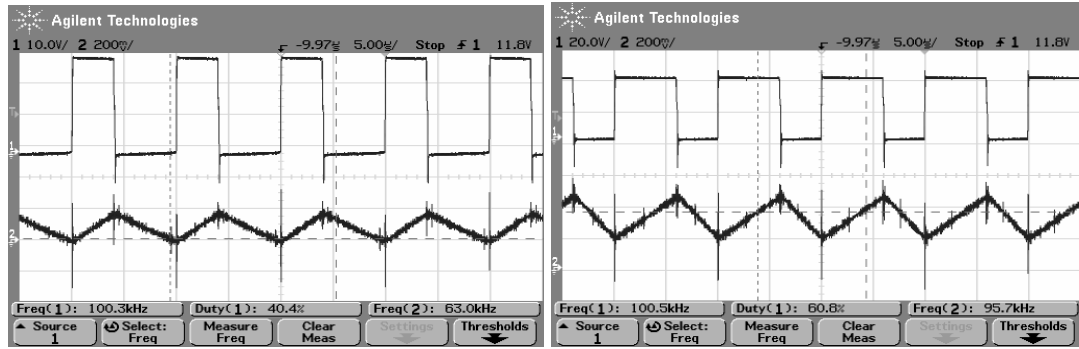


Figure 4.25 The connection diagram of power-pole board for the buck-boost converter.

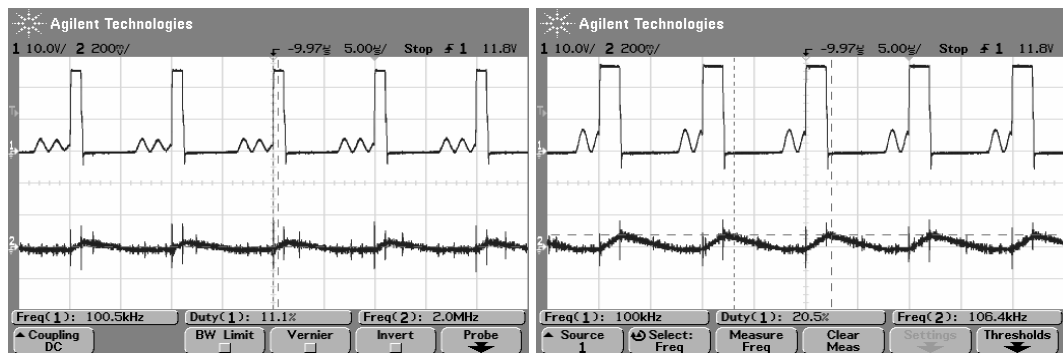
The load resistance is set to  $30\Omega$  and the input voltage is adjusted to 10V. Since the upper MOSFET is utilized in buck-boost converter, the upper PWM selection switch is set to on state again. The measurements are initiated with the inductor current again and the results for the inductor current ripple are shown in Figure 4.26 at two different duty cycles. A buck-boost converter operates at the buck mode until the duty cycle reaches to 50% value. Therefore, at low values of duty cycles the output voltage and, hence the average current becomes low. For that reason the converter may enter into the DCM at low duty cycles. The effects of this situation are shown as gate-source voltage and inductor current ripple in Figure 4.27.



(a)

(b)

Figure 4.26 The inductor current ripple (bottom, 400mA/div ) of buck-boost converter for different duty cycles (top, 10V/div for (a), 20V/div for (b)): (a) for 40% duty cycle; (b) for 60% duty cycle.



(a)

(b)

Figure 4.27 MOSFET gate-source voltage and inductor current discontinuity at low duty cycles: (a) 10% duty cycle; (b) 20% duty cycle (scales 10V/div, 200mV/div).

The figures show the oscillation at gate-source voltage. As a corollary, in the design process of a converter a duty-cycle range should be defined for a specific load range to guarantee whether CCM or DCM operation. That is because the converter may not provide CCM operation in all duty cycle range. The output voltage stage of buck-boost converter exhibits a different character with respect to the direct converters. In order to verify this behavior the simulation circuit and the resulting output voltage ripple of the simulation is shown in Figure 4.28.

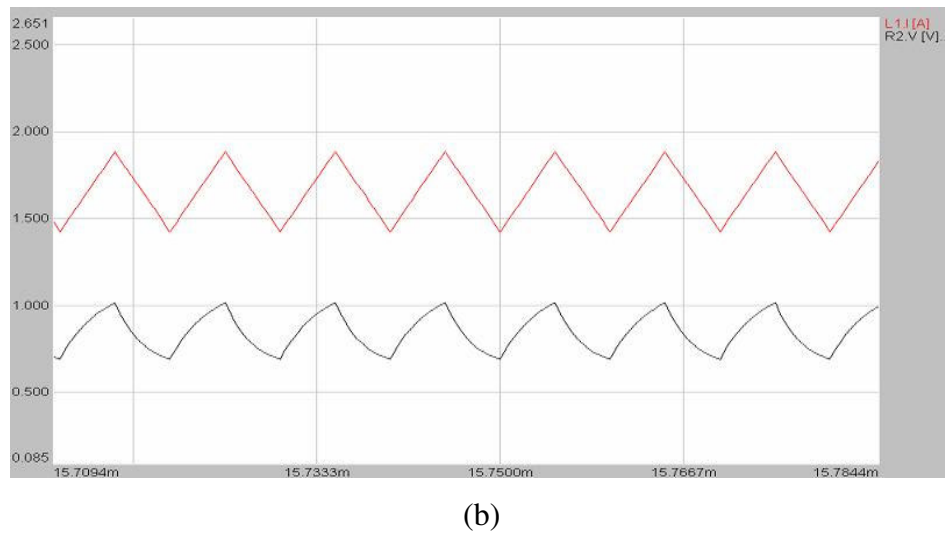
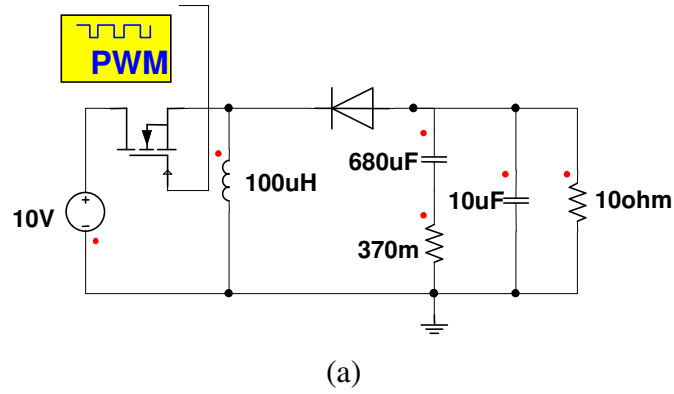


Figure 4.28 The buck-boost converter simulation: (a) circuit diagram; (b) inductor current ripple waveform (top) and output voltage ripple waveform(bottom) at 50% duty cycle.

As seen on the simulation results, the buck-boost converter output stage integrates the current. The waveform that is obtained from the power-pole board is shown in Figure 4.29. The DCM of buck-boost converter can be observed at 40% duty cycle. The result for 100 kHz and 65 kHz are illustrated in Figure 4.30.

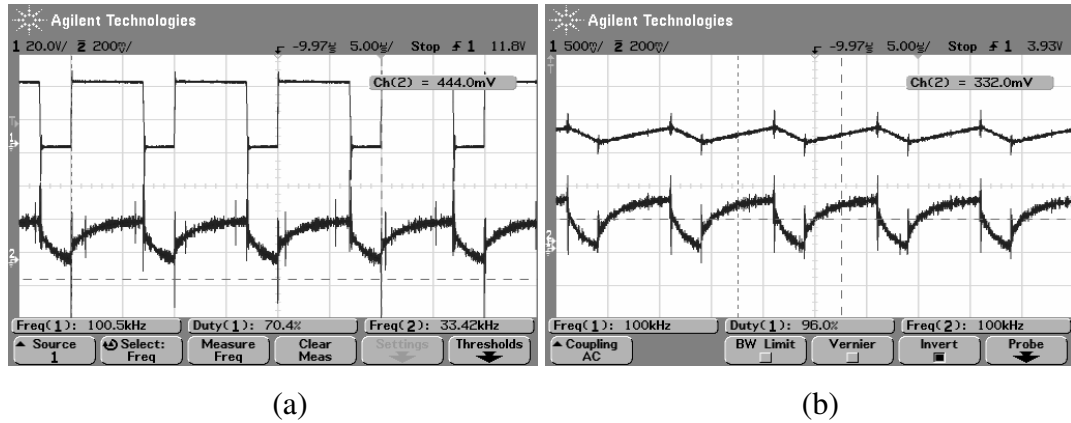


Figure 4.29 Buck-boost converter waveforms for 70% duty cycle; (a): duty cycle (top, 20V/div) and output voltage ripple (bottom, 200mV/div); (b) inductor current ripple (top, 1A/div) and output voltage ripple (bottom, 200mV/div).

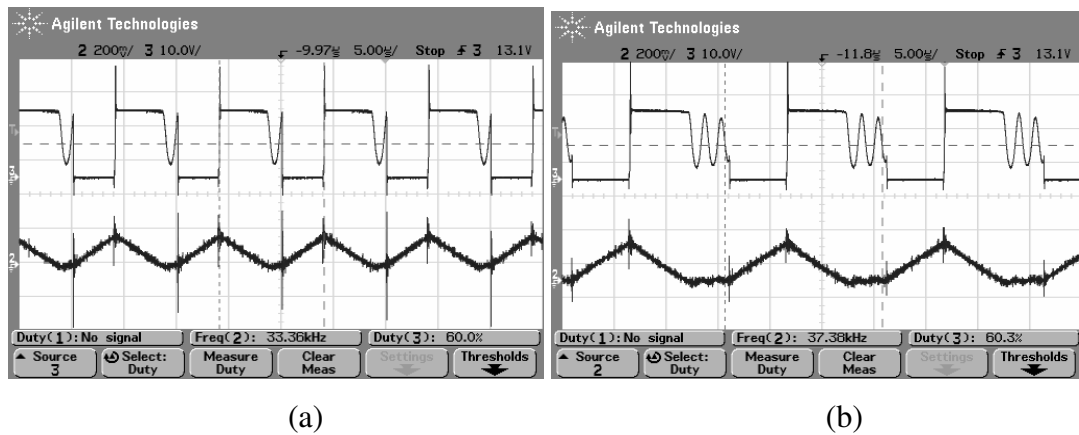


Figure 4.30 MOSFET drain-source voltage (top, 10V/div) and inductor current (bottom, 400mA/div) at DCM of buck-boost converter for 95Ω load resistance: (a) at 100 kHz; (b) at 65 kHz.

As the final step, buck boost converter duty-cycle to output characterization graph is plotted by measuring output voltage for nine different duty cycle values. The result is shown in Figure 4.31. The buck–boost converter exhibits a similar characteristic with the boost converter. The output voltage cannot be increased after

70% duty cycle because of the losses caused by the overstresses on the converter circuit. The practical results are as expected and coincides with the curves in [1] and [13].

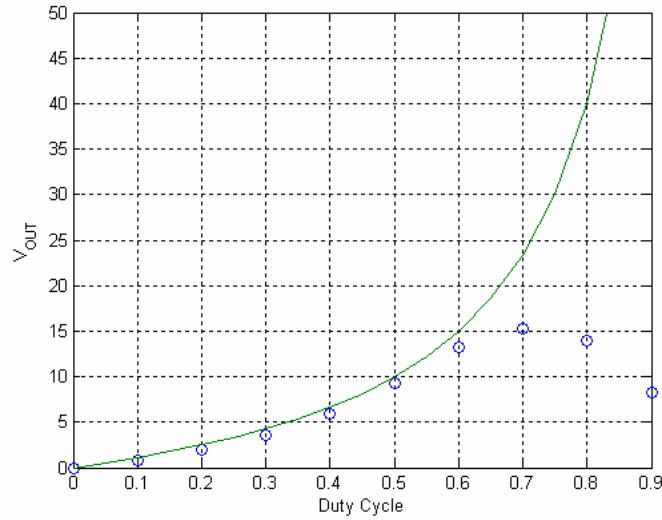


Figure 4.31 The DC input to output voltage characterization of buck boost converter.

#### 4.3.5 Flyback Converter Results

In the flyback converter, the flyback magnetic board is plugged in. Since the diode is at the secondary side of the circuit, the primary side only utilizes a low side switch. The connection diagram for flyback converter is shown in Figure 4.32. In the schematic only the topological components are shown however in the actual magnetics board a snubber is included to damp the oscillations caused by the leakage inductance of the flyback transformer. Therefore, before presenting the flyback converter results the design of the flyback transformer will be discussed. For the transformer core, EE25 type ferrite core is chosen which is suitable for 10-20W applications. However there are a few types of EE25 core and EE25E is the type that is used. The EE25E core dimensions are shown in Figure 4.33.



the equivalent of these two legs is in series with the center gap reluctance. Hence if the center gap reluctance is  $R$ , the equivalent reluctance is equal to  $2R$ . Using equation (3.7) the primary turn number can be calculated. Maximum current ripple is chosen as  $0.5A$  and maximum flux swing is chosen as  $0.15T$ . Substituting these values in equation (3.7) primary turns number is found as 25. The total reluctance can be found using equation (3.8). This reluctance value is the equivalent reluctance described above. Hence, the reluctance of the center gap is equal to the half of the calculated reluctance. Using the conventional reluctance equation given in (3.9) the air gap length can be calculated as  $0.0524mm$ . This value is too low to implement. For that reason the air gap should be increased by increasing the turn number to keep the inductance value constant. The relation between the turn number and air gap size is given below. This ratio keeps the desired inductance value constant. The desired air gap size is chosen as  $0.2\text{ mm}$  which is an appropriate value for implementation.

$$\frac{l_{g1}}{l_{g2}} = \frac{N_1^2}{N_2^2} \quad (4.1)$$

$$\frac{0.0524}{0.2} = \frac{25^2}{N^2} \quad \text{The new turn number is found as } N=48 \text{ turns.}$$

Changing the turn number, decreases the maximum flux swing in the core since the inductance and maximum current swing is unchanged as well. By means of changing the turn number and air gap size, the physical operating point of the core is changed.

As previously mentioned, the flyback magnetics board includes an RCD clamp snubber. Figure 4.34 reveals the primary voltage of the flyback converter without snubber. It is clear that the leakage inductance causes high frequency oscillations. Hence, the circuit requires an RCD clamping snubber. The values of the resistor and capacitor can be easily calculated. The leakage inductance of the transformer can be estimated as 10% of its main inductance value since the transformer is



wounded and assembled by hand. Hence the leakage inductance is assumed as  $37\mu\text{H}$ . The worst case can be thought as the peak current is flowing through the leakage inductance. In this case the total energy stored can be calculated from well-known inductor energy equation. The result is  $41,5 \times 10^{-6}$  Joule. By multiplying this value with the switching frequency the power that the snubber will dissipate in its worst case can be obtained which is equal to  $4,15\text{W}$ . The clamp voltage is chosen as 10 volts. Using these two values, the resistor value can be found as  $24\Omega$ . This is the minimum resistance value required. Any higher resistance value will result a less lossy circuit. The capacitance value can be chosen to provide a RC time constant that is much greater than the switching time period. Now the flyback converter results will be presented. In Figure 4.34 the primary and the secondary voltage is shown at two different duty cycles.

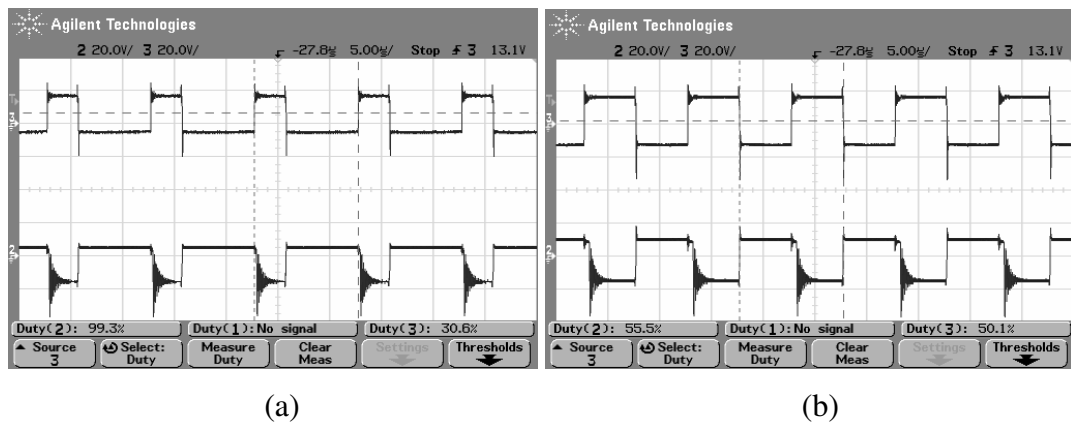


Figure 4.34 The primary (top, 20V/div) and the secondary (bottom, 20V/div) voltage waveforms of flyback converter: (a) at 30% duty cycle; (b) at 50% duty cycle.

The oscillation at the secondary side is caused by the diode reverse recovery and the secondary leakage inductor. To damp the oscillation an RC snubber can be placed for the diode. Figure 4.35 shows waveforms with the snubber across diode. The output current ripple of a flyback converter is limited by the secondary inductance of the flyback converter. Figure 4.36 shows the primary voltage and the output current.

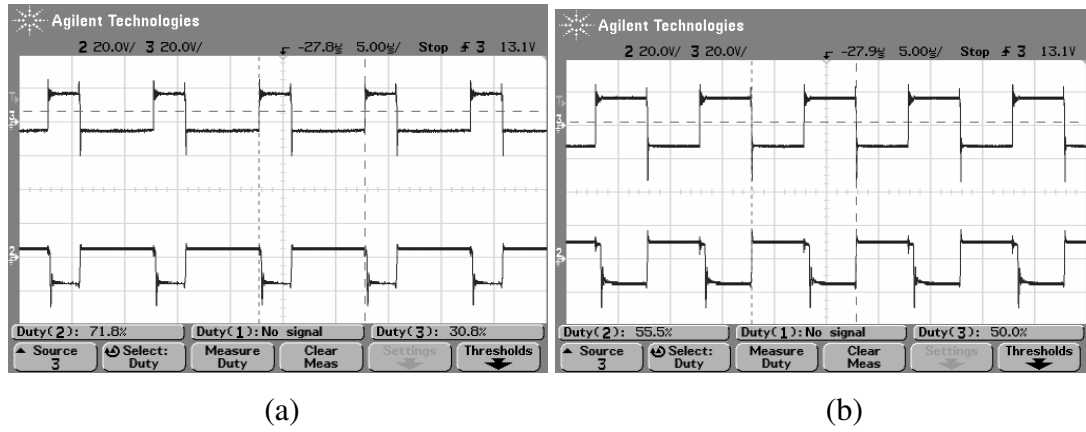


Figure 4.35 Primary (top, 20V/div) and secondary (bottom, 20V/div) voltage waveforms with output diode snubber: (a) at 30% duty cycle; (b) at 50% duty cycle.

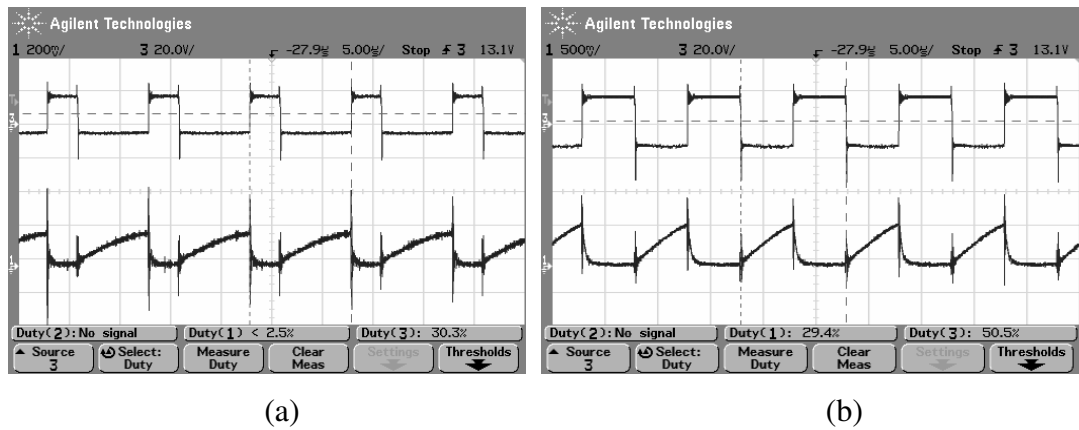


Figure 4.36 Primary voltage (top, 20V/div) and the output current (bottom, 400mA/div for (a), 1A/div for (b)) of flyback converter: (a) at 30% duty cycle; (b) at 50% duty cycle.

Since the flyback converter is a buck-boost derived converter the output current does not have linear relation with duty cycle. Starting from the 50% duty cycle, the output current may increase to excessive values causing the increase of losses. Therefore the flyback converters are generally operated around 50% duty cycle with a maximum of 60% duty cycle. The input current waveform is shown in Figure 4.37. The rate of rise of the input current is limited by the primary inductance. It is

seen in Figure 4.37 that the duty cycle increases two times its value, the input current increases approximately five times of its value at this operating point. One of the important issues of the flyback converter is the device stress caused by the voltage spikes. Figure 4.38 shows the MOSFET drain-source voltage.

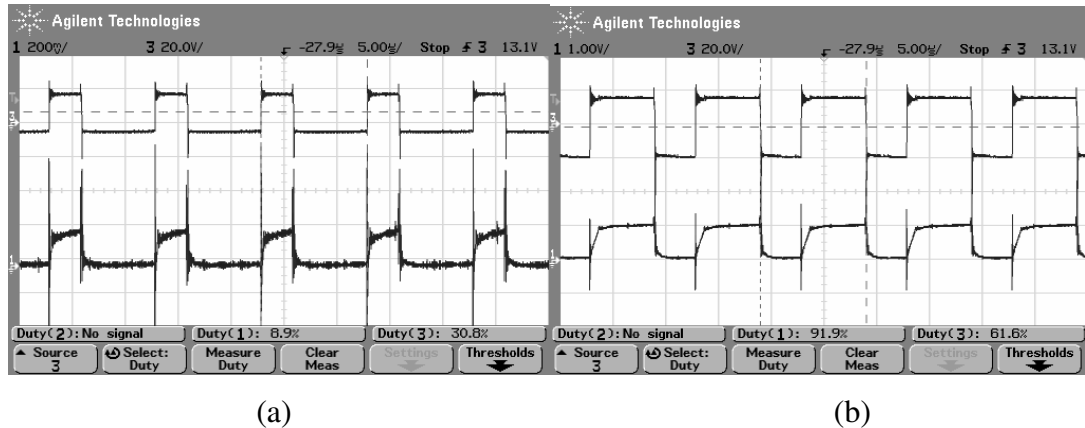


Figure 4.37 Primary voltage (top, 20V/div) and primary current (bottom, 400mA/div for (a), 1A/div for (b)) waveforms: (a) at 30% duty cycle; (b) at 60 % duty cycle.

It is clear that the voltage peak can reach to the 4 times to the applied voltage which is 15V. The device stress is too much in comparison to the buck converter because of the leakage inductance of the flyback transformer which increases  $L di/dt$  spikes. The increase of the inductance causes the oscillation frequency to decrease. As shown in Figure 4.38 (b) the oscillation frequency is about 8-9 MHz which is a low value with respect to the 40 MHz level switching transients of buck converter.

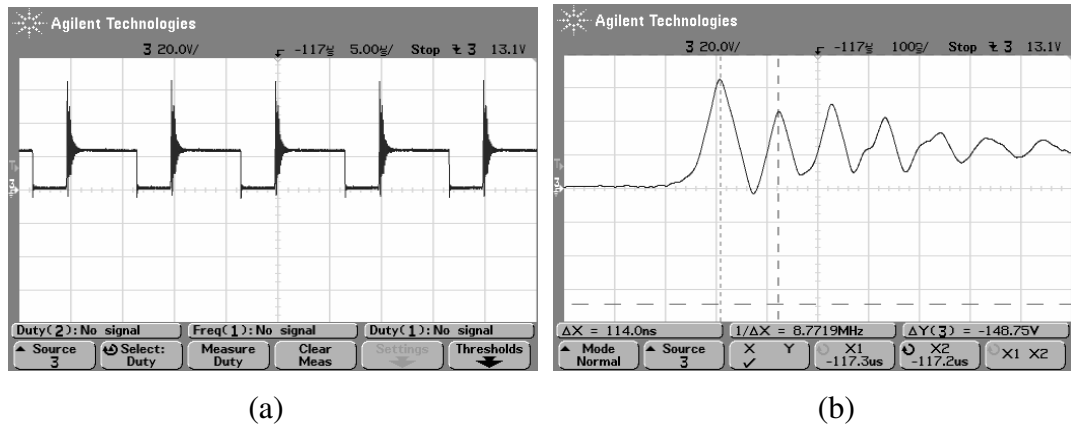


Figure 4.38 MOSFET drain-source voltage at the flyback operation (20V/div): (a) for 5μs/div; (b) for 100ns/div.

As the final step the dc voltage transfer characteristic of the flyback converter is shown in Figure 4.39. The input voltage is 15V and the transformer is constructed to have a 1:1 turns ratio. Since the flyback converter switches to the boost mode after 50% duty cycle, the current and hence the losses increase too much over this duty cycle value. Therefore, the flyback converters are not operated over 50% duty cycle. Figure 4.39 demonstrates the deviation of output voltage from the theoretical curve after 50% duty cycle.

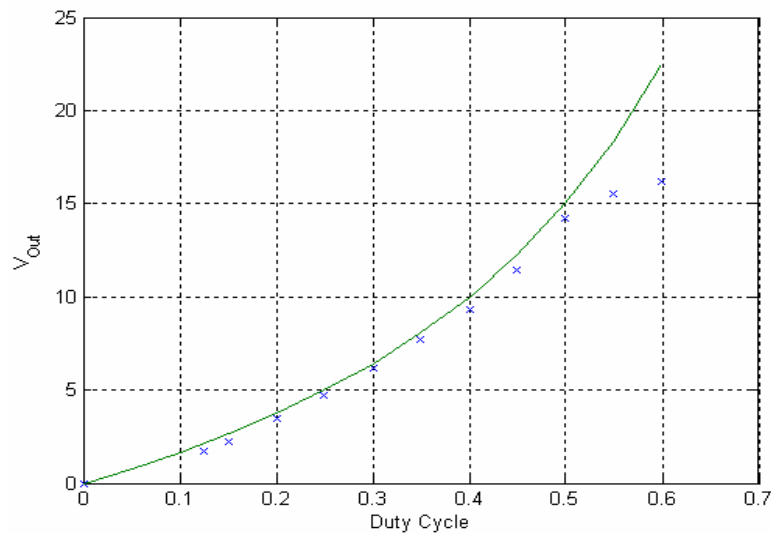


Figure 4.39 DC voltage transfer characteristic of the flyback converter.

### 4.3.6 Forward Converter Results

In the forward converter, a different magnetic board is used, as shown in Figure 4.40. The primary side of the forward converter is the same as the flyback converter and only the lower MOSFET is utilized. Hence the lower PWM switch must be set as active. Since the forward converter transformer does not have an inductor characteristic as flyback converter, an external output inductor exists in topology. In the magnetic board circuit, only topological componenets are shown discarding the RCD snubber circuit. There is also the tertiary winding of the flyback converter which is not shown in the diagram.

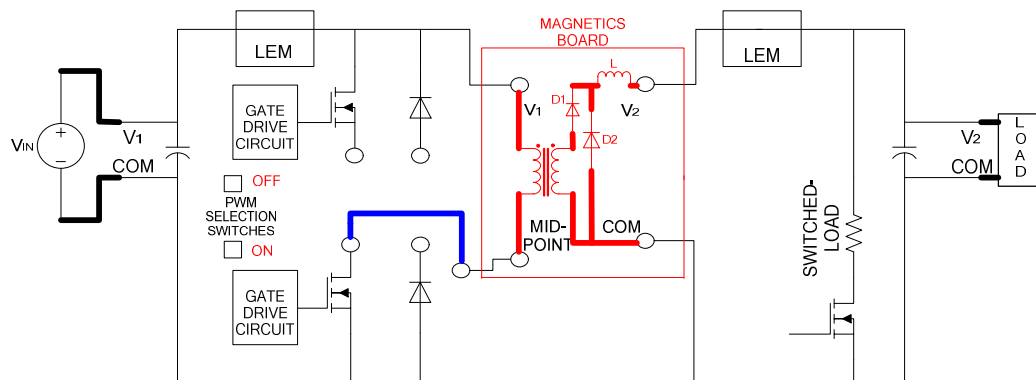


Figure 4.40 The connection diagram of power-pole board for forward converter.

The transformer design of the forward converter is based on the equations 3.10, 3.11, and 3.12. The maximum duty cycle can be found using equation 3.10. By selecting  $N_1=N_3$ ,  $D_{MAX}$  is calculated as 0,5. The primary and secondary winding ratio is arbitrarily chosen as  $N_1:N_2=1:1,5$ . The core type is the same as the flyback core type which is shown in Figure 4.33. Now the number of primary turns can be calculated using equation 3.12.  $B_{MAX}$  is chosen as 0,15T again and the nominal value of the input voltage is 15V. By substituting these values into equation 3.12 the primary turns number is found as 10. Hence the secondary winding becomes 15, and the tertiary winding becomes 10 turns. After determining the transformer turns numbers, last step is to determine the snubber parameters for leakage inductance.

The primary inductance is measure as  $57\mu\text{H}$ . As the worst case 10% of primary inductance  $5\mu\text{H}$  leakage inductance is adopted. Maximum DC current in  $D_{\text{MAX}}$  is about 1.1A. Once more, as a worst case value, 1,5A of current is taken for the calculations. The inductor energy and the corresponding power dissipation are calculated. The worst case power dissipation is 0,563W. For example, for a 5V of clamping voltage results  $44\Omega$  resistor however in application high resistor value created problem about energy transfer process in the flyback mode. The problem is solved by decreasing the resistor value. This may be caused by the error on the prediction of leakage inductance or the interaction of tertiary winding with primary during flyback period. After completing the snubber design, the forward converter results can be presented. Since the duty cycle is restricted to 50%, the measurements are taken under this duty cycle value. Figure 4.41 shows the primary and the secondary voltages of the forward converter. The secondary voltage transients exhibit a quite oscillatory behavior since in both two modes of the secondary side the current is carried by the diodes. Therefore the diode interacts with the transformer leakage as shown in the flyback converter operation. These oscillations can be damped by an RC snubber. When a snubber is added to the one of the diodes the results on Figure 4.42 is obtained. One of the advantages of the forward converter is the output inductor. This inductor filters the output current and prevents the pulsating structure. This reduces the EMI radiation and hence the noise coupling. The output inductor current with primary voltage is shown in Figure 4.43.

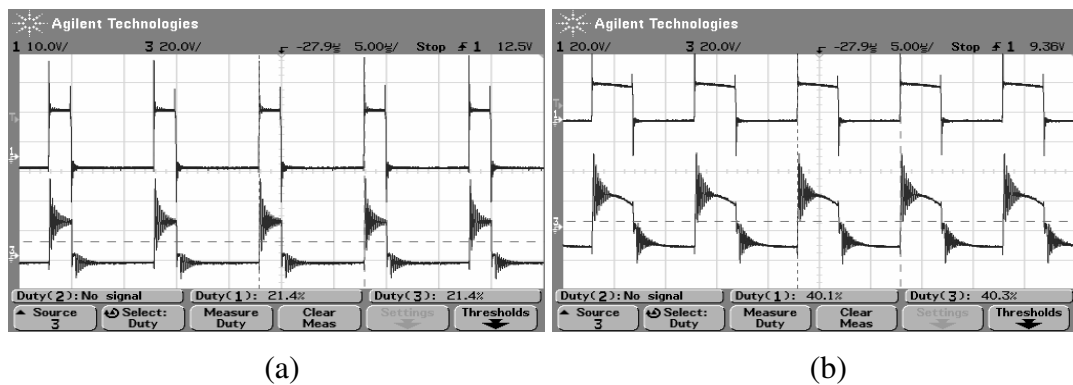


Figure 4.41 The primary voltage (top, 10V/div for (a) and 20V/div for (b)) and the secondary voltage of forward converter (bottom, 20V/div): (a) at 20 % duty cycle; (b) at 40% duty cycle.

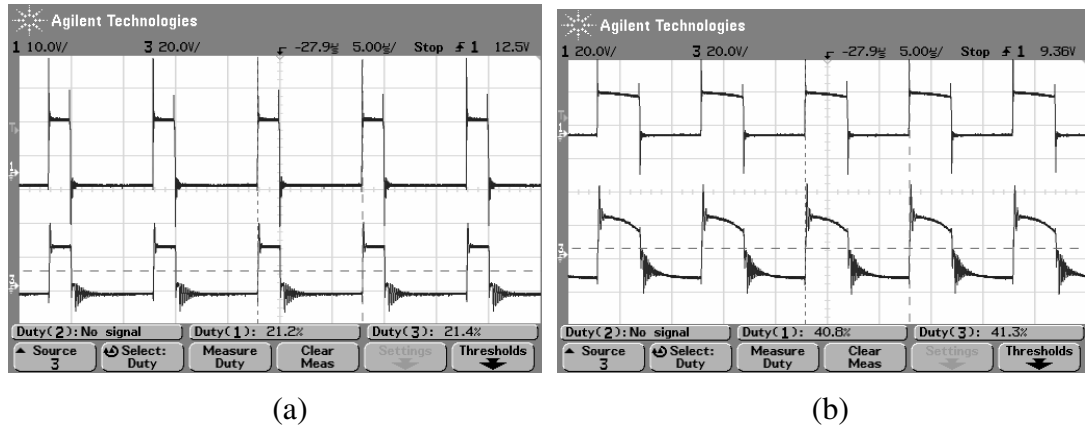


Figure 4.42 The primary voltage (top, 10V/div for (a) and 20V/div for (b)) and the secondary voltage (bottom, 20V/div) waveforms with one of the output diodes snubbed: (a) at 20% duty cycle; (b) at 40% duty cycle.

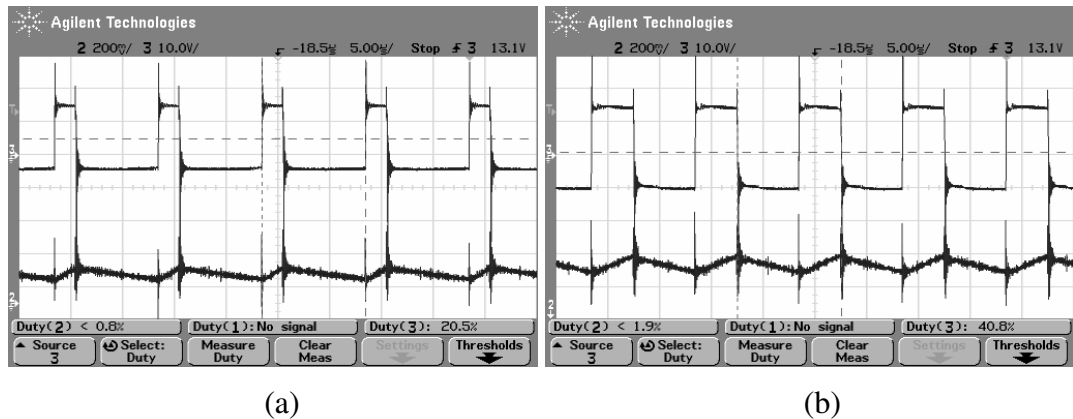


Figure 4.43 Primary voltage (top, 10V/div) and inductor current (400mA/div): (a) at 20% duty cycle; (b) 40% duty cycle.

As the final step, the DC voltage transfer characteristic of the forward converter is illustrated in Figure 4.44. The straight line illustrates the theoretical results of the forward converter. For the theoretical calculations the input voltage is taken as 15V and the turns ratio is 1:1.5. Since the transformer resetting cannot be supplied over 50 % duty cycle in forward converter, the theoretical values are recorded up to 40% duty cycle which is shown as “x” in the associated figure. The measured values seem to be higher than the theoretical values. The reason of this deviation is the error in the turns ratio from the specified theoretical value.

When the duty cycle reaches 40% the forward converter loss becomes visible since the output voltage value goes below the theoretical value despite the error in the turns ratio. For that reason the forward converters are operated at these maximum values (around 40% duty cycle) and the converter optimization is achieved by adjusting the turns ratios.

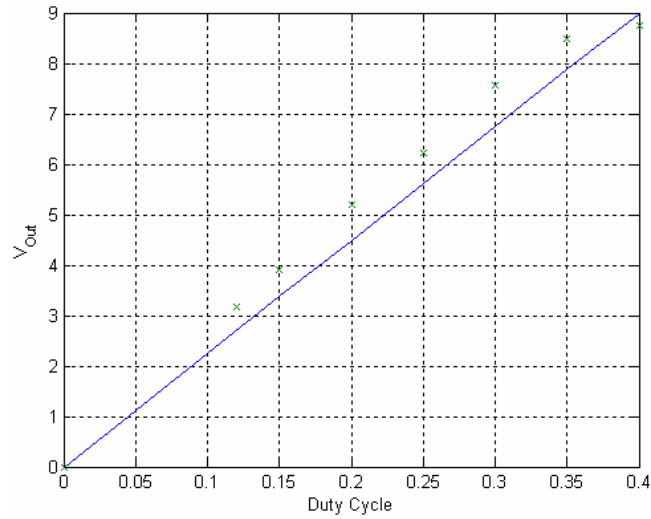


Figure 4.44 DC voltage transfer characteristic of forward converter.

#### 4.3.7 Voltage Mode Control Results

In this section, a single loop controller is designed with voltage feedback. The switched load on the power-pole board is used to emulate the load change. For the converter response a small-signal voltage injection pin is available on the board however, the controller design is made according to the theoretical representation of the system parameters. The parameter list is given in Table 4.1. All parameters are explained previously except the PWM modulator gain  $V_M$ .  $V_M$  is given as the difference between the peak and the valley values of the modulating ramp signal and can be obtained from the manufacturer's datasheet of any PWM controller.



Table 4.1 Buck converter parameters for controller design.

$R_{LOAD}$	10 $\Omega$	Load resistance
L	100 $\mu$ H	Filter inductance
C	690 $\mu$ F	Output capacitance
ESR	370m $\Omega$	Current measurement resistance in series with capacitor and equivalent series resistance of capacitor
$V_{IN}$	24V	Input voltage
$V_M$	1.8V	Modulator peak-to-valley voltage
D	0.5	DC operating point duty cycle
H	0.2	Feedback path gain

Using the Table 2.3. and equations (2.53) and (2.54) the following transfer functions can be obtained.

$$G_{vd} = \frac{0.006127s + 24}{7.155 \times 10^{-8}s^2 + 0.0002653s + 1} \quad (4.2)$$

$$G_{vi} = \frac{0.0001276s + 0.5}{7.155 \times 10^{-8}s^2 + 0.0002653s + 1} \quad (4.3)$$

The important quantity here is the overall loop gain which is formulated in (2.59). To see the uncompensated loop behavior, the controller transfer function  $G_C(s)$  is taken as 1. Thus, the uncompensated loop gain  $T(s)$  becomes

$$T(s) = \frac{0.002206s + 8.64}{7.155 \times 10^{-8}s^2 + 0.0002653s + 1} \quad (4.4)$$

The Bode diagram of  $T(s)$  is given in Figure 4.45. It is clear that the ESR zero provides a 90° phase lead and the loop phase yields to -90° which means a 90° positive phase margin. The open-loop gain crossover occurs at about 5kHz and this

value is adequate for closed-loop operation as well. To provide a good voltage regulation the loop gain must be large. Equation (2.60) states that the output voltage follows the reference correctly if the loop gain is sufficiently large. The relationship between the output voltage and the reference voltage depends on the quantity  $T/(1+T)$ . The Bode plot of this quantity is shown in Figure 4.46. It is obvious in Figure 4.46 that the absolute value of the magnitude is about 0.9. That means when a reference is applied to obtain 10 volts, the converter will output 9 volts because of the insufficient loop gain. Therefore the compensated loop gain must have larger value to provide the dc regulation. By placing a pole at  $s=0$  the loop gain can be improved. This pole will introduce an additional  $90^\circ$  phase lag, which results a  $180^\circ$  phase lag at crossover. To improve the phase margin a low frequency zero must be placed. As a design criterion, to improve the phase margin, the phase angle of the compensator is chosen as  $60^\circ$  at crossover frequency. By using equations (2.62) and (2.63) the zero and pole frequencies are determined as follows:

Table 4.2 Compensator pole, zero, and crossover frequency values.

$f_C$	5 kHz	Gain crossover frequency of closed-loop system
$f_Z$	1.33 kHz	Compensator zero frequency
$f_P$	18 kHz	Compensator pole frequency

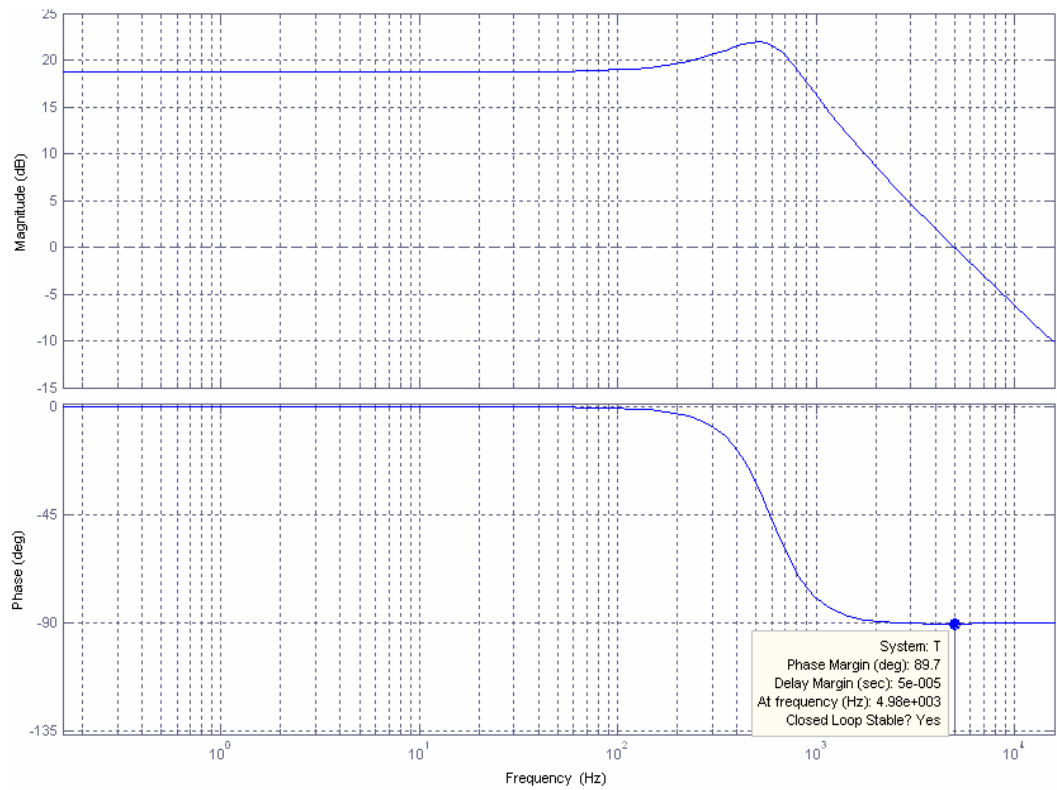


Figure 4.45 Bode diagram of the uncompensated loop gain.

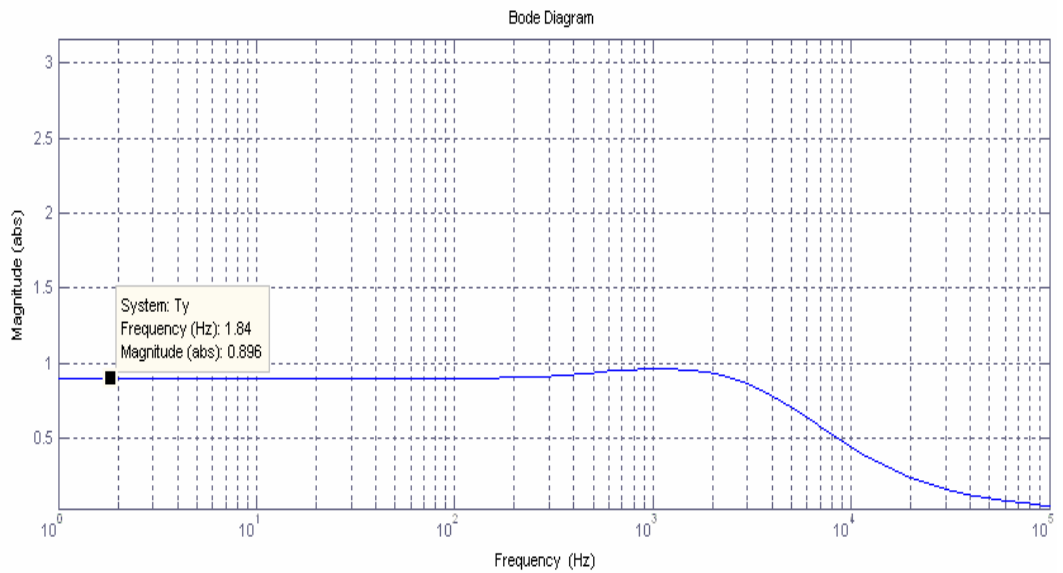


Figure 4.46 Bode diagram of the quantity  $T/(1+T)$ .

The transfer functions of compensator becomes

$$G_C(s) = G_{CO} \frac{1 + \frac{s}{w_Z}}{s(1 + \frac{s}{w_P})} \quad (4.5)$$

This transfer function can be implemented using type-II controller as introduced in section 2.4.3.2. The bode diagram of type-II controller is shown in Figure 2.27. Since the open loop crossover frequency is determined to remain unchanged, the mid-band gain of the compensator is chosen as 1 which is defined as  $R_2/R_1$ . Hence choosing an arbitrary resistor value of  $R_1=R_2=10K\Omega$ , the component values can be calculated. Using  $R_2$  value and the zero frequency,  $C_2$  is calculated as 12nF. Using  $R_2$ , pole frequency and  $C_2$ ,  $C_1$  is calculated as 954pF. For the implementation following standard component values are chosen.

Table 4.3 Compensator component values.

R1	10k $\Omega$	Input resistance
R2	10k $\Omega$	Zero resistance
C1	1nF	Pole capacitance
C2	10nF	Zero capacitance

By substituting the values in equation (2.68) the transfer function of the controller can be obtained as.

$$G_C(s) = \frac{10^5 s + 10^9}{s^2 + 1.1 \times 10^5 s} \quad (4.6)$$

The bode plot of the compensator is shown in Figure 4.47. As seen on the bode diagram, the gain around 5 kHz is close to 0dB and the phase angle around 5 kHz is  $-33^\circ$  which means a  $57^\circ$  of phase lead is provided by the controller as intended. By multiplying the equations of (4.4) and (4.6) the compensated loop gain  $T_C(s)$  can be obtained.

$$T_C(s) = \frac{220.6s^2 + 3.07 \times 10^6 s + 8.64 \times 10^9}{7.155 \times 10^{-8} s^4 + 0.008136 s^3 + 30.18 s^2 + 1.1 \times 10^5 s} \quad (4.7)$$

The bode plot of this compensated loop gain is shown in Figure 4.48. The bode plot reveals that phase margin is  $56^\circ$  approximately and the gain crossover occurs at 4.6 kHz. The low frequency gain is improved up to 100dB at DC level. The plot for the  $T_C/(1+T_C)$  quantity is shown in Figure 4.49. The gain is expressed in its absolute value not in dB. The plot shows that the low frequency gain of the quantity  $T_C/(1+T_C)$  is 1 which means there is sufficient loop gain for good DC regulation.

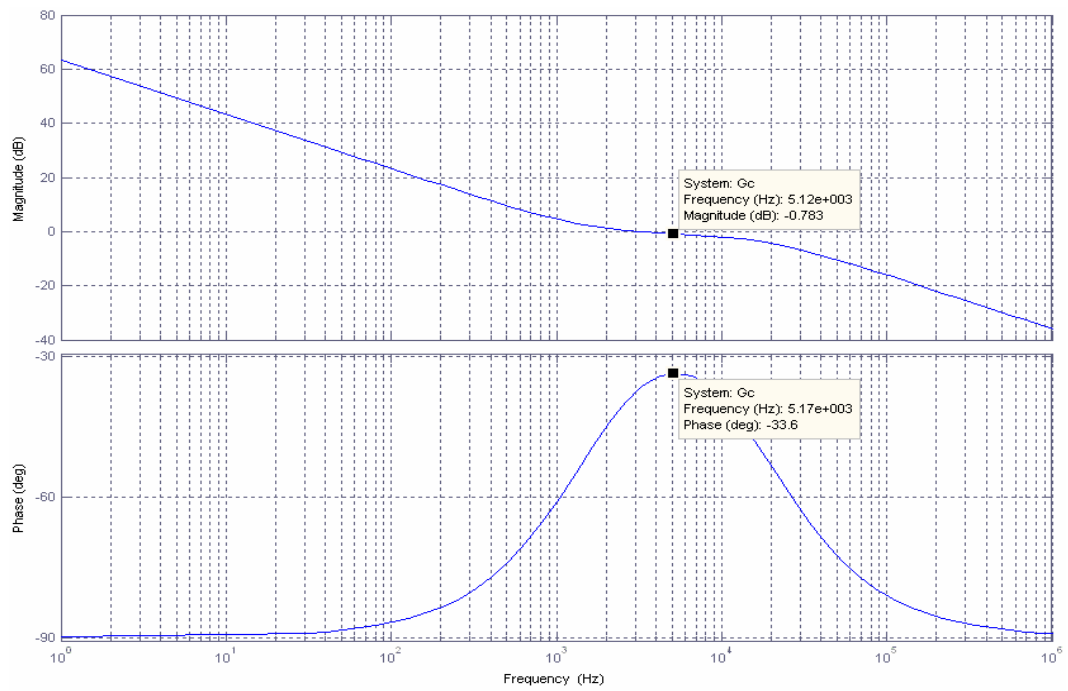


Figure 4.47 Bode plot of the compensator.

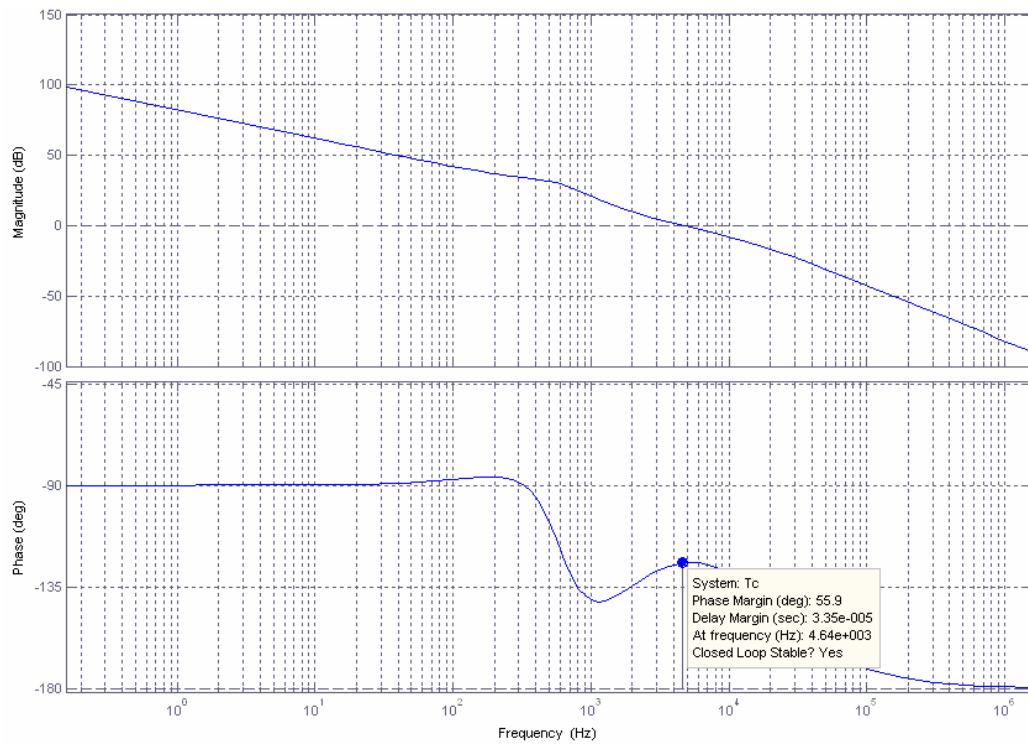


Figure 4.48 Bode plot of the compensated loop.

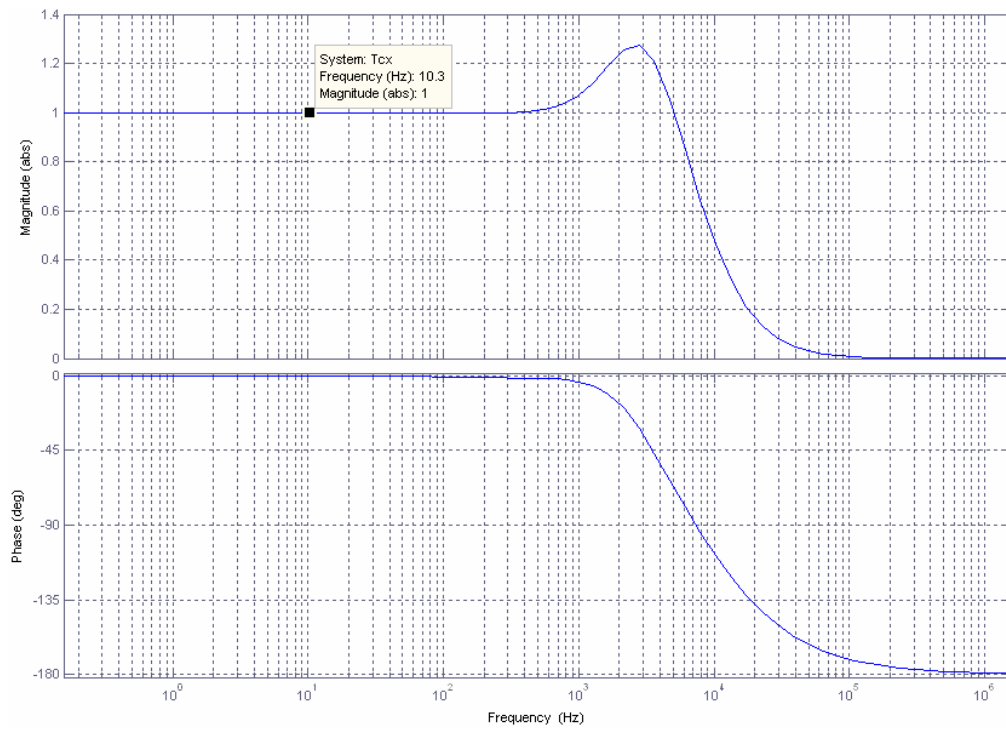


Figure 4.49 Bode plot of the quantity  $T_c/(1+T_c)$ .

After the theoretical design, these values are applied to the buck converter set up of the power pole board. The buck converter connections are the same as shown in Figure 4.11. However, the control selection jumper must be switched from open loop position to the closed-loop position. The control selection jumper is shown in the photo of the power pole board and presented in Appendix A with the further explanations. Now the type-II controller shown in Figure 4.50 can be connected using the daughter board connection pins. The numbers shown in the figure implies the number of terminals to be connected. The internal error amplifier of PWM controller is used in the voltage mode control. Therefore, no external component is required except from the discrete resistors and capacitors.

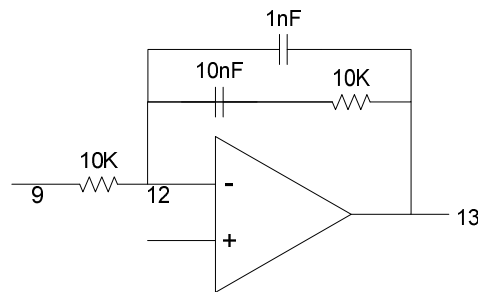


Figure 4.50 Type-II controller for the voltage mode control.

The inverting input which is the reference voltage input to the compensator is internally connected to the duty cycle pot. Hence the reference voltage can be applied using the duty cycle pot. Since the output voltage is brought into feedback amplifier as scaled to its 1/5 value, the reference value must be applied according to this feedback gain. If an external reference source is desired to be used, the reference input jumper which is again shown in Appendix A, should be changed. In this case the reference voltage can be applied to the pin 14 of the daughter board connection pins.

In order to observe the transients, the switched load will be used in this experiment. The switched-load is normally passive in the open-loop operation. By changing

switched-load jumper position, it can be set to active mode for closed-loop applications. The controller is tested under two different conditions. In the first condition the main load is  $10\Omega$  which means the system draws relatively high current. The Figure 4.51 reveals the effect of  $10\Omega$  switched-load on the output voltage in open-loop mode.

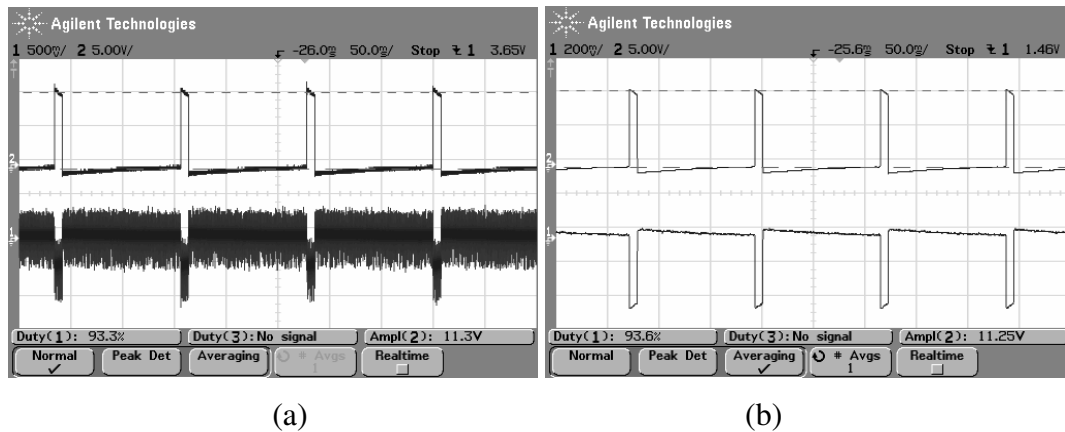


Figure 4.51 The switched-load pulses (top, 5V/div) and output voltage (bottom, 500mV/div for (a), 200mV/div for (b)) waveforms at open-loop operation: (a) at normal mode of the scope; (b) at averaging mode of the scope.

The waveforms are both observed at normal and averaged mode since the switched-load time period is quite large with respect to the output converter switching period. The averaged mode provides a clearer representation. The output voltage is 12V and the voltage sag is about 0.5V. When the jumpers are switched to the closed-loop mode and the output voltage is adjusted to 12V by setting the reference input to the 2.4V ( the voltage feedback is scaled to its 1/5 value), the waveforms of Figure 4.52 is obtained.



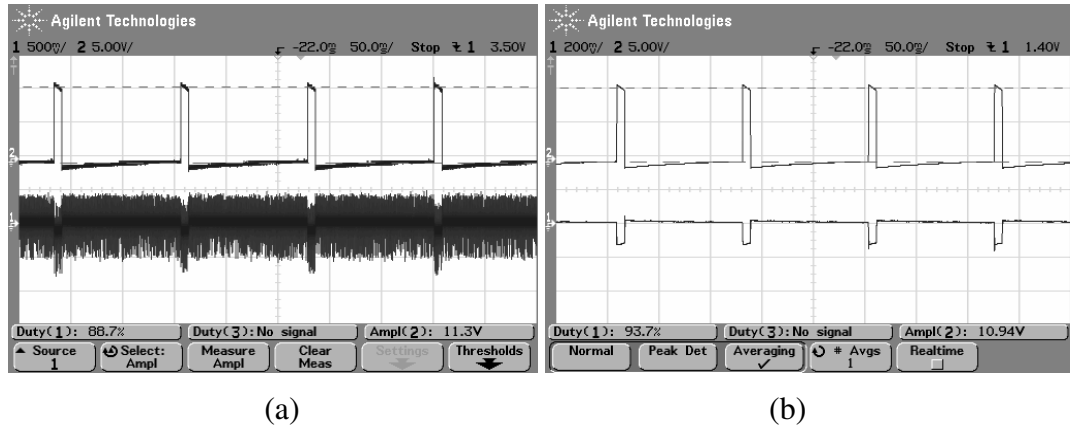


Figure 4.52 The switched-load pulses (top, 5V/div) and output voltage (bottom, 500mV/div for (a), 200mV/div for (b)) waveforms at closed-loop operation: (a) at normal mode of the scope; (b) at averaging mode of the scope.

Besides the DC regulation, it is clear in the figure that the amplitude of the voltage sag is decreased by the controller action. Figure 4.53 shows the output voltage in a small time division. The controller response can be seen at the switching instants of the switched-load.

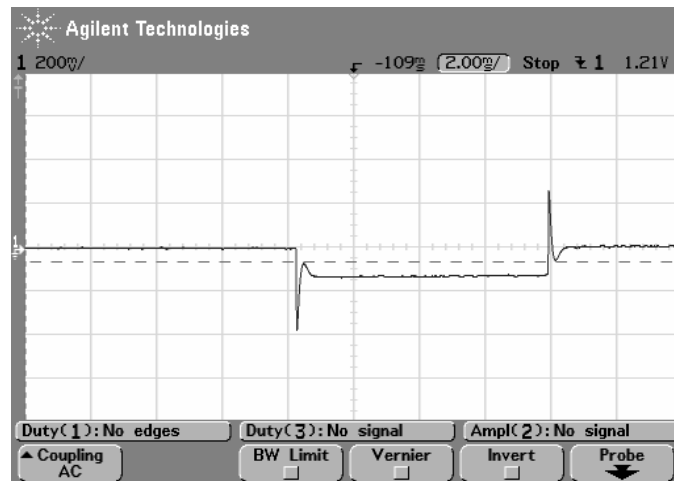


Figure 4.53 Output voltage in closed-loop control with smaller time division (2 V/div and 2 ms/div).

The same procedure is repeated by setting the converter main load to  $90\Omega$ . In this operation, the switched-load value is unchanged. Since the converter current in this operating conditions is low, the switched-load effect is distinct. Figure 4.54 shows the effects of the switched-load at open-loop operation and the controller response in closed-loop. The output voltage is represented in small time division to inspect controller response. It is clear that in Figure 4.55 the output voltage collapses more than 4 volts. Figure 4.55 shows that controller reacts to the voltage drop and at the maximum the voltage drop is about 0.6V and only in a small time period.

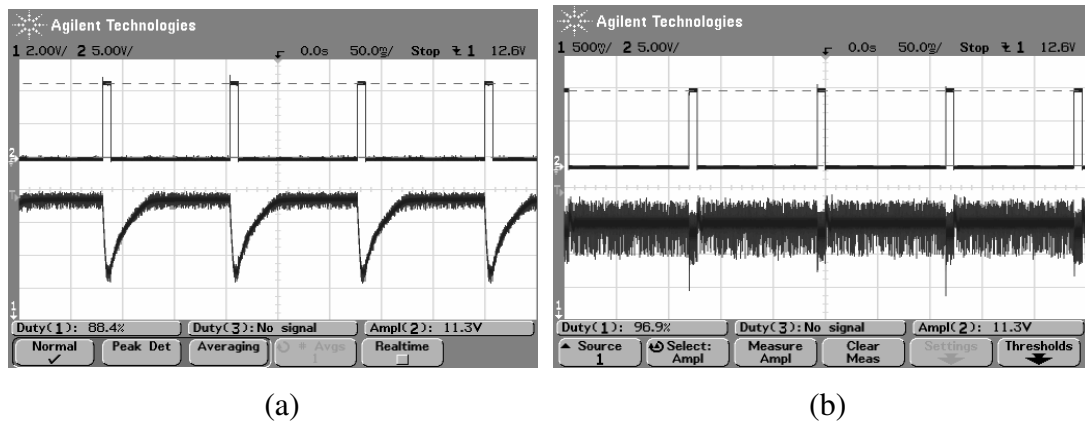


Figure 4.54 The switched-load pulses (top, 5V/div) and the output voltage (bottom, 2V/div for (a), 500mV/div for (b)) responses at light load: (a) open-loop response; (b) closed-loop response.

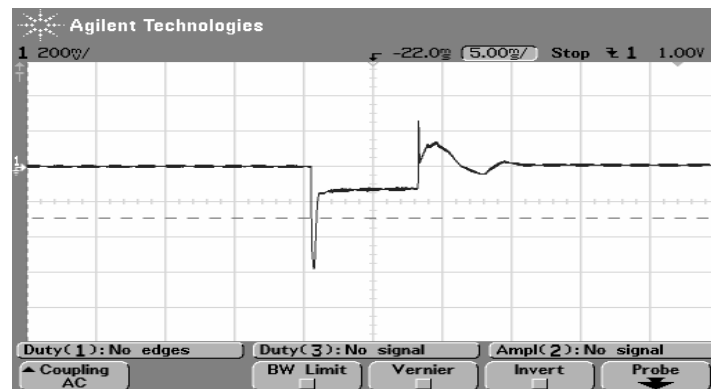


Figure 4.55 The output voltage with small time division.

### 4.3.8 Peak Current Control Results

As the last experiment, peak current mode control will be applied to the buck-boost converter. For the power-pole board connection, the buck-boost converter configuration is used which is shown in Figure 4.25.

At first step, the current loop will be operated with no voltage feedback. The peak current mode control method has an inherent stability problem when the duty cycle exceeds 50%. The first observation will be the demonstration of this condition of instability. Therefore the power-pole board will be switched to the peak current control mode by removing the ramp signal jumper (refer to Appendix A); and by connecting number 6 and 11 of daughter board connection pins via a 10K resistor. In this configuration the measured inductor current ramp will directly be applied to the input of the ramp signal waveform. Figure 4.56 shows the inductor current, and the PWM pulses at minimum possible duty cycle and at maximum stability point.

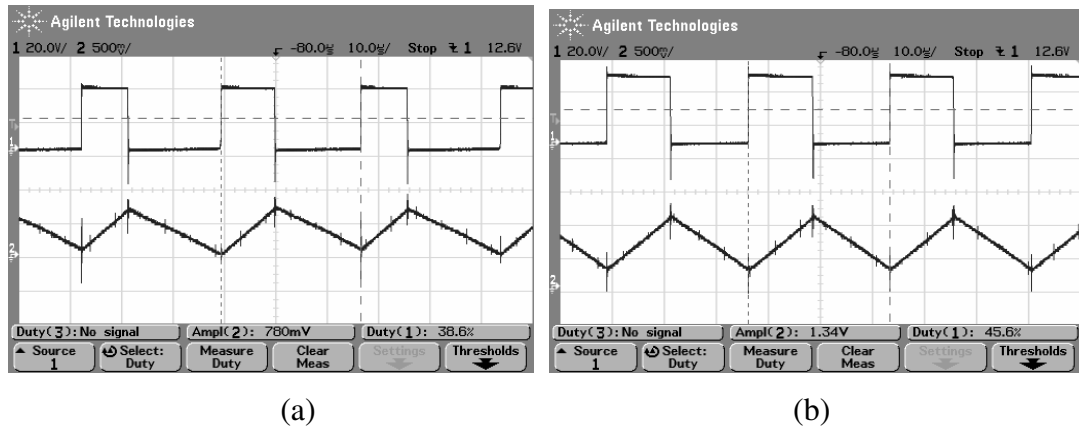


Figure 4.56 Inductor current (bottom, 1A/div) and duty cycle signal (gate-source voltage, top, 20V/div) at peak current control: (a) at minimum duty cycle; (b) at maximum stable duty cycle.

Figure 4.56 shows that there is no instability at the inductor current hence at the PWM signal of the converter. The maximum stable duty cycle is theoretically 50%,

however at about 47% duty cycle level, the converter becomes unstable. When the duty cycle exceeds this duty cycle value, the subharmonic oscillations begin to appear. This condition is shown in Figure 4.57.

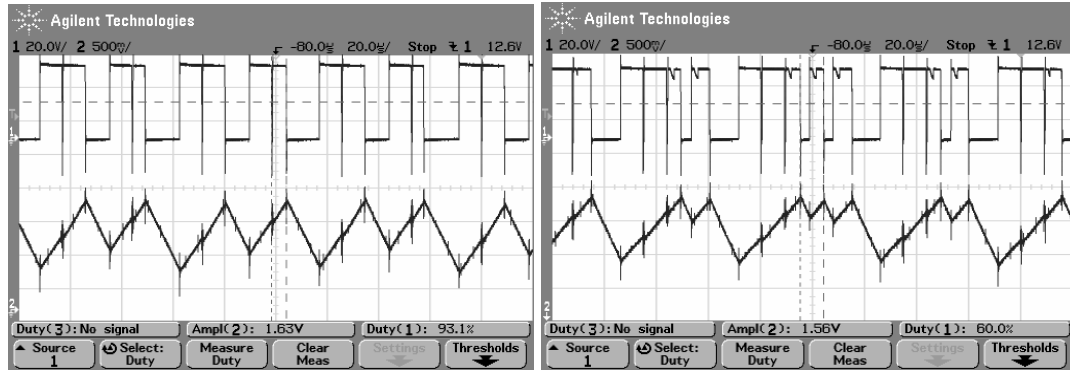


Figure 4.57 The subharmonic oscillations of duty cycle (top, 20V/div) and inductor current (bottom, 1A/div) at peak current control: (a) current reference closer to the sub limit 50%; (b) excessive value of current reference.

The solution for the instability problem is the slope compensation method which is introduced in section 2.4.5. An external ramp waveform is added to the inductor current ramp waveform. The slope of this waveform determines the duty cycle limit for the stability. To apply the slope compensation on power-pole board, the slope compensation jumper should be plugged instead of ramp signal jumper. The two different duty cycle results are shown in Figure 4.58. As seen in the figure, although the duty cycle is 64% the inductor current and the PWM pulses exhibit no oscillations. The slope compensation stabilizes the current loop.

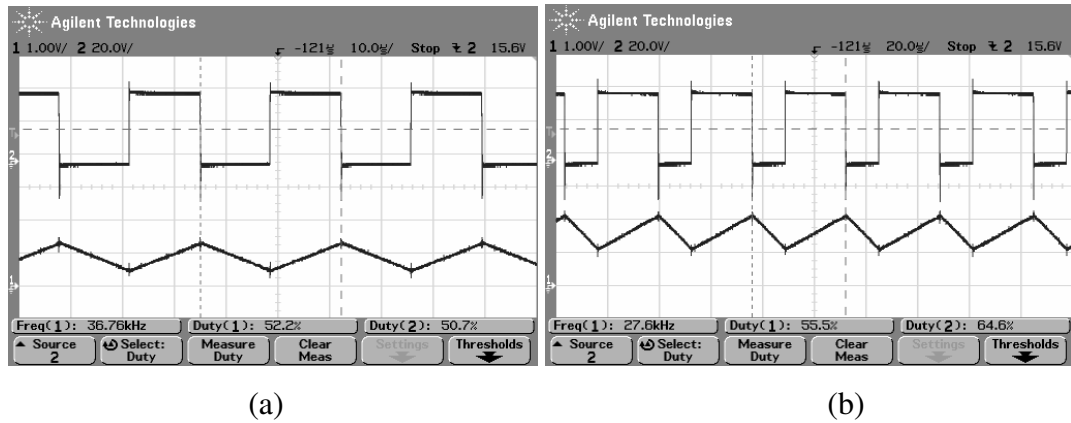


Figure 4.58 Duty cycle (top, 20V/div) and the inductor current (bottom, 2A/div) for the slope compensation step of the peak current mode control: (a) at 50% duty cycle; (b) at 64% duty cycle.

After stabilizing the current loop, the last step is closing the voltage loop. For the voltage loop, a type-II controller is designed again. This time a generic design is carried out without inspecting the converter deeply. An integrator-pole is placed at  $s=0$  to provide low frequency regulation. To improve the phase margin and the midband gain a low frequency zero is placed near 2 kHz. For high frequency rejection a pole is placed near one decade of the zero frequency. The corresponding type-II controller circuit is shown in Figure 4.59.

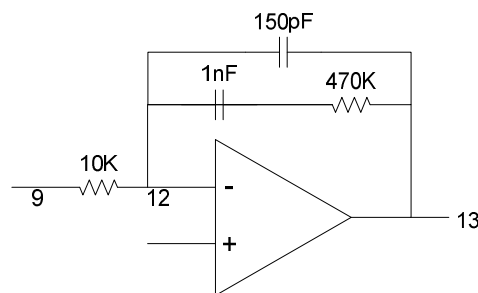


Figure 4.59 The type-II controller for the voltage loop of peak current mode control.

Before closing the voltage loop, the inductor current and the output voltage ripple will be observed by activating the switched-load again in the open-loop mode. Now

by switching the control selection jumper to the closed-loop mode and connecting type-II controller to the corresponding number of pins the multi-loop control structure is completed. The open-loop and the closed loop results are presented in Figure 4.60 (a) and (b) respectively.

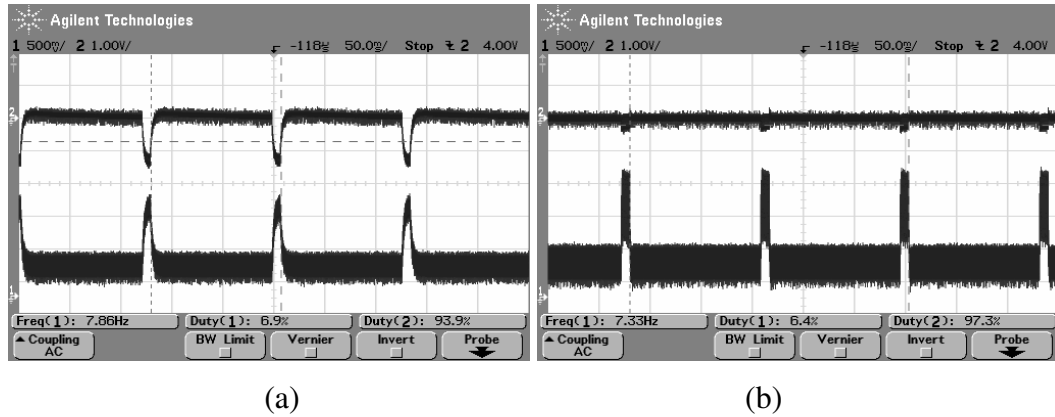


Figure 4.60 Inductor current (bottom, 1A/div) and output voltage (top, 1V/div) waveforms: (a) open-loop response; (b) closed-loop response.

The peak current mode control experiment on the power-pole board was the last demonstration of the chapter 4 which is allocated to explain the whole experimentation process. Along this chapter, the open loop operation of basic isolated and non-isolated converters was carried out. The buck converter and the buck-boost converter were chosen to demonstrate the voltage-mode and the peak current controls respectively. Along with the converter experiments, the design process of the magnetic components in the isolated converters and the compensator design through the closed-loop sections were also explained. The design process was based on the theoretical structure which has been introduced in chapter 2. Hence a complete application chapter has been finalized.

## **CHAPTER 5**

### **CONCLUSIONS**

Switch-mode DC/DC converters are the most important stages of the SMPSs which are defined as the key technology in modern power electronics. They reduce size and cost in comparison to linear power supply, which are based on the linear scaling of rectified input by means of a switch that is operated in linear region. With the efficiency and the topological limits, the linear supplies generally are not proposed as a choice in power supply design.

Unlike the linear supplies, the SMPSs can provide efficient energy conversion by operating the controlled switches out of their linear region. Reducing the switching losses by this way, the higher frequencies can be reached which provides the small amount of energy transfer between the passive components. That means energy is transferred in the form of small packets but in a fast way. This also brings the reduction in the passive components size since the amount of energy that the component will store and release at one time is reduced by means of fast switching.

The fast switching phenomena provides the advantages stated above in one side, however in the other side, new problems are introduced because of the nonidealities of the components. The parasitic components inherent in the structure of semiconductors or passive elements begin to appear as the frequency gets higher. Hence, special care must be given to the design process in the SMPS since any component may exhibit unexpected behaviors at the high frequency levels. A

capacitor behaves as an inductor over some frequency range; the capacitances between the inductor windings start to appear with increasing frequency. All PCB traces include stray inductors and resistors in high frequency applications. Briefly hardware design becomes more and more important.

While the practical topics are going wider and deeper in the SMPS technology, the modern power electronics curricula include the basics of these topics in the undergraduate level. The theoretical courses introduce the basic principles of switch-mode conversion and undergraduate students get familiar with the different non-isolated and isolated topologies.

Beyond the theoretical education in SMPS technology, the application of the converters have great effect on understanding the switch-mode phenomena. Realizing the topological relations, how a converter topology transforms to another or briefly how all topologies are derived from one basic topology will provide a wiser approach to any type of DC/DC converter. Along with the relations between topologies, observing how the volt-seconds balance of the inductor is provided inherently; how the switches respond to turn on or off comments; or how the converter behavior deviates from the theoretical derivations because of the parasitic effects mentioned in the previous paragraph will take the students out of the theoretical aspect and provide practical points of view. Therefore, some practical studies must be carried out along with the theoretical work.

The idea behind this thesis was to built a circuit or circuits to compose a basic SMPS laboratory for undergraduate study. Furthermore, instead of discrete boards for each topology, to show the topological relations was the main philosophy: A single board that can be transformed between five basic topologies by simple connection or passive element changes.

To realize this project, the Power Pole Board of Ned Mohan is adopted, examined and implemented. As a result of implementation, three basic non-isolated (buck, boost, and buck-boost) and two basic isolated (flyback and forward) totally five



topologies are combined on a single board for open loop operation and in open-architecture. Voltage mode control of buck converter and peak current mode control of buck-boost converter were experienced and prepared for the laboratory demonstration as well.

Another advantage of this board is the flexibility of the board based on its plug-in magnetics boards, reconfigurable terminal connections, and variable switching frequency. This may supply a medium for the trial of student projects. For example a flyback transformer or a high-frequency inductor design project may be submitted to the students and the designed components can be tried on Power Pole Board from 100 kHz down to 30 kHz. This flexibility can make the Power Pole Board a progressive circuit rather than a strict experimental tool.

Beyond the power-pole board, a small, simple, device characterization board is also built to observe the switching characteristic of different switches at different conditions. A simple linear power supply is also built for the required voltage levels to carry out all these experiments. By using all these circuits, an SMPS laboratory can be composed.

As the future work, the other control methods such as average current control or tolerance-band (hysteresis) control methods can be developed for demonstration to higher level students. By designing an interface, the power pole board may be integrated with a digital microcontroller or a signal processor. This provides the application of basic discrete control algorithms such as discrete PI or PID.

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## APPENDIX A

### Power-Pole Board Visual Explanation

The terminals, jumpers, and other tools on power-pole board are explained below.  
The figure is shown in the next page.

T1: Power terminal 1: Power input for buck, flyback and forward converters. Output for boost converter.

T2: Supply terminal :  $\pm 12\text{V}$  supply terminal for the ICs and hall-effect sensors.

T3: Power terminal 2: Power input for buck-boost converter.

T4: Power terminal 3: Power input for boost converter. Output for buck, buck-boost, flyback, and forward converters.

T5: Switched-load terminal : Terminal to connect the external load to be switched in the closed-loop applications.

T6: Switch selection terminals : Terminals to select the upper or lower diodes/MOSFETs.

T7: Mid-point Terminal : Terminal of the MOSFET and diode joint.

T8: Magnetic board terminals : Terminal to plug the magnetic boards in.

T9: Daughter board terminals : Terminals to connect the daughter control boards.

S1: Supply switch :  $\pm 12\text{V}$  supply on-off switch.

S2: PWM selection switch : Switch to send the PWM signals to the upper MOSFET.

- S3: PWM selection switch : Switch to send the PWM signals to the lower MOSFET.
- R1: Duty cycle POT : 10K pot to adjust the duty cycle.
- R2: Frequency POT : 100K Trimmer POT to adjust the switching frequency.
- L1: +12V LED : Indicates that the board has connection with +12V.
- L2: Error LEDs : Error indicator LEDs, from left to right, fault LED, overvoltage LED and overcurrent LED.
- J1: Small-signal injection jumper : Jumper to inject a small AC signal to obtain converter frequency response. If the jumper is in the middle of the terminals as shown in the figure, the terminals are shorted hence there is no small signal activity. The small AC signal can be applied to the terminals at two different sides after removing the jumper.
- J2: Control selection jumper : Selects the open-loop mode when justified to right as in the figure, the system switches to closed-loop mode when switched to the left side.
- J3: Ramp signal jumper : Conducts the ramps signal created by the controller, to the controllers ramp input. Slope compensation jumper is connected here in the peak current control mode.
- J4: Reference signal selection jumper : Selects the voltage reference input for the closed-loop operation modes. Duty cycle POT is used when justified to the right hand side, external reference is accepted from the daughter board connection terminals when justified to the left hand side.
- J5: Switch-load jumper : Activates the switched-load when switched to the left terminals. No function available otherwise.



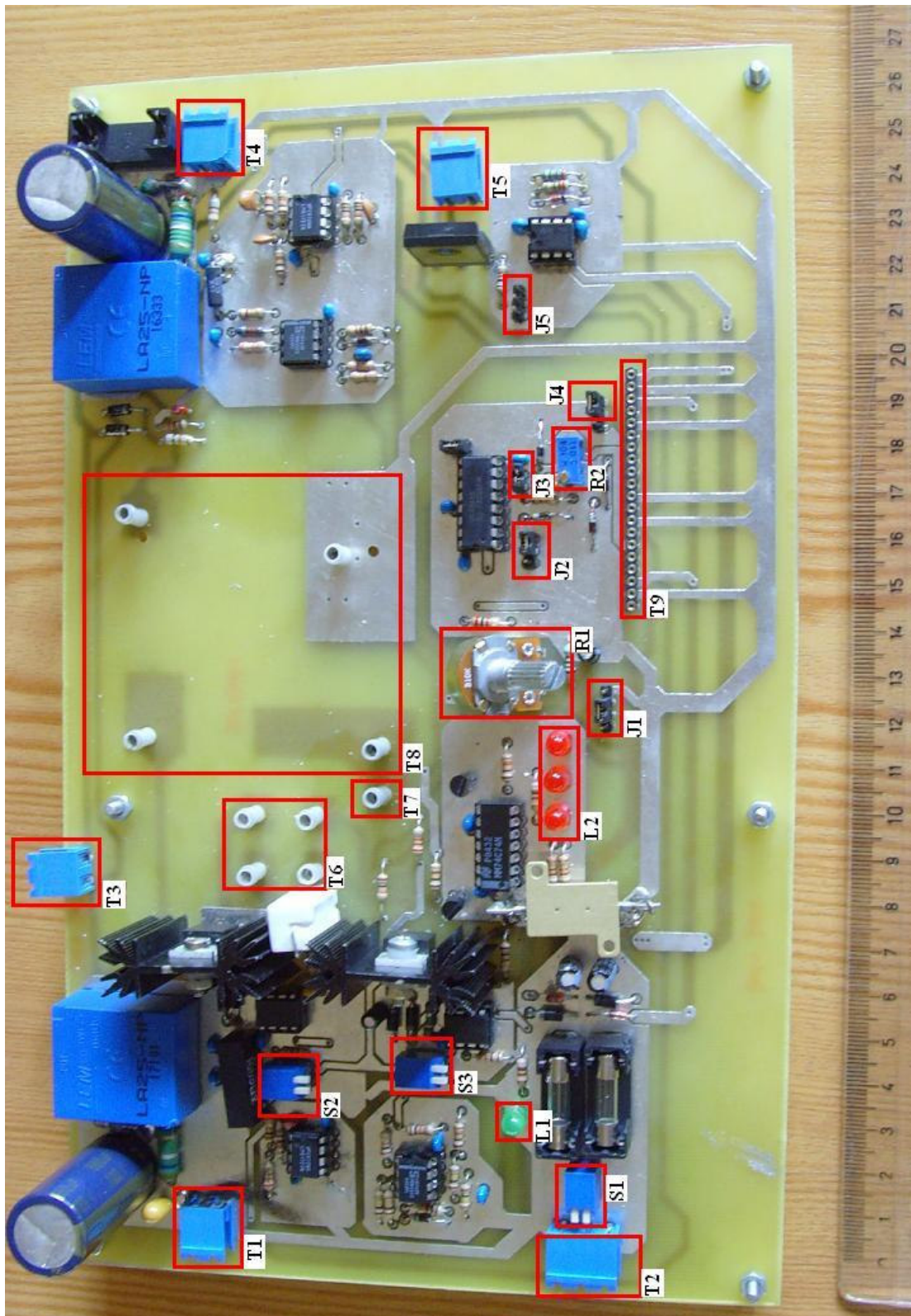


Figure A1. Power-pole board.

## APPENDIX B

## Power-Pole Board Schematic

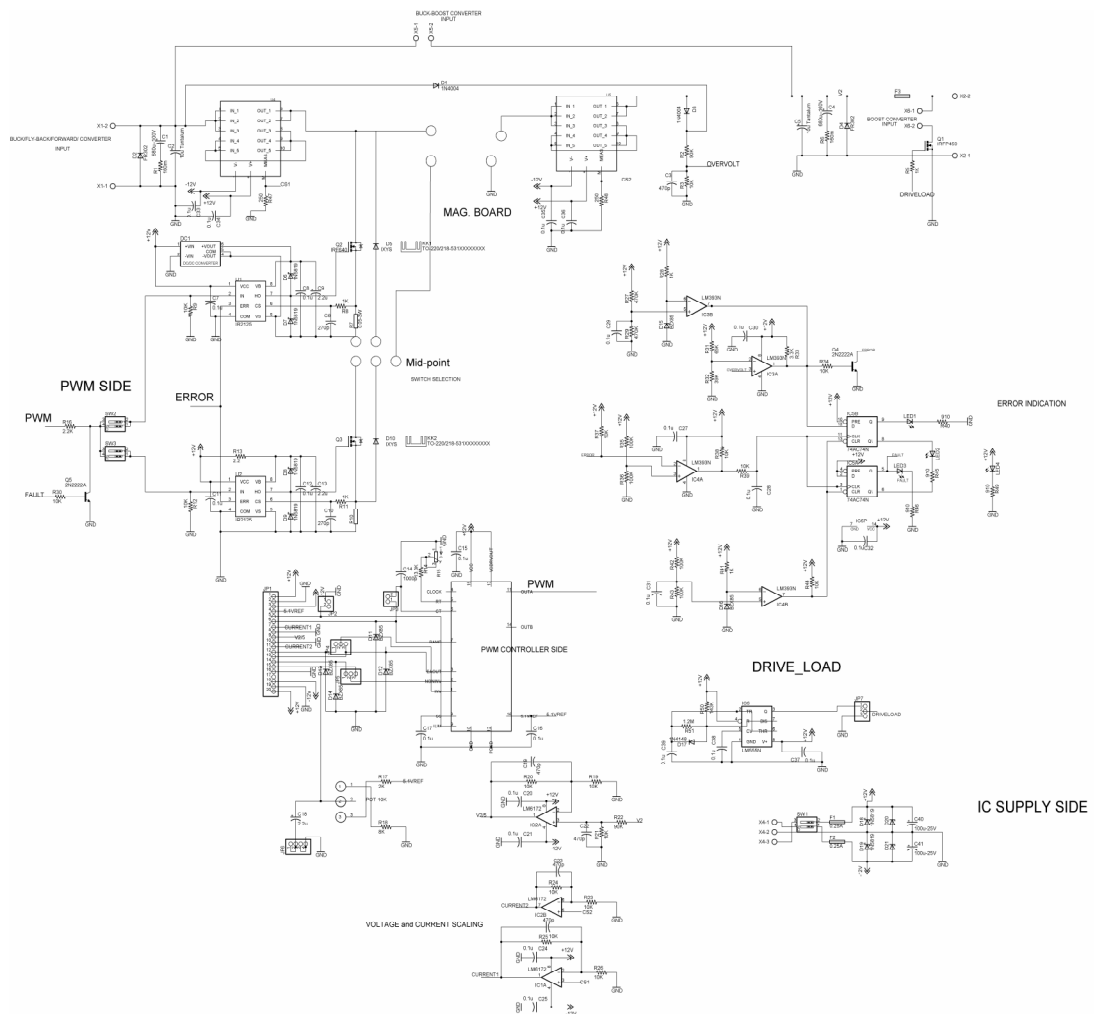


Figure B1- Power-pole board schematic.

## APPENDIX C

### PCB and Layout of Power-Pole Board

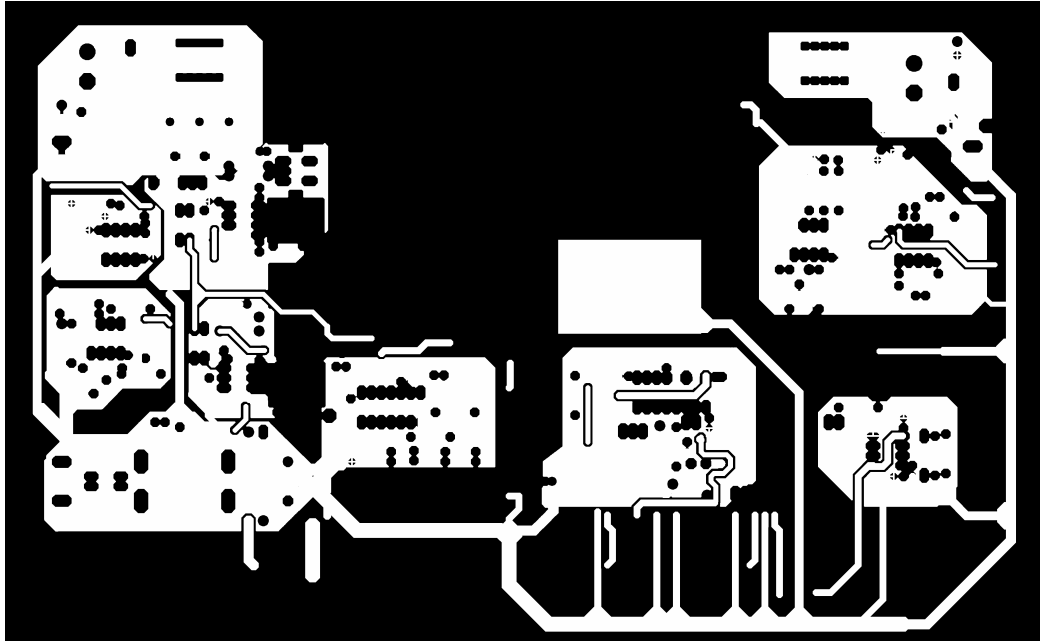


Figure C-1 Top copper layer of power-pole board.

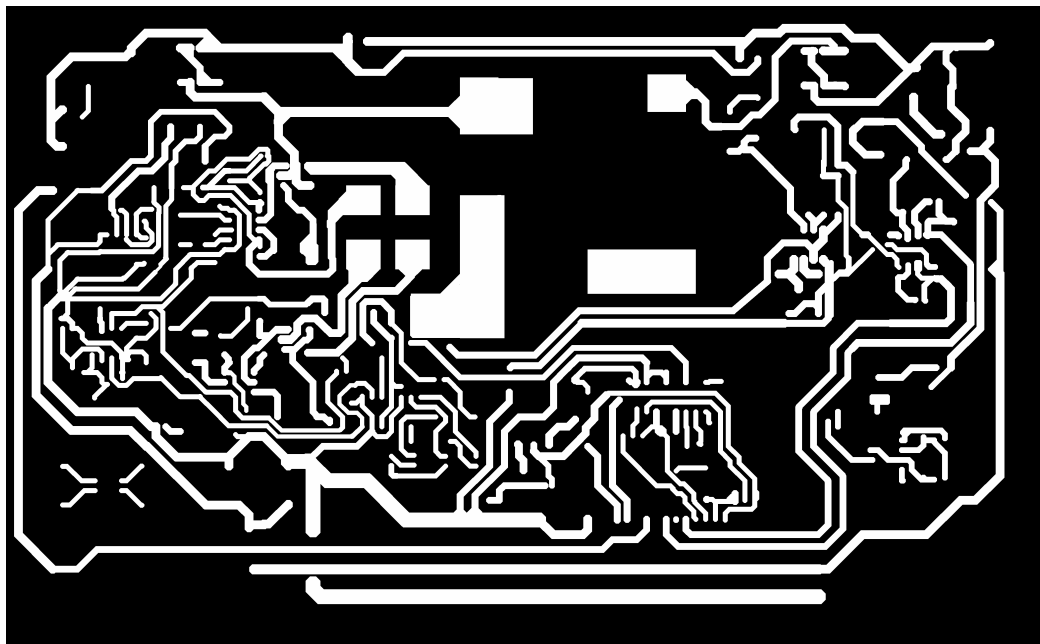


Figure C-2 Bottom copper layer of power-pole board.

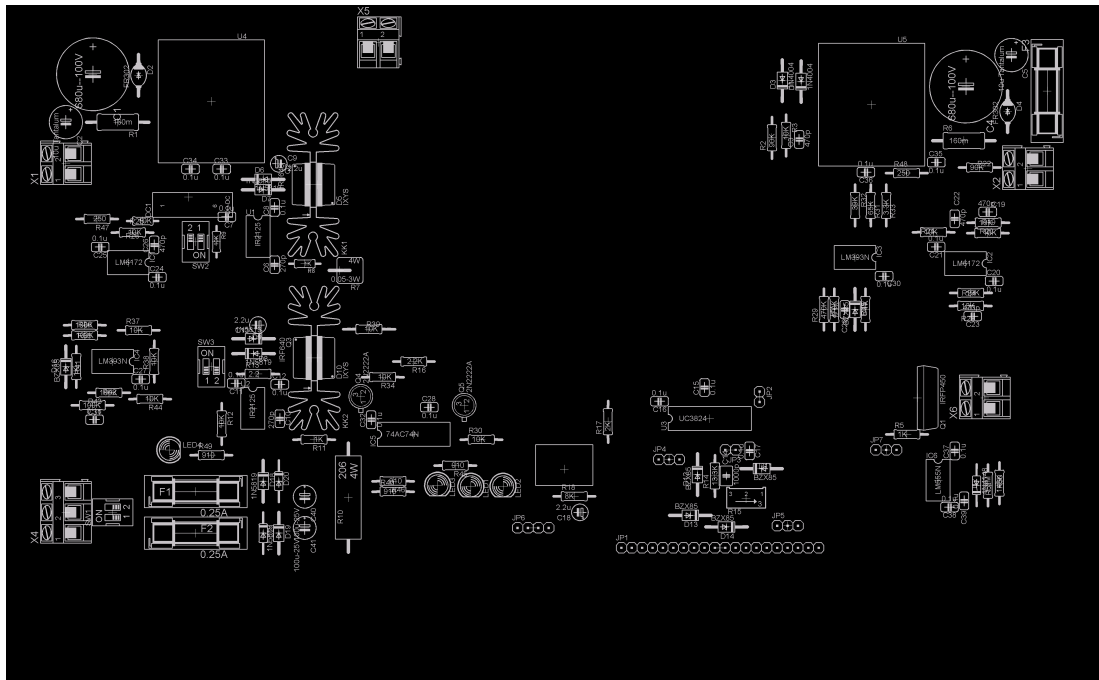


Figure C-3 Power-pole board layout.

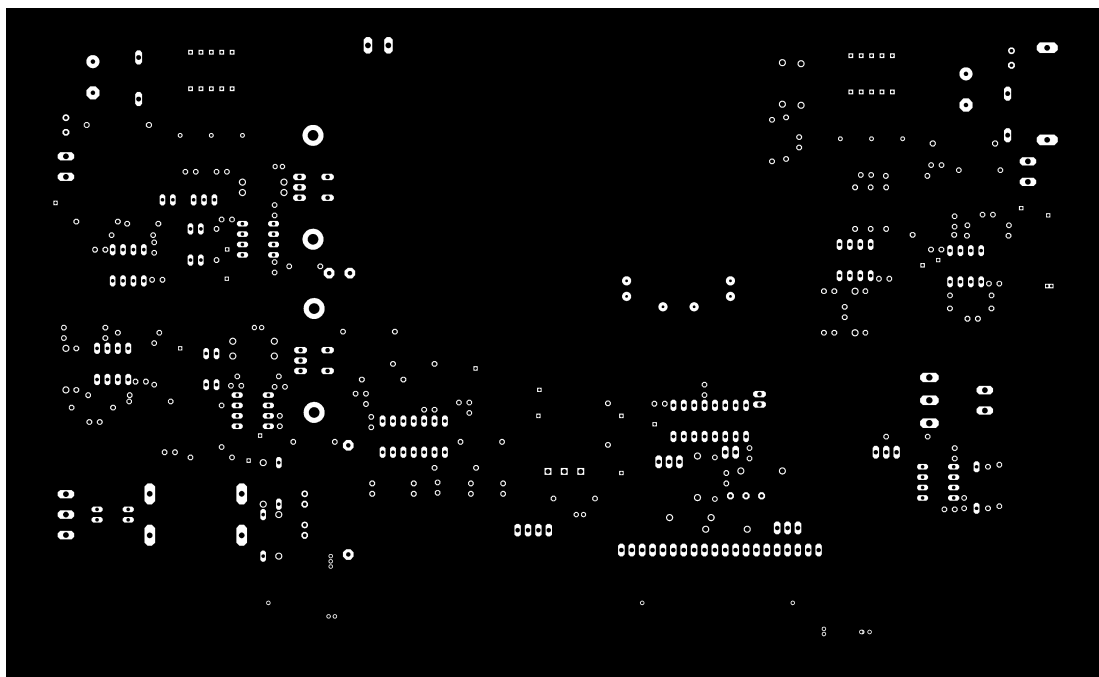


Figure C-4 Pads and vias of power-pole board.

## APPENDIX D

### Real Appearance, Schematic, PCB, and Layout of Linear Power Supply



Figure D-1 Real appearance of linear power supply.

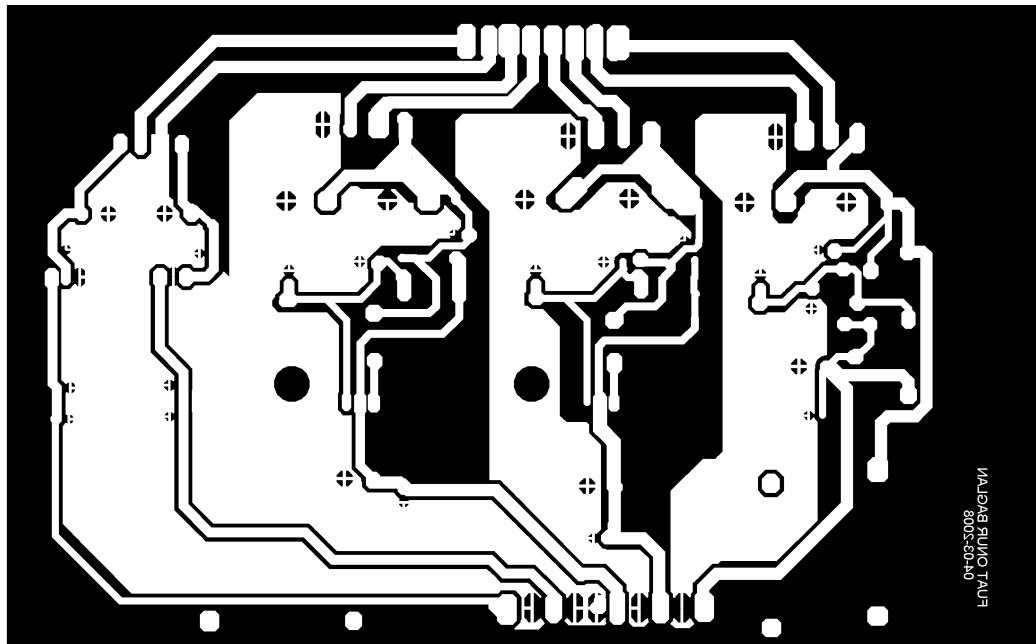


Figure D-2 Bottom copper layer of linear power supply.

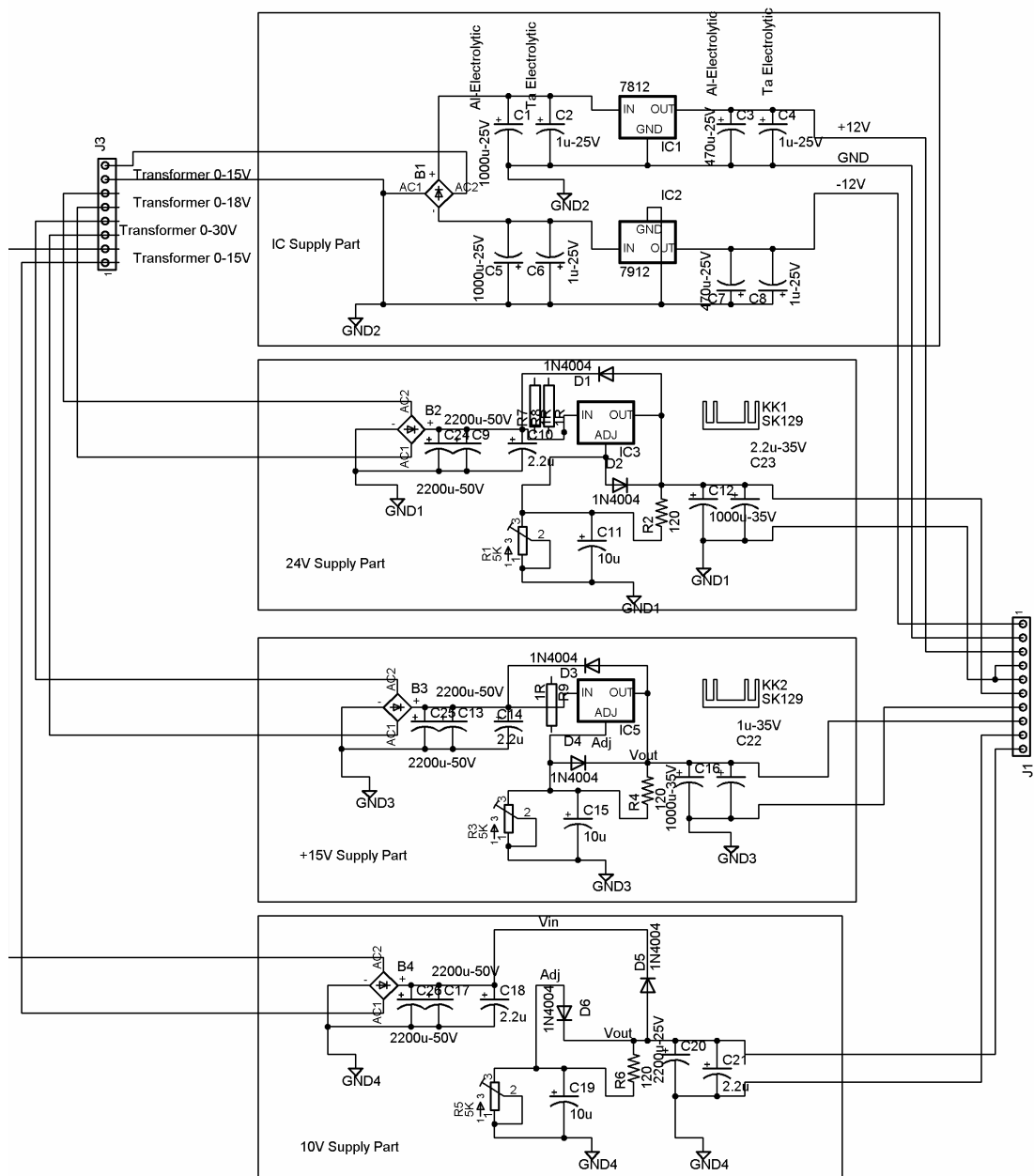


Figure D-3 Schematic diagram of linear power supply.

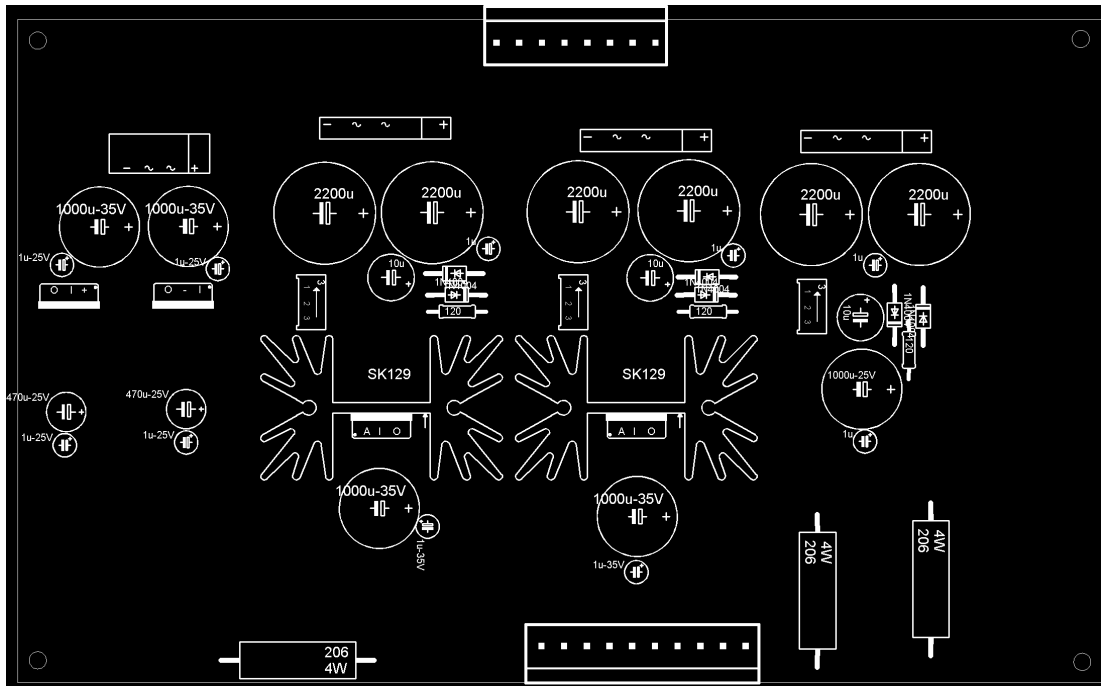


Figure D-4 PCB layout of linear power supply.

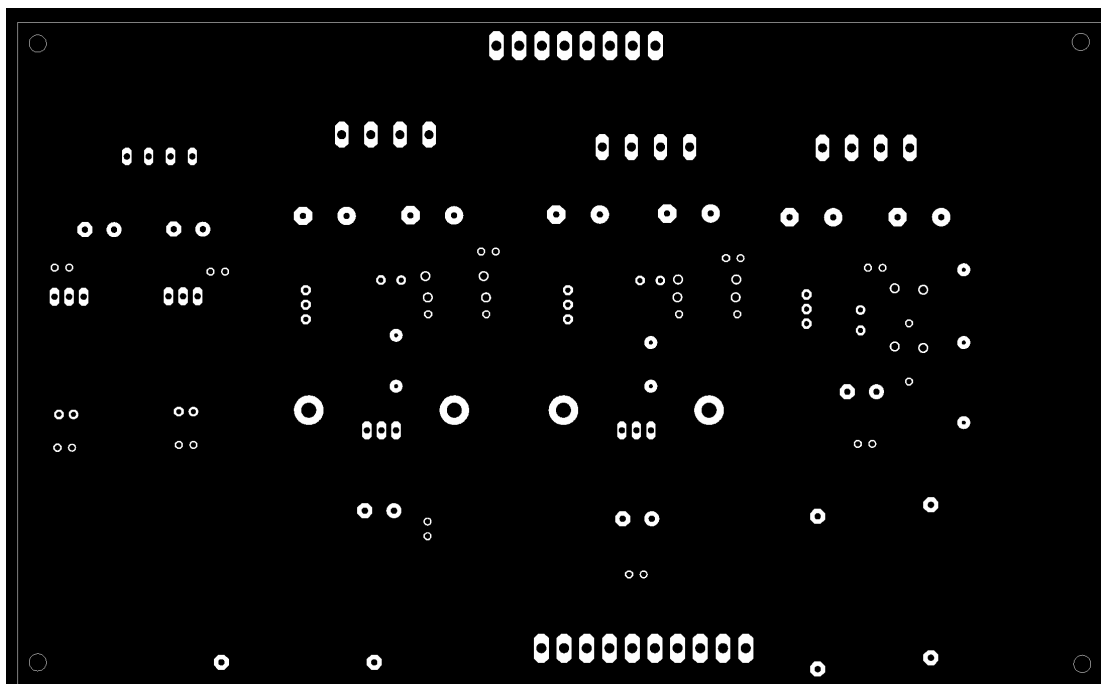


Figure D-5 Pads and vias of linear power supply.