Design Example Report

Title	***65 W Adapter Using TOPSwitch™-JX TOP269EG***
Specification	90 VAC – 265 VAC Input; 19 V, 3.42 A Output
Application	Notebook Adapter
Author	Applications Engineering Department
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Summary and Features

- Highly energy efficient
  - Very low no-load input power: <90 mW at 230 VAC
  - High full-load efficiency: >86% at 90 VAC / 60 Hz
  - High average efficiency: >89.5%
- Very compact, low parts-count design
  - Internal current limit reduction eliminates need for current limit on secondary-side
  - Primary side latching overvoltage protection (OVP) eliminates second optocoupler
  - 132 kHz operation reduces transformer size, reducing cost and improving efficiency
  - Hysteretic thermal protection
- Excellent transient load response
- Latching overvoltage protection
- 80% MOSFET BV de-rating at 65 W and 240 VAC

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This engineering report describes a notebook adapter power supply employing the Power Integrations TOPSwitch-JX TOP269EG. This power supply operates over a universal input range and provides a 19 V, 65 W output. It has been designed and tested to operate in a sealed enclosure in an external ambient temperature environment of up to +40 °C.

The TOPSwitch-JX, by design, maintains virtually constant efficiency across a very wide load range without using special operating modes to meet specific load thresholds. This optimizes performance for existing and emerging energy-efficiency regulations. Maintaining constant efficiency ensures design optimization for future energy-efficiency regulation changes without the need for redesign.

The low MOSFET capacitance of TOPSwitch-JX allows a higher switching frequency without the efficiency penalty which occurs with standard discrete MOSFET. The 132 kHz switching frequency (rather than the 60 kHz to 80 kHz frequency used for a discrete MOSFET) reduces the transformer size required, and so reduces cost.

This power supply offers the following protection features:

- Output OVP with latching shutdown
- Latching open-loop protection
- Auto-recovery type overload protection
- Auto-restart during brownout or line sag conditions
- Accurate thermal overload protection with auto-recovery, using a large hysteresis

This document provides complete design details including specifications, the schematic, bill of materials, and transformer design and construction information. This information includes performance results pertaining to regulation, efficiency, standby, transient load, power-limit data, and conducted EMI scans.

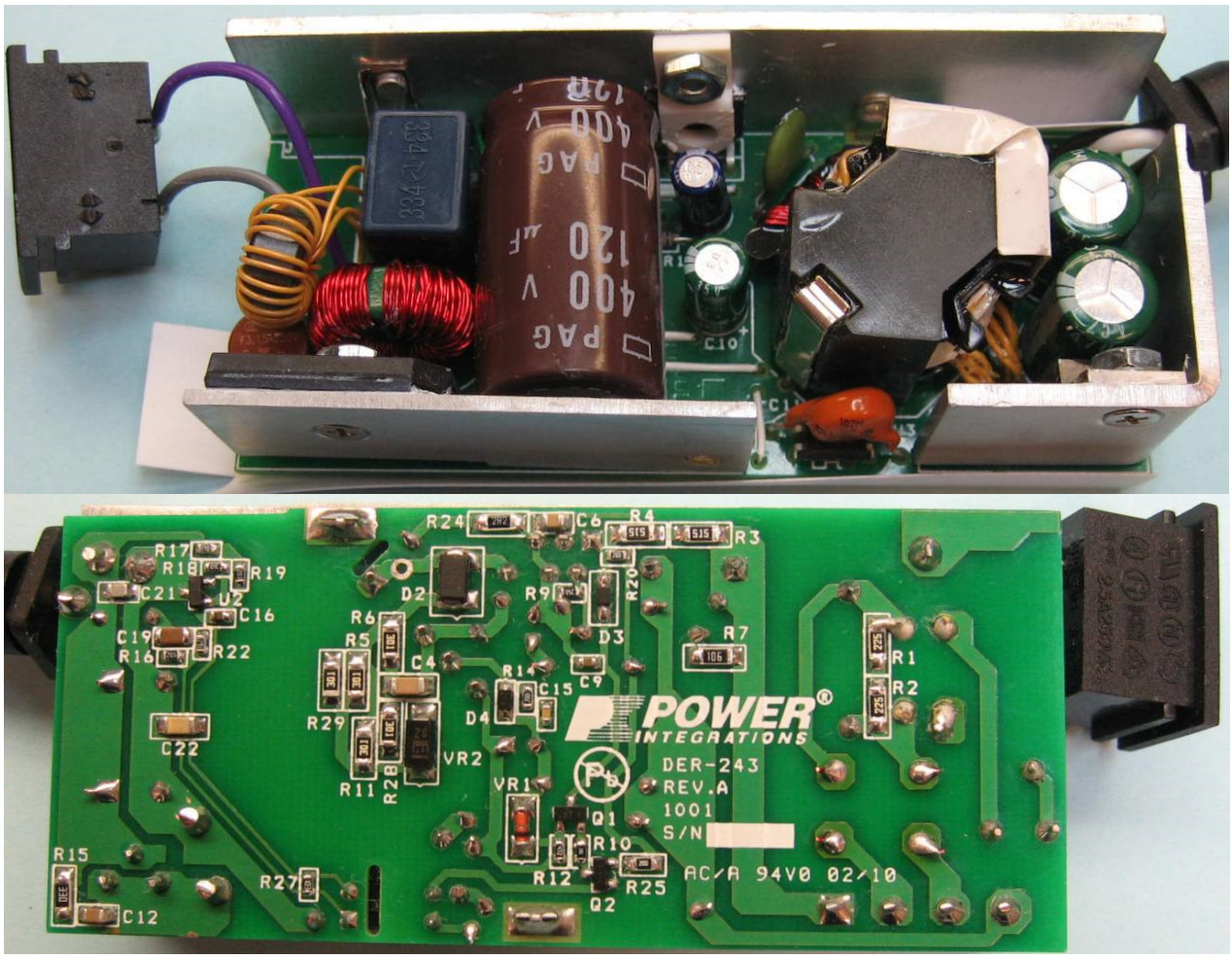

Figure 1 – Populated Circuit Board Photographs.

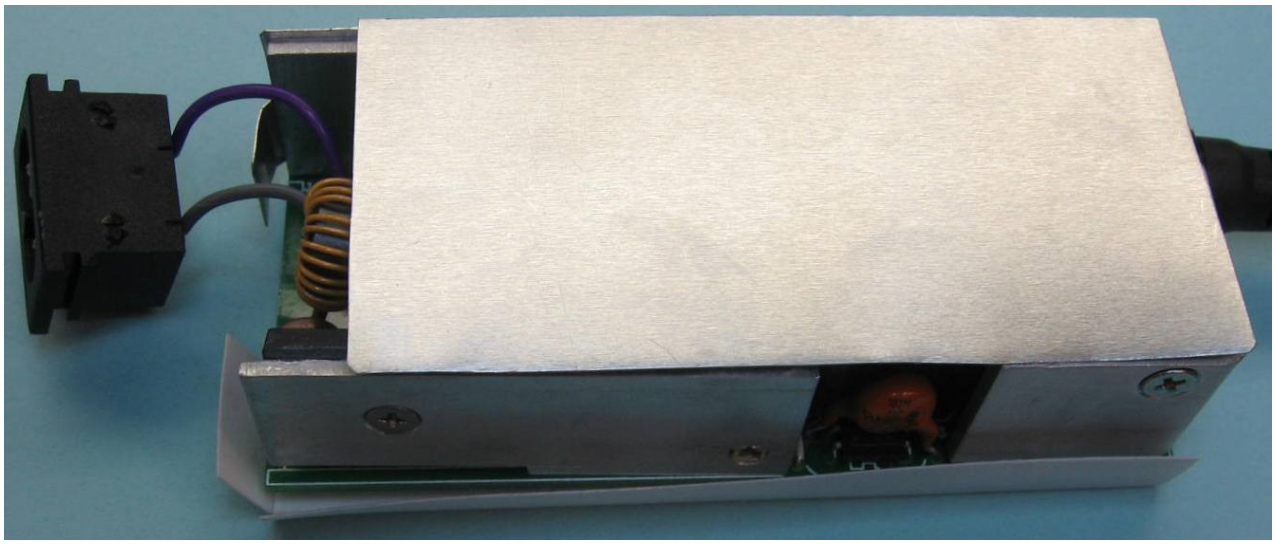

Figure 2 – Assembly Unit with Heat Spreader.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
No-load Input Power (264 VAC)				0.100	W	
Output						
Output Voltage 1	V_{OUT1}	18.05	19	19.95	V	± 5%, end of 1.8 m 18 AWG cable
Output Ripple Voltage 1	$V_{RIPPLE1}$			250	mV	20 MHz bandwidth
Output Current 1	I_{OUT1}	0		3.42	A	
Total Output Power						
Continuous Output Power	P_{OUT}		65		W	
LPS	P_{OUT_PEAK}			100	W	
Efficiency						
Full Load	η	86			%	Measured at P_{OUT} 25 °C, 90 VAC / 60Hz
Required average efficiency at 25, 50, 75 and 100 % of P_{OUT}	$\eta_{ES2.0}$	87			%	Per ENERGY STAR V2.0
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950 / UL1950 Class II				
Line Surge						1.2/50 μs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω Common Mode: 12 Ω
Differential Mode (L1-L2)	1.5				kV	
Common mode (L1/L2-PE)	3				kV	
Ambient Temperature	T_{AMB}	0		40	°C	Free convection, sea level

3 Schematic

Input Voltage (VAC)	90	115	230
Full Power Efficiency (%)	86.6	88.4	89.1
Average Efficiency (%)		89.8	89.5
No-load Input Power (mW)	57.7	59.7	86.7

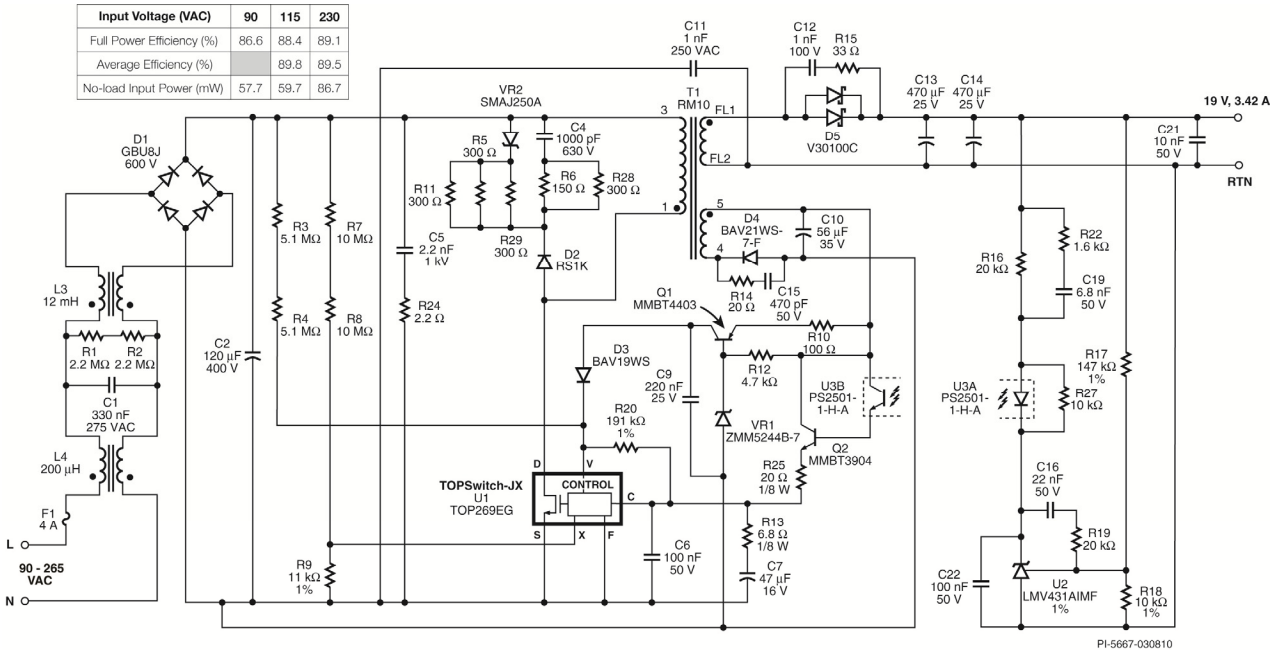

Figure 3 – Schematic.

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4 Circuit Description

This power supply employs a TOP269EG off-line switcher IC, (U1), in a flyback configuration. IC U1 has an integrated 725 V MOSFET and a multi-mode controller. It regulates the output by adjusting the MOSFET duty cycle, based on the current fed into its CONTROL (C) pin.

The goals of the design were highest full load efficiency, average efficiency (average of 25%, 50%, 75% and 100% load points), very low no-load consumption. Additional requirements included latching output overvoltage shutdown and compliance to safety agency limited power source (LPS) limits.

4.1 Key Design Decisions

The following key decisions were made during the design of this supply.

4.1.1 PI part selection

- A larger device was selected than required for power delivery to increase efficiency and offset effect of smaller input capacitor value (lower value of DC bus voltage).
    - In an open frame configuration the TOP268 device could be used for lower cost.

4.1.2 Increased Line Sense Resistor Values

- The line sensing resistance (R3 + R4) was increased from 4 MΩ to 10.2 MΩ to reduce no-load input power dissipation by ~16 mW. This required the addition of R20 to maintain the same line under-voltage threshold.

4.1.3 Clamp Configuration Selection – RZCD vs RCD

- An RZCD (Zener bleed) was selected over RCD to give higher light load efficiency and lower no-load consumption.

4.1.4 Feedback configuration

- A Darlington configuration was formed by adding Q2 to the optocoupler transistor to reduce secondary side feedback current and no-load input power.
- Low voltage, low current voltage reference IC used on secondary side to reduce secondary side feedback current and no-load input power.
- The bias winding voltage tuned to ~9 V at no-load, high line to reduce no-load input power.

4.1.5 Output Rectifier Choice

- High current rating, low V_F Schottky rectifier diode selected for output rectifier to reduce diode loss and improve efficiency.

4.1.6 Increased output overvoltage shutdown sensitivity

- Transistor Q1 and VR1 added to improve the output overvoltage shutdown sensitivity.

4.2 Input EMI and Rectification Stage

Common-mode inductors L3 and L4 provide filtering on the AC input. X class capacitor C1 provides differential filtering, and resistors R1 and R2 provide safety from shock if the AC is removed, by ensuring a path for C1 to discharge. This is required by safety agencies when the capacitor value exceeds 100 nF. Bridge rectifier D1 rectifies the AC input, and bulk capacitor C2 filters the DC. Due to the space constraints of the case the value of C2 is smaller than typically recommended (1.8 μF/W_{OUT} vs 2-3 μF/W_{OUT} typically recommended).

Y capacitor C11, connected between the primary and secondary side provides common mode filtering.

4.3 TOPSwitch-JX Primary

The EcoSmart feature of U1 automatically provides constant efficiency over the entire load range. It uses a proprietary Multi-cycle-modulation (MCM) function to eliminate the need for special light or no-load operating modes triggered at specific loads. This simplifies circuit design since it removes the need to design for aberrant or specific operating conditions or load thresholds.

Capacitor C7 provides the auto-restart timing for U1. At startup this capacitor is charged through the DRAIN (D) pin. Once it is charged U1 begins to switch. Capacitor C7 stores enough energy to ensure the power supply starts up. After start-up the bias winding powers the controller via the CONTROL pin. Bypass capacitor C6 is placed as physically close as possible to U1. Resistor R13 provides compensation to the feedback loop.

4.4 Clamp Configuration

The clamp network is formed by VR2, C4, R5, R6, R11, R28, R29 and D2. It limits the peak drain voltage spike caused by leakage inductance to below the BV_{DSS} rating of the internal TOPSwitch-JX MOSFET. This arrangement was selected over a standard RCD clamp to improve light load efficiency and no-load input power.

In a standard RCD clamp C4 would be discharged by a parallel resistor rather than a resistor and series Zener. In an RCD clamp the resistor value is selected to limit the peak drain voltage under full load and over-load conditions. However under light or no-load conditions this resistor value now causes the capacitor voltage to discharge significantly as both the leakage inductance energy and switching frequency are lower. As the capacitor has to be recharged to above the reflected output voltage each switching cycle the lower capacitor voltage represents wasted energy. It has the effect of making the clamp dissipation appear as a significant load just as if it were connected to the output of the power supply.

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The RZCD arrangement solves this problem by preventing the voltage across the capacitor discharging below a minimum value (defined by the voltage rating of VR2) and therefore minimizing clamp dissipation under light and no-load conditions.

Resistors R6 and R28 provide damping of high frequency ringing to reduce EMI. Due to the resistance in series with VR2, limiting the peak current, standard power Zeners vs a TVS type may be used for lower cost (although a TVS type was selected due to availability of a SMD version). Diode D2 was selected to have an 800 V vs the typical 600 V rating due to its longer reverse recovery time of 500 ns. This allows some recovery of the clamp energy during the reverse recovery time of the diode improving efficiency. Multiple resistors were used in parallel to share dissipation as SMD components were used.

4.5 Thermal Overload Protection

IC U1 has an integrated accurate hysteretic thermal overload protection function. When the junction temperature of U1 reaches +142 °C (typical temperature shutdown threshold) during a fault condition, the IC shuts down. It automatically recovers once the junction temperature has decreased by 75 °C.

4.6 Output Overvoltage Protection

Open-loop faults cause the output voltage to exceed the specified maximum value. To prevent excessive output voltage levels in such cases, U1 utilizes an output overvoltage shutdown function. An increase in output voltage causes an increase in the bias winding on the primary side, sensed by VR1. A sufficient rise in the bias voltage causes VR1 to conduct and bias Q1 to inject current into the Voltage Monitor (V) pin of U1. When the current exceeds 336 μA, U1 enters the overvoltage shutdown mode and latches off. To change this mode to a hysteretic shutdown wherein attempts are made to restart the power supply at regular intervals to check if the fault condition is removed, increase the value of R10 enough to limit current into the V pin below 336 μA during an open-loop condition.

The addition of Q1 ensures that the current into the V pin is sufficient to exceed the latching shutdown threshold even when the output is fully loaded and operating at low line as under this condition the output voltage overshoot is typically relatively small.

4.7 Line Under-voltage lockout

Line sensing is provided by resistors R3 and R4 and sets the line under-voltage and over-voltage thresholds. The combined value of these resistors was increased from the standard 4 MΩ to 10.2 MΩ. This reduced the resistor, and therefore contribution to no-load input power, from ~26 mW to ~10 mW. To compensate the resultant change in the UV (turn-on) threshold (defined by a 25 μA current into the V pin) resistor R20 was added between the CONTROL and VOLTAGE-MONITOR pins. This adds a DC current equal to ~16 μA into the V pin, requiring only 9 μA to be provided via R3 and R4 to reach the V pin UV (turn-on) threshold current of 25 μA and setting the UV threshold to 95 VDC.

This technique does effectively disable the line OV feature as the resultant OV threshold is raised from ~450 VDC to ~980 VDC. However in this design there was no impact as the value of input capacitance (C2) was sufficient to allow the design to withstand differential line surges greater than 2 kV without the peak drain voltage reaching the BV_{DSS} rating.

Specific guidelines and detailed calculations for the value of R20 may be found in the TOPSwitch-JX Application Note (AN-47).

4.8 Output Power Limiting with Line Voltage

Resistors R7, R8, and R9 reduce the external current limit of U1 as the line voltage increases. This allows the supply to limit the output power to <100 VA at high line while still delivering the rated output power at low line, and to provide a nearly constant output over-load power level with changing line voltages.

4.9 Output Rectification and Filtering

A dual 15 A, 100 V Schottky rectifier diode with a V_F of 0.455 V at 5 A was selected for D5. This is a higher current rating than required to reduce resistive and forward voltage losses to improve both full load and average efficiency. The use of a 100 V Schottky was possible due to the high transformer primary to secondary turns ratio (V_{OR}=110 V) which was in turn possible due to the high voltage rating of the TOPSwitch-JX internal power MOSFET.

A snubber network (C12, R15) dampens ringing across the diodes and reduces high frequency conducted and radiated noise. Capacitors C13 and C14 provide output filtering and achieve the required ripple performance without requiring an output inductor post filter.

4.10 Output Feedback

Resistors R17 and R18 provide a voltage divider and set the DC set point of the output via the reference input of U2. The output of U2 (cathode) drives optocoupler U3 to provide a feedback signal to the primary side and CONTROL pin of U1. An increase in optocoupler current results in reduced primary MOSFET duty cycle.

Typically the feedback current into the CONTROL pin at high line, no-load is ~3 mA. This current is both sourced from the bias winding (voltage across C10) and directly from the output. Both of these represent a load on the output of the power supply.

To minimize the dissipation from the bias winding under no-load conditions the number of bias winding turns and value of C10 was adjusted to give a minimum voltage across C10 of ~9 V. This is the minimum required to keep the optocoupler biased.

To minimize the dissipation of the secondary side feedback circuit Q2 was added to form a Darlington connection with U3B. This reduced the feedback current on the secondary to ~1 mA. The increased loop gain (due to the h_{FE} of the transistor) was compensated by

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increasing the value of R16 and the addition of R25. A standard 2.5 V TL431 voltage reference was replaced with the 1.24 V LMV431 to reduce the supply current requirement from 1 mA to 100 μA.

Control loop compensation is provided by C16 and R19 with C19 and R22 forming a phase boost to improve the phase margin. Resistor R16 limits the DC gain of the feedback system to ensure power supply stability throughout the range of operation. Resistor R27 ensures the minimum bias to U2 and C22 provides a soft finish rise of the output. The relatively small value for C22 is due to the reduced feedback currents.

5 PCB Layout

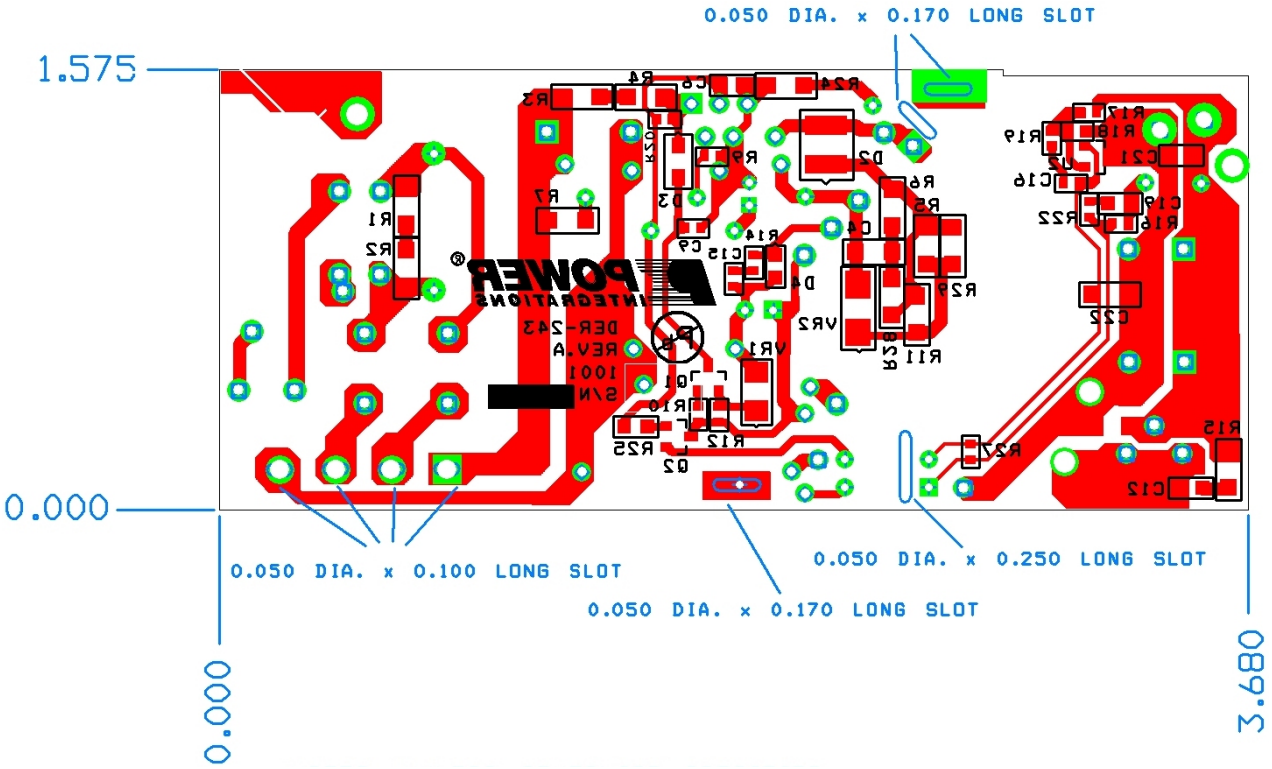

Figure 4 – Bottom Printed Circuit Layout.

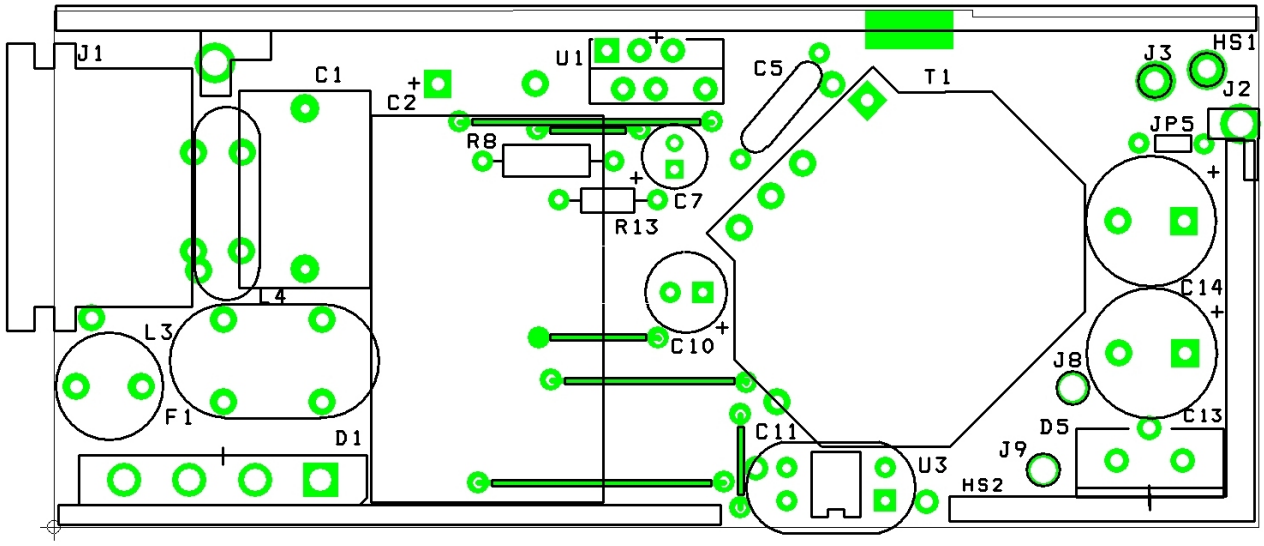

Figure 5 – Top Printed Circuit Layout.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Manufacturer P/N	Manufacturer
1	1	C1	330 nF, 275 VAC, Film, X2	LE334-M	OKAYA
2	1	C2	120 µF, 400 V, Electrolytic, (18 x 30)	EPAG401ELL121MM30S	Nippon Chemi-Con
3	1	C4	1000 pF, 630 V, Ceramic, X7R, 1206	ECJ-3FB2J102K	Panasonic
4	1	C5	2.2 nF, 1 kV, Disc Ceramic	NCD222K1KVY5FF	NIC Components
5	1	C6	100 nF, 50 V, Ceramic, X7R, 0805	ECJ-2YB1H104K	Panasonic
6	1	C7	47 µF, 16 V, Electrolytic, Low ESR, 500 mΩ, (5 x 11.5)	ELXZ160ELL470MEB5D	Nippon Chemi-Con
7	1	C9	220 nF, 25 V, Ceramic, X7R, 0603	06033D224KAT2A	AVX
8	1	C10	56 µF, 35 V, Electrolytic, Gen. Purpose, (6.3 x 11)	EKZE350ELL	Nippon Chemi-Con
9	1	C11	1 nF, Ceramic, Y1	440LD10-R	Vishay
10	1	C12	1 nF, 100 V, Ceramic, X7R, 0805	ECJ-2VB2A102K	Panasonic
11	2	C13 C14	470 µF, 25 V, Electrolytic, Very Low ESR, 38 mΩ, (10 x 16)	EKZE250ELL471MJ16S	Nippon Chemi-Con
12	1	C15	470 pF 50 V, Ceramic, X7R, 0603	ECJ-1VC1H471J	Panasonic
13	1	C16	22 nF, 50 V, Ceramic, Y5V, 0603	ECJ-1VF1H223Z	Panasonic
14	1	C19	6.8 nF, 50 V, Ceramic, X7R, 0805	ECJ-2VB1H682K	Panasonic
15	1	C21	10 nF, 50 V, Ceramic, X7R, 0805	ECJ-2VB1H103K	Panasonic
16	1	C22	100 nF, 50 V, Ceramic, X7R, 1206	ECJ-3VB1H104K	Panasonic
17	1	D1	600 V, 8 A, Bridge Rectifier, GBU Case	GBU8J	Vishay
18	1	D2	800 V, 1 A, Fast Recovery, 250 ns, SMA	RS1K-13-F	Diodes, Inc.
19	1	D3	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
20	1	D4	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
21	1	D5	100 V, 30 A, Dual Schottky, TO-220AB	V30100C	Vishay
22	1	F1	4 A, 250V,Fast, TR5	3701400041	Wickman
23	1	L3	12 mH, xA, Ferrite Toroid, 4 Pin, Output	Custom made	Custom made
24	1	L4	200 µH, 2 A, Ferrite Toroid, 4 Pin, Output	Custom made	Custom made
25	1	Q1	PNP, Small Signal BJT, 40 V, 0.6 A, SOT-23	MMBT4403	Fairchild
26	1	Q2	NPN, Small Signal BJT, 40 V, 0.2 A, SOT-23	MMBT3904LT1G	On Semi
27	2	R1 R2	2.2 MΩ, 5%, 1/4 W, Metal Film, 1206	ERJ-8GEYJ225V	Panasonic
28	2	R3 R4	5.1 MΩ, 5%, 1/4 W, Metal Film, 1206	ERJ-8GEYJ515V	Panasonic
29	5	R5 R6 R11 R28 R29	300 Ω, 5%, 1/4 W, Metal Film, 1206	ERJ-8GEYJ301V	Panasonic
30	1	R7	10 MΩ, 5%, 1/4 W, Metal Film, 1206	ERJ-8GEYJ106V	Panasonic
31	1	R8	10 MΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-10M	Yageo
32	1	R9	11 kΩ, 1%, 1/16 W, Metal Film, 0603	ERJ-3EKF1102V	Panasonic
33	1	R10	100 Ω, 5%, 1/10 W, Metal Film, 0603	ERJ-3GEYJ101V	Panasonic
34	1	R12	4.7 kΩ, 5%, 1/10 W, Metal Film, 0603	ERJ-3GEYJ472V	Panasonic
35	1	R13	6.8 Ω, 5%, 1/8 W, Carbon Film	CFR-12JB-6R8	Yageo
36	1	R14	20 Ω, 5%, 1/10 W, Metal Film, 0603	ERJ-3GEYJ200V	Panasonic
37	1	R15	33 Ω, 5%, 1/4 W, Metal Film, 1206	ERJ-8GEYJ330V	Panasonic
38	2	R16 R19	20 kΩ, 5%, 1/10 W, Metal Film, 0603	ERJ-3GEYJ203V	Panasonic
39	1	R17	147 kΩ, 1%, 1/16 W, Metal Film, 0603	ERJ-3EKF1473V	Panasonic
40	1	R18	10 kΩ, 1%, 1/16 W, Metal Film, 0603	ERJ-3EKF1002V	Panasonic
41	1	R20	191 kΩ, 1%, 1/16 W, Metal Film, 0603	ERJ-3EKF1913V	Panasonic
42	1	R22	1.6 kΩ, 5%, 1/10 W, Metal Film, 0603	ERJ-3GEYJ162V	Panasonic
43	1	R24	2.2 Ω, 5%, 1/4 W, Metal Film, 1206	ERJ-8GEYJ2R2V	Panasonic
44	1	R25	20 Ω, 5%, 1/8 W, Metal Film, 0805	ERJ-6GEYJ200V	Panasonic
45	1	R27	10 kΩ, 5%, 1/10 W, Metal Film, 0603	ERJ-3GEYJ103V	Panasonic
46	1	T1	Bobbin, RM10, Vertical, 5 pins	P-1031	Pin Shine
47	1	U1	TOPSwitch-JX, eSIP-7C	TOP269EG	Power Integrations
48	1	U2	1.24 V Shunt Regulator IC, 1%, -40 to 85 C, SOT23-3	LMV431AIMF	National Semi

49	1	U3	Optocoupler, 80 V, CTR 80-160%, 4-DIP	PS2501-1-H-A	NEC
50	1	VR1	14 V, 5%, 500 mW, DO-213AA (MELF)	ZMM5244B-7	Diodes, Inc.
51	1	VR2	250 V, 1 W, 11%, DO214AC (SMA)	SMAJ250A-13	Diodes, Inc.

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7 Common Mode Choke Specification (L3)

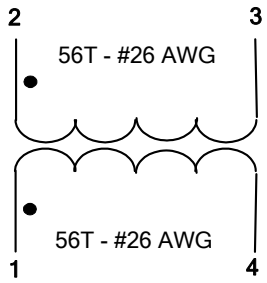

Figure 6 – CMC Electrical Diagram.

7.1 Electrical Specifications

Inductance (LCM)	Pins 1-4 or 2-3. measured at 100 kHz	12 mH ±10%
Leakage (LL)	Pins 1-4 with pins 2-3 shorted or versa at 100 kHz	80 μH (Max.) ±20%
Core Effective Inductance		3795 nH/N²

7.2 Materials

Item	Description
[1]	Toroid Core: MN-ZN T14X9X5 R10K U1000; Dimension: OD:14.35 mm / ID:7.5mm / HT:5.3mm
[2]	Magnet Wire: #26 AWG, Heavy Nyleze

7.3 Winding instructions

- Use 4 ft of item [2], start at pin 1 wind 56 turns end at pin 4.
- Do the same for another half of Toroid, start at pin 2 and end at pin 3.

7.4 Illustrations

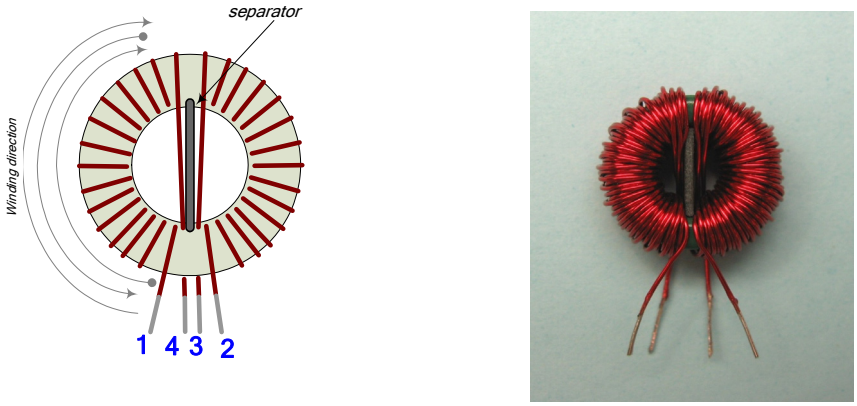

Figure 7 – CMC Build Illustration.

8 Common Mode Choke Specification (L4)

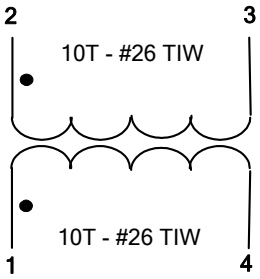

Figure 8 – CMC Electrical Diagram.

8.1 Electrical Specifications

Inductance (LCM)	Pins 1-4 or 2-3. measured at 100 kHz	47 µH ±10%
Leakage (LL)	Pins 1-4 with pins 2-3 shorted or versa at 100 kHz	0.5 µH (Max.) ±20%
Core Effective Inductance		460 nH/N²

8.2 Materials

Item	Description
[1]	Toroid Core: K5B T10X5X5 (King Core); PI P/N 32-00086-00.
[2]	Magnet Wire: #26 AWG, Triple-insulated Wire.

8.3 Winding instructions

- Use 1 ft of item [2], start at pin 1 and 2 wind 10 turns end at pin 4 and 3.

8.4 Illustrations

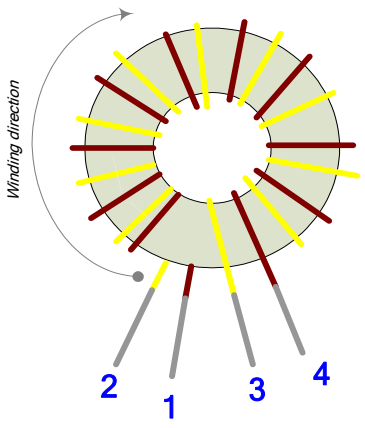

Figure 9 – CMC Build Illustration.

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9 Transformer Specification

9.1 Electrical Diagram

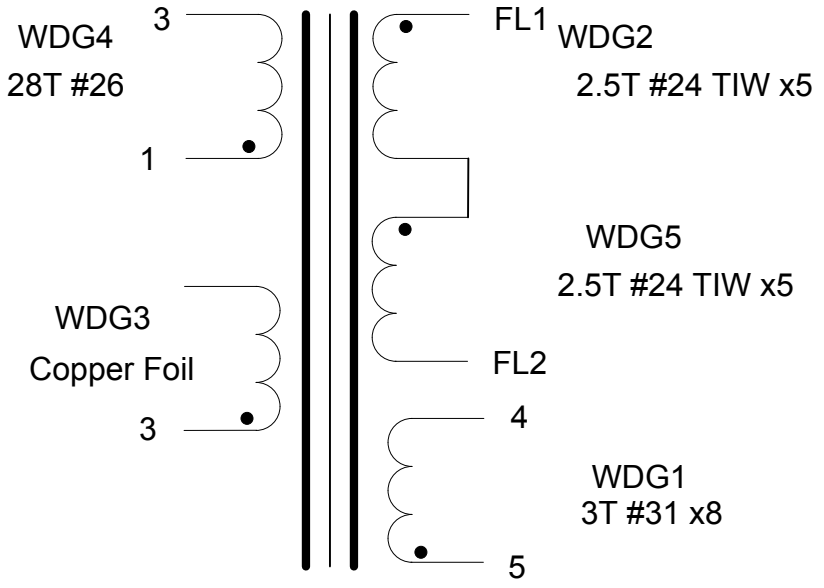

Figure 10 – Transformer Electrical Diagram.

9.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-3 to pins FL1-FL2	3000 VAC
Primary Inductance	Pins 1-3, all other windings open, measured at 100 kHz, 0.4 V_{RMS}	415 μH, -0/+5%
Resonant Frequency	Pins 1-3, all other windings open	1200 kHz (Min.)
Primary Leakage Inductance	Pins 1-3, with pins FL1-FL2 shorted, measured at 100 kHz, 0.4 V_{RMS}	3 μH (Max.)

9.3 Materials

Item	Description
[1]	Core: 3F3 Ferroxcube RM10.
[2]	Bobbin: RM10 Vertical, 5 – 0 pins.
[3]	Magnet wire: #31 AWG.
[4]	Magnet wire: #26 AWG.
[5]	Magnet wire: #24 AWG. Triple-insulated Wire.
[6]	Tape: 3M 1298 Polyester Film, 9.8 mm width.
[7]	Tape: Copper foil 2 mil, 8.0 mm width.
[8]	Varnish.

9.4 Transformer Build Diagram

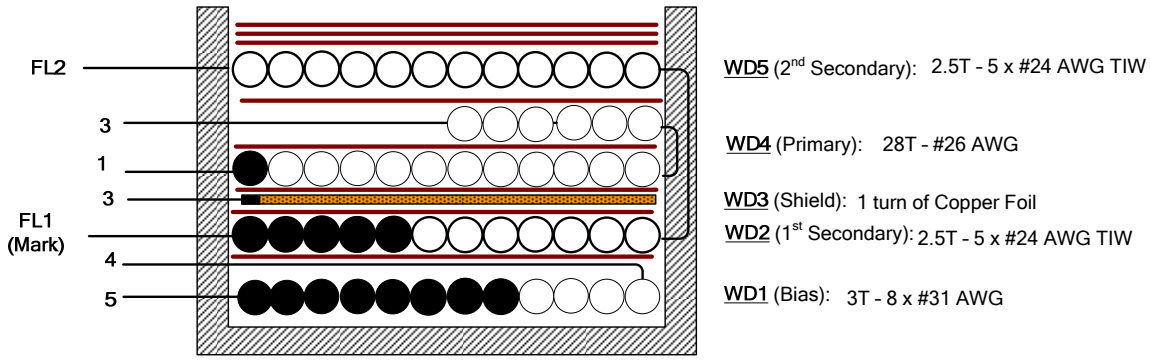

Figure 11 – Transformer Build Diagram.

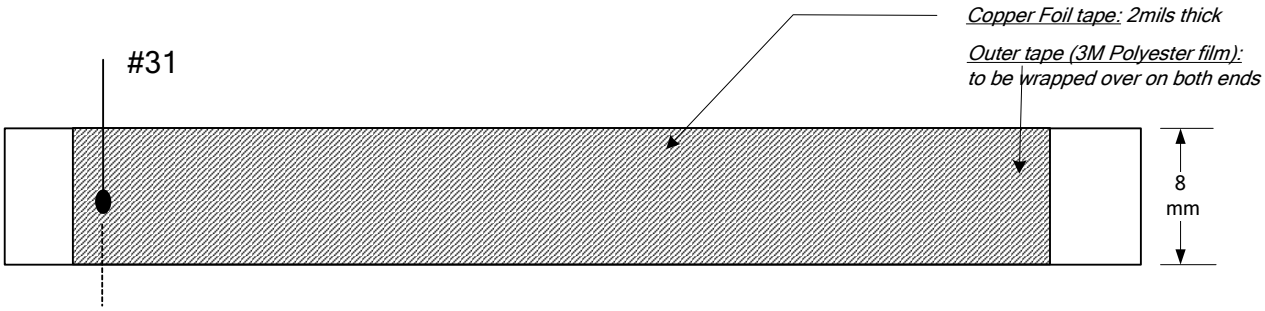

Figure 12 – Shield.

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9.5 Transformer Construction

Bobbin Preparation	Pull pin 2 on bobbin [2] to provide polarization. Position the bobbin such that the pins are on the left side of the bobbin chuck. Machine rotates in forward direction.
WDG1 Bias	Start at pin 5; wind 3 octa-filar turns of item [3], with firm tension, from left to right and finish at pin 4.
Insulation	1 Layers of tape [6] for insulation.
WDG2 Secondary	Fix FL1 and mark the wire, wind with firm tension 2.5 turns penta-filar of item [5] from left to right. Finish at uppermost of the bobbin and leave it hanging.
Insulation	1 Layers of tape [6] for insulation.
WDG3 Shield	Terminate the shield at pin 3 then wind 1 turn. Use tape of item [6] in order to avoid possible short between the start and end of the shield.
Insulation	1 Layers of tape [6] for insulation.
WDG4 Primary	Start at pin 1; wind with firm tension 18 turns of item [4] from left to right for the 1st layer. Add one layer insulation tape; continue winding remaining 10 turns from right to center for the 2nd layer. Finish at pin 3.
Insulation	1 Layers of tape [6] for insulation.
WDG5 Secondary	From WDG2 continue to wind with firm tension 2.5 turns penta-filar of item [5] from right to left. Wire end is the FL2.
Insulation	3 Layers of tape [6] for insulation.
Assemble Core	Assemble and secure the cores with core clip and glue.
Tape Barrier	Add 2 layers of tape on the left side of the transformer to isolate the core to secondary. Refer figure below:
Finish	Varnish transformer assembly.

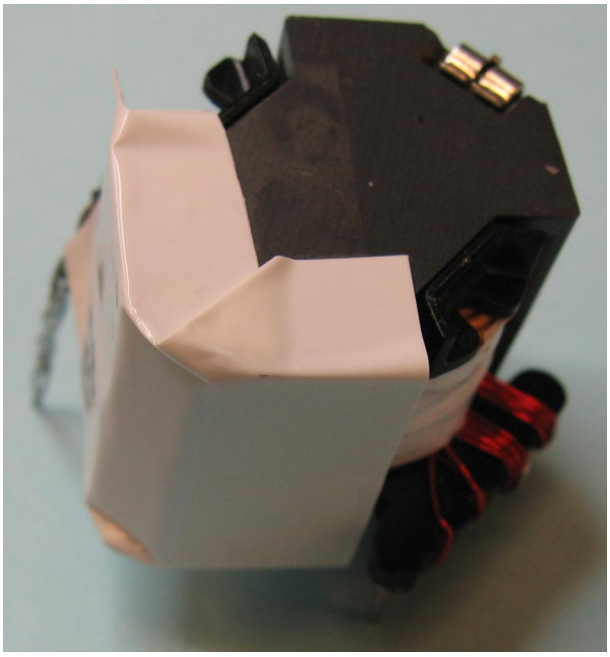

Figure 13 – Completed Transformer.

10 Transformer Design Spreadsheet

ACDC_TOPSwitchJX_120709; Rev.1.1; Copyright Power Integrations 2009	INPUT	INFO	OUTPUT	UNIT	TOP_JX_120709: TOPSwitch-JX Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	90			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	19.00			Volts	Output Voltage (main)
PO_AVG	65.00			Watts	Average Output Power
PO_PEAK			65.00	Watts	Peak Output Power
Heatsink Type	**External**		External		Heatsink Type
Enclosure	**Adapter**				Open Frame enclosure assume sufficienct airflow while adapter means a sealed enclosure.
n	0.86			%/100	Efficiency Estimate
Z	0.50				Loss Allocation Factor
VB	15			Volts	Bias Voltage - Verify that VB is > 8 V at no load and VMAX
tC	3.00			ms	Bridge Rectifier Conduction Time Estimate
CIN	110.0		110	uFarads	Input Filter Capacitor
ENTER TOPSWITCH-JX VARIABLES					
TOPSwitch-JX	**TOP269E**			Universal / Peak	115 Doubled/230V
Chosen Device		*TOP269E*	Power Out	80 W / 120 W	128W
KI	0.69				External Ilimit reduction factor (KI=1.0 for default ILIMIT, KI <1.0 for lower ILIMIT)
ILIMITMIN_EXT			2.233	Amps	Use 1% resistor in setting external ILIMIT
ILIMITMAX_EXT			2.569	Amps	Use 1% resistor in setting external ILIMIT
Frequency (F)=132kHz, (H)=66kHz	**F**		F		Select 'H' for Half frequency - 66kHz, or 'F' for Full frequency - 132kHz
fS			132000	Hertz	TOPSwitch-JX Switching Frequency: Choose between 132 kHz and 66 kHz
fSmin			119000	Hertz	TOPSwitch-JX Minimum Switching Frequency
fSmax			145000	Hertz	TOPSwitch-JX Maximum Switching Frequency
High Line Operating Mode			FF		Full Frequency, Jitter enabled
VOR	110.00			Volts	Reflected Output Voltage
VDS			10	Volts	TOPSwitch on-state Drain to Source Voltage
VD	0.50			Volts	Output Winding Diode Forward Voltage Drop
VDB	0.70			Volts	Bias Winding Diode Forward Voltage Drop
KP	0.48				Ripple to Peak Current Ratio (0.3 < KRP < 1.0 : 1.0< KDP<6.0)
PROTECTION FEATURES					
LINE SENSING					V pin functionality
VUV_STARTUP			101	Volts	Minimum DC Bus Voltage at which the power supply will start-up
VOV_SHUTDOWN			490	Volts	Typical DC Bus Voltage at which power supply will shut-down (Max)
RLS			4.4	M-ohms	Use two standard, 2.2 M-Ohm, 5% resistors in series for line sense

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					functionality.
OUTPUT OVERVOLTAGE					
VZ			27	Volts	Zener Diode rated voltage for Output Overvoltage shutdown protection
RZ			5.1	k-ohms	Output OVP resistor. For latching shutdown use 20 ohm resistor instead
OVERLOAD POWER LIMITING					X pin functionality
Overload Current Ratio at VMAX			1.2		Enter the desired margin to current limit at VMAX. A value of 1.2 indicates that the current limit should be 20% higher than peak primary current at VMAX
Overload Current Ratio at VMIN			1.10		Margin to current limit at low line.
ILIMIT_EXT_VMIN			2.02	A	Peak primary Current at VMIN
ILIMIT_EXT_VMAX			1.73	A	Peak Primary Current at VMAX
RIL			9.19	k-ohms	Current limit/Power Limiting resistor.
RPL			N/A	M-ohms	Resistor not required. Use RIL resistor only
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**Auto**		EI30		Core Type
Core		*RM10*		*P/N:*	PC40EI30-Z
Bobbin		*RM10*		*P/N:*	BE-30-1112CP
AE	0.9910		0.991	cm^2	Core Effective Cross Sectional Area
LE	4.1700		4.17	cm	Core Effective Path Length
AL	5200.0		5200	nH/T^2	Ungapped Core Effective Inductance
BW	41.5		41.5	mm	Bobbin Physical Winding Width
M	0.00			mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	1.00				Number of Primary Layers
NS	5		5		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			81	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.61		Maximum Duty Cycle (calculated at PO_PEAK)
IAVG			0.93	Amps	Average Primary Current (calculated at average output power)
IP			2.02	Amps	Peak Primary Current (calculated at Peak output power)
IR			0.97	Amps	Primary Ripple Current (calculated at average output power)
IRMS			1.22	Amps	Primary RMS Current (calculated at average output power)
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			417	uHenries	Primary Inductance
LP Tolerance	5		5		Tolerance of Primary Inductance
NP			28		Primary Winding Number of Turns
NB			4		Bias Winding Number of Turns
ALG			524	nH/T^2	Gapped Core Effective Inductance
BM		***Warning***	3013	Gauss	Operating flux density should be below 3000 Gauss, Increase turns OR increase core size
BP			4026	Gauss	Peak Flux Density (BP<4200) at ILIMITMAX and LP_MAX. Note: Recommended values for adapters and external power supplies <=3600 Gauss
BAC			723	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)

ur			1741		Relative Permeability of Ungapped Core
LG			0.21	mm	Gap Length (Lg > 0.1 mm)
BWE			41.5	mm	Effective Bobbin Width
OD			1.47	mm	Maximum Primary Wire Diameter including insulation
INS			0.09	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			1.38	mm	Bare conductor diameter
AWG			16	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			2580	Cmils	Bare conductor effective area in circular mils
CMA		*Warning*	2123	Cmils/Amp	!!! DECREASE CMA> (decrease L(primary layers),increase NS,smaller Core)
Primary Current Density (J)			0.93	Amps/mm^2	!!! Info. Primary current density is low. Can increase Primary current density. Reduce primary layers, or use smaller core
TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)					
Lumped parameters					
ISP			11.39	Amps	Peak Secondary Current
ISRMS			5.51	Amps	Secondary RMS Current
IO_PEAK			3.42	Amps	Secondary Peak Output Current
IO			3.42	Amps	Average Power Supply Output Current
IRIPPLE			4.32	Amps	Output Capacitor RMS Ripple Current
CMS			1102	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			19	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.91	mm	Secondary Minimum Bare Conductor Diameter
ODS			8.30	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS			3.69	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS					
VDRAIN			593	Volts	Maximum Drain Voltage Estimate (Includes Effect of Leakage Inductance)
PIVS			85	Volts	Output Rectifier Maximum Peak Inverse Voltage
PIVB			68	Volts	Bias Rectifier Maximum Peak Inverse Voltage
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					
VO1			19	Volts	Output Voltage
IO1_AVG			3.42	Amps	Average DC Output Current
PO1_AVG			65.00	Watts	Average Output Power
VD1			0.5	Volts	Output Diode Forward Voltage Drop
NS1			5.00		Output Winding Number of Turns
ISRMS1			5.512	Amps	Output Winding RMS Current
IRIPPLE1			4.32	Amps	Output Capacitor RMS Ripple Current
PIVS1			85	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS1			1102	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			19	AWG	Wire Gauge (Rounded up to next

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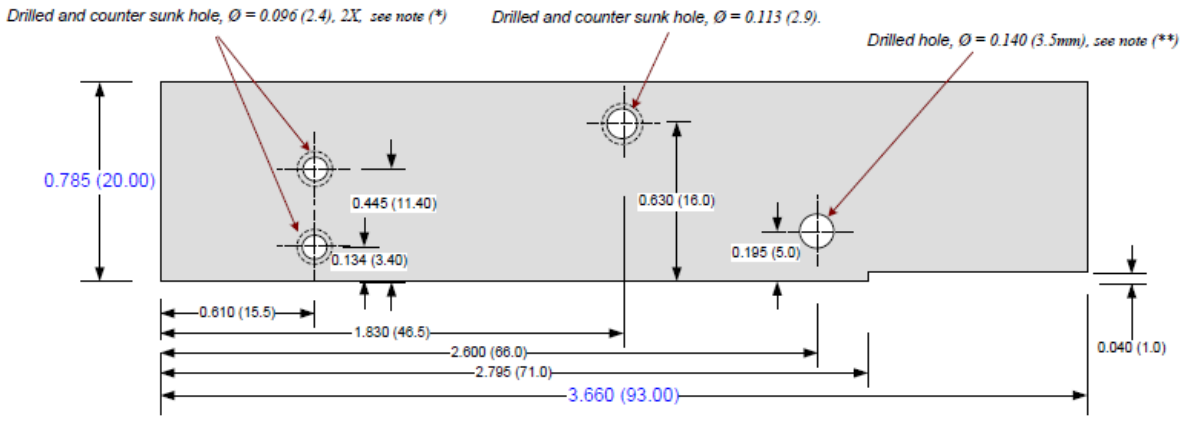
					larger standard AWG value)
DIAS1			0.91	mm	Minimum Bare Conductor Diameter
ODS1			8.30	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output					
VO2				Volts	Output Voltage
IO2_AVG				Amps	Average DC Output Current
PO2_AVG			0.00	Watts	Average Output Power
VD2			0.7	Volts	Output Diode Forward Voltage Drop
NS2			0.18		Output Winding Number of Turns
ISRMS2			0.000	Amps	Output Winding RMS Current
IRIPPLE2			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS2			2	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS2			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2			N/A	mm	Minimum Bare Conductor Diameter
ODS2			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
3rd output					
VO3				Volts	Output Voltage
IO3_AVG				Amps	Average DC Output Current
PO3_AVG			0.00	Watts	Average Output Power
VD3			0.7	Volts	Output Diode Forward Voltage Drop
NS3			0.18		Output Winding Number of Turns
ISRMS3			0.000	Amps	Output Winding RMS Current
IRIPPLE3			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS3			2	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS3			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS3			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS3			N/A	mm	Minimum Bare Conductor Diameter
ODS3			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
Total Continuous Output Power			65	Watts	Total Continuous Output Power
Negative Output			N/A		If negative output exists enter Output number; eg: If VO2 is negative output, enter 2

Note – The flux density maximum flux density limit of 3000 Gauss was slightly exceeded. It was verified that the supply did not saturate under any conditions and therefore this warning can be ignored.

11 Mechanical Parts Specification

11.1 eSIP Heat Sink



Note:
(*) Bracket (PI#: 60-00043-01) attached to heat sink with rivets: Al, 0.0093x3/16 (PI#: 75-00084-00) thru these 2 holes.
(**) Eyelet Zierick 190 (PI#: 60-00016-00) to be inserted to this hole

- Company:	Power Integration	- Material:	Al, 3003.
- Job Title:	65W-Chunky – Heat sink for eSip	- Thickness:	0.090" (2.3mm)
- Revision:	1	- Unit measurement:	Inch (mm)
- Location:		- Tolerance:	+/- 0.010 (0.2).
- PI #:	61-00037-00	- Scale:	3:2
- Drawn by:	LN Date: 10/30/09		

Figure 14 – TOPSwitch (U1) Heat Sink Drawing.

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11.2 Bridge Heat Sink

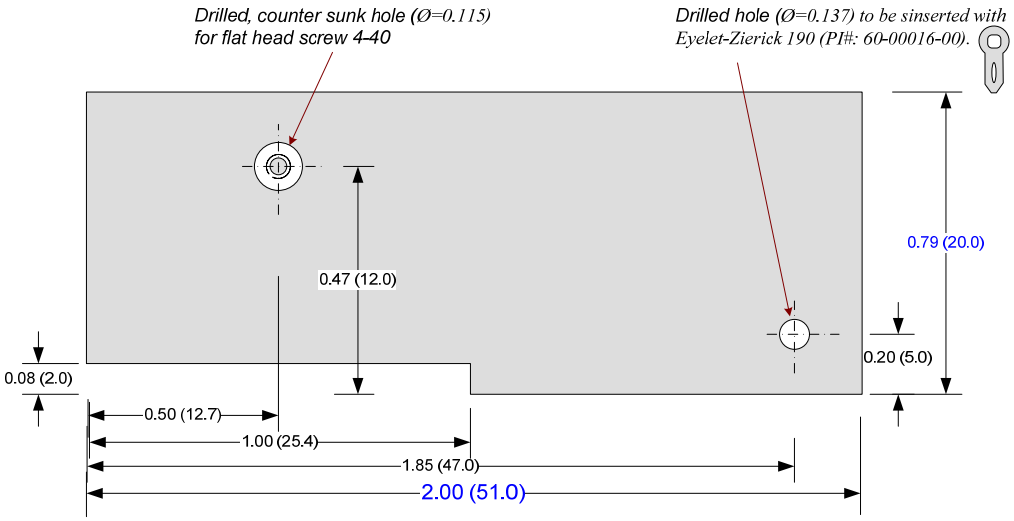
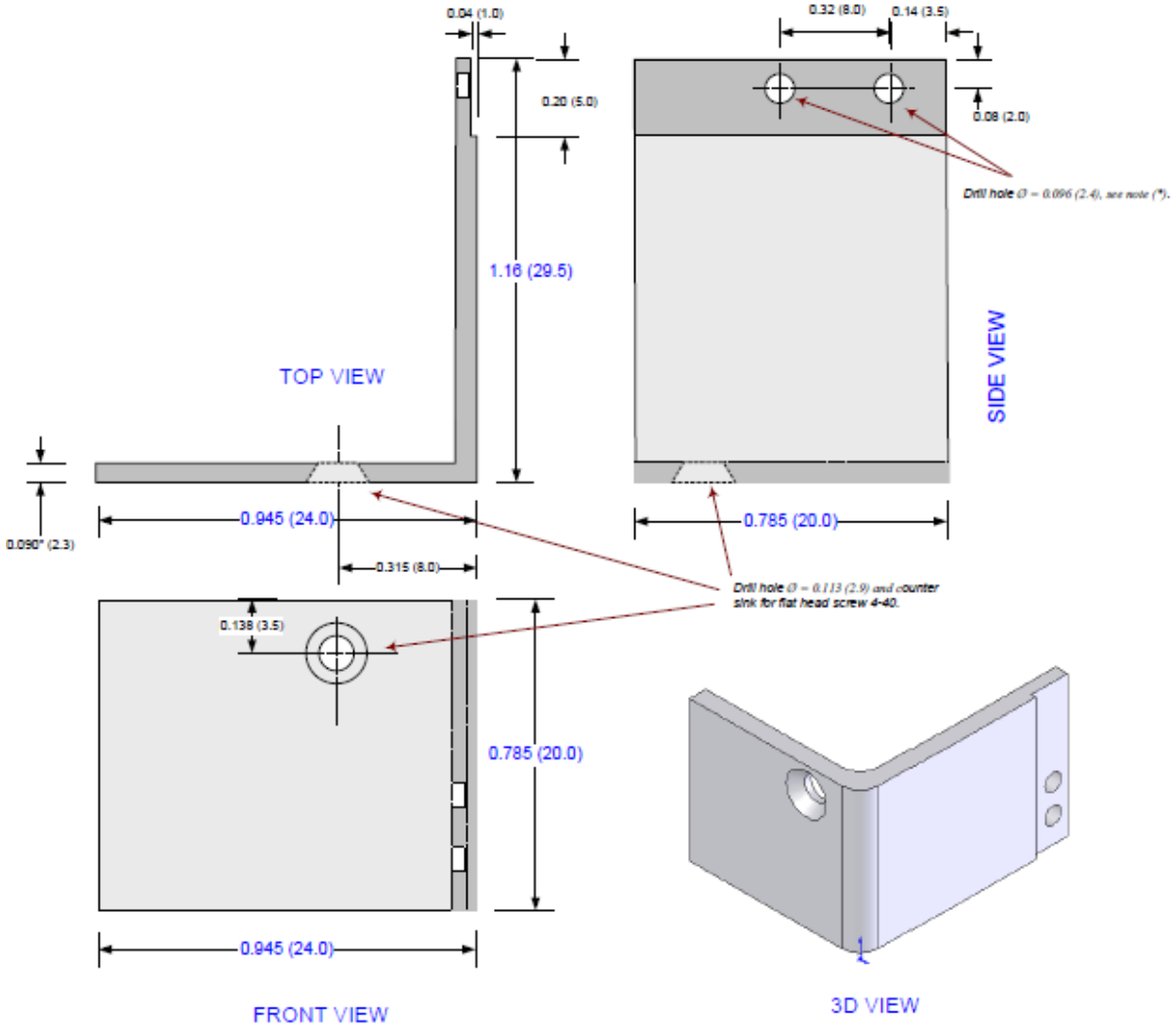


Figure 15 – Bridge (D1) Heat Sink Drawing.

11.3 Output Diode Heat Sink



Note:
(*) Bracket (PI#: 60-00043-01) attached to heat sink with rivets: Al, 0.0093x3/16 (PI#: 75-00084-00) thru these 2 holes.

- Company: Power Integration - Job Title: 65W-Chunky – Diode Heat sink - Revision: 1 - Location: - PI#: 61-00036-00 - Drawn by: LN Date: 10/30/09	- Material: Al, 3003. - Thickness: 0.090" (2.3mm) - Unit measurement: Inch (mm) - Tolerance: +/- 0.2mm (0.010) - Do not scale the drawing

Figure 16 – Output Diode (D5) Heat Sink Drawing.

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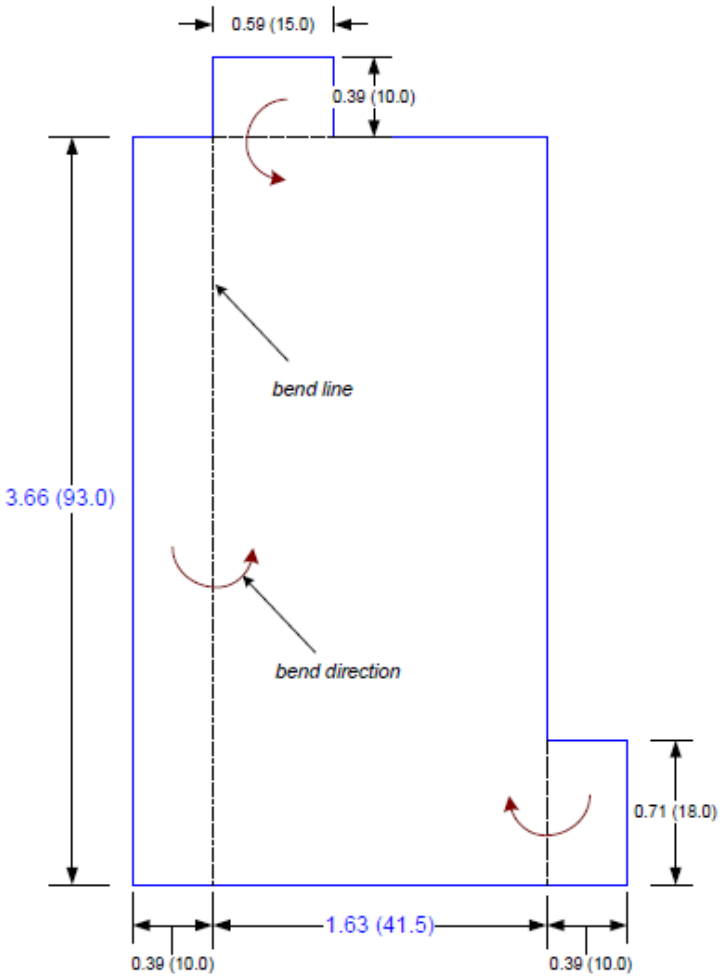
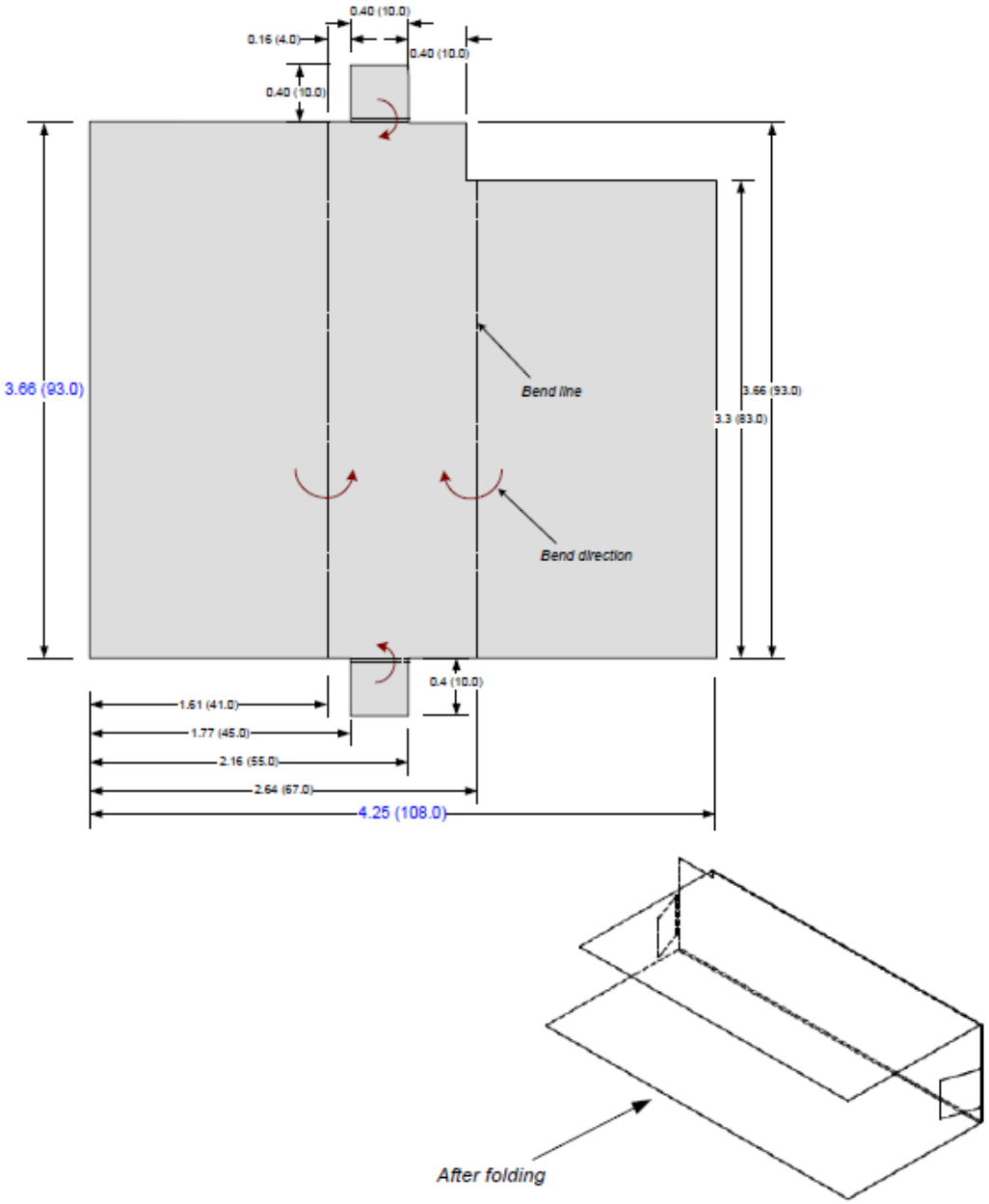
11.4 Insulator



- **Company:** Power Integration - **Job Title:** 65W-Chunky – Heat Insulator - **Revision:** 1 - **Location:** - **PI#:** 61-00038-01 - **Drawn by:** LN **Date:** 11/05/09	- **Material:** Polypropylene, (PI#: 61-00023-00). - **Thickness:** 0.010" (0.25mm) - **Unit measurement:** Inch (mm) - **Tolerance:** +/- 0.01 (0.2mm). - **Sacle:** 1/1

Figure 17 – Insulator Drawing Used to Isolate Bottom PCB Circuits to Heat Spreader.

11.5 Heat Spreader



- Company: Power Integration - Job Title: 65W-Chunky – Heat Spreader - Revision: 1 - Location: - PI#: 61-00034-00 - Drawn by: LN Date: 10/30/09	- Material: Al, 3003. - Thickness: 0.010" (0.25mm) - Unit measurement: Inch (mm) - Tolerance: +/- 0.010 (0.2) - Sacle: 1/1

Figure 18 – Heat Spreader Drawing.

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12 Performance Data

All measurements performed at room temperature, 60 Hz input frequency. All output measurements were taken at the end of a 1.8 meter #18 AWG (100 m-ohms) output cable.

12.1 Active Mode Efficiency

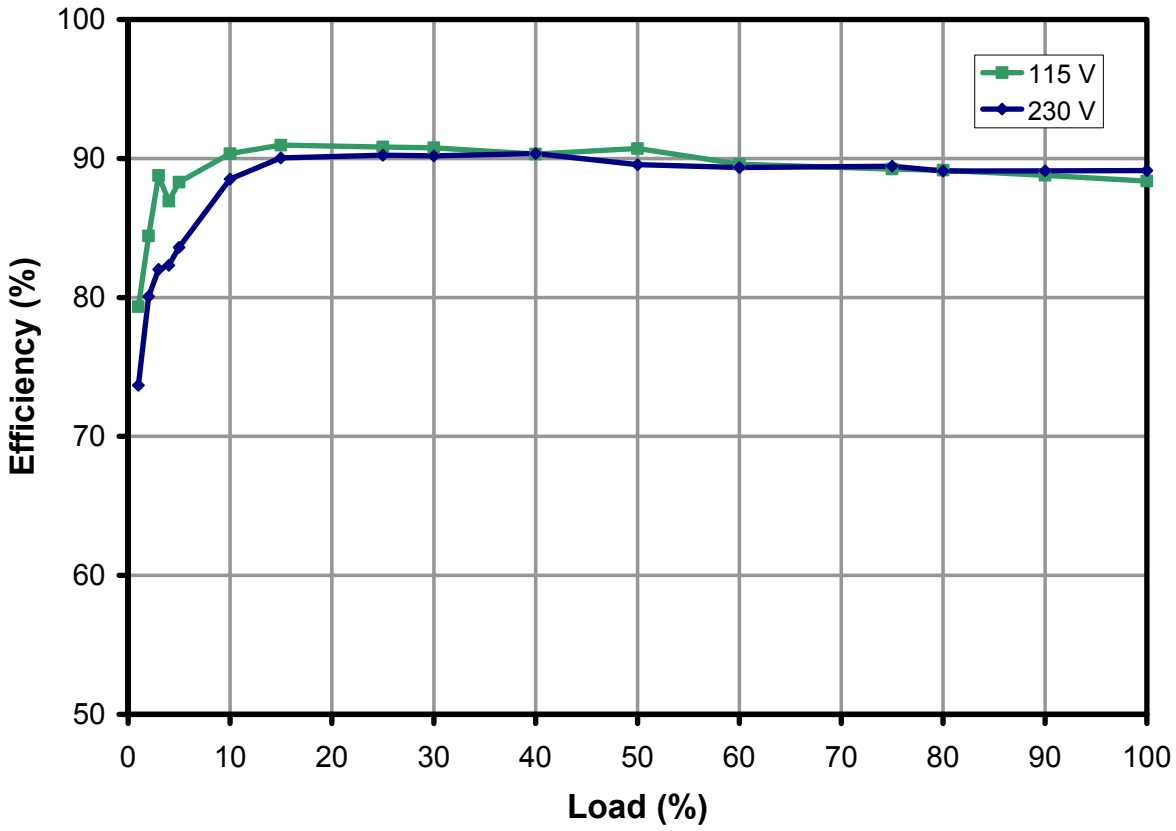

Figure 19 – Efficiency vs. Input Voltage, Room Temperature, 60 Hz.

Load (%)	I_{OUT} (A)	V_{OUT} (V)	P_{OUT} (W)	P_{IN} (W)	Efficiency (%)
1.00	0.027	19.54	0.53	0.665	79.34
2.00	0.062	19.54	1.21	1.435	84.42
3.00	0.100	19.53	1.95	2.200	88.77
4.00	0.131	19.53	2.56	2.943	86.93
5.00	0.166	19.52	3.24	3.670	88.29
10.00	0.335	19.50	6.53	7.230	90.35
15.00	0.505	19.49	9.84	10.820	90.97
25.00	0.849	19.45	16.51	18.180	90.83
30.00	1.018	19.43	19.78	21.790	90.77
40.00	1.357	19.40	26.33	29.150	90.31

50.00	1.700	19.36	32.91	36.280	90.72
60.00	2.039	19.32	39.39	43.970	89.59
75.00	2.550	19.26	49.11	55.030	89.25
80.00	2.721	19.24	52.35	58.720	89.16
90.00	3.064	19.20	58.83	66.250	88.80
100.00	3.418	19.16	65.49	74.100	88.38
				Average Efficiency	**89.79**

Table 1 – Data at 115 VAC / 60 Hz for Figure 19.

Load (%)	I_{OUT} (A)	V_{OUT} (V)	P_{OUT} (W)	P_{IN} (W)	Efficiency (%)
1.00	0.027	19.54	0.53	0.716	73.68
2.00	0.062	19.54	1.21	1.513	80.07
3.00	0.097	19.53	1.89	2.310	82.01
4.00	0.131	19.53	2.56	3.108	82.32
5.00	0.166	19.52	3.24	3.876	83.60
10.00	0.335	19.50	6.53	7.380	88.52
15.00	0.505	19.49	9.84	10.930	90.05
25.00	0.849	19.45	16.51	18.300	90.24
30.00	1.018	19.43	19.78	21.930	90.19
40.00	1.357	19.40	26.33	29.140	90.34
50.00	1.700	19.36	32.91	36.750	89.56
60.00	2.039	19.33	39.41	44.110	89.35
75.00	2.552	19.27	49.18	54.980	89.45
80.00	2.721	19.25	52.38	58.790	89.10
90.00	3.060	19.22	58.81	66.000	89.11
100.00	3.420	19.18	65.60	73.600	89.12
				Average Efficiency	**89.59**

Table 2 – Data at 230 VAC / 50Hz for Figure 19.

Percent of Full Load	Efficiency (%)	
	115 VAC	**230 VAC**
25	90.83	90.24
50	90.72	89.56
75	89.32	89.45
100	88.38	89.07
Average	**89.81**	**89.53**
US EISA (2007) requirement	*85*	
ENERGY STAR 2.0 requirement	*87*	

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12.2 Energy Efficiency Requirements

The external power supply requirements below all require meeting active mode efficiency and no-load input power limits. Minimum active mode efficiency is defined as the average efficiency of 25, 50, 75 and 100% of output current (based on the nameplate output current rating).

For adapters that are single input voltage only then the measurement is made at the rated single nominal input voltage (115 VAC or 230 VAC), for universal input adapters the measurement is made at both nominal input voltages (115 VAC and 230 VAC).

To meet the standard the measured average efficiency (or efficiencies for universal input supplies) must be greater than or equal to the efficiency specified by the standard.

The test method can be found here:

http://www.energystar.gov/ia/partners/prod_development/downloads/power_supplies/EPSupplyEffic_TestMethod_0804.pdf

For the latest up to date information please visit the PI Green Room:

http://www.powerint.com/greenroom/regulations.htm

12.2.1 USA Energy Independence and Security Act 2007

This legislation mandates all single output single output adapters, including those provided with products, manufactured on or after July 1st, 2008 must meet minimum active mode efficiency and no load input power limits.

Active Mode Efficiency Standard Models

Nameplate Output (P_O)	**Minimum Efficiency in Active Mode of Operation**
< 1 W	$0.5 \times P_O$
≥ 1 W to ≤ 51 W	$0.09 \times \ln(P_O) + 0.5$
> 51 W	0.85

ln = natural logarithm

No-load Energy Consumption

Nameplate Output (P_O)	**Maximum Power for No-load AC-DC EPS**
All	≤ 0.5 W

This requirement supersedes the legislation from individual US States (for example CEC in California).

12.2.2 ENERGY STAR EPS Version 2.0
This specification takes effect on November 1st, 2008.

Active Mode Efficiency Standard Models

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
≤ 1 W	$0.48 \times P_O + 0.14$
> 1 W to ≤ 49 W	$0.0626 \times \ln(P_O) + 0.622$
> 49 W	0.87

ln = natural logarithm

Active Mode Efficiency Low Voltage Models (V_O<6 V and $I_O \geq 550$ mA)

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
≤ 1 W	$0.497 \times P_O + 0.067$
> 1 W to ≤ 49 W	$0.075 \times \ln(P_O) + 0.561$
> 49 W	0.86

ln = natural logarithm

No-load Energy Consumption (both models)

Nameplate Output (P_O)	Maximum Power for No-load AC-DC EPS
0 to < 50 W	≤ 0.3 W
≥ 50 W to ≤ 250 W	≤ 0.5 W

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12.3 No-load Input Power

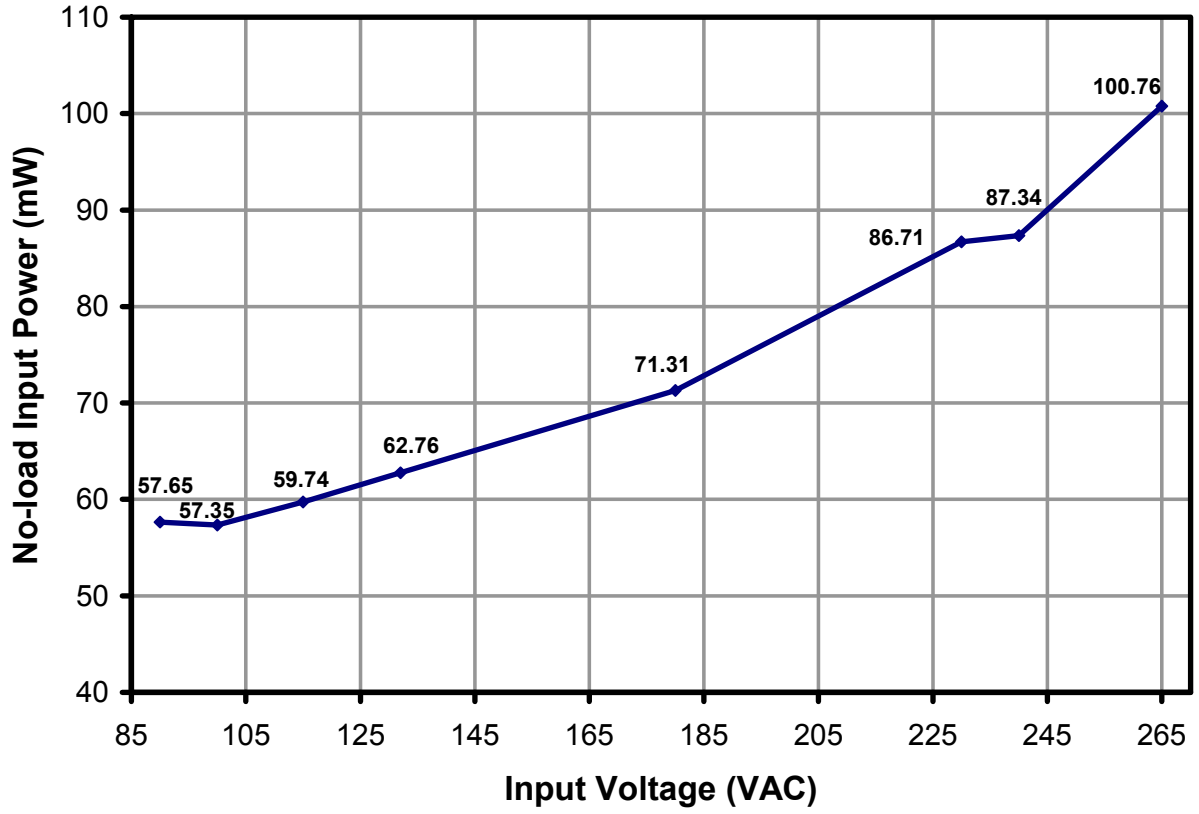

Figure 20 – Zero Load Input Power vs. Input Line Voltage, Room Temperature, 60 Hz.

Input Line	P_{IN} (mW)	V_{OUT}
90 V / 50 Hz	57.648	19.6
100 V / 50 Hz	57.348	19.6
115 V / 60 Hz	59.736	19.6
132 V / 60 Hz	62.760	19.6
180 V / 50 Hz	71.310	19.6
230 V / 50 Hz	86.712	19.6
240 V / 50 Hz	87.342	19.6
265 V / 50 Hz	100.764	19.6

Table 3 – No-load Input Power vs. Input Voltage.

12.4 Available Standby Output Power

The chart below shows the available output power vs. line voltage for an input power of 1 W, 2 W and 3 W.

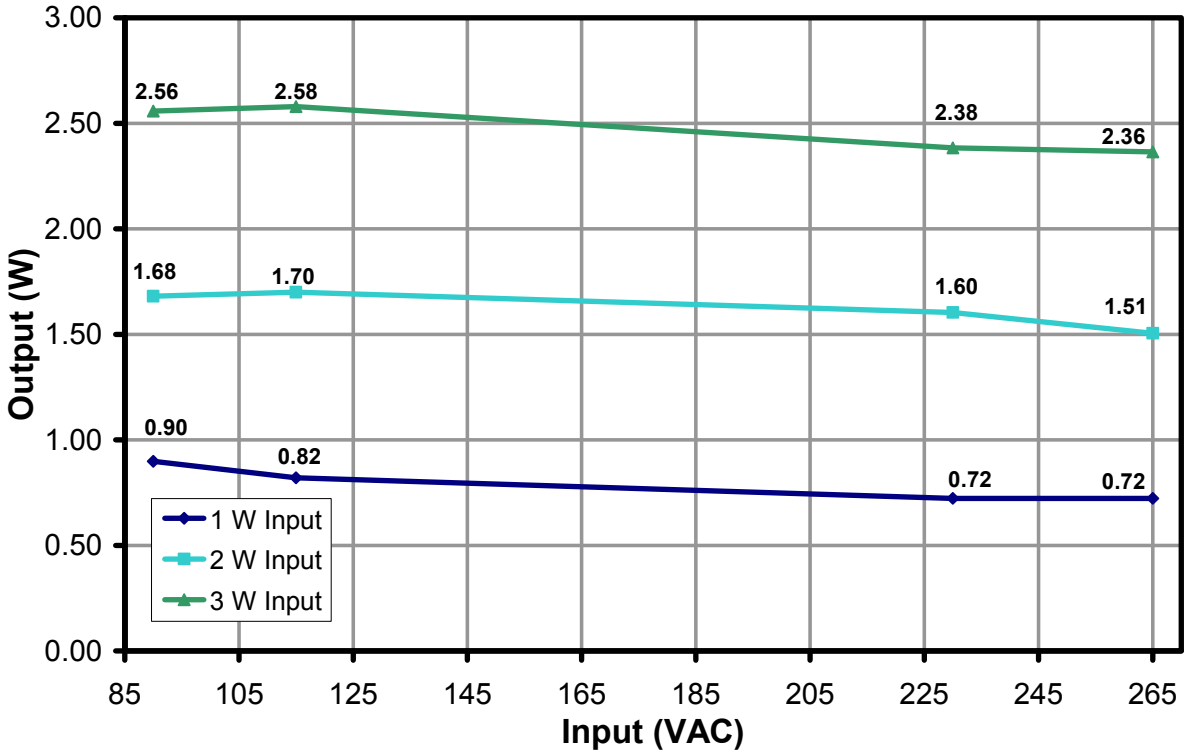

Figure 21 – Available Standby Power.

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12.5 Regulation

12.5.1 Load

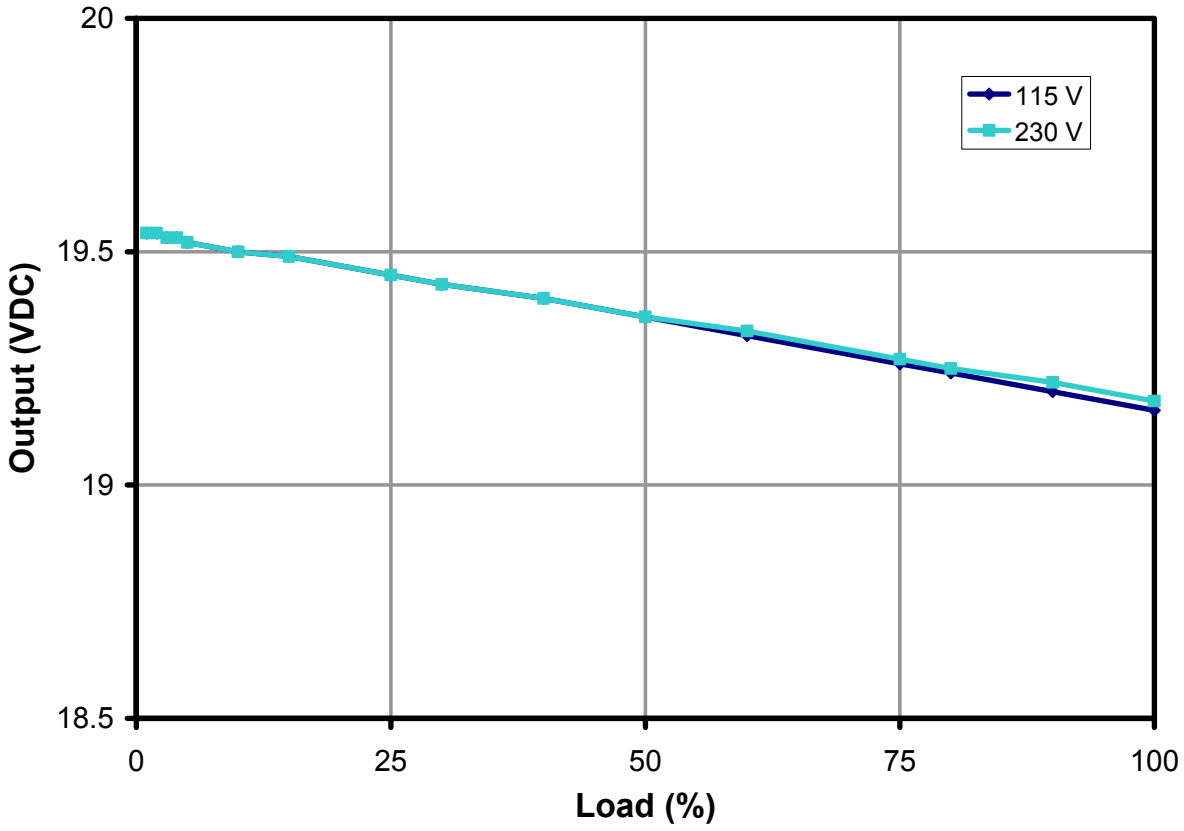

Figure 22 – Load Regulation, Room Temperature.

12.5.2 Line

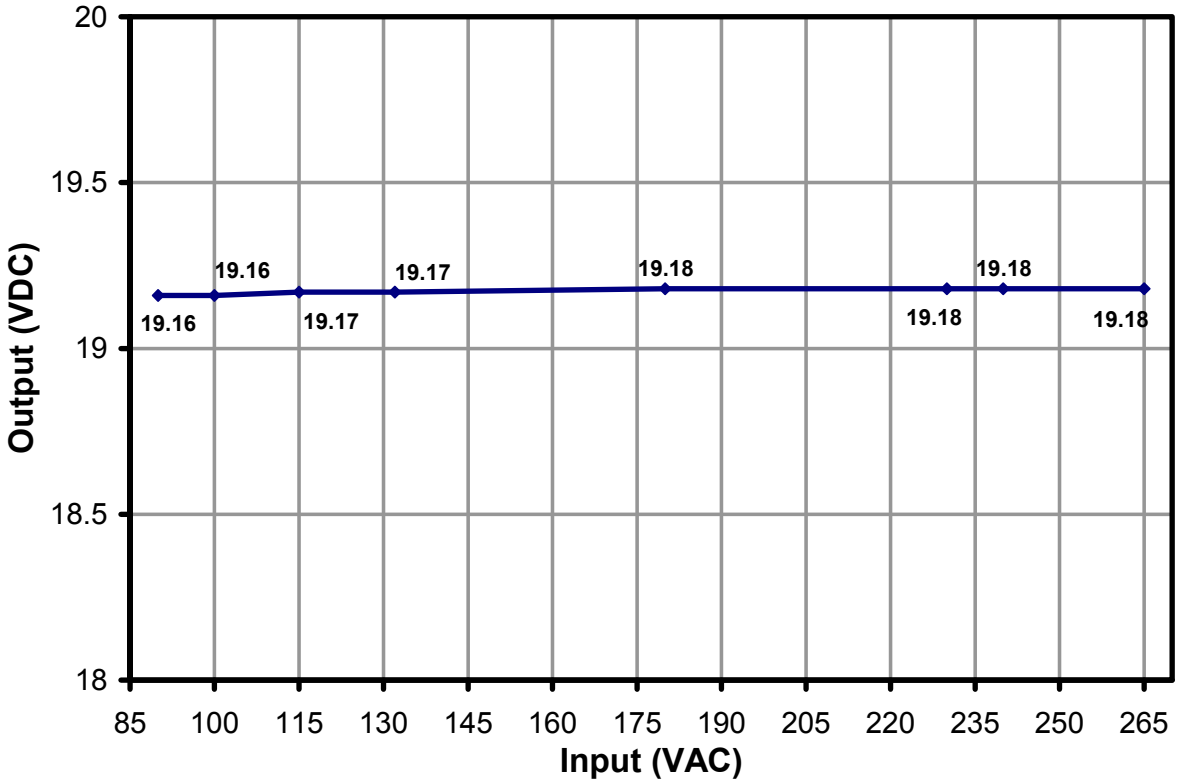

Figure 23 – Line Regulation, Room Temperature, Full Load.

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12.6 Efficiency

12.6.1 Line

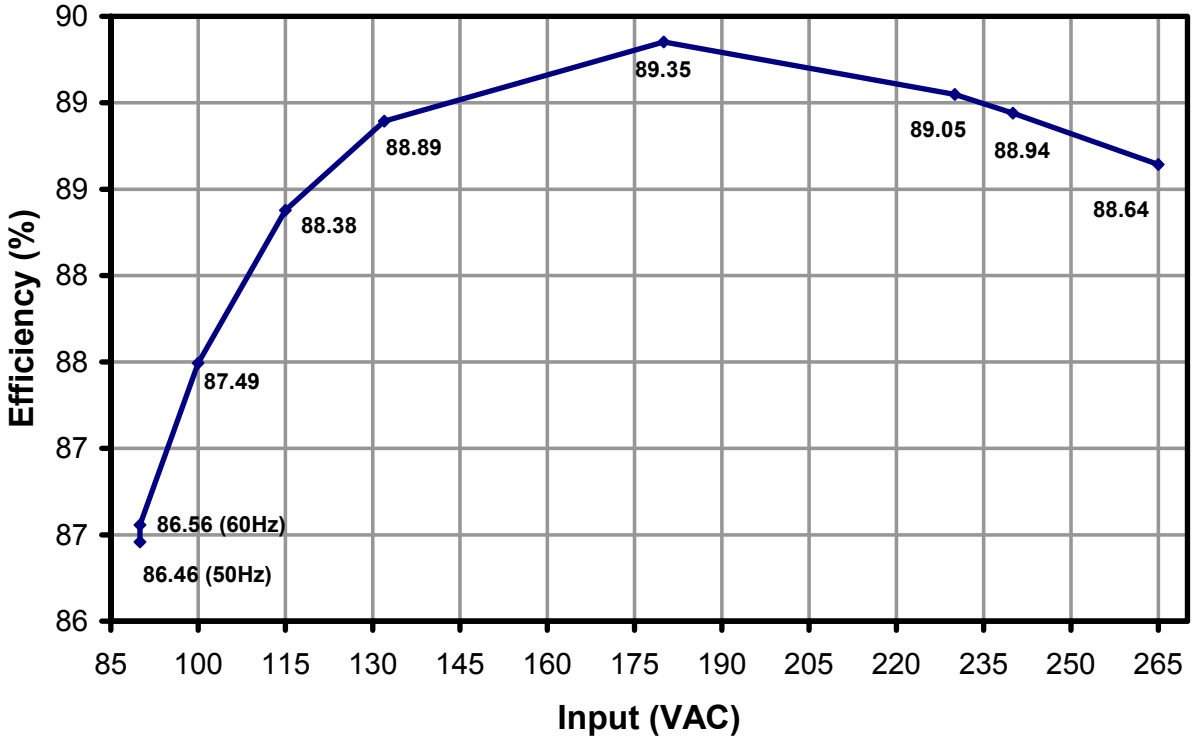

Figure 24 – Line Efficiency at Full-load, Room Temperature.

13 Thermal Performance

The power supply was placed inside a sealed adapter plastic case to restrict airflow. The chamber temperature was controlled to maintain a constant temperature inside the box. The supply was operated at its rated output power (65 W). To measure the device (U1) temperature, a T-type thermocouple was attached on to the tab. The input diode (D1) and output diode (D5) temperature was measured by attaching a thermocouple to its case. The transformer (T1) core temperature was measured by attaching thermocouple firmly to the outer side of the winding and core.

Item	Temperature (°C)				
	90 VAC 47 Hz	90 VAC 60 Hz	115 VAC 60 Hz	230 VAC 50 Hz	265 VAC 63 Hz
Ambient	40	40	40	40	40
Common Mode (L3)	112.8	112.6	103	95.5	78.8
Bridge (D1)	107.8	106.6	99	91.5	75.8
***PI Device* (TOP269) (U1)**	98.8	96.6	91	85.5	85.8
Transformer Core (T1)	105.8	100.6	100	96.5	103.8
Transformer Winding (T1)	111.8	107.6	106	102.5	106.8
Rectifier (D5)	115.8	114.6	111	108.5	113.8

Table 4 – Thermal Data at Full Load

Figure 25 – Thermal Unit Set-up.

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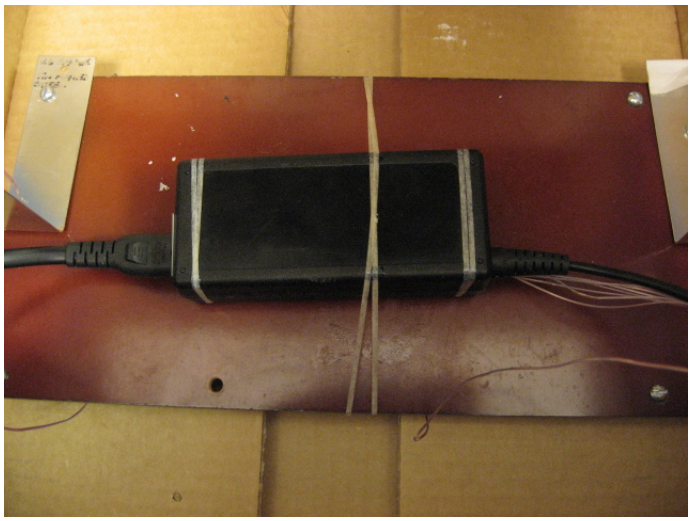

Figure 26 – Unit Inside the Box to Avoid Chamber Fan Influence.

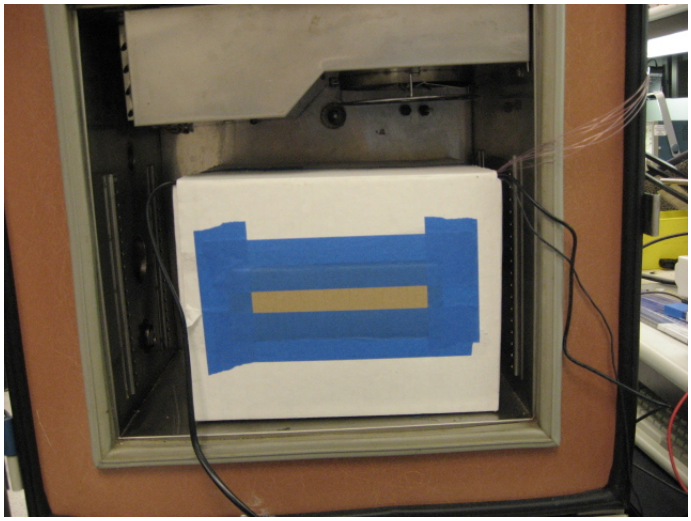

Figure 27 – Chamber Set-up.

14 Waveforms

14.1 Drain Voltage and Current, Normal Operation

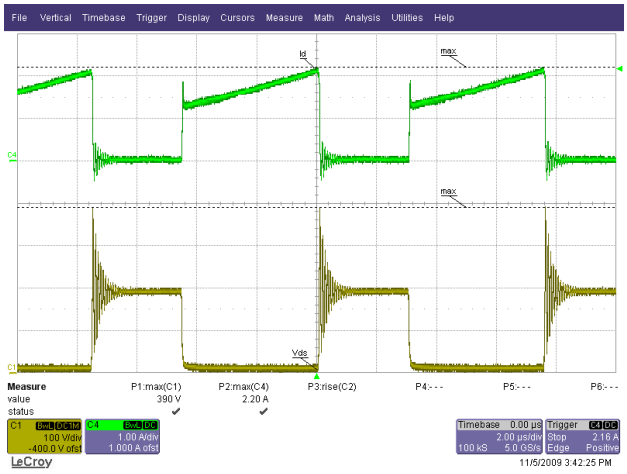

Figure 28 – 90 VAC, Full Load.
Upper: I_{DRAIN}, 1 A / div.
Lower: V_{DRAIN}, 100 V, 2 µs / div.

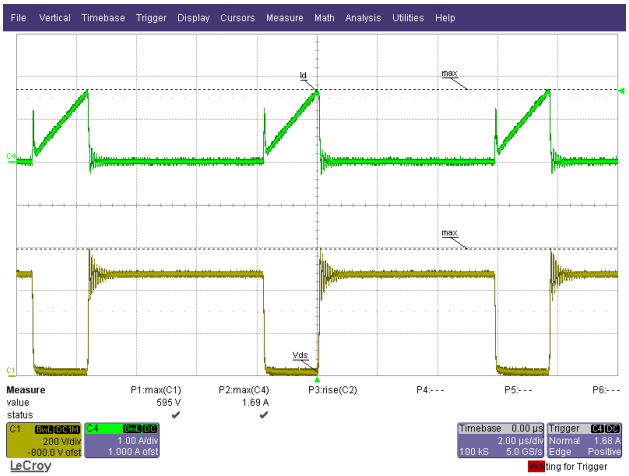

Figure 29 – 265 VAC, Full Load.
Upper: I_{DRAIN}, 1 A / div.
Lower: V_{DRAIN}, 200 V / div.

14.2 Drain Voltage and Current Start-up Profile

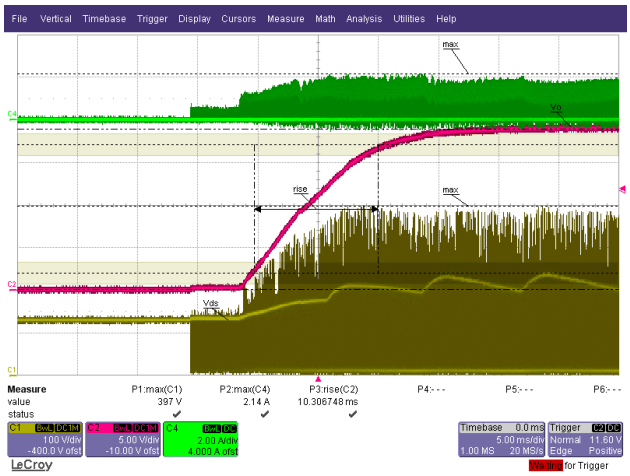

Figure 30 – 90 VAC, Full Load.
Upper: I_{DRAIN}, 2 A / div.
Center: V_{OUT}, 5 V / div.
Lower: V_{DRAIN}, 100 V / div.
Time Scale: 5 ms / div.

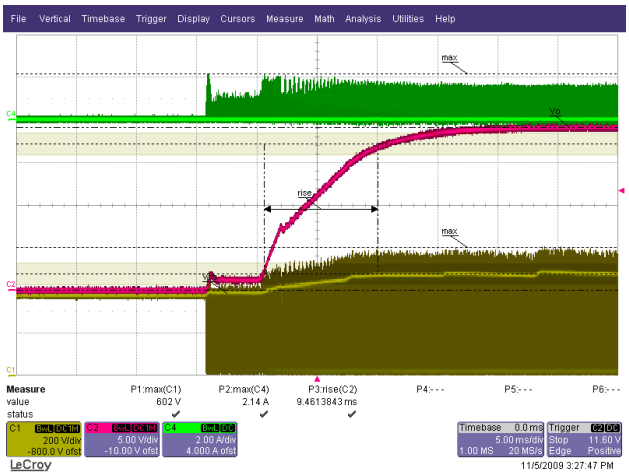

Figure 31 – 265 VAC, Full Load.
Upper: I_{DRAIN}, 2 A / div.
Center: V_{OUT}, 5 V / div.
Lower: V_{DRAIN}, 200 V / div.
Time Scale: 5 ms / div.

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14.3 Output Voltage Start-up Profile

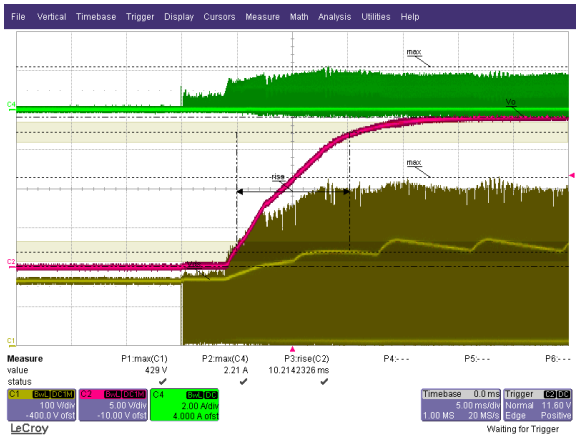

Figure 32 – 115 VAC, Full Load.
Upper: I_{DRAIN}, 2 A / div.
Center: V_{OUT}, 5 V / div.
Lower: V_{DRAIN}, 100 V / div.
Time Scale: 5 ms / div.

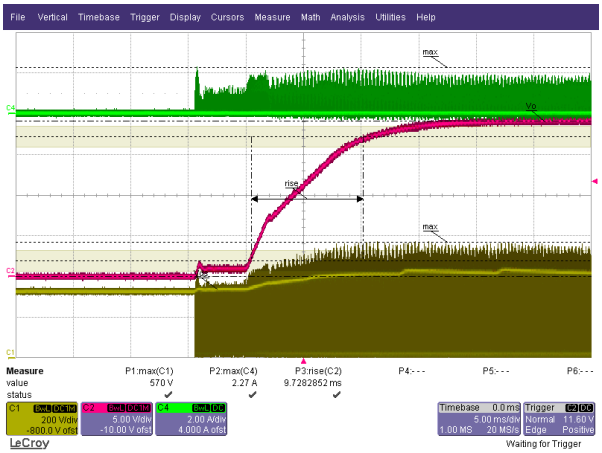

Figure 33 – 230 VAC, Full Load.
Upper: I_{DRAIN}, 2 A / div.
Center: V_{OUT}, 5 V / div.
Lower: V_{DRAIN}, 200 V / div.
Time Scale: 5 ms / div.

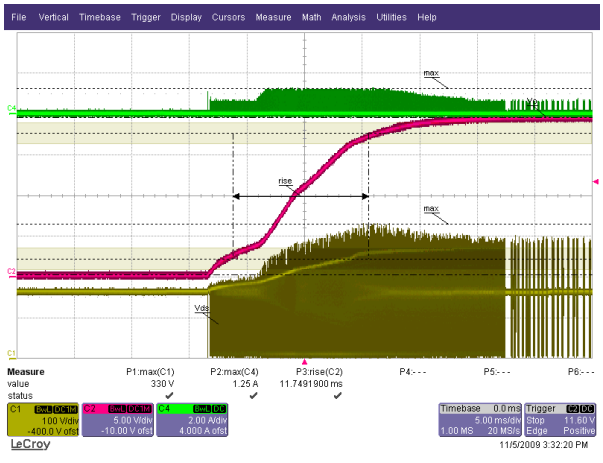

Figure 34 – 115 VAC, No-load.
Upper: I_{DRAIN}, 2 A / div.
Center: V_{OUT}, 5 V / div.
Lower: V_{DRAIN}, 100 V / div.
Time Scale: 5 ms / div.

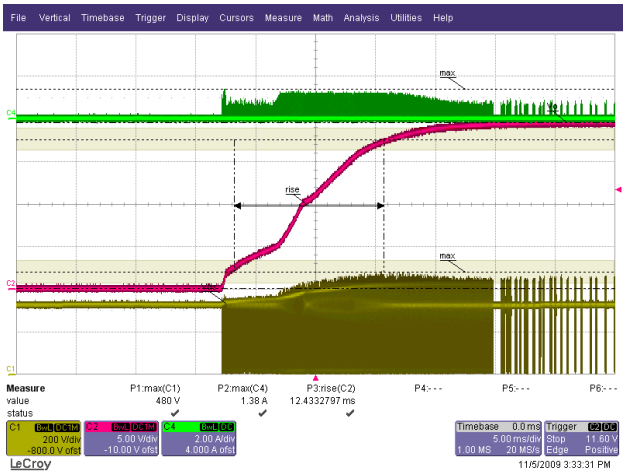

Figure 35 – 230 VAC, No-load.
Upper: I_{DRAIN}, 2 A / div.
Center: V_{OUT}, 5 V / div.
Lower: V_{DRAIN}, 200 V / div.
Time Scale: 5 ms / div.

14.4 Output Short and OCP

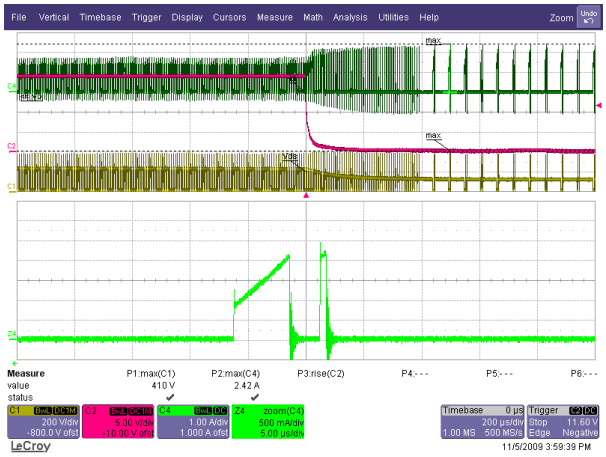

Figure 36 – 90 VAC, Full Load then Output Short.
Upper: I_{DRAIN}, 2 A / div.
Center: V_{OUT}, 5 V / div.
Lower: 100 V / div.
Time Scale: 200 µs / div.

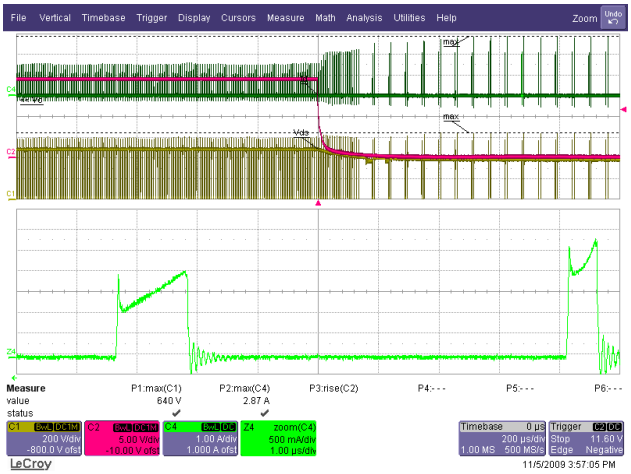

Figure 37 – 265 VAC, Full Load then Output Short.
Upper: I_{DRAIN}, 2 A / div.
Center: V_{OUT}, 5 V / div.
Lower: 100 V / div.
Time Scale: 200 µs / div.

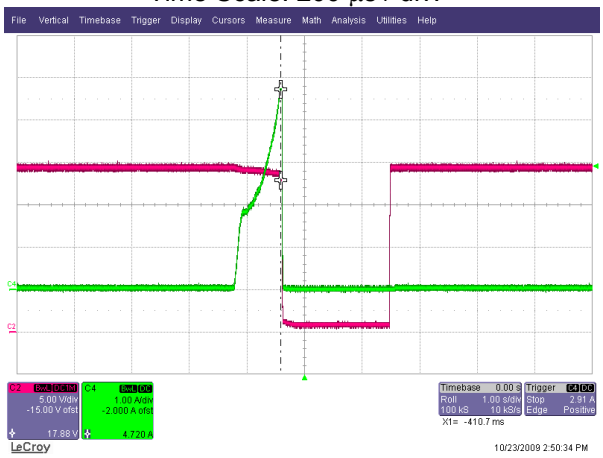

Figure 38 – 115 VAC, OCP Auto Recovery.
Upper: I_{OUT}, 1 A / div.
Lower: V_{OUT}, 5 V / div.

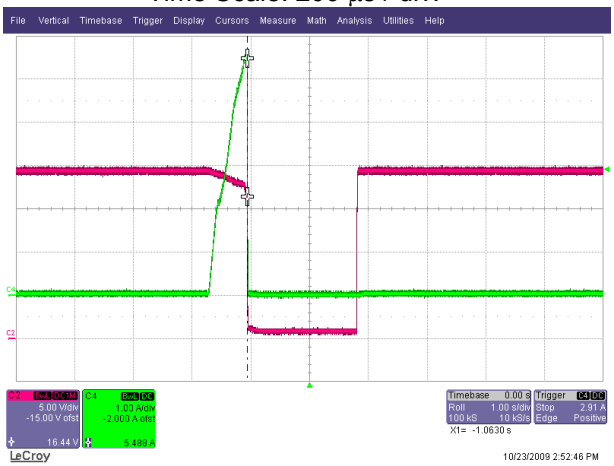

Figure 39 – 230 VAC, OCP Auto Recovery.
Upper: I_{OUT}, 1 A / div.
Center: V_{OUT}, 5 V / div.

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14.5 Overvoltage Protection (Open Loop Test)

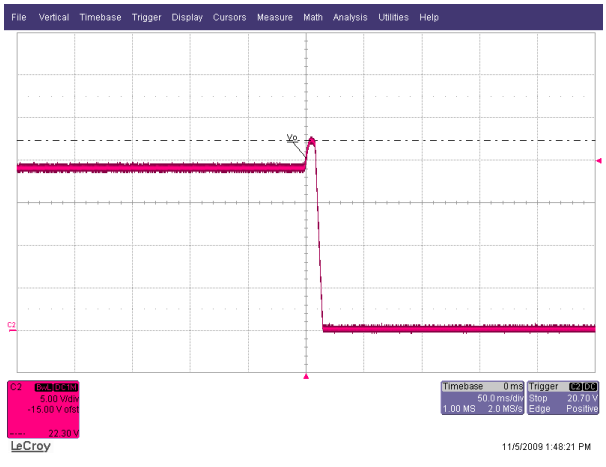

Figure 40 – OVP at 90 VAC, Full load.
OVP Trip Point = 22.3 V.

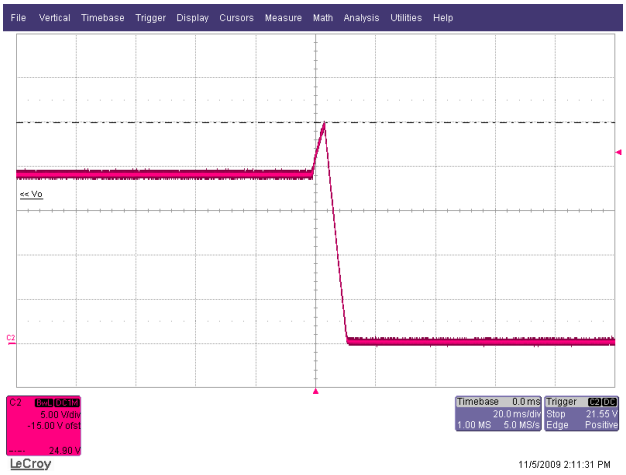

Figure 41 – OVP at 265 VAC, Full Load.
OVP Trip Point = 24.9 V.

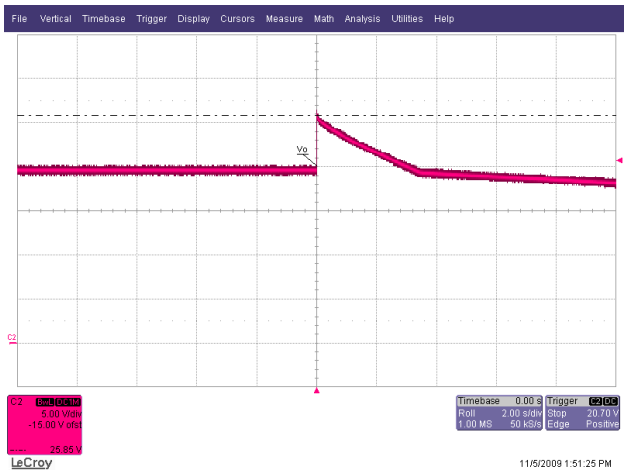

Figure 42 – OVP at 90 VAC, No-load.
OVP Trip Point = 25.85 V.

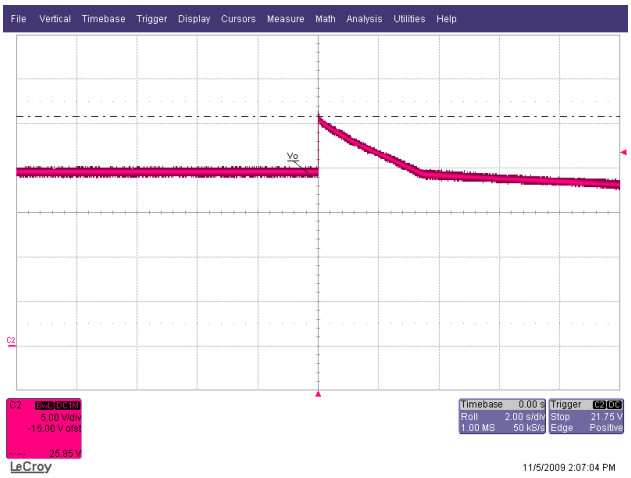

Figure 43 – OVP at 265 VAC, Full Load.
OVP Trip Point = 25.85 V.

14.6 Load Transient Response

In the figures shown below, output offset was used to enable view the load transient response. The oscilloscope was triggered using the load current step as a trigger source. A capacitive load of 560 μF / 35 V is terminated at the end of the cable. Higher than this value will further improve the overshoot and undershoot of the output and better performance above 90 VAC input voltage.

Figure 44 – Transient Response, 90 VAC,
0.1 A - 3.4 A - 0.1 A Load Step.
Upper: Load Current, 1 A / div.
Lower: V_{OUT} ,1 V / div.
Time Scale: 10 ms / div.

Figure 45 – Transient Response, 90 VAC,
25-100-25% Load Step.
Upper: Load Current, 1 A / div.
Lower: V_{OUT} ,1 V / div.
Time Scale:10 ms / div.

Figure 46 – Transient Response, 90 VAC,
50-100-50% Load Step.
Upper: Load Current, 1 A / div.
Lower: V_{OUT} ,1 V / div.
Time Scale: 10 ms / div.

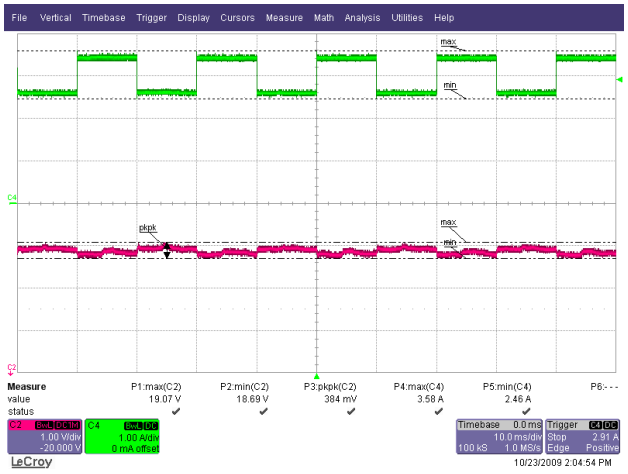

Figure 47 – Transient Response, 90VAC,
75-100-75% Load Step.
Upper: Load Current, 1 A / div.
Lower: V_{OUT} ,1 V / div.
Time Scale:10 ms / div.

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14.7 Output Ripple Measurements

14.7.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47.0 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

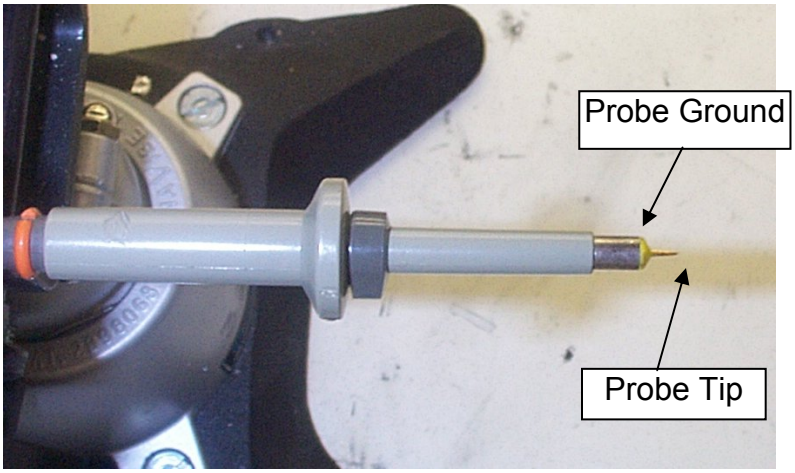

Figure 48 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

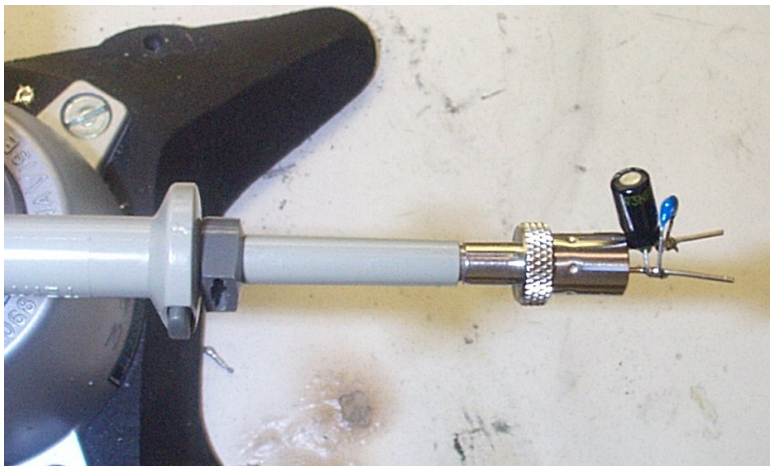

Figure 49 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

14.7.2 Ripple and Noise Measurement Results

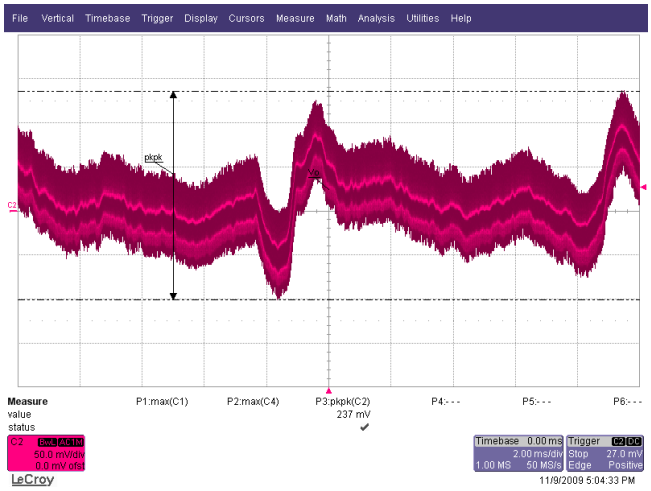

Figure 50 – Ripple, 90 VAC, Full Load.
2 ms, 50 mV / div.

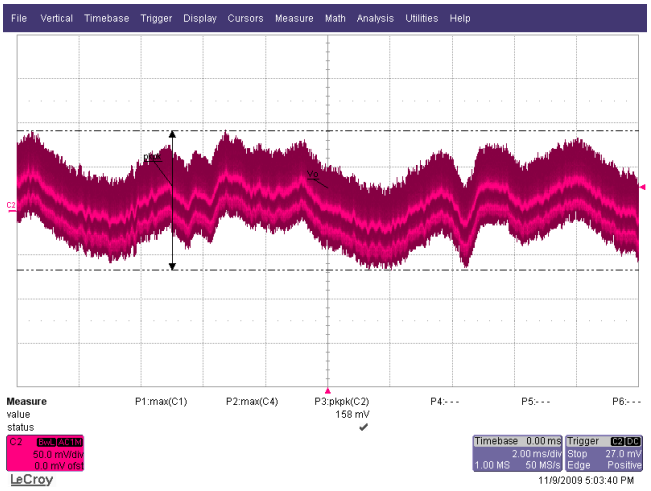

Figure 51 – 5 V Ripple, 115 VAC, Full Load.
2 ms, 50 mV / div.

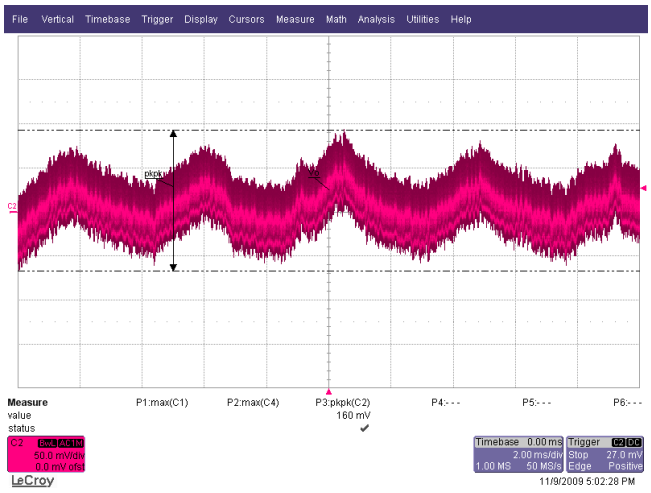

Figure 52 – Ripple, 230 VAC, Full Load.
2 ms, 50 mV /div.

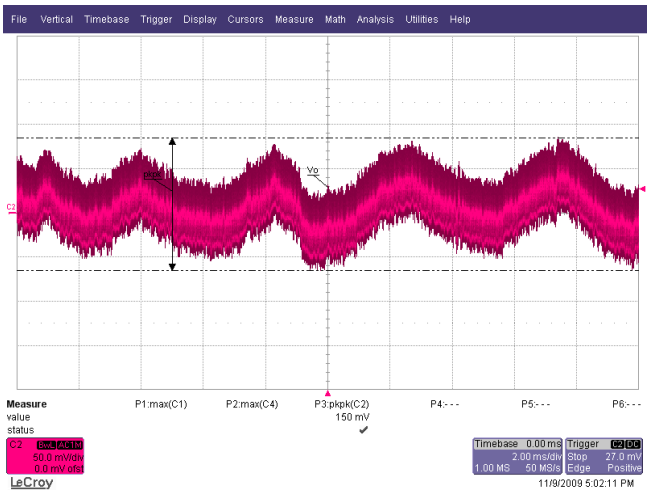

Figure 53 – Ripple, 265 VAC, Full Load.
2 ms, 50 mV /div.

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15 Control Loop Measurements

15.1 115 VAC Maximum Load

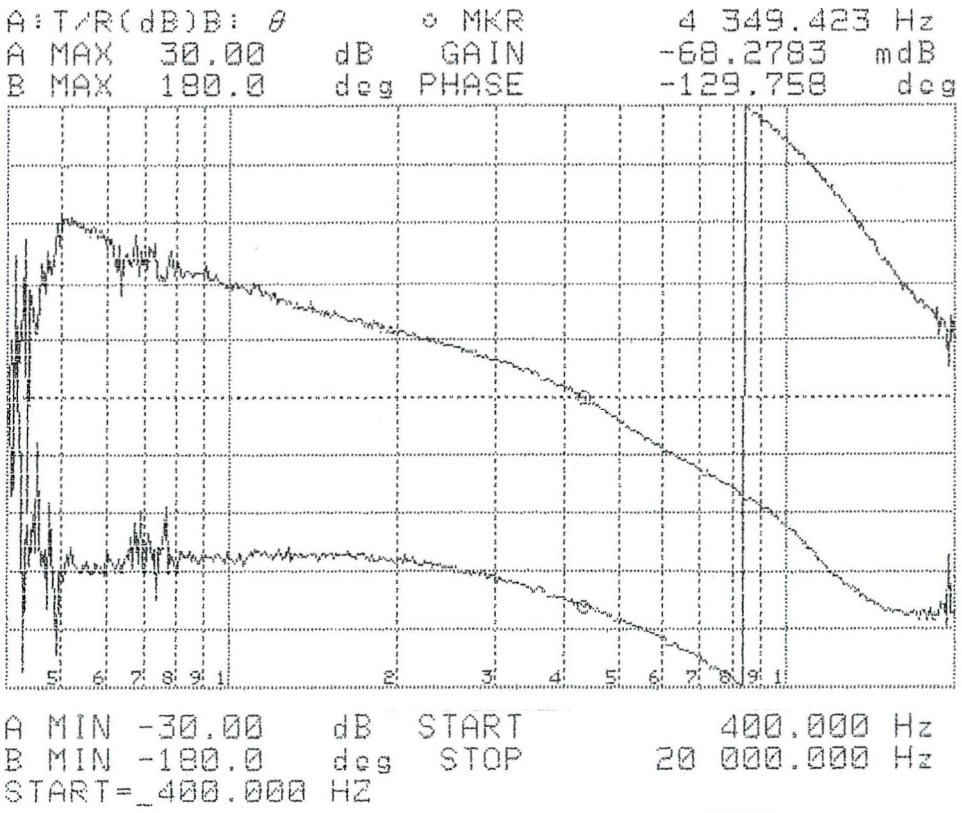

Figure 54 – Gain-Phase Plot, 115 VAC, Maximum Steady State Load.
Vertical Scale: Gain = 6 dB / div., Phase = 36 °/div.
Crossover Frequency = 4.3 kHz Phase Margin = 50°.

15.2 230 VAC Maximum Load

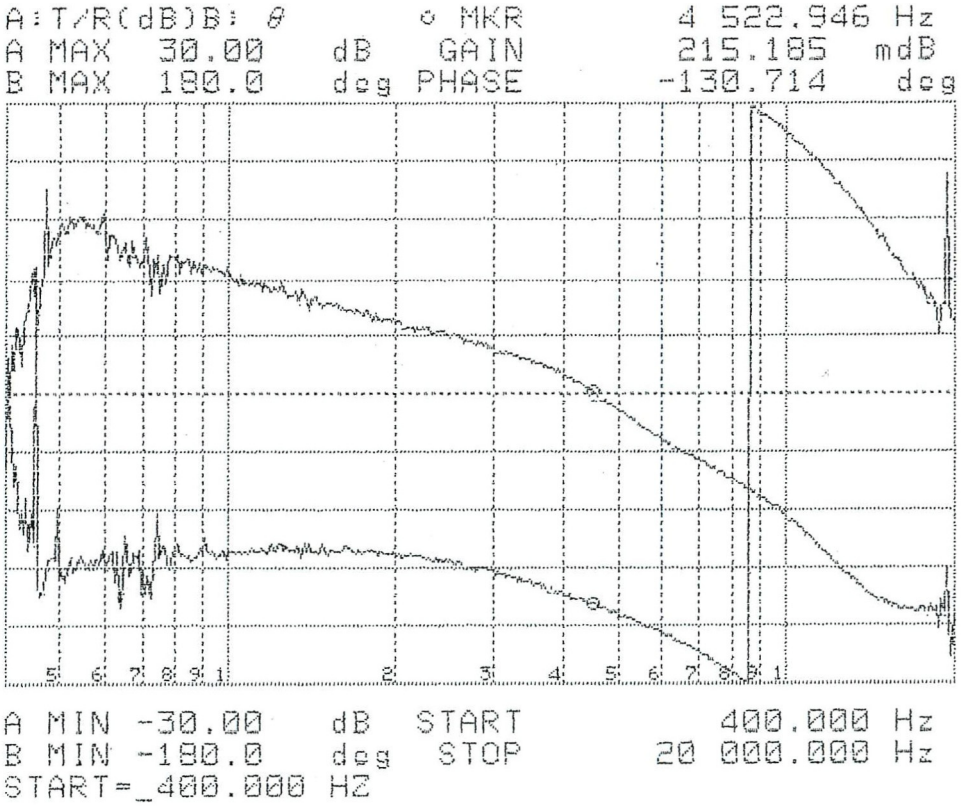

Figure 55 – Gain-Phase Plot, 230 VAC, Maximum Steady State Load.
Vertical Scale: Gain = 6 dB /div., Phase = 36 °/div.
Crossover Frequency = 4.52 kHz, Phase Margin = 49°.

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16 Conducted EMI

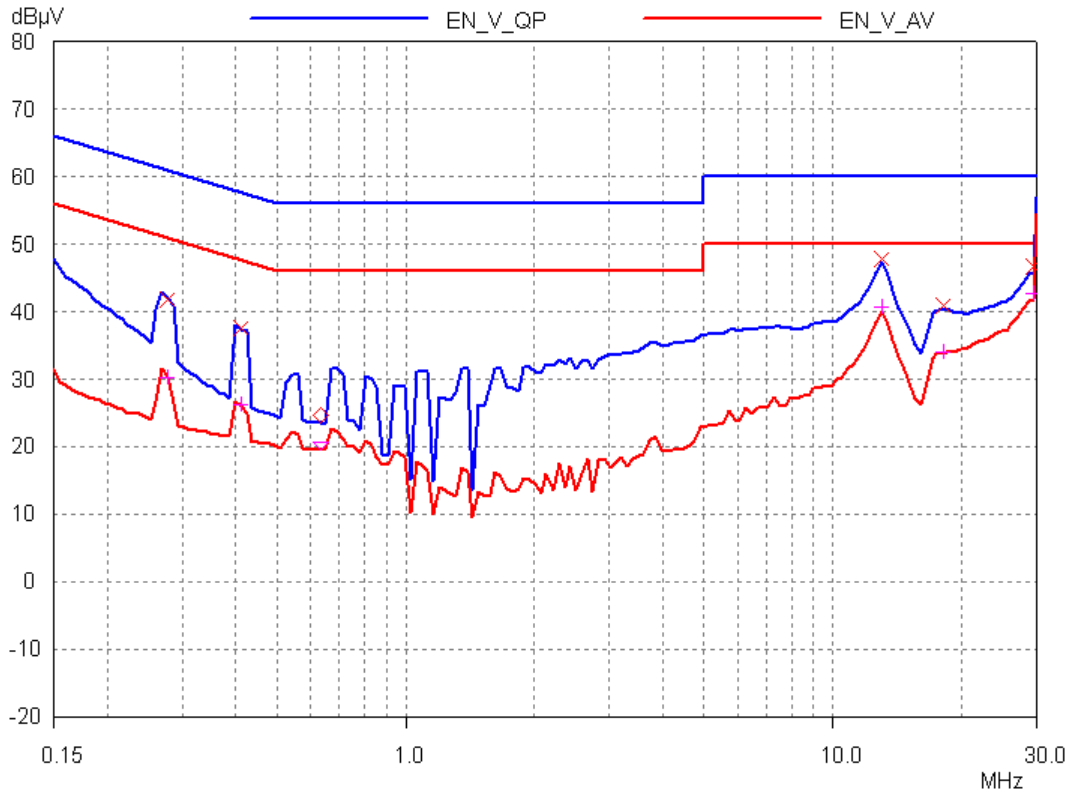

Figure 56 – Conducted EMI, Maximum Steady State Load, 115 VAC, 60 Hz, and EN55022 B Limits. Output Terminal Floating.

Frequency MHz	Quasi Pk dBµV	Limit dBµV	Delta dB	Phase /PE	Average dBµV	Limit dBµV	Delta dB	Phase /PE
0.27622	41.80	60.93	19.13	N /f1	30.16	50.93	20.77	N /f1
0.41079	37.52	57.63	20.11	N /f1	26.24	47.63	21.39	N /f1
12.93767	47.82	60.00	12.18	N /f1	40.72	50.00	9.28	N /f1
18.10096	40.99	60.00	19.01	N /f1	34.11	50.00	15.89	N /f1
29.50124	46.64	60.00	13.36	N /f1	42.69	50.00	7.31	N /f1

Table 5 – Conducted EMI, Maximum Steady State Load, 115 VAC, 60 Hz, and EN55022 B Limits. Output Terminal Floating.

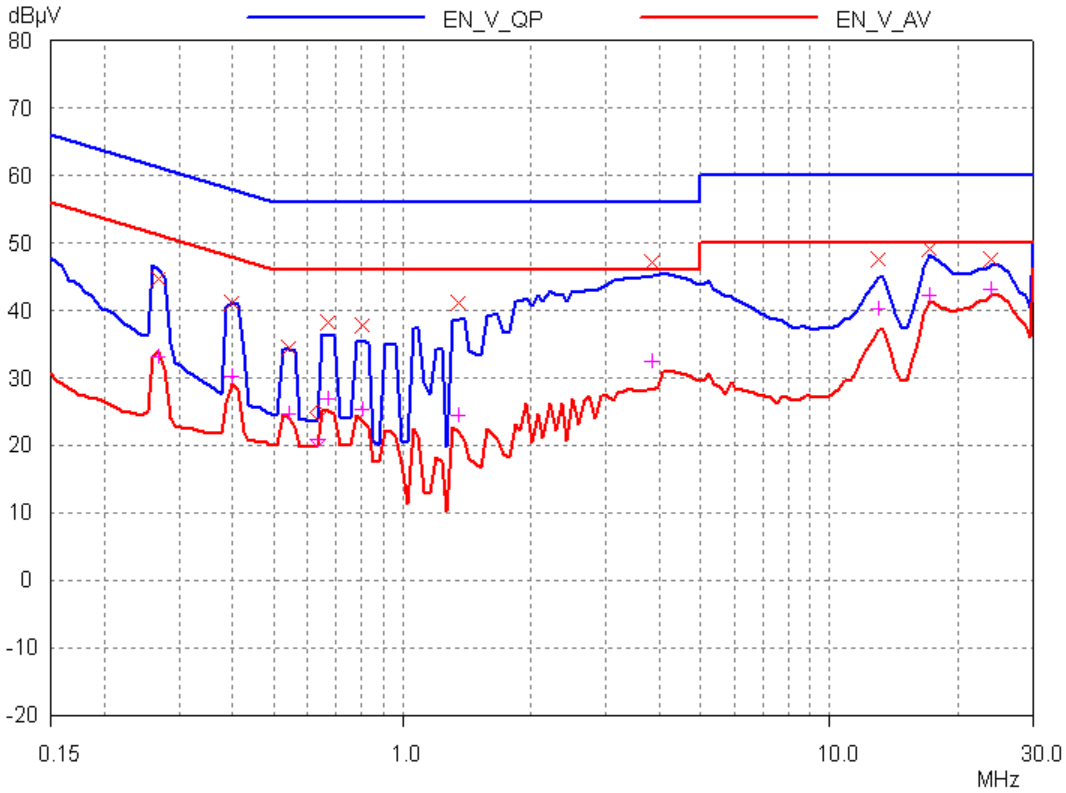

Figure 57 – Conducted EMI, Maximum Steady State Load, 115 VAC, 60 Hz, and EN55022 B Limits. Output Terminal PE Connected.

Frequency MHz	Quasi Pk dBµV	Limit dBµV	Delta dB	Phase /PE	Average dBµV	Limit dBµV	Delta dB	Phase /PE
0.26792	44.63	61.18	16.55	L1/gnd	33.10	51.18	18.08	N /gnd
0.39844	41.05	57.89	16.84	N /gnd	30.26	47.89	17.63	N /fl
0.54069	34.42	56.00	21.58	N /fl	24.74	46.00	21.26	N /gnd
0.66952	38.30	56.00	17.70	N /fl	26.98	46.00	19.02	N /gnd
0.80411	37.77	56.00	18.23	N /gnd	25.22	46.00	20.78	N /gnd
1.35118	41.20	56.00	14.80	N /fl	24.33	46.00	21.67	N /gnd
3.81513	47.21	56.00	8.79	N /fl	32.36	46.00	13.64	N /gnd
12.93767	47.64	60.00	12.36	L1/fl	40.20	50.00	9.80	N /gnd
17.02881	49.14	60.00	10.86	N /fl	42.35	50.00	7.65	N /gnd
23.82482	47.53	60.00	12.47	N /fl	43.15	50.00	6.85	N /fl

Table 6 – Conducted EMI, Maximum Steady State Load, 115 VAC, 60 Hz, and EN55022 B Limits. Output Terminal PE Connected.

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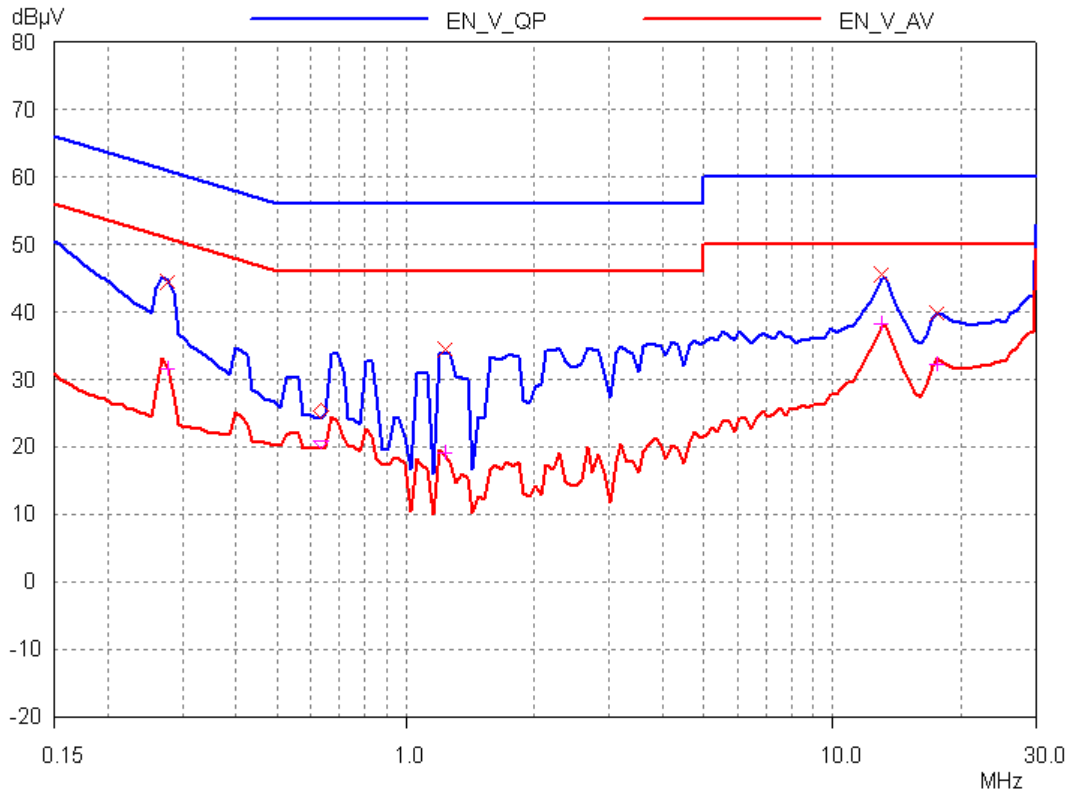

Figure 58 – Conducted EMI, Maximum Steady State Load, 230 VAC, 60 Hz, and EN55022 B Limits. Output Terminal Floating.

Frequency MHz	Quasi Pk dBµV	Limit dBµV	Delta dB	Phase /PE	Average dBµV	Limit dBµV	Delta dB	Phase /PE
0.27622	44.57	60.93	16.36	L1/fl	31.66	50.93	19.27	N /fl
1.23293	34.50	56.00	21.50	N /fl	19.14	46.00	26.86	N /fl
12.93767	45.50	60.00	14.50	N /fl	38.18	50.00	11.82	N /fl
17.5567	39.81	60.00	20.19	N /fl	32.30	50.00	17.70	N /fl

Table 7 – Conducted EMI, Maximum Steady State Load, 230 VAC, 60 Hz, and EN55022 B Limits. Output Terminal Floating.

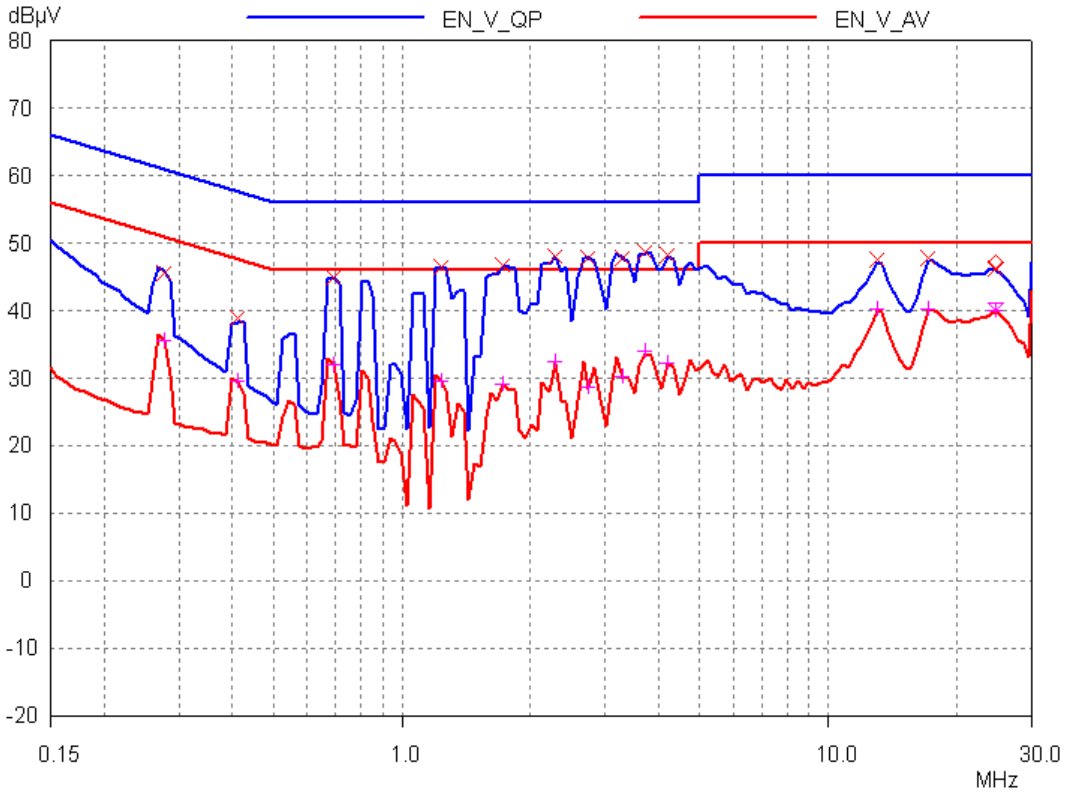

Figure 59 – Conducted EMI, Maximum Steady State Load, 230 VAC, 60 Hz, and EN55022 B Limits. Output Terminal PE Connected.

Frequency MHz	Quasi Pk dBµV	Limit dBµV	Delta dB	Phase /PE	Average dBµV	Limit dBµV	Delta dB	Phase /PE
0.27622	45.67	60.93	15.26	N /gnd	35.64	50.93	15.29	N /fl
0.41079	38.98	57.63	18.65	Ll/gnd	29.63	47.63	18.00	N /gnd
0.69027	44.98	56.00	11.02	N /gnd	32.03	46.00	13.97	N /gnd
1.23293	46.50	56.00	9.50	N /gnd	29.62	46.00	16.38	N /fl
1.72498	46.65	56.00	9.35	N /gnd	29.11	46.00	16.89	N /gnd
2.27045	48.02	56.00	7.98	N /gnd	32.34	46.00	13.66	N /gnd
2.72687	47.84	56.00	8.16	N /gnd	28.56	46.00	17.44	N /fl
3.27503	47.89	56.00	8.11	N /gnd	30.33	46.00	15.67	N /gnd
3.70042	48.73	56.00	7.27	N /gnd	33.97	46.00	12.03	N /gnd
4.18105	48.20	56.00	7.80	N /fl	32.28	46.00	13.72	N /gnd
12.93767	47.48	60.00	12.52	N /gnd	40.20	50.00	9.80	N /gnd
17.02881	47.72	60.00	12.28	N /fl	40.20	50.00	9.80	N /fl
24.56339	46.16	60.00	13.84	N /fl	39.92	50.00	10.08	N /fl

Table 8 – Conducted EMI, Maximum Steady State Load, 230 VAC, 60 Hz, and EN55022 B Limits. Output Terminal PE Connected.

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17 Revision History

Date	Author	Revision	Description & changes	Reviewed
19-Jan-10	ME	1.4	Initial Release	Apps & Mktg

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