

# A Novel High Step-Up DC–DC Converter for a Microgrid System

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**Abstract**—A novel high step-up dc–dc converter for a distributed generation system is proposed in this paper. The concept is composed of two capacitors, two diodes, and one coupled inductor. Two capacitors are charged in parallel, and are discharged in series by the coupled inductor. Thus, high step-up voltage gain can be achieved with an appropriate duty ratio. The voltage stresses on the main switch and output diode are reduced by a passive clamp circuit. Therefore, low resistance  $R_{DS(ON)}$  for the main switch can be adopted to reduce conduction loss. In addition, the reverse-recovery problem of the diode is alleviated, and thus, the efficiency can be further improved. The operating principle and steady-state analyses of the voltage gain are also discussed in detail. Finally, a 24-V input voltage, 400-V output voltage, and 400-W output power prototype circuit of the proposed converter are implemented in the laboratory to verify the performance.

**Index Terms**—Coupled inductor, distributed generation (DG) system, high step-up, microgrid.

## I. INTRODUCTION

THE distributed generation (DG) systems based on the renewable energy sources have rapidly developed in recent years [1], [2]. These DG systems are powered by microsources such as fuel cells, photovoltaic (PV) systems, and batteries [3]–[7]. Fig. 1 shows a PV distributed system in which the solar source is low dc input voltage. PV sources can also connect in series to obtain sufficient dc voltage for generating ac utility voltage; however, it is difficult to realize a series connection of the PV source without incurring a shadow effect [8], [9]. High step-up dc–dc converters are generally used as the front-end converters to step from low voltage (12–40 V) up to high voltage (380–400 V) [10]. High step-up dc–dc converters are required to have a large conversion ratio, high efficiency, and small volume [11]–[16].

The isolated converters such as forward, flyback, push-pull, half-bridge, and full-bridge types can adjust the turns ratio of the transformer to achieve high step-up voltage gain. However,

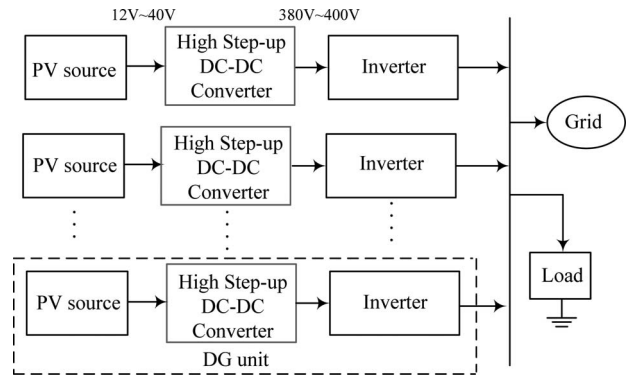


Fig. 1. PV distributed system.

the main switches of these converters will suffer a high voltage spike and high power dissipation from the leakage inductor of the transformer [17]. To reduce these drawbacks, the nondissipative snubber circuits and active-clamp circuits are employed. However, the cost increases accordingly due to the extra power switch and high side driver [18].

Theoretically, the nonisolated converters can be adopted to provide high step-up voltage gain with extremely high duty cycle [19]. However, the step-up voltage gain is limited by the effect of the power switches, rectifier diodes, and equivalent series resistance of the inductors and capacitors. The extreme duty cycle operation may also result in serious reverse-recovery problem and electromagnetic interference problem [20].

To improve the conversion efficiency and achieve high step-up voltage gain, many topologies have been proposed [19]–[28]. High step-up gain can be achieved by the use of the switched capacitor technique [22]–[25]. However, the main switch will suffer high transient current, and the conduction loss is high. Another method for achieving high step-up gain is the use of the voltage-lift technique [26]–[28]. However, it has the same drawback.

The converters employ the coupled-inductor technique to achieve high step-up gain by adjusting the turns ratio [29]. However, the leakage inductor of the coupled inductor incurs a voltage spike on the main switch and affects the conversion efficiency. For this reason, the converters using the coupled-inductor technique with an active clamp circuit have also been proposed [30], [31]. An integrated boost-flyback converter is presented, in which the secondary side of the coupled inductor is used as a flyback type [32], [33]. The leakage-inductor energy of the coupled inductor is recycled into the load during the switch-off period; thus, the voltage spike on the main switch can be limited. Additionally, the voltage stress of the main switch

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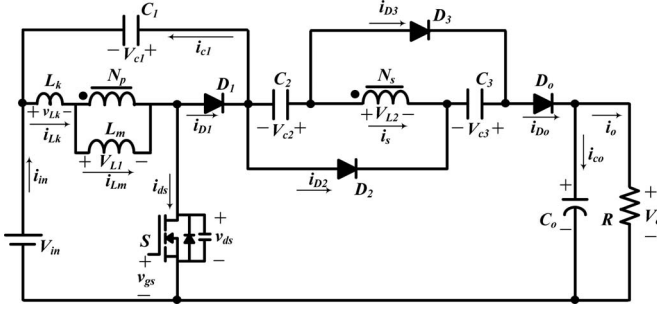


Fig. 2. Circuit configure of the proposed converter.

can be adjusted by the turns ratio of the coupled inductor. To achieve high step-up voltage gain, it has been proposed that the secondary side of the coupled inductor can be used as a flyback and a forward type [34]–[36]. Also, several converters that combine output-voltage stacking to increase voltage gain are proposed [37], [38]. The sepic–flyback converter with the coupled inductor and output stacking techniques has been proposed [39]. Additionally, a high step-up boost converter that uses multiple coupled inductors with output stacking has been proposed [40], [41].

This paper proposes a high efficiency, high step-up voltage gain, and clamp-mode converter. The proposed converter adds two pairs of additional capacitors and diodes to achieve high step-up voltage gain. The coupled inductor is used as both a forward and flyback type; thus, the two capacitors can be charged in parallel and discharged in series via the coupled inductor. The transit current does not flow through the main switch compared with earlier studies [22]–[28]. Thus, the proposed converter has low conduction loss. Additionally, this converter allows significant weight and volume reduction compared with other converters [29]–[40]. Another benefit is that the voltage stresses on the main switch and output diode are reduced. However, the leakage inductor of the coupled inductor may cause high power loss and voltage spike. Thus, a passive clamping circuit is needed to recycle the leakage-inductor energy of the coupled inductor and to clamp the voltage across the main switch. The reverse-recovery problems in the diodes are alleviated, and thus, high efficiency can be achieved.

## II. OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

Fig. 2 shows the circuit topology of the proposed converter. This converter consists of dc input voltage  $V_{in}$ , power switch  $S$ , coupled inductors  $N_p$  and  $N_s$ , one clamp diode  $D_1$ , clamp capacitor  $C_1$ , two blocking capacitors  $C_2$  and  $C_3$ , two blocking diodes  $D_2$  and  $D_3$ , output diode  $D_o$ , and output capacitor  $C_o$ . The coupled inductor is modeled as the magnetizing inductor  $L_m$  and leakage inductor  $L_k$ .

To simplify the circuit analysis, the following conditions are assumed.

- 1) Capacitors  $C_2$ ,  $C_3$ , and  $C_o$  are large enough that  $V_{c2}$ ,  $V_{c3}$ , and  $V_o$  are considered to be constant in one switching period.

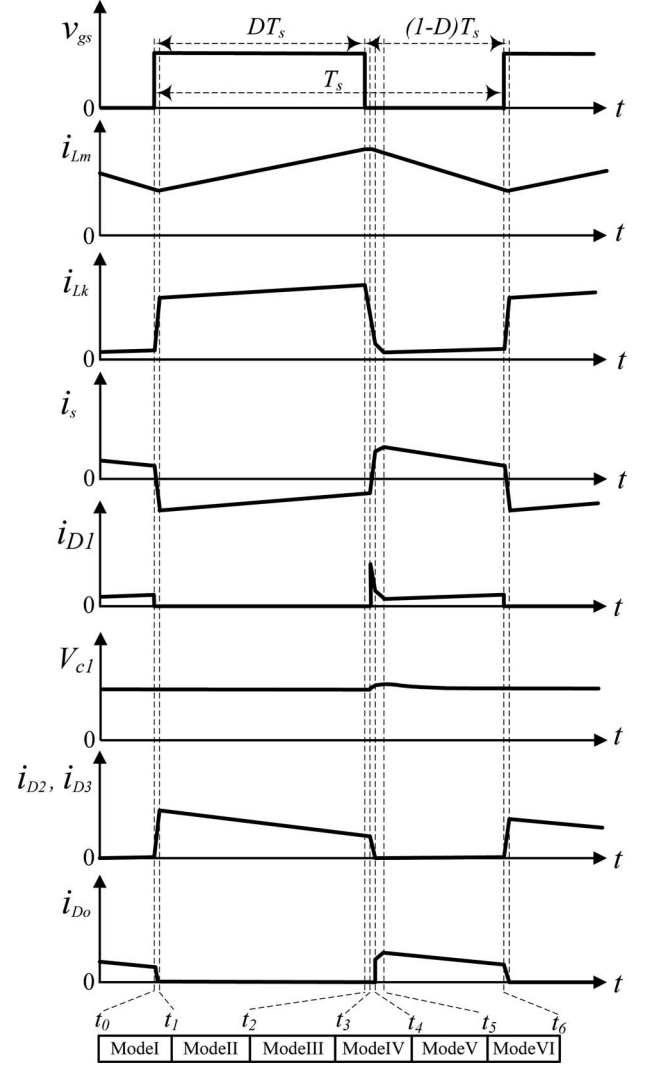


Fig. 3. Some typical key waveforms of the proposed converter at CCM operation.

- 2) The power MOSFET and diodes are treated as ideal, but the parasitic capacitor of the power switch is considered.
- 3) The coupling coefficient of coupled inductor  $k$  is equal to  $L_m/(L_m + L_k)$  and the turns ratio of coupled inductor  $n$  is equal to  $N_s/N_p$ .

### A. Continuous-Conduction Mode (CCM) Operation

In CCM operation, there are six operating modes in one switching period of the proposed converter. Fig. 3 shows the typical waveforms and Fig. 4 shows the current-flow path of the proposed converter for each modes. The operating modes are described as follows.

- 1) *Mode I* [ $t_0, t_1$ ]: During this time interval,  $S$  is turned on. Diodes  $D_1$ ,  $D_2$ , and  $D_3$  are turned off, and  $D_o$  is turned on. The current-flow path is shown in Fig. 4(a). The primary-side current of the coupled inductor  $i_{Lk}$  is increased linearly. The magnetizing inductor  $L_m$  stores its energy from dc source  $V_{in}$ . Due to the leakage inductor  $L_k$ , the secondary-side current of the coupled inductor  $i_s$

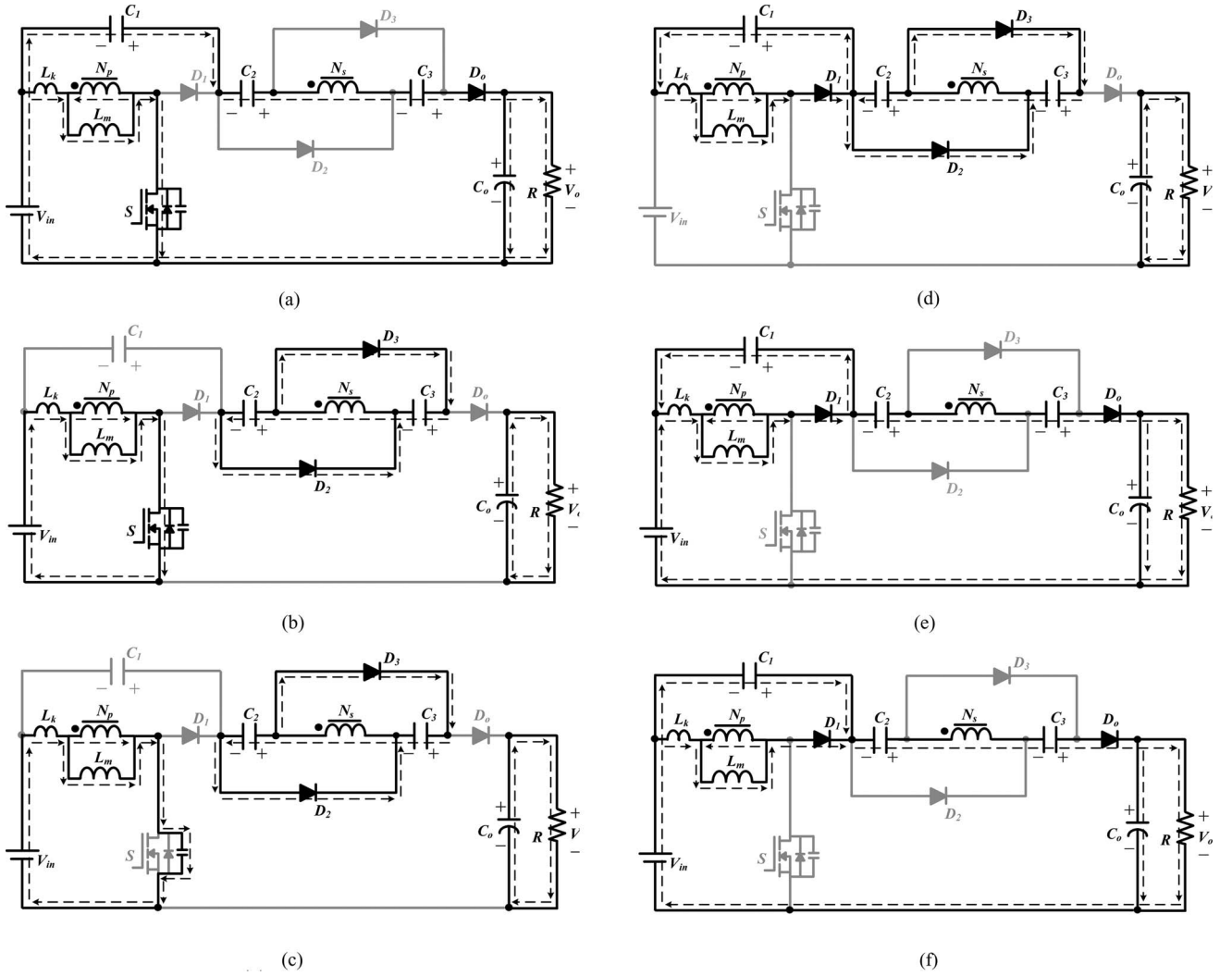


Fig. 4. Current flowing path of operating modes during one switching period at CCM operation. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V. (f) Mode VI.

is decreased linearly. The voltage across the secondary-side winding of the coupled inductor  $V_{L2}$ , and blocking voltages  $V_{c2}$  and  $V_{c3}$  are connected in series to charge the output capacitor  $C_o$  and to provide the energy to the load  $R$ . When the current  $i_s$  becomes zero, dc source  $V_{in}$  begins to charge capacitors  $C_2$  and  $C_3$  via the coupled inductor. When  $i_{Lk}$  is equal to  $i_{Lm}$  at  $t = t_1$ , this operating mode ends.

- 2) *Mode II* [ $t_1, t_2$ ]: During this time interval,  $S$  is still turned on. Diodes  $D_1$  and  $D_o$  are turned off, and  $D_2$  and  $D_3$  are turned on. The current-flow path is shown in Fig. 4(b). The magnetizing inductor  $L_m$  is stored energy from dc source  $V_{in}$ . Some of the energy from dc source  $V_{in}$  transfers to the secondary side of the coupled inductor to charge the capacitors  $C_2$  and  $C_3$ . Voltages  $V_{c2}$  and  $V_{c3}$  are approximately equal to  $nV_{in}$ . Output capacitor  $C_o$  provides the energy to load  $R$ . This operating mode ends when switch  $S$  is turned off at  $t = t_2$ .
- 3) *Mode III* [ $t_2, t_3$ ]: During this time interval,  $S$  is turned off. Diodes  $D_1$  and  $D_o$  are turned off, and  $D_2$  and  $D_3$  are

turned on. The current-flow path is shown in Fig. 4(c). The energies of leakage inductor  $L_k$  and magnetizing inductor  $L_m$  are released to the parasitic capacitor  $C_{ds}$  of switch  $S$ . The capacitors  $C_2$  and  $C_3$  are still charged by the dc source  $V_{in}$  via the coupled inductor. The output capacitor  $C_o$  provides energy to load  $R$ . When the capacitor voltage  $V_{in} + V_{ds}$  is equal to  $V_{c1}$  at  $t = t_3$ , diode  $D_1$  conducts and this operating mode ends.

- 4) *Mode IV* [ $t_3, t_4$ ]: During this time interval,  $S$  is turned off. Diodes  $D_1$ ,  $D_2$ , and  $D_3$  are turned on and  $D_o$  is turned off. The current-flow path is shown in Fig. 4(d). The energies of leakage inductor  $L_k$  and magnetizing inductor  $L_m$  are released to the clamp capacitor  $C_1$ . Some of the energy stored in  $L_m$  starts to release to capacitors  $C_2$  and  $C_3$  in parallel via the coupled inductor until secondary current  $i_s$  equals to zero. Meanwhile, current  $i_{Lk}$  is decreased quickly. Thus, diodes  $D_2$  and  $D_3$  are cut off at  $t = t_4$ , and this operating mode ends.
- 5) *Mode V* [ $t_4, t_5$ ]: During this time interval,  $S$  is turned off. Diodes  $D_1$  and  $D_o$  are turned on, and  $D_2$  and  $D_3$  are turned

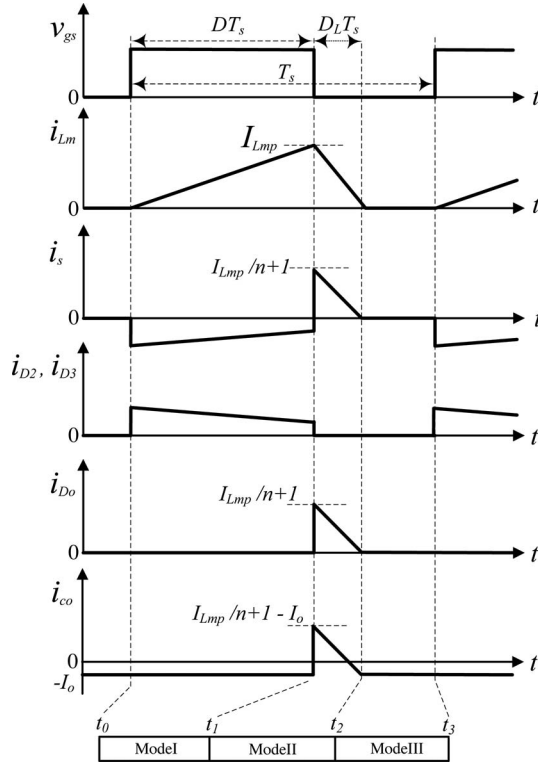


Fig. 5. Some typical key waveforms of the proposed converter at DCM operation.

off. The current-flow path is shown in Fig. 4(e). The energies of leakage inductor  $L_k$  and magnetizing inductor  $L_m$  are released to the clamp capacitor  $C_1$ . The primary and secondary windings of the coupled inductor, dc sources  $V_{in}$ , and capacitors  $C_2$  and  $C_3$  are in series to transfer their energies to the output capacitor  $C_o$  and load  $R$ . This operating mode ends when capacitor  $C_1$  starts to discharge at  $t = t_5$ .

- 6) *Mode VI*  $[t_5, t_6]$ : During this time interval,  $S$  is still turned off. Diodes  $D_1$  and  $D_o$  are turned on, and  $D_2$  and  $D_3$  are turned off. The current-flow path is shown in Fig. 4(f). The primary-side and secondary-side windings of the coupled inductor, dc sources  $V_{in}$ , and capacitors,  $C_1$ ,  $C_2$ , and  $C_3$ , transfer their energies to the output capacitor  $C_o$  and load  $R$ . This mode ends at  $t = t_6$  when  $S$  is turned on at the beginning of the next switching period.

### B. Discontinuous-Conduction Mode (DCM) Operation

In order to simplify the analysis for DCM operation, leakage inductor  $L_k$  of the coupled inductor is neglected. Fig. 5 shows the typical waveforms when the proposed converter is operated in DCM, and Fig. 6 shows the current-flow path of the proposed converter for each mode. There are three modes in DCM operation. The operating modes are described as follows.

- 1) *Mode I*  $[t_0, t_1]$ : During this time interval,  $S$  is turned on. The current-flow path is shown in Fig. 6(a). The part energy of dc source  $V_{in}$  transfers to magnetizing inductor  $L_m$ . Thus,  $i_{Lm}$  is increased linearly. The dc source  $V_{in}$

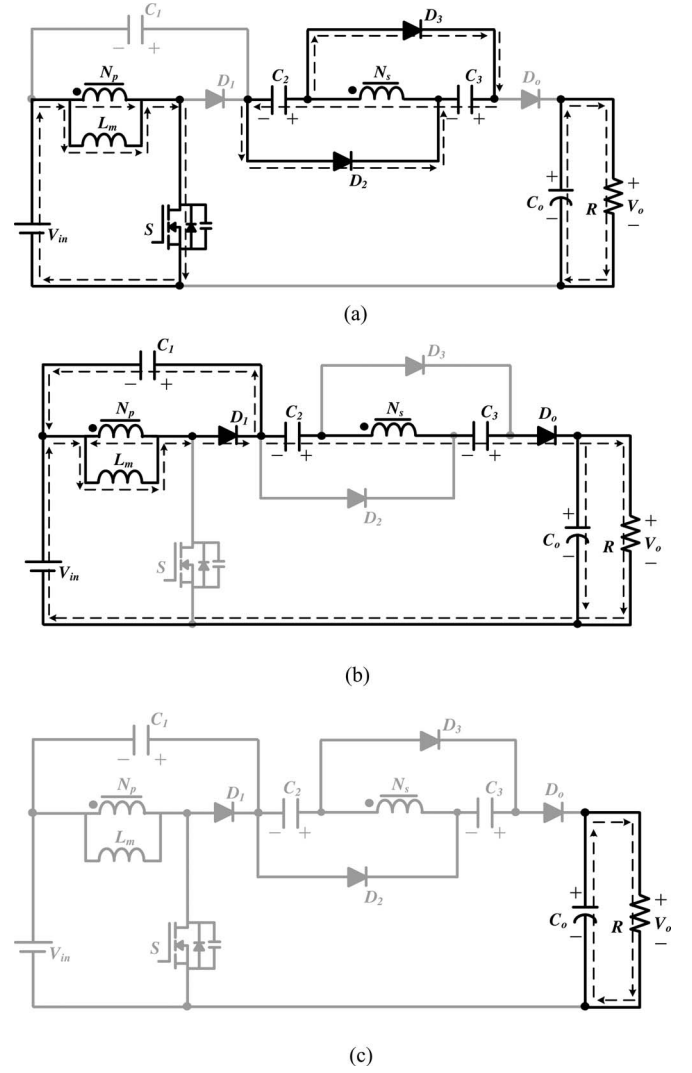


Fig. 6. Current flowing path of operating modes during one switching period at DCM operation. (a) Mode I. (b) Mode II. (c) Mode III.

also transfers another part energy to charge capacitors  $C_2$  and  $C_3$  via the coupled inductor. The energy of the output capacitor  $C_o$  is discharged to load  $R$ . This mode ends when  $S$  is turned off at  $t = t_1$ .

- 2) *Mode II*  $[t_1, t_2]$ : During this time interval,  $S$  is turned off. The current-flow path is shown in Fig. 6(b). The energy of the magnetizing inductor  $L_m$  is released to the capacitor  $C_1$ . Similarly, capacitors  $C_2$  and  $C_3$  are discharged in a series with dc source  $V_{in}$  and magnetizing inductor  $L_m$  to the capacitor  $C_o$  and load  $R$ . This mode ends when the energy stored in  $L_m$  is depleted at  $t = t_2$ .
- 3) *Mode III*  $[t_2, t_3]$ : During this time interval,  $S$  remains turned off. The current-flow path is shown in Fig. 6(c). Since the energy stored in  $L_m$  is depleted, the energy stored in  $C_o$  is discharged to load  $R$ . This mode ends when  $S$  is turned on at  $t = t_3$ .



### III. STEADY-STATE ANALYSIS OF THE PROPOSED CONVERTER

#### A. CCM Operation

At modes IV and V, the energy of the leakage inductor  $L_k$  is released to the clamped capacitor  $C_1$ . According to previous work [15], the duty cycle of the released energy can be expressed as

$$D_{c1} = \frac{t_{c1}}{T_s} = \frac{2(1-D)}{n+1} \quad (1)$$

where  $T_s$  is the switching period,  $D_{c1}$  is the duty ratio of the switch, and  $t_{c1}$  is the time of modes IV and V.

By applying the voltage-second balance principle on  $L_m$ , the voltage across the capacitor  $C_1$  can be represented by

$$V_{c1} = \frac{D}{1-D} \cdot V_{in} \cdot \frac{(1+k) + (1-k)n}{2}. \quad (2)$$

Since the time durations of modes I, III, and IV are significantly short, only modes II, V, and VI are considered in CCM operation for the steady-state analysis.

In the time period of mode II, the following equations can be written based on Fig. 4(b):

$$v_{L1}^{II} = \frac{L_m}{L_m + L_{k1}} V_{in} = k V_{in} \quad (3)$$

$$v_{L2}^{II} = n v_{L1}^{II} = n k V_{in}. \quad (4)$$

Thus, the voltage across capacitors  $C_2$  and  $C_3$  can be written as

$$V_{c2} = V_{c3} = v_{L2}^{II} = n k V_{in}. \quad (5)$$

During the time duration of modes V and VI, the following equation can be formulated based on Fig. 4(f):

$$v_{L2}^V = v_{L2}^{VI} = V_{in} + V_{c1} + V_{c2} + V_{c3} - V_o. \quad (6)$$

Thus, the voltage across the magnetizing inductor  $L_m$  can be derived as

$$v_{L1}^V = v_{L1}^{VI} = \frac{v_{L2}^{VI}}{n} = \frac{V_{in} + V_{c1} + V_{c2} + V_{c3} - V_o}{n}. \quad (7)$$

Using the volt-second balance principle on  $L_m$ , the following equation is given:

$$\int_0^{DT_s} v_{L1}^{II} dt + \int_{DT_s}^{T_s} v_{L1}^{VI} dt = 0. \quad (8)$$

Substituting (2), (3), (5), and (7) into (8), the voltage gain is obtained as

$$M_{CCM} = \frac{1+nk}{1-D} + nk + \frac{D}{1-D} \cdot \frac{(1-k)(n-1)}{2}. \quad (9)$$

The schematic of the voltage gain versus the duty ratio under various coupling coefficients of the coupled inductor is shown in Fig. 7. It is seen that the voltage gain is not very sensitive to the coupling coefficient. When  $k$  is equal to 1, the ideal voltage gain is written as

$$M_{CCM} = \frac{1+n}{1-D} + n. \quad (10)$$

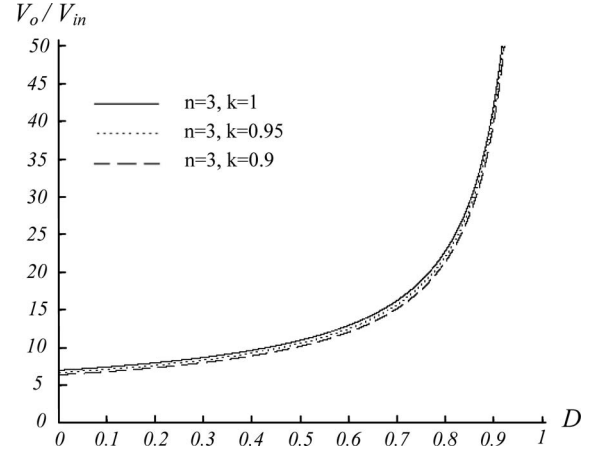


Fig. 7. Voltage gain versus duty ratio at CCM operation under  $n = 3$  and various  $k$ .

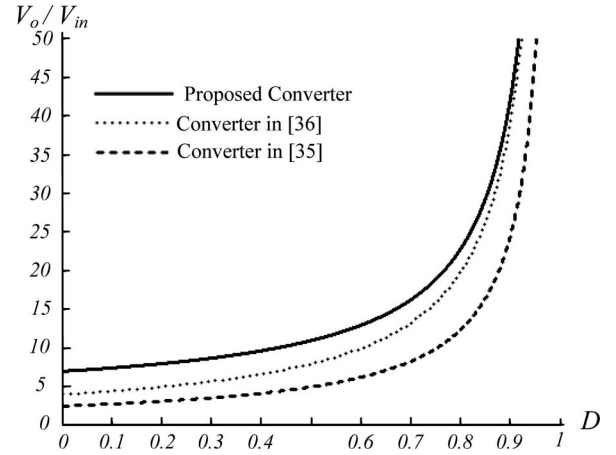


Fig. 8. Voltage gain versus duty ratio of the proposed converter, the converters in [35] and [36] at CCM operation under  $n = 3$  and  $k = 1$ .

Fig. 8 shows the voltage gain versus the duty ratio of the proposed converter as compared with the converters in previous work [35] and [36] at CCM operation under  $k = 1$  and  $n = 3$ . One can see that the voltage gain of the proposed converter is higher than those of the converters in [35] and [36].

According to the description of the operating modes, the voltage stresses on the active switch  $S$  and diodes  $D_1$ ,  $D_2$ ,  $D_3$ , and  $D_o$  are given as

$$V_{DS} = \frac{1}{1-D} V_{in} = \frac{V_o - nV_{in}}{n+1} \quad (11)$$

$$V_{D1} = \frac{1}{1-D} V_{in} = \frac{V_o - nV_{in}}{n+1} \quad (12)$$

$$V_{D2} = V_{D3} = V_{D_o} = \frac{n}{1-D} V_{in} = \frac{n}{n+1} (V_o - nV_{in}). \quad (13)$$

Equations (11)–(13) mean that with the same specifications, the voltage stresses on the main switch and diodes can be adjusted by the turns ratio of the coupled inductor.

### B. DCM Operation

In DCM operation, three modes are discussed. The key waveform is shown in Fig. 5. During the time of mode I, the switch  $S$  is turned on. Thus, the following equations can be formulated based on Fig. 6(a):

$$v_{L1}^I = V_{in} \quad (14)$$

$$v_{L2}^I = nV_{in}. \quad (15)$$

The peak value of the magnetizing inductor current is given as

$$I_{Lmp} = \frac{V_{in}}{L_m} DT_s. \quad (16)$$

Furthermore, the voltage across capacitors  $C_2$  and  $C_3$  can be written as

$$V_{c2} = V_{c3} = v_{L2}^I = nV_{in}. \quad (17)$$

In the time interval of mode II, the following equations can be expressed based on Fig. 6(b):

$$v_{L1}^{II} = -V_{c1}, \quad (18)$$

$$v_{L2}^{II} = V_{in} + V_{c1} + V_{c2} + V_{c3} - V_o. \quad (19)$$

During the time of mode III, the following equation can be derived from Fig. 6(c):

$$v_{L1}^{III} = v_{L2}^{III} = 0. \quad (20)$$

Applying the voltage-second balance principle on  $N_p$ ,  $N_s$  of the coupled inductor, the following equations are given as

$$\int_0^{DT_s} v_{L1}^I dt + \int_{DT_s}^{(D+D_L)T_s} v_{L1}^{II} dt + \int_{(D+D_L)T_s}^{T_s} v_{L1}^{III} dt = 0 \quad (21)$$

$$\int_0^{DT_s} v_{L2}^I dt + \int_{DT_s}^{(D+D_L)T_s} v_{L2}^{II} dt + \int_{(D+D_L)T_s}^{T_s} v_{L2}^{III} dt = 0. \quad (22)$$

Substituting (14), (15), (17), (18), (19), and (20) into (21) and (22), the voltage gain is obtained as follows:

$$V_{c1} = \frac{D}{D_L} V_{in} \quad (23)$$

$$V_o = \left[ \frac{D}{D_L} (n+1) + (2n+1) \right] V_{in}. \quad (24)$$

According to (24), the duty cycle  $D_L$  can be derived as

$$D_L = \frac{(1+n)DV_{in}}{V_o - (1+2n)V_{in}}. \quad (25)$$

From Fig. 5, the average current of  $i_{co}$  is computed as

$$I_{co} = \frac{1}{2} D_L \frac{I_{Lmp}}{n+1} - I_o. \quad (26)$$

Since  $I_{co}$  is equal to zero under steady state, (16), (25), and  $I_{co} = 0$  into (26) yield

$$\frac{D^2 V_{in}^2 T_s}{2 [V_o - (1+2n)V_{in}] L_m} = \frac{V_o}{R}. \quad (27)$$

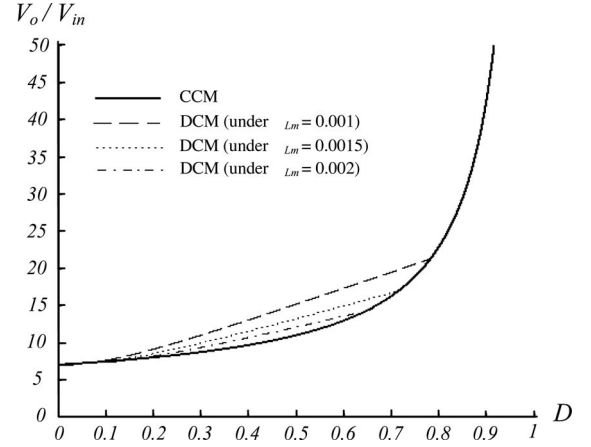


Fig. 9. Voltage gain versus duty ratio at DCM operation under various  $\tau_{Lm}$  and at CCM operation under  $n = 3$  and  $k = 1$ .

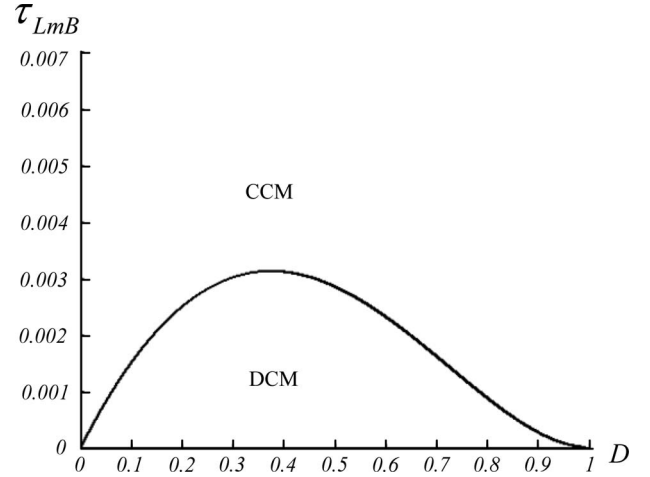


Fig. 10. Boundary condition of the proposed converter under  $n = 3$ .

Then, the normalized magnetizing-inductor time constant is defined as

$$\tau_{Lm} \equiv \frac{L_m}{RT_s} = \frac{L_m f_s}{R} \quad (28)$$

where  $f_s$  is the switching frequency.

Substituting (28) into (27), the voltage gain is given by

$$M_{DCM} = \frac{V_o}{V_{in}} = \frac{1+2n}{2} + \sqrt{\frac{(1+2n)^2}{4} + \frac{D^2}{2\tau_{Lm}}}. \quad (29)$$

The curve of the voltage gain, shown in Fig. 9, illustrates the voltage gain versus the duty ratio under various  $\tau_{Lm}$ .

### C. Boundary Operating Condition Between CCM and DCM

If the proposed converter is operated in boundary-condition mode, the voltage gain of CCM operation is equal to the voltage gain of DCM operation. From (10) and (29), the boundary normalized magnetizing-inductor time constant  $\tau_{LmB}$  can be derived as

$$\tau_{LmB} = \frac{D(1-D)^2}{2(1+n)(1+2n-nD)}. \quad (30)$$

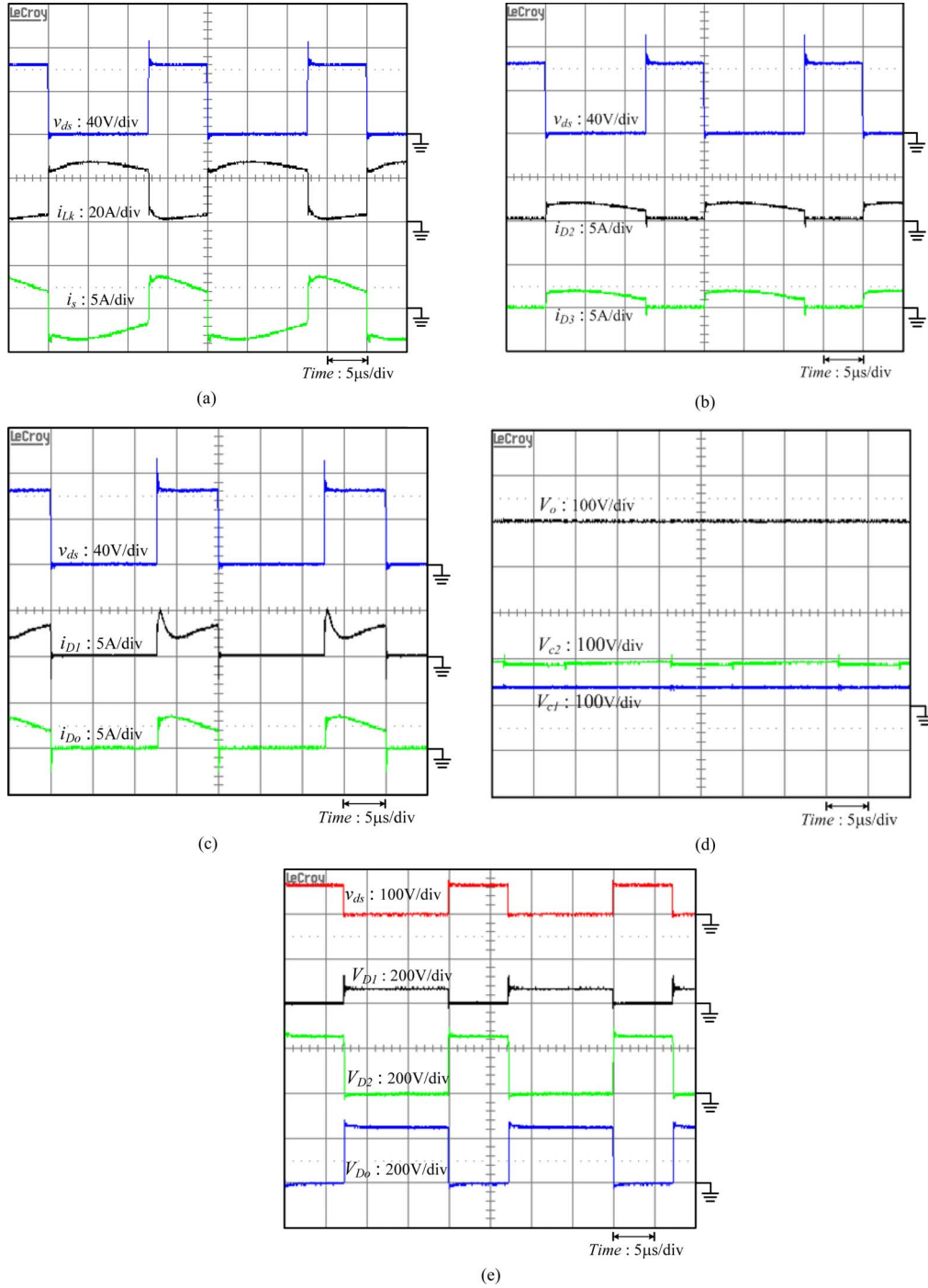


Fig. 11. Experiment results under full-load  $P_o = 400$  W.

The curve of  $\tau_{LmB}$  is plotted in Fig. 10. If  $\tau_{Lm}$  is larger than  $\tau_{LmB}$ , the proposed converter is operated in CCM.

#### IV. DESIGN AND EXPERIMENT OF THE PROPOSED CONVERTER

To verify the performance of the proposed converter, a prototype circuit is implemented in the laboratory. The specifications are as follows:

- 1) input dc voltage  $V_{in}$ : 24 V;
- 2) output dc voltage  $V_o$ : 400 V;

- 3) maximum output power: 400 W;
- 4) switching frequency: 50 kHz;
- 5) MOSFET  $S$ : IRFB4410ZPBF;
- 6) diodes  $D_1$ : SBR20A100CTFP,  $D_2/D_3$ : DESI30, and  $D_0$ : BYR29;
- 7) coupled inductor: ETD-59, core pc40,  $N_p:N_s = 1:4$   $L_m = 48 \mu\text{H}$ ;  $L_k = 0.25 \mu\text{H}$ ;
- 8) capacitors  $C_1$ :  $56 \mu\text{F}/100$  V,  $C_2/C_3$ :  $4.7 \mu\text{F}/200$  V, and  $C_o$ :  $180 \mu\text{F}/450$  V.

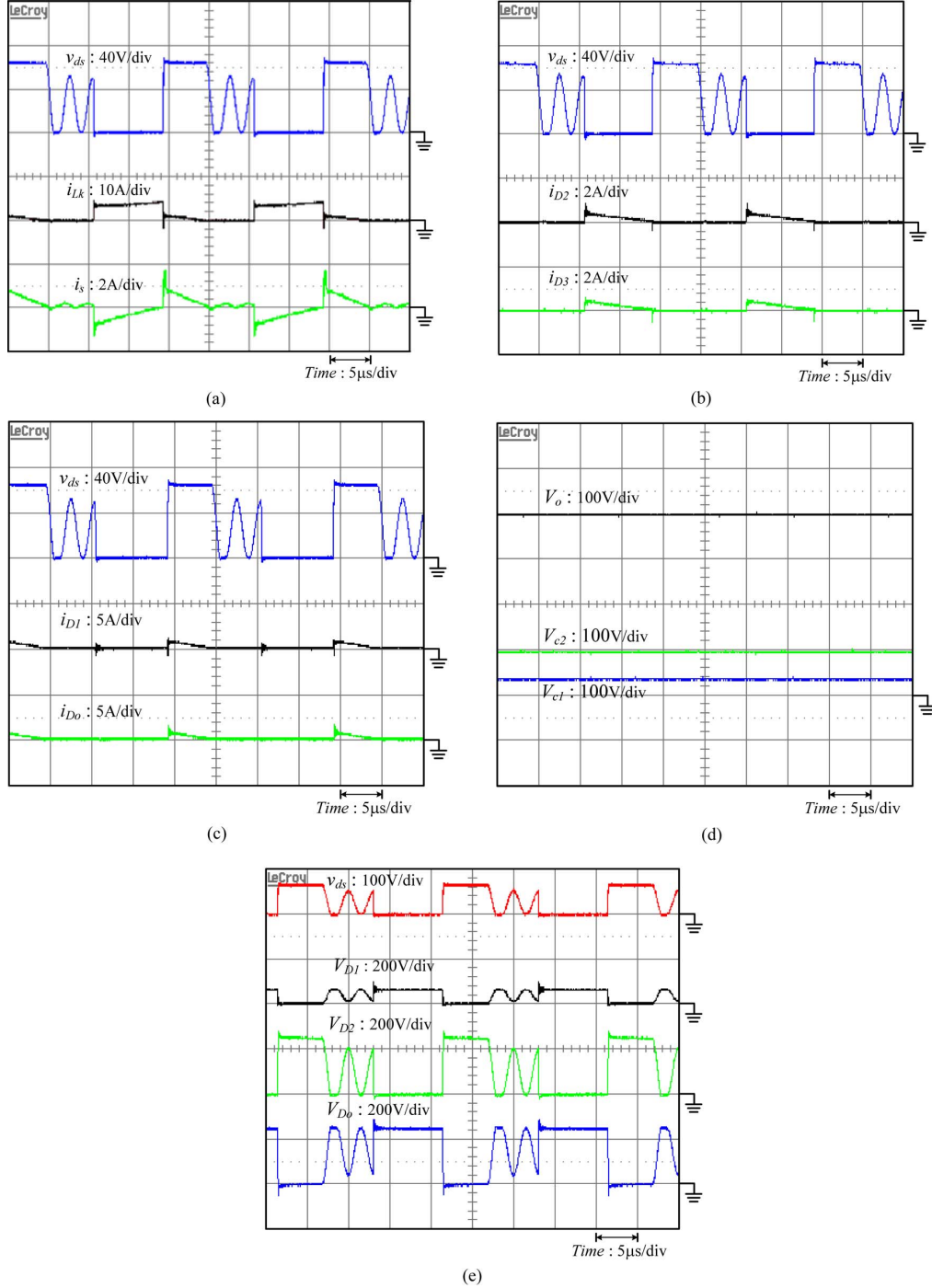


Fig. 12. Experiment results under light-load  $P_o = 40$  W.

Fig. 11 shows the measured waveforms for full-load  $P_o = 400$  W and  $V_{in} = 24$  V. The proposed converter is operated in CCM under full-load condition. The waveforms demonstrate that the steady-state analysis is correct. In the measured waveforms,  $v_{ds}$  is clamped at appropriately 90 V during the switch-off period. Therefore, a low-voltage-rated switch is adopted to achieve high efficiency for the proposed converter.

The waveform of the secondary-side current of the coupled inductor  $i_s$  in Fig. 11(a) shows that the proposed converter is operated in CCM because the current is not equal to zero when

the switch is turned on. In Fig. 11(b), the waveforms of  $i_{D2}$  and  $i_{D3}$  show that capacitors  $C_2$  and  $C_3$  are charged in parallel. Fig. 11(c) shows that the energy of leakage inductor  $L_k$  is released to capacitor  $C_1$  from  $i_{D1}$ . Fig. 11(d) reveals that  $V_{c1}$  and  $V_{c2}$  are able to satisfy (2) and (5). In addition, output voltage  $V_o$  is consistent with (10). Fig. 11(e) shows the voltage stresses of the main switch and diodes, and demonstrates the consistency of (11), (12), and (13). Fig. 12 shows the light-load waveforms. The output voltage is about 400 V and the analysis of the DCM of the proposed converter is demonstrated.



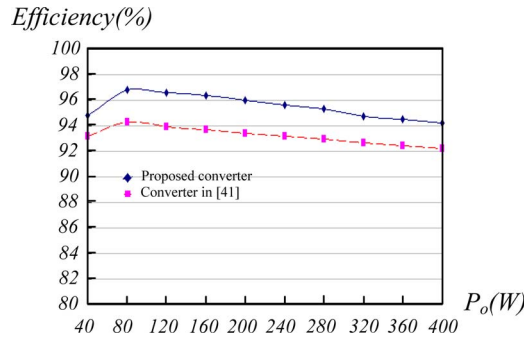


Fig. 13. Experimental conversion efficiency.

Fig. 13 shows the experimental conversion efficiency of the proposed converter, in which the maximum efficiency is around 96.8% at  $P_o = 80$  W and the full-load efficiency is appropriately 94.2% at  $P_o = 400$  W. The efficiency of converter in [41] is also showed. The maximum efficiency is 94.3% and the full-load efficiency is 92.25%. The results show that the proposed converter has promoted the efficiency about 2%.

The results verify the high efficiency of the proposed converter. Because the low input voltage is applied in this converter, the proposed converter should experience extremely high input current at full load, which would lead to high conduction loss during the switch turn-on period. To further improving the conduction loss, two of the proposed converter can be used in interleaved operation where the input current is shared by two switches to achieve high efficiency.

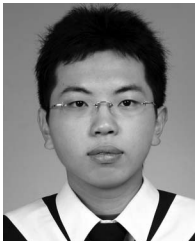
## V. CONCLUSION

This paper proposed a novel, high efficiency, and high step-up dc–dc converter. By using the capacitor charged in parallel and discharged in a series by the coupled inductor, high step-up voltage gain and high efficiency are achieved. The steady-state analyses of voltage gain and boundary operating condition are discussed in detail. A prototype circuit of the proposed converter is built in the laboratory. Experimental results confirm that high efficiency and high step-up voltage gain can be achieved. The efficiency is 96.8%. The voltage stress on the main switches is 90 V; thus, low voltage ratings and low on-state resistance levels  $R_{DS(ON)}$  switch can be selected. Moreover, the proposed converter has simple structure. It is suitable for renewable energy systems in microgrid applications.

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