AN-9765

LED Backlight Driving Boost Switch

Introduction

FAN7340 is a single-channel boost controller that integrates an N-channel dimming MOSFET using Fairchild's proprietary planar DMOS technology. The IC operates as a constant-current source for driving high-current LEDs. FAN7340 uses a current-mode control with programmable slope compensation to prevent sub-harmonic oscillation and provides protections such as Open-LED Protection (OLP) and Over-Voltage Protection (OVP) for system reliability. The IC internally generates a FAULT_OUT signal with a delay in case of abnormal LED string conditions. A dimming function is implemented with a PWM or analog method. An internal soft-start function prohibits inrush current flowing into the output capacitor during startup. The circuit operation and design procedure are explained in the following sections.

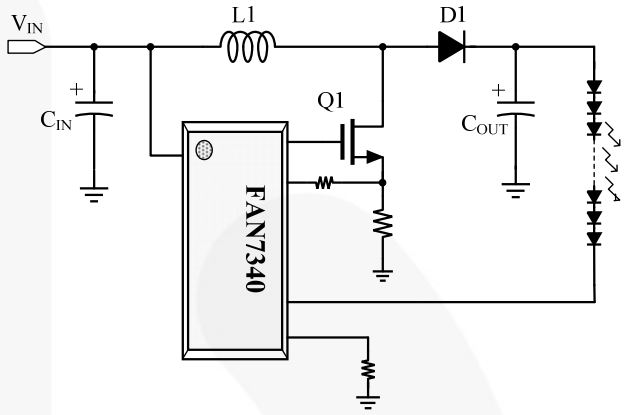

Figure 1. Boost Converter Using FAN7340

Description

A boost converter circuit using FAN7340 is shown in Figure 1. There are a couple of merits with a boost topology as LED backlight drivers as compared with a buck topology. Even though a buck is configured as a low-side driven one, there is no way to detect the LED current directly. A method to sense the high-side current should be used at least. Meanwhile, in a boost topology; not only the gate driver for the switching device, but also the LED string is connected to the secondary ground of the pre-regulator, such as an LLC converter. Therefore, the LED current can be detected precisely using a sensing resistor.

An LLC is generally used to provide an appropriate output voltage to the boost stage from a Power Factor Corrector (PFC) circuit due to its high efficiency. The secondary side of the LLC is composed of only an output capacitor so that the output current is filtered with no inductor. Therefore, a boost topology is more suitable as a post-regulator because the output capacitor ripple current stress of the LLC is reduced with an input inductor of the boost stage.

In addition, the low input voltage of the boost stage allows selecting low voltage-rated rectifiers in the LLC secondary side, compared to the buck topology. This helps lower total Bill of Materials (BOM) cost.

Design Guidance

Boost converters can be designed and operated in three modes; Discontinuous Conduction Mode (DCM), Continuous Conduction Mode (CCM), and Boundary Conduction Mode (BCM). In a feedback network, DCM operation is better than the CCM operation because a Right-Half Plane (RHP) zero disappears in the DCM operation. There is no reverse-recovery problem of the boost diode in the DCM operation due to the soft turn-off of the diode. However, the switch peak current in the DCM operation is higher than in the CCM operation, so that the root mean square (rms) current of the switch is also higher, resulting in the increase of the conduction loss.

BCM operation takes advantage of the DCM with reduced conduction loss. The RHP zero disappears and the reverse-recovery problem doesn't need to be considered as in the DCM operation. At the same time, the rms current of the switch can be reduced more than in DCM operation even if the conduction loss is still larger than in CCM operation. When the switching device turns on, the boost inductor current builds up. After the turn-off of the switching device, the energy stored in the boost inductor is fully discharged at the beginning of the next switching cycle. The switch peak current lowers due to the full usage of the total switching period, compared to DCM operation.

As an example, a boost converter using the FAN7340 is designed with the conditions of V_{IN}=120V, V_{OUT}=230V, I_{OUT}=300mA, f_S=100kHz, operating in BCM under full-load condition and in DCM under light-load conditions.

BCM Boost Converter Design Procedure

Calculating Inductance

When the boost converter operates in BCM, the voltage conversion ratio is obtained for CCM as:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D_1} \quad (1)$$

where V_{IN} is the input voltage; V_{OUT} is the output voltage; and D_1 is the duty ratio of the main switch. The inductor peak current (same as the switch peak current) can be calculated as:

$$I_{L\_peak} = \frac{V_{IN}}{L_{IN}} \times D_1 T_s \quad (2)$$

where L_{in} is the boost inductance and T_s is the switching period.

Since the average value of the boost diode current over one switching period is equivalent to the LED current, the critical value of the boost inductance at BCM can be obtained as:

$$L_{critical} = \frac{T_s V_{OUT}}{2 I_{OUT}} \times D_1 (1-D_1)^2 \quad (3)$$

where I_{OUT} is the nominal output LED current.

Table 1. Specifications for an Example

LED Module (1-String LED: 72EA)			
V_{IN}	V_{CC} of IC	V_{OUT}	I_{OUT} (1Ch)
$120V_{DC}$ ±10%	15V ±10%	230V	300mA

(Example) The duty cycle of the boost converter in BCM for the specifications in Table 1 is obtained from Equation (1). To guarantee BCM operation even with the minimum input voltage condition, calculate the maximum duty ratio**:**

$$D_{\max} = \frac{V_{out} - V_{in,\min}}{V_{out}} = \frac{230 - 120 \times 0.9}{230} = 0.53$$

If the operating frequency is 100kHz, the critical value of the boost inductor in BCM is:

$$L_{critical} = \frac{10 \times 10^{-6} \times 230}{2 \times 0.3} \times 0.53 \times (0.47)^2 = 4.49 \times 10^{-4} [H]$$

Therefore, the inductance for BCM operation is selected as 450µH. The inductor peak current is also obtained with $L_{critical}$ as:

$$I_{L\_peak} = \frac{120 \times 0.9}{450 \times 10^{-6}} \times 0.53 \times 10 \times 10^{-6} = 1.27 \quad [A] \cdot$$

Selection of the Power MOSFET

The power MOSFET for the main switch should be selected taking into account the voltage and current stresses on the switch. The voltage stress on the switch in the boost topology is the same as the output voltage, V_{OUT}. When selecting the power MOSFET, the derating should be considered so that 20% is generally added as a margin.

The rms current of the switch is obtained as:

$$I_{MOS,rms} = \sqrt{\frac{D_1}{3}} I_{L\_peak} \quad (4)$$

The conduction loss of the power MOSFET can be calculated with the rms current and its $R_{DS(ON)}$. Select an appropriate power MOSFET as long as the conduction loss is acceptable.

(Example) The voltage stress on the switch is the same as the output voltage, 230V, and considering 20% derating, the BV_{DSS} of the power MOSFET should be greater than 276V. The rms current of the switch is:

$$I_{MOS,rms} = \sqrt{\frac{0.53}{3}} \times 1.27 = 0.53 \quad [A] \cdot$$

If the expected conduction loss must be less than 0.5W, the $R_{DS(ON)}$ of the power MOSFET should be selected for less than 1.18Ω.

$$R_{DS(ON)} = \frac{P_{cond\_loss}}{I_{MOS,rms}^2} = \frac{0.5}{0.65^2} = 1.18 \quad [\Omega]$$

Selecting the Power Diode

The power diode for the boost diode should be selected taking the voltage and current stresses on the diode into account as well. There is no need to consider the reverse recovery problem due to the BCM and/or DCM operation.

The voltage stress on the diode in the boost topology is the same as the output voltage. The 20% derating must be considered when selecting the power diode also.

The average current of the boost diode at DCM operation is obtained as Equation (5):

$$I_{D\_avg} = \frac{V_{IN} \cdot D_1 \cdot D_2}{2 L_{critical} \cdot f_s} \quad (5)$$

where D_2 is the duty ratio of the power diode and f_s is the switching frequency. Equation (5) equals to the nominal output LED current, I_{OUT}.

(Example) The voltage stress on the boost diode is 230V and, considering 20% derating, the required voltage rating of the power diode is more than 276V. The average current of the boost diode is the same as the nominal output LED current, so $I_{D\_avg}=I_{OUT}=0.3A$.

Selecting the Output Capacitance

The value of the output capacitor can be selected based on the output voltage ripple requirements. Without consideration of the effect of Effective Series Resistance (ESR) of the electrolytic capacitors as output capacitors, the output voltage ripple in a peak-to-peak manner is obtained as Equation (6):

$$V_{ripple,pp} = \frac{\left(2D_1 + \frac{I_{OUT} \cdot D_2 \cdot L_{critical}}{V_{IN} \cdot D_1 T_s}\right) \cdot I_{OUT} \cdot T_s}{2C_{OUT}} \quad (6)$$

Therefore, the output capacitance can be selected with the given output voltage ripple specification according to Equation (7):

$$C_{OUT} \geq \frac{\left(2D_1 + \frac{I_{OUT} \cdot D_2 \cdot L_{critical}}{V_{IN} \cdot D_1 T_s}\right) \cdot I_{OUT} \cdot T_s}{2V_{ripple,pp}} \quad (7)$$

In BCM operation, D_2 is equal to 1-D_1.

On the other hand, it needs to check the required ESR, depending on the output voltage ripple specification, as calculated in Equation (8).

$$ESR \leq \frac{V_{ripple,pp} \times L_{critical}}{V_{IN} \times D_1 T_s} \quad (8)$$

After finding an appropriate capacitor with the calculated ESR; compare its capacitance with the result from Equation (8) and select larger one.

(Example) If the output voltage ripple is required to be less than 5% of the rated value, i.e. 11.5V, then the output capacitance should be greater than:

$$C_{OUT} \geq \frac{\left(2 \times 0.53 + \frac{0.3 \times 0.47 \times 450 \times 10^{-6}}{120 \times 0.9 \times 0.53 \times 10 \times 10^{-6}}\right) \times 0.3 \times 10 \times 10^{-6}}{2 \times 11.5} = 152 \times 10^{-9} \quad [F]$$

Meanwhile, the ESR of the output capacitor should be less than 7.4Ω:

$$ESR \leq \frac{11.5 \times 450 \times 10^{-6}}{120 \times 1.1 \times 0.53 \times 10 \times 10^{-6}} = 7.4 \quad [\Omega]$$

Since the capacitance multiplied by its ESR is around 100μ as a general rule, the required capacitance is about 13.5μF. Therefore, 15μF is selected (at least). To get an optimal capacitance value, refer to the electrolytic capacitor datasheet that provides the allowable rms current.

Main Features

Described below are the main features of the FAN7340 and the operating principles with the protection functions of the IC against the LED string failures.

V_{CC} Under-Voltage Lockout (UVLO)

To avoid the malfunction of the IC with a low supply voltage, the Under-Voltage Lockout (UVLO) turns off the IC in the event of supply voltage V_{CC} dropping below 8.0V (typical). The UVLO circuit operates to inhibit powering to the IC until V_{CC} is established up to 9.0V (typical).

Enable / Disable the IC

Applying a voltage higher than 1.22V (typical) to the ENA pin enables the IC. Applying a voltage lower than 1.15V (typical) to the ENA pin disables the IC. When the ENA pin voltage is higher than 1.22V (typical) and V_{CC} is higher than 9.0V (typical), the IC starts to supply the reference voltage, 5V to its internal blocks.

Oscillator (Boost Operating Frequency)

The boost operating frequency is programmed by a resistor (R_T) connected from the RT pin to ground. The RT pin voltage is internally regulated to 2V. The current flowing through R_T determines the operating frequency as:

$$f_{OSC} = \frac{1}{(46.5 \times RT\,[k\Omega] + 350) \times 10^{-6}} \quad [kHz] \quad (9)$$

If 100kΩ is used as R_T, the operating frequency is 200kHz. The soft-start time, OLP blanking time, and OCP auto-restart time are determined by the operating frequency.

Soft-Start Function at Startup

In the non-isolation boost converters, the initial feedback voltage is 0V at startup because the output voltage is 0V. According to the negative feedback control, the PWM comparator's output controls the converter to operate with maximum duty cycle. As a result, switching devices can be damaged due to the large current that occurs with the maximum duty cycle. Moreover, it can also result in the initial overshoot of the LED current.

Therefore, during the startup, the soft-start function increases the duty cycle gradually so that the output voltage and current can rise smoothly. The FAN7340 adopts the soft-start function to avoid an inrush current flowing to the output capacitor during startup. The soft-start function operates until the CMP voltage reaches to 4V. The soft-start period can be designed up to 3ms at 200kHz of the operating frequency, which is set to be accumulative time when the BDIM (PWM dimming) signal is HIGH. The soft-start period is related to the operating frequency decided by RT pin resistor, calculated as:

$$t_{SS} = \frac{600}{f_{OSC}} \quad [s] \quad (10)$$

The soft-start period is a cumulative time when the BDIM (PWM dimming) signal is HIGH. Therefore, if PWM dimming duty is 10% and operating frequency is 200kHz, soft-start time could be 30ms.

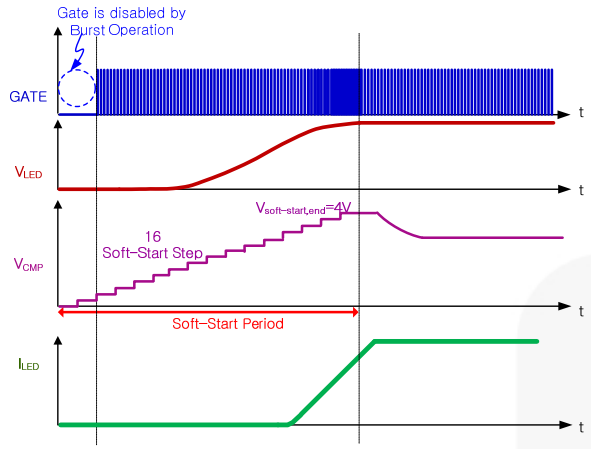

Figure 2. Soft-Start Waveforms

LED Current Setting

The output LED current can be set by Equation (11):

$$I_{OUT} = \frac{V_{ADIM}[V]}{R_{SENSE} + 60[m\Omega]} \quad [A] \tag{11}$$

where V_{ADIM} is the voltage applied to the ADIM pin and R_{SENSE} is the sensing resistor. Additional 60mΩ is the internal wire bonding resistor. To calculate LED current precisely, wire bonding resistor needs to be considered.

Analog Dimming and PWM Dimming

Analog dimming is achieved by varying the voltage at the ADIM pin. It can be implemented either with a potentiometer from the VREF pin or from an external voltage source and a resistor divider circuit. The feedback level (V_{SENSE}) is controlled to follow the ADIM voltage with the feedback gain in the compensation network. Recommended range of V_{ADIM} is from 0.3V to 3.0V.

Internal PWM dimming (BDIM) helps achieve a very fast PWM dimming response in spite of the shortcomings of the boost converter. The PWM dimming signal controls three nodes internally; the gate signal to the switching MOSFET, the gate signal to the dimming MOSFET, and the output connection of the transconductance amplifier. When PWM dimming signal is HIGH, the gates of the switching MOSFET and dimming MOSFET are enabled. At the same time, the output of the transconductance op-amp is connected to the compensation network. It allows the boost converter to operate normally.

PWM Dimming Range

The Dynamic Contrast Ratio (DCR) is the maximum contrast ratio achievable by adjusting the amount of light (dimming) of the screen instantaneously using the backlight during the extremely short time period. The FAN7340 can normally drive the LED backlight under 0.1% dimming duty cycle at 200Hz of dimming frequency. Even turning on during 5μs (dimming MOSFET turn-on time when 0.1% duty cycle with 200Hz of dimming frequency is applied), the FAN7340 can operate the LEDs at a normal peak current level.

Internal Dimming MOSFET

A dimming MOSFET (400V N-channel MOSFET; such as FDD3N40) is included in the FAN7340. The power transistor is manufactured using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology is suitable to minimize on-state resistance ($R_{DS(ON)}$=3.4Ω) to provide superior switching performance. This device is well suited for high-efficiency systems and shows desirable thermal characteristic during operation. To meet the temperature specification of the system, the maximum allowable LED current of the FAN7340 is 300mA with 100% dimming duty. To prevent initial LED current overshoot at low V_{ADIM} levels, the gate resistance of the internal dimming MOSFET is designed as 5kΩ.

Feedback Loop Compensation Design

The compensation network to stabilize the system could be either Type-I configuration (a simple integrator) or Type-II (an integrator with additional pole-zero pair). The type of the compensation circuit is selected according to the gain and the phase of the transfer function of the power plant at the cross-over frequency.

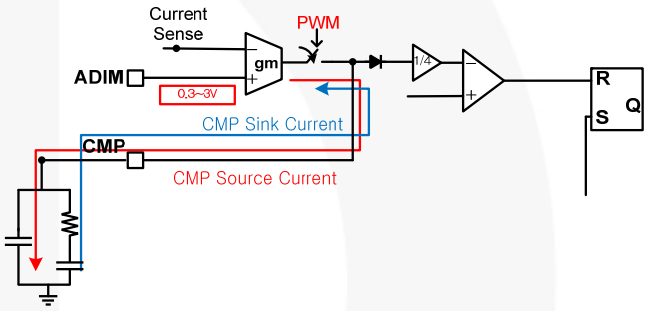

Figure 3. Negative Feedback Compensation Loop

Current Mode Control

While the duty cycle of the main switch is produced by comparing a control signal reflecting the system output voltage or current with an internal sawtooth waveform in voltage-mode control, the inductor current or main switch current is sensed and directly compared with a control signal in current-mode control.

Current-mode control has two feedback loops: an outer loop compares the output-voltage (or output-current) with a reference and delivers the control signal resulting from the comparison to an inner one that compares the current of the main switch with the received control signal and produces an appropriate duty cycle of the main switch. According to the methods of comparing the inductor current with the control signal, there are a couple of types of current-mode control: peak current mode control, average current mode control, and hysteresis current mode control.

One of the advantages of current-mode control is a good line regulation because the change of the input line voltage is reflected to the slope of the main switch directly so the duty cycle of the main switch is changed directly as well.

On the other hand, there is a disadvantage of current mode control when operating in CCM. When the duty cycle of the main switch is less than 50%, even if a disturbance is applied to the inductor current, it becomes smaller in successive cycles, as shown in Figure 4(a). When the duty cycle of the main switch is greater than 50%, a disturbance applied is larger in successive cycles, resulting in the sub-harmonic oscillation shown in Figure 4(b). To avoid the sub-harmonic oscillation or divergence, the programmable slope compensation function is required, as shown in Figure 4(c). The system can be stabilized by adding an internal artificial ramp, called slope compensation, on the control signal or the sensed signal of the switch current. Even though the normal operation mode of the boost converter is BCM, CCM operation may occur. Therefore, the FAN7340 uses Peak Current Mode control with programmable slope compensation.

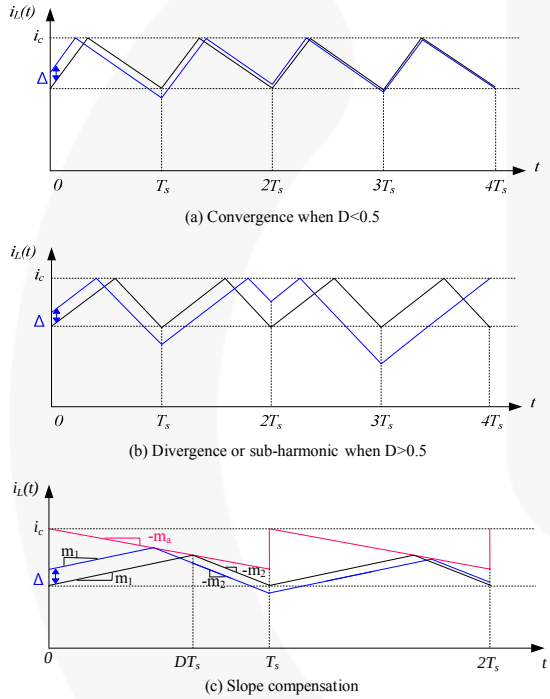

Figure 4. Slope Compensation

Internal R_{slope} resistor (5kΩ) connected to sensing resistor R_s through external resistor R_1 can control the slope of V_{SC} for the slope compensation function in Figure 5. In FAN7340, slope compensation is programmable by changing the external series resistor (R_1).

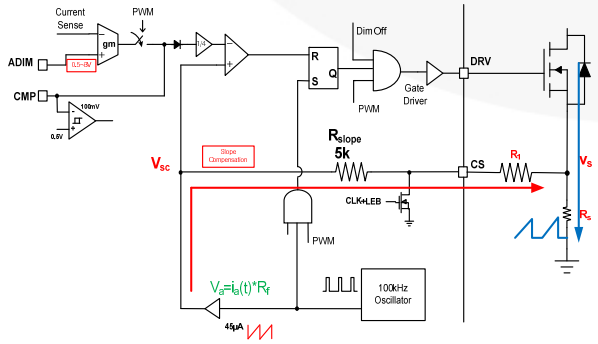

Figure 5. Programmable Slope Compensation

Slope Compensation Circuit Design

Figure 6 shows the internal/external circuit related to the slope compensation network.

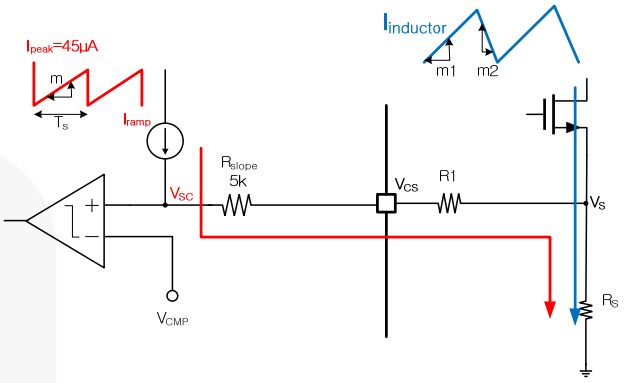

Figure 6. Circuits for Slope Compensation

Since the boost converter operates in CCM (constant frequency) for transient duration, the slope compensation is required to ensure the stability of the converter. This can be achieved by the proper selection of R_1.

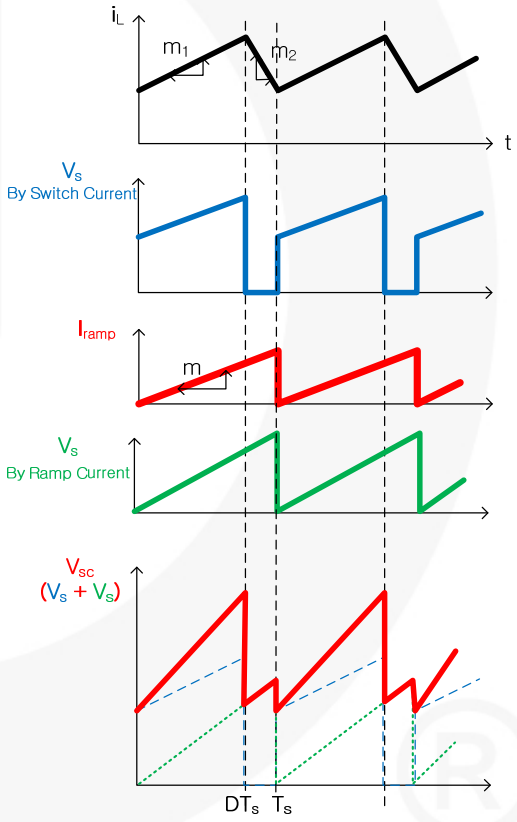

Figure 7. Waveforms of V_{SC}

Figure 7 shows the inductor current and waveforms at the internal V_{SC} node. m_1 is the inductor current slope during the rising time, m_2 is the slope during the falling time. The inductor current slopes are calculated as follows:

$$m_1 = \frac{V_{IN}}{L_{IN}}, \qquad m_2 = \frac{V_{IN} - V_{OUT}}{L_{IN}} \tag{12}$$

When the absolute value of the falling slope is greater than the rising slope, a disturbance applied is larger in successive cycles, resulting in the sub-harmonic oscillation described in the previous section. To avoid the sub-harmonic oscillation, the rising slope has to be steeper than the falling slope. So the slope of the internal ramp current at V_{SC} node, m' should make the rising slope of the sensed inductor current increase and the falling slope decrease to comply with this equation:

$$m_1'+m'>-m_2'-m' \tag{13}$$

Therefore, the required artificial ramp slope is:

$$m'>\frac{1}{2}(-m_2'-m_1') \tag{14}$$

The sensed inductor current slopes at V_{SC} node are represented using the sensing resistor R_s as follows:

$$m_1'=\frac{V_{IN}}{L_{IN}}\cdot R_S,\qquad m_2'=\frac{V_{IN}-V_{OUT}}{L_{IN}}\cdot R_S \tag{15}$$

Since the peak value of the ramp current is 45μA and the maximum duty cycle is 0.9 in the FAN7340, the artificial ramp slope is:

$$m=\frac{I_{peak}}{D_{\max}T_S}=\frac{45\,[\mu A]}{0.9\times T_S} \tag{16}$$

Therefore, the artificial ramp slope at V_{SC} node is:

$$m'=m\times(R_{slope}+R_1+R_S)\approx\frac{45\,[\mu A]}{0.9\times T_S}\times(R_{slope}+R_1) \tag{17}$$

(Example) Using Example 1, R_1 can be calculated with R_S=0.2Ω, R_{slope}=5kΩ.

$$\frac{45\,[\mu A]}{0.9\times T_S}\times(R_{slope}+R_1)>\frac{1}{2}\left(-\frac{V_{IN}-V_{OUT}}{L_{IN}}\cdot R_S-\frac{V_{IN}}{L_{IN}}\cdot R_S\right)$$

$$R_1>\frac{1}{2}\left(\frac{V_{OUT}-2V_{IN}}{L_{IN}}\cdot R_S\right)\times\frac{0.9\times T_S}{45\times10^{-6}}-R_{slope}$$

$$=\frac{1}{2}\left(\frac{230-2\times120}{450\times10^{-6}}\cdot0.2\right)\times\frac{0.9\times10\times10^{-6}}{45\times10^{-6}}-5\times10^{3}$$

$$=-5.4\quad[k\Omega]$$

The negative value means that the slope compensation is enough due to the internal resistor R_{slope}. There is no need to add an external resistor for the slope compensation.

Cycle-by-Cycle Over-Current Protection

A desired output voltage can be obtained by controlling the inductor current directly. It is always necessary to sense the switch current to protect against over-current failures. Switch failures due to an excessive current can be prevented by limiting the drain current, as can be seen in Figure 8.

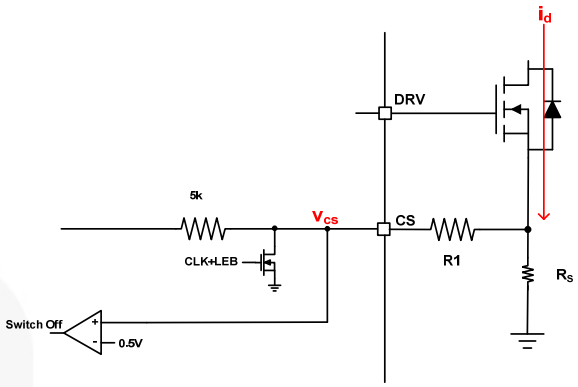

Figure 8. Cycle-by-Cycle OCP Circuit

The drain current of the power MOSFET is sensed by the sensing resistor R_S. If the CS pin voltage exceeds the threshold of approximately 0.5V, the over-current protection function is triggered after a minimum turn-on time or leading-edge blanking (LEB) time.

Due to the internal slope compensation circuit, the CS pin voltage is obtained as follows:

$$V_{CS,pk}=m\times(R_1+R_S)\times DT_S+i_{ds,pk}\times R_S \tag{18}$$

Therefore, the term regarding the slope compensation circuit must be considered when the sensing resistor is designed as Equation (19).

$$R_S=\frac{\left(0.5-m\times(R_1+R_S)\times DT_S\right)}{i_{ds,pk,required}} \tag{19}$$

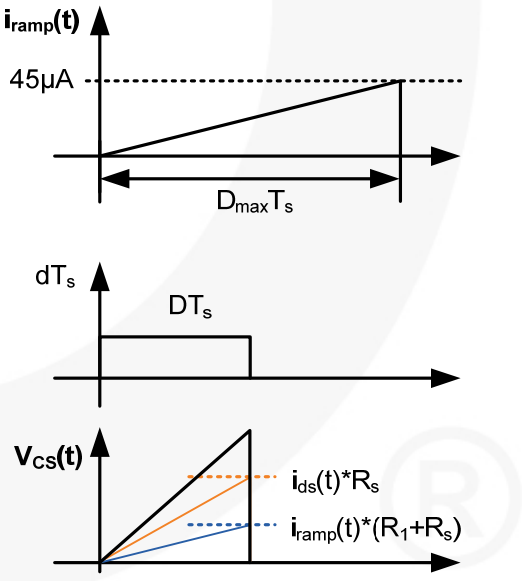

Figure 9. CS Pin Voltage

Over-Voltage Protection (OVP)

The OVP is triggered when the divided output voltage is larger than 3V, as shown in Figure 10. When OVP is triggered, both the dimming switch and boost switch are turned off. The protection is released when the divided output voltage drops below 2.9V, as can be seen in Figure 11. In fact, the abnormal "Open-LED String" status can be protected by the OVP function during open-LED condition.

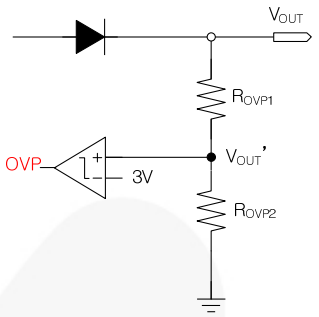

Figure 10. Over-Voltage Protection Circuit

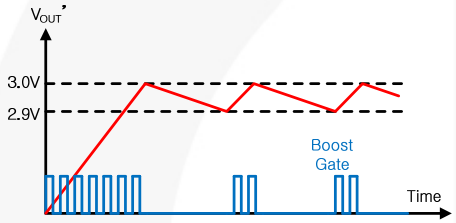

Figure 11. OVP Protection Triggers and Releases

Open-LED Protection (OLP)

The internal circuit for OLP is shown in Figure 12. After a HIGH signal is applied to the ENA and BDIM pins, the LED current is sensed through the feedback sensing resistor (R_{SENSE}) on the SENSE pin. If the voltage on the SENSE pin (V_{SENSE}) drops below 0.2V and lasts 5µs during HIGH BDIM, OLPi signal is generated. Since the LED current cannot be sensed during the PWM dimming off period (BDIM is LOW), the dimming MOSFET is always turned on once OLPi is generated to sense the LED current and count the delay for the OLP signal. Once the OLPi signal is generated, the OLP signal to make the FAULT pin HIGH is produced after a delay of $2^{13}/f_{SW,boost}$, where $f_{SW,boost}$ is the switching frequency of the boost converter. The OLPi signal is disabled during soft-start to avoid a malfunction during that time. The operating timing chart is shown in Figure 13.

Actually, in open-LED condition, the OVP triggers to shutdown the boost and dimming MOSFETs to protect the system. However, in some abnormal conditions (e.g. parts of the LEDs are shorted to the ground, such as direct LED-short condition), the OLP is needed to protect the system because the OVP can't be triggered. In direct LED-short conditions, the duty cycle of the boost switch increases because no LED current is sensed. The output voltage can't increase no matter how much current flow through to the output LEDs, because it is limited to be the sum of LEDs' forward-drop voltage not shorted. This is why the OVP is not triggered in direct LED-short conditions. However, V_{SENSE} is lower than 0.2V, so that the OLPi signal is generated and eventually OLP is triggered after a delay.

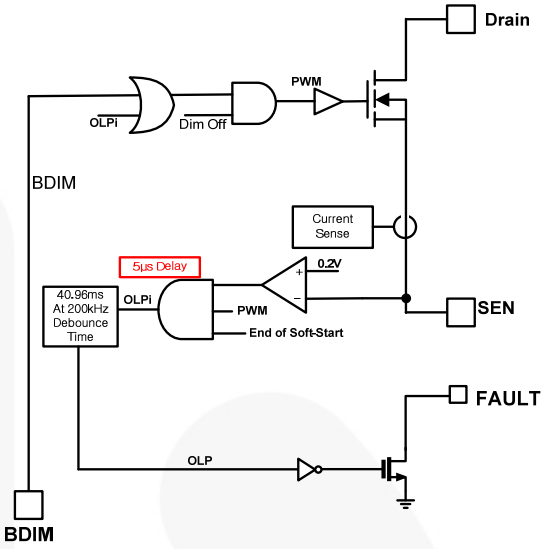

Figure 12. Internal circuit for OLP

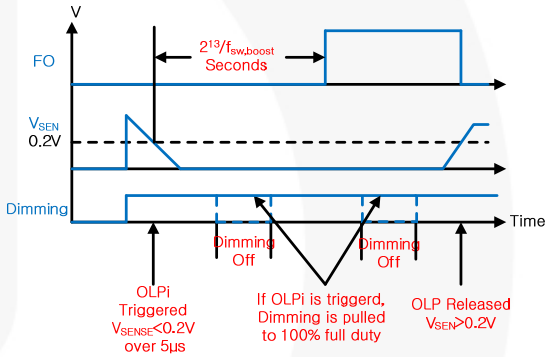

Figure 13. Timing Chart for OLP

LED Over-Current Protection (OCP)

The main purpose of the Over-Current Protection (OCP) is to protect the internal dimming MOSFET from an excessive current. The OCP threshold level is dependent on the ADIM voltage V_{ADIM}, as shown in Figure 14; 1.4V when $V_{ADIM} \leq$ 0.35V, 4 times V_{ADIM} when 0.35V < V_{ADIM} < 1V, and 4V when $V_{ADIM} \geq$ 1V. After V_{SENSE} exceeds the OCP threshold, the boost MOSFET and dimming MOSFET are turned off with a delay of 1µs. The OCP operates as an auto-restart with the period as follows:

$$t_{AR} = \frac{2^7}{f_{SW,boost}} \quad (20)$$

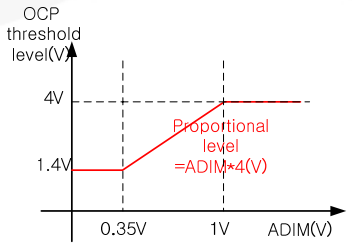

Figure 14. OCP Threshold Level vs. V_{ADIM}

Miscellaneous

PCB Layout Guideline

The power ground (PGND) patterns should be separated from the signal ground (SGND) patterns. All external components connected to the IC GND should be placed near the IC as close as possible. The capacitor connected between the REF pin and GND should be placed far away from the switching components and it is necessary to make the ground pattern as short as possible. Inductors, switching MOSFETs, and output diodes are kinds of noise sources on the PCB, so the PCB pattern for them should be thick and short. Because the noise intensity is inversely proportional to the square of the distance, noise-susceptive external components (e.g. wires, jumpers, chip resistors, and MLCCs) should be placed far from the noise sources. The V_{CC} filter capacitor should be placed as close to the corresponding pin of the IC as possible to avoid noise from the switching devices. The IC GND should be connected to the power GND of the output capacitor.

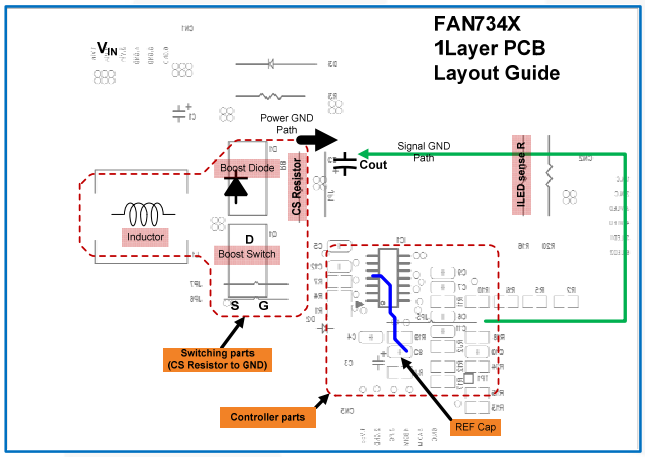

Figure 15. PCB Layout for Evaluation Test Board

External Input UVP using ENA Pin

The inductor peak current is large if input voltage is small. To prevent over-current caused by low input voltage, the system is protected by the Under-Voltage Protection (UVP) using the ENA pin. The input voltage is sensed through the dividing resistors connected between positive rail and the return rail, as shown in Figure 16. When the input voltage is low enough, the input of ENA pin becomes LOW, then the FAULT pin lets the PMOS off.

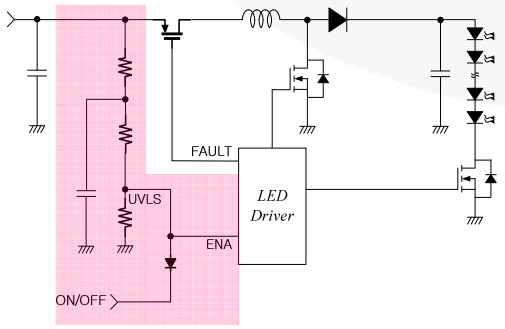

Figure 16. Input UVP Using ENA Pin

Compensation Network Design

Figure 17 shows the internal block diagram and the vicinity of the FAN7340 for regulating the output LED current.

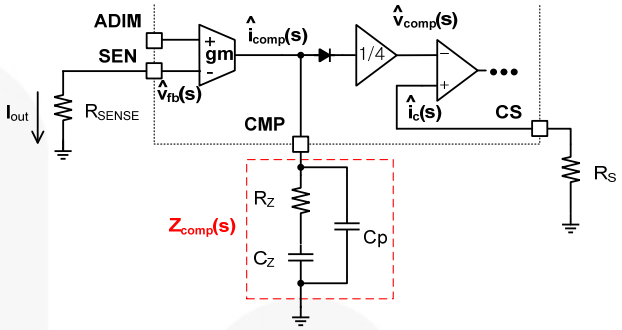

Figure 17. Internal Block Diagram and Compensation Gain for Regulating the Output LED Current

Equations (21)~ (23) are obtained from Figure 17.

$$\hat{v}_{comp}(s) = \hat{i}_c(s) \times R_S \tag{21}$$

$$\hat{v}_{comp}(s) = \frac{1}{4} \times \hat{i}_{comp}(s) \times Z_{comp}(s) \tag{22}$$

$$\hat{i}_{comp}(s) = \hat{v}_{fb}(s) \times g_m = (\hat{i}_{out}(s) \times R_{SENSE}) \times g_m \tag{23}$$

Combining the above equations gives the following:

$$\frac{\hat{i}_c(s)}{\hat{i}_{out}(s)} = \frac{R_{SENSE} \times g_m \times Z_{comp}(s)}{4R_S} \tag{24}$$

where:

$$Z_{comp}(s) = \frac{1}{sC_Z} \cdot \frac{1 + sR_ZC_Z}{1 + sR_ZC_P} \tag{25}$$

On the other hand, when the boost converter is operating in BCM or DCM, the simplified small-signal model is obtained by letting the input inductor zero, as depicted in Figure 18.

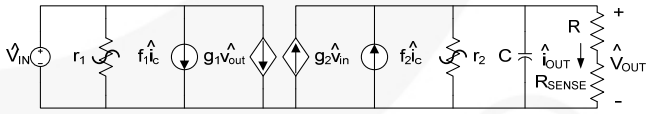

Figure 18. Small-Signal Model for DCM Boost Converter

The control-to-output transfer function $G_{ic}(s)$, ignoring the effective-series-resistor ESR of the output capacitor, is:

$$G_{ic}(s) = \left.\frac{\hat{i}_{out}(s)}{\hat{i}_c(s)}\right|_{\hat{v}_{in}(s)=0} = \frac{K}{1 + \frac{s}{\omega_p}} \tag{26}$$

where:

$$K = f_2 \cdot \frac{(R \parallel r_2)}{R}, \tag{27}$$

$$f_2 = \frac{2I_{OUT}}{I_c},$$ I_{OUT} is the output LED current, (28)

$$I_c = \sqrt{(V_{OUT} - V_{IN}) \cdot \left(1 + \frac{m'}{m_1}\right)^2 \cdot \frac{2I_{OUT}}{L_{IN} f_{OSC}}},$$ (29)

m' is defined in Equation (17).

$R = nr_{LED}$, n is the number of LED,
r_{LED} is the dynamic resistance of LED,
$r_2 = R_{LED} \frac{M-1}{M}$, (30)

$$R_{LED} = \frac{V_{OUT}}{I_{OUT}}, \quad M = \frac{V_{OUT}}{V_{IN}},$$, and (31)

$$\omega_p = \frac{1}{(R \parallel r_2)C},$$

C is the output capacitor.

The dynamic resistance of LED, r_{LED}, is obtained from the I-V characteristic curve provided by LED manufacturers. Figure 19 shows an example of the I-V characteristic curve of X-Lamp® XB-D LEDs of Cree®. Assuming the output LED current is 300mA and the output voltage is 230V, r_{LED} is the slope of the tangent line at 300mA of LED current. In this case, r_{LED} is about 0.67Ω. To provide the output voltage, 80EA of LED is connected in series. Therefore, the total dynamic resistance of LED string nr_{LED} is 80 times 0.67, i.e. 53.6Ω.

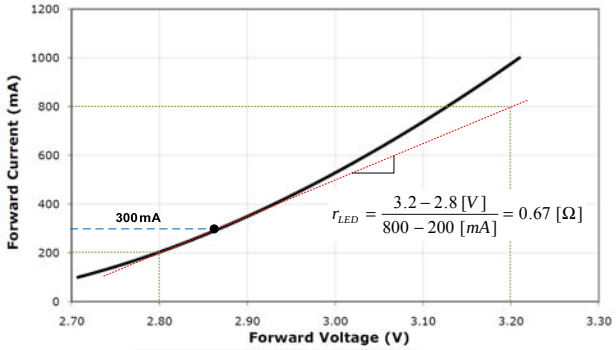

Figure 19. I-V Characteristic Curve and r_{LED}

The procedure to design the feedback loop is as follows:

(1) Obtain the control-to-output transfer function of the power stage using Equation (26). It is one-pole system whose pole frequency is ω_p with the DC gain of K.

(2) Determine the crossover frequency (f_c) around 1/20 of the switching frequency. Since the control-to-output transfer function of the power stage has -20dB/dec slope and -90° of phase shift at the crossover frequency, as shown in Figure 20; it is required to place a zero of the compensation network (f_{cz}) around the crossover frequency so that 45° of phase margin is obtained.

(3) Place a pole of the compensation network (f_{cp}) at least a decade higher than f_c to ensure that it does not affect the phase margin of the compensated system. It should also be sufficiently lower than the switching frequency of the system so the switching noise can be attenuated.

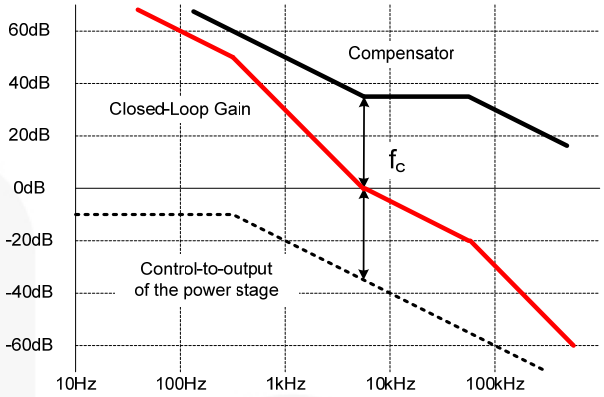

Figure 20. Gain Plot of the System

(Example) Find the control-to-output transfer function of the power stage. The parameters in the previous examples are summarized in Table 2.

Table 2. System Parameters

Parameters	Value
V_{IN}	120V
V_{OUT}	230V
I_{OUT}	300mA
f_{OSC}	100kHz
L_{IN}	450μH
m1'	53,333
m'	25,000
r_{LED}	0.67Ω
n	80
C	15μF
R_{SENSE}	9.94Ω
R_S	0.2Ω
g_m	300μmho

The slope m_1 and m' are obtained from Equations (15) and (17). R_{SENSE} comes from Equation (11) and g_m is found in the datasheet of FAN7340.

The control reference current I_c is calculated as:

$$I_c = \sqrt{(V_{OUT} - V_{IN}) \cdot \left(1 + \frac{m'}{m_1'}\right)^2 \cdot \frac{2I_{OUT}}{L_{IN} f_{OSC}}}$$
$$= \sqrt{(230 - 120) \cdot \left(1 + \frac{25{,}000}{53{,}333}\right)^2 \cdot \frac{2 \times 0.3}{450 \times 10^{-6} \times 100 \times 10^3}}$$
$$= 1.78\,[A]$$

f_2 is obtained as:

$$f_2 = \frac{2I_{out}}{I_c} = \frac{2 \times 0.3}{1.78} = 0.337$$

R is calculated as:

$$R = nr_{LED} = 80 \times 0.67 = 53.6[\Omega]$$

r_2 is obtained as:

$$r_2 = R_{LED}\frac{M-1}{M} = \frac{230}{0.3} \times \frac{230/120 - 1}{230/120} = 367[\Omega]$$

Therefore, the DC gain K and the frequency of the pole are calculated as:

$$K = f_2 \cdot \frac{(R \,\|\, r_2)}{R} = 0.337 \cdot \frac{(53.6 \,\|\, 367)}{53.6} = 0.294 = -10.6dB$$

$$f_p = \frac{1}{2\pi(R \,\|\, r_2)C} = \frac{1}{2\pi \times (53.6 \,\|\, 367) \times 15 \times 10^{-6}} = 227\,[Hz]$$

Next, design the compensation network. Place the crossover frequency of the compensated system at 5kHz, 1/20 of the switching frequency. The gain of the uncompensated power stage at 5kHz is calculated as:

$$G_{@5kHz} = -10.6 - 20 \times (\log(5000) - \log(227)) = -37.45dB$$

Since the DC gain of the compensator should be 37.45dB at 5kHz, R_Z can be obtained as:

$$R_Z = \frac{4R_S}{R_{SENSE} \times g_m} 10^{\left(\frac{37.45}{20}\right)} = 20000 = 20\,[k\Omega]$$

Therefore, C_Z is obtained as:

$$C_Z = \frac{1}{2\pi R_Z \times f_{cz}} = \frac{1}{2\pi \times 20k \times 5k} = 1.59 \times 10^{-9} \approx 1.5\,[nF]$$

Let the frequency of the pole of the compensator placed at 50kHz be a decade higher than the zero. C_P is obtained as:

$$C_P = \frac{1}{2\pi R_Z \times f_{cp}} = \frac{1}{2\pi \times 20k \times 50k} = 0.16 \times 10^{-9} \approx 150\,[pF]$$

Figure 21 shows the result of the compensation network design.

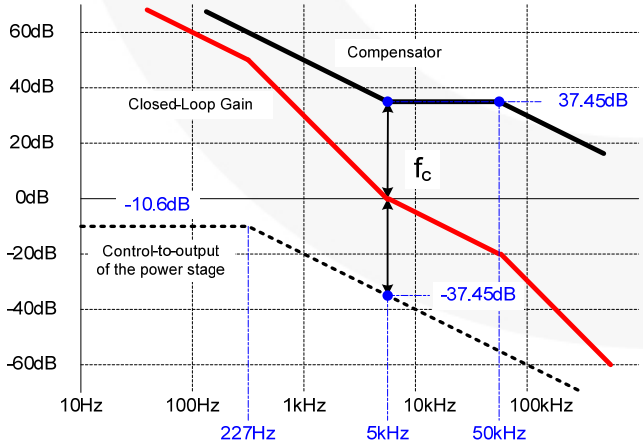

Figure 21. Compensation Network Design

Figure 21 shows the actual Bode plot of the gain and phase of the designed system. The crossover frequency lies around 7.5kHz and the phase margin is more than 45°. The flat region of the compensator has some slope in the actual plot so that the crossover frequency shifts to the higher frequency range compared to the expected and more phase margin is guaranteed.

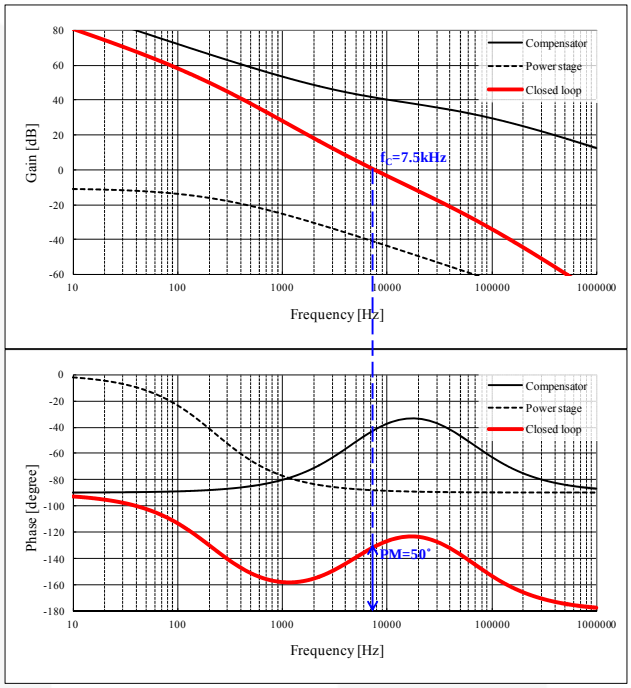

Figure 22. Compensation Network Design in the Actual Bode Plot

References

[1] *Fairchild Semiconductor Application Note "AN-8035, Design Consideration for Boundary Conduction Mode Power Factor Correction (PFC) using FAN7930."*

Related Datasheets

FAN7340 — LED Backlight Driving Boost Switch