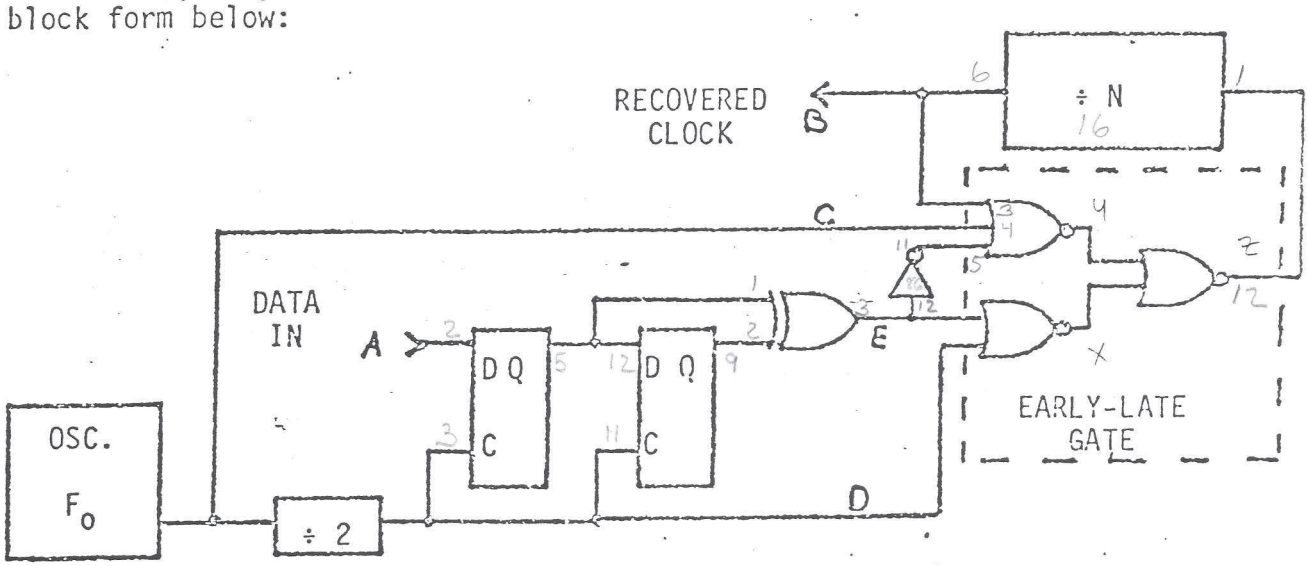
I. Basic Clock Recovery

APPENDIX I

The main purpose of any clock recovery system is to derive from the detected baseband signal, a clock synchronous to the signal for integration sampling or bit detection. Both frequency and phase information are needed to adequately compensate for transmit oscillator offsets and phase detection respectively. Hence, in a phase/frequency locked-loop clock recovery system, bandwidth, aquisition time, stability, phase, and implementation are parameters usually tailored and designed for each particular system. One particular scheme that may be used for clock recovery in data communication systems is the early-late gate digital loop shown in block form below:



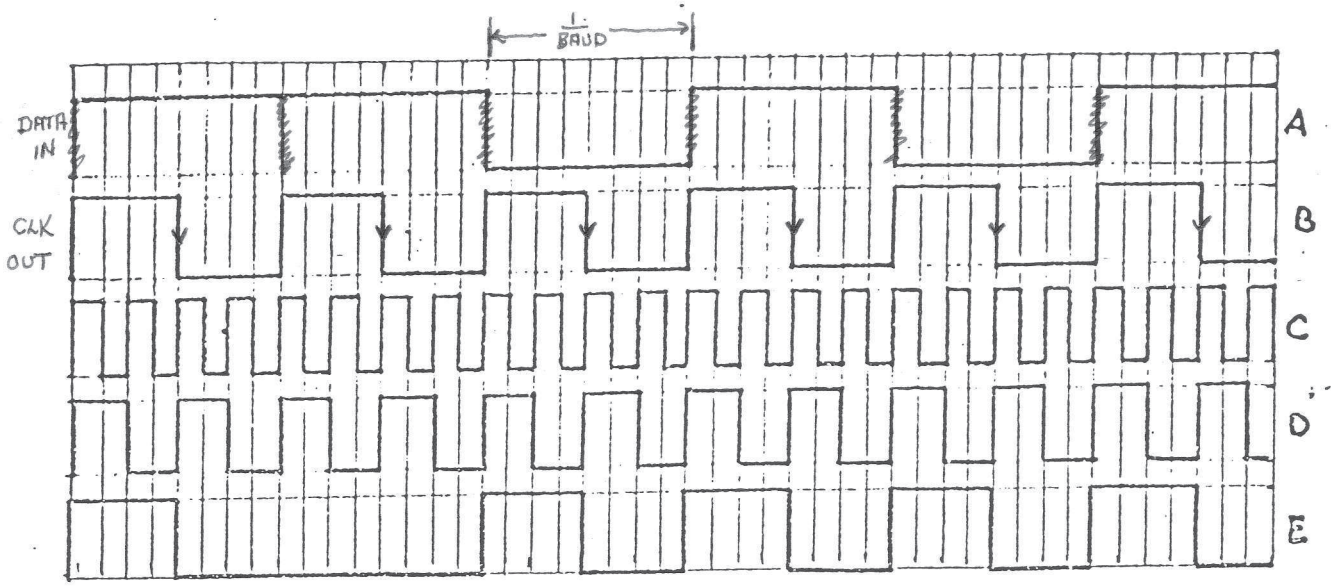
$F_o = 2NR$

Where R is the bit rate in bits/sec.

N = OUTPUT DIVIDER

B_W = BANDWIDTH = $\frac{2R}{N}$

The oscillator produces pulses equal to the pulse width of the synchronous edges of the data (transitions in the data stream) and pulses which are half the duration of the edge pulses. The early-late gate sychronously compares each edge pulse and the rising edge of each divide-by-N clock cycle. If the derived clock is lagging the edge pulse in phase, extra pulses are gated through the divider chain. If leading, pulses are removed from the divider chain. When locked, no pulses are added or removed to the normal number of equilibrium pulses which, when divided, will yield the desired bit clock. Refer to the following timing diagram of an early-late gate when locked:



The bandwidth (tracking) is determined by the expression: $B = 2R/N$ where B is the bandwidth in hertz, R is the bit rate in bits/sec, and N is the basic divide number, or phase increment. The tracking bandwidth is usually symmetric about the center frequency, i.e., the free running frequency with no input applied. Thus a loop for a 3600 BPS data input and a requirement of 10 Hz bandwidth, requires a divide chain of 720 and an oscillator of 5.184 MHz.

The aquisition time is also a function of the loop bandwidth as in any PLL system. Since the digital system will respond to phase variations up to 180^{o} and make incremental phase corrections with one correction per bit transition, lock time, in response to a data signal 180^{o} out of phase with good S/N ratios, is a function of the loop divide chain directly. N/2 bit transitions are required to achieve lock. Thus in the previous example, 360 bit transitions are required to lock to a signal 180^{o} out of phase with high S/N ratios. Of course, in low S/N conditions, the lock time is much longer. Lock time will also be a function of oscillator stability and the transition population of the data signal.

On a dedicated data channel where inband signal rejection is not a problem, the loop should be designed to track the data signal only to the point where the information is useful, i.e., an acceptable channel bit error rate. Nothing is gained by having the loop track lower in S/N beyond this point. The bandwidth can then be made as wide as necessary, thereby achieving the best possible lock times.

The early-late gate loop can also be used for tone detection and the above parameters apply. Tone detection may be accomplished by implementing a loop-lock indicator or correlation using the loop for synchronization. Detailed examples are discussed later for tone detection systems.

The following sections offer a new approach to clock recovery and tone detection that may be implemented, quite simply, using processors. The advantages of a processor phase-locked loop are numerous; no dedicated hardware is needed; since the loop is software, individual

parameters are programable; extremely high Q's or narrow bandwidths are possible; sophisticated algorithms can be integrated into the loop for special functions such as integrate and dump detectors, matched filters, majority logic sampling, etc. The technique is very simplistic and can be implemented in any machine or microprocessor and requires very little memory for the basic loop. Many of the following schemes have been implemented in MC6800 and F8 code.

References:

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