Cost-effective PCB Impedance & Insertion Loss Simulation for a Specific Stackup

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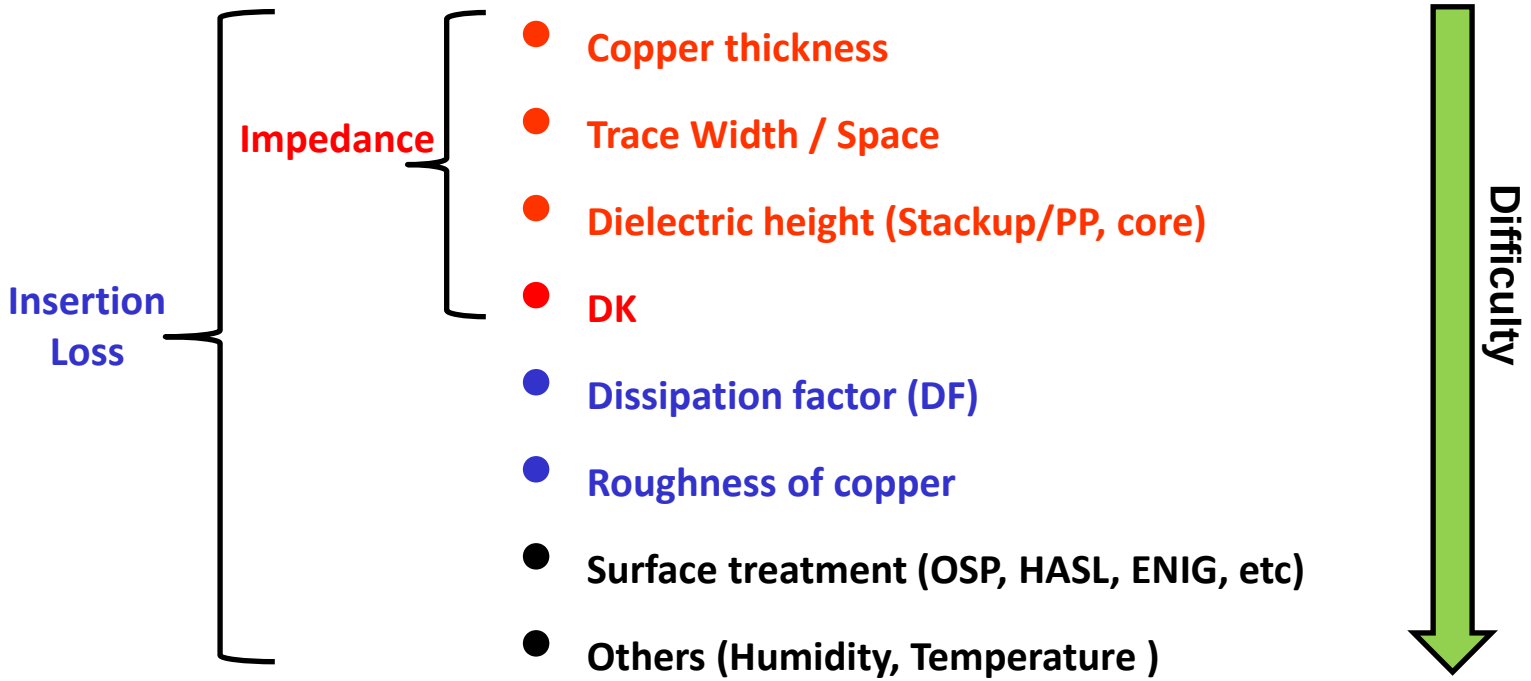
1. Issues of specific stackup design/simulation
2. Basic of impedance / insertion loss
3. Root causes analysis
4. Cost-effective solution

1. Issues of specific stackup simulation

- **Design and simulation of PCB impedance & insertion loss for a specific stackup is challenging**
  - There is 5%~10% impedance off between cross-section model and measurement.
  - High cost repeated trial runs for empirical DK extraction/material characterization.
  - Specific stackup design/simulation almost be considered as a secret on PCB house.

2. Basic of impedance / insertion loss

Key Factors: Dielectric thickness (H), Width (W), Copper thickness (T), Dielectric constant (DK).

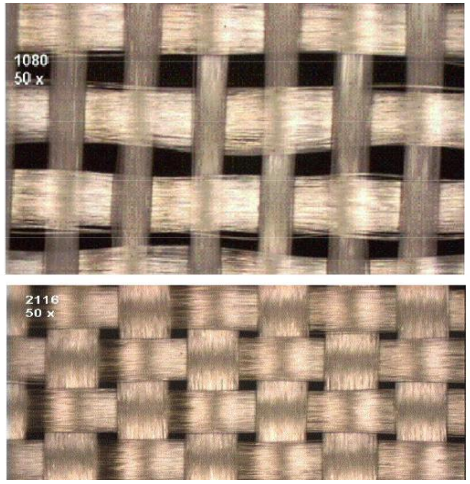


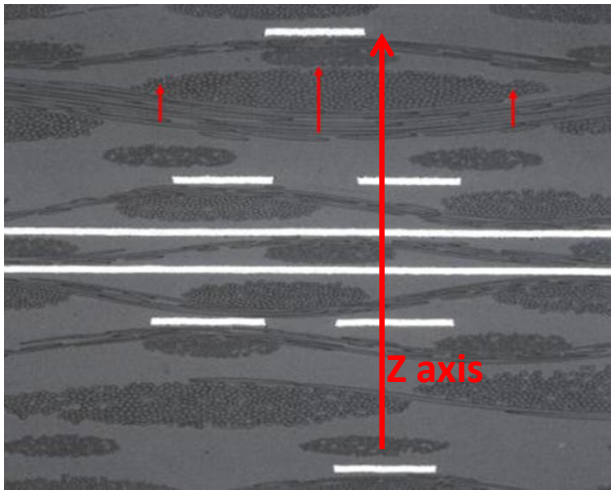
The cross section parameters : H,W,T can be directly measured, but DK is an exception.

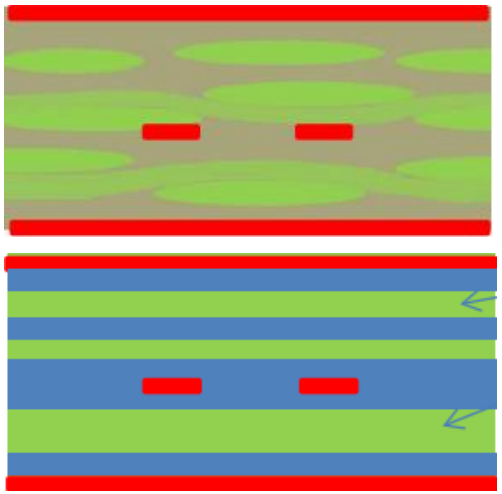
3. Root Causes Analysis

Dielectric constant (Dk):

(1). FR4 is mixture dielectric with glass fiber(DK:4.0~6.5) and resin (DK:2.0 ~ 3.5). DK is inhomogeneous.







(2). Hard to define the DK of multiply PP combination after lamination pressed;

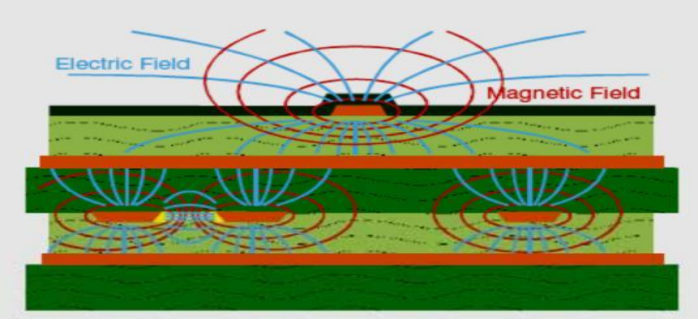
(3). Hard to directly measure the Dk after lamination due to the Dk has been changed;

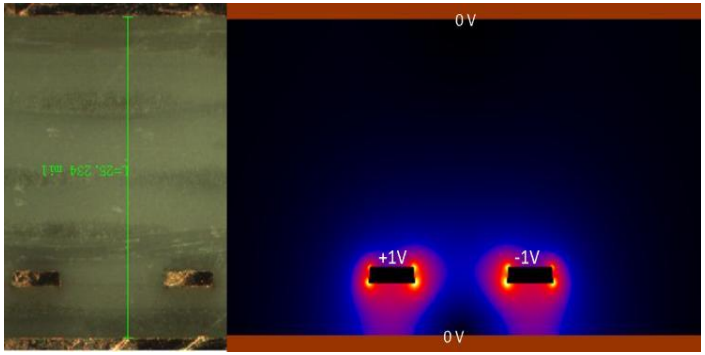
Summary: DK is variable; there is pure resin filled layer surrounds the trace.

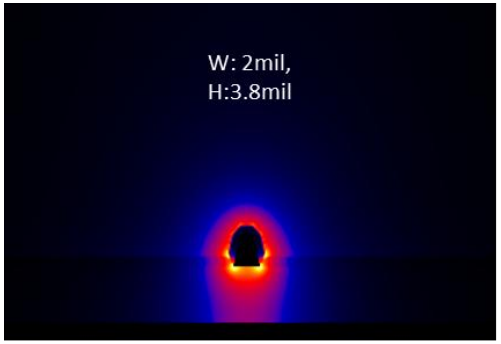
3. Root Causes Analysis

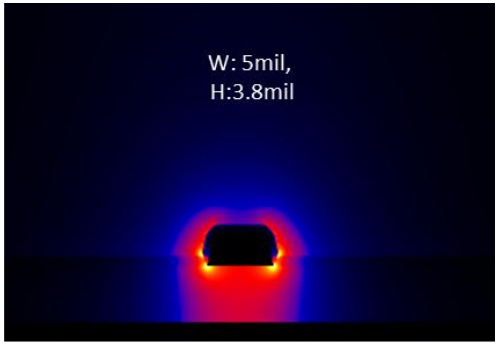
Impedance model: the nature of electromagnetic field.

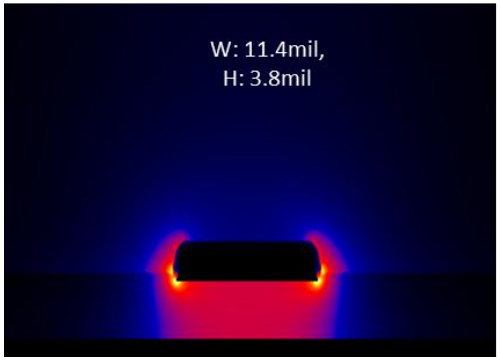
The electromagnetic field density will be different if anyone parameter changed. So the electromagnetic field density is not uniform.

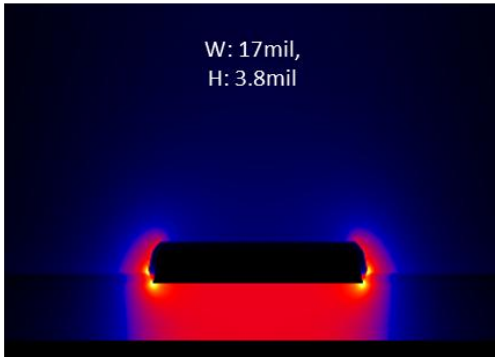








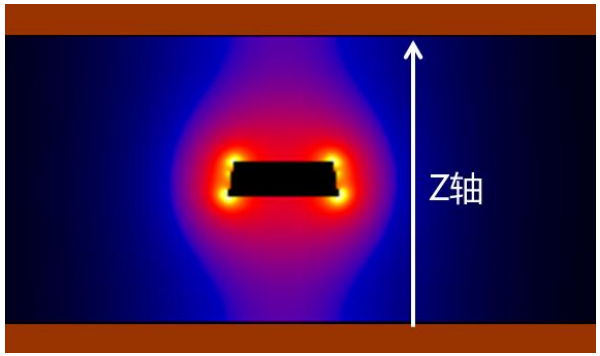




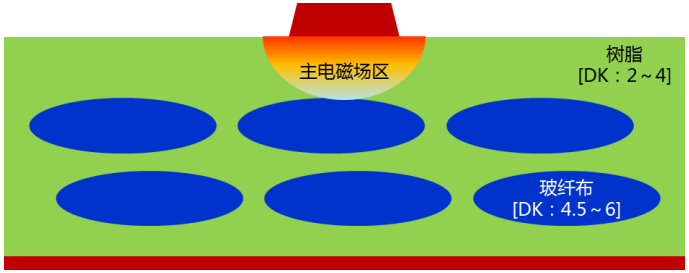
3. Root Causes Analysis

Impedance model With FR4 Dielectric:

(1) Single-end: DK is sensitive effected by the fiber wave effect on Z axis.



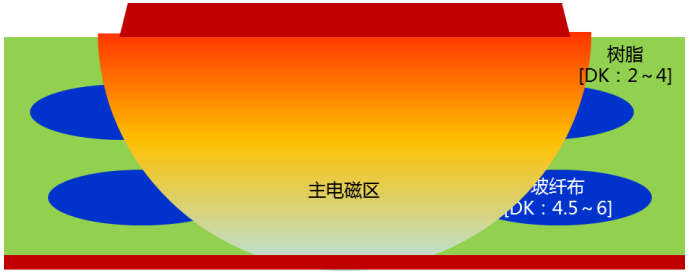
Inner layer single-end stripline



Out layer
Microstrip

Small width with lower DK

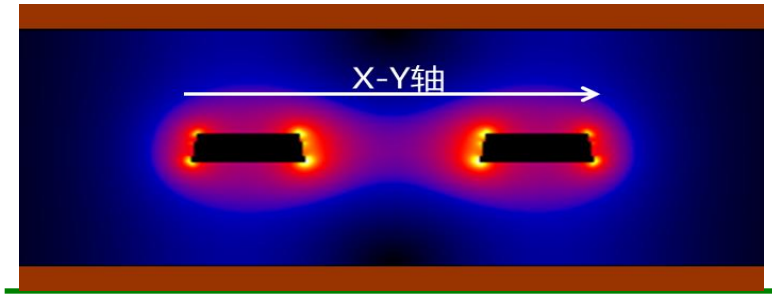
DK ≈ 90%* resign+ 10%*fiber

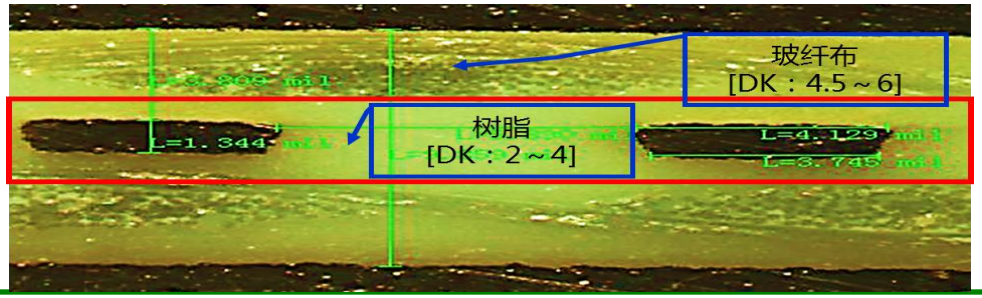


Big width with bigger DK

DK ≈ 30%*resign+ 70%*fiber

(2) Differential stripline: Resin filled DK is sensitive on X-Y axis

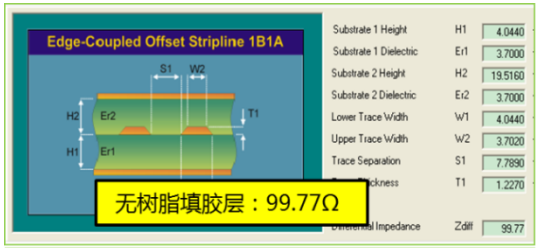


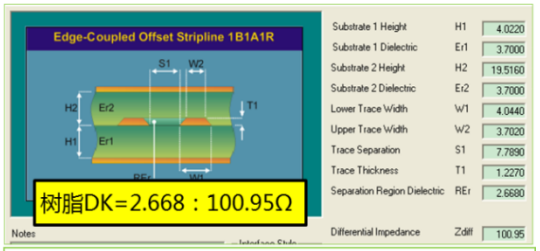


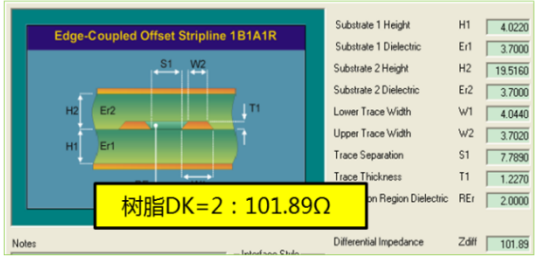
3. Root Causes Analysis

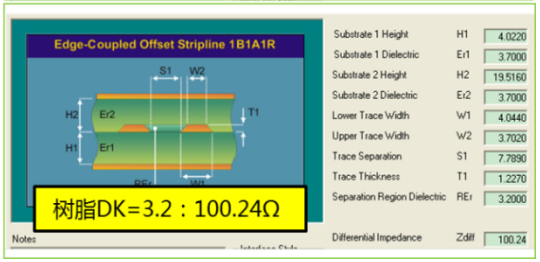
Simulation software accuracy:

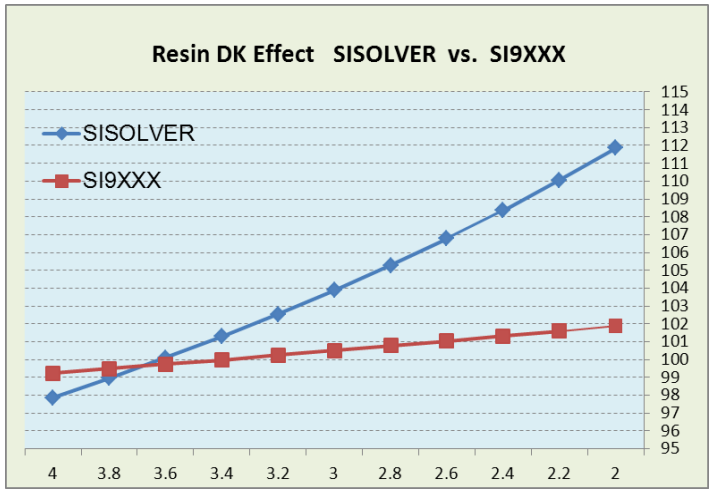
The most popular software is Polar SI8000/SI9000, but there are some accuracy problems on resin filled model.











- **Differential stripline: Allocating different resin DK for resin filled model, but the impedance results almost the same. It disobeys the electromagnetic field theory.**

3. Root Causes Analysis

Back-calculated DK (Empirical DK)

Test boards DK analysis Summary					
Base Material	PP Style	DK Simulation			
		CITS25	SI8000	Datasheet	Difference
Isola-FR408	1080 RC63%	3.08	3.12	3.51	0.39
Isola-FR408	2116 RC53%	3.12	3.13	3.73	0.6
Isola-IS415	1080 RC65%	3.05	3.02	3.52	0.5
Isola-IS415	2116 RC55%	3.06	3.08	3.72	0.64
TUC-TU862	1080 RC67%	3.4	3.43	4.1	0.67
TUC-TU862	2116 RC56%	3.63	3.6	4.3	0.7
TUC-TU862	2116 RC60%	3.8	3.81	4.3	0.49
EMC-EM370D	1080 RC63%	3.24	3.28	3.8	0.52
EMC-EM370D	2116 RC52%	3.47	3.44	4.1	0.66
EMC-EM370D	7629 RC44%	3.66	3.7	4.2	0.5
ITEQ-IT200LK	1080 RC65%	3.14	3.15	3.68	0.53
ITEQ-IT200LK	2116 RC57%	3.14	3.13	3.83	0.7
ITEQ-IT200LK	7628 RC50%	3.31	3.3	3.99	0.69

Base on the experiment:

(1) The experienced data shows big variation between Back-calculated DK and datasheet (range 0.2 ~ 1.5).

(2) The same stackup, different impedance model got different empirical DK.

Conclusion:

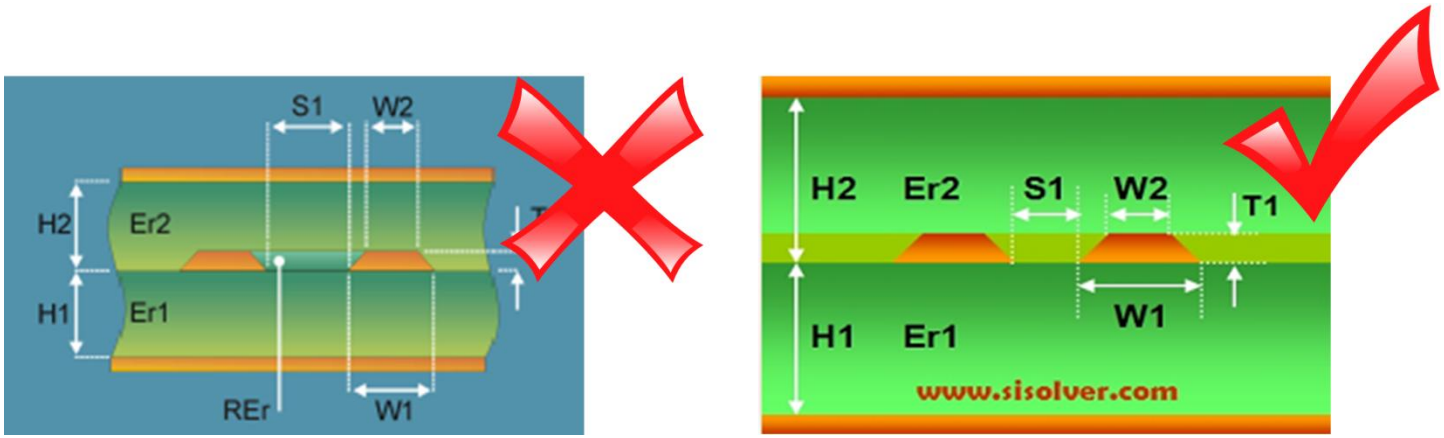
The experiments data proved the real DK of a specific impedance model is variable. Empirical DK can be used for debug, but can not be used for design.

3. Root Causes Analysis

Conclusion:

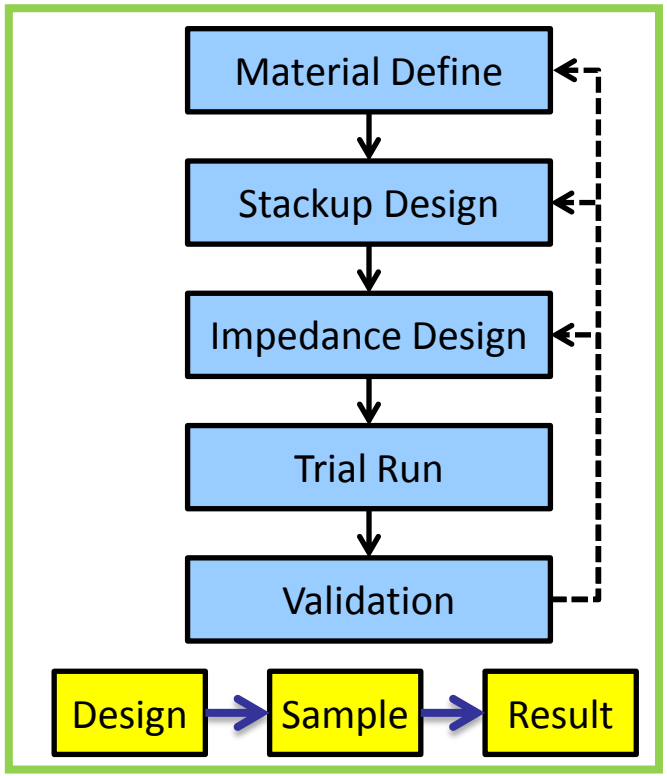
(1) DK：FR4 is inhomogeneous dielectric material, the DK is variable.

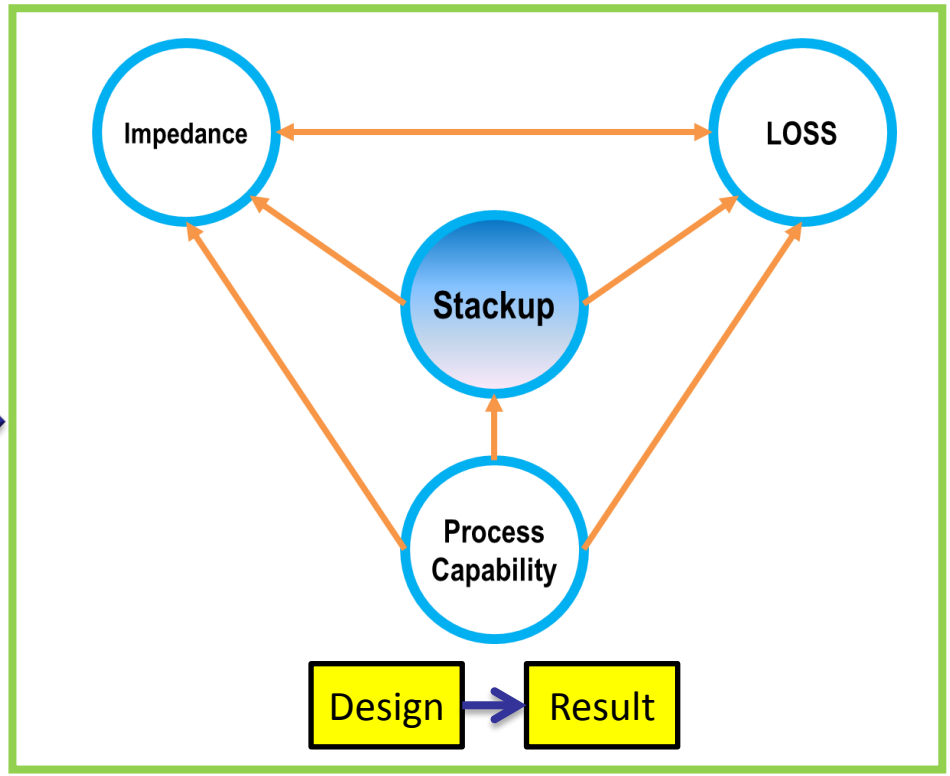
(2) Impedance models accuracy: traditional field solver can not deal with resin filled impedance models.



4. Cost-effective Solution

"All factors, all tools" integrated simulation system:



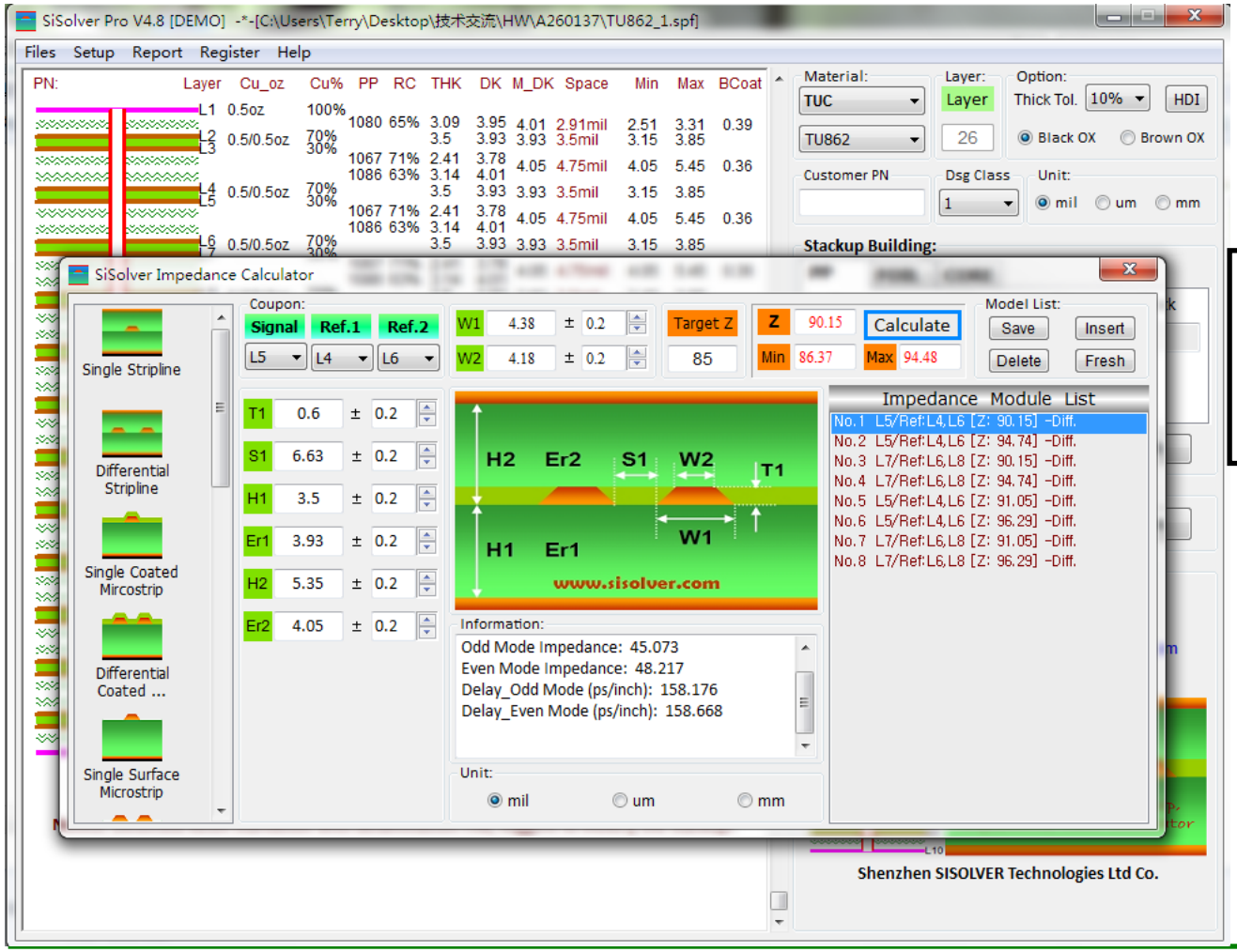


- Avoid to material characterization
- Avoid to repeat trial run
- Easy & fast simulation

- Specific Stackup design and simulation
- DK simulation
- Impedance and loss simulation

4. Cost-effective Solution

“All factors, all tools” integrated simulation system:



- Stackup simulation
- DK simulation Technology
- Resin filled impedance models

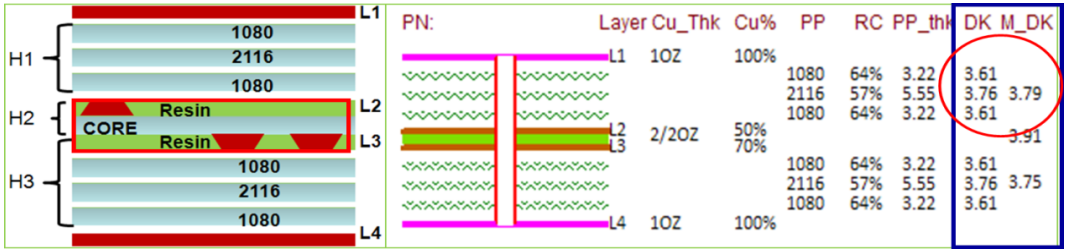
4. Cost-effective Solution

(1) DK Simulation: Any Stackup DK simulation technology solves the Dk variable issue.

Root Cause：
DK is Variable

DK Simulation

- Mixed dielectric DK simulation after pressed
- Pure Resin DK simulation
- Dynamic DK simulation for Single-end models

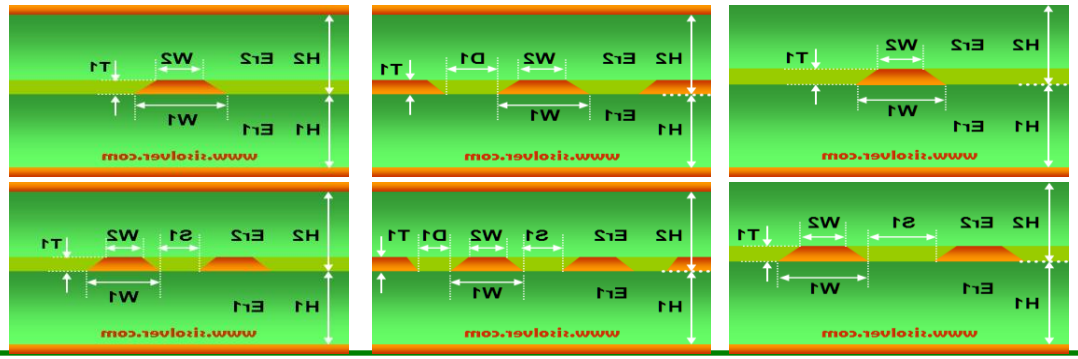


(2) Dedicated Impedance model: high accuracy multi-layer resin filled impedance models

Root Cause：
Model accuracy issue

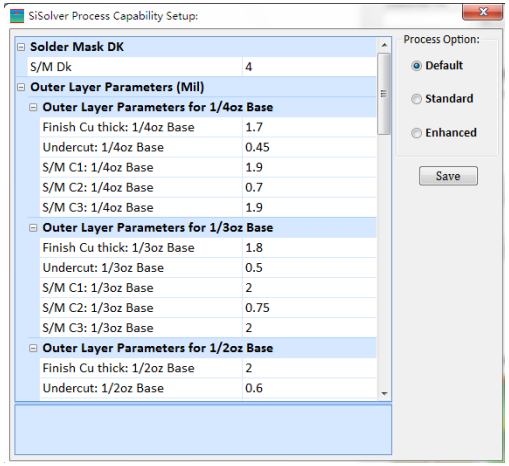
Dedicated model

- High accurate multilayer field solver
- Pure resin DK simulation
- Electromagnetic field density simulation for SE models



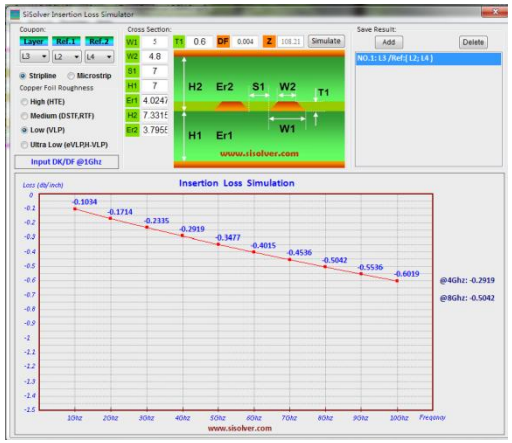
4. Cost-effective Solution

(3) Integrated manufacture process capability



- Finish copper foil thickness
- Etch Factor
- Solder mask thickness
- Resin flow compensation

(4) Fast Loss simulation technology



- Integrated Impedance /Effective DK simulation
- Auto-get stackup parameters
- Integrated 5 types different copper roughness parameters.

4. Cost-effective Solution

Simulation accuracy comparison:

◆ **Fab--F** (TUC-TU768 ， 10L)

Layer	Measure（Ohm）	Polar	Polar Off	SiSolver	SiSolver Off	With（mil）	H（mil）	T（mil）
L3 47+/-4.7	49.25	47.2	4.16%	48.41	**1.71%**	5.12	14.46	0.68
L7 63+/-6.3	64.08	61.05	4.73%	62.88	**1.87%**	2.55	3.73	0.64
L5 98+/-9.8	96.74	92	4.90%	96.81	**0.07%**	4.14	6.92	0.68
L3 83+/-8.3	82.37	76.97	6.56%	82.81	**0.53%**	4.24	4.55	0.61
L3 95+/-9.5	97.63	89.35	8.48%	95.91	**1.76%**	3.77	4.41	0.68
L1 49+/-4.7	50.57	51.91	2.65%	51.39	**1.62%**	12.32	7.16	1.93

◆ **Fab--H** (Panasonic-M6NE, 14L)

Layer	Measure (Ohm)	SiSolver	SiSolver Off	Polar	Polar Off
L3	88.85	87.9	**0.95%**	84.23	**4.62%**
L5	92.39	89.92	**2.47%**	87.2	**5.19%**
L9	92.42	90.28	**2.14%**	86.89	**5.53%**
LII	88.28	85.89	**2.39%**	81.85	**6.43%**

Summary：

- **High efficient**
  - Accuracy improved by 2 to 5 times, help to meet 7%, 5% impedance tolerance.
  - Void to material characterization; avoid to repeat trial run.
- **Cost-effective**
  - High FPY and significantly reduce the scrap rate.
  - Sample cost saving and lead time saving.
- **Communication**
  - Let the design more transparent, build a bridge between layout and PCB house.

SiSolver "All factors, all tools" integrated design system ; easy & fast to simulate /assess any specific stackup!

Q & A

Thank You !