



A Comparison of CML and LVDS for High-speed Serial Links

Introduction

LVDS (Low-Voltage Differential Signaling) is a widely used low-power, low-voltage standard for implementing parallel and low-rate serial differential links in data communication applications. The LVDS standard as currently defined and implemented has some limitations at signaling rates above 1 Gbit/s. CML (Current Mode Logic) I/O buffers such as those used on the HOTLink II™ family of devices offer a simple and effective output structure for use in systems that support signaling rates well above this.

This purpose of this application note is to explain the advantages of serial links over parallel buses, to describe and compare the operation and specifications of the LVDS and CML standards, and detail the methods for interfacing these two standards.

Serial Links vs. Parallel Buses

LVDS has traditionally been used as a standard for implementing parallel buses between chips on PCBs or for connecting boards together with ribbon cables. The low power consumption of LVDS makes it attractive for these types of applications. However, there are problems associated with operating a parallel bus structure like this as system speed and bandwidths increase. These problems and the solution using SERDES devices are detailed in the Cypress application note “Serializing High-Speed Parallel Buses to Extend their Operational Length.” A summary is presented here:

Transmitting a parallel bus between boards via a ribbon cable can result in skewing the arrival time of individual bits with respect to each other and the transmitted clock. This skew can result in set-up or hold time violations at the receiving end and thus limits both the distance and speed that parallel transmission can operate at. This problem compounds as the speed and/or distance of the parallel link is increased.

Using a SERDES (SERializer/DESerializer) device such as the HOTLink II to transmit and receive the data as a serial stream eliminates the problems associated with parallel skew:

- The clock is embedded with the data, thus there is no skew between data and clock signals
- The distance over which the serial link is operated can be changed significantly and the link will remain operational
- The transfer rate of the serial link can be scaled up significantly and the link will remain operational
- Fewer cables are required to implement a serial link than a parallel link.

These benefits of serial links over parallel buses especially apply when transmitting over a backplane, a board that connects multiple cards together within a chassis. Changing from a parallel bus to a serial point-to-point link both simplifies the design and complexity of the backplane as well as allowing for a greater number of cards to be connected together via one backplane.

LVDS and CML Operation

The most common implementation of LVDS is defined in the TIA/EIA-644 standard. The basic LVDS transmitter/receiver structure is shown in *Figure 1*. A switch box in the transmitter steers a small current across the termination resistor (V_{tt}), usually located inside the receiver, to create a differential voltage. This differential voltage should be in the range of 250 mV to 450 mV, requiring a small current source (2.5–4.5 mA) providing LVDS with very low power consumption.

Some of the key specifications of LVDS and the HOTLink II CML IOs are compared in *Table 1*.

Table 1. Comparison of TIA/EIA-644 LVDS and HOTLink II CML IO Specifications

Parameter	Symbol	TIA/EIA-644 LVDS		HOTLink II CML ^[1]		Unit
		Min.	Max.	Min.	Max.	
Output High Voltage	VOH		1.5	2.8	3.1	V
Output Low Voltage	VOL	0.9		2.2	2.6	V
Differential Output Voltage	VOD	250	450	450	800	mV
Offset Output Voltage	VCM	1.125	1.375	2.425	2.875	V
Output Rise/Fall Time	Tr, Tf	260	1500	50	270	ps
Input Voltage Range	Vi	0	2.4	1.15	3.3	
Input Differential Voltage	VDIFFS	100	600	100	1200	mV
Differential Input Impedance	Rin	90	132	HIGH	HIGH	Ohms

Note:

1. Assuming nominal V_{CC} of 3.3V.

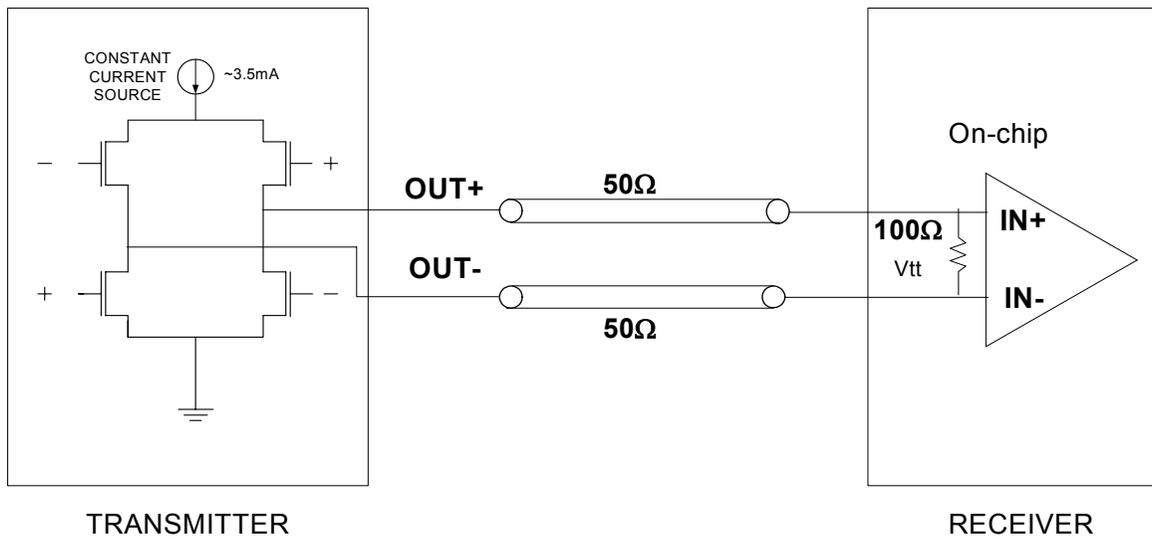


Figure 1. LVDS Transmitter/Receiver Structure

CML (Current Mode Logic) is a de facto standard that is used extensively, industry wide for Physical Layer Devices with serial signaling rates over 1 Gbaud.

A typical CML transmitter/receiver structure is shown in *Figure 2*. The transmitter is constructed from a common-emitter differential pair with 50Ω collector resistors. The output voltage swing is generated by switching the tail current (I_{BIAS}) through the output transistors. Switching a tail current of 16 mA across a 50Ω resistor will create a differential signal swing of 800 mV (1600 mVp-p).

The CML output transistors are permanently biased in the active region, resulting in the ability for much faster switching than technologies that use saturated transistor operation, such as CMOS or most LVDS implementations.

The 50Ω collector resistors also supply source termination when driving 50Ω transmission lines to help increase the signal integrity performance of systems using CML outputs. This source termination prevents any reflections due to imperfect impedance matching between the transmission line and the differential load termination being propagated back down the line. This helps to limit any “ringing” effect seen on the transmission line without requiring any additional external components.

The Cypress HOTLink II serial receivers are implemented using high-impedance input buffers with on chip DC-restoration. The 100Ω differential resistor termination shown external to the receiver in *Figure 2* is necessary to perform impedance matching to the 50Ω external transmission lines. The internal DC-restoration centers the incoming differential signal to V_{CC}/2.

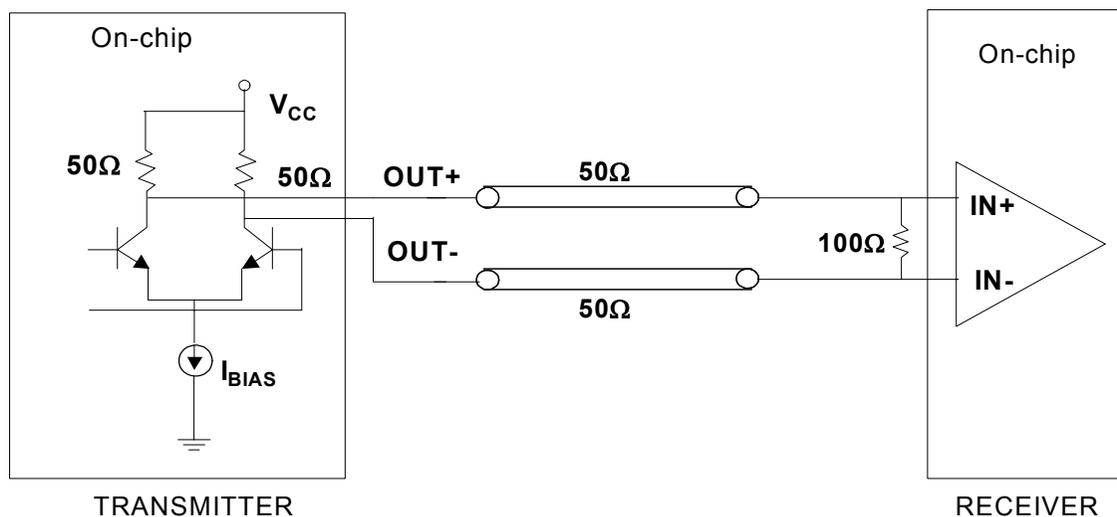


Figure 2. CML Transmitter/Receiver Structure

Maximum Signaling Rates

The TIA/EIA LVDS specification recommends a maximum signaling rate of 655 Mbit/s and a theoretical maximum limit of 1.923 Gbit/s.

This theoretical maximum signaling rate limit is derived from the minimum rise and fall time specification of 260 ps, which aims to minimize the adverse affects of switching noise. The rise and fall time can be a maximum of one half of the transmitted signals Unit Interval to preserve signal quality.

A Unit Interval (UI) is defined as one bit time, which is equal to 1/signaling rate. For example a signalling rate of 500 Mbit/s will have a UI of 2 ns, therefore a minimum rise and fall time of 260 ps allows for a minimum unit interval of 520 ps which is equal to a theoretical maximum signaling rate of (1/520 ps) 1.923 Gbit/s.

The recommended maximum signaling rate limit is derived from the rise time degradation characteristics of a typical cable being driven by an LVDS interface. Assuming a 500-ps rise time degradation across 5 meters of typical cable the minimum rise and fall time seen at the receiver is 500 + 260 ps = 760 ps. This figures yields a maximum UI of 1/(2 * 760 ps) = 655 Mbit/s.

CML output structures are capable of rise and fall times much smaller than this while still preserving quality signal transmission. The constant current source used in the CML output structure creates less switching noise so output rise and fall times of less than 100 ps are possible. CML output structures are currently used almost exclusively for Serial transmission above 1 Gbit/s.

Interfacing between CML and LVDS.

HOTLink II devices can be interfaced to standard LVDS devices easily. The following sections describe suggested methods and circuits for implementing a link from:

- an LVDS output to a CML input.
- a CML output to an LVDS input.

LVDS Output to CML Input

Interfacing from LVDS to the HOTLink II is straightforward. The suggested implementation is shown in *Figure 3*. The minimum output common mode of LVDS (1.125V) is lower than the minimum input common mode of the HOTLink II CML receivers (1.25V), therefore the AC-coupling capacitors, C1 and C2 are necessary to remove the DC content of the LVDS output signal. The DC-restoration of the HOTLink II receiver will re-center the transmitted signal around $V_{CC}/2$ without the need for external components. The 100Ω differential termination (R1) performs impedance matching to the 50Ω lines.

CML Output to LVDS Input

The HOTLink II CML outputs are V_{CC} referenced and as such will be too high to interface directly to standard LVDS inputs, AC-coupling will be necessary to interface between HOTLink II outputs and LVDS inputs. The TIA/EIA spec defines the maximum differential input as 600 mV, though most LVDS implementations will operate correctly with differential input swings much higher than this. It is necessary to check that the maximum input differential voltage of the LVDS buffer is greater than the maximum output voltage swing of the HOTLink II CML output buffers. A suggested implementation is shown in *Figure 4*. The AC-coupling capacitors (C1 and C2) remove the DC-content of the output signal. The resistors R1 through R4 are used for 2 purposes:

1. To restore a 1.2V common mode at the LVDS inputs.
2. For LVDS inputs that do not have on-chip 100Ω termination, to terminate the transmission line to 50Ω, its characteristic impedance.

The resistor values in *Figure 4* have been chosen for the case where the LVDS inputs do not have on-chip termination.

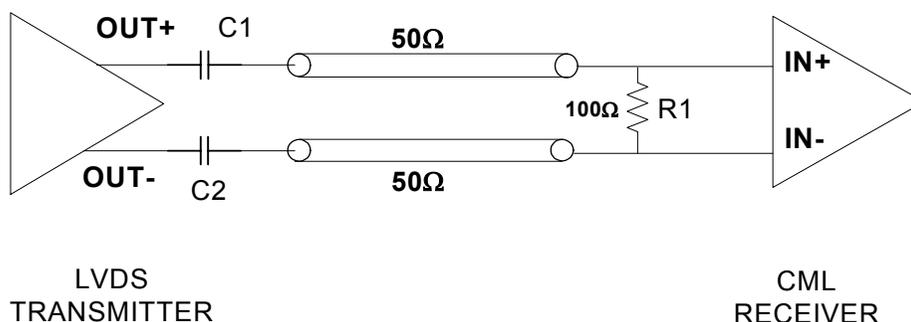


Figure 3. Interfacing LVDS Output to HOTLink II CML Input

The parallel combination of R1//R2 and R3//R4 creates 50Ω termination.

$$\frac{1}{R1} = \frac{1}{R1} + \frac{1}{R2}$$

$$50\Omega = \frac{R1 \times R2}{R1 + R2}$$

The voltage divider creates 1.2V DC biasing on the LVDS input.

$$1.2 = 3.3 \frac{R2}{R1 + R2}$$

$$R1 = 1.75 \times R2$$

Solving these equations and using standard 1% resistors gives the values 137Ω for R1 and R3 and 78.7Ω for R2 and R4. In cases where the receiver has on chip termination then the values of R1 through R4 can be chosen only to satisfy point 1 above and much larger resistor values can be used.

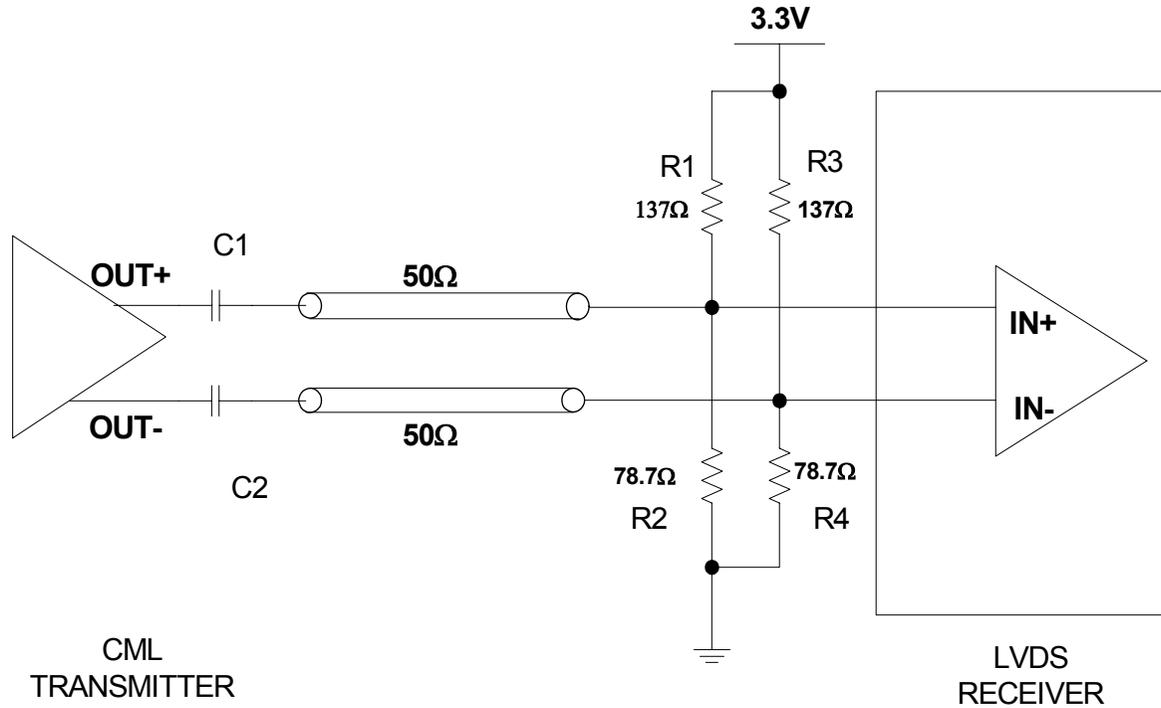


Figure 4. Interfacing from CML to LVDS without On-chip Termination

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approved dsg 12/20/02