

On Process Variation Tolerant Low Cost Thermal Sensor Design in 32nm CMOS Technology

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ABSTRACT

Thermal management has emerged as an important design issue in a range of designs from portable devices to server systems. Internal thermal sensors are an integral part of such a management system. Process variations in CMOS circuits cause accuracy problems for thermal sensors which can be fixed by calibration tables. Stand-alone thermal sensors are calibrated to fix such problems. However, calibration requires going through temperature steps in a tester, increasing test application time and cost. Consequently, calibrating thermal sensors in typical digital designs including mainstream desktop and notebook processors increases the cost of the processor. This creates a need for design of thermal sensors whose accuracy does not vary significantly with process variations. Other qualities desired from thermal sensors include low area requirement so that many of them maybe integrated in a design as well as low power dissipation, such that the sensor itself does not become a significant source of heat. In this paper, we present a process variation tolerant thermal sensor design with (i) active compensation circuitry and (ii) signal dithering based self calibration technique to meet the above requirements in 32nm technology. Results show that we achieve $\pm 3^\circ\text{C}$ temperature accuracy, with a relatively small design. This compares well with designs that are currently used.

Categories and Subject Descriptors

B.8.1 [Integrated Circuits]: VLSI(very large scale integration).

General Terms

Design, Measurement, Performance

Keywords

Thermal sensor, Self Compensating Comparator, Dithering

1. INTRODUCTION

As CMOS technology continues to scale down to attain higher performance and integration, power densities also continue to increase. Higher power densities lead to higher temperatures of operation of a chip, which may cause it to malfunction [1]. The

recommended junction temperatures of Intel 1.5Ghz Pentium 4 processor and AMD 1.2Ghz Athlon processor are 72°C and 95°C respectively [2]. It is also reported that 1°C decrement in temperature can reduce IC failure by 2-3% [2], which emphasizes the need temperature control of a chip. On-die thermometers are an integral part of this thermal control system and are the subject of study in this paper.

From a digital design perspective, if a processor is designed for the worst case power dissipation and the worst case ambient temperature, the design needs to maintain a large performance guardband, leading to poor performance. A more preferred approach is to reduce performance guardband that allows a chip to operate at higher performance levels while avoiding chip failures at high temperatures by implementing a thermal sense and respond technique. The response typically involves relaxation of cycle time by throttling clock and lowering frequency.

Until recently, thermal sensing was done by off-chip thermometers. However, due to the thermal resistance and capacitance of chip packaging, they suffer from time lag in sensing. This, points to a need for integrated on-die thermal sensors [3]. Integrating thermal sensor provides instant information to enable real time thermal management [3]. There are many off-chip thermal sensors which provide high accuracy in sensing which is not the case with the integrated thermal sensors. Also, on-chip thermal sensors are required to be compact in area and easy to integrate leading to some compromises.

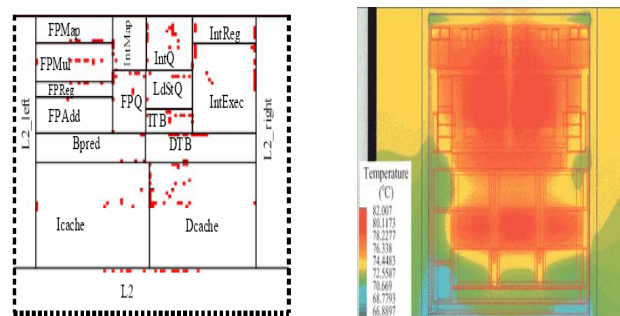


Figure 1 a) Distribution of hotspots for each processor block for SPEC 2000 benchmarks [4]. b) Map of FET junction temperatures for 115W packaged Power4 chip [4].

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Another problem in today's processors is that the temperature is not evenly distributed across the chip. Units like ALU, register banks have higher temperatures than units like caches that tend to have low temperature [4]. Also the temperatures of the units vary with time and are specific to workload. Figure 1 shows the

distribution of temperature for processor block for SPEC2000 benchmark [4]. Efficient thermal management techniques can be employed if we can sense the temperature of the thermal hotspots on the chip.

In most thermal sensors used today, the accuracy of sensing is improved by temperature calibration. Temperature calibration compensates for inaccuracies in temperature measurement and helps improve system accuracy. However, temperature sensor calibration is expensive. First, it imposes an overhead in design cost and silicon area. Secondly, there is a calibration cost as it requires pre heating and testing the sensor to know the offset, drift, slope and uncertainty errors. Once these errors are known the sensing unit is calibrated using A/D converters and look-up tables. Compensating for dynamic errors require even more complex signal processing. Thus, testing imposes test time overhead that translates to cost, while A/D converters and look-up tables impose area overhead. It is well known that the accuracy of the thermal sensors decrease dramatically without calibration. Table 1 shows the un-calibrated readings of the thermal assist unit used in IBM25PPC750L processors [5]. The difference between highest and lowest reading shows the sensitivity range of the TAU which is reproduced below for readers' convenience.

Table 1. Un-calibrated Worst case readings of Thermal Assist Unit(TAU) readings for IBM25PPC750L Processors (°C).

Actual temperature	Highest reading	Lowest reading
35	46	13
95	109	61

The cost of calibration can be expensive. Particularly in products featuring more than one thermal sensor [6] can be prohibitive. Consequently, many commodity microprocessors use uncalibrated thermal sensors [7]. Our goal is to devise an architecture which eliminates the need of calibration while providing high accuracy sensing.

In un-calibrated sensors, an effect of process variation on sensing accuracy is of paramount importance. Unfortunately, process variation has become a larger concern with rapidly scaling technology [8]. The basic element of the proposed sensing circuit uses a pair of matched transistors which are highly sensitive to process variation. The central goal of this paper is to reduce the effect of process variation between the matched transistors and increase the accuracy of sensing.

In most of the reported literature, impact of process variation and calibration/test cost has not received adequate attention. In this paper, we mainly focus on how to devise an on chip sensor architecture that senses most of the hotspots, occupy little area, provide high accuracy in sensing and reduce the test and calibration cost. Figure 2 shows the overview of our design approach.

The rest of the paper is as organized. In section 2 architecture and design of the thermal sensor is discussed. Section 3 shows the effect of process variation on the sensing accuracy of the thermal sensor. Compensation circuitry to overcome the limitations posed by process variation is discussed in section 4. Section 5 introduces dithering and demonstrates how the compensation circuitry and dithering together reduces the effect of process variation and help

increase accuracy of the thermal sensor. Conclusions and future work are described in section 7.

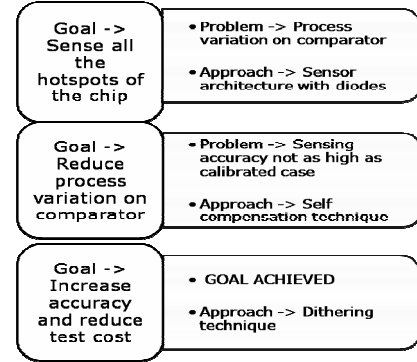


Figure 2 Overview of design approach

2. RELATED WORK

Many on-chip thermal sensor designs have been proposed in the recent years based either on MOS or bipolar circuits [3]. Sensor size is a critical design concern in embedded thermal sensors. Unfortunately, there appears to be a direct trade-off between sensor accuracy and sensor area.

CMOS sensor for low cost applications with limited measurement range based on time-to-digital converter was proposed by Chen et al [9]. Differential cascade amplifier based sensor working on dynamically biasing the sensor based on output current was proposed by Syal et al [10] [11]. Kohari et al [12] developed cascade current mirror based frequency output thermal sensor, which produced currents and voltage independent of supply voltage. Ring oscillator based temperature sensor with very limited accuracy was proposed [13]. For wide range of temperature sensitivity substrate PNP transistor based thermal sensor was proposed [14]. Comparison of these sensors on accuracy, power dissipation and area is given in [15].

Most of these sensors have large area overhead. Low area overhead differential temperature sensor was proposed by Roy et al in [16]. However, this design suffers from relatively low accuracy. In most of the reported literature, impact of process variation has not received adequate attention. In this paper, impact of process variation on sensing accuracy is of paramount importance.

3. THERMAL SENSOR ARCHITECTURE AND DESIGN

3.1 Sensor architecture

In this section, the overall architecture of the proposed sensor is described. Figure 3 shows the block diagram of the sensor architecture. If sensor size is large, it cannot be placed where the thermal hotspots are as the thermal hotspots on a chip also happen to be some of the densest circuit regions. Instead of placing the entire sensor near a thermal hotspot, we propose to use a probe. The probe is simply a p-n junction diode connected to resistors. p-n junction diodes occupy little area and have strong temperature dependence ($-1.6\text{mV}/^\circ\text{C}$) [17]. Thus they are ideal to be placed in a highly dense area of a chip. The rest of the unit comprise of analog multiplexor to probe multiple points on a chip and a comparator to compare the reference voltage that corresponds to

some temperature. The comparator unit works as a single-bit A/D converter that tells whether the sense voltage is above or below a threshold.

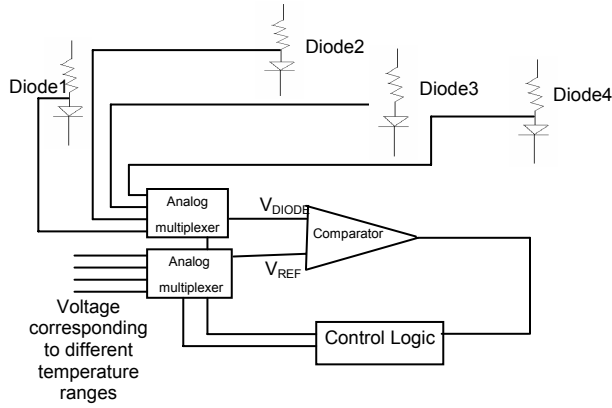


Figure 3 Sensor architecture

Selection of the reference voltage corresponding to specific temperature and selection of sensing module is done by analog multiplexers, which are controlled by control logic. Thus wide ranges of temperature at different parts of the chip can be sensed by multiplexing. As the comparator is based on MOS technology, effect of temperature on it is minimal [18].

3.2 Comparator design

In this thermal sensor architecture accuracy and speed of sensing mainly depends on accuracy and speed of the comparator. It is a general practice to use op-amps as comparators, but using op-amps as comparators often degrade the performance of the comparator [19]. The design of comparator here is based on Differential Cascade Voltage Switch Logic (DCVSL). DCVSL is constructed of differential NMOS pair which senses the input difference and cross coupled PMOS transistors which act as load. DCVSL has lower power dissipation, occupies lesser area and has lesser delay compared to the traditional CMOS designs [20].

The Figure 4 shows the comparator design. The NMOS transistors M1 and M2 are the differential pair which senses the reference voltage V_{REF} and the output voltage V_{DIODE} of the sensing module respectively. The NMOS transistor M3 acts as a constant current source for transistors M1 and M2. The PMOS transistors M6 and M7 drive the output HIGH if SEN signal is low, i.e. when it is not sensing.

When SEN is high transistor M3 is ON and transistors M6 and M7 are OFF. If V_{DIODE} is higher than V_{REF} , slightly more current flows through transistor M2. This causes unequal voltage drop across M4 and M5 and thus the voltage at the drain of M1 and M2 are different. As drains of M2 and M1 drive the gates of M4 and M5, regenerative action takes place pulling M5 to saturation and M4 to triode region and drives the output HIGH. If V_{DIODE} is less than V_{REF} , more current flows through M1 and the output is driven LOW. When SEN is low transistor M3 is OFF, the sources of M1 and M2 are floating and the output is driven HIGH by transistors M6 and M7.

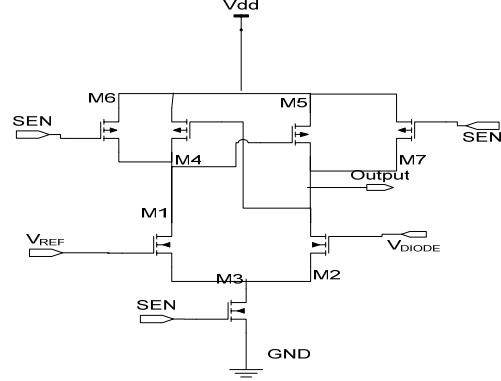


Figure 4 Comparator circuit

3.3 Impact of process variation

Operation of the comparator is based mainly on the difference in current flowing through M1 and M2, to which input voltages are fed. The current through drains of M1 and M2 is determined by the overdrive voltage of the transistors, which is given by

$$I_D = K' * (V_{GS} - V_T)^2$$

$$K' = \mu_n * C_{ox} * \left(\frac{W}{L}\right)$$

When both the transistors have identical dimensions and threshold voltages, drain current only depends on the gate-source voltage V_{GS} . Since both the transistors have identical source voltage, the drain current depends on the gate input voltage only. Due to process variation, threshold voltage V_T of the transistors M1 and M2 may differ which result in variation of the current through transistors. Even when the inputs are at same voltage the currents through the transistors are not same. This leads to incorrect sensing of the temperature. Thus there is certain voltage difference between the inputs called the input offset voltage for which the currents through the transistors are same and the comparator operates properly.

The input offset voltage of the comparator plays a major role in determining the accuracy of the comparator. The offset voltage may result from transistor dimension mismatch as well. However, it can be mapped as a function of threshold voltage of the transistors.

$$V_{os} = f(V_T)$$

As described earlier, process variation causes the input offset voltage to be higher leading to incorrect sensing of temperature. Moreover diode voltage changes only $-1.6\text{mV}/^\circ\text{C}$ [17], so input offset increase of 5mV can lead to 3°C of incorrect sensing.

We performed Monte Carlo simulations for analyzing sensing accuracy of comparator circuits while varying threshold voltage V_T of all the transistors. Fifty comparators were taken as input sample and their operation is observed for 15°C above and below the target temperature of 85°C .

Figure 5 shows the histogram for the number of comparators switching at various temperature points. All the measurements are made on the basis that output voltage of comparator should be LOW below 85°C and HIGH above 85°C .

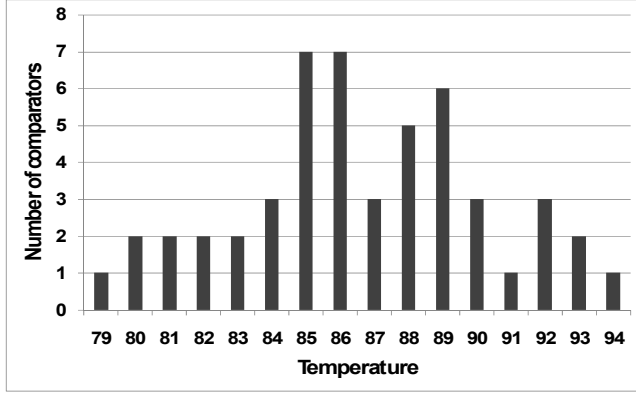


Figure 5 Histogram of trigger temperature for comparator without compensation

From the histogram it is seen that the number of comparators V_s temperature follows a Gaussian distribution with mean at 85 °C. The 3σ variation extends 6 degrees above and 9 degrees below the mean value. This shows that the sensor has less than 7 degrees accuracy in presence of process variation with respect to 3σ variation. All the circuit simulation results are based on HSPICE [21] using 32nm PTM [22] models.

4. SELF-COMPENSATING COMPARATOR

As described earlier, the NMOS differential pair is most sensitive to process variation. Hence comparator can be made process variation resilient by compensating the process variations in NMOS differential pair. To achieve this we added a compensation circuitry for the crucial transistors M1 and M2. We have also seen in the previous section that current changes in transistors M1 and M2 lead to incorrect sensing of the comparator. The idea of compensation circuitry is to map the current flowing through the transistors to voltage across capacitors, and use this voltage to reduce the current through the other transistor by body biasing. The body effect describes the changes in the threshold voltage by the change in voltage between source and body, called the source-bulk voltage. For an enhancement mode, NMOS body effect upon threshold voltage is computed according to the Shichman-Hodges model [23].

$$V_T = V_{T0} + \gamma \left(\sqrt{(2\Phi_f + V_{SB})} - \sqrt{2\Phi_f} \right)$$

$$\gamma = \sqrt{\frac{2qE_{Si}N_{SUB}}{C_{ox}}}$$

For $V_{sb} < 0$ threshold voltage V_T increases which increases the current through transistor and $V_{sb} > 0$ vice versa happens.

The self compensating circuitry can also be build by connecting two transistors called back-gates in parallel to the two critical NMOS transistors. These back-gate transistors can be biased through the voltages on the capacitor and the current flowing through the critical transistors can be controlled.

4.1 Operation of self compensating comparator based on body biasing

The self compensating comparator based on body biasing is shown in the Figure 6. The body of transistors M1 and M2 is connected to the compensation circuitry, which includes capacitance C1 and C2 for storing the source-bulk voltage for M2 and M1 respectively. Transistors M3 and M4 act as training transistors, that map the current in M1 and M2 to voltage on C1 and C2. Transistors M5 and M6 pull body of M1 and M2 to ground while transistors M7 and M8 pull the body to voltage on C2 and C1 during different phases of operation. The transistors M14 and M15 act as switches for SEN signal.

The operation of self compensating comparator is divided into two phases, namely training phase and sensing phase. During training phase FET_TRAIN is high and transistors M3, M4, M5, M6, M19 and M16 are ON. Capacitors C1 and C2 are charged through M3 and M4 and body of M1 and M2 is pulled to ground. Same voltage V_{DD} is given to the gates of both M1 and M2 through transistors M16 and M19. Let us assume that due to process variation M1 conducts more current than M2. Since C1 is charged through M1 and C2 is charged through M2, C2 will develop more voltage than C1. During the sensing phase SEN is high and body of M1 and M2 is connected to C2 and C1 respectively as transistors M7 and M8 are ON. As voltage on C2 is higher than C1, due to body biasing the V_T of M2 will decrease and V_T of M1 will increase. Thus V_T mismatch between the two critical transistors is reduced. The value of C1 and C2 and the pulse width of FET_TRAIN pulse is chosen such that charge on them do not leak away before the SEN signal is applied. It is to be noted that before every FET_TRAIN pulse voltages C1 and C2 have to be completely discharged.

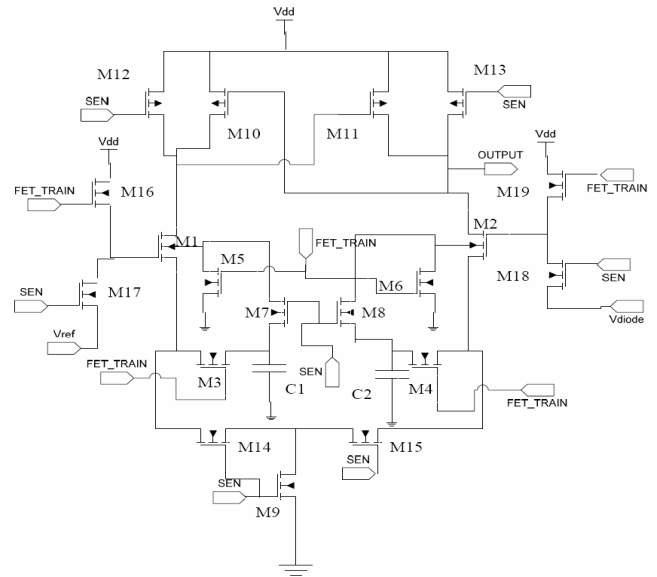


Figure 6 Self-compensating comparator based on body biasing

4.2 Impact of process variation on self compensating comparator

The accuracy of thermal sensor is determined by its ability to sense in presence of process variation. The effect of process variation on self compensated comparator is studied from Monte

Carlo Simulations through HSPICE [21] where all the transistors are subjected to process variation. As M1 and M2 are the differential part of the circuit, they are most sensitive to process variation, and hence the compensation for M1 and M2 yields most benefit.

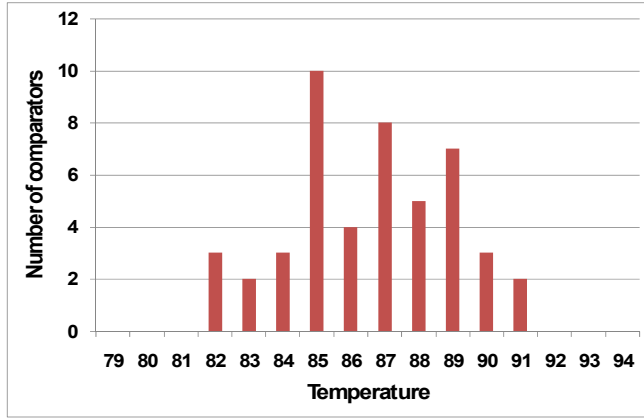


Figure 7 Histogram of trigger temperature for comparator with compensation.

As in the study of process variation on comparator without compensation circuitry, fifty comparators were taken as input sample and their operation was observed for 15 °C above and below the original temperature. From the histogram it is seen that the 3σ variation extends 3 degrees above and 4 degrees below the mean value. This shows that the sensor has less than 5 degrees accuracy in presence of process variation with respect to 3σ variation. This is an improvement from 7 °C to 4 °C without any instrumentation.

5. SELF-CALIBRATION USING DITHERED REFERENCE

We have seen earlier that testing and calibration of on-chip thermal sensors is expensive and time consuming. We have also shown that accuracy of sensing can be increased but is still not comparable to the calibrated sensor. To increase the accuracy further, without an increase in test cost we propose a novel idea of signal dithering. Dithering is the process of injecting noise into the reference signal in order to reduce noise in measurement. This technique has been used in signal and image processing [24]. We have seen earlier that the process variation of the sensor can be mapped to offset voltage of the comparator. However, after the chip has been manufactured the threshold voltages of the transistors are fixed and the offset voltage of the comparator does not change. To find out the offset voltage of the comparator we dither the reference voltage V_{REF} of the comparator keeping the diode voltage (V_{DIODE}) constant. This can be done by adding a random or for more practical purpose a sinusoidal noise into the reference voltage. Once the offset voltage of the comparator is known the control logic multiplexes the V_{REF} such that the offset voltage is zero or very less.

Figure 8 gives an overview of how dithering is done on the sensor. In order to calculate the offset voltage, multiple measurements are made at a constant temperature with dithered reference signal. Depending on the number of 1s and 0s obtained at the output of the comparator we calculate the offset voltage. If

the number of 1s and 0s are equal then there is no offset or in other words offset is zero. If the number of 1s is greater than number of 0s then the offset is negative i.e. the reference voltage has to be shifted left in order to make the offset zero and vice versa if number of 1s is less than number of 0s.

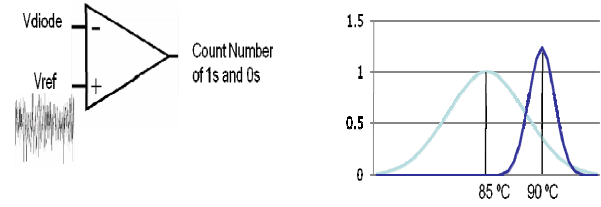


Figure 8 Overview of how dithering is done

The offset voltage is computed based on number of 0(1) at the output of the comparator. The conversion table is based on $\text{erfc}()$ function and is omitted here for the sake of brevity. Once we know the offset voltage of the comparator the sensing can be done accurately by changing the input reference V_{REF} with the offset obtained. Figure 9 shows the histogram of final offset temperature. Final offset temperature results after compensating process variation with dithering based offset estimate. As the histogram shows that dithering improves in sensor accuracy by bringing them closer to the target temperature.

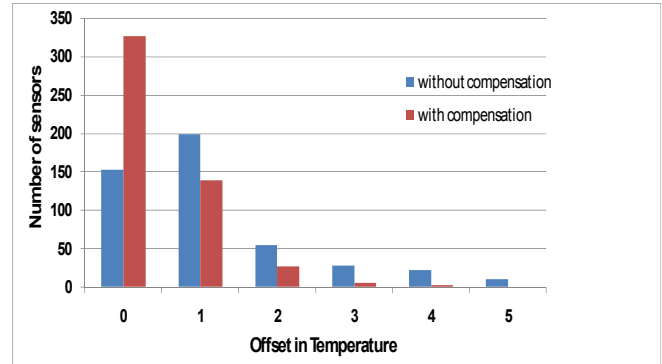


Figure 9 Number of sensors Vs Offset in temperature without compensation circuitry.

The two cases –without compensation and compensation with body biasing are shown in the histogram. It is clear from the histogram that the accuracy improves with combination of active compensation by body biasing and dithering. A single technique is not adequate to narrow the sensor temperature spread. With this calibration technique and compensation scheme presented earlier, we achieve the targeted goal of less than 3 degree inaccuracy for 3σ variation in thermal sensing without using a tester based calibration system. This was the major goal of this work.

6. AREA OVERHEAD AND LEAKAGE POWER

Comparator circuit with compensation deploys twelve more transistors than the comparator circuit without compensation. This results in an area overhead of ~114% for the comparator circuit. However, in this architecture as diodes are the sensing units that

are replicated throughout the chip, the extra transistors added do not cause much area overhead to the entire chip. Also in this architecture there is no area overhead due to the calibration unit.

The difference in the leakage power between the original comparator and self compensating comparator is 0.01nW. This is because the body voltage of the critical transistors M1 and M2 is changed only when they are operating in saturation region. In the rest cases the body of transistors M1 and M2 is connected to ground.

7. CONCLUSION

As thermal management systems gain greater use from mobile devices to mainstream processors, embedded thermal sensors are used more widely. Inaccuracy of thermal sensors reduces effectiveness of thermal management systems. Manufacturing process variations cause inaccuracy problems in thermal sensors. However, in many applications, cost considerations prevent calibration of thermal sensors. We have presented a very small thermal sensor design with active process variation compensation circuitry that improves thermal sensor accuracy by 3 degrees. We are studying various alternatives for improving sensor accuracy and reach the aimed target of 2 degrees. However, the reported scheme is the best so far.

8. ACKNOWLEDGMENTS

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