The George Washington University
Department of Electrical and Computer Engineering

CMOS Operational Amplifier

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Data: 05/14/07

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Introduction

In analog and mixed-signal systems, an operational amplifier (op amp) is commonly used to amplify small signals, to add or subtract voltages, and in active filtering. It must have high gain, low current draw (high input resistance), and should function over a variety of frequencies. The goal of the project is to design a two-stage CMOS operational amplifier with low power dissipation and high gain by using AMI C5N 0.6μm technology.

Architecture and Operation

The two-stage CMOS operational amplifier in this project includes four major circuitries—a bias circuit, an input differential amplifier, a second gain stage, a compensation circuit. The *Input Differential Amplifier* block forms the input of the op amp and provides a good portion of the overall gain to improve noise and offset performance. The *Second Gain Circuit* block is typically configured as a simple common-source stage so as to allow maximum output swings. The *Bias Circuit* is provided to establish the proper operating point for each transistor in its saturation region. The purpose of the *Compensation Circuit* is to maintain stability when negative feedback is applied to the op amp. Figure 1 shows the block diagram of the op amp circuit:

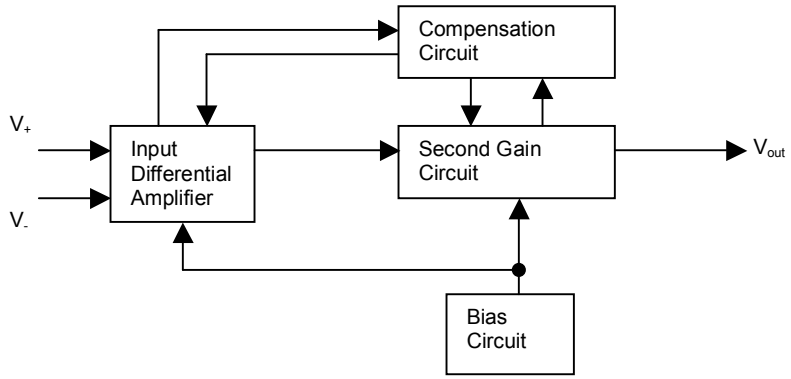

Figure 1 Block diagram of a two-stage operational amplifier

A typical circuit configuration of an unbuffered two-stage op amp (including the *Input Differential Amplifier* and the *Second Gain Circuit*) is shown in Figure 2. Transistors *M1*, *M2*, *M3*, and *M4* form the first stage of the op amp—the differential amplifier with differential to single ended transformation. In this stage, the conversion from differential to single ended is achieved by using a current mirror (*M3* and *M4*). The current from *M1* is mirrored by *M3* and *M4* and subtracted from the current from *M2*. The differential current from *M1* and *M2* multiplied by the output resistance of the first stage gives the single-ended output voltage, which constitutes the input of the second gain stage. The second stage is a current sink load inverter. *M6* is the driver while *M7* acts as the load. Capacitor C_c is used to lower the gain at high frequencies and provide the compensation for the op amp. The first stage and the second stage circuits use the same reference current; hence, the bias currents in the two stages are controlled together.

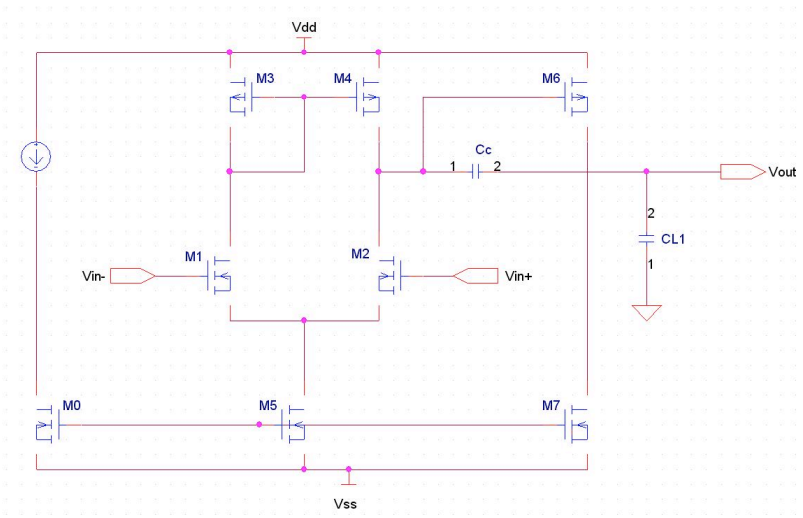

Figure 2 Circuit Configuration for a two-stage op amp with an n-channel input pair

Circuit Design

The design in this project is a two-stage op amp with an n-channel input pair. The op amp uses a dual-polarity power supply (V_{dd} and V_{ss}) so the ac signals can swing above and below ground and also be centered at ground. However, a negative power supply can be a problem for a CMOS circuit due to remaining reverse bias of the source-substrate and drain-substrate p-n junctions. To solve this problem, the substrate of the nMOS transistors should be always tied to the most negative voltage (V_{ss}) in the circuit. The power supply here is constrained within +3.3V and -3.3V (Table 1). Based on the SPICE parameters of AMI C5N 0.6μm technology, the topology was determined to achieve the specifications listed below in table 2 through the op amp design procedure provided in the section 6.3 of CMOS Analog Circuit Design by Phillip Allen. The hand calculation results provided the estimated parameters (such as transistor width and length, capacitance, etc.) to make the circuit schematic (shown in figure 3) in Cadence Virtuoso Schematic Editor and for the circuit analysis in Cadence SpectreS.

Boundary Conditions	**Requirement**
Supply Voltage	±3.3V
Temperature Range	0 ~ 70°C

Table 1 Boundary conditions for the CMOS op amp

Specifications	**Proposed Value**
Gain	≥ 70dB
Gain Bandwidth	≥ 5MHz
Phase Margin	≥ 45°
Settling Time	≤ 1μs
Slew Rate	≥ 5V/μs
Input Common Mode Range (ICMR)	-1.5V ~ 2.5V
Common Mode Rejection Ratio (CMRR)	≥ 60dB
Power Supply Rejection Ratio (PSRR)	≥ 60dB
Output Swing	≥ ±2.5V
Offset	≤ ±10mV
Power Dissipation	≤ 2mW

Table 2 Specifications for the CMOS op amp

Design Procedure (Hand calculation):

This design procedure is to determine each device's size in figure 2

1. Determine C_c to ensure phase margin > 45°:
   $C_c > 0.22 \times C_L = 0.22 \times 10\text{pF} = 2.2\text{pF}$
   (60° phase margin was chosen to ensure phase margin > 45°)

2. Choose C_c as 2.5pF to calculate the current through *M5* in order to meet slew rate specification:
   $I_5 = 2.5\text{pF} \times 10\text{V}/\mu\text{s} = 25\ \mu\text{A}$
   (10V/μs as slew rate was chosen to ensure the slew rate > 5V/μs)

3. Decide *M3* and *M4* size using ICMR $V_{in(max)}$ specification :
   $$(W/L)_3 = (W/L)_4 = \frac{25\mu\text{A}}{(37\mu\text{A/V}^2) \times (3.3\text{V} - 2.5\text{V} - 0.99\text{V} + 0.57\text{V})^2} = 4.7$$

4. Determine *M1* and *M2* size by using gain bandwidth specification:
   $g_{m1} = \text{GB} \times C_c = 5\text{MHz} \times 2\pi \times 2.5\text{pF} = 78.54\mu\text{S}$
   $$(W/L)_1 = (W/L)_2 = \frac{(78.54\mu\text{S})^2}{2 \times 110\mu\text{A/V}^2 \times 12.5\mu\text{A}} = 2.3$$

5. Determine *M5* size using ICMR $V_{in(min)}$ specification ::
   $$V_{ds5} = (-1.5\text{V}) - (-3.3\text{V}) - \sqrt{\frac{25\mu\text{A}}{110\mu\text{A/V}^2 \times 2.3}} - 0.99\text{V} = 0.49$$
   $$(W/L)_5 = \frac{2 \times 25\mu\text{A}}{110\mu\text{A/V}^2 \times (0.5\text{V})^2} = 1.8$$

6. Find *M6* size and the current through *M6* by letting the second pole be equal to 2.2 times GB:
   $g_{m6} = 10 \times g_{m1} = 785.4\mu\text{S}$
   $g_{m4} = \sqrt{2 \times 37\mu\text{A/V}^2 \times 4.7 \times 25\mu\text{A}} = 93.25\ \mu\text{S}$
   $(W/L)_6 = (W/L)_4 \times (g_{m6}/g_{m4}) = 4.7 \times (785.4\ \mu\text{S}/93.25\ \mu\text{S}) = 39.6$

7. Decide *M7* size:
   $$I_6 = \frac{(785.4\mu\text{S})^2}{2 \times 37\mu\text{A/V}^2 \times 39.6} = 210\mu\text{A}$$
   $(W/L)_7 = (I_6/I_5) \times (W/L)_5 = (210\ \mu\text{A}/25\ \mu\text{A}) \times 1.8 = 15.12$

After all the simulations by using parametric analysis, all the transistors' size was adjusted to achieve optimized performance (Table 3 and figure 3).

Device (Figure 2)	Calculated Size	Simulated Size
C_L	10pF	5pF
C_c	2.5pF	2.2pF
M0	1.08μm/0.6μm	1.5μm/0.6μm
M1	1.38μm/0.6μm	8.1μm/1.5μm
M2	1.38μm/0.6μm	8.1μm/1.5μm
M3	4.7μm/0.6μm	8.4μm/1.5μm
M4	4.7μm/0.6μm	8.4μm/1.5μm
M5	1.08μm/0.6μm	1.5μm/0.6μm
M6	23.76μm/0.6μm	72.6μm/1.5μm
M7	9.07 μm/0.6μm	9.45μm/1.5μm

Table 2 Summary of device size parameter

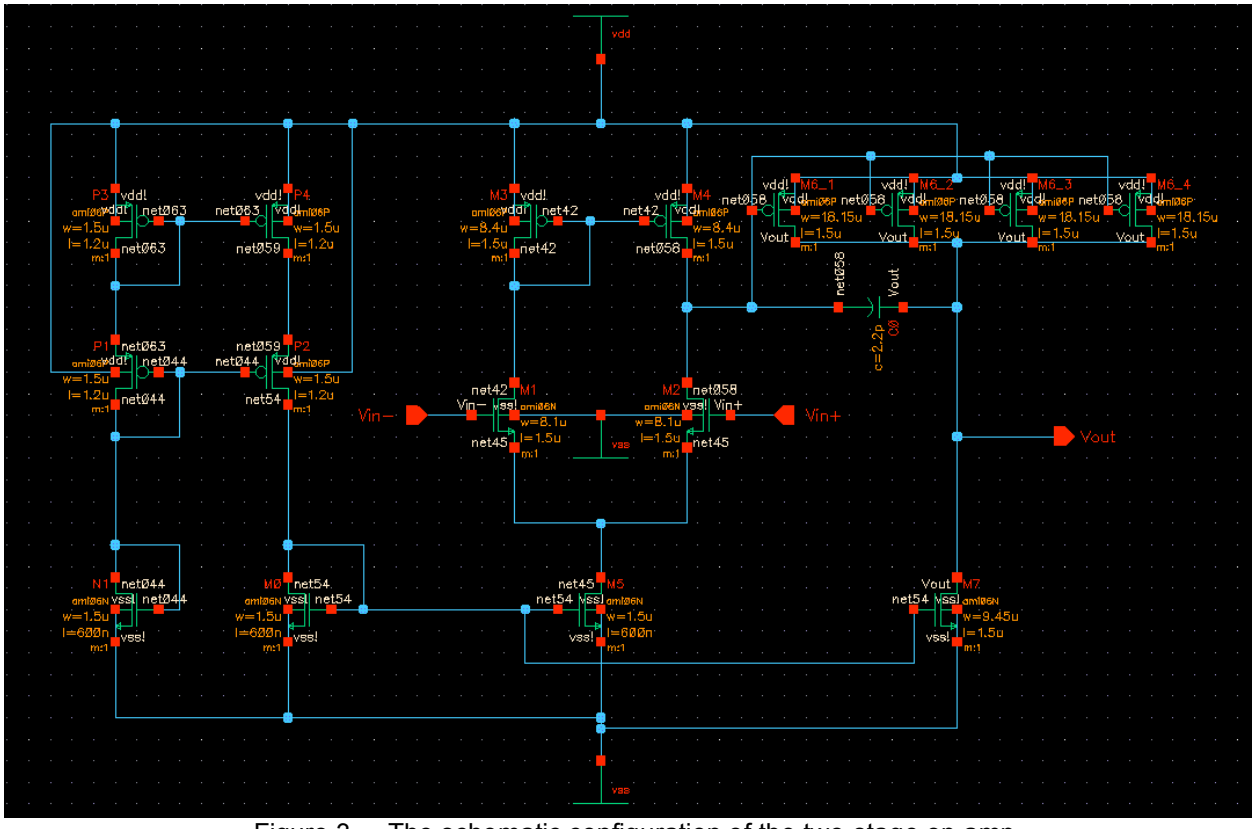

Figure 3 The schematic configuration of the two-stage op amp

Simulation

For circuit analysis, eight different test-bench circuits were made and simulated to examine the performance for each specifications listed above in table 2. All of the simulations used 5pF for capacitance load and 1 MΩ for resistance load.

Frequency Response:

The open-loop gain, gain bandwidth, cut-off frequency, and phase margin were obtained by using ac frequency sweep analysis. In the test-bench circuit (shown in figure 4), the ac voltage source was connected to the V_{in}+ and V_{in}- of the op amp.

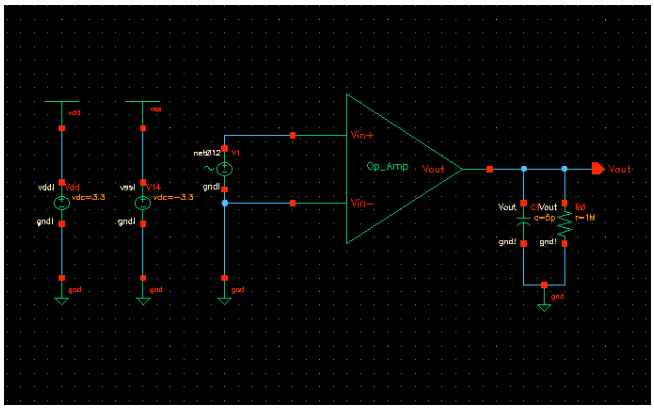

Figure 4 Frequency response test-bench

The graph in figure 5 shows the results of simulation. The open-loop voltage gain is 72.47dB (slightly bigger than the desired specification 70dB). The gain starts to cut off around 1.68KHz (the -3dB frequency). The gain bandwidth is 6.74MHz (the unity gain frequency, 0dB). The phase margin for a 5pF load is 59.1°. The schematic circuit and extracted layout have exactly the same simulation results, and the simulation results compare well with the proposed specifications.

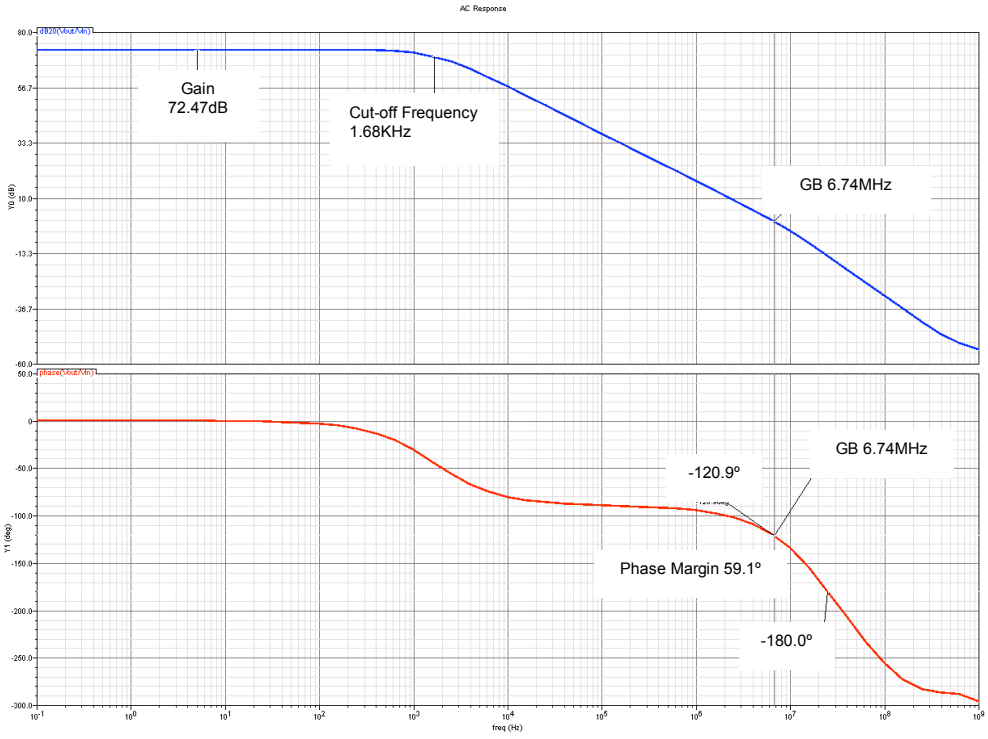

Figure 5 Frequency response simulation result

Slew Rate and Settling Time:

The slew rate is determined from the slope of the output waveform during the rising or fall of the output when input is applied a 0.1V pulse voltage source with a 2µs period. The positive slew rate is 5.53V/µs for schematic simulation and 5.54V/µs for layout extracted, and the negative slew rate is -5.50V//µs for both simulations. The settling time is 0.25µs faster than the proposed specification 1µs for both schematic and layout extracted simulations.

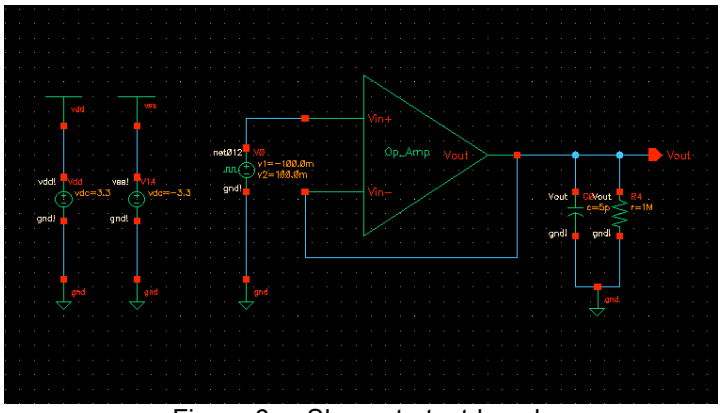

Figure 6 Slew rate test-bench

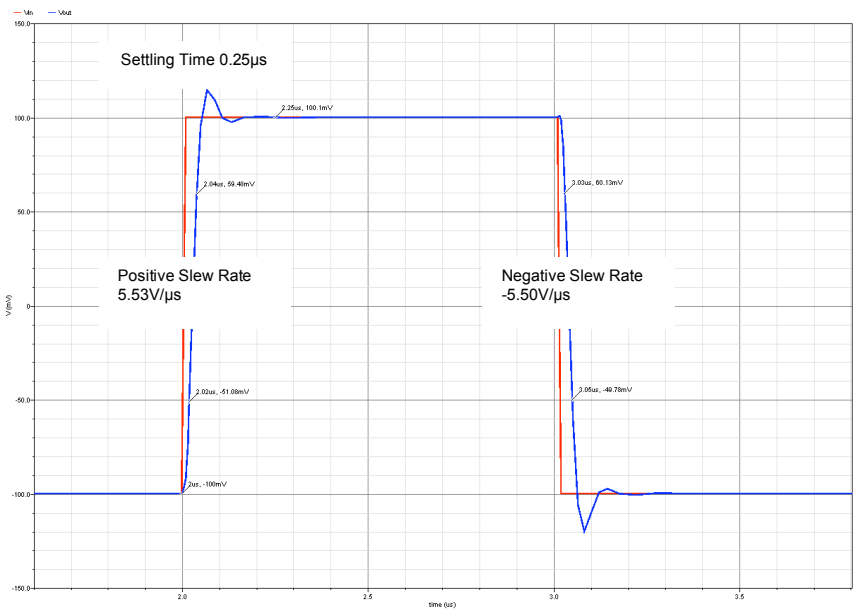

Figure 7 Slew rate simulation result of the schematic

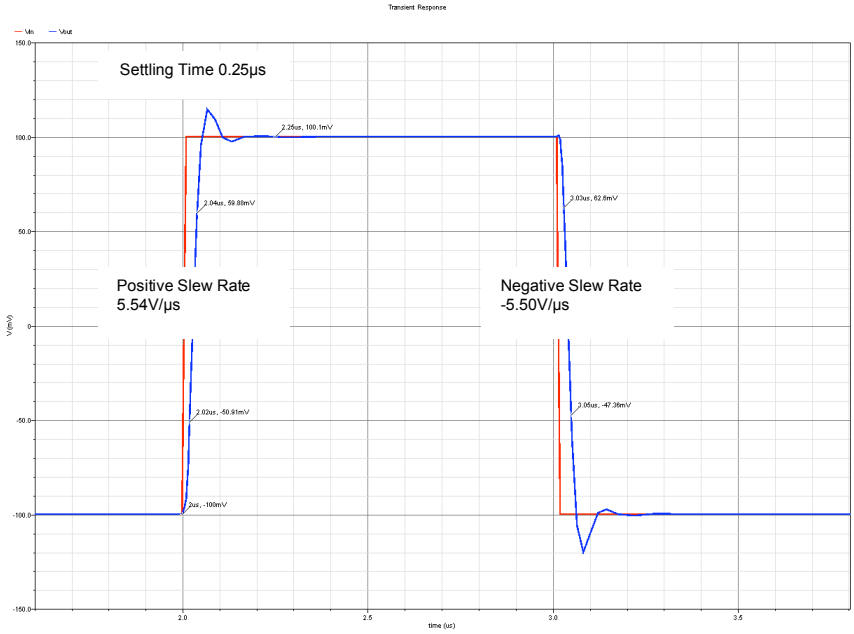

Figure 8 Slew rate simulation result of the extracted layout

Input Common Mode Range (ICMR):

The test-bench configuration for the simulation of input common mode range (ICMR) is shown in figure 9. The lower limit of ICMR is determined by when the transistor M5 is in its saturation region, which is the current in M5 reaches its quiescent state. The ICMR for both schematic and extracted layout simulations (shown in figure 10) is from -1.8V to 3.2V, which has wider range than the proposed specification of ICMR (-1.5 ~ 2.5V).

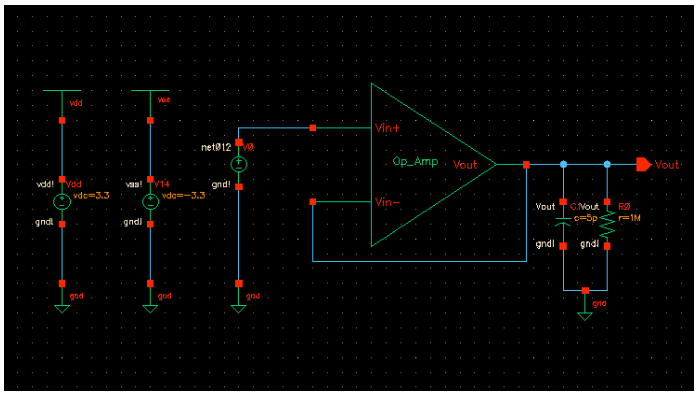

Figure 9 ICMR test-bench

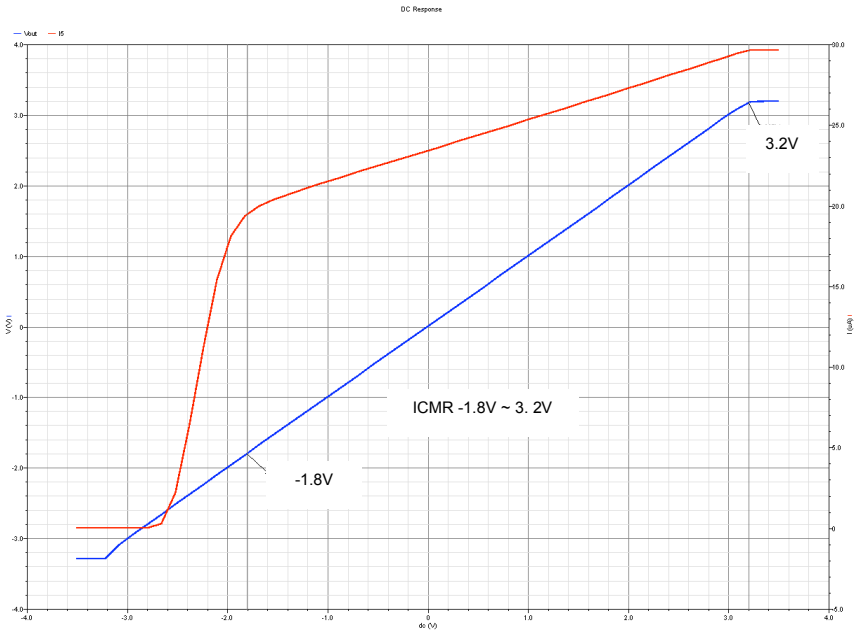

Figure 10 ICMR simulation result

Common Mode Rejection Ratio (CMRR):

The common mode rejection ratio measures how the output changes in response to a change in the common-mode input level. Ideally, the common mode gain of an Op amp is zero. For the test-bench of CMRR simulation, two identical voltage sources designated as V_{cm} are placed in series with both op amp inputs (V_{in}+ and V_{in}-) where the op amp is connected in the unity gain configuration (figure 11). CMRR can be performed through V_{cm} divided by V_{out}. The CMRR simulation result (figure 12) for both schematic and layout is 71.42dB (larger than the proposed specification 60dB).

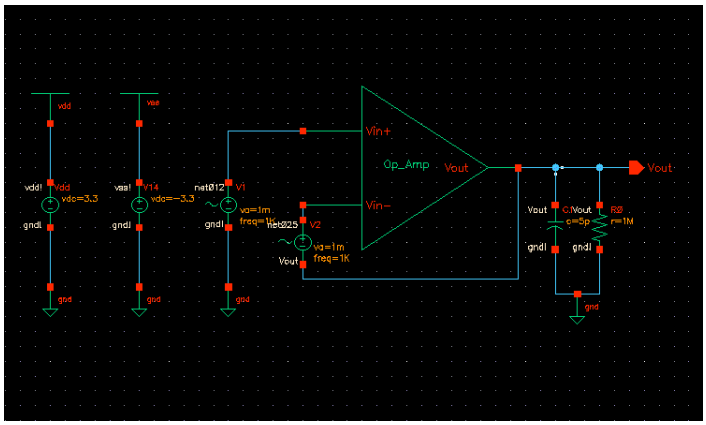

Figure 11 CMRR test-bench

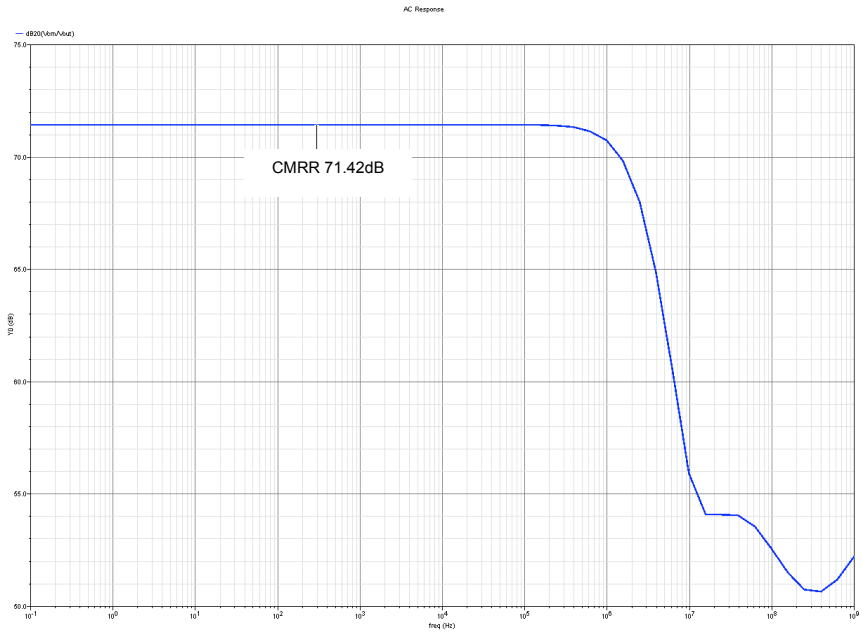

Figure 12 CMRR simulation result

Power Supply Rejection Ratio (PSRR):

A small sinusoidal voltage is placed in series with V_{dd} to measure PSRR+ while V_{ss} for PSRR- (figure 13 and 15). The measurements can be shown by PSRR+ = V_{dd}/V_{out} and PSRR- = V_{ss}/V_{out}. For both schematic and layout simulation results, PSRR+ is 72.88dB while PSRR- is 70.87dB (figure 14 and 16).

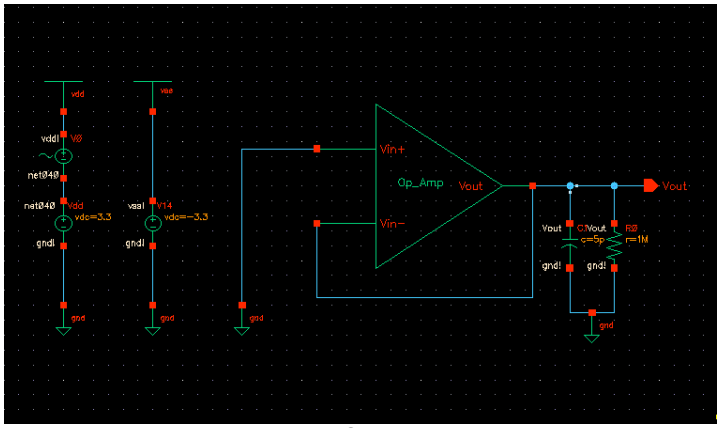

Figure 13 PSRR+ test-bench

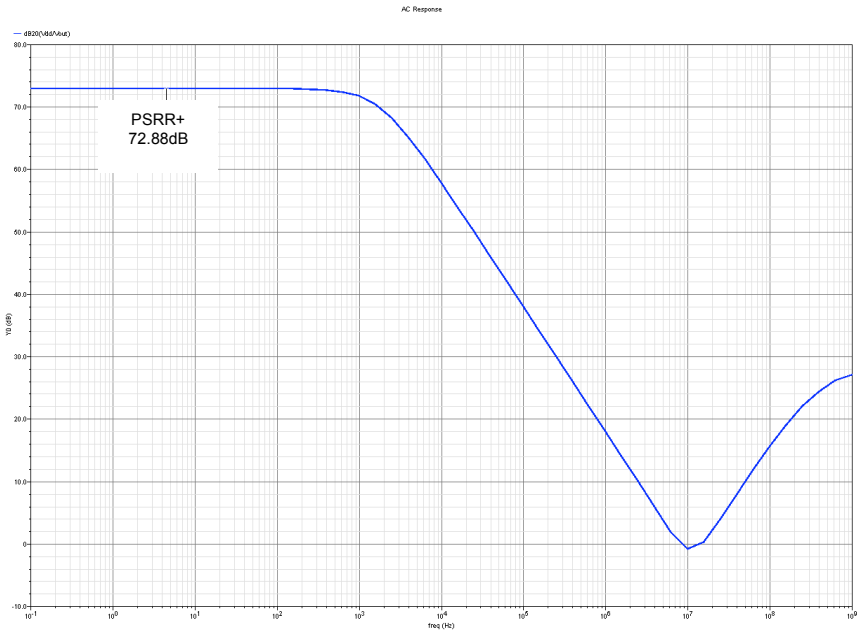

Figure 14 PSRR+ simulation result

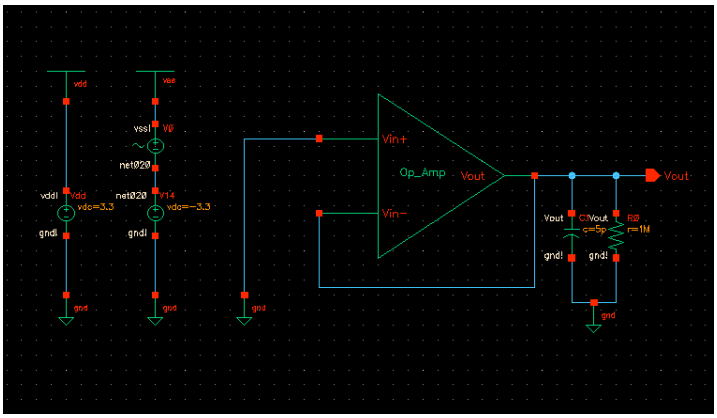

Figure 15 PSRR- test-bench

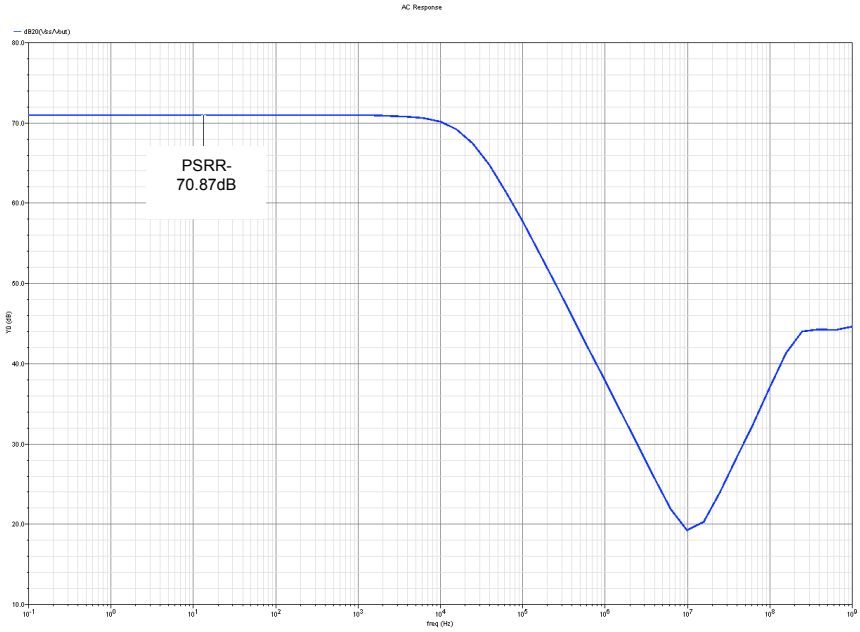

Figure 16 PSRR- simulation result

Output Swing:

The output swing simulation can be obtained by using a configuration of close-loop inverting gain. The linear part of the transfer curve represents output voltage swing of the amplifier. The amount of current flowing in R_L has a strong influence on the output voltage swing. This op amp has better output swing range when the load R_L is above 30kΩ. Also the resistors connected to the op amp input should be large than the load R_L. The simulation is examined by using both DC sweep and transient analysis. The output swing for the op amp here is from -3.29V to 3.27V (wider range than the proposed specification -2.5V ~2.5V).

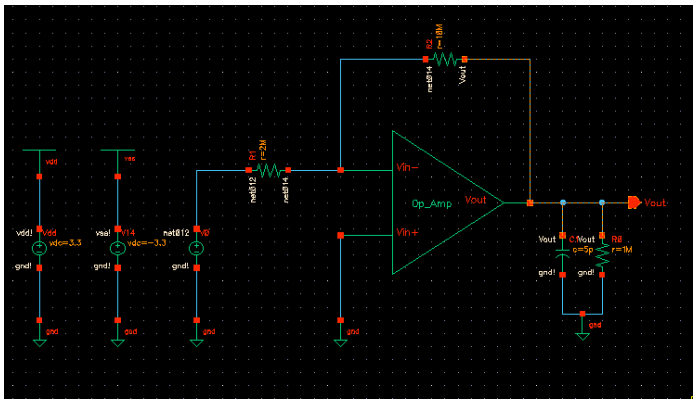

Figure 17 Output swing test-bench

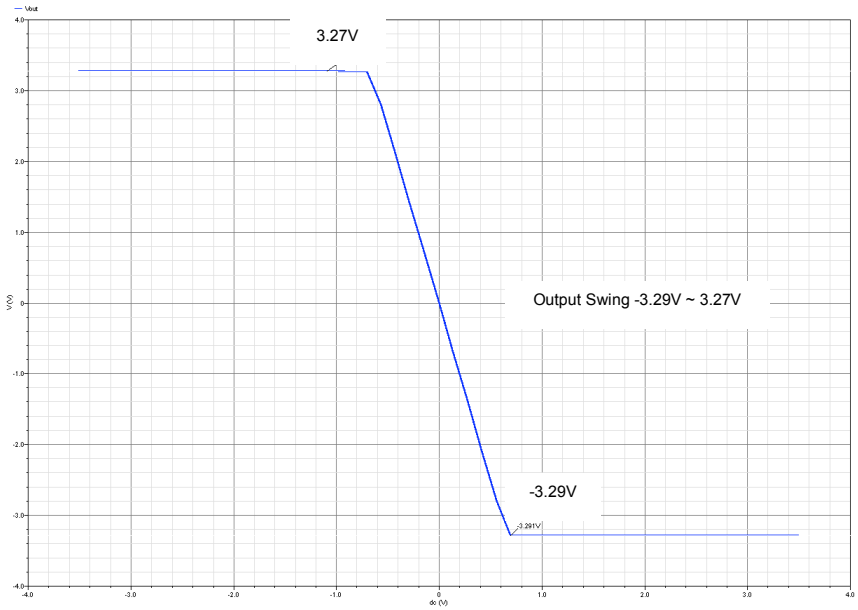

Figure 18 Output swing simulation result (DC sweep)

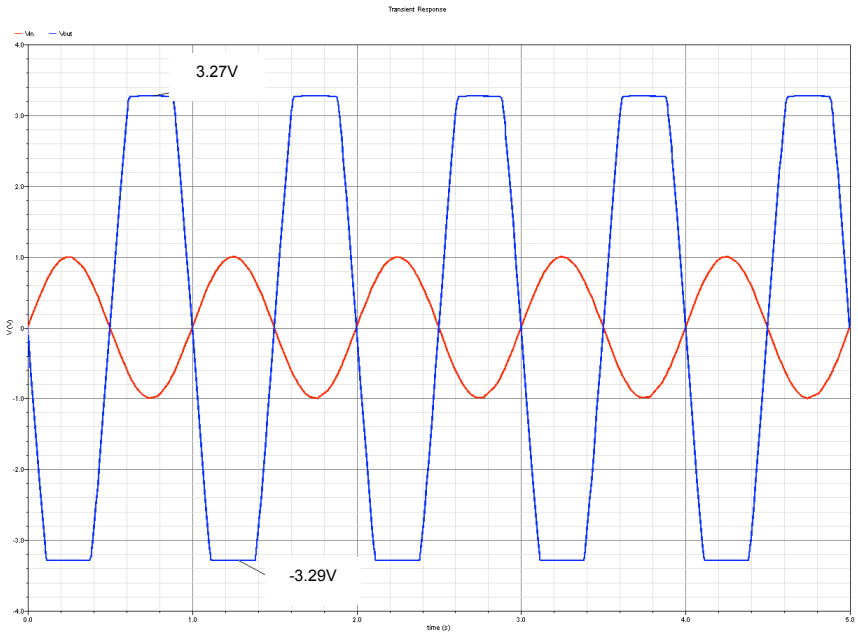

Figure 19 Output swing simulation result (Transient)

Output Resistance:

The simulation of output resistance is approached by using the circuit shown in figure 20. The output voltage characteristics are obtained by simulated the circuit below with and without the load R_L. The voltage drop caused by R_L is used to calculate the output resistance as

$$R_{out} = R_L\,(V_{o1}/V_{o2} - 1)$$

V_{o1}: the output voltage without R_L
V_{o2}: the output voltage with R_L

The simulation result (figure 21) shows that the output resistance for this op amp is 113KkΩ.

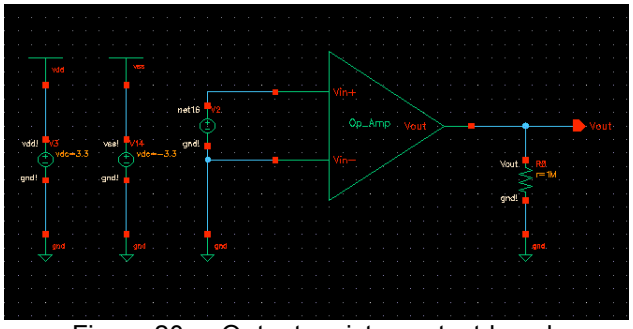

Figure 20 Output resistance test-bench

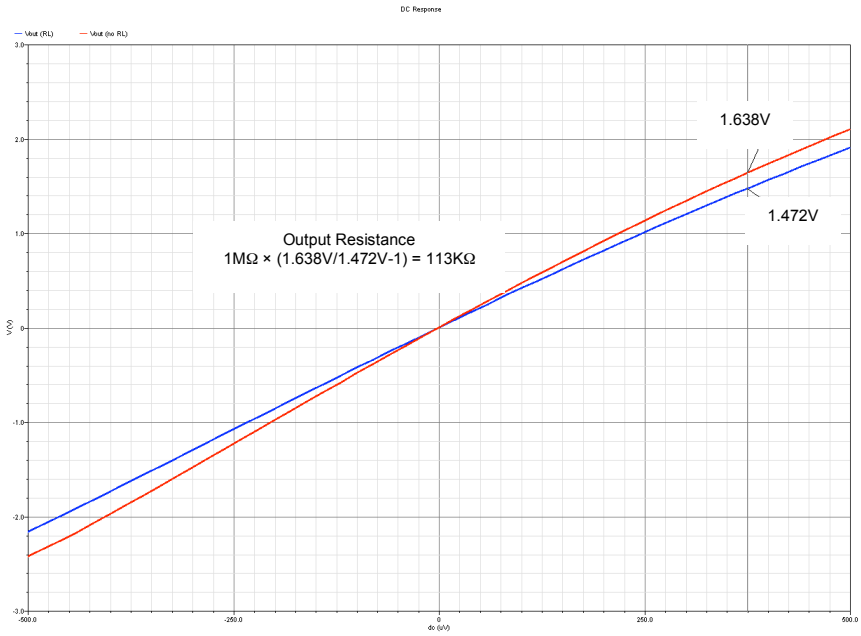

Figure 21 Output resistance simulation result

DC Offset:

The simulation configuration of DC offset is to connect both inputs to the ground. The output voltage result is around -1.367mV, which is much smaller than the proposed offset specification (±10mV).

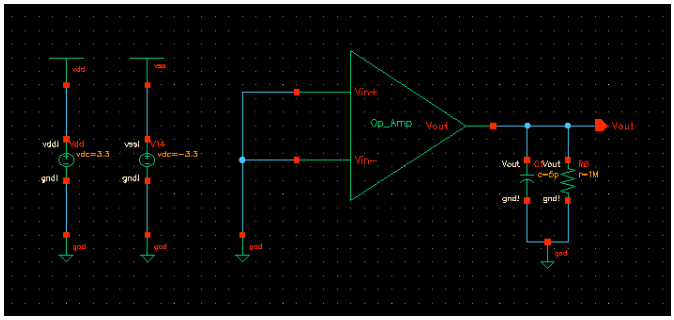

Figure 22 DC offset test-bench

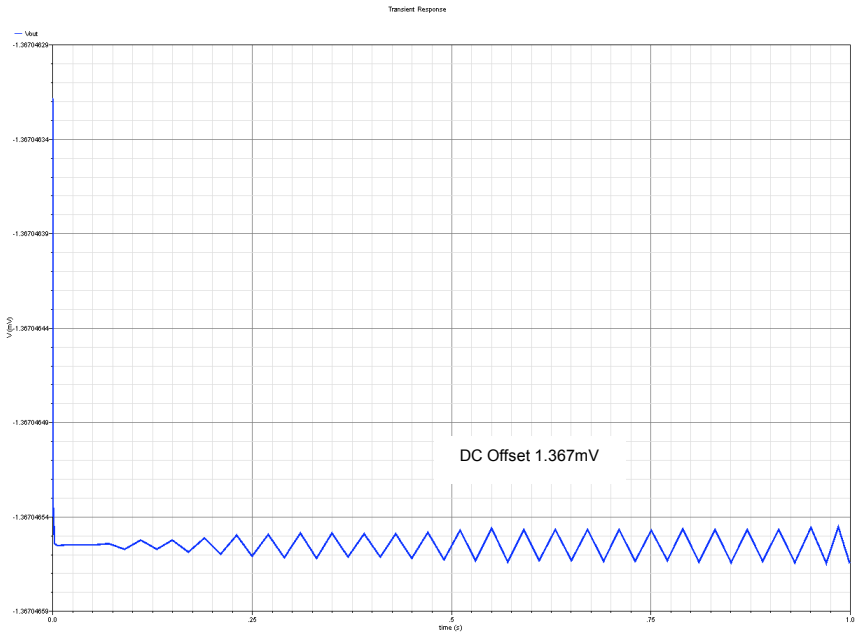

Figure 23 DC offset simulation result

Power Dissipation:

Through DC sweep analysis on the voltage source at the inputs of the op amp, the power dissipation is around 1.19mW for the low DC input with -1.8V and 1.36mW for the high DC input with 3.3V. The DC sweeps from -1.8V to 3.3V due to the ICMR of the op amp.

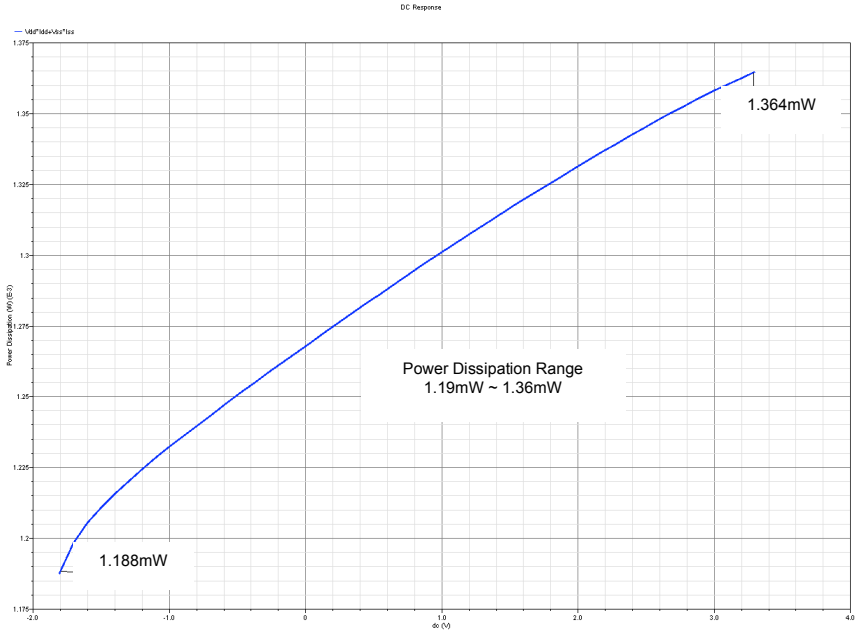

Figure 24 Power dissipation simulation result

Summary:

Overall, the op amp design in this project achieved all of the specification requirements for both schematic and layout simulation results.

Specifications	Proposed Value	Schematic Simulation	Layout Simulation
Gain	≥ 70dB	72.47 dB	72.47 dB
Gain Bandwidth	≥ 5MHz	5.736MHz	5.736MHz
Settling Time	≤1μs	0.25μs	0.25μs
Phase Margin	≥ 45°	59.1°	59.1°
Slew Rate	≥ 5V/μs	positive: 5.53 V/μs negative: -5.50 V/μs	positive: 5.54 V/μs negative: -5.50 V/μs
Input Common Mode Range (ICMR)	-1.5V~2.5V	-1.8V ~ 3.2V	-1.8V ~ 3.2V
Common Mode Rejection Ratio (CMRR)	≥ 60dB	71.42dB	71.42dB
Power Supply Rejection Ratio (PSRR)	≥ 60dB	PSRR+: 72.88dB PSRR-: 70.87dB	PSRR+ :72.88dB PSRR-: 70.87dB
Output Swing	-2.5V ~ 2.5V	-3.29V ~ 3.27V	-3.29V ~ 3.27V
Offset	≤ ±10mV	-1.37mV	-1.37mV
Output Resistance	N/A	113KΩ	113KΩ
Power Dissipation	≤ 2mW	1.19~1.36mW	1.19~1.36mW

Table 4 Comparison of the desired specifications and the schematic and layout simulation results

Layout Design

The layout design of the op amp is shown in the figure 25. The total area is around $105\mu m \times 60.3\mu m = 6331.5\mu m^2$.

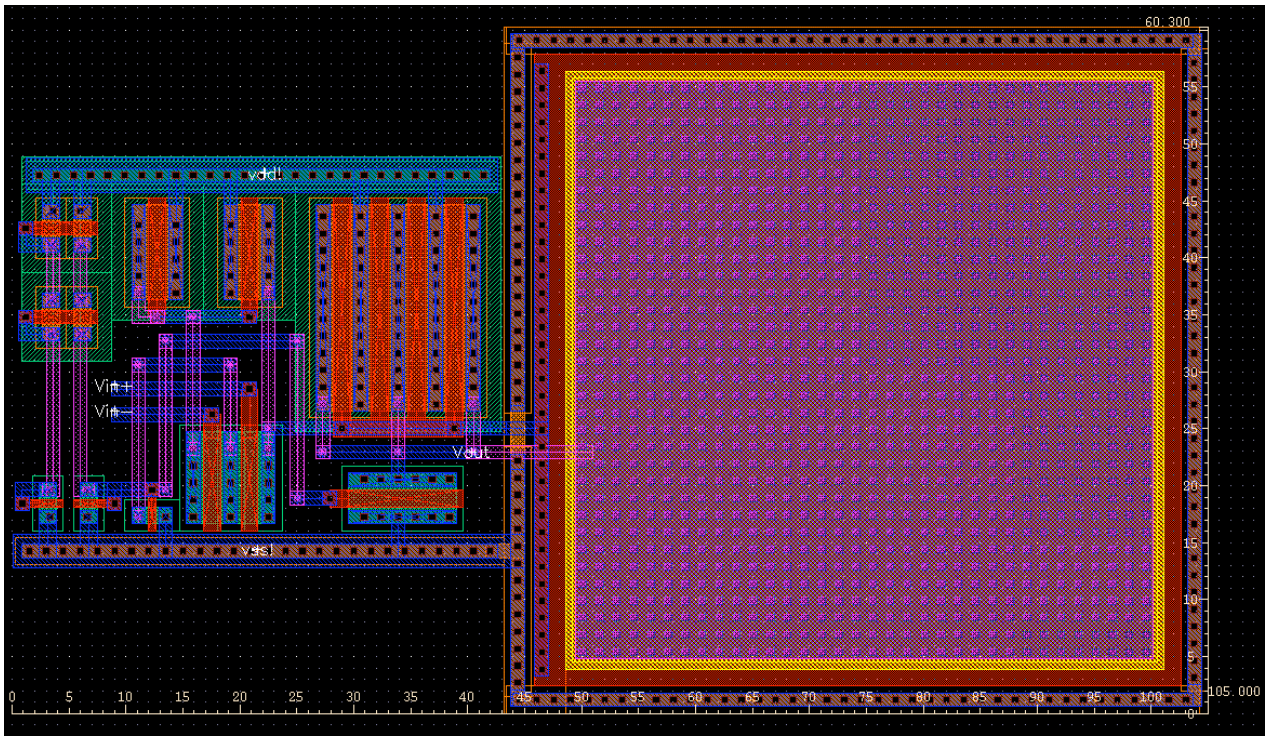

Figure 25 Layout design of the op amp

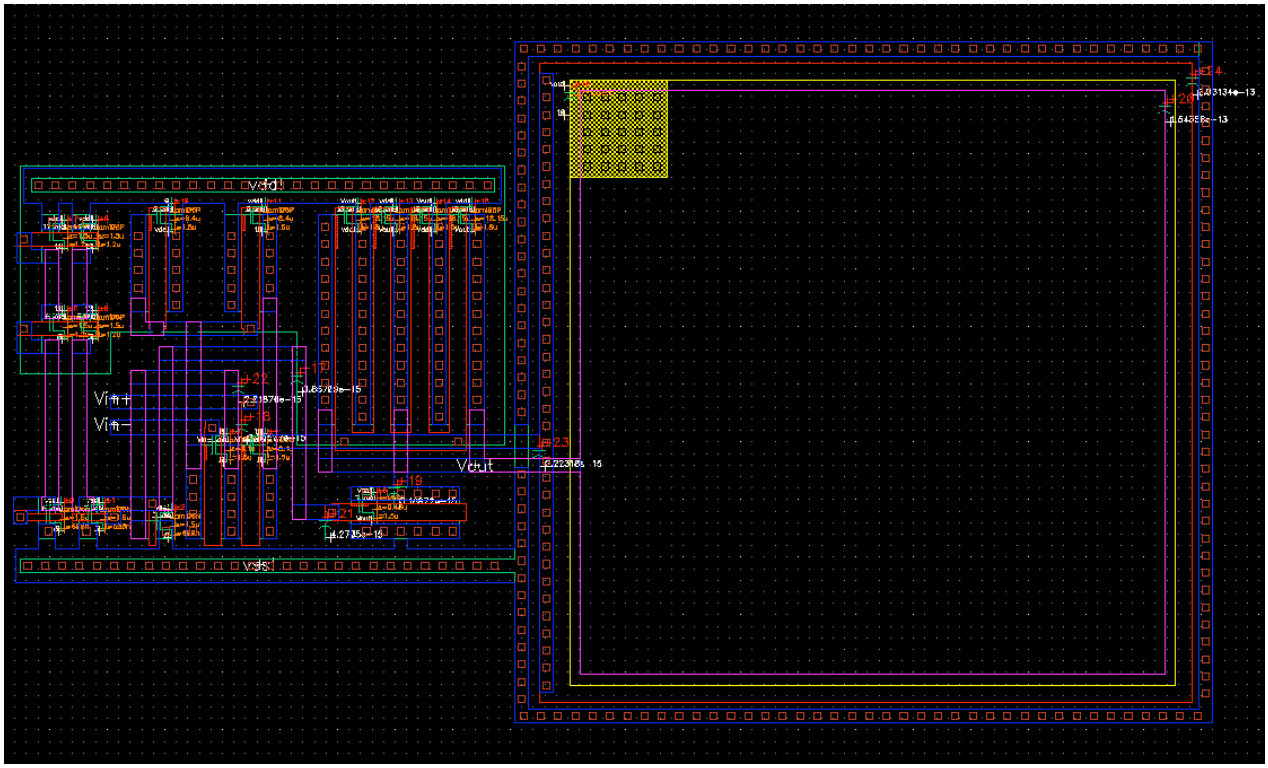

Figure 26 Extracted view with parasitic capacitance of the op amp layout

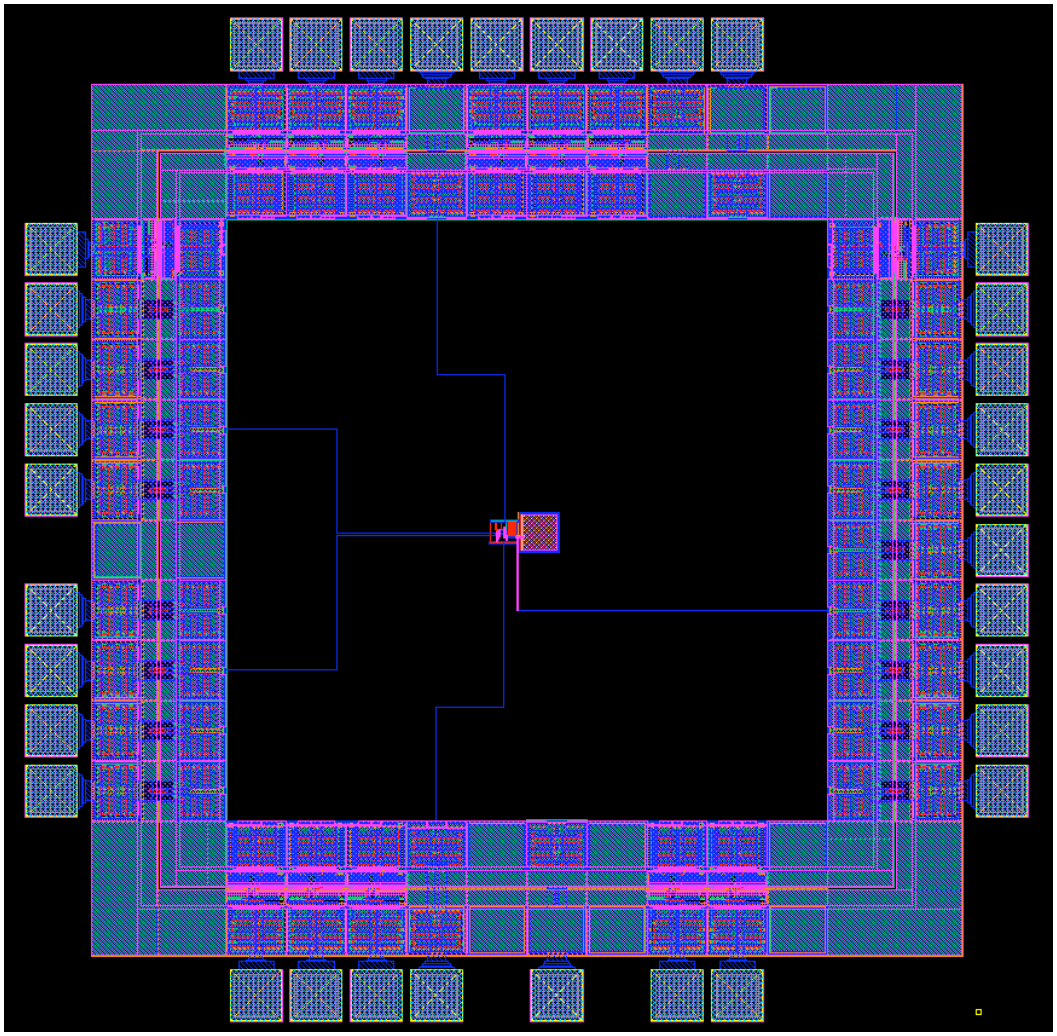

Figure 27 The op amp layout with the outside pad frame

Conclusion

In this project, the hardest part was to match hand calculation to simulation results. The channel length modulation (λ) was actually not considered during hand calculation. However, it had a significant influence on the schematic simulation. Some other factors such as C_{gd}, C_{gs}, V_{th}, etc. also caused the mismatch between calculation and simulation. Therefore, after the simulation, most of the transistors' size still needed to be modified in order to optimize the performance. In fact, both hand calculation and simulation are very important when designing a circuit since hand calculation gives an estimation range for all parameters, and simulation presents the results closer to the real circuit. The parametric analysis was a very useful function that enabled to run different values for different variables at the same time and plotted all different performances. Through many experimental trials, the desired performance of op amp circuit was finally achieved. Even though the parametric analysis helped to save a lot of time for finding out good parameters for each device, it would have been more efficient if the optimization function would have been used.

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Appendix

Layout vs. schematic report:

```
@(#)$CDS: LVS.exe version 5.1.0 07/17/2006 01:47 (cds125839) $
Command line: /apps/cadence2005/ic51/tools/dfII/bin/32bit/LVS.exe -dir
/home/grad/neilppt/ece218/LVS -l -s -x/home/grad/neilppt/ece218/LVS/xref.out -
t /home/grad/neilppt/ece218/LVS/layout /home/grad/neilppt/ece218/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Creating cross reference file /home/grad/neilppt/ece218/LVS/xref.out.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/grad/neilppt/ece218/LVS/layout/netlist
       count
        12        nets
         5        terminals
         1        cap
        10        pmos
         6        nmos

    Net-list summary for /home/grad/neilppt/ece218/LVS/schematic/netlist
       count
        12        nets
         5        terminals
         1        cap
        10        pmos
         6        nmos

    Terminal correspondence points
    N9        N9        Vin+
    N8        N7        Vin-
    N10       N12       Vout
    N0        N0        vdd!
    N4        N1        vss!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        nfet pfet nmos4 pmos4

The net-lists match.
                     layout  schematic
                        instances
      un-matched         0     0
      rewired            0     0
      size errors        0     0
      pruned             0     0
      active            17    17
      total             17    17

                          nets
      un-matched         0     0
      merged             0     0
      pruned             0     0
      active            12    12
      total             12    12
```

```
                    terminals
      un-matched        0     0
      matched but
      different type    0     0
      total             5     5


Probe files from /home/grad/neilppt/ece218/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:


Probe files from /home/grad/neilppt/ece218/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```