

1.0 CMOS OPAMP

1.1. General Opamp Block Diagram

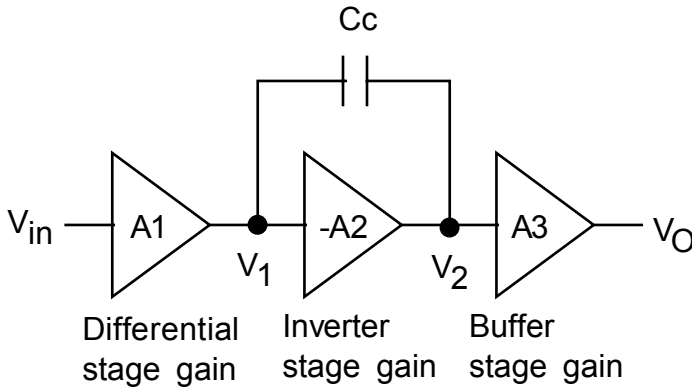


Figure 1. Opamp General Block Diagram

Note the second stage needs to have a negative gain because of the feedback capacitor. With a positive gain an oscillator or unstable system will be implemented instead. The last stage is a buffer to convert the high output impedance of the inverter stage to a low output impedance. This is needed in developing a good opamp. Ideal opamp requires $r_{in} = \infty$ and $r_o = 0$.

Figure 2. The Effect of Compensation Capacitance C_c .

At the input side,

$$\frac{V_1 - V_2}{I_1} = \frac{1}{sC_c}; \quad \frac{V_1 + AV_1}{I_1} = \frac{1}{sC_c}; \quad \frac{V_1(1+A)}{I_1} = \frac{1}{sC_c}; \quad \frac{V_1}{I_1} = \frac{1}{sC_c(1+A)}$$

This is known as the miller capacitance. The feedback capacitance value appears at the input side of the gain stage with a value magnified by $(1+A)$.

At the output side,

$$\frac{V_2 - V_1}{I_2} = \frac{1}{sC_c}; \quad \frac{V_2 + \frac{V_2}{A}}{I_2} = \frac{1}{sC_c}; \quad \frac{V_2(1 + \frac{1}{A})}{I_2} = \frac{1}{sC_c}; \quad \frac{V_2}{I_2} = \frac{1}{sC_c(1 + \frac{1}{A})} = \frac{1}{sC_c}; \quad \text{when } A \gg 1$$

Due to Miller effect, the load of the first stage is effectively the compensation capacitance C_c magnified by $(1+A_2)$

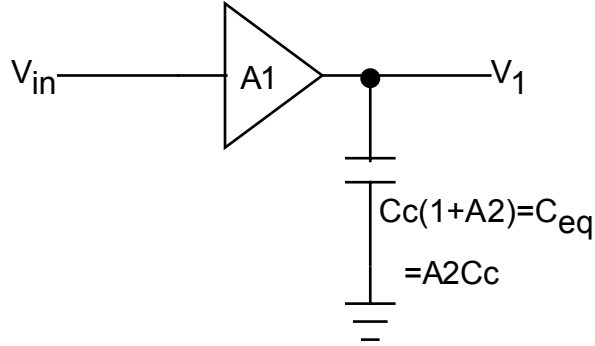


Figure 3. The Miller Capacitance Loading the First Stage.

The gain

$$A_1 = \frac{V_1}{V_{in}} = -g_{m1}Z_{o1} = g_{m2}Z_{o1}$$

where:

$$Z_{o1} \cong r_{ds2} // r_{ds4} // \left(\frac{1}{sC_{eq}} \right) \cong \frac{1}{sC_{eq}} = \frac{1}{s(1+A_2)C_c} \cong \frac{1}{sA_2C_c}$$

The voltage gain of the opamp, assuming the output buffer has unity gain ($A_3=1$),

$$A_v(s) = \frac{V_o}{V_{in}} = A_3A_2A_1 = A_3A_2 \left(\frac{g_{m2}}{sA_2C_c} \right) = A_3 \frac{g_{m2}}{sC_c} = \frac{g_{m2}}{sC_c}$$

The unity gain bandwidth, w_{GB} is the radian frequency when the gain is 1. That is,

$$|A_v(s)| = |A_v(jw_{GB})| = \left| \frac{g_{m2}}{jw_{GB}C_c} \right| = 1$$

Solving for w_{GB} ,

$$w_{GB} = \frac{g_{m2}}{C_c}$$

1.2. Slew Rate Determination

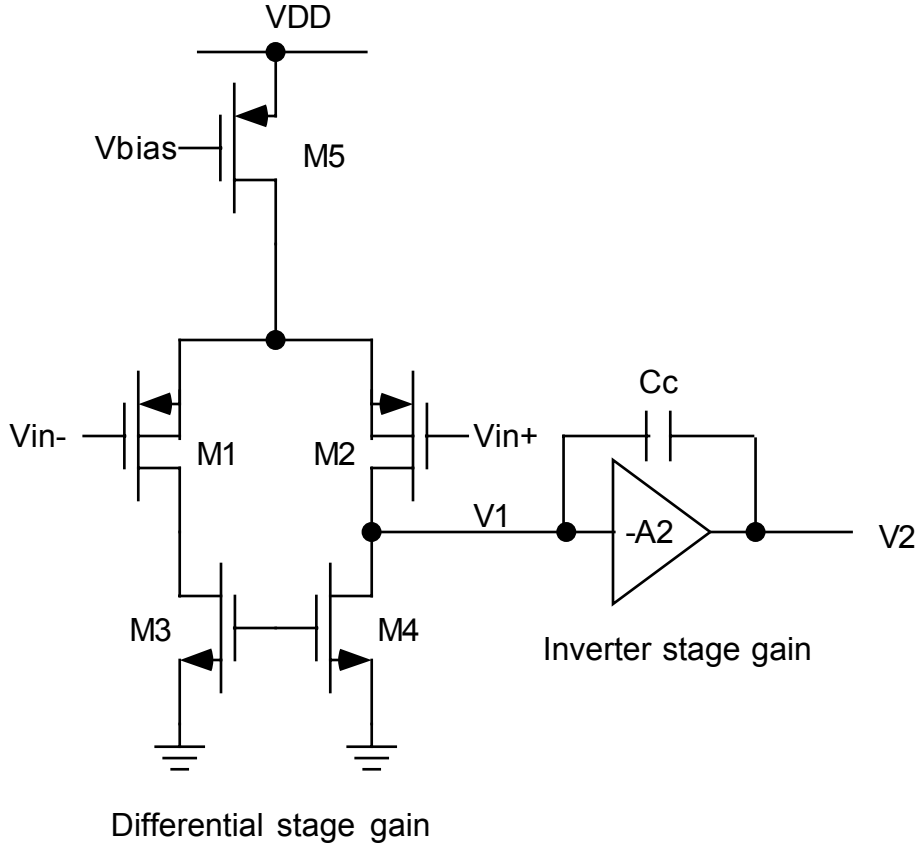


Figure 4. The Differential Gain Stage of the Opamp.

Slew rate is the maximum rate at which the output changes when input signals are large. When $v_{in+} \gg 0$ ($v_{in-} \ll 0$) is large positive (negative), M1 is on and M2 is off. Hence $I_{SD1} = I_{SD5}$, since $I_{SD2} = 0$. The current flows through M3 which is then mirrored to M4, therefore $I_{SD1} = I_{DS3} = I_{DS4} = I_{SD5}$. The current in the compensation capacitor can only flow through M4, since M2 is off and the input impedance of the second stage A2 is ∞ . That is $I_{Cc} = I_{DS4} = I_{SD5}$.

On the other hand, when $v_{in+} \ll 0$ ($v_{in-} \gg 0$) is large negative (positive), M1 is off and M2 is on. Hence, $I_{SD1} = 0$ which flows through M3 and mirrored to M4, therefore $I_{DS3} = I_{DS4} = 0$. That is, current source I_{SD5} flows through M2, then to Cc directly, since M4 is off.

In both cases, the maximum current that flows through Cc is I_{SD5} .
The output voltage of the opamp is approximately equal to v_2 , since $A_3 \approx 1$.

$$SR = \frac{d(V_o)}{dt} = \frac{d\left(\frac{q}{Cc}\right)}{dt} = \frac{I_{SD5}}{Cc} = \frac{2I_{SD1}}{Cc}$$

1.3. OpAmp First Order Model

The objective of compensation is to make the opamp to behave as a single pole in the frequency of interest. That is, at least within the unity gain bandwidth frequency, w_{GB} . The desired transfer function is

$$A_v(s) = \frac{A_{VO}}{1 + \frac{s}{p_1}}$$

where:

A_{VO} is the dc gain of the opamp, and p_1 is the real axis dominant pole.

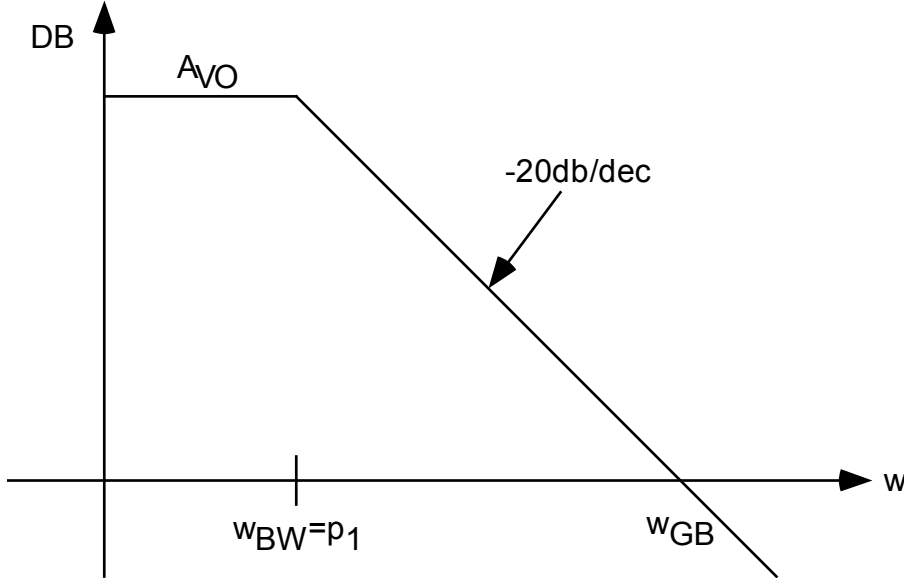


Figure 5. Bode Plot of Opamp First Order Model

The relation between the unity gain bandwidth, w_{GB} , and the dominant pole p_1 can be obtained by the finding the radian frequency when the magnitude of the voltage gain is equal to 1. That is,

$$|A_v(jw_{GB})| = \left| \frac{A_{VO}}{1 + j \frac{w_{GB}}{p_1}} \right| \cong \left| \frac{A_{VO}}{j \frac{w_{GB}}{p_1}} \right| = 1$$

$$w_{GB} \cong A_{VO} p_1$$

At midband frequency, the gain is approximately given by :

$$A_v(s) = \frac{A_{VO}}{1 + \frac{s}{p_1}} \cong \frac{A_{VO}}{\frac{s}{p_1}} = \frac{A_{VO} p_1}{s} = \frac{w_{GB}}{s}$$

1.4. An Opamp with Feedback

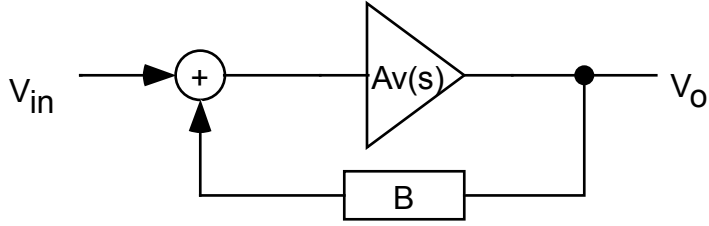


Figure 6. Ideal Feedback Configuration.

$$\begin{aligned} V_O &= A_v V_{in} - \beta A_v V_O \\ V_O (1 + \beta A_v) &= A_v V_{in} \end{aligned}$$

Hence, the closed loop response is given by:

$$A_{CL}(s) = \frac{A_v(s)}{1 + \beta A_v(s)} = \frac{w_{GB}/s}{1 + \beta w_{GB}/s} = \left(\frac{1}{\beta} \right) \frac{1}{1 + \frac{s}{\beta w_{GB}}}$$

where: $(1/\beta)$ is the dc gain of the closed loop system. $LG(s) = \beta A_v(s)$ is the loop gain. The frequency when the closed gain is 3 Db down occurs when the LG becomes unity. That is,

$$|LG(s)| = \left| \beta \frac{w_{GB}}{jw_{-3db}} \right| = 1$$

That is,

$$w_{-3db} = \beta w_{GB} = w_{GB} ; \beta = 1$$

1.5. Settling Time Determination

Opamps are compensated to behave as a simple pole system up to a radian frequency of w_{GB} . This is the case whenever the PM of the Opamp is designed for at least 60° . The settling time is the time needed for the output of the opamp to reach a final value to within a predetermined tolerance. This can be determined using the first order model of the opamp given by:

$$A_v(s) = \frac{A_{vo}}{\left(1 + \frac{s}{p_1}\right)}$$

The unity feedback ($\beta=1$) closed loop gain is given by:

$$\begin{aligned}
A_{CL}(s) &= \frac{A_V(s)}{1 + A_V(s)} = \frac{A_{VO}}{1 + \frac{s}{p_1} + A_{VO}} = \frac{1}{(1 + \frac{1}{A_{VO}}) + \frac{s}{A_{VO}p_1}} \\
&= \frac{\frac{1}{1 + \frac{1}{A_{VO}}}}{1 + \frac{s}{A_{VO}p_1(1 + \frac{1}{A_{VO}})}} \approx \frac{(1 + \frac{1}{A_{VO}})^{-1}}{1 + \frac{s}{A_{VO}p_1}}
\end{aligned}$$

The step response is obtained as follows:

$$V_O(s) = A_{CL}(s)U(s) = \frac{(1 + \frac{1}{A_{VO}})^{-1}}{s(1 + \frac{s}{A_{VO}p_1})}$$

Taking the inverse Laplace Transform, one gets,

$$V_O(t) = (1 + \frac{1}{A_{VO}})^{-1} (1 - e^{-w_{GB}t})u(t)$$

$$V_O(\infty) = (1 + \frac{1}{A_{VO}})^{-1} = 1 - \frac{1}{A_{VO}} = 1 - \varepsilon$$

For large A_{VO} ,

$$V_O(t) = (1 - e^{-w_{GB}t})u(t)$$

$$V_O(t_s) = (1 - e^{-w_{GB}t_s}) \approx V_O(\infty) = 1 - \varepsilon$$

Solve for t_s in term of ε

$$t_s(\varepsilon) = \frac{1}{w_{GB}} \ln\left(\frac{1}{\varepsilon}\right) = \frac{1}{A_{VO}p_1} \ln\left(\frac{1}{\varepsilon}\right) = \tau \ln\left(\frac{1}{\varepsilon}\right)$$

For a step input the output initially slews, then slowly settles toward its final value, determined by the gain bandwidth product.

ε	t_s (settling time)
<1%	$4.6\tau \cong 5\tau$
<.5%	$5.3\tau \cong 6\tau$

1.6. Opamp Second Order Model

For compensation of an Opamp, we need at least a second order model

$$A_v(s) = \frac{A_{VO}}{(1 + s/p_1)(1 + s/p_2)}$$

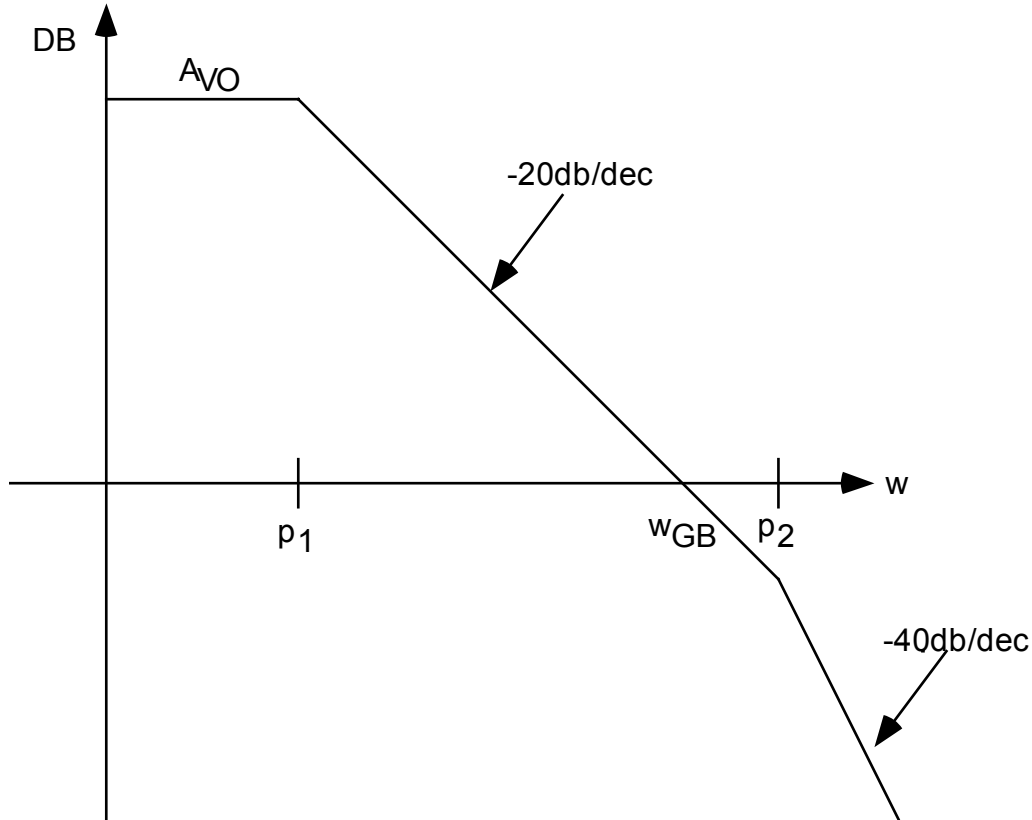


Figure 7. Bode Plot of Opamp Second Order Model.

For frequency $w \gg p_1$, the model reduces to:

$$A_v(s) \cong \frac{A_{VO}}{(s/p_1)(1 + s/p_2)} = \frac{A_{VO}p_1}{s(1 + s/p_2)} = \frac{w_{GB}}{s(1 + s/p_2)}$$

The loop gain for this second order model is given by:

$$LG(s) = \beta A_v(s) = \frac{\beta w_{GB}}{s(1 + s/p_2)}$$

The radian frequency at 3db down is obtained by setting the magnitude of $LG(s)$ to 1.

$$|LG(jw_{-3db})| = \left| \frac{\beta w_{GB}}{jw_{-3db}(1 + jw_{-3db}/p_2)} \right| = 1$$

When $p_2 \gg w_{-3db}$, then

$$w_{GB} = \frac{w_{-3db}}{\beta} \sqrt{1 + (w_{-3db}/p_2)^2} \cong \frac{w_{-3db}}{\beta} = w_{-3db} ; \beta = 1$$

Phase margin is the phase angle between the loop gain phase angle and -180 degree. It is a measure of stability. First let us determine the loop gain phase angle:

$$LG(jw) = \frac{\beta w_{GB}}{(jw)(1 + jw/p_2)}$$

$$\Theta(LG(jw)) = -90^\circ - \tan^{-1}(w/p_2)$$

The phase margin is computed as follows:

$$PM = \Theta(LG(jw_{-3db})) - (-180) = 90^\circ - \tan^{-1}(w_{-3db}/p_2)$$

$$w_{-3db} = p_2 \tan(90^\circ - PM)$$

The closed loop gain is given by:

$$A_{CL}(s) = \frac{Av(s)}{1 + \beta Av(s)} = \frac{A_{CL0}}{1 + \frac{(1/p_1 + 1/p_2)}{1 + \beta A_{VO}}s + \frac{1}{(1 + \beta A_{VO})(p_1 p_2)}s^2}$$

where:

$$A_{CL0} = \frac{A_{VO}}{1 + \beta A_{VO}} \cong \frac{1}{\beta}; \quad A_{VO} \gg 1$$

Comparing with general second order transfer function:

$$H_2(s) = \frac{A_{VO}}{1 + \frac{1}{w_0 Q}s + \frac{1}{(w_0)^2}s^2}$$

where:

w_0 is the resonant frequency, and Q is the Q factor. We obtain,

$$w_0 = \sqrt{(1 + \beta A_{VO})(p_1 p_2)} \cong \sqrt{\beta w_{GB} p_2}$$

$$w_0 Q = \frac{1 + \beta A_{VO}}{(1/p_1 + 1/p_2)}$$

$$Q = \frac{\sqrt{(1 + \beta A_{VO})/(p_1 p_2)}}{(1/p_1 + 1/p_2)} = \frac{\sqrt{(1 + \beta A_{VO})(p_1 p_2)}}{(p_1 + p_2)}$$

$$= \frac{\sqrt{(1 + \beta A_{VO})p_1}}{(\frac{p_1}{\sqrt{p_2}} + \sqrt{p_2})} \cong \sqrt{\frac{\beta A_{VO} p_1}{p_2}} = \sqrt{\frac{\beta w_{GB}}{p_2}}$$

The step response overshoot is a function of Q,

$$\%overshoot = 100e^{\frac{-\pi}{\sqrt{4Q^2-1}}}$$

That is, when Q=0.5 there is no overshoot (%overshoot=0). In addition,

$$w_0 = w_{-3db} \text{ and } PM \approx 65^\circ$$

PM	w_{p2}/w_{GB}	Q	%overshoot
55°	1.4285	0.925	13.3%
60°	1.733	0.817	8.7%
65°	2.1459	0.717	4.7%
70°	2.748	0.622	1.4%
75°	3.733	0.527	0.008%

For no overshoot, select PM=75°. Note that Q is proportional to β . That is the worst case PM occurs when $\beta=1$. Thus for opamp compensation where $0 < \beta(s) \leq 1$ is frequency dependent, if the opamp is compensated for $\beta=1$, it is guaranteed to be stable for all other β .

1.7. Small Signal Equivalent Circuit

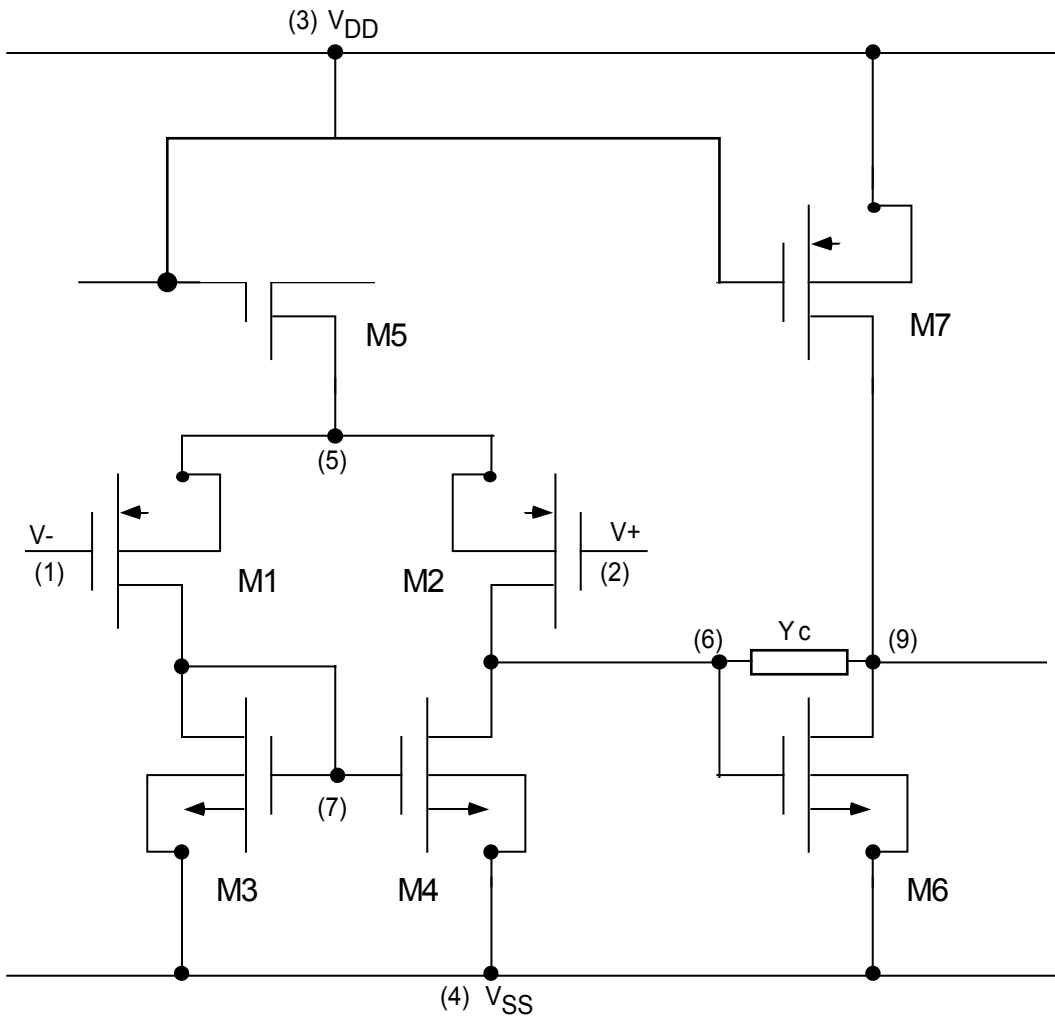


Figure 8a. Schematic Diagram of Unbuffered Opamp Circuit.

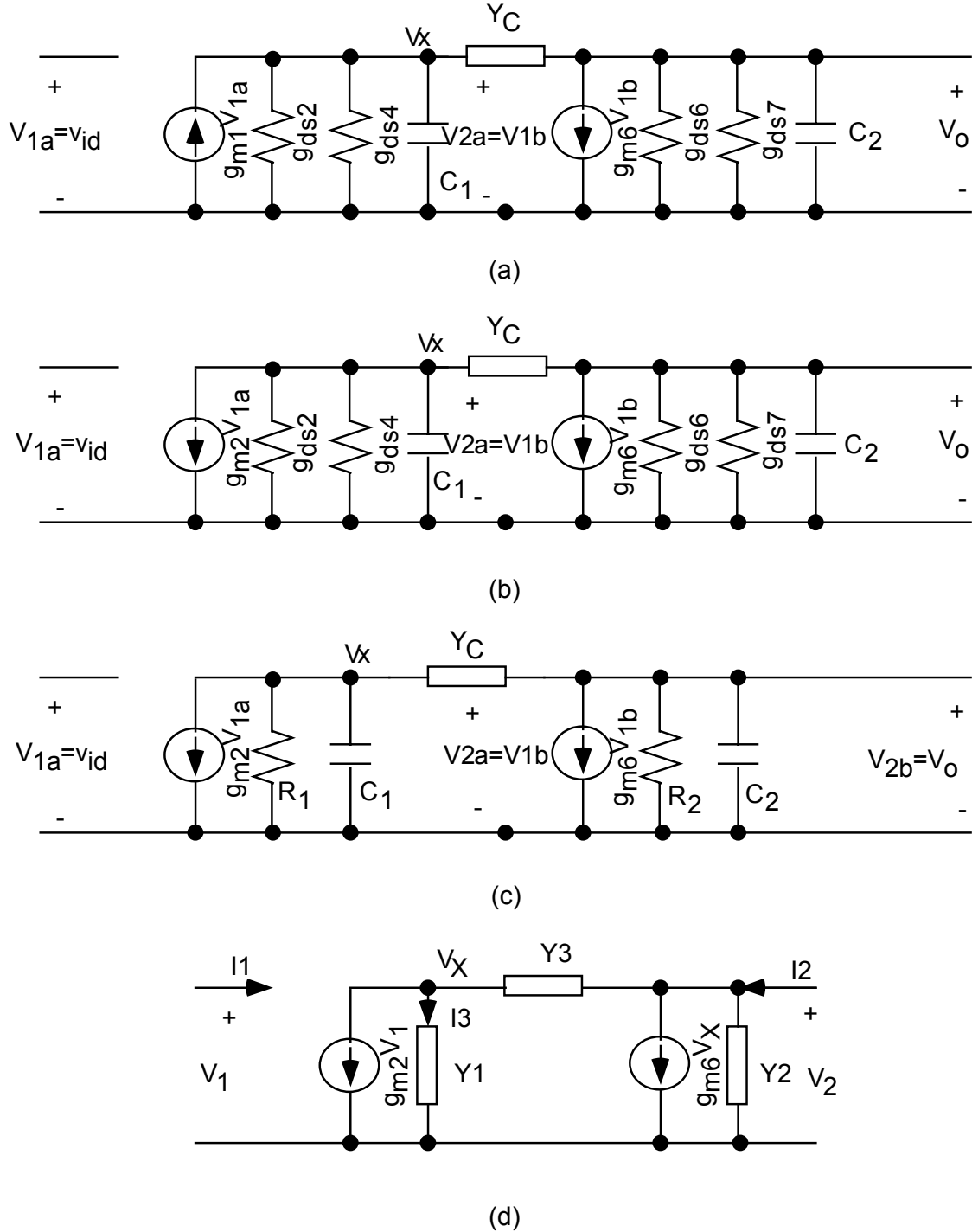


Figure 8. Opamp Small Signal Equivalent Circuit of the First Two Stages.

In Figure 8(a) each amplifier stage is replaced by its equivalent circuit. C_1 and C_2 are the parasitic capacitances of the Opamp at node 6 and 9 respectively. The second stage of an opamp is an inverter stage. The overall gain of the opamp can be made positive, by switching the positive and negative inputs of the differential gain stage. That is the positive input is now the gate of M2. Figure 8(b) shows this by reversing the polarity of the first controlled current source and replacing g_{m1} by g_{m2} to indicate M2 gate is the positive input. Figure 8(c) simplifies the equivalent circuit by combining the resistances and capacitances. That is,

$$R_1 = \frac{1}{g_{ds2} + g_{ds4}} = \frac{1}{(\lambda_2 + \lambda_4)I_{SD2}}$$

$$R_2 = \frac{1}{g_{ds6} + g_{ds7}} = \frac{1}{(\lambda_6 + \lambda_7)I_{DS6}}$$

From Figure 8(c), the port current equations are derived to obtain the Y parameters:

$$I_1 = 0$$

$$I_2 = g_{m6}V_x + Y_2V_2 + Y_3(V_2 - V_x) = (Y_2 + Y_3)V_2 + (g_{m6} - Y_3)V_x$$

At node V_x

$$I_3 + g_{m2}V_1 + Y_3(V_x - V_2) = 0$$

$$I_3 = Y_1V_x$$

Substitute I_3 and solve for V_x ,

$$Y_1V_x + g_{m2}V_1 + Y_3(V_x - V_2) = 0$$

$$(Y_1 + Y_3)V_x + g_{m2}V_1 - Y_3V_2 = 0$$

$$V_x = -\frac{g_{m2}}{Y_1 + Y_3}V_1 + \frac{Y_3}{Y_1 + Y_3}V_2$$

Substituting V_x to I_2

$$I_2 = (Y_2 + Y_3)V_2 + (g_{m6} - Y_3)\left[-\frac{g_{m2}}{Y_1 + Y_3}V_1 + \frac{Y_3}{Y_1 + Y_3}V_2\right]$$

$$= \frac{(Y_3 - g_{m6})g_{m2}}{Y_1 + Y_3}V_1 + \frac{Y_1Y_2 + Y_1Y_3 + Y_2Y_3 + g_{m6}Y_3}{Y_1 + Y_3}V_2$$

The resulting Y-parameter matrix is

$$Y = \begin{bmatrix} 0 & 0 \\ \frac{(Y_3 - g_{m6})g_{m2}}{Y_1 + Y_3} & \frac{\Delta + g_{m6}Y_3}{Y_1 + Y_3} \end{bmatrix}$$

where $\Delta = Y_1Y_2 + Y_1Y_3 + Y_2Y_3$

The voltage gain is

$$A_v = \frac{V_2}{V_1} = \frac{-y_{21}}{y_{22} + Y_L} = \frac{(g_{m6} - Y_3)g_{m2}}{\Delta + g_{m6}Y_3}$$

Case1: $Y_3 = 0$, or $C_c = 0$

$$Y_1 = G_1 + sC_1$$

$$Y_2 = G_2 + sC_2$$

$$\Delta = Y_1 Y_2$$

Solving for the voltage gain,

$$A_v = \frac{V_2}{V_1} = \frac{-y_{21}}{y_{22} + Y_L} = \frac{(g_{m6} - Y_3)g_{m2}}{\Delta + g_{m6} Y_3} = \frac{g_{m2}g_{m6}}{Y_1 Y_2} = \frac{g_{m2}g_{m6}}{(G_1 + sC_1)(G_2 + sC_2)} = \frac{g_{m2}g_{m6}}{G_1 G_2 (1 + sR_1 C_1)(1 + sR_2 C_2)}$$

$$A_v = \frac{g_{m1}g_{m2}R_1 R_2}{(1 + R_1 C_1 s)(1 + R_2 C_2 s)} = \frac{A_{v0}}{(1 - \frac{s}{p_1})(1 - \frac{s}{p_2})}$$

where:

$$A_{v0} = g_{m1}g_{m2}R_1 R_2$$

$$p_1 = \frac{-1}{R_1 C_1}$$

$$p_2 = \frac{-1}{R_2 C_2}$$

Case2: $Y_3 = sC_3 = sC_c$

$$\Delta = Y_1 Y_2 + Y_1 Y_3 + Y_2 Y_3 = (G_1 + sC_1)(G_2 + sC_2) + (G_1 + sC_1)(sC_3) + (G_2 + sC_2)(sC_3)$$

$$= G_1 G_2 + [G_1(C_2 + C_3) + G_2(C_1 + C_3)]s + \Delta_C s^2$$

$$\text{where } \Delta_C = C_1 C_2 + C_2 C_3 + C_1 C_3$$

Solving for the voltage gain,

$$\begin{aligned} A_v &= \frac{(g_{m6} - Y_3)g_{m2}}{\Delta + g_{m6} Y_3} = \frac{(g_{m6} - sC_3)g_{m2}}{G_1 G_2 + [G_1(C_2 + C_3) + G_2(C_1 + C_3)]s + \Delta_C s^2 + sg_{m6} C_3} \\ &= \frac{g_{m2}g_{m6}R_1 R_2 (1 - s\frac{C_3}{g_{m6}})}{1 + s[(C_2 + C_3)R_2 + (C_1 + C_3)R_1 + g_{m6}R_1 R_2 C_3] + s^2 R_1 R_2 \Delta_C} \end{aligned}$$

Compare the denominator with,

$$D(s) = (1 - \frac{s}{p_1})(1 - \frac{s}{p_2}) = 1 - s(\frac{1}{p_1} + \frac{1}{p_2}) + s^2 \frac{1}{p_1 p_2} \cong 1 - s\frac{1}{p_1} + s^2 \frac{1}{p_1 p_2}$$

$$p_1 \cong \frac{-1}{(C_2 + C_C)R_2 + (C_1 + C_C)R_1 + g_{m6}R_1R_2C_C} \cong \frac{-1}{g_{m6}R_1R_2C_C}$$

$$p_2 \cong \frac{-g_{m6}C_C}{C_1C_2 + C_2C_C + C_1C_C} = \frac{-g_{m6}}{C_2} = \frac{-g_{m6}}{C_L}; C_2 \gg C_1 \quad C_C \gg C_1 \quad C_2 \approx C_L$$

$$z_1 = \frac{g_{m6}}{C_C}$$

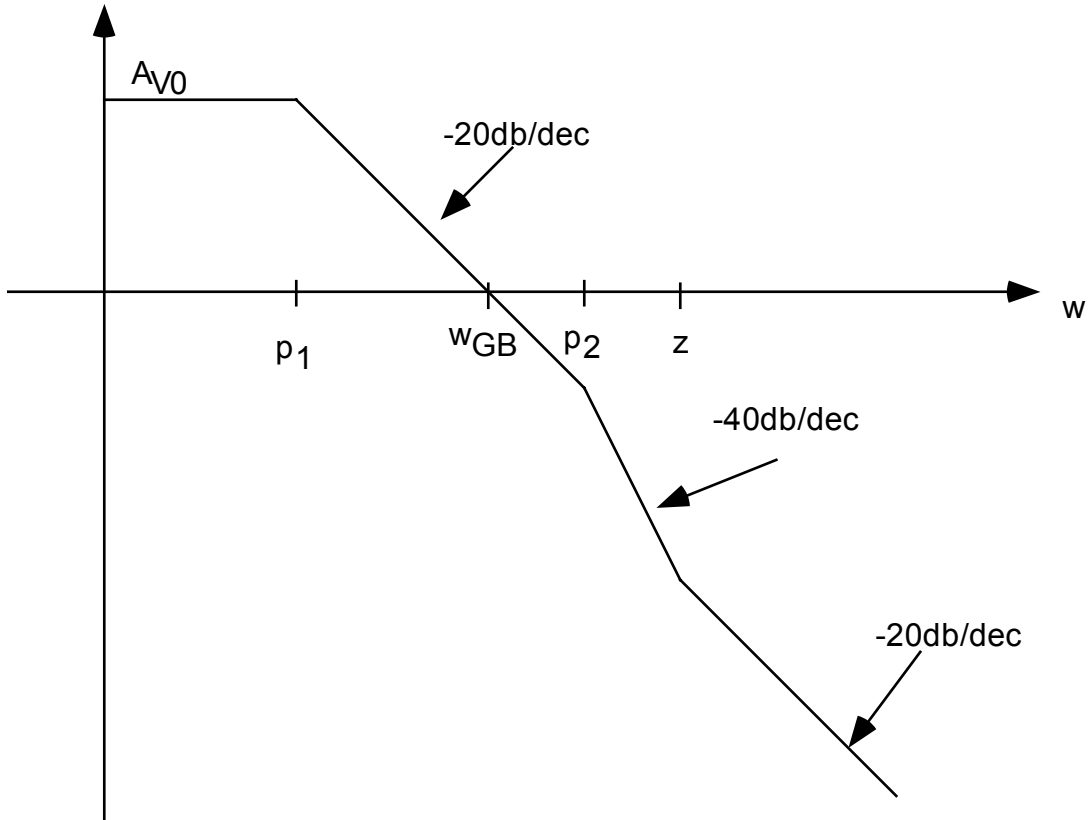


Figure 9. Bode Plot of Second Order System with RHP zero

For good stability a phase margin of at least 60° is desirable This can be achieved as follows:

$$w_{GB} = A_{v0}p_1; A_{v0} \approx \infty$$

$$z \geq 10w_{GB}$$

Then

$$p_2 = 2.2w_{GB}$$

or

$$g_{m6} = 2.2 \frac{C_L}{C_C} g_{m2}$$

This is shown below:

That is, the transfer function has two poles and one RHP zero. The RHP zero contributes a negative phase angle.

$$A_v(s) = \frac{A_{v0}(1 - \frac{s}{z})}{(1 + \frac{s}{p_1})(1 + \frac{s}{p_2})}$$

The phase angle at the unity gain radian frequency (w_{GB}) is

$$\angle A_v(w_{GB}) = -\tan^{-1}(w_{GB}/z) - \tan^{-1}(w_{GB}/p_1) - \tan^{-1}(w_{GB}/p_2)$$

The phase margin PM is given by:

$$PM = 180 + \angle A_v(w_{GB}) = 180 + [-\tan^{-1}(w_{GB}/z) - \tan^{-1}(w_{GB}/p_1) - \tan^{-1}(w_{GB}/p_2)] =$$

$$60^\circ = 180 + [-\tan^{-1}(0.1) - \tan^{-1}(A_{v0}) - \tan^{-1}(w_{GB}/p_2)] \approx 180 + [-5.7^\circ - 90^\circ - \tan^{-1}(w_{GB}/p_2)]$$

$$\tan^{-1}(w_{GB}/p_2) = 24.3^\circ$$

$$p_2 = 2.2w_{GB}$$

$$\frac{g_{m6}}{C_L} = 2.2 \frac{g_{m2}}{C_C}$$

$$g_{m6} = 2.2 \frac{C_L}{C_C} g_{m2}$$

To achieve the assumption $z=10w_{GB}$, the compensation capacitance C_c must be selected properly.

$$z = 10w_{GB}; \frac{g_{m6}}{C_C} = 10 \frac{g_{m2}}{C_C} \Rightarrow g_{m6} = 10g_{m2}$$

$$p_2 > 2.2w_{GB}; \frac{g_{m6}}{C_L} > 2.2 \frac{g_{m2}}{C_C} \Rightarrow g_{m6} > 2.2 \frac{C_L}{C_C} g_{m2}$$

Combining

$$C_C \geq 0.22C_L$$

$$\text{In addition, } p_2 < z \Rightarrow \frac{g_{m6}}{C_L} < \frac{g_{m6}}{C_C} \Rightarrow C_C < C_L. \text{ Hence,}$$

$$0.22C_L < C_C < C_L$$

$$\text{Case 3: } Z_3 = R_3 + \frac{1}{sC_3} = \frac{1}{G_3} + \frac{1}{sC_3} = \frac{1}{G_C} + \frac{1}{sC_C}; Y_3 = \frac{sG_3C_3}{G_3 + sC_3}$$

$$\begin{aligned}
\Delta &= Y_1 Y_2 + Y_1 Y_3 + Y_2 Y_3 \\
&= (G_1 + sC_1)(G_2 + sC_2) + (G_1 + sC_1) \left(\frac{sG_3 C_3}{G_3 + sC_3} \right) + (G_2 + sC_2) \left(\frac{sG_3 C_3}{G_3 + sC_3} \right) \\
&= \frac{G_1 G_2 G_3 + (\Delta_G C_3 + G_1 G_3 C_2 + G_2 G_3 C_1)s + (G\Delta_C + G_2 C_1 C_3 + G_1 C_2 C_3)s^2 + C_1 C_2 C_3 s^3}{G_3 + sC_3}
\end{aligned}$$

where :

$$\Delta_G = G_1 G_2 + G_1 G_3 + G_2 G_3$$

$$\Delta_C = C_1 C_2 + C_1 C_3 + C_2 C_3$$

$$\begin{aligned}
A_V &= \frac{(g_{m6} - Y_3)g_{m1}}{\Delta + g_{m6} Y_3} = \frac{(g_{m6} - \frac{sG_3 C_3}{G_3 + sC_3})g_{m1}}{\Delta + g_{m6} \frac{sG_3 C_3}{G_3 + sC_3}} \\
&= \frac{[g_{m6} G_3 + (g_{m6} C_3 - G_3 C_3)s]g_{m1}}{G_1 G_2 G_3 + (\Delta_G C_3 + G_1 G_3 C_2 + G_2 G_3 C_1 + g_{m6} G_3 C_3)s + (G\Delta_C + G_2 C_1 C_3 + G_1 C_2 C_3)s^2 + C_1 C_2 C_3 s^3} \\
&= \frac{g_{m1} g_{m6} G_3 \left[1 + \frac{g_{m6} C_3 - G_3 C_3}{g_{m6} G_3} s \right]}{G_1 G_2 G_3 \{1 + cs + bs^2 + as^3\}}
\end{aligned}$$

where :

$$c = [(R_1 + R_2 + R_3)C_3 + R_2 C_2 + R_1 C_1 + g_{m6} R_1 R_2 C_3]$$

$$b = [R_1 R_2 \Delta_C + R_1 R_3 C_1 C_3 + R_2 R_3 C_2 C_3]$$

$$a = R_1 R_2 R_3 C_1 C_2 C_3$$

$$A_V = \frac{g_{m1} g_{m6} R_3 \left[1 + \left(R_3 C_3 - \frac{C_3}{g_{m6}} \right) s \right]}{1 + c's + b's^2 + a's^3}$$

where :

$$c' = [(C_2 + C_3)R_2 + (C_1 + C_3)R_1 + g_{m6} R_1 R_2 C_3 + R_3 C_3]$$

$$b' = R_1 R_2 \Delta_C + R_1 R_3 C_1 C_3 + R_2 R_3 C_2 C_3$$

$$a' = R_1 R_2 R_3 C_1 C_2 C_3$$

2.0Opamp Design Specification

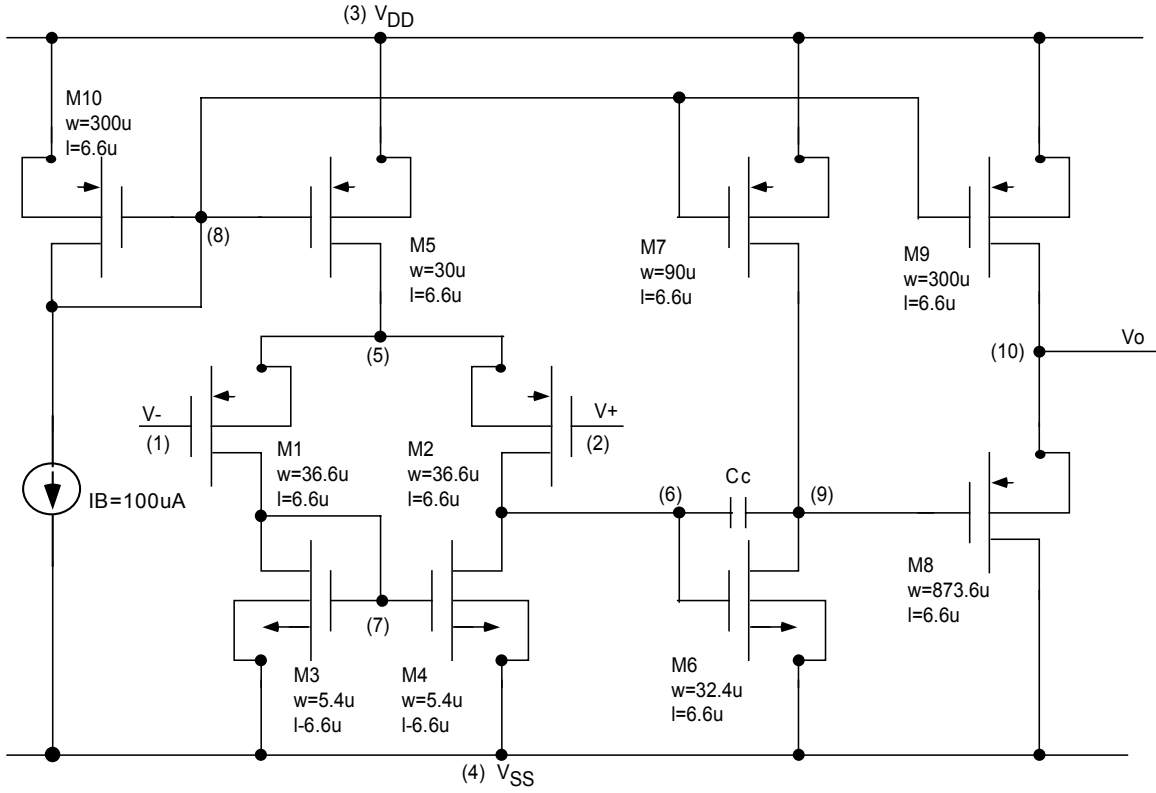


Figure 10

$V_{DD} = +5V$, $V_{SS} = -5V$, $A_o \geq 15,000$, $GB = 2\pi(5MHz)$, $SR = 10V/\mu s$, $R_o \leq 1.46k$
 $-4.5 \leq CMR \leq 3$, $PM > 60^\circ$

SPICE Parameters: $K_n = 40\mu A/V^2$, $K_p = 15\mu A/V^2$, $\lambda = 0.02$

(1) Determine I_{D5} from the SR specification.

Let $C_c = 1pF$

$$SR = \frac{I_{SD5}}{C_c}$$

$$I_{SD5} = (SR)(C_c) = (10E-6)(1E-12) = 10\mu A$$

$$V_{SD5(SAT)} = V_{SG5} - |V_{TP0}| = V_{DD} - V_{bias} - |V_{TP0}| = 5 - 3.5 - |-1| = 0.5$$

$$\left(\frac{W}{L}\right)_5 = \frac{2I_{SD5}}{K_p V_{SD5(SAT)}^2} = \frac{2(10E-6)}{(15E-6)(0.5)^2} = 5.333$$

$$I_{SD1} = I_{SD2} = \frac{I_{SD5}}{2} = \frac{10\mu A}{2} = 5\mu A$$

(2) Determine $(W/L)_1$ from the w_{GB} and positive CMR specifications

From w_{GB} specification,

$$w_{GB} = \frac{g_{m1}}{C_C} = \frac{1}{C_C} \sqrt{2K_p (W/L)_1 I_{SD1}}$$

$$g_{m1} = C_C w_{GB} = (1E-12)(2\pi 5E6) = 31.4 \mu mho$$

$$\left(\frac{W}{L}\right)_1 = \frac{(g_{m1})^2}{2K_p I_{SD1}} = \frac{[31.4E-6]^2}{2(15E-6)(5E-6)} = 6.57$$

From the positive CMR specification,

$$V_{G1(max)} = V_{DD} - V_{SD5(SAT)} - V_{SG1}$$

$$V_{SG1} = V_{DD} - V_{SD5(SAT)} - V_{G1(max)}$$

From the gate bias, V_{bias} , V_{SD5} can be determined.

$$V_{SG1} = V_{DD} - V_{SD5(SAT)} - V_{G1(max)} = 5 - 0.5 - 3 = 1.5$$

$$V_{SD1(SAT)} = V_{SG1} - |V_{TP0}| = 1.5 - |-1| = 0.5$$

$$\left(\frac{W}{L}\right)_1 = \frac{2I_{SD1}}{K_p V_{SD1(SAT)}^2} = \frac{2(5E-6)}{(15E-6)(0.5)^2} = 2.666$$

To satisfy both specifications select the higher (W/L) ratio. For matching and symmetry, we also choose $(W/L)_2 = (W/L)_1 = 6.57$

(3) Determine $(W/L)_3 = (W/L)_4$ ratio from negative CMR

$$\left(\frac{W}{L}\right)_3 = \frac{2I_{DS3}}{K_N (V_{G1(min)} - V_{SS})^2} = \frac{2(5E-6)}{(40E-6)(-4.5 - (-5))^2} = 1 = \left(\frac{W}{L}\right)_4$$

(4) Determine $(W/L)_6$ from the $PM > 60$ specification.

$$PM = 90 - \tan^{-1}(w_{GB} / z) - \tan^{-1}(w_{GB} / p_2)$$

$$w_{GB} = \frac{g_{m2}}{C_C}; z = \frac{g_{m6}}{C_C}; p_2 = \frac{g_{m6}}{C_1 + C_2}; z < p_2; \text{ since } C_C > C_1 + C_2$$

A pessimistic estimate of PM is obtained by assuming $z = p_2$. That is,

$$PM < 90 - 2 \tan^{-1} \left(\frac{g_{m2}/C_c}{g_{m6}/C_c} \right) = 90 - 2 \tan^{-1} \left(\frac{g_{m2}}{g_{m6}} \right)$$

$$\tan^{-1} \left(\frac{g_{m2}}{g_{m6}} \right) < \frac{90 - PM}{2}$$

$$\frac{g_{m2}}{g_{m6}} < \tan \left(\frac{90 - PM}{2} \right)$$

$$g_{m6} > \frac{g_{m2}}{\tan \left(\frac{90 - PM}{2} \right)}$$

To achieve $PM > 60$,

$$g_{m6} > \frac{31.4E - 6}{\tan((90 - 60)/2)} = 117.122E - 6 \approx 120E - 6$$

From step 4 $V_{DS6(SAT)} = V_{DS3(SAT)} = 0.5V$

$$\left(\frac{W}{L} \right)_6 = \frac{g_{m6}}{K_N V_{DS6(SAT)}} = \frac{120E - 6}{(40E - 6)(0.5)} = 6$$

The current through M6 is given by

$$I_{DS6} = \frac{g_{m6}^2}{2K_N (W/L)_6} = \frac{(120E - 6)^2}{2(40E - 6)(6)} = 30uA$$

For balance condition the current through M6 must be properly ratioed with the current through M3,

$$I_{DS6} = \frac{(W/L)_6}{(W/L)_3} I_{DS3} = \frac{6}{1} (5uA) = 30uA$$

(5) Determine $(W/L)_7$ from the balance condition and that $I_{SD7} = I_{DS6}$

$$(W/L)_7 = \frac{I_{SD7}}{I_{SD5}} (W/L)_5 = \frac{30uA}{10uA} (5.333) = 15.999 \approx 16$$

(6) DC gain A_{VO} is computed and compared with the specification:

$$\begin{aligned} A_{VO} &= g_{m2} g_{m6} R_1 R_2 = \frac{g_{m2} g_{m6}}{(g_{ds2} + g_{ds4})(g_{ds5} + g_{ds6})} = \frac{g_{m2} g_{m6}}{(\lambda_2 + \lambda_4) I_{SD2} (\lambda_6 + \lambda_7) I_{DS6}} \\ &= \frac{(31.4E - 6)(120E - 6)}{(.02 + .02)(5E - 6)(.02 + .02)(30E - 6)} = 15,700 \geq 15,000 \end{aligned}$$

(7) From the output resistance specification $R_o \leq 1.46k$, $(W/L)_8$ can be determined. The output resistance is given by:

$$R_o = \frac{1}{g_{m8}} = \sqrt{\frac{1}{2\beta_8 I_{SD8}}} = \sqrt{\frac{1}{2K_p (W/L)_8 I_{SD8}}}$$

Solving for $(W/L)_8$, assuming $I_{SD8} = 100\mu A$ and Pspice parameter $K_p = 15 \mu A/V^2$

$$(W/L)_8 = \frac{1}{2K_p R_o^2 I_{SD8}} = \frac{1}{2(15E-6)(1.46E+3)^2(100E-6)} = 156$$

(8) Determine the (W/L) of the current mirrors. First set up the current source M10 to $100\mu A$ using the biasing current source IB. The V_{GS8} is set up to guarantee it operates at saturation by adding $-0.5v$ beyond its threshold voltage of $V_{tp} = -1v$. That is $V_{SG10} = 1.5v$. $(W/L)_{10}$ can now be determined as follows:

$$(W/L)_{10} = \frac{2I_{SD10}}{K_p (V_{SG10} - |V_{tp}|)^2} = \frac{2(100E-6)}{(15E-6)(1.5 - (-1))^2} = 53.33$$

The rest of current sources are determined by proportionality as follows:

$$I_{SD9} = 100\mu A \Rightarrow (W/L)_9 = (W/L)_{10}(I_{SD9}/I_{SD10}) = (53.33)(100\mu A/100\mu A) = 53.33$$

This complete the design. The results is summarized in the following table:

PAR	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10
I(Ua)	5	5	5	5	10	30	30	100	100	100
T	P	P	N	N	P	N	P	P	P	P
W/L	6.57	6.57	1	1	5.333	6	16	156	53.33	53.33
W(u)	36.792	36.792	5.6	5.6	29.865	33.6	89.6	873.6	298.65	298.65
L(u)	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6
Leff(u)	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6

Finding the W, L to the nearest multiple of $\lambda = 0.6$ length.

PAR	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10
I(Ua)	5	5	5	5	10	30	30	100	100	100
T	P	P	N	N	P	N	P	P	P	P
W/L	6.57	6.57	1	1	5.333	6	16	156	53.33	53.33
W(u)	36.6	36.6	5.4	5.4*	30*	32.4*	90*	873.6	300	300
L(u)	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6
Leff(u)	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6

* Adjusted to satisfy the balance condition to minimize the input offset voltage, Vos:

$$\frac{(W/L)_6}{(W/L)_4} = 2 \frac{(W/L)_7}{(W/L)_5}$$
$$\frac{32.4}{5.4} = 2 \frac{90}{30}$$
$$6 = 6$$

3.0 Opamp Simulation

3.1. DC Offset Voltage and Differential Gain Determination

* Filename="opamp11.cir"

* MOS Diff Amp with PMOS Input and Current Mirror Load

* Input Signals

VID 11 0 DC 0V

E- 1 12 11 0 -0.5

E+ 2 12 11 0 0.5

VIC 12 0 DC 0V

* Power Supplies

VDD 3 0 DC 5VOLT

VSS 4 0 DC -5VOLT

* Netlist for OpAmp Offset Measurement

M1 7 1 5 5 PMOS1 W=36.6U L=6.6U

M2 6 2 5 5 PMOS1 W=36.6U L=6.6U

M3 7 7 4 4 NMOS1 W=5.4U L=6.6U

M4 6 7 4 4 NMOS1 W=5.4U L=6.6U

M5 5 8 3 3 PMOS1 W=30U L=6.6U

M6 9 6 4 4 NMOS1 W=32.4U L=6.6U

M7 9 8 3 3 PMOS1 W=90U L=6.6U

M8 4 9 10 10 PMOS1 W=873.6U L=6.6U

M9 10 8 3 3 PMOS1 W=300U L=6.6U

M10 8 8 3 3 PMOS1 W=300U L=6.6U

Cc 9 6 1pF

*Bias current

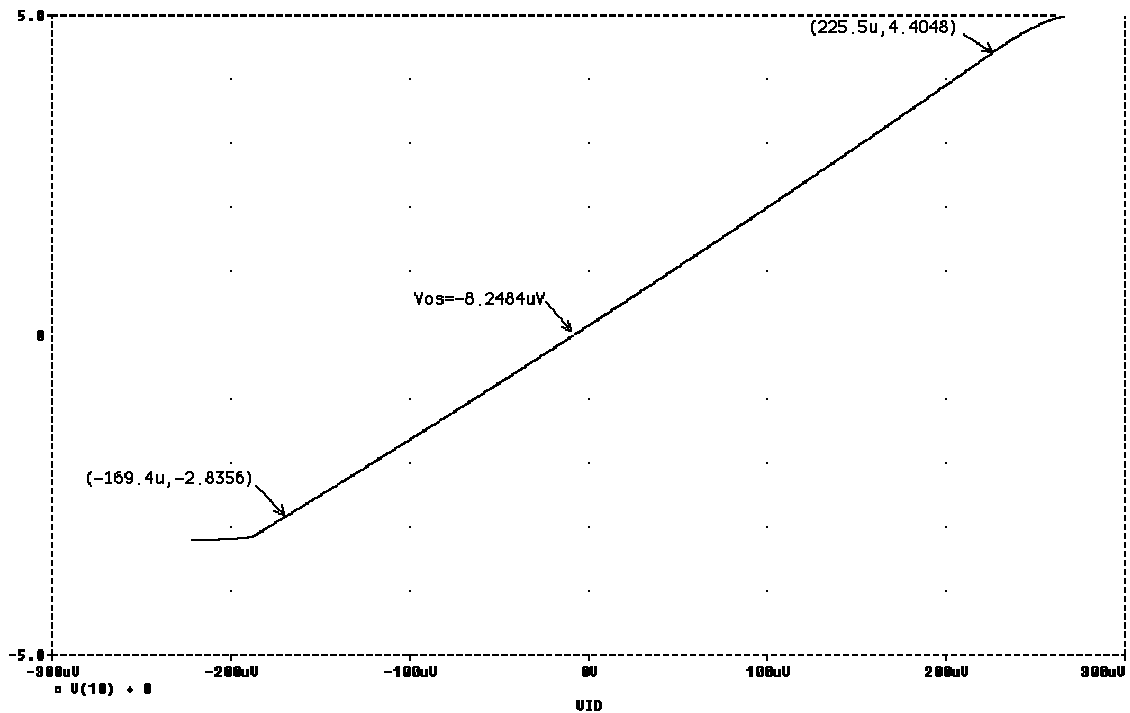
IB 8 4 100UA

* SPICE Parameters

```
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
```

```
*Analysis
.OP
.DC VID -300uV 300uV .1uV
.TF V(10) VID
.PROBE
.END
```

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	0.0000	(2)	0.0000	(3)	5.0000	(4)	-
(5)	1.3115	(6)	-3.4878	(7)	-3.4878	(8)	
(9)	-1.1378	(10)	.1495	(11)	0.0000	(12)	



The output voltage $V_o = V(10)$ is 0.145V at quiescent operating point. This non-zero output voltage can be corrected or reduced by applying an input offset voltage, V_{os} . This offset is determined by finding the value of VID that makes the output

voltage $V_o = V(10) = 0$. From the above graph, this is equal to $-8.2484\mu\text{V}$. The resulting output voltage from simulation is $-2.753\text{E-}6\text{V}$, as shown below:

Modify the VID line in the netlist as follow:

VID 11 0 DC $-8.2484\mu\text{V}$

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	$4.124\text{E-}06$	(2)	$-4.124\text{E-}06$	(3)	5.0000	(4)	-
5.0000							
(5)	1.3115	(6)	-3.4864	(7)	-3.4878	(8)	
3.5084							
(9)	-1.2881	(10)	$-2.753\text{E-}06$	(11)	$-8.248\text{E-}06$	(12)	
0.0000							

The differential gain can be obtained from the DC transfer characteristic by locating two points centered about the bias point of $V_{id} = V_{os} = -8.2484\mu\text{V}$. For accuracy, the two points must be far apart. From the graph:

$$A_{vd} = \frac{4.4048 - (-2.8356)}{(225.5\text{E-}6) - (-169.4\text{E-}6)} = 1.833\text{E} + 4$$

This is very closed to the value obtained using TF analysis of $1.810\text{E} + 4$, as shown below:

**** SMALL-SIGNAL CHARACTERISTICS

$V(10)/VID = 1.810\text{E} + 04$

INPUT RESISTANCE AT VID = $1.000\text{E} + 20$

OUTPUT RESISTANCE AT V(10) = $1.342\text{E} + 03$

3.2. Common-mode Voltage Range Determination

* Filename="opamp24.cir"

* MOS Diff Amp with PMOS Input and Current Mirror Load

* Input Signals

VID 11 0 DC $-8.2484\mu\text{V}$

E- 1 12 11 0 -0.5

E+ 2 12 11 0 0.5

VIC 12 0 DC 0V

* Power Supplies

VDD 3 0 DC 5VOLT

VSS 4 0 DC -5VOLT

* Netlist for Measuring Input CMR

M1 7 1 5 5 PMOS1 W=36.6U L=6.6U

M2 6 2 5 5 PMOS1 W=36.6U L=6.6U

```

M3 7 7 4 4 NMOS1 W=5.4U L=6.6U
M4 6 7 4 4 NMOS1 W=5.4U L=6.6U
M5 5 8 3 3 PMOS1 W=30U L=6.6U
M6 9 6 4 4 NMOS1 W=32.4U L=6.6U
M7 9 8 3 3 PMOS1 W=90U L=6.6U
M8 4 9 10 10 PMOS1 W=873.6U L=6.6U
M9 10 8 3 3 PMOS1 W=300U L=6.6U
M10 8 8 3 3 PMOS1 W=300U L=6.6U
Cc 9 6 1pF

```

```

* Bias current
IB 8 4 100UA

```

```

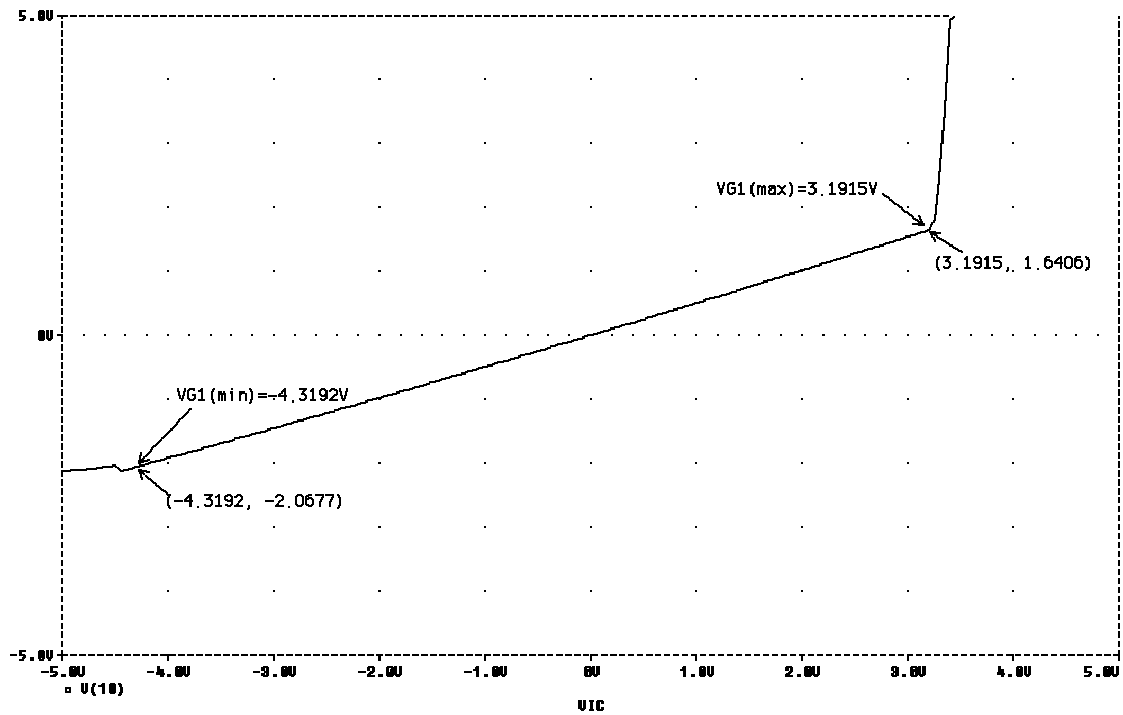
* SPICE Parameter
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

```

```

* Analysis
.DC VIC -5V 5V .05V
.TF V(10) VIC
.PROBE
.END

```



The common-mode input range is determined when the output cease to follow the input linearly. At the low end, it determines $V_{G1}(\min)=-4.4255$, and at the high end, it determines $V_{G1}(\max)=3.1383$. These are very closed to the corresponding design specifications of $V_{G1}(\min)=-4.5$ and $V_{G1}(\max)=3$. The common-mode gain is obtained by locating two points as far apart in the linear range about the operating point. This is shown in the graph above, and computed as follows:

$$A_{cm} = \frac{1.6406 - (-2.0677)}{3.1915 - (-4.3192)} = 0.49373$$

This is very closed to the value obtained using the TF analysis of 0.4984, as shown below:

**** SMALL-SIGNAL CHARACTERISTICS

V(10)/VIC = 4.984E-01

INPUT RESISTANCE AT VIC = 1.000E+20

OUTPUT RESISTANCE AT V(10) = 1.342E+03

The common mode reject ration CMRR is calculated as follows:

$$CMRR = \frac{A_{vd}}{A_{cm}} = \frac{1.833E+4}{0.49373} = 37125.5$$

3.3. Opamp Frequency Response

```
* Filename="opamp33.cir"
* MOS Diff Amp with PMOS Input and Current Mirror Load

* Input Signals
VID 11 0 DC -8.2484uV AC 1V
E- 1 12 11 0 -0.5
E+ 2 12 11 0 0.5
VIC 12 0 DC 0V

* Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC -5VOLT

* Netlist for Frequency Response Measurement
M1 7 1 5 5 PMOS1 W=36.6U L=6.6U
M2 6 2 5 5 PMOS1 W=36.6U L=6.6U
M3 7 7 4 4 NMOS1 W=5.4U L=6.6U
M4 6 7 4 4 NMOS1 W=5.4U L=6.6U
M5 5 8 3 3 PMOS1 W=30U L=6.6U
M6 9 6 4 4 NMOS1 W=32.4U L=6.6U
M7 9 8 3 3 PMOS1 W=90U L=6.6U
M8 4 9 10 10 PMOS1 W=873.6U L=6.6U
M9 10 8 3 3 PMOS1 W=300U L=6.6U
M10 8 8 3 3 PMOS1 W=300U L=6.6U
```

```

Cc 9 6 1pF
CL 10 0 2pF

```

```

*Bias current
IB 8 4 100UA

```

```

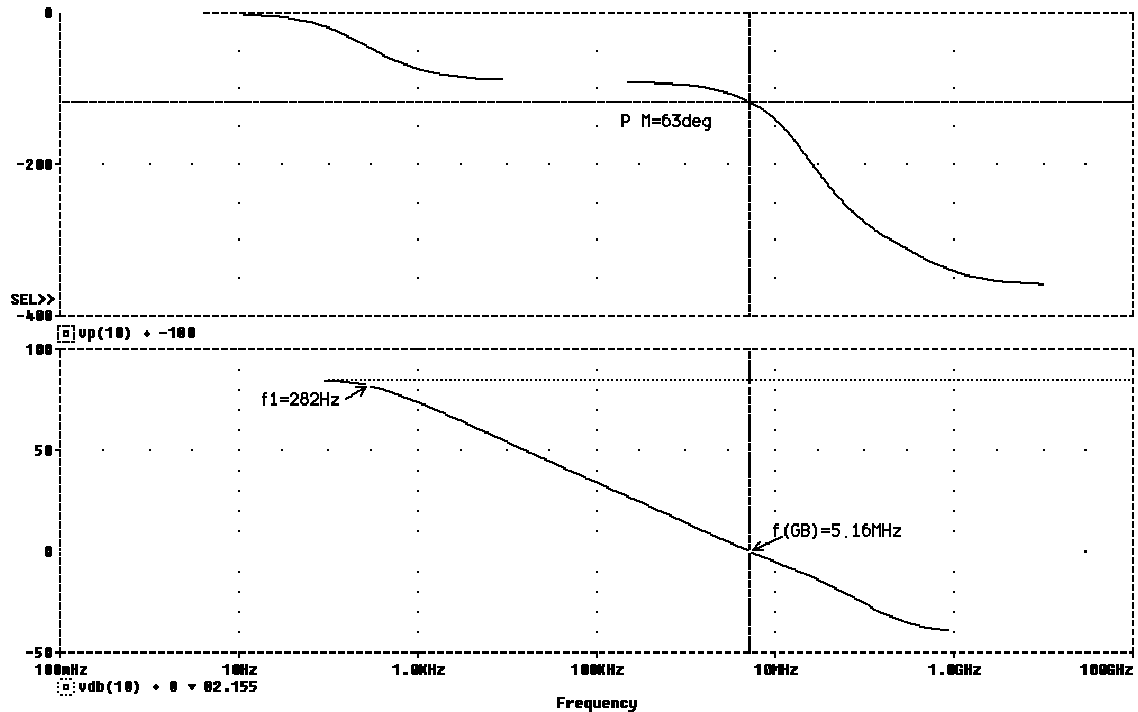
* SPICE Parameters
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

```

```

* Analysis
.AC DEC 10 0.1HZ 10000MegHz
.TF V(10) VID
.PROBE
.END

```



Pspice simulation results:

$A_{VO} = 1.810E + 4$; $PM = 63^\circ$; $f_{GB} = 5.16M$

**** SMALL-SIGNAL CHARACTERISTICS

$V(10)/VID = 1.810E+04$

INPUT RESISTANCE AT VID = $1.000E+20$

OUTPUT RESISTANCE AT $V(10) = 1.342\text{E}+03$

The theoretical bandwidth and gain bandwidth are calculated as follows:

$$g_{m2} = 31.4\mu\text{mho}$$

$$g_{m6} = 140\mu\text{mho}$$

$$R_1 = \frac{1}{(\lambda_2 + \lambda_4)I_2} = \frac{1}{(.02 + .02)(5\text{E} - 6)} = 5\text{M}$$

$$R_2 = \frac{1}{(\lambda_6 + \lambda_7)I_6} = \frac{1}{(.02 + .02)(35\text{E} - 6)} = .714\text{M}$$

$$p_1 \cong \frac{-1}{g_{m2}R_1R_2C_C} = \frac{-1}{(140\text{E} - 6)(5\text{E}6)(.714\text{E}6)(1\text{E} - 12)} = 2000$$

$$f_1 = \frac{p_1}{2\pi} = \frac{2000}{2\pi} = 318\text{Hz}$$

$$f_{GB} = A_{v0}f_1 = (15700)(318) = 5\text{M}$$

$$z = \frac{g_{m6}}{C_C} = \frac{(140\text{E} - 6)}{(1\text{E} - 12)} = 140\text{E}6$$

$$f_z = \frac{z}{2\pi} = \frac{140\text{E}6}{2\pi} = 22.3\text{M}$$

Simulation results are : $f_1 = 258\text{Hz}$, $f_{GB} = 5.16\text{M}$, f_z and f_2 are difficult to obtain accurately from bode plot.

3.4. Slew Rate Measurement

* Filename="opamp44.cir"

* MOS Diff Amp with PMOS Input and Current Mirror Load

* Input Signal

VIN 2 0 PWL(0,-5V 10us,-5V 10.01us,5V 30us, 5V 30.01us,-5V 1s, -5V)

*Power Supplies

VDD 3 0 DC 5VOLT

VSS 4 0 DC -5VOLT

* Netlist for Slew Rate Measurement

M1 7 1 5 5 PMOS1 W=36.6U L=6.6U

M2 6 2 5 5 PMOS1 W=36.6U L=6.6U

M3 7 7 4 4 NMOS1 W=5.4U L=6.6U

M4 6 7 4 4 NMOS1 W=5.4U L=6.6U

M5 5 8 3 3 PMOS1 W=30U L=6.6U

M6 9 6 4 4 NMOS1 W=32.4U L=6.6U

M7 9 8 3 3 PMOS1 W=90U L=6.6U

M8 4 9 10 10 PMOS1 W=873.6U L=6.6U

M9 10 8 3 3 PMOS1 W=300U L=6.6U

M10 8 8 3 3 PMOS1 W=300U L=6.6U

Cc 9 6 1pF

* Bias current

IB 8 4 100UA

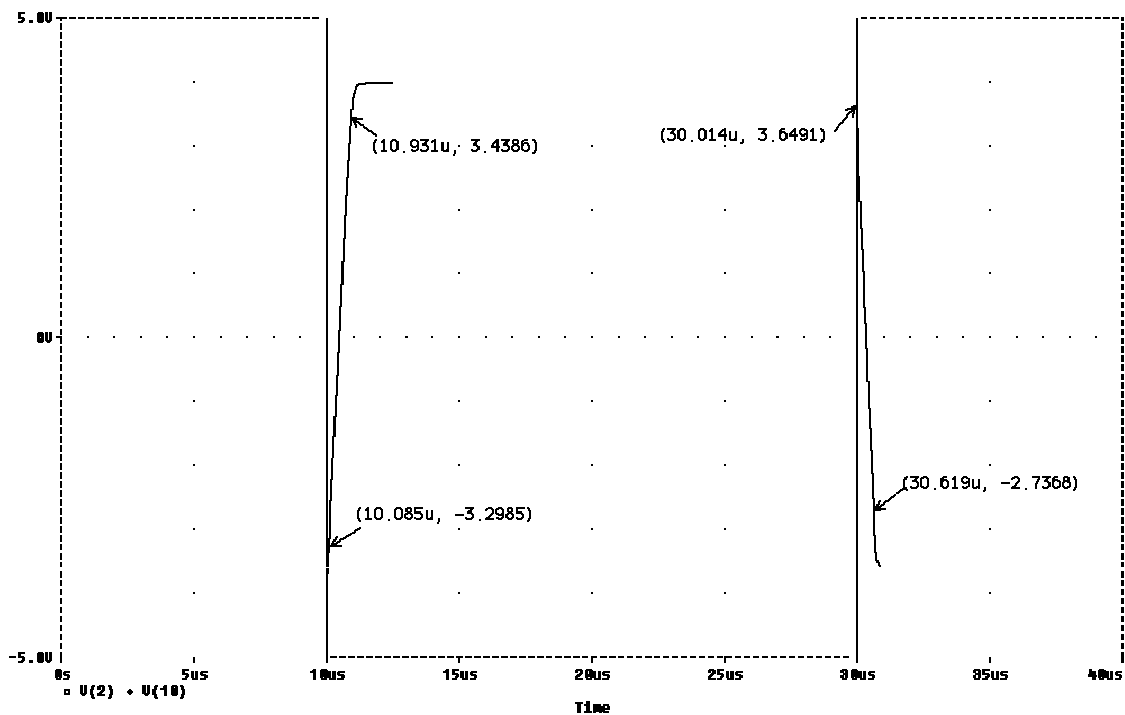
```

* External Component for Slew Rate Measurement
VSH 1 10 DC 0V

* SPICE Parameters
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

*Analysis
.TRAN .1ns 40us
.PROBE
.END

```



The positive slew rate is the slope of the rising edge of the output. This is computed from the two points on the rising edge. That is,

$$SR^+ = \frac{3.4386 - (-3.2985)}{10.931 - 10.085} = 7.96 \text{ V/us}$$

Similarly, the new slew rate is computed as follows:

$$SR = \frac{-2.7368 - 3.6491}{30.619 - 30.014} = -10.55 \text{ V/us}$$

4.0 Op Amp Design Specification

V_{dd} = +5V, V_{ss} = -5V, A_o ≥ 30,000, GB = 2π(5MHz), SR = 10V/uS, R_o ≤ 1.46k
-4.5 ≤ CMR ≤ 3

SPICE Parameters: K_n = 40uA/V², K_p = 15uA/V², λ = 0.02

Increasing Overall DC Gain

DC gain A_{VO} is computed and compared with the specification:

$$\begin{aligned} A_{VO} = A_{V1} A_{V2} &= [g_{m2} R_1][g_{m6} R_2] = \left[\frac{g_{m2}}{(g_{ds2} + g_{ds4})} \right] \left[\frac{g_{m6}}{(g_{ds5} + g_{ds6})} \right] \\ &= \left[\frac{g_{m2}}{(\lambda_2 + \lambda_4) I_{SD2}} \right] \left[\frac{g_{m6}}{(\lambda_6 + \lambda_7) I_{DS6}} \right] \\ &= \left[\frac{(31.4E-6)}{(.02 + .02)(5E-6)} \right] \left[\frac{(120E-6)}{(.02 + .02)(30E-6)} \right] = 15,700 \leq 30,000 \end{aligned}$$

Pspice simulation results:

$$A_{VO} = 1.810E+4; \text{ PM} = 63^\circ; f_{GB} = 5.16M$$

Increasing Overall Gain By Increasing A_{V1}

$$A_{V1} = \frac{g_{m2}}{(\lambda_2 + \lambda_4) I_{SD2}} = \frac{\sqrt{2K_P (W/L)_2 I_{SD2}}}{(\lambda_2 + \lambda_4) I_{SD2}} = \frac{\sqrt{2K_P}}{(\lambda_2 + \lambda_4)} \sqrt{\frac{(W/L)_2}{I_{SD2}}}$$

The current I_{SD2} is half the bias current I_{SD5} and is independent of (W/L)₂. That is, the gain can be adjusted by simply adjusting (W/L)₂ while I_{SD2} remains constant. The gain A_{V1} is proportional to $\sqrt{(W/L)_2}$. For example to increase the overall gain by 2, one needs to increase (W/L)₁, (W/L)₂ by a factor of 4.

PAR	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10
I(Ua)	5	5	5	5	10	30	30	100	100	100
T	P	P	N	N	P	N	P	P	P	P

W/L	6.57	6.57	1	1	5.333	6	16	156	53.33	53.33
W(u)	4*36.6	4*36.6	5.4	5.4	30	32.4	90	873.6	300	300
L(u)	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6
Leff(u)	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6

Increasing Av1

* Filename="opamp331.cir"

* MOS Diff Amp with PMOS Input and Current Mirror Load

* Increasing Overall Gain By Increasing W/L of M1 & M2

* Input Signals

VID 11 0 DC -8.2484uV AC 1V

E- 1 12 11 0 -0.5

E+ 2 12 11 0 0.5

VIC 12 0 DC 0V

* Power Supplies

VDD 3 0 DC 5VOLT

VSS 4 0 DC -5VOLT

* Netlist for Frequency Response Measurement

M1 7 1 5 5 PMOS1 W={4*36.6U} L=6.6U

M2 6 2 5 5 PMOS1 W={4*36.6U} L=6.6U

M3 7 7 4 4 NMOS1 W=5.4U L=6.6U

M4 6 7 4 4 NMOS1 W=5.4U L=6.6U

M5 5 8 3 3 PMOS1 W=30U L=6.6U

M6 9 6 4 4 NMOS1 W={32.4U} L=6.6U

M7 9 8 3 3 PMOS1 W={90U} L=6.6U

M8 4 9 10 10 PMOS1 W=873.6U L=6.6U

M9 10 8 3 3 PMOS1 W=300U L=6.6U

M10 8 8 3 3 PMOS1 W=300U L=6.6U

Cc 9 6 1pF

*Bias current

IB 8 4 100UA

* SPICE Parameters

.MODEL NMOS1 NMOS VTO=1 KP=40U

+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6

+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10

+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

.MODEL PMOS1 PMOS VTO=-1 KP=15U

+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6

+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10

+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

* Analysis

.AC DEC 10 0.1HZ 10000MegHz

```
.TF V(10) VID
.PROBE
.END
```

Before increasing (W/L) of M1 and M2

*** SMALL-SIGNAL CHARACTERISTICS

V(10)/VID = 1.810E+04

INPUT RESISTANCE AT VID = 1.000E+20

OUTPUT RESISTANCE AT V(10) = 1.342E+03

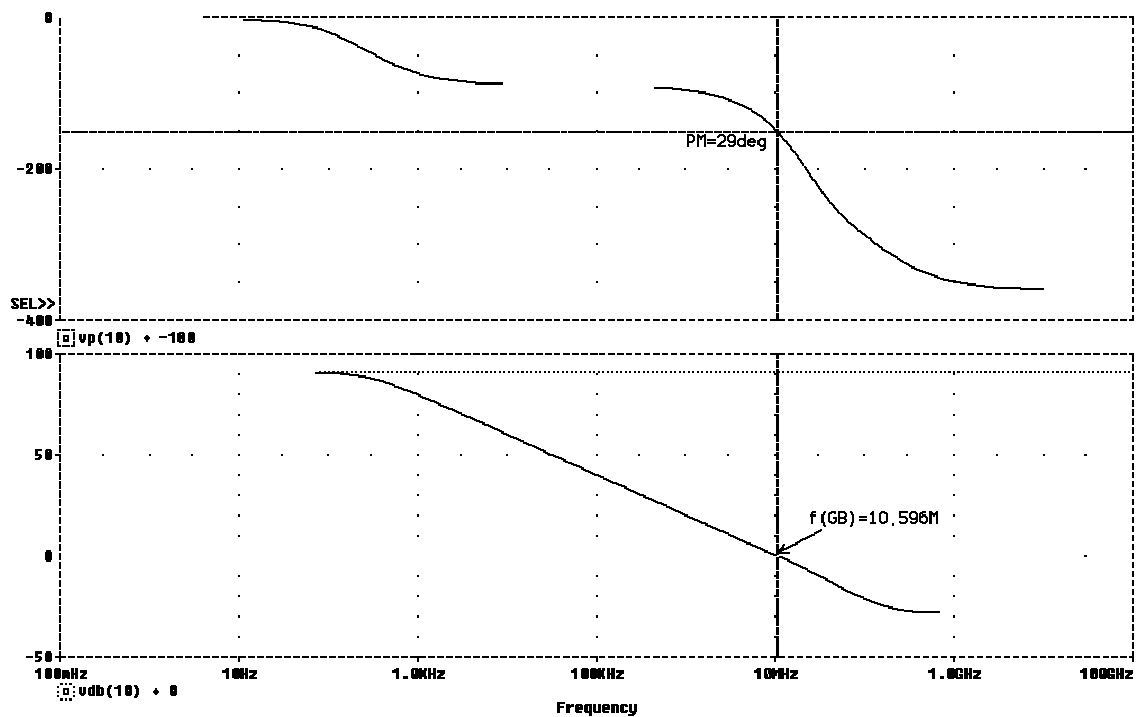
After Increasing (W/L) of M1 and M2 by 4

*** SMALL-SIGNAL CHARACTERISTICS

V(10)/VID = 3.590E+04

INPUT RESISTANCE AT VID = 1.000E+20

OUTPUT RESISTANCE AT V(10) = 1.342E+03



Although the DC gain increases the PM decreases.

AV0=3.590E+4; PM=29°; f_{GB}=10.596M

The Overall Gain Is Independent of A_{v2}

The second stage gain can not be used to increase the overall gain but is used to adjust the phase margin as shown below:

$$A_{v2} = \frac{g_{m6}}{(\lambda_6 + \lambda_7)I_{DS6}} = \frac{\sqrt{2K_N(W/L)_6 I_{DS6}}}{(\lambda_6 + \lambda_7)I_{DS6}} = \frac{\sqrt{2K_N}}{(\lambda_6 + \lambda_7)} \sqrt{\frac{(W/L)_6}{I_{DS6}}}$$

Since I_{DS6} is determined by current mirror, increasing (W/L)₆ increases I_{DS6} proportionately as shown below:

$$I_{DS6} = \frac{(W/L)_6}{(W/L)_4} I_{DS4} \Rightarrow \frac{(W/L)_6}{I_{DS6}} = \frac{(W/L)_4}{I_{DS4}} = \text{constant}$$

That is, increasing I_{DS6} or (W/L)₆ does not increase the overall gain, but g_{m6} is increased by $\sqrt{(W/L)_6 I_{DS6}}$. That is, g_{m6} is doubled by increasing (W/L)₆ by a factor of 2, and by current mirror I_{DS6} is also increase by a factor of 2. Similarly, (W/L)₇ must be doubled, since I_{DS6}=I_{DS7}. The phase margin, which deteriorates when increasing (W/L)₂ or g_{m2}, can be compensated by increasing g_{m6}.

PAR	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10
I(Ua)	5	5	5	5	10	2*30	2*30	100	100	100
T	P	P	N	N	P	N	P	P	P	P
W/L	6.57	6.57	1	1	5.333	6	16	156	53.33	53.33
W(u)	4*36.6	4*36.6	5.4	5.4	30	2*32.4	2*90	873.6	300	300
L(u)	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6
Leff(u)	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6

Pspice simulation results:

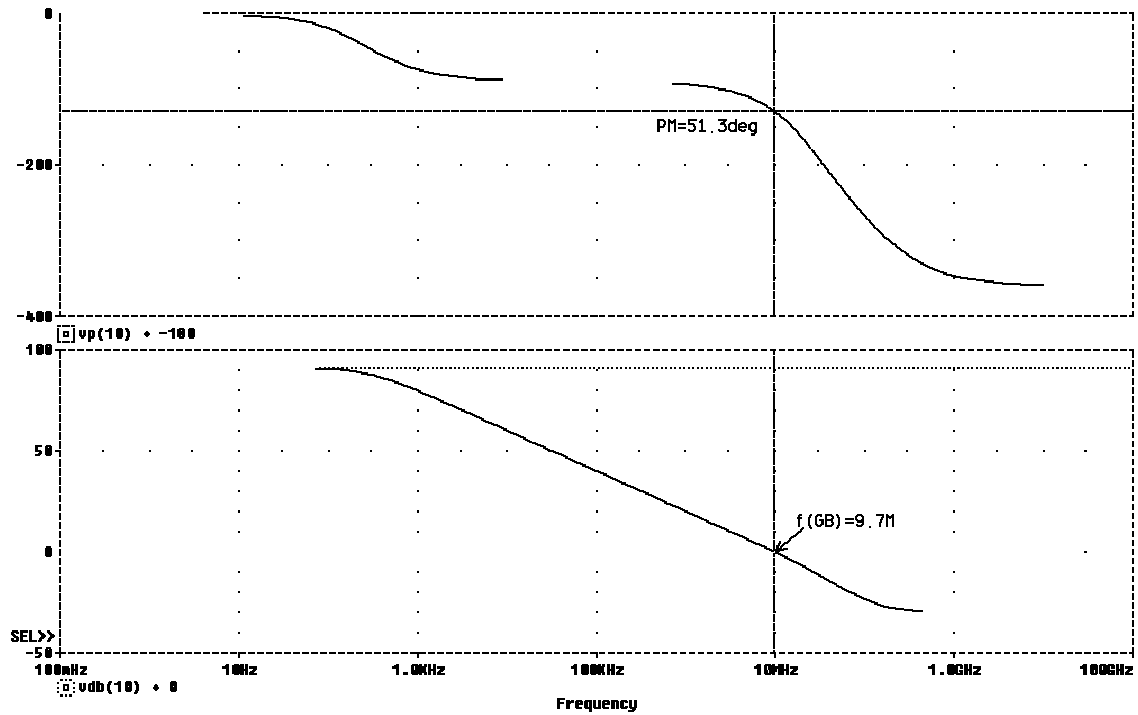
$$A_{v0} = 3.590E + 4; PM = 51.3^\circ; f_{GB} = 9.7M$$

**** SMALL-SIGNAL CHARACTERISTICS

$$V(10)/VID = 3.590E+04$$

$$\text{INPUT RESISTANCE AT VID} = 1.000E+20$$

$$\text{OUTPUT RESISTANCE AT V(10)} = 1.342E+03$$



The phase margin can be increased further by increasing both $(W/L)_6$ and $(W/L)_7$. The desired phase margin of 65° is approached when $(W/L)_6$ and $(W/L)_7$ are increased by a factor of 4

PAR	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10
I(Ua)	5	5	5	5	10	4*30	4*30	100	100	100
T	P	P	N	N	P	N	P	P	P	P
W/L	6.57	6.57	1	1	5.333	6	16	156	53.33	53.33
W(u)	4*36.6	4*36.6	5.4	5.4	30	4*32.4	4*90	873.6	300	300
L(u)	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6
Leff(u)	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6

The Overall Gain Is Independent of A_{v2} But Adjust Phase Margin

* Filename="opamp331.cir"
 * MOS Diff Amp with PMOS Input and Current Mirror Load
 * Increasing Overall Gain By Increasing W/L of M1 & M2
 * Input Signals
 VID 11 0 DC -8.2484uV AC 1V
 E- 1 12 11 0 -0.5
 E+ 2 12 11 0 0.5
 VIC 12 0 DC 0V
 * Power Supplies
 VDD 3 0 DC 5VOLT
 VSS 4 0 DC -5VOLT

* Netlist for Frequency Response Measurement

```

M1 7 1 5 5 PMOS1      W={4*36.6U}  L=6.6U
M2 6 2 5 5 PMOS1      W={4*36.6U}  L=6.6U
M3 7 7 4 4 NMOS1      W=5.4U      L=6.6U
M4 6 7 4 4 NMOS1      W=5.4U      L=6.6U
M5 5 8 3 3 PMOS1      W=30U       L=6.6U
M6 9 6 4 4 NMOS1      W={4*32.4U}  L=6.6U
M7 9 8 3 3 PMOS1      W={4*90U}   L=6.6U
M8 4 9 10 10 PMOS1    W=873.6U   L=6.6U
M9 10 8 3 3 PMOS1     W=300U      L=6.6U
M10 8 8 3 3 PMOS1     W=300U      L=6.6U
Cc 9 6 1pF

```

*Bias current

```
IB 8 4 100UA
```

* SPICE Parameters

```

.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

```

* Analysis

```

.AC DEC 10 0.1HZ 10000MegHz
.TF V(10) VID
.PROBE
.END

```

Pspice simulation results:

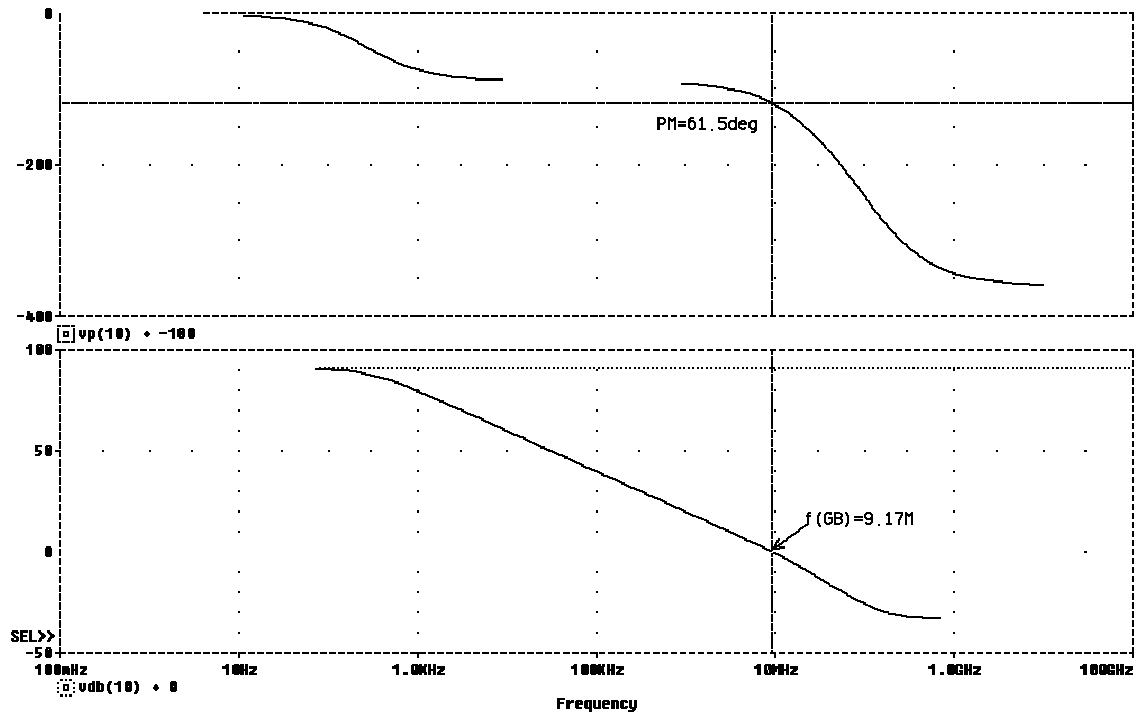
$$A_{VO} = 3.590E + 4; PM = 61.5^\circ; f_{GB} = 9.17M$$

**** SMALL-SIGNAL CHARACTERISTICS

$$V(10)/VID = 3.590E+04$$

$$INPUT\ RESISTANCE\ AT\ VID = 1.000E+20$$

$$OUTPUT\ RESISTANCE\ AT\ V(10) = 1.342E+03$$



5.0 Phase Margin Correction By Moving the Zero from RHP to LHP

The location of zero is given by:

$$z = \frac{1}{C_3 \left(\frac{1}{g_{m6}} - R_3 \right)} = \frac{1}{C_C \left(\frac{1}{g_{m6}} - R_C \right)}$$

The zero can be moved from the RHP to the LHP by selecting $R_C \gg \frac{1}{g_{m6}}$, with this choice the zero is approximately given by:

$$z \approx \frac{-1}{R_C C_C}$$

A zero in the LHP increase the phase margin rather decrease as in the case of RHP zero. The transfer function of an op amp compensated by resistor R_C and capacitor C_C connected in series is given by:

$$A_v(s) = \frac{A_{v0} \left(1 - \frac{s}{z}\right)}{\left(1 - \frac{s}{p_1}\right) \left(1 - \frac{s}{p_2}\right) \left(1 - \frac{s}{p_3}\right)}$$

where:

$$p_1 \approx \frac{-1}{g_{m6} R_1 R_2 C_C}$$

$$p_2 \approx \frac{-g_{m6}}{C_1 + C_2}$$

$$p_3 \approx \frac{-1}{R_C C_1}$$

$$z \approx \frac{-1}{R_C C_C}$$

$$A_v(s) \approx \frac{A_{v0} \left(1 - \frac{s}{z}\right)}{\left(1 - \frac{s}{p_1}\right) \left(1 - \frac{s}{p_2}\right)}; \text{ since } p_1 \ll p_2 \ll p_3$$

$$\angle A_v(\omega_{GB}) = \tan^{-1} \left(\frac{\omega_{GB}}{z} \right) - \tan^{-1} \left(\frac{\omega_{GB}}{p_1} \right) - \tan^{-1} \left(\frac{\omega_{GB}}{p_2} \right)$$

$$PM = 180^\circ + \angle A_v(\omega_{GB}) = 180^\circ + \tan^{-1} \left(\frac{\omega_{GB}}{z} \right) - \tan^{-1} \left(\frac{\omega_{GB}}{p_1} \right) - \tan^{-1} \left(\frac{\omega_{GB}}{p_2} \right)$$

With extra phase margin introduced by the LHP zero, the phase margin can be increased without increasing the sizes of M6 and M7. To make sure that the op amp behaves as single order system within the gain bandwidth, ω_{GB} . One positions the zero 20% ($z = 1.2\omega_{GB}$) over the gain bandwidth. In the previous example, the non-dominant pole was position at $p_2 = 1.1\omega_{GB} = 2.2\omega'_{GB}$. Where ω'_{GB} is the original gain bandwidth prior to doubling g_{m2} which double the gain bandwidth. The new phase margin gain be calculated as follows:

$$\begin{aligned} PM &= 180^\circ + \angle A_v(\omega_{GB}) = 180^\circ + \tan^{-1} \left(\frac{\omega_{GB}}{z} \right) - \tan^{-1} \left(\frac{\omega_{GB}}{p_1} \right) - \tan^{-1} \left(\frac{\omega_{GB}}{p_2} \right) \\ &= 180^\circ + \tan^{-1} \left(\frac{\omega_{GB}}{1.2\omega_{GB}} \right) - \tan^{-1} \left(\frac{A_{v0} p_1}{p_1} \right) - \tan^{-1} \left(\frac{\omega_{GB}}{1.1\omega_{GB}} \right) \\ &\approx 180^\circ + \tan^{-1}(.833) - \tan^{-1}(A_{v0}) - \tan^{-1}(0.909) \approx 87.53 \end{aligned}$$

The value of R_C to place the zero is calculated as follows:

$$z = \frac{1}{R_C C_C} = 1.2 \omega_{GB} = 1.2 \frac{g_{m2}}{C_C}$$

$$R_C = \frac{1}{1.2 g_{m2}} = \frac{1}{1.2 (2 \times 31.4 \text{E} - 6)} = 13.25 \text{k}$$

PAR	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10
I(Ua)	5	5	5	5	10	35	35	100	100	100
T	P	P	N	N	P	N	P	P	P	P
W/L	6.57	6.57	1	1	5.333	7	18.665	156	53.33	53.33
W(u)	4*36.6	4*36.6	5.4	5.4	30	37.8	105	873.6	300	300
L(u)	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6
Leff(u)	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6

$$R_C = 13.25 \text{k}, C_C = 1 \text{pF}$$

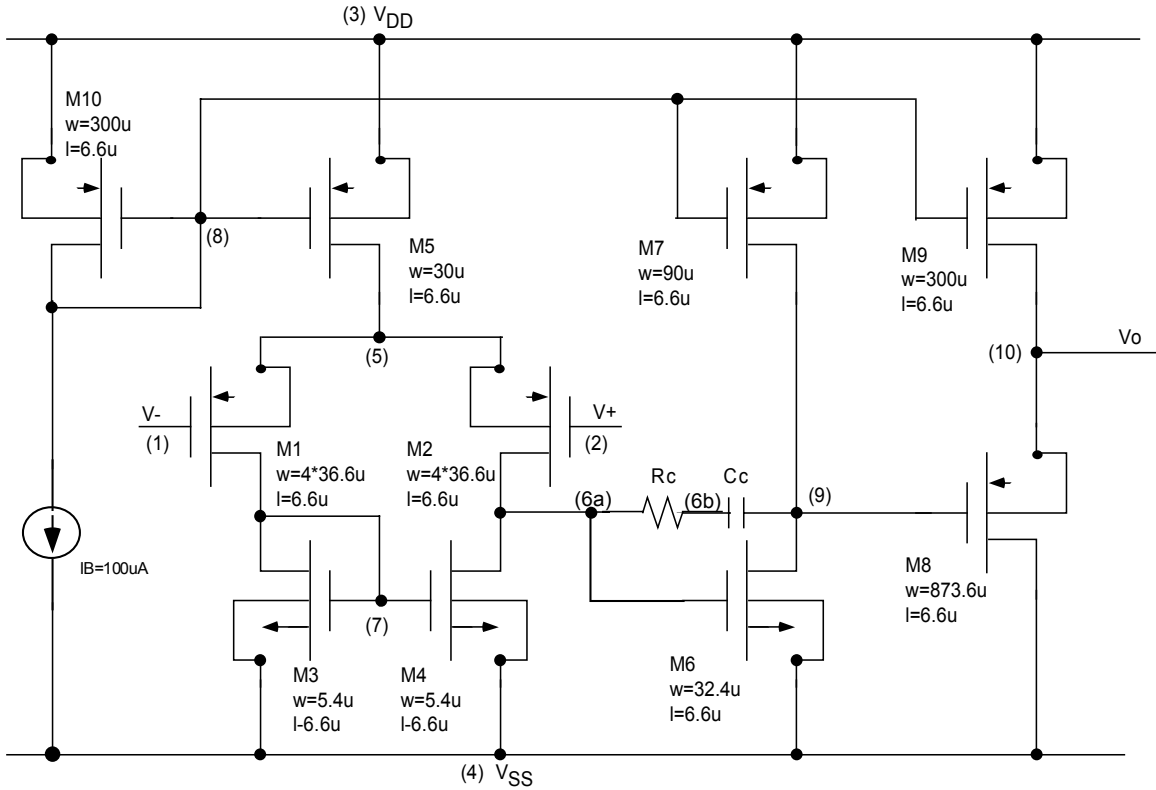


Fig 10a

- * Filename="opamp33z.cir"
- * MOS Diff Amp with PMOS Input and Current Mirror Load
- * Input Signals

```

VID 11 0 DC -8.2484uV AC 1V
E- 1 12 11 0 -0.5
E+ 2 12 11 0 0.5
VIC 12 0 DC 0V

```

```

* Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC -5VOLT

```

```

* Netlist for Frequency Response Measurement
M1 7 1 5 5      PMOS1      W={4*36.6U}  L=6.6U
M2 6a 2 5 5     PMOS1      W={4*36.6U}  L=6.6U
M3 7 7 4 4      NMOS1      W=5.4U      L=6.6U
M4 6a 7 4 4      NMOS1      W=5.4U      L=6.6U
M5 5 8 3 3      PMOS1      W=30U       L=6.6U
M6 9 6a 4 4      NMOS1      W={32.4U}   L=6.6U
M7 9 8 3 3      PMOS1      W={90U}     L=6.6U
M8 4 9 10 10     PMOS1      W=873.6U    L=6.6U
M9 10 8 3 3      PMOS1      W=300U      L=6.6U
M10 8 8 3 3      PMOS1      W=300U      L=6.6U
Cc 9 6b 1pF
Rc 6a 6b {13.25k}

```

```

*Bias current
IB 8 4 100UA

```

```

* SPICE Parameters
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

```

```

* Analysis
.AC DEC 10 0.1HZ 10000MegHz
.TF V(10) VID
.PROBE
.END

```

Pspice simulation results:

$$A_{VO} = 3.590E + 4; PM = 85.5^\circ; f_{GB} = 10.294M$$

***** SMALL-SIGNAL CHARACTERISTICS

$$V(10)/VID = 3.590E+04$$

INPUT RESISTANCE AT VID = 1.000E+20

OUTPUT RESISTANCE AT V(10) = 1.342E+03

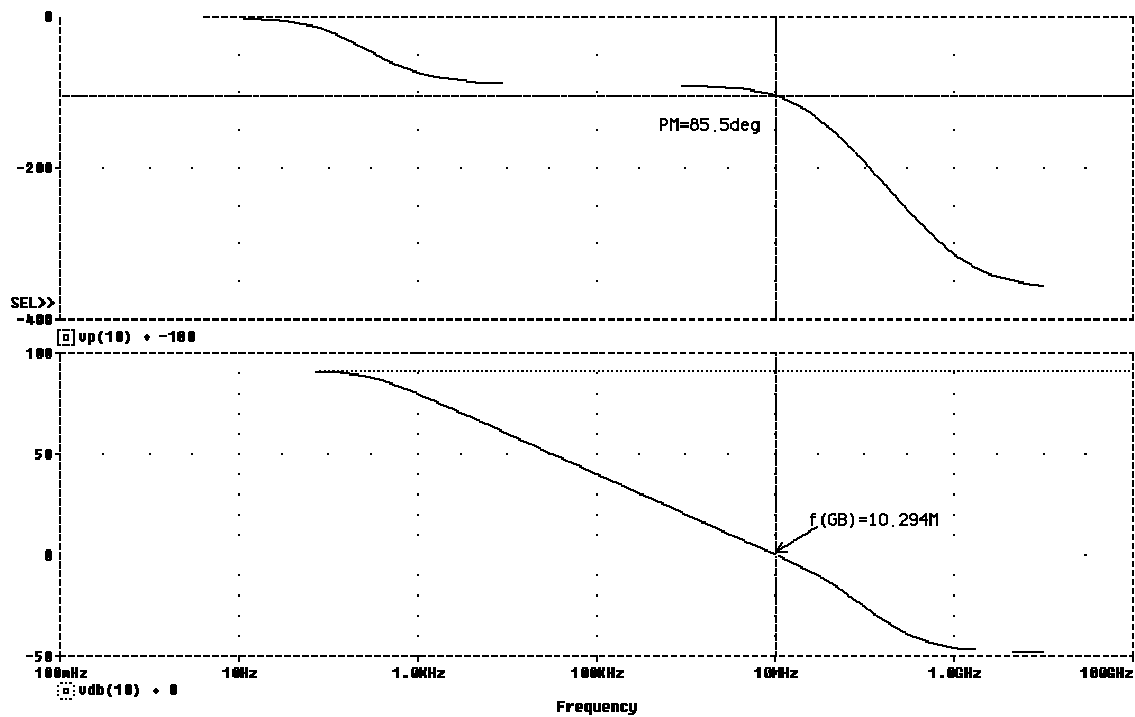
NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE

(1) 4.124E-06 (2) -4.124E-06 (3) 5.0000 (4) -5.0000

(5) 1.1562 (7) -3.4870 (8) 3.5084 (9) -1.5153

(10) -0.2260 (11) -8.248E-06 (12) 0.0000 (6a) -3.4842

(6b) -3.4842



6.0 Implementation of Rc with NMOS Transistor

Transistor M11 has $V_{DS11}=0$ since no dc bias current flows through its because of capacitor Cc. Therefore, it is operating at the ohmic or triode region. That is,

$$I_D = K_N (W/L) [V_{GS} - V_{TN} - V_{DS}/2] V_{DS}$$

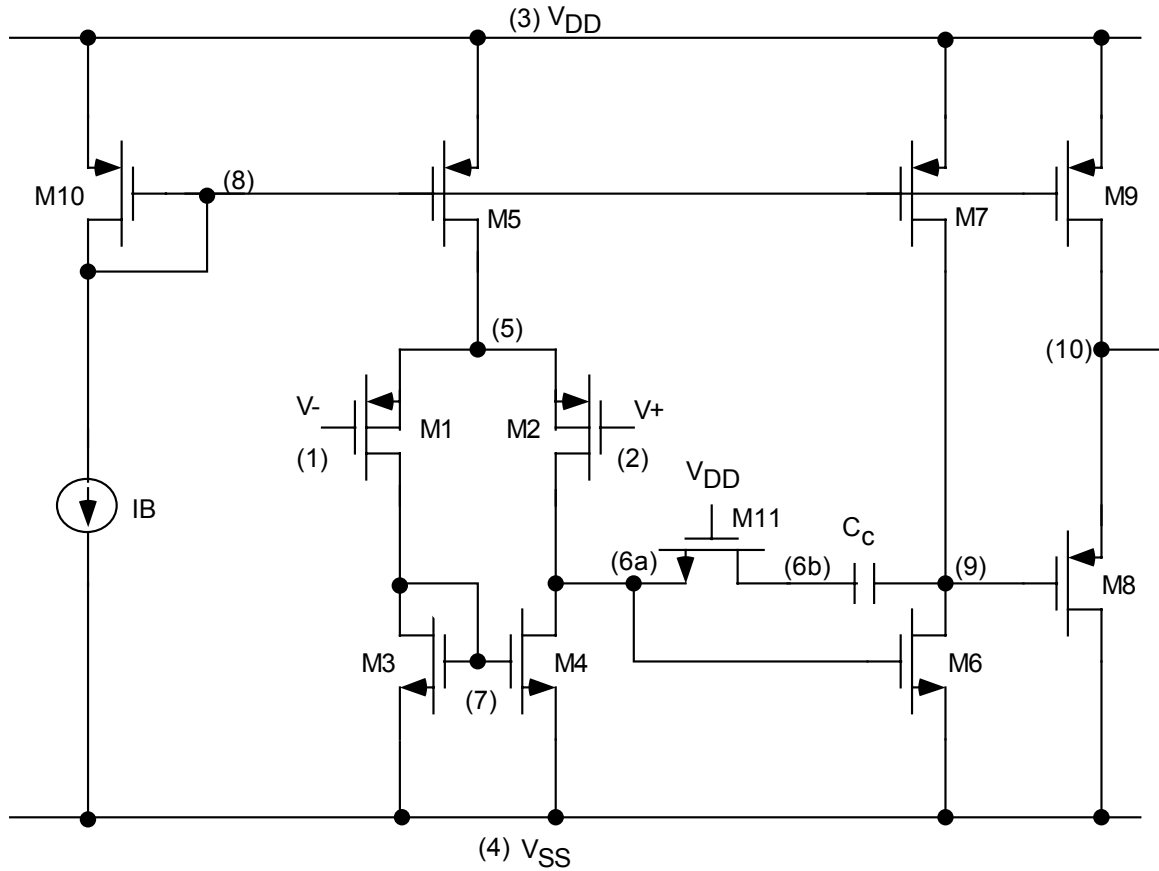
The resistance value implemented by this transistor is given by

$$V_{TN} = V_{TO} + \gamma \left[\sqrt{2\phi + V_{SB}} - \sqrt{2\phi_F} \right]$$

$$= 1 + 1 \left[\sqrt{2(0.6) + (-3.4836 - (-5))} - \sqrt{2(0.6)} \right] = 1.65$$

$$R_C = r_{DS10} = \left(\frac{\partial I_D}{\partial V_{DS}} \right)^{-1} = \frac{1}{K_N (W/L) (V_{GS} - V_{TN})}$$

$$(W/L) = \frac{1}{K_N R_C (V_{GS} - V_{TN})} = \frac{1}{40E-6 (13.25E+3) (5 - (-3.4842) - 1.65)} = 0.276 = \frac{6u}{27u}$$



* Filename="opamp33m.cir"
 * MOS Diff Amp with PMOS Input and Current Mirror Load
 * Input Signals
 VID 11 0 DC -8.2484uV AC 1V
 E- 1 12 11 0 -0.5

E+ 2 12 11 0 0.5
VIC 12 0 DC 0V

* Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC -5VOLT

* Netlist for Frequency Response Measurement

M1 7 1 5 5	PMOS1	W={4*36.6U}	L=6.6U
M2 6a 2 5 5	PMOS1	W={4*36.6U}	L=6.6U
M3 7 7 4 4	NMOS1	W=5.4U	L=6.6U
M4 6a 7 4 4	NMOS1	W=5.4U	L=6.6U
M5 5 8 3 3	PMOS1	W=30U	L=6.6U
M6 9 6a 4 4	NMOS1	W={32.4U}	L=6.6U
M7 9 8 3 3	PMOS1	W={90U}	L=6.6U
M8 4 9 10 10	PMOS1	W=873.6U	L=6.6U
M9 10 8 3 3	PMOS1	W=300U	L=6.6U
M10 8 8 3 3	PMOS1	W=300U	L=6.6U
M11 6b 3 6a 4	NMOS1	W=6U	L=27U

Cc 9 6b 1pF

*Rc 6a 6b {13.25k}

*Bias current
IB 8 4 100UA

* SPICE Parameters

.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

* Analysis

.PROBE
.AC DEC 10 0.1HZ 10000MegHz
.TF V(10) VID
.END

Pspice simulation results:

$A_{VO} = 3.590E + 4$; $PM = 87.7^\circ$; $f_{GB} = 11.9M$

**** SMALL-SIGNAL CHARACTERISTICS

V(10)/VID = 3.590E+04

INPUT RESISTANCE AT VID = 1.000E+20

OUTPUT RESISTANCE AT V(10) = 1.342E+03

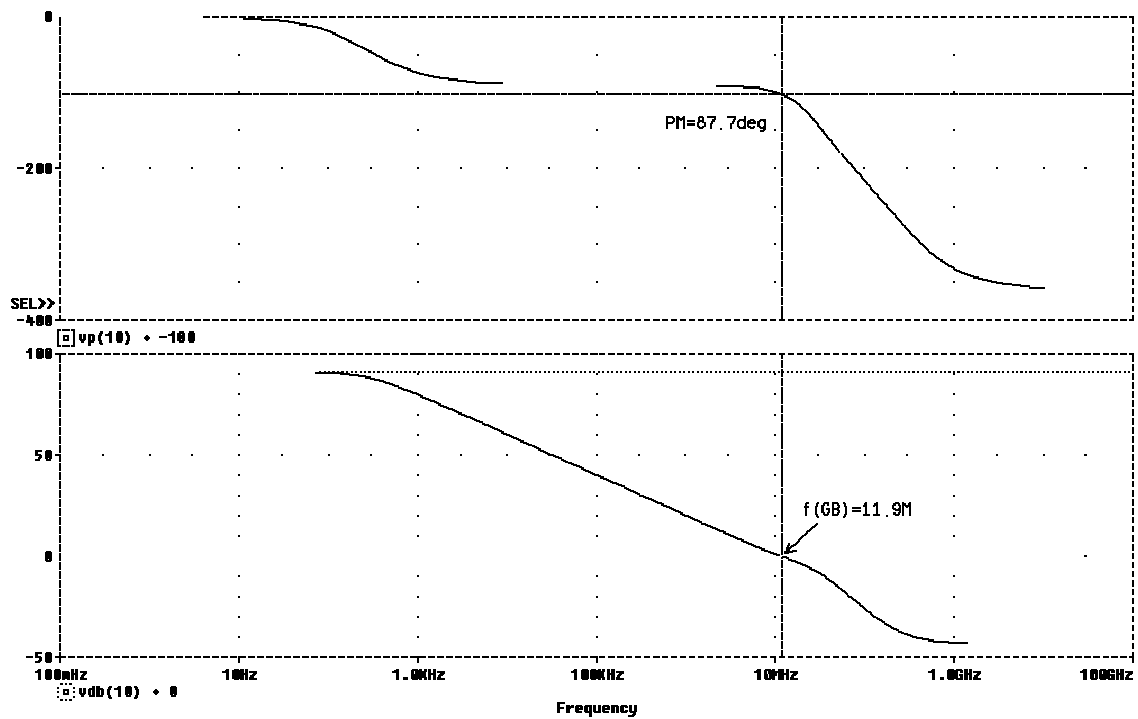
NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE

(1) 4.124E-06 (2) -4.124E-06 (3) 5.0000 (4) -5.0000

(5) 1.1562 (7) -3.4870 (8) 3.5084 (9) -1.5137

(10) -0.2244 (11) -8.248E-06 (12) 0.0000 (6a) -3.4843

(6b) -3.4843



7.0 Opamp with ClassAB Output Buffer

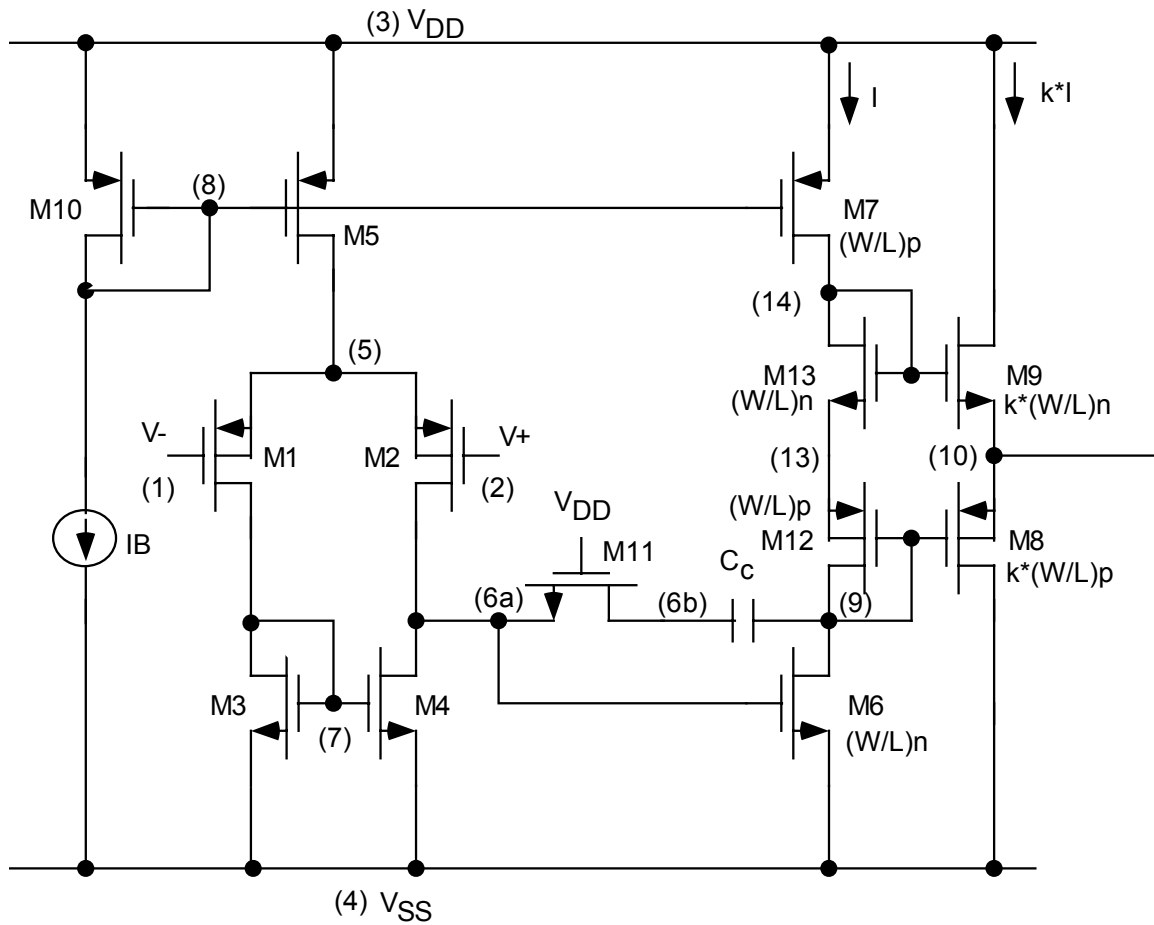


Figure 12b

k=3

```
* Filename="op33zab2.cir"
* MOS Diff Amp with PMOS Input and Current Mirror Load
* Input Signals
VID 11 0 DC -8.2484uV AC 1V
E- 1 12 11 0 -0.5
E+ 2 12 11 0 0.5
VIC 12 0 DC 0V

* Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC -5VOLT

* Netlist for Frequency Response Measurement
M1 7 1 5 5      PMOS1      W={4*36.6U}   L=6.6U
M2 6a 2 5 5     PMOS1      W={4*36.6U}   L=6.6U
M3 7 7 4 4      NMOS1      W=5.4U      L=6.6U
```

```

M4 6a 7 4 4    NMOS1    W=5.4U    L=6.6U
M5 5 8 3 3    PMOS1    W=30U    L=6.6U
M6 9 6a 4 4    NMOS1    W={32.4U} L=6.6U
M7 14 8 3 3    PMOS1    W={90U}  L=6.6U
M8 4 9 10 10   PMOS1    W={3*90U} L=6.6U
M9 3 14 10 4    NMOS1    W={3*32.4U} L=6.6U
M10 8 8 3 3    PMOS1    W=300U   L=6.6U
M11 6b 3 6a 4  NMOS1    W=6U     L=27U
M12 9 9 13 13  PMOS1    W=90U    L=6.6U
M13 14 14 13 4 NMOS1    W=32.4U  L=6.6U
Cc 9 6b 1pF

```

```

*Bias current
IB 8 4 100UA

```

```

* SPICE Parameters
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

```

```

* Analysis
.PROBE
.DC VID -5V 5V .1V
.AC DEC 10 0.1HZ 10000MegHz
.TF V(10) VID
.END

```

Pspice simulation results:

$$A_{v0} = 3.065E + 4; PM = 86.1^\circ; f_{GB} = 10.9M; R_o = 1.113E + 3$$

**** SMALL-SIGNAL CHARACTERISTICS

$$V(10)/VID = 3.065E+04$$

$$\text{INPUT RESISTANCE AT VID} = 1.000E+20$$

$$\text{OUTPUT RESISTANCE AT V(10)} = 1.113E+03$$

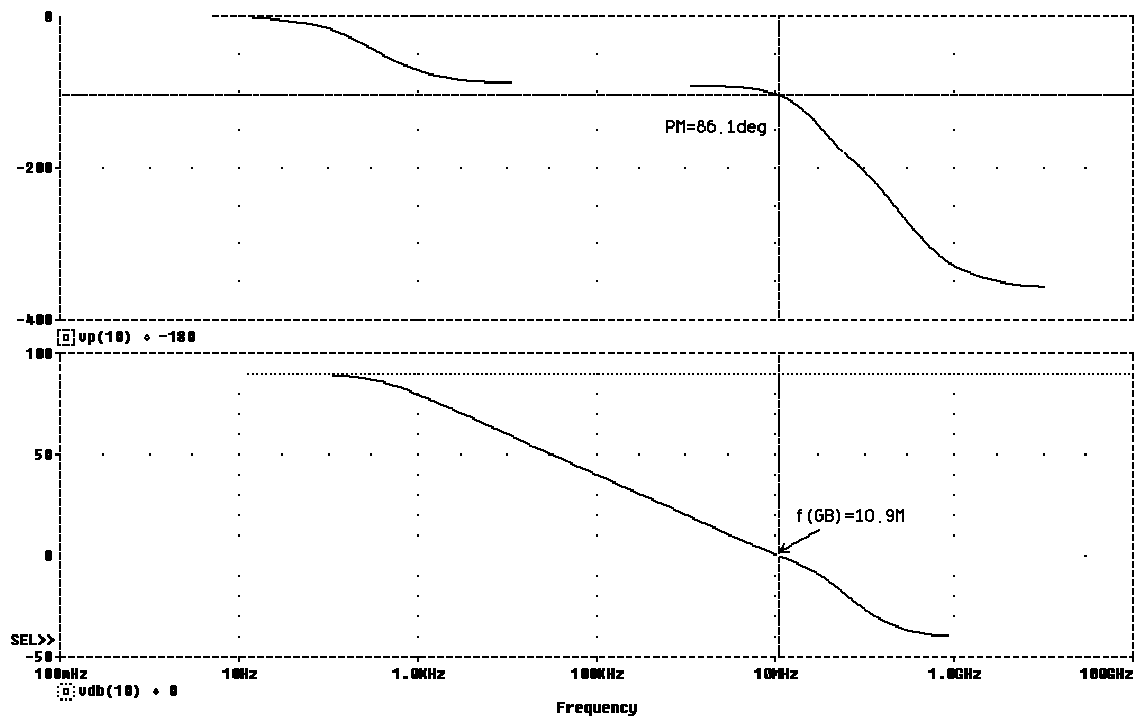
NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE

(1) 4.124E-06 (2) -4.124E-06 (3) 5.0000 (4) -5.0000

(5) 1.1562 (7) -3.4870 (8) 3.5084 (9) -3.5234

(10) -2.0125 (11) -8.248E-06 (12) 0.0000 (13) -2.0182

(14) .6098 (6a) -3.4843 (6b) -3.4843



8.0 Process and Temperature Independent Opamp Design Using Widlar Current Source

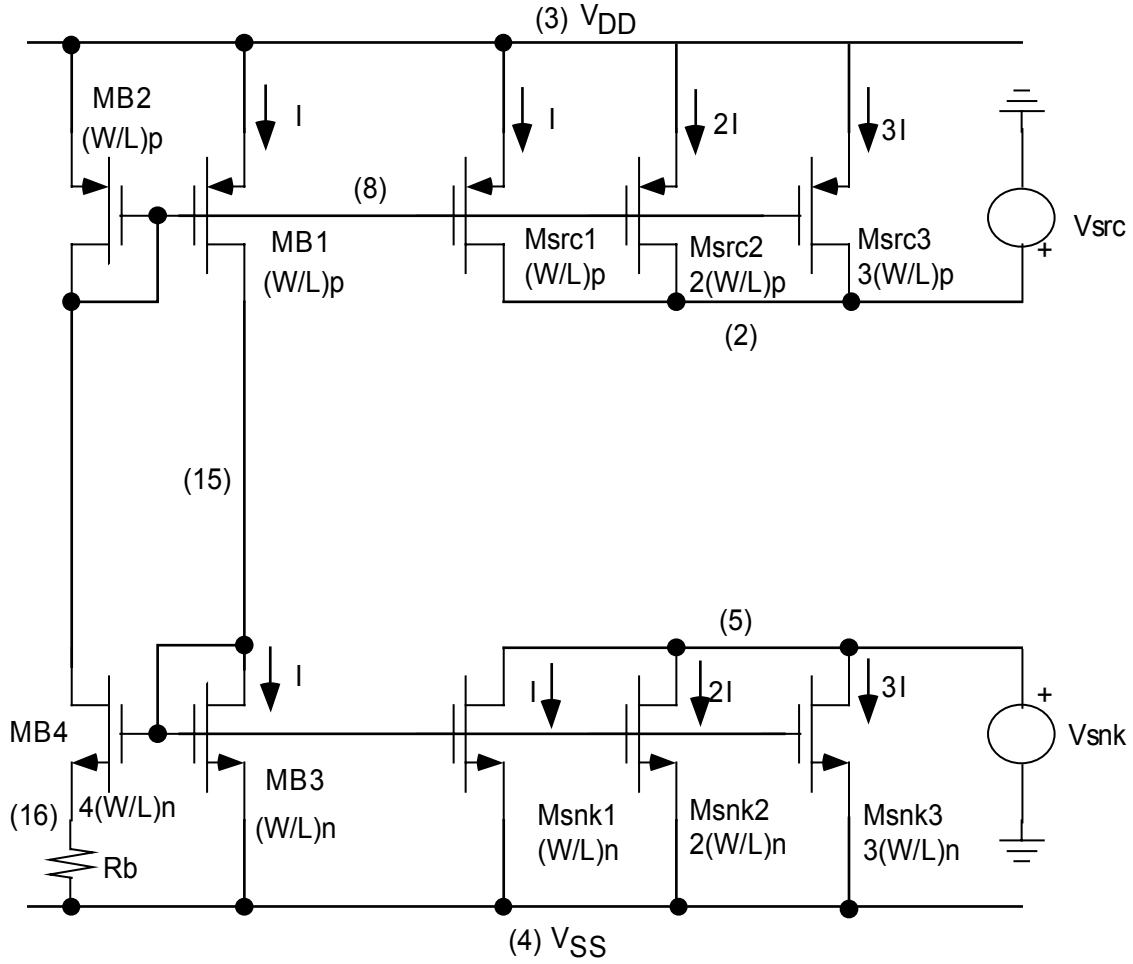


Figure 12

$$I_{D3} = I_{D4} = I$$

$$V_{GS3} = V_{GS4} + IR_b$$

Subtracting the threshold voltage V_{TN0} (neglecting body effect) from both sides, one obtains:

$$V_{GS3} - V_{TN0} = V_{GS4} - V_{TN0} + IR_b$$

$$\sqrt{\frac{2I}{K_N(W/L)_3}} = \sqrt{\frac{2I}{K_N(W/L)_4}} + IR_b$$

Solve for R_b ,

$$\frac{2}{\sqrt{2K_N(W/L)_3 I}} \left[1 - \sqrt{\frac{(W/L)_3}{(W/L)_4}} \right] = R_b$$

or

$$g_{m3} = \frac{2 \left[1 - \sqrt{\frac{(W/L)_3}{(W/L)_4}} \right]}{R_b}$$

$$g_{m3} = \frac{1}{R_b}; \text{ If } (W/L)_4 = 4(W/L)_3$$

Thus g_{m3} is determined by geometric ratio only. It is independent of power supply voltage, process parameter, and temperature. This is only true to the first order of approximation, since the body effect is neglected. In addition all other transconductance are also stabilized since all transistor currents are derived from the same biasing network. That is,

$$g_{mi} = \sqrt{\frac{(W/L)_i I_{Di}}{(W/L)_3 I_{D3}}} g_{m3}; \text{ for n - channel transistor}$$

$$g_{mi} = \sqrt{\frac{K_p (W/L)_i I_{Di}}{K_N (W/L)_3 I_{D3}}} g_{m3}; \text{ for p - channel transistor}$$

Design a 10uA widlar current source with the minimum transistor sizes for biasing an opamp circuit. Assuming all transistors are of the same length $L=6.6\mu$. The minimum width corresponding to $(W/L)=1$ and $\lambda = 0.6$ is obtained as follows:

$$\frac{W}{L_{eff}} = \frac{W}{L - 2LD} = \frac{W}{6.6\mu - 2(0.5)} = 1$$

$$W \approx 5.4\mu$$

The minimum W for the widlar current source is $2(5.4\mu)=10.8\mu$, since the differential amplifier input stage load current is half of the widlar design current value. The minimum pmos transistor (W/L) is calculated to achieve the same transconductance. That is,

$$\left(\frac{W}{L_{eff}} \right)_p = \frac{K_N}{K_P} \left(\frac{W}{L_{eff}} \right)_N$$

$$W_p = \frac{K_N}{K_P} W_N = \frac{40\mu}{15\mu} (10.8\mu) = 28.8\mu \approx 30\mu$$

The widlar cu

* Filename="op33zab4.cir"

* Widlar Source = Supply Independent

* Input Signals

* Power Supplies

VDD 3 0 DC 5VOLT

VSS 4 0 DC -5VOLT

VSNK 5 0 DC 0VOLT

VSRC 2 0 DC 0VOLT

* Netlist for Frequency Response Measurement

MB1 15 8 3 3 PMOS1 W=30U L=6.6U
MB2 8 8 3 3 PMOS1 W=30U L=6.6U
MB3 15 15 4 4 NMOS1 W={10.8U} L=6.6U
MB4 8 15 16 4 NMOS1 W={4*10.8U} L=6.6U
Msrc1 2 8 3 3 PMOS1 W=30U L=6.6U
Msrc2 2 8 3 3 PMOS1 W={2*30U} L=6.6U
Msrc3 2 8 3 3 PMOS1 W={3*30U} L=6.6U
Msnk1 5 15 4 4 NMOS1 W=10.8U L=6.6U
Msnk2 5 15 4 4 NMOS1 W={2*10.8U} L=6.6U
Msnk3 5 15 4 4 NMOS1 W={3*10.8U} L=6.6U
Rb 16 4 20K

* SPICE Parameters

.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

* Analysis

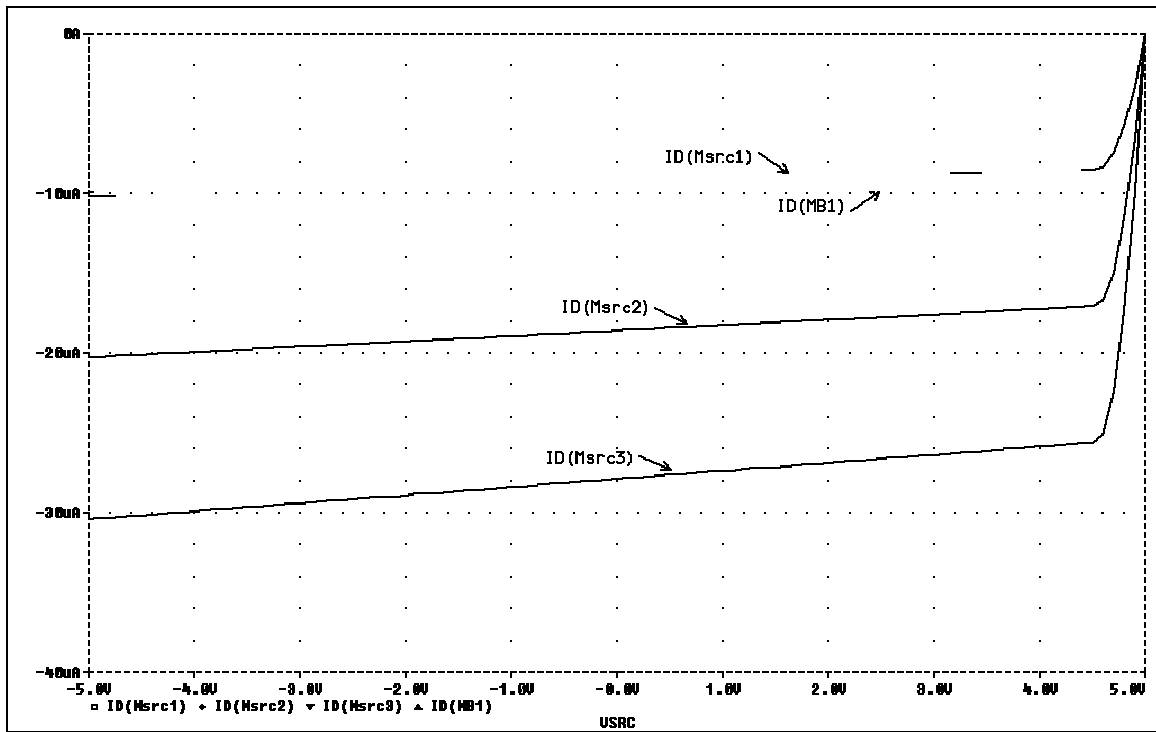
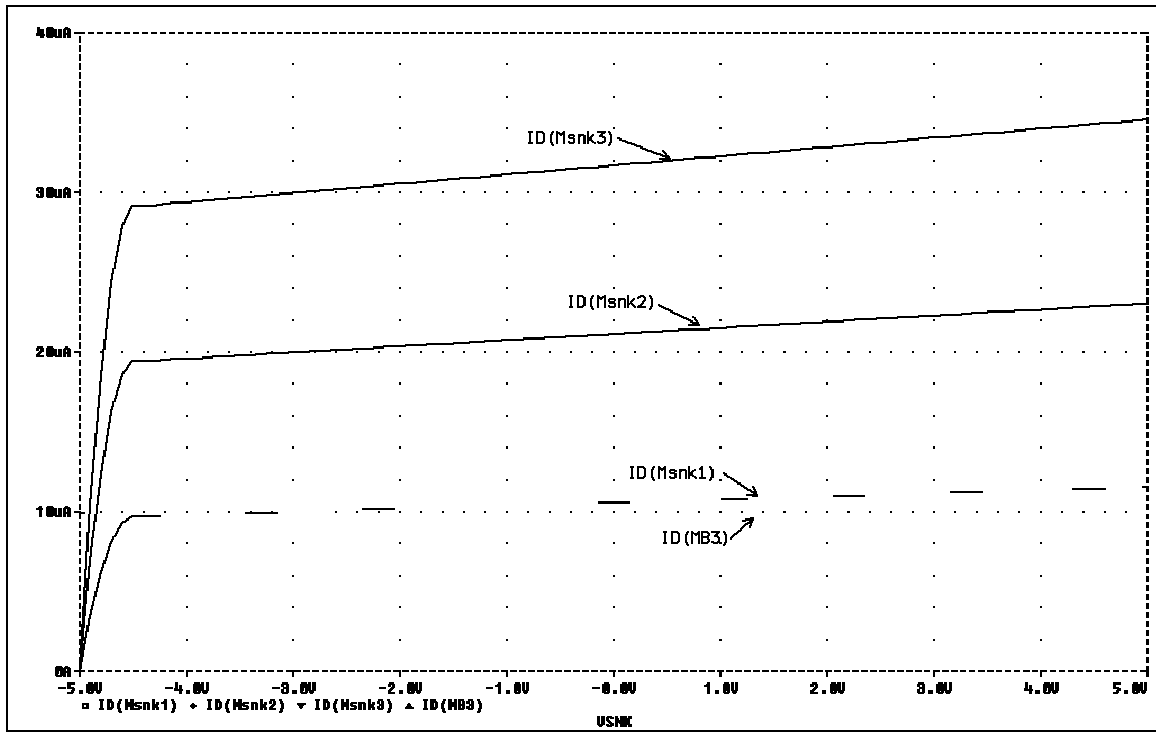
.PROBE

.OP

.DC VSNK -5V 5V .1V

*.DC VSRC -5V 5V .1V

.END



NAME	MB1	MB2	MB3	MB4	Msrc1
MODEL	PMOS1	PMOS1	NMOS1	NMOS1	PMOS1
ID	-9.89E-06	-8.70E-06	9.89E-06	8.70E-06	-9.30E-06
VGS	-1.46E+00	-1.46E+00	1.50E+00	1.33E+00	-1.46E+00
VDS	-8.50E+00	-1.46E+00	1.50E+00	8.37E+00	-5.00E+00
VBS	0.00E+00	0.00E+00	0.00E+00	-1.74E-01	0.00E+00
VTH	-1.00E+00	-1.00E+00	1.00E+00	1.11E+00	-1.00E+00
VDSAT	-4.59E-01	-4.59E-01	4.99E-01	2.20E-01	-4.59E-01

NAME	Msrc2	Msrc3	Msnk1	Msnk2	Msnk3
MODEL	PMOS1	PMOS1	NMOS1	NMOS1	NMOS1
ID	-1.86E-05	-2.79E-05	1.06E-05	2.11E-05	3.17E-05
VGS	-1.46E+00	-1.46E+00	1.50E+00	1.50E+00	1.50E+00
VDS	-5.00E+00	-5.00E+00	5.00E+00	5.00E+00	5.00E+00
VBS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
VTH	-1.00E+00	-1.00E+00	1.00E+00	1.00E+00	1.00E+00
VDSAT	-4.59E-01	-4.59E-01	4.99E-01	4.99E-01	4.99E-01

9.0 Inferred Biasing

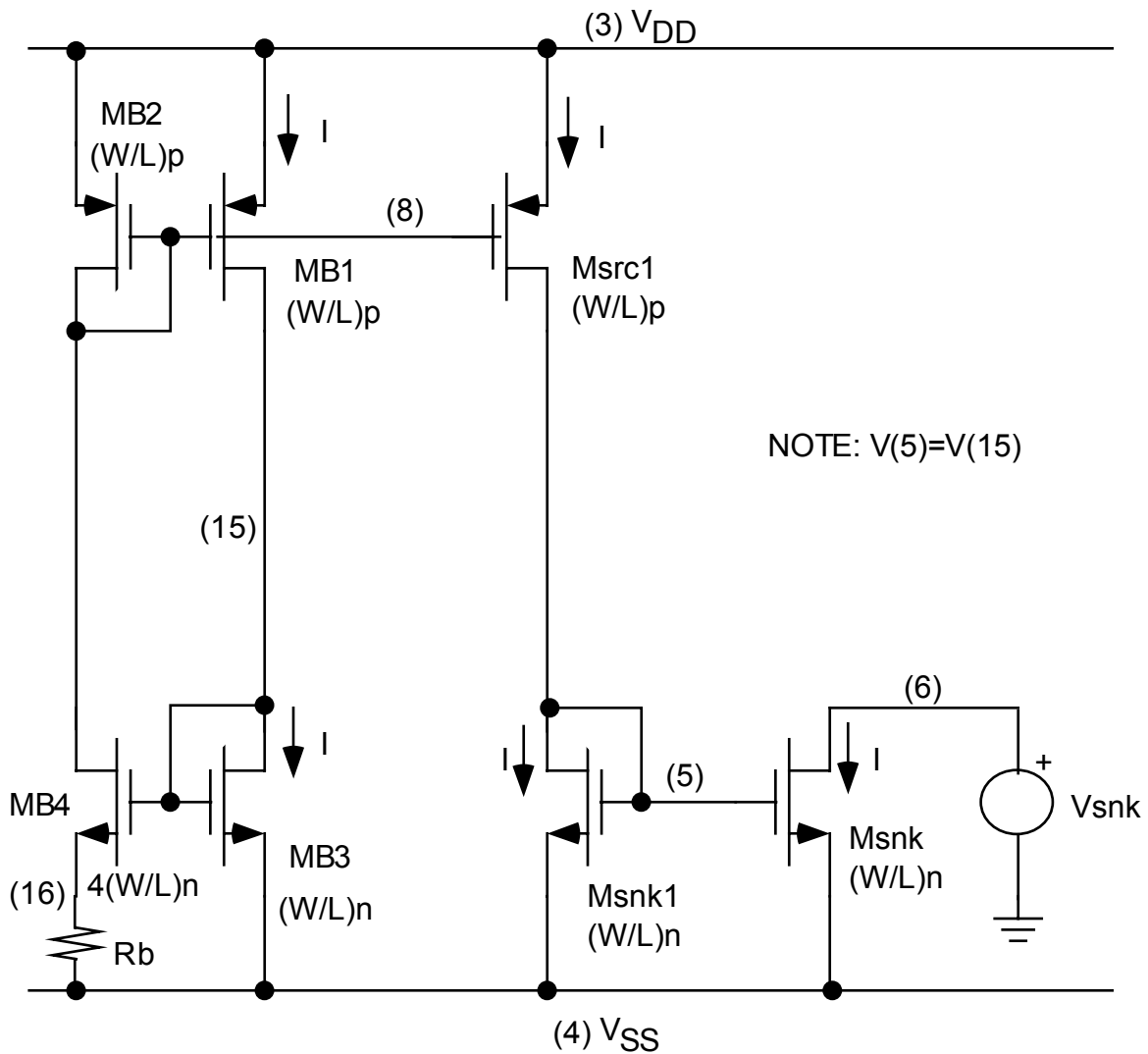


Figure 12a

* Filename="op33zab5.cir"
 * Widlar Source = Supply Independent
 * Input Signals

* Power Supplies
 VDD 3 0 DC 5VOLT
 VSS 4 0 DC -5VOLT

VSNK 6 0 DC 0VOLT

* Netlist for Frequency Response Measurement

MB1 15 8 3 3	PMOS1 W=30U	L=6.6U
MB2 8 8 3 3	PMOS1 W=30U	L=6.6U

```

MB3 15 15 4 4 NMOS1 W={10.8U} L=6.6U
MB4 8 15 16 4 NMOS1 W={4*10.8U} L=6.6U
Msrc1 5 8 3 3 PMOS1 W=30U L=6.6U
Msnk1 5 5 4 4 NMOS1 W=10.8U L=6.6U
Msnk 6 5 4 4 NMOS1 W=10.8U L=6.6U

```

```
Rb 16 4 20K
```

```
* SPICE Parameters
```

```

.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

```

```
* Analysis
```

```

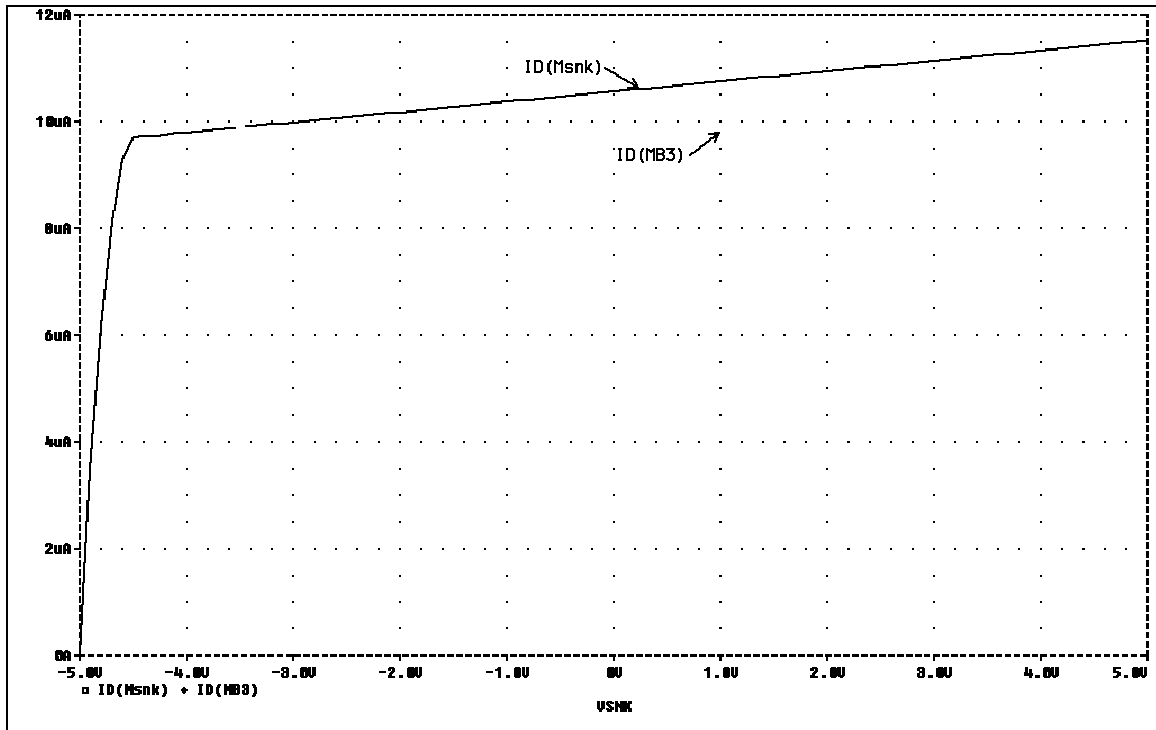
.PROBE
.OP
.DC VSNK -5V 5V .1V
*.DC VSRC -5V 5V .1V
.END

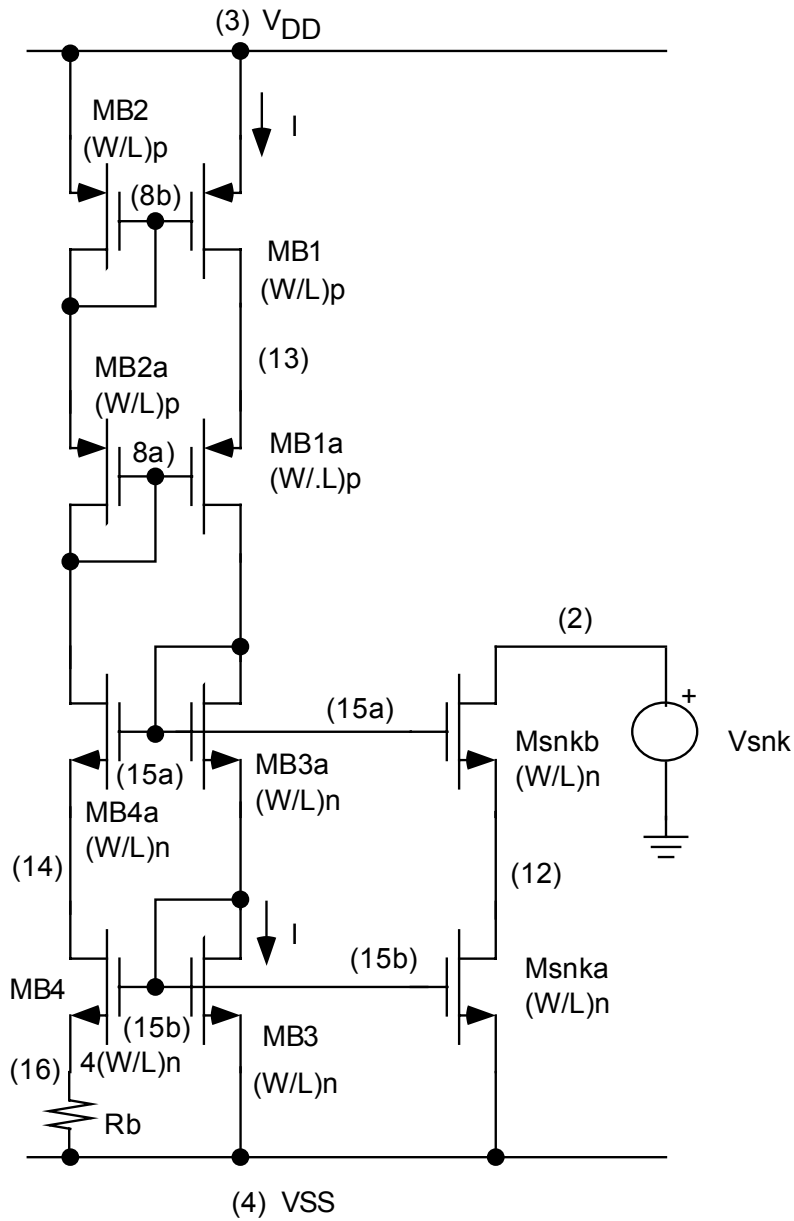
```

```
NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE
```

```
( 3) 5.0000 ( 4) -5.0000 ( 5) -3.5010 ( 6) 0.0000
```

```
( 8) 3.5413 ( 15) -3.5010 ( 16) -4.8260
```





10.0 Cascode Widlar Current Sink

Figure 12b

```

* Filename="op33zab6.cir"
* Widlar Source = Supply Independent
* Input Signals

* Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC -5VOLT

VSNK 2 0 DC 0VOLT

* Netlist for Frequency Response Measurement

MB1 13 8b 3 3      PMOS1 W=30U      L=6.6U
MB1a 15a 8a 13 13  PMOS1 W=30u      L=6.6U
MB2 8b 8b 3 3      PMOS1 W=30U      L=6.6U
MB2a 8a 8a 8b 8b   PMOS1 W=30U      L=6.6U
MB3 15b 15b 4 4     NMOS1 W={10.8U}   L=6.6U
MB3a 15a 15a 15b 4 NMOS1 W=10.8U     L=6.6U
MB4 14 15b 16 4     NMOS1 W={4*10.8U} L=6.6U
MB4a 8a 15a 14 4    NMOS1 W=10.8U     L=6.6U
Msnka 12 15b 4 4    NMOS1 W=10.8U     L=6.6U
Msnkb 2 15a 12 4    NMOS1 W=10.8U     L=6.6U

Rb 16 4 15.5K

* SPICE Parameters
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

* Analysis
.PROBE
.OP
.DC VSNK -5V 5V .1V
.TF V(2) VSNK
.END

****  SMALL-SIGNAL CHARACTERISTICS

V(2)/VSNK = 1.000E+00

INPUT RESISTANCE AT VSNK = 1.489E+09

OUTPUT RESISTANCE AT V(2) = 0.000E+00

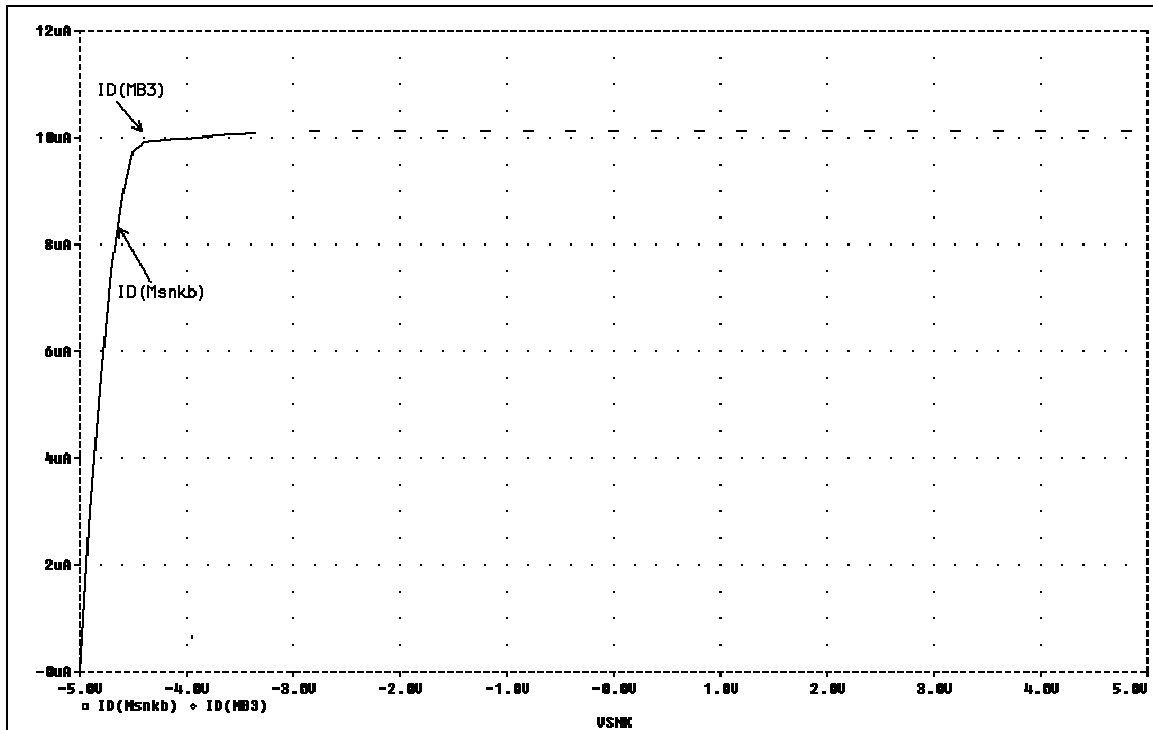
```

NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE

(2) 0.0000 (3) 5.0000 (4) -5.0000 (12) -3.4910

(13) 3.4907 (14) -3.4842 (16) -4.8434 (8a) 2.0117

(8b) 3.5058 (15a) -1.3184 (15b) -3.4956



11.0 Opamp Design with Process and Temperature Independent Implementation 1

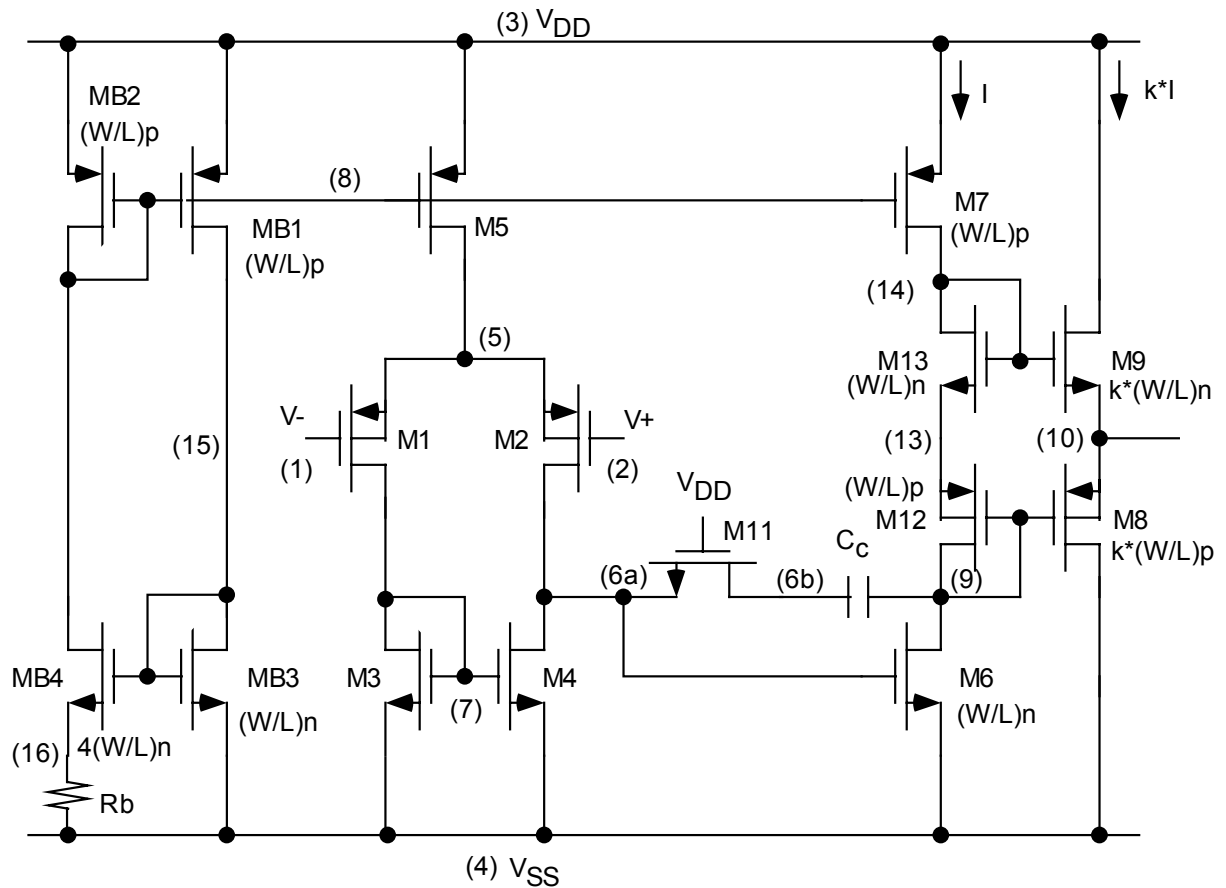


Figure 12c

```
* Filename="op33zab3.cir"
* MOS Diff Amp with PMOS Input and Current Mirror Load
* Input Signals
VID 11 0 DC -8.2484uV AC 1V
E- 1 12 11 0 -0.5
E+ 2 12 11 0 0.5
VIC 12 0 DC 0V

* Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC -5VOLT

* Netlist for Frequency Response Measurement
M1 7 1 5 5      PMOS1      W={4*36.6U}   L=6.6U
```

```

M2 6a 2 5 5    PMOS1    W={4*36.6U}  L=6.6U
M3 7 7 4 4    NMOS1    W=5.4U      L=6.6U
M4 6a 7 4 4    NMOS1    W=5.4U      L=6.6U
M5 5 8 3 3    PMOS1    W=30U       L=6.6U
M6 9 6a 4 4    NMOS1    W={32.4U}   L=6.6U
M7 14 8 3 3    PMOS1    W={90U}     L=6.6U
M8 4 9 10 10   PMOS1    W={3*90U}   L=6.6U
M9 3 14 10 4   NMOS1    W={3*32.4U} L=6.6U
M11 6b 3 6a 4  NMOS1    W=6U        L=27U
M12 9 9 13 13  PMOS1    W=90U       L=6.6U
M13 14 14 13 4 NMOS1    W=32.4U     L=6.6U
MB1 15 8 3 3   PMOS1    W=30U       L=6.6U
MB2 8 8 3 3    PMOS1    W=30U       L=6.6U
MB3 15 15 4 4  NMOS1    W={10.8U}   L=6.6U
MB4 8 15 16 4  NMOS1    W={4*10.8U} L=6.6U
Rb 16 4 19K
Cc 9 6b 1pF

```

* SPICE Parameters

```

.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

```

* Analysis

```

.PROBE
.DC VID -5V 5V .1V
.AC DEC 10 0.1HZ 10000MegHz
.TF V(10) VID
.END

```

Pspice simulation results:

$$A_{v_0} = 3.180E + 4; PM = 88.5^\circ; f_{GB} = 9.43M; R_o = 1.113E + 3$$

**** SMALL-SIGNAL CHARACTERISTICS

$$V(10)/VID = 3.180E+04$$

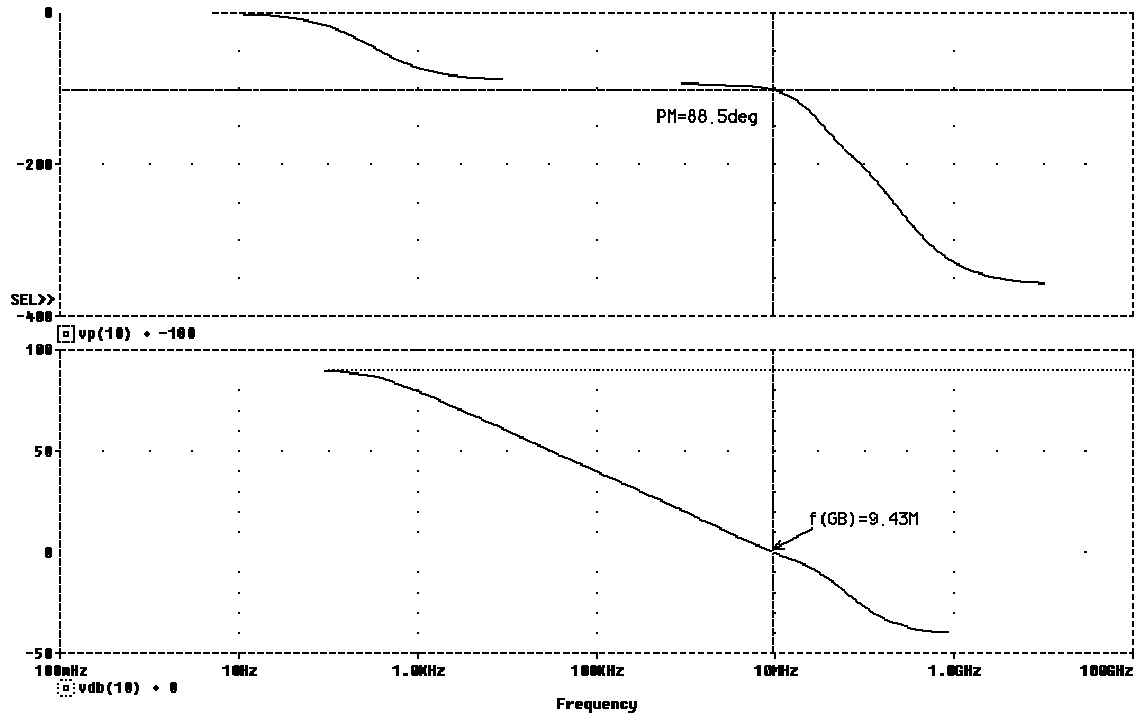
$$\text{INPUT RESISTANCE AT VID} = 1.000E+20$$

$$\text{OUTPUT RESISTANCE AT V(10)} = 1.133E+03$$

NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE

$$(\ 1) 4.124E-06 \ (\ 2) -4.124E-06 \ (\ 3) \ 5.0000 \ (\ 4) -5.0000$$

(5) 1.1533 (7) -3.4964 (8) 3.5174 (9) -3.5295
 (10) -2.0277 (11)-8.248E-06 (12) 0.0000 (13) -2.0334
 (14) .5814 (15) -3.4753 (16) -4.8170 (6a) -3.4936
 (6b) -3.4936



12.0 Opamp Design with Process and Temperature Independent Implementation 2

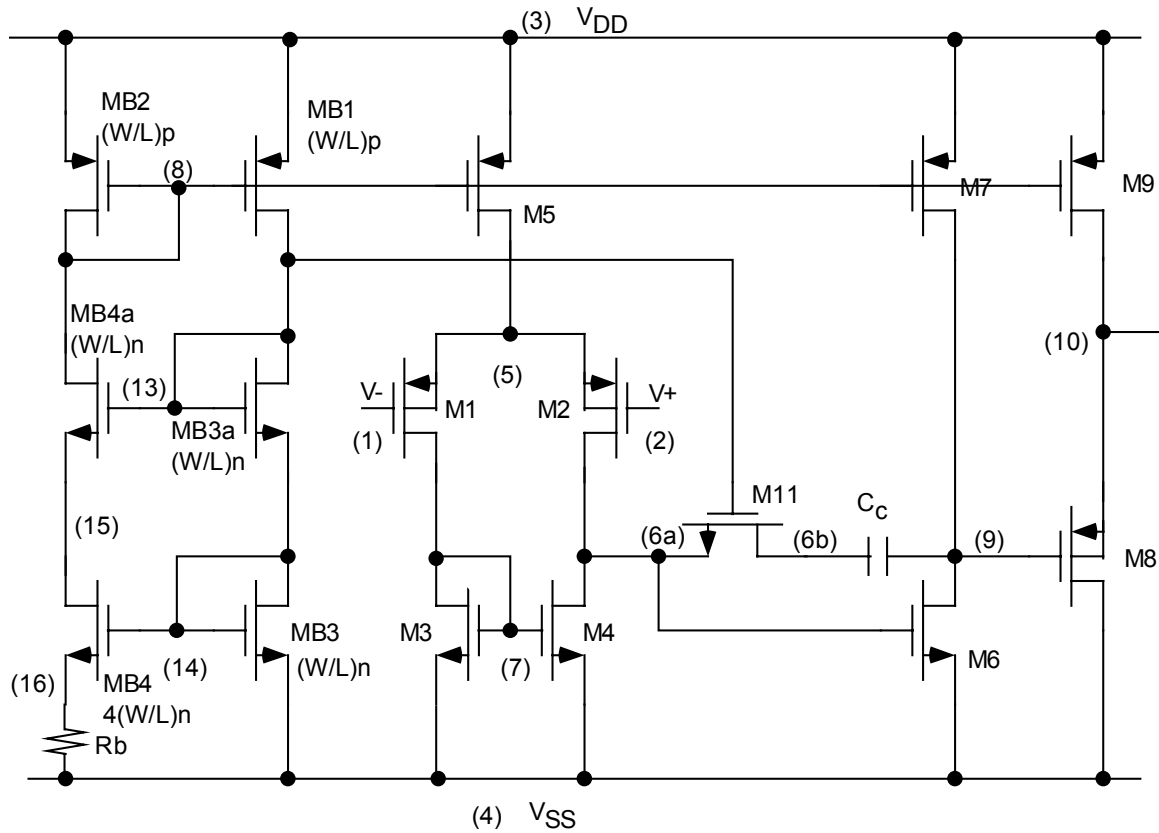


Figure 12a

```
* Filename="opamp33b.cir"
* MOS Diff Amp with PMOS Input and Current Mirror Load
* Input Signals
VID 11 0 DC -8.2484uV AC 1V
E- 1 12 11 0 -0.5
E+ 2 12 11 0 0.5
VIC 12 0 DC 0V
```

```
* Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC -5VOLT
```

```
* Netlist for Frequency Response Measurement
M1 7 1 5 5 PMOS1 W={4*36.6U} L=6.6U
M2 6a 2 5 5 PMOS1 W={4*36.6U} L=6.6U
M3 7 7 4 4 NMOS1 W=5.4U L=6.6U
M4 6a 7 4 4 NMOS1 W=5.4U L=6.6U
M5 5 8 3 3 PMOS1 W=30U L=6.6U
```

M6 9 6a 4 4	NMOS1	W={32.4U}	L=6.6U
M7 9 8 3 3	PMOS1	W={90U}	L=6.6U
M8 4 9 10 10	PMOS1	W=873.6U	L=6.6U
M9 10 8 3 3	PMOS1	W=300U	L=6.6U
M11 6b 13 6a 4	NMOS1	W={20.4U}	L=6.6U
MB1 13 8 3 3	PMOS1	W=30U	L=6.6U
MB2 8 8 3 3	PMOS1	W=30U	L=6.6U
MB3a 13 13 14 4	NMOS1	W=10.8U	L=6.6U
MB3 14 14 4 4	NMOS1	W=10.8U	L=6.6U
MB4a 8 13 15 4	NMOS1	W=10.8U	L=6.6U
MB4 15 14 16 4	NMOS1	W=43.2U	L=6.6U

Cc 9 6b 1pF

*External Bias Resistor

Rb 16 4 {17.5K}

* SPICE Parameters

```
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
```

* Analysis

```
.DC VID -5V 5V .1V
.AC DEC 10 0.1HZ 10000MegHz
.TF V(10) VID
.PROBE
.END
```

Pspice simulation results:

$$A_{v_0} = 3.790E + 4; PM = 83^\circ; f_{GB} = 8.65M; R_o = 1.379E + 3$$

**** SMALL-SIGNAL CHARACTERISTICS

$$V(10)/VID = 3.790E+04$$

$$\text{INPUT RESISTANCE AT VID} = 1.000E+20$$

$$\text{OUTPUT RESISTANCE AT V(10)} = 1.379E+03$$

NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE

(1) 4.155E-06 (2) -4.155E-06 (3) 5.0000 (4) -5.0000

(5) 1.1520 (7) -3.5007 (8) 3.5216 (9) -1.5420

(10) -2.603 (11)-8.310E-06 (12) 0.0000 (13) -1.3042

(14) -3.4895 (15) -3.4575 (16) -4.8343 (6a) -3.4979

(6b) -3.4979

$$V_{TN} = V_{TO} + \gamma \left[\sqrt{2\phi + V_{SB}} - \sqrt{2\phi_F} \right] = V_{TO} + \gamma \left[\sqrt{2\phi + V(6a) - VSS} - \sqrt{2\phi_F} \right]$$

$$= 1 + 1 \left[\sqrt{2(0.6) + (-3.4979 - (-5))} - \sqrt{2(0.6)} \right] = 1.64$$

$$R_C = r_{DS10} = \left(\frac{\partial I_D}{\partial V_{DS}} \right)^{-1} = \frac{1}{K_N (W/L) (V_{GS} - V_{TN})} = \frac{1}{K_N (W/L) (V(13) - V(6a) - V_{TN})}$$

$$(W/L) = \frac{1}{K_N R_C (V(13) - V(6a) - V_{TN})} = \frac{1}{40E-6 (13.25E+3) (-1.3042 - (-3.4979) - 1.64)} = 3.4 \approx \frac{20.4u}{6.6u}$$

