Design Procedure for Two-Stage CMOS Opamp With Flexible Noise-Power Balancing Scheme

Jirayuth Mahattanakul, *Member, IEEE,* and Jamorn Chutichatuporn

***Abstract*—This paper presents a basic two-stage CMOS opamp design procedure that provides the circuit designer with a means to strike a balance between two important characteristics in electronic circuit design, namely noise performance and power consumption. It is shown in this paper that, unlike the previously reported design procedures, the proposed design step allows opamp designers to trade between noise performance and power consumption with greater flexibility. In order to verify the viability of the proposed design step, SPICE simulation results of the opamp designed by the proposed procedure, under a variety of temperature and process conditions, are given.**

***Index Terms*—CMOS analog integrated circuits, frequency compensation, operational amplifier, poles and zeroes.**

I. Introduction

CMOS opamps are ubiquitous integral parts in various analog and mixed-signal circuits and systems. The two-stage CMOS opamp shown in Fig. 1 is widely used because of its simple structure and robustness. In designing an opamp, numerous electrical characteristics, e.g., gain-bandwidth, slew rate, common-mode range, output swing, offset, all have to be taken into consideration. Furthermore, since opamps are designed to be operated with negative-feedback connection, frequency compensation is necessary for closed-loop stability. Unfortunately, in order to achieve the required degree of stability, generally indicated by phase margin, other performance parameters are usually compromised. As a result, designing an opamp that meets all specifications needs a good compensation strategy and design methodology.

The simplest frequency compensation technique employs the Miller effect by connecting a compensation capacitor C_c across the high-gain stage. A design procedure for this type of opamp can be found in [1]. However, due to an unintentional feed-forward path through the Miller capacitor, a right-half-plane (RHP) zero is also created and the phase margin is degraded. Such a zero, however, can be removed if a proper nullifying resistor is inserted in series with the Miller capacitor [1]–[5]. A design procedure for the zero-nullification opamp can be found in [2].

It will be shown in Section III that the value of C_c is an important factor when determining noise and power, e.g., by decreasing C_c, power consumption can be reduced but at the expense of noise performance. Unfortunately, one of the necessary imposing conditions of the design procedure in [2] is C_c being much larger than the parasitic capacitance associated with the input node of the high-gain stage. This condition thus reduces one important degree-of-freedom in analog circuit design, namely the tradeoff between noise and power consumption.

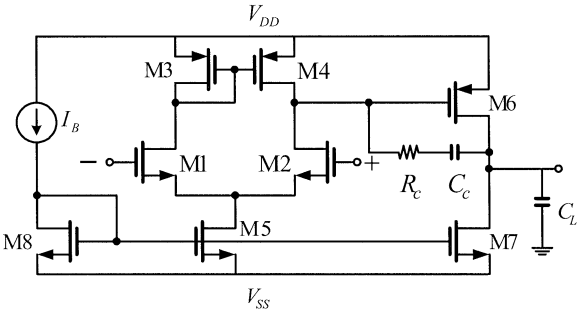

Fig. 1. Basic two-stage CMOS opamp.

In this work, it has been shown that by employing such a technique, the value of the compensation capacitor, C_c, can be made much smaller than when employing other techniques. As such, the flexibility of choosing a wider range of C_c provides the designer with a greater degree of freedom to optimize the opamp in terms of noise and power.

II. Basic Opamp Equations

For simplicity, both the mobility reduction due to the normal field and the velocity saturation effect associated with MOS devices will be neglected. The following MOSFET, strong-inversion, square-law equations:

$$I_D = \frac{\mu_{n,p} C_{\text{ox}}}{2} \left(\frac{W}{L}\right) V_{\text{eff}}^2 \tag{1}$$

$$g_m = \sqrt{2\mu_{n,p} C_{\text{ox}} \left(\frac{W}{L}\right) I_D} \tag{2}$$

$$g_m = \frac{2I_D}{V_{\text{eff}}} \tag{3}$$

where $V_{\text{eff}} = V_{GS} - V_{tn}$ for nMOS and $V_{\text{eff}} = V_{SG} - |V_{tp}|$ for PMOS, will be used throughout the paper. Strong inversion typically requires values of V_{eff} greater than approximately 200 to 250 mV for bulk MOSFET's at room temperature.

The equations for determining various opamp characteristics can be shown as follows [1]–[4].

A. Gain and Bandwidth

According to the equivalent circuit shown in Fig. 2, under typical conditions $g_{m6}R_B \gg C_{gs6}/C_c$, $g_{m6}R_A \gg C_L/C_c$ and $R_c \ll R_A, R_B$, the small-signal transfer function of the CMOS

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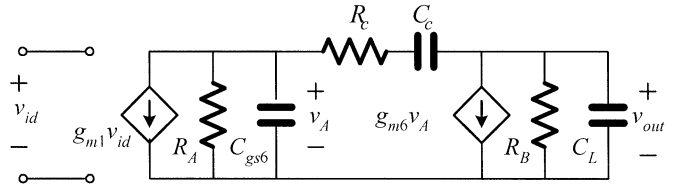

Fig. 2. Small-signal equivalent circuit of CMOS opamp in Fig. 1 where $R_A = r_{ds2}//r_{ds4}$ and $R_B = r_{ds6}/r_{ds7}$.

opamp in Fig. 1 can be shown as (4), shown at the bottom of the page, where $A_o = g_{m1}g_{m6}R_AR_B$ is the opamp dc gain.

The opamp's dominant pole frequency and unity-gain bandwidth, also commonly known as gain-bandwidth, can be found to be

$$\omega_{p1} \cong \frac{1}{g_{m6}R_AR_BC_c} \tag{5}$$

and

$$\omega_u \cong A_o\omega_{p1} = \frac{g_{m1}}{C_c} \tag{6}$$

respectively.

It can also be shown that for, $w \gg w_{p1}$, (4) can be approximated as

$$A(s) = \frac{\omega_u}{s}\frac{1 - sC_c\left(\frac{1}{g_{m6}} - R_c\right)}{1 + \frac{C_{gs6}C_L + C_{gs6}C_c + C_cC_L}{g_{m6}C_c}s + \frac{R_cC_{gs6}C_L}{g_{m6}}s^2}. \tag{7}$$

B. Output Swing

By defining $V_{\rm HR}^{\rm out}$ as the opamp headroom voltage at output, i.e.,

$$V_{\rm HR}^{\rm out+} = V_{\rm DD} - V_{\rm out(max)} \text{ and } V_{\rm HR}^{\rm out-} = V_{\rm out(min)} - V_{\rm SS}$$

according to Fig. 1, it is easy to show that

$$V_{\rm HR}^{\rm out+} = V_{\rm eff6} \tag{8}$$
$$V_{\rm HR}^{\rm out-} = V_{\rm eff7}. \tag{9}$$

C. Common-Mode Range

If we define $V_{\rm HR}^{\rm CM}$ as the opamp head room voltage of the input common-mode range, i.e.,

$$V_{\rm HR}^{CM+} = V_{\rm DD} - V_{CM(\max)} \text{ and } V_{\rm HR}^{CM-} = V_{CM(\min)} - V_{ss}$$

according to Fig. 1, it can be shown that

$$V_{\rm HR}^{CM+} = V_{\rm eff3} - V_{tn} \tag{10}$$
$$V_{\rm HR}^{CM-} = V_{\rm eff5} + V_{tn} + V_{\rm eff1,2}. \tag{11}$$

D. Internal Slew Rate

The slew rate associated with C_c can be found to be

$$SR = \frac{I_{D5}}{C_c}. \tag{12}$$

E. External Slew Rate

The slew rate associated with C_L can be found to be

$$SR = \frac{I_{D7} - I_{D5}}{C_L}. \tag{13}$$

Combining (12) and (13), we obtain

$$I_{D7} = SR(C_c + C_L). \tag{14}$$

Combining (3), (6), (12), and $I_{D5} = 2I_{D1} = 2I_{D2}$ yields

$$V_{\rm eff1,2} = \frac{SR}{\omega_u}. \tag{15}$$

F. Offset Voltage Minimization

Systematic offset is caused by current imbalance in the output stage, i.e., between I_{D6} and I_{D7}, when there is no input voltage. Under such a condition, $I_{D3} = I_{D4} = I_{D5}/2$ and V_{SD4} is thus forced to be equal to V_{SD3}. Since $V_{SG6} = V_{SD4}$ and $V_{SD3} = V_{SG3}$, we then have $V_{SG3} = V_{SG6}$, which implies that $I_{D6}/I_{D3} = 2I_{D6}/I_{D5} = (W/L)_6/(W/L)_3$.

Now considering M_5 and M_7, we have $I_{D7}/I_{D5} = (W/L)_7/(W/L)_5$. As a result, the current imbalance in the output stage can be minimized by the following condition:

$$\frac{\left(\frac{W}{L}\right)_{5,8}}{2\left(\frac{W}{L}\right)_{3,4}} = \frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_6} \tag{16}$$

which can be used to minimize the offset voltage.

G. Input-Referred Thermal Noise Spectral Density

The input-referred thermal noise spectral density of the two-stage opamp in Fig. 1 can be shown to be

$$S_n(f) = 4kT\left\{2\left(\frac{2}{3g_{m1,2}}\right)\right\}\left[1 + \frac{g_{m3,4}}{g_{m1,2}}\right]. \tag{17}$$

From (3), (10), and (12), we obtain

$$g_{m3} = \frac{C_cSR}{\left(V_{\rm HR}^{CM+} + V_{tn}\right)}. \tag{18}$$

Substitute (6) and the above equation into (17) yields

$$S_n(f) = 4kT\left\{2\left(\frac{2}{3\omega_uC_c}\right)\right\}\left[1 + \frac{SR}{\omega_u\left(V_{\rm HR}^{CM+} + V_{tn}\right)}\right]. \tag{19}$$

$$\frac{V_{\rm out}}{V_{id}} = A_o\frac{1 - sC_c\left(\frac{1}{g_{m6}} - R_c\right)}{1 + g_{m6}R_AR_BC_cs + R_AR_B(C_{gs6}C_L + C_{gs6}C_c + C_cC_L)s^2 + R_AR_BR_cC_{gs6}C_cC_Ls^3} \tag{4}$$

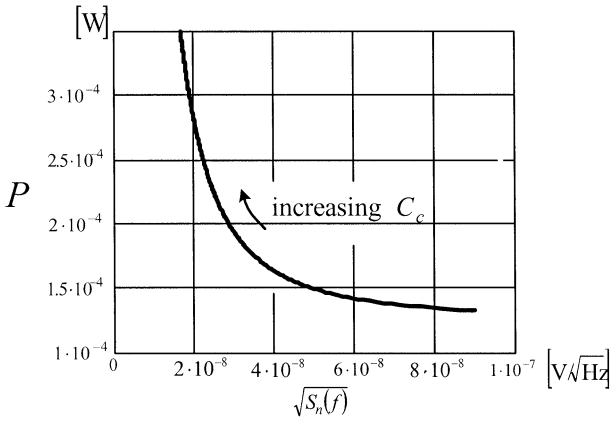

Fig. 3. Noise-spectral density versus power consumption.

III. Noise Versus Power Tradeoff

In this section, we will consider in detail the noise and power tradeoff encountered in the opamp design. The quiescent power consumption of the two-stage opamp shown in Fig. 1 can be found to be

$$P = (2I_{D5} + I_{D7})V_{\text{sup}} \tag{20}$$

where $V_{\text{sup}} = V_{\text{DD}} - V_{\text{SS}}$. Substitute (12) and (14) into the above equation gives

$$P = SR(3C_c + C_L)V_{\text{sup}}. \tag{21}$$

According to (19) and (21), Fig. 3 illustrates conflict between noise and power consumption in two-stage CMOS opamp design. For example, by decreasing C_c, power consumption can be reduced at the expense of the noise performance. Consequently, the compensation scheme that allows a wider range of C_c would provide a higher degree of freedom in noise and power tradeoff.

It should be highlighted that one of the necessary conditions of the design procedure in [2] is that $C_c \gg C_{gs6}$. This condition would clearly reduce the degree of freedom in the tradeoff between noise and power consumption.

IV. Compensation Scheme and Phase Margin Control

It can be shown that Fig. 4(a) is a circuit that corresponds to the transfer function (7), i.e., it is a small-signal circuit of the opamp in Fig. 1 in the higher frequency range where $\omega \gg \omega_{p1}$. Under the condition

$$R_c = \frac{1}{g_{m6}}\left(1 + \frac{C_L}{C_c}\right) \tag{22}$$

it can be shown that (see Appendix A) the circuit of Fig. 4(a) can be transformed into that of Fig. 4(b) where C_{gs6} and R_c are effectively connected in parallel. It is thus easy to show that

$$\frac{v_{\text{out}}}{v_{id}} = \left(\frac{\omega_u}{s}\right)\left(\frac{1}{1 + sR_cC_{gs6}}\right) \tag{23}$$

where $\omega_u = g_{m1}/C_c$ is the unity-gain frequency of an opamp. Equation (23) indicates that the condition of (22) results in a system with only one nondominant pole

$$p_{\text{nd}} = -\frac{1}{R_cC_{gs6}} = -\frac{g_{m6}}{C_{gs6}}\frac{C_c}{(C_c + C_L)} \tag{24}$$

and no finite zero.

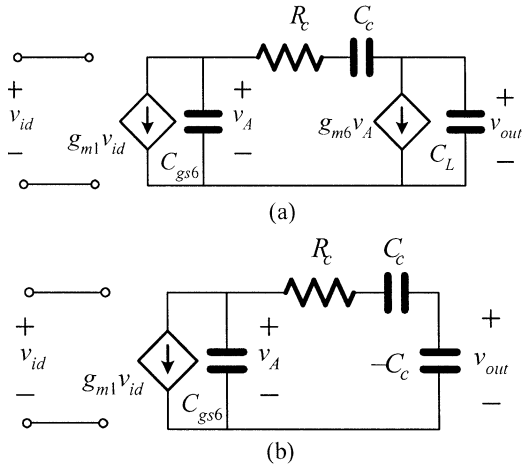

Fig. 4. High-frequency small-signal equivalent circuit of CMOS opamp in Fig. 1.

Alternatively, the above compensation scheme can be viewed as a mean to locate the extra zero and pole of the system at exactly the same location. This can be explained as follows. By substituting the condition (22) into (7), which is a transfer function of the opamp for $\omega \gg \omega_{p1}$, the zero of the transfer function can be easily identified as

$$z = -\frac{g_{m6}}{C_L} \tag{25}$$

and the nondominant poles are the roots of a polynomial

$$D(s) = 1 + \left(\frac{C_L}{g_{m6}} + \frac{C_{gs6}(C_L + C_c)}{g_{m6}C_c}\right)s + \left(\frac{C_L}{g_{m6}}\right)\left(\frac{C_{gs6}(C_L + C_c)}{g_{m6}C_c}\right)s^2 \tag{26}$$

which are exactly

$$p_2 = -\frac{g_{m6}}{C_L} \tag{27}$$

$$p_3 = -\frac{g_{m6}}{C_{gs6}}\frac{C_c}{(C_L + C_c)}. \tag{28}$$

It can be seen that the condition (22) results in the cancellation of p_2 and z. Also, p_3 is identical to the pole expressed in (24). It should be pointed out here that, unlike the analysis presented elsewhere [1]–[5], the pole location shown in (28) are the exact solutions of the second-order polynomial and no approximation is involved.

The phase margin of an opamp with one nondominant pole, considered for 100% feedback, can be shown to be

$$\phi_M = \tan^{-1}\frac{|p_{\text{nd}}|}{\omega_u}. \tag{29}$$

From (24) and (29), we obtain

$$\tan(\phi_M) = \frac{\omega_{T6}}{\omega_u}\left(\frac{C_c}{C_c + C_L}\right) \tag{30}$$

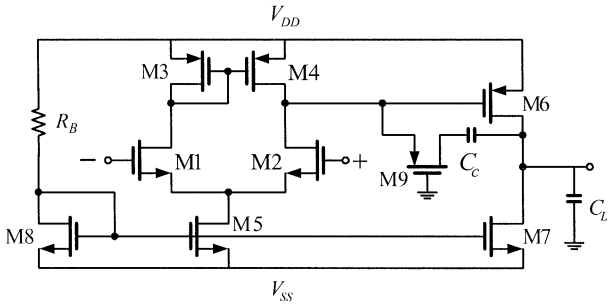

Fig. 5. Two-stage CMOS opamp.

where

$$\omega_{T6} = \frac{g_{m6}}{C_{gs6}} = \frac{3}{2}\frac{\mu_p}{L_6^2}V_{\text{eff}6} \tag{31}$$

is a transition frequency of M6 and $V_{\text{eff}6} = V_{SG6} - |V_{t6}|$ [3]. Combining (8), (30) and (31), we find that

$$L_6 = \sqrt{\frac{3}{2}\frac{\mu_p V_{\text{HR}}^{\text{out}+} C_c}{\omega_u (C_c + C_L)\tan(\phi_M)}} \tag{32}$$

is a necessary condition in our opamp design.

It is important to note that as opposed to the method in [2] the condition $C_c \gg C_{gs6}$ is not necessary for the compensation scheme presented in this section. Furthermore, for $C_L \gg C_c$, it can be shown that

$$\begin{aligned} C_c|_{\text{method in [2]}} &\gg C_c|_{\text{proposed method}} \\ &\cong \frac{2}{3}\frac{\omega_u C_L \tan(\phi_M)}{\mu_p V_{\text{HR}}^{\text{out}+}} L_6^2 \end{aligned}$$

which indicates that, compared to [2], the proposed method allows the use of smaller C_c.

V. Design Procedure

A design step for two-stage opamp (Fig. 5) can be constructed as follows.

Step 1) From (19), we have

$$C_c = \frac{16kT}{3\omega_u S_n(f)}\left[1 + \frac{SR}{\omega_u\left(V_{\text{HR}}^{CM+} + V_{tn}\right)}\right]. \tag{33}$$

Step 2) Calculate I_{D7} from (14)

$$I_{D7} = SR(C_c + C_L). \tag{34}$$

Step 3) Using (32) to calculate L_6

$$L_6 = \sqrt{\frac{3\mu_p V_{\text{HR}}^{\text{out}+} C_c}{2\omega_u (C_c + C_L)\tan(\phi_M)}}. \tag{35}$$

Step 4) Calculate $V_{\text{eff}6}$ from (8) and use the result to calculate $(W/L)_6$ from (1) yields

$$W_6 = \frac{2SR(C_c + C_L)}{\mu_p C_{\text{ox}}\left(V_{\text{HR}}^{\text{out}+}\right)^2} L_6. \tag{36}$$

Step 5) Calculate I_{D5} from (12)

$$I_{D5} = C_c SR. \tag{37}$$

Step 6) Calculate g_{m1} from (6) and use the result with $I_{D1} = I_{D2} = I_{D5}/2$ to calculate $(W/L)_{1,2}$ from (2) yields

$$\left(\frac{W}{L}\right)_{1,2} = \frac{\omega_u^2 C_c}{\mu_n C_{\text{ox}} SR}. \tag{38}$$

Step 7) Calculate $V_{\text{eff}5}$ from (11) and (15) and substitute the result into (1) gives

$$\left(\frac{W}{L}\right)_{5,8} = \frac{2SRC_c}{\mu_n C_{\text{ox}}\left(V_{\text{HR}}^{CM-} - V_{tn} - \frac{SR}{\omega_u}\right)^2}. \tag{39}$$

Step 8) Calculate $(W/L)_7$ from the basic relation $(I_{D7}/I_{D5}) = ((W/L)_7/(W/L)_5)$ in conjunction with (12) and (13) yields

$$\left(\frac{W}{L}\right)_7 = \left(\frac{C_c + C_L}{C_c}\right)\left(\frac{W}{L}\right)_{5,8}. \tag{40}$$

Step 9) Calculate $(W/L)_{3,4}$ from (16)

$$\left(\frac{W}{L}\right)_{3,4} = \frac{\left(\frac{W}{L}\right)_6}{2\left(\frac{W}{L}\right)_7}\left(\frac{W}{L}\right)_{5,8}. \tag{41}$$

Step 10) Calculate R_c from (22) and use (3), (14) and the triode equation

$$R_c = \frac{1}{\mu_p C_{\text{ox}}\left(\frac{W}{L}\right)_9 V_{\text{eff}9}}$$

where $V_{\text{eff}9} = V_{\text{DD}} - V_{\text{HR}}^{\text{out}+} - 2|V_{tp}|$ to calculate $(W/L)_9$ gives

$$\left(\frac{W}{L}\right)_9 = \frac{2C_c SR}{\mu_p C_{\text{ox}} V_{\text{HR}}^{\text{out}+}\left(V_{\text{DD}} - V_{\text{HR}}^{\text{out}+} - 2|V_{tp}|\right)}. \tag{42}$$

The design steps outlined above can be summarized as shown in Table I.

VI. Simulation Results

For the process parameters shown in Table II and opamp specification shown in Table III, design parameters of opamp in Fig. 4 are obtained from our proposed procedure (Table I) and the procedure proposed in [2]. These parameters are shown in Table IV for $C_c = 2.5$ and 0.5 pF. HSPICE simulation results of the designed opamps are shown in Tables V and VI.

It can be observed from Table V that for $C_c = 2.5$ pF, the characteristics of both opamps meet all the specifications. However in the case for $C_c = 0.5$ pF, while the characteristics of the opamp designed by the proposed procedure pass all the specifications, such is not the case for those of the opamp designed by the procedure in [2], notably the phase margin.

It should be noted that, as expected, by using the same value of C_c, there is no improvement in terms of noise performance

TABLE I
OPAMP DESIGN STEP

Step 1	$C_c = \frac{16kT}{3\omega_u S_n(f)}\left[1+\frac{SR}{\omega_u(V_{HR}^{\mathrm{CM}+}+V_{tn})}\right]$
Step 2	$I_{D7} = SR(C_c + C_L)$
Step 3	$L_6 = \sqrt{\frac{3\mu_p V_{HR}^{\mathrm{out}+} C_c}{2\omega_u(C_c+C_L)\tan(\phi_M)}}$
Step 4	$W_6 = \frac{2SR(C_c+C_L)}{\mu_p C_{ox}\left(V_{HR}^{\mathrm{out}+}\right)^2} L_6$
Step 5	$I_{D5} = C_c SR$
Step 6	$(W/L)_{1,2} = \frac{\omega_u^2 C_c}{\mu_n C_{ox} SR}$
Step 7	$(W/L)_{5,8} = \frac{2SRC_c}{\mu_n C_{ox}\left(V_{HR}^{\mathrm{CM}-} - V_{tn} - SR/\omega_u\right)^2}$
Step 8	$(W/L)_7 = \left(\frac{C_c+C_L}{C_c}\right)(W/L)_{5,8}$
Step 9	$(W/L)_{3,4} = \frac{(W/L)_6}{2(W/L)_7}(W/L)_{5,8}$
Step 10	$(W/L)_9 = \frac{2C_c SR}{\mu_p C_{ox} V_{HR}^{\mathrm{out}+}\left(V_{DD} - V_{HR}^{\mathrm{out}+} - 2\lvert V_{tp}\rvert\right)}$

TABLE II
PROCESS PARAMETERS (0.5 MICRON HP'S CMOS14TB) [6]

Process parameters	NMOS	PMOS
$\mu\ (\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s})$	506.0	115.6
T_{ox} (m)	9.6×10^{-9}	9.6×10^{-9}
V_t (V)	0.711	-0.901

TABLE III
SPECIFICATION OF CMOS OPAMP

Electrical parameters	Expected
Supply voltages	± 2.5 V
Load capacitance: C_L (pF)	5
DC gain: A_o (dB)	≥ 80
Unity-gain frequency: f_u (MHz)	5
Phase margin: ϕ_M (deg)	65
Slew rate: SR (V/μsec)	+5/-5
Input common range: CMR (V)	+1/-1
Output swing: OS (V)	+2/-2

when using the method proposed. However, by using the proposed method, the value of C_c can be made much smaller than the method in [2] without affecting the phase margin. This provides the designer with a higher degree of freedom to optimize the opamp in terms of noise and power.

TABLE IV
DESIGN PARAMETERS

Procedure	From [2]		Proposed		Unit
C_C	2.5	0.5	2.5	0.5	pF
$(W/L)_{1,2}$	4/1	1/1	4/1	1/1	μm/μm
$(W/L)_{3,4}$	12/1	4/1	3/1	1/1	μm/μm
$(W/L)_{5,8}$	1.5/1	1/3	1.5/1	1/3	μm/μm
$(W/L)_6$	143/2	195/2	110/4.5	31/2.5	μm/μm
$(W/L)_7$	4/1	3/1	4.5/1	3/1	μm/μm
$(W/L)_9$	20/1	26/1	10/1	1/2	μm/μm

TABLE V
SIMULATION RESULTS FOR $C_c = 2.5$ pF

Design procedure	From [2]	Proposed
A_o (dB)	83.9	83.1
f_u (MHz)	5.4	5.44
ϕ_M (deg)	66	67
SR (V/μsec)	6.24/-5.42	6.37/-5.36
CMR (V)	2.1/-2.2	2.2/-2.12
OS (V)	2.2/-2.2	2.2/-2.19
Input-referred noise @ 1MHz	21 nV/$\sqrt{\text{Hz}}$	18 nV/$\sqrt{\text{Hz}}$
Total area (μm^2)	1040	1220
I_{D5}(μA)	15.35	15.35
I_{D7}(μA)	42.97	48.40
Power consumption	367 μW	394 μW

TABLE VI
SIMULATION RESULTS FOR $C_c = 0.5$ pF

Design procedure	From [2]	Proposed
A_o (dB)	85.4	85.1
f_u (MHz)	**4.74**	6.0
ϕ_M (deg)	**46**	65
SR (V/μsec)	5.62/-5.2	6.0/-5.2
CMR (V)	2.15/-2.2	2.1/-2.18
OS (V)	2.3/-2.25	2.16/-2.2
Input-referred noise @ 1MHz	44 nV/$\sqrt{\text{Hz}}$	38 nV/$\sqrt{\text{Hz}}$
Total area (μm^2)	571	234
I_{D5} (μA)	3.03	3.03
I_{D7} (μA)	35.33	35.33
Power consumption	207 μW	207 μW

Fig. 6 shows a two-stage opamp with robust bias part [4]. For $(W/L)_{10} = (W/L)_{11} = (W/L)_{12} = (W/L)_{13}$ and $(W/L)_6/(W/L)_{13} = (W/L)_7/(W/L)_8$, it can be shown that

$$V_{\mathrm{eff}6} = V_{\mathrm{eff}9} = V_{\mathrm{eff}10-13}. \tag{43}$$

If $(W/L)_{14}$ is chosen to be $4(W/L)_8$, we have

$$R_B = \frac{1}{\sqrt{2\mu_n C_{\mathrm{ox}}\left(\frac{W}{L}\right)_8 C_c SR}} \tag{44}$$

$$\left(\frac{W}{L}\right)_9 = \frac{\left(\frac{W}{L}\right)_6}{1+\frac{C_L}{C_C}}. \tag{45}$$

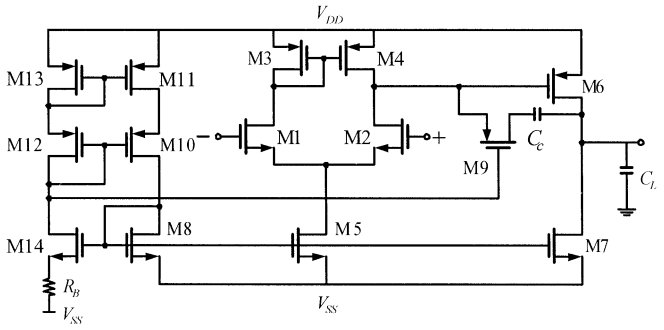

Fig. 6. Two-stage CMOS opamp with robust bias circuit.

TABLE VII
DESIGN PARAMETERS OF OPAMP IN FIG. 6

C_c	0.5	pF
R_B	62	kΩ
$(W/L)_{1,2}$	1/1	μm/μm
$(W/L)_{3,4}$	1/1	μm/μm
$(W/L)_{5,8}$	1/3	μm/μm
$(W/L)_6$	31/2.5	μm/μm
$(W/L)_7$	3/1	μm/μm
$(W/L)_9$	1/1	μm/μm
$(W/L)_{10\text{-}13}$	1/1	μm/μm
$(W/L)_{14}$	2.5/2	μm/μm

TABLE VIII
PROCESS AND TEMPERATURE VARIATION

Parameter variation	Typical	Slow	Fast
Supply voltages (V)	± 2.5	± 2.25	± 2.75
Temperature (°C)	25	100	0
T_{ox} (nm)	9.6	10.17	9.02
C_c (pF)	0.5	0.47	0.53
V_{tn} (V)	0.711	0.8	0.6
V_{tp} (V)	-0.901	-1.0	-0.8

TABLE IX
SIMULATION RESULTS FOR PROCESS AND TEMPERATURE VARIATION

Design procedure	Typical	Slow	Fast
A_0 (dB)	85	84.2	86
f_u (MHz)	6.15	5.61	6.57
ϕ_M (deg)	65	62	65
SR (V/μsec)	6.21/-5.25	10.1/-7.3	4.88/-4.4
CMR (V)	2.0/-2.2	1.5/-1.82	2.31/-2.4
OS (V)	2.15/-2.15	1.76/-1.75	2.45/-2.46
Input-referred noise @ 1MHz	44 nV/$\sqrt{\text{Hz}}$	50 nV/$\sqrt{\text{Hz}}$	42 nV/$\sqrt{\text{Hz}}$

Design parameters of the opamp designed by our proposed design step, complete with robust bias part, is shown in Table VII. HSPICE simulation results of such an opamp under a variety of process conditions and parameters (Table VIII) are shown in Table IX where its robustness is evident.

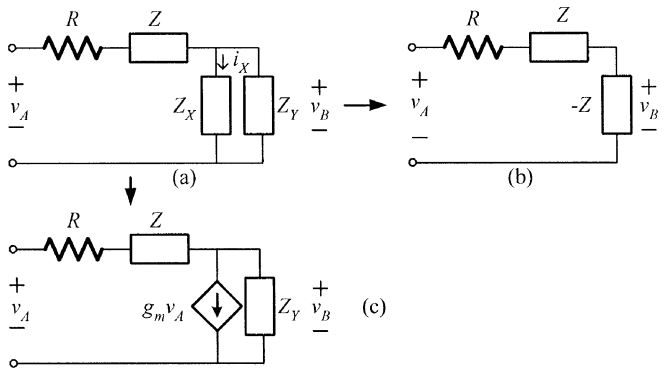

Fig. 7. Network transformation.

VII. CONCLUSION

The design procedure for two-stage CMOS opamp has been presented. Simulation results confirm that the proposed design step is more flexible than the one proposed in [2]. This is due to the fact that condition $C_c \gg C_{gs6}$ is not required in the proposed step. The Proposed procedure thus provides circuit designers with a higher degree-of-freedom to optimize their opamps in terms of noise performance and power consumption. Furthermore it has been shown that with proper biasing circuit, the opamp designed from the proposed procedure is tolerant to various process and temperature variation. However, since the pole/zero cancellation scheme seems to be more susceptible to variations than other compensation techniques, further investigation might be necessary to ensure suitability of the proposed procedure for particular applications. It should also be pointed out that although this paper does not concern power-supply rejection ratio, mismatched offset and $1/f$ noise contribution, these quantities can be improved by increasing the device area (i.e., increasing WL) while maintaining the W/L ratio.

APPENDIX
NETWORK TRANSFORMATION

For a network shown in Fig. 7(a), it can be shown that if

$$Y_X = -(Y + Y_Y) \tag{A1}$$

where $Y_X = 1/Z_X$ and $Y_Y = 1/Z_Y$, such a network can be transformed into that shown in Fig. 7(b) where the voltage V_B is found to be

$$V_B = -V_A \frac{Z}{R}. \tag{A2}$$

Hence, under the condition (A1), the current flowing through Z_X in Fig. 7(a) is

$$i_X = -\frac{Y_X Z}{R} V_A. \tag{A3}$$

Substituting (A1) into (A3) yields

$$i_X = \frac{\left(1 + \frac{Y_Y}{Y}\right)}{R} V_A. \tag{A4}$$

According to (A4), it is apparent that under the condition of (A1), the network shown in Fig. 7(a) can be transformed into that shown in Fig. 7(c) where

$$g_m = \frac{\left(1 + \frac{Y_Y}{Y}\right)}{R}. \tag{A5}$$

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