

**A Low-Noise CMOS Fully Differential
Telescopic Cascode Operational
Transconductance Amplifier**

Submitted in Partial

Fulfillment of the

Requirements of EE 240

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Design Outline

Introduction

We have designed a fully differential amplifier to meet the specifications of 85 dB dynamic range and 5 ns settling time using a telescopic cascoded topology. Because MOSFETs are non-ideal small-signal transconductance elements, the amplifier design must achieve a balance between a web of tradeoffs such as power, gain, noise, capacitance, and speed. The first step in the design process is to choose a topology by which we intend to meet the specifications using less power than alternative topologies.

Choice of Topology

Our hand calculations showed that for the specifications required, the open-loop voltage gain of the amplifier must be on the order of the square of the MOSFET intrinsic gain $g_m r_o$. Three differential amplifier topologies are appropriate to achieve this gain: telescopic cascode, folded-cascode, two-stage, and gain-booster. In Razavi's Design of Analog CMOS Integrated Circuits, on page 314, a quick reference guide is given comparing the performance of various op amp topologies. The table is reproduced below:

Topology	Gain	O/P Swing	Speed	Power Diss.	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded-Cascode	Medium	Medium	High	Medium	Medium
Two-stage	High	Highest	Low	Medium	Low
Gain-Boosted	High	Medium	Medium	High	Medium

We were familiar with the folded-cascode topology used to illustrate concepts in class, but realize that it would require more power than the telescopic cascode topology because the “extra fold” requires more current sources. We decided against using a two-stage amplifier because it would require more power to bias more series-FET legs in the circuit. In addition, stability would become a bigger issue as a second stage may introduce another dominant pole.

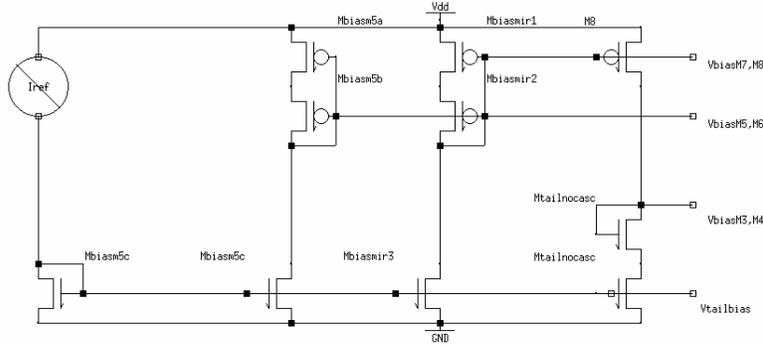
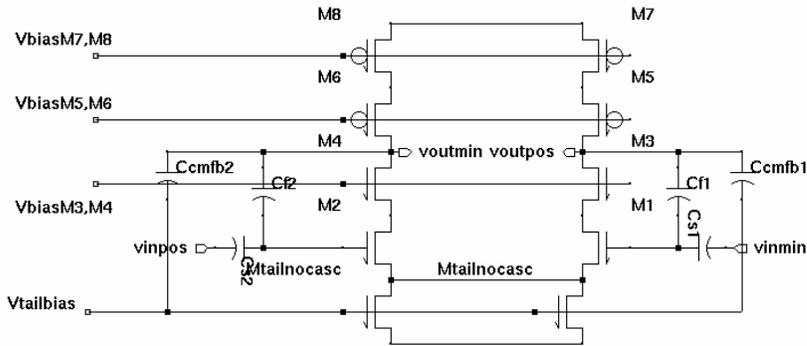
The gain-boosting topology tends to dissipate higher power because for reasons that it would require more devices, more supply-to-ground legs, and a more complex biasing circuit drawing power. However, past designs have shown that a gain-boosted topology can indeed yield low power dissipation if properly designed. Despite its appeal as an interesting design challenge, this topology was not chosen because of its stability issues. We also would like to avoid pole-zero doublets of gain-boosted amplifiers that would lengthen the settling time.

The telescopic-cascode design is so appealing because it consumes fairly low power in general because it draws current through only two current lines. Although the cascodes can limit the output swing, it still would also be feasible to meet the Dynamic Range (DR) requirement of 85 dB by designing in a low noise factor. We initially chose the telescopic topology for its seemingly straightforward design and low power. As we progressed with the initial design, we found that the benefits of the telescopic cascode come at the price of high sensitivity to the biasing network.

MOSFET device sizings

Main Amplifier MOSFETs

Device	W	L	gm	Id	gm/Id
M1	679.2u	0.5u	26.7419m	1.7973mA	14.8789
M2	679.2u	0.5u	26.7419m	1.7973mA	14.8789
M3	679.2u	0.5u	27.1421m	1.7973mA	14.8789
M4	679.2u	0.5u	27.1421m	1.7973mA	14.8789
M5	654.5u	0.5u	16.4164m	1.7973mA	9.1339
M6	654.5u	0.5u	16.4164m	1.7973mA	9.1339
M7	1440u	1.0u	15.5264m	1.7973mA	8.6387
M8	1440u	1.0u	15.5264m	1.7973mA	8.6387
Mtailnocasc1	660.0u	1.0u	18.8276m	1.7676mA	10.65
Mtailnocasc2	660.0u	1.0u	18.8276m	1.7676mA	10.65



Bias Network MOSFETs

Device	W	L	gm	Id	gm/Id
Mtailmirror	1320u	1.0u	38.6188m	3.6000mA	10.7274
MbiasMir1	1440u	1.0u	15.7042m	1.8162mA	8.6467
MbiasMir2	1440u	0.5u	6.7050m	1.8162mA	3.6918
MbiasMir3	660u	1.0u	19.5123m	1.8162mA	10.7465
MbiasM3a	1398u	1.0u	15.3537m	1.7756mA	8.647
MbiasM3b	16u	0.5u	3.1229m	1.7756mA	1.7587
MbiasM3c	660u	1.0u	18.8276m	1.7756mA	10.6035
MbiasM5a	96u	1.0u	2.9885m	1.8116mA	1.6496
MbiasM5b	720u	0.5u	17.2851m	1.8116mA	9.5413
MbiasM5c	660u	1.0u	15.3537m	1.8116mA	8.4752

Key Design Calculations

Our goal in designing the telescopic amplifier input transistors to provide the gain and the cascode FETs to provide higher output resistance. If we give half of the settling accuracy to static accuracy, we know that $F = C_f / (C_s + C_f + C_{in}) < 5/6$ and $A_{vo} = 2/F / \epsilon_{\text{settling}} > 1200 \text{ V/V}$. FETs in our EE240 0.35um CMOS technology can provide an intrinsic gain $g_m r_o$ of about 30 V/V to 50 V/V. A cascode topology achieves an open-loop gain A_{vo} of approximately $(g_m r_o)^2$, and would satisfy the A_{vo} if we adjust our FET sizings to achieve a $g_m r_o$ intrinsic gain of about 35 V/V. This A_{vo} must be met or exceeded over the entire claimed output DM swing of the amplifier.

As we began this project, we had looked at other OTAs in order to gain an intuition of what could be done. We also based much of our calculations off the technique explained in class used to design the folded cascode example. From our intuition, we decided that we should design initially for a 1.5 V swing with 1K gain at the corners. Also, as we began dealing with allocating error in settling, we used 0.5 for the factors initially and later adjusted them.

$$\frac{1}{f} := 1 + c + \frac{C_i}{C_f} \quad \text{Realizing that the last term of the sum would be tiny (an order smaller than F), the } F=5/6.$$

$$n_f := 1 + 2 \cdot \frac{V_{ov1}}{V_{ov9}} + \frac{V_{ov1}}{V_{ov7}} \quad n_f := 3.125$$

When we picked the V_{ov} values, we realized that we needed high swing meaning small V_{ov} s. This basically meant that we restricted v_{ov} s to be within the range of approximately 150-250mV.

$$P_{\text{noise}} := \frac{2 \cdot K_B \cdot T_r}{\text{Cleff}} \cdot \frac{n_f}{F} \quad 10^{0.1 \cdot \text{DR}} := \frac{P_{\text{sig}}}{P_{\text{noise}}} \quad \text{These two equations give the Cleff we need}$$

Thus our Cleff = 9.2pF.

The DR of the output signal is proportional to the claimed output DM swing of the amplifier, and inversely proportional to the noise of the circuit. The noise power at the output is determined by the effective load capacitance and the noise factor, which is determined by V_{OV} ratios. $n_f = 1 + 2 \cdot V_{OV_IN} / V_{OV_NCS} + V_{OV_IN} / V_{OV_PCS}$. For a claimed output swing, the effective load capacitance must be sufficiently large to keep the noise down to meet the dynamic range of 85 dB.

In slewing:

$$\text{SR} := \frac{\frac{V_{od_step}}{F} - V_{ov1}}{F \cdot t_{\text{slew}}} \quad \text{and} \quad \text{SR} := \frac{I_{ss}}{C_{\text{Leff}}} \quad \text{so } I_{ss} = 2.3\text{mA.}$$

Linear Setting:

$$\text{err}_{\text{lin}} := \text{err}_{\text{dyn}} \cdot \frac{V_{\text{od_step}} \cdot F}{V_{\text{ov1}}} \quad (\text{Where err}_{\text{dyn}} \text{ was chosen initially to be half the total error.})$$

$$n := -\ln(\text{err}_{\text{lin}}) \quad \text{tao} := \frac{t_{\text{lin}}}{n} \quad \text{and} \quad \text{tao} := \frac{C_{\text{eff}}}{g_{\text{m1}}} \cdot \frac{1}{F} \quad \text{so} \quad g_{\text{m1}} := \frac{C_{\text{eff}}}{\text{tao}} \cdot \frac{1}{F}$$

$$I_{\text{d1}} := g_{\text{m1}} \cdot \frac{V_{\text{ov1}}}{2} \quad , \text{where our } I_{\text{d1}} \text{ came out to about half the } I_{\text{ss}}. \text{ This meant that we would have a a maximum power efficiency for our operational amplifier.}$$

From this initial start, we were able to iterate with MATLAB and adjust the values so that all specifications are met.

Biasing Network

In the initial design of the amplifier, we used ideal voltage sources in HSPICE to bias the gates of the current source and cascade transistors. We eventually replaced these voltage sources with a high-swing cascade biasing network, but we did not spend much time optimizing it for power. We only tweaked some sizings to improve our swing and open-loop gain A_{VO} .

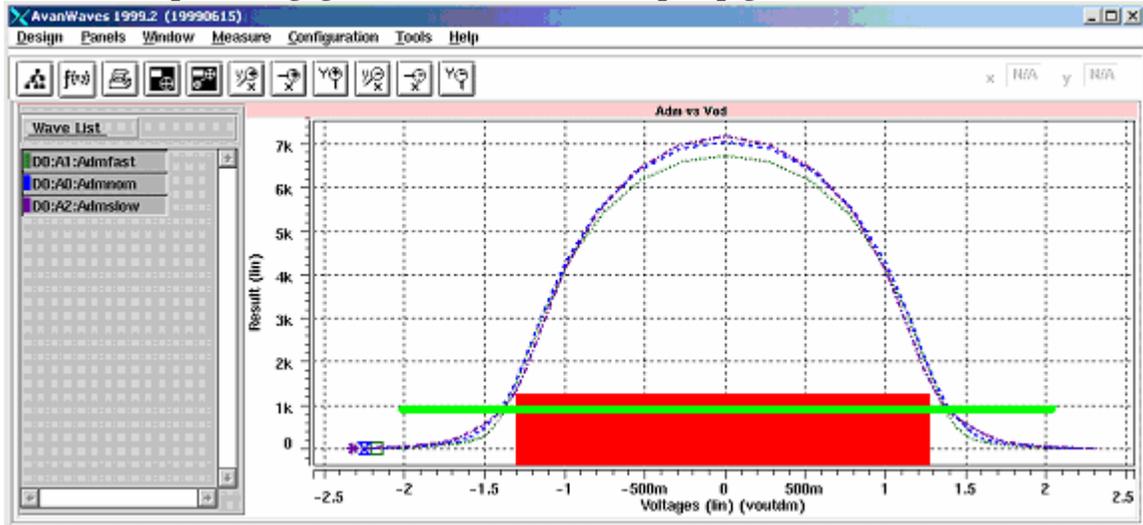
Common-Mode Feedback (CMFB) Design

The need for CMFB comes from the fact that the sum of the currents from the current sources in the two branches must sum to the current that the tail FET is trying to source. Even if the currents from both branches match exactly at input DM of 0, the branches are likely to mismatch when the DM input signal is nonzero. Therefore, we must use a feedback mechanism to ensure that the all the FETs stay in saturation and the CM output voltage stays constant under different input conditions.

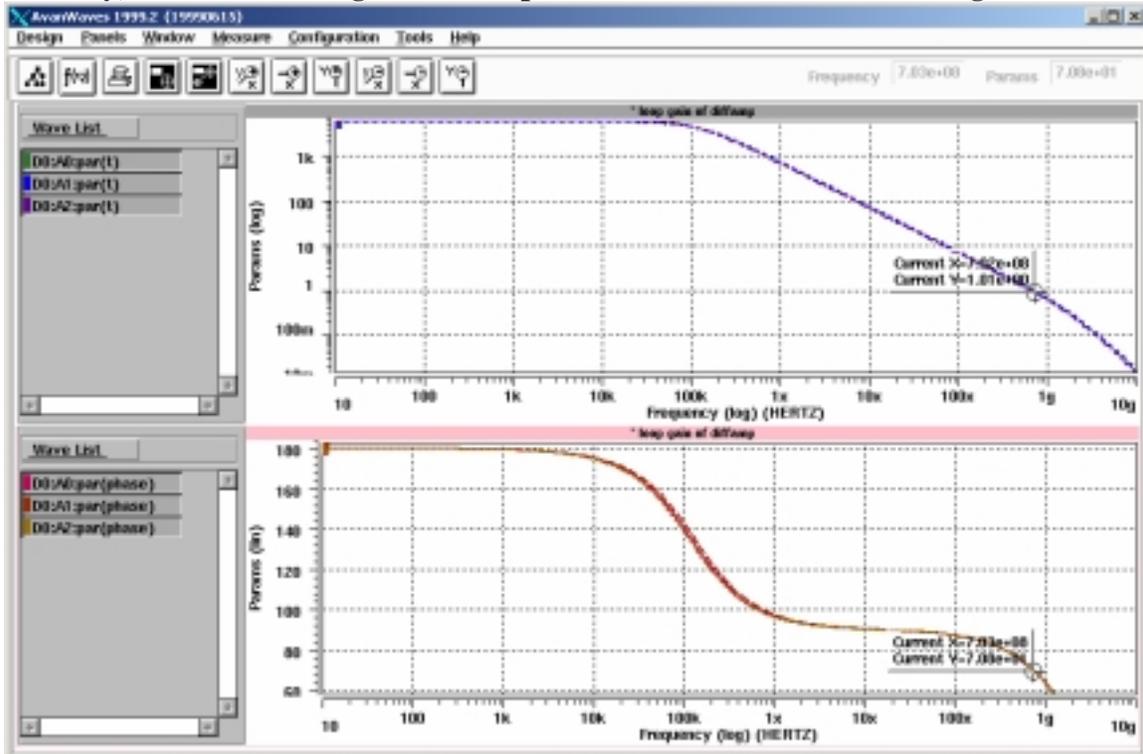
In a capacitive common-mode sensing circuit, we must define the output CM level by using a dynamic scheme with switched capacitances. With large output swings, the speed of the CMFB loop may influence the settling of the output DM signal. That is why we choose to provide part of the tail current by a constant current source, while the CMFB MOSFET makes small adjustments in the tail current.

Verification Plots

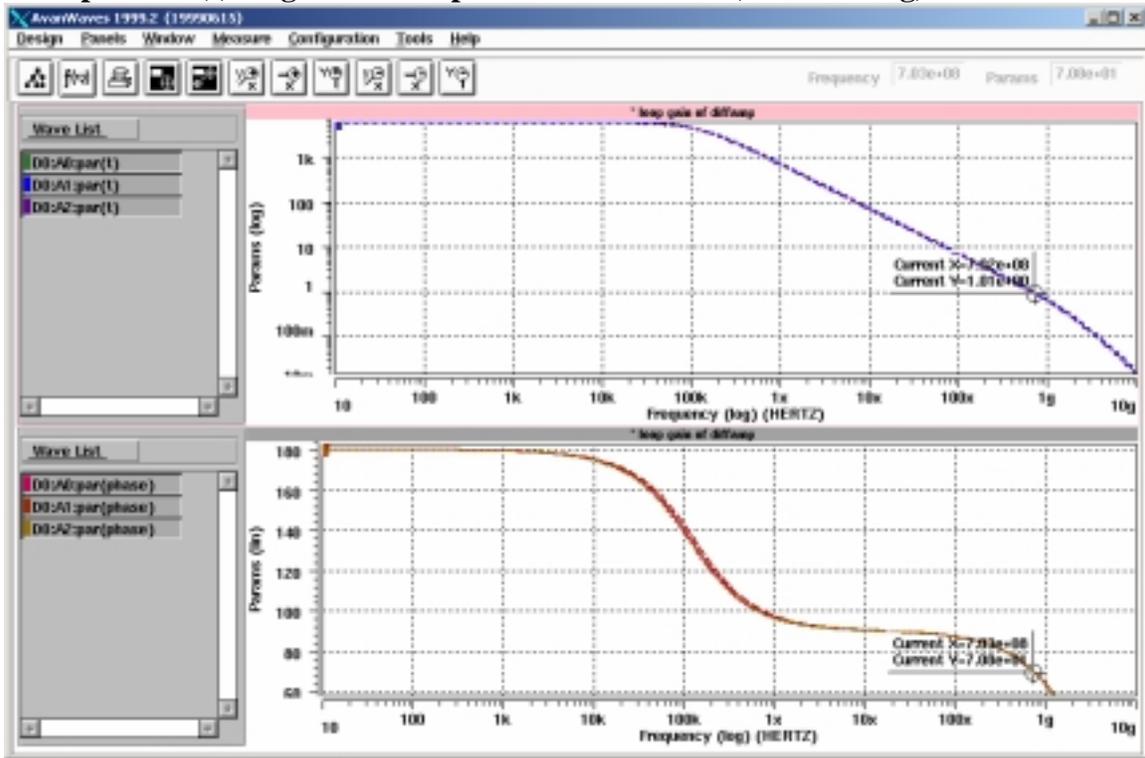
$A_{V0} = dV_{od}/dV_{id}$ vs V_{od} , Open-loop gain versus Output Swing, Claimed output swing, gain, and $F \cdot A_{V0}$ (low freq loop gain)



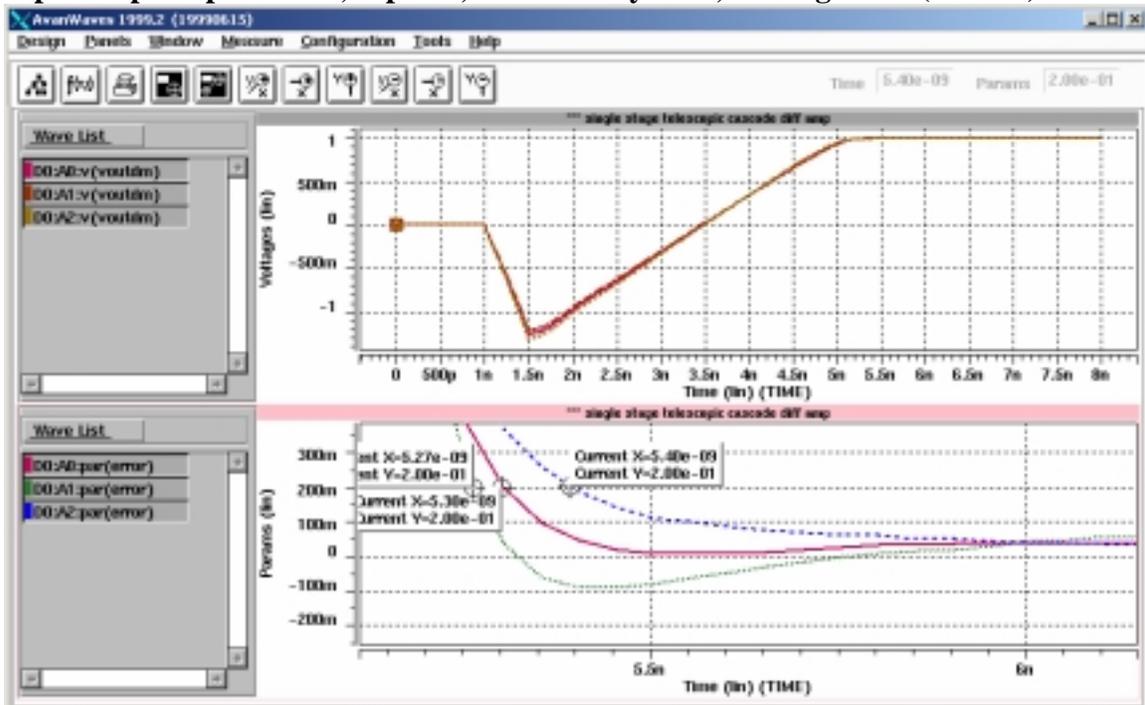
Stability, Bode of $T(s)$ magnitude and phase for $V_{od}=0.0V$ (PM is 70deg)



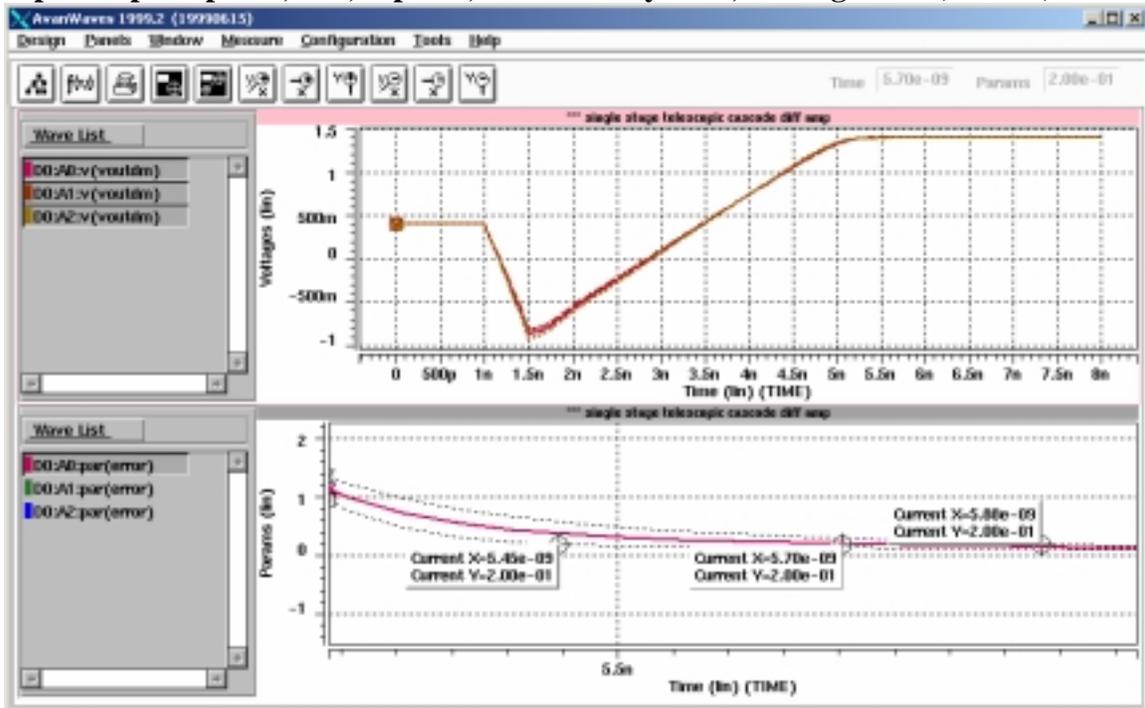
Bode plot of T(s) magnitude and phase for $V_{od}=1.4V$ (PM is 70 deg)



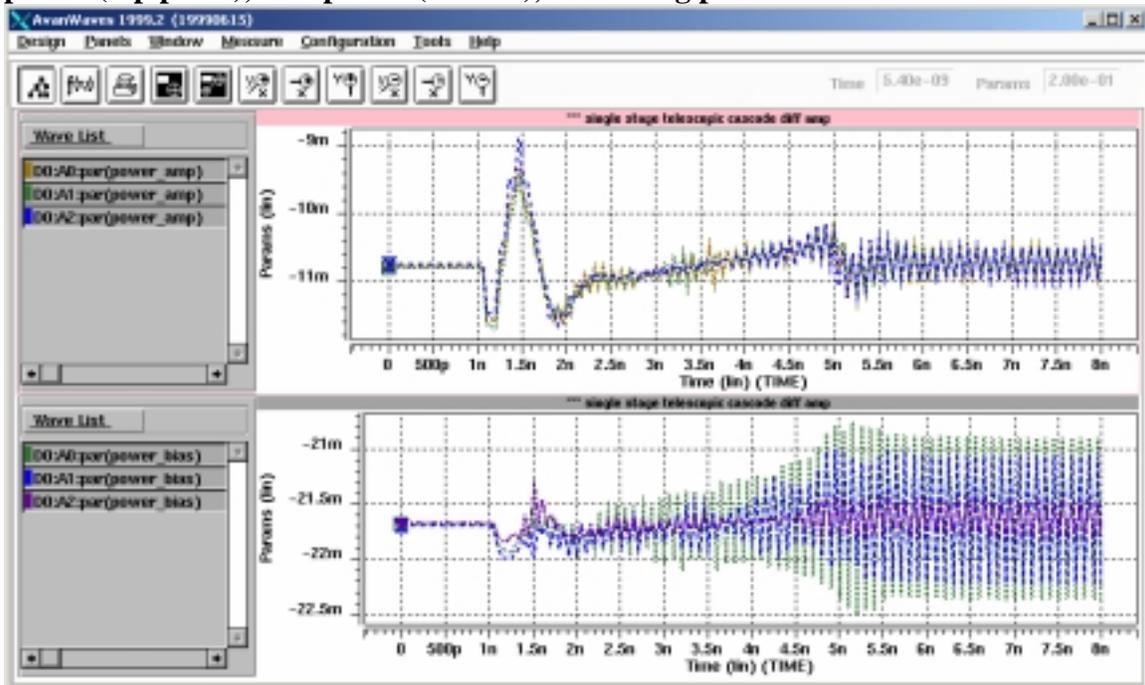
Input Step Response $V_{id,step}=5V$, V_{od} initially 0.0V, settling error (bottom)



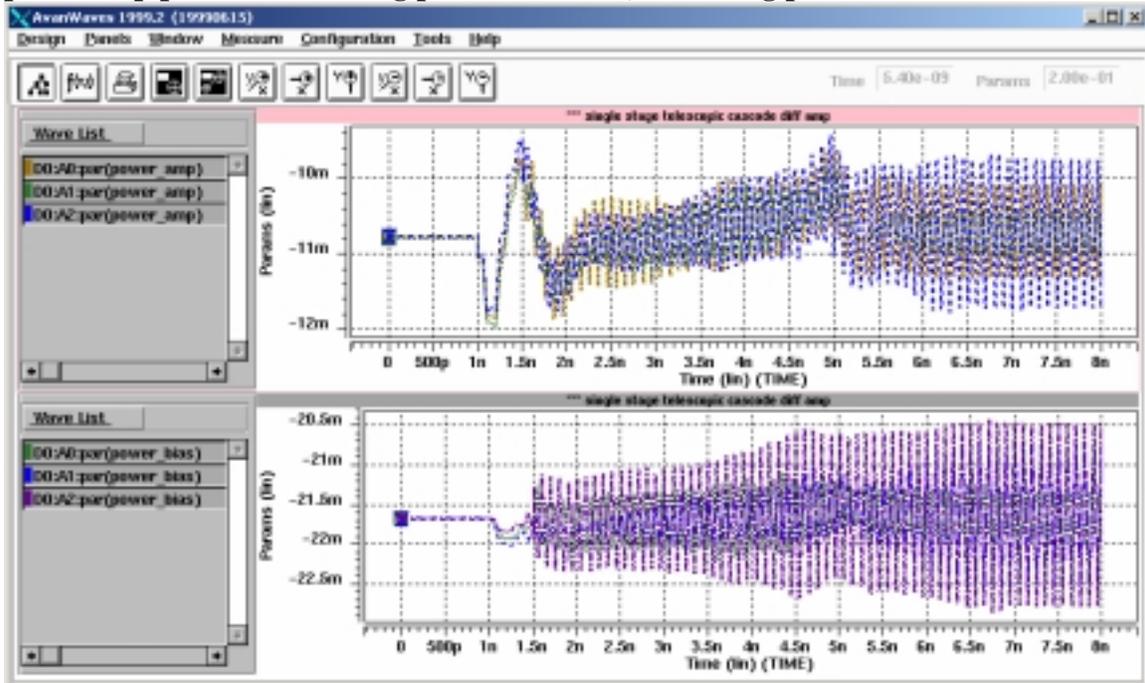
Input Step Response, Vid,step=5V, Vod initially 0.4V, settling error (bottom)



Instantaneous Power Dissipation during Vid,step=+5V, Vod initially 0.0V, amplifier power (top panel), bias power (bottom), Mark Avg power



Instantaneous Power Dissipation during $V_{id,step}=+5V$, V_{od} initially $0.4V$, amplifier power (top panel) and biasing power (bottom), Mark avg power



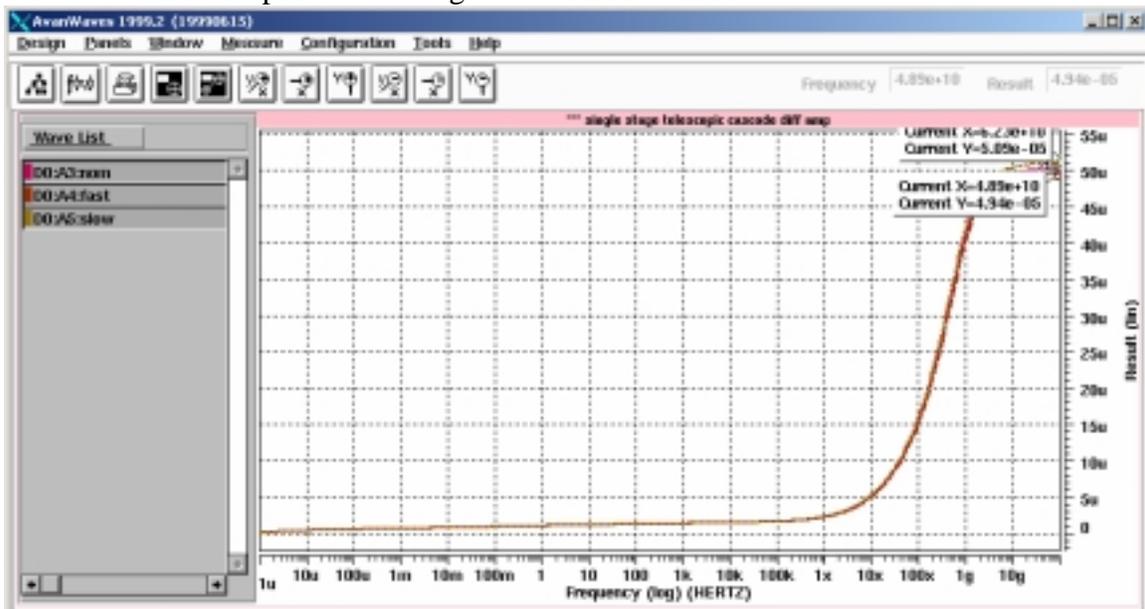
Noise: total noise at V_{od} for $V_{od} = 0.0V$

Total output noise voltage (VRMS) for $V_{od}=0$

Nominal **** total output noise voltage = 50.1667μ volts

Fast **** total output noise voltage = 49.5107μ volts

Slow **** total output noise voltage = 50.9867μ volts



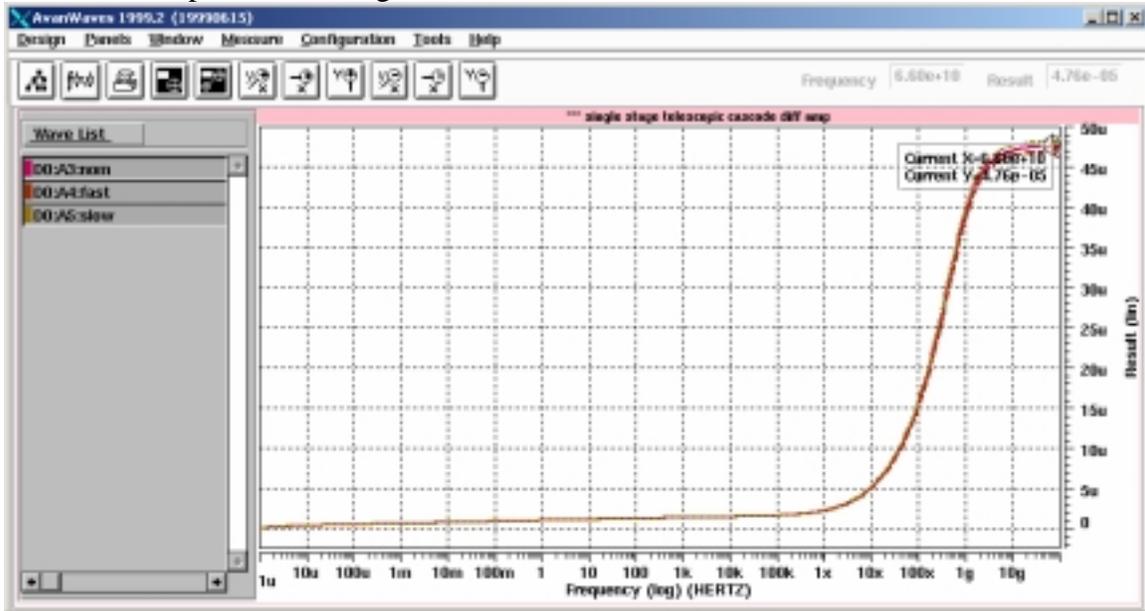
Noise: total noise at V_{od} for $V_{od}=1.4V$

Total output noise voltage (VRMS) for $V_{od}=1.4V$

**** total output noise voltage = 47.6224u volts

**** total output noise voltage = 46.9922u volts

**** total output noise voltage = 48.1949u volts



Comments, Further Considerations, Conclusions

In the design of the Telescopic Cascode Amplifier, the NMOS tail current source was not implemented as a cascode. We decided against using a cascaded NMOS tail current source because we needed to maximize our output swing to meet the noise specification. Cascoding would decrease our output swing by several tenths of a volt. The benefit of cascoding, however is a higher CMRR, where while in this project, we did not need to examine this aspect, in practice, we should.

We started with the very simple circuits in order to get to the bigger circuit. In order to deal with the differences between simulation and hand calculations, we still had to do a considerable amount of tweaking due to non-idealities in the transistors. We feel that we cannot totally rely on square-law models, but they are fairly useful for first-order approximations.

We realized the sensitivity of the biasing to the performance would limit our control of the biasing conditions of all transistors. This led to the discrepancy in achieving the overdrive voltages and transconductances targeted by the initial design. In the end, this led to a power dissipation of approximately **11mW** - higher than we had anticipated.

Appendix

Matlab script

```
function tele0()
% calculates important requirements of a telescopic cascode amplifier
% to meet given specifications

format compact;
format short g;
%specifications (sorry, cannot change these)
eps_sett=0.002 %settling accuracy within tsett
c=0.2 %closed loop gain
tsett=5e-9 % time to settle within eps_sett accuracy
VDD=3 %volts power supply
DR=85 %dB

%settling constraint is two things: static + dynamic
%static accuracy
F=1/(1+c+0.01) %guess, maybe Ci is significant for Wide Input FETs
eps_stat=0.5*eps_sett, avo=1/F/eps_stat
%avo=900, eps_stat=1/F/avo %need more if Ci significant

%dynamic range, max output over noise floor
Vdsat=300e-3 %design choice
Vodppmax=2*(VDD-5*Vdsat) %Vrms^2 design choice
eps_stat_div_eps_sett=eps_stat/eps_sett
Psigmax=(Vodppmax^2) / 8 %Vrms^2
Vovin=150e-3 %input NMOS
Vovncs=250e-3 %current src PMOS
Vovpcs=250e-3 %cascode PMOS
nf=1+2*Vovin/Vovncs+Vovin/Vovpcs % pick Vov wisely
%nf=4 % pick Vov wisely
kBT=4e-21
CLeff=10^(DR/10)*2*kBT*nf/F/Psigmax
CDB=0 %find from SPICE
%CL=CLeff-Cf*(1-F)-CDB

% dynamic settling time (worst case)
% two components: slewing, then linear response
eps_dyn=eps_sett-eps_stat
Vod_step=Vodppmax/2

% ** slewing **
rslew=0.57 %design guess, slew longer, less Iss
tslew=rslew*tsett
tlin=tsett-tslew
slewrates=(Vod_step/F - Vovin)/F/tslew
Iss_slew=CLeff*slewrates
Iss_slew_power=Iss_slew*VDD

% ** linear **
eps_lin=eps_dyn*Vod_step*F/Vovin
numtaus=-log(eps_lin)
tau=tlin/numtaus
gmin=CLeff/tau/F
ID1=gmin*Vovin/2
```

```
IssdivID1=Iss_slew/ID1
Iss_slew
Iss_lin=2*ID1
Iss_max=max(Iss_lin, Iss_slew)
Isspow=VDD*Iss_max
```

```
gm_in=Iss_max/Vovin
gm_ncs=2*Iss_max/Vovncs
gm_pcs=Iss_max/Vovpcs
```

HSpice Netlists

```
*** tele10parameters
```

```
*square law sizings
```

```
.param vddval=3.0v vincmval=1.1v vocmval=1.5v vbm3val=1.5
+ vindmdc=0 $0.61mv
+ win='566u*currentfact' wncasc='566u*currentfact'
+ wpcasc='1200u*currentfact/2' $530u
+ wpcs='1200u*currentfact' wtailcs='1100u*currentfact'
**+ win=411u wncasc=160u wpcasc=431u wpcs=1090u wtailcs=592u
+ lin=0.5u lncasc=0.5u lpcasc='0.5u' lpcs=1.0u ltailcs=1.0u
+ wbias5a='wpcs/15' lbias5a=lpcs
+ wbias5b='wpcasc' lbias5b=lpcasc
+ wbias5c='wtailcs/2' lbias5c=ltailcs
+ currentfact=1.2
+ refcurrent='3mA*currentfact'
+ Csval=2.1p Cfval='5*Csval' Cloadval=1p
```

```
vdd vdd 0 dc vddval
vddbias vddbias 0 dc vddval
vbM3 vbncasc 0 DC vbm3val '$1.1+0.25'
*VbM5 vbpcasc 0 DC 1.7
*VbM7 vbpcs 0 DC 1.95
*VbM9 vbtailca 0 DC 0.85v
*VbM10 vbtailcs 0 DC 0.6v
```

```
M1 d1 vinpos vtail 0 nmos W='win' L=lin geo=3
M2 d2 vinmin vtail 0 nmos W='win' L=lin geo=3
M3 voutmin vbncasc d1 0 nmos W='wncasc' L=lncasc geo=2
M4 voutpos vbncasc d2 0 nmos W='wncasc' L=lncasc geo=2
M5 voutmin vbpcasc d7 vdd pmos W='wpcasc/1.1' L=lpcasc geo=2
M6 voutpos vbpcasc d8 vdd pmos W='wpcasc/1.1' L=lpcasc geo=2
M7 d7 vbpcs vdd vdd pmos W='wpcs' L=lpcs geo=1
M8 d8 vbpcs vdd vdd pmos W='wpcs' L=lpcs geo=1
```

```
*tail current source
```

```
Mtailnocasc1 vtail tailbias 0 0 nmos W='wtailcs/2' L=ltailcs geo=1
Mtailnocasc2 vtail tailbias 0 0 nmos W='wtailcs/2' L=ltailcs geo=1
Mtailmirror tailbias tailbias 0 0 nmos W=wtailcs L=ltailcs
Iref vddbias tailbias 'refcurrent'
```

```
*string biasing for the top transistor
```

```
Mbiasmir1 dmir1 vbpcs vddbias vddbias pmos W='wpcs' L=lpcs
Mbiasmir2 vbpcs vbpcasc dmir1 0 pmos W='wpcasc' L=lpcasc
*Rmir2gs vbpcasc vbpcs 1T
```

Mbiasmir3 vbpcs tailbias 0 0 nmos W='wtailcs/2' L=ltailcs

*string for the M5 transistors

**remember to remove Rmir2gs if use this

MbiasM5a dbiasm5a vbpcasc vddbias vddbias pmos W=wbias5a L=lbias5a

MbiasM5b vbpcasc vbpcasc dbiasm5a vddbias pmos W=wbias5b L=lbias5b

MbiasM5c vbpcasc tailbias 0 0 nmos W=wbias5c L=lbias5c