Items to keep in mind for constraining clocks or debugging clock related issues

Is it a Master or Generated clock?	• How many levels of generation?
Virtual clock or real?	
If real, Source pin & its drive and transition characterizations	• Non physical hierarchical block ports not recommended. • Specifying both min and max recommended for timing model generation
Are both rising edge and falling edges used?	• Is such a use allowed.?
Any Level sensitive sequential elements. (Latches)	• If so, is it both high and low? Max time borrow>
Thus the waveform.	• Most restrictive edges are used.
Any Multicycle Path (MCP) restrictions.	• Intermediate edges skipping not done automatically by synthesis tool. MCP is ONLY for timing checks. Designer should put extra logic matching MCP.
Source latency.	• Will get cancelled for same clk paths • Impacts only for inter domain paths
Network Latency: Ideal (& thus user annotated) or propagated (Tool calculated)?	
Uncertainity (Inter and Intra clock)	
Non disabled Arcs/Paths from master to Generated. (Very Important)	• Any restrictions in calculating gen clocks latency. Like trace only combinational paths
Nature of relationship. (ie divide by, multiplied by)	• Realization in design?
Addition of clock or overriding clocks at the source pin.	
Types of clock gatings along the path. (AND, OR only or XOR also?)	• Determines arc's traced in clock propagation
Automatic Clock gating inferences or directives	
Logical exclusivity (asynchronous relationships with other clocks)	
Physically exclusivity (Important for coupled timing analysis)	
Clock groups formation.	
Clock propagation restrictions. (Positive unate or negitive unate arc or non unate and set_clock_sense)	
Is it Active or inactive in present scenario?	• Any Gen clocks whose master is Inactive?
Clock topology & Pessimism reduction through CRPR	• CRPR_threshold to tradeoff runtime & pessimism removal