Chapter 13: Introduction to Switched-Capacitor Circuits

13.1 General Considerations

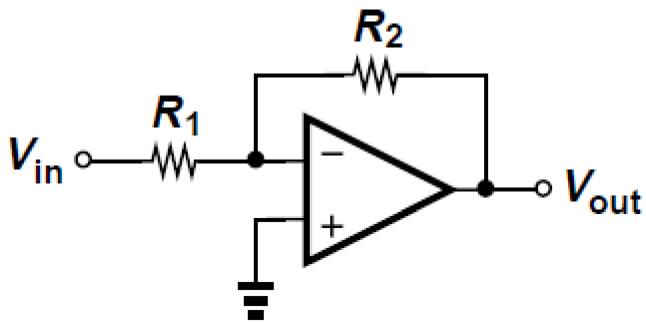
13.2 Sampling Switches

13.3 Switched-Capacitor Amplifiers

13.4 Switched-Capacitor Integrator

13.5 Switched-Capacitor Common-Mode Feedback

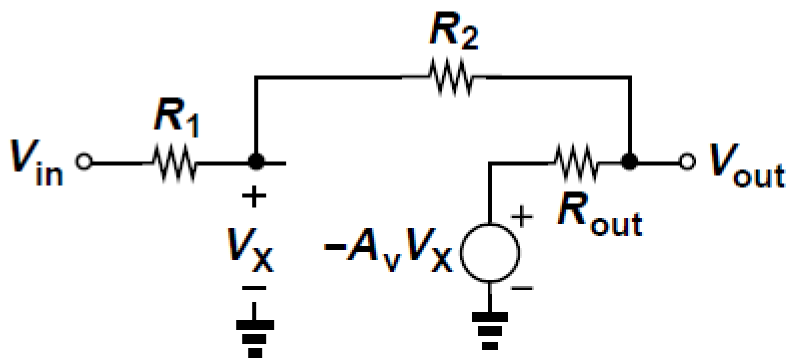
General Considerations



(a)

- For continuous-time amplifier [Fig. (a)], $V_{out}/V_{in} = -R_2/R_1$ ideally
- Difficult to implement in CMOS technology
- Typically, open-loop output resistance of CMOS op-amps is maximized to maximize A_v
- R_2 heavily drops open-loop gain, affecting precision

General Considerations



(b)

- In equivalent circuit of Fig. (b), we can write

$$-A_v\left(\frac{V_{out}-V_{in}}{R_1+R_2}R_1+V_{in}\right)-R_{out}\frac{V_{out}-V_{in}}{R_1+R_2}=V_{out}$$

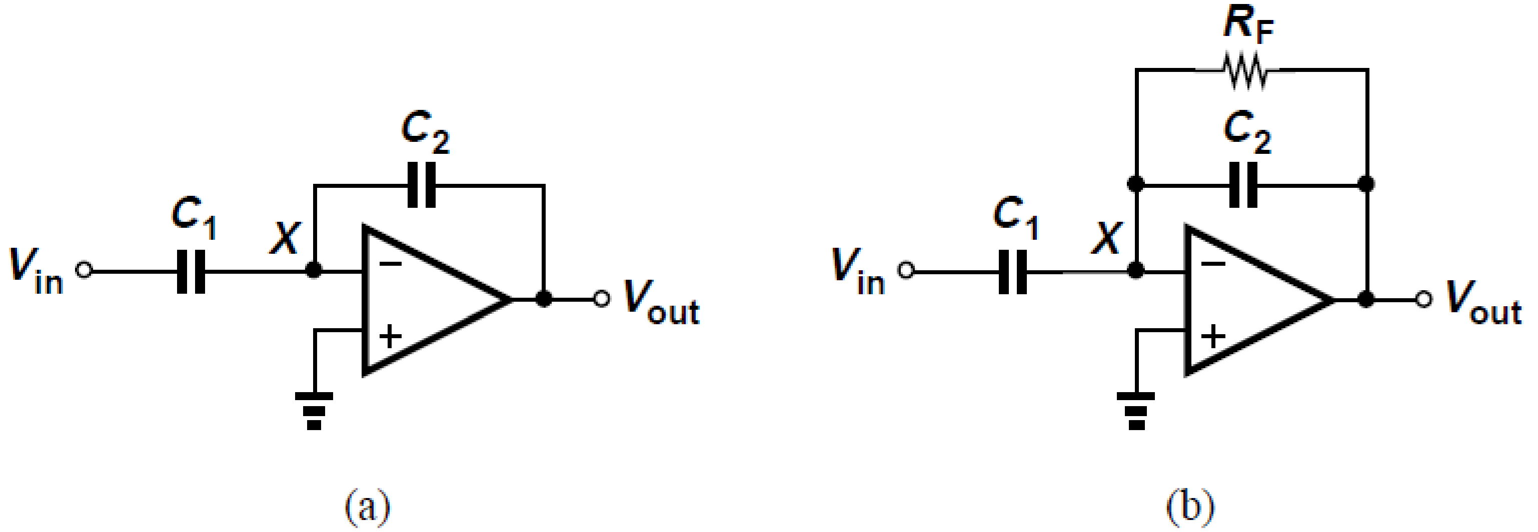
- Hence,

$$\frac{V_{out}}{V_{in}}=-\frac{R_2}{R_1}\cdot\frac{A_v-\dfrac{R_{out}}{R_2}}{1+\dfrac{R_{out}}{R_1}+A_v+\dfrac{R_2}{R_1}}$$

- Closed-loop gain is inaccurate compared to when $R_{out} = 0$

General Considerations

- To reduce open-loop gain, resistors can be replaced by capacitors [Fig. (a)]
- Gain of this circuit is ideally $-C_1/C_2$
- To set bias voltage at node X, large feedback resistor can be added [Fig. (b)]



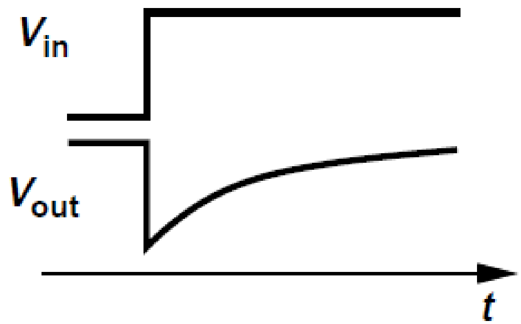
General Considerations

- **Feedback resistor is not suited to amplify wideband signals**
- **Charge on C_2 is lost through R_F resulting in "tail"**
- **Circuit exhibits high-pass transfer function given by**

$$\frac{V_{out}}{V_{in}}(s) \approx -\frac{R_F\frac{1}{C_2 s}}{R_F+\frac{1}{C_2 s}} \div \frac{1}{C_1 s}$$

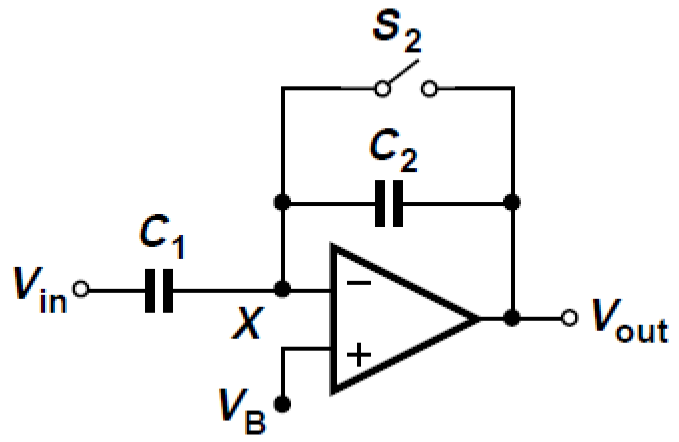
$$= -\frac{R_F C_1 s}{R_F C_2 s + 1},$$

- $V_{out}/V_{in} \approx -C_1/C_2$ **only if** $\omega \gg (R_F C_2)^{-1}$.

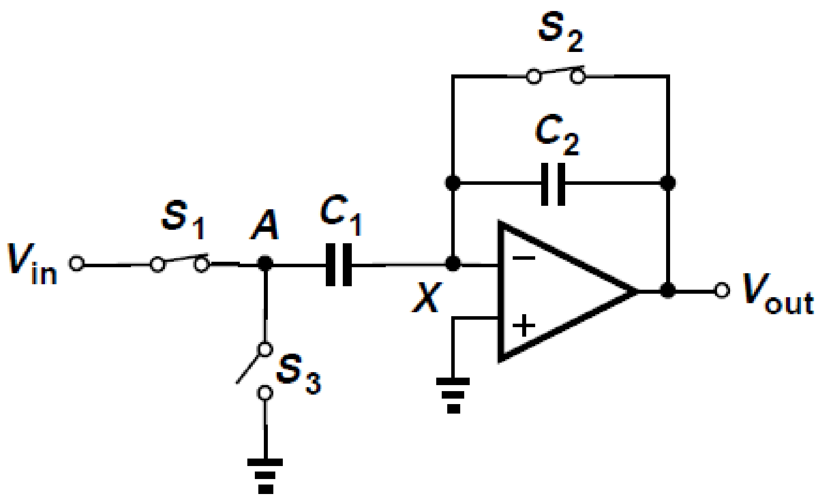


General Considerations

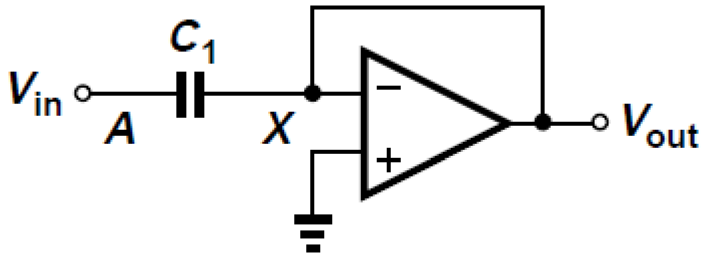
- R_F can be replaced by a switch
- S_2 is turned on to place op amp in unity gain feedback to force V_X equal to V_B, a suitable common-mode value
- When S_2 turns off, node X retains the voltage allowing amplification
- When S_2 is on, circuit does not amplify V_{in}



General Considerations

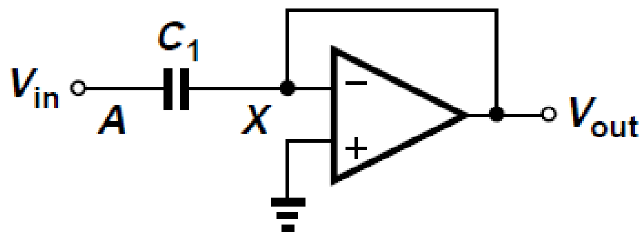


- In above circuit, S_1 and S_3 connect left plate of C_1 to Vin and ground, S_2 for unity-gain feedback
- Assume large open-loop gain of op amp
- First phase: S_1 and S_2 on, S_3 off [Fig. (a)]



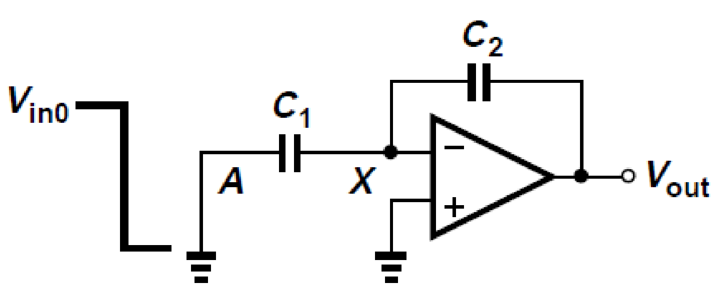
(a)

General Considerations

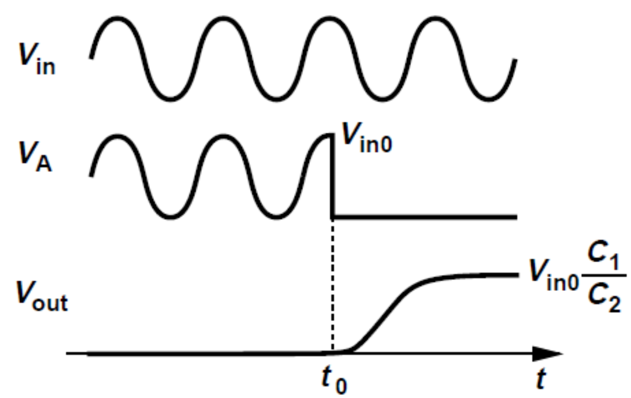


(a)

- Here, $V_B = V_{out} \approx 0$ and C_1 samples the input V_{in}
- Second phase: At $t = t_0$, S_1 and S_2 turn off and S_3 turns on, pulling node A to ground [Fig. (b)]
- V_A changes from V_{in} to 0, therefore V_{out} must change from zero to $V_{in0}C_1/C_2$ [Fig. (c)]



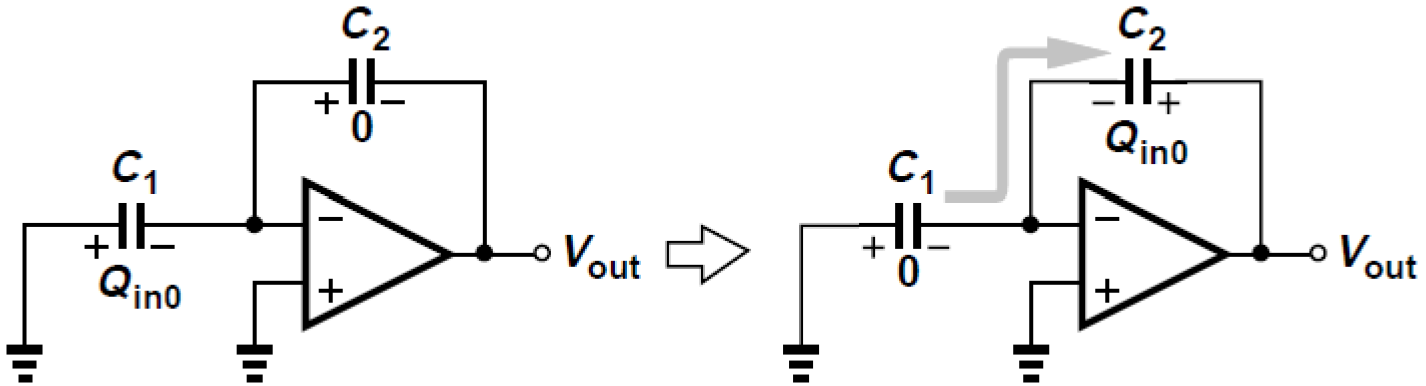
(b)



(c)

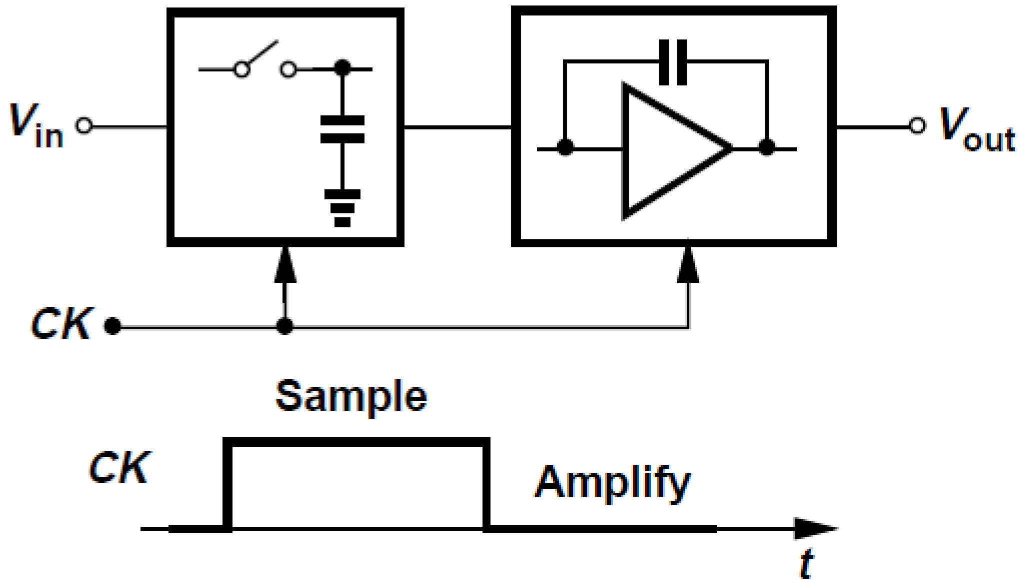
General Considerations

- **Circuit devotes some time to sample input, setting output to zero and providing no amplification**
- **After sampling, for $t > t_0$, circuit ignores input voltage, amplifies sampled voltage**



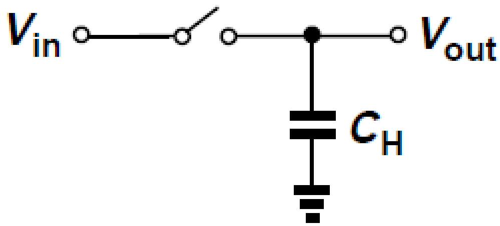
General Considerations

- Switched-capacitor amplifiers operate in two phases: Sampling and Amplification
- Clock needed in addition to analog input V_{in}

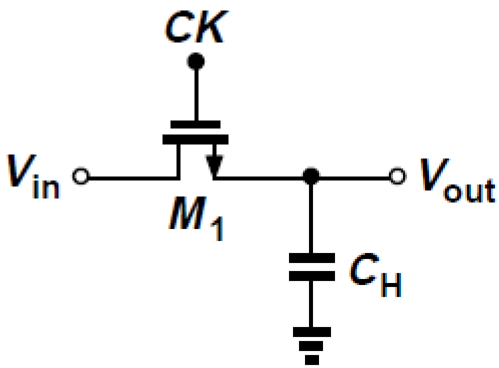


MOSFETS as Switches

- Sampling circuit consists of a switch and a capacitor [Fig. (a)]
- MOS transistor can function as switch [Fig. (b)] since it can be on while carrying zero current

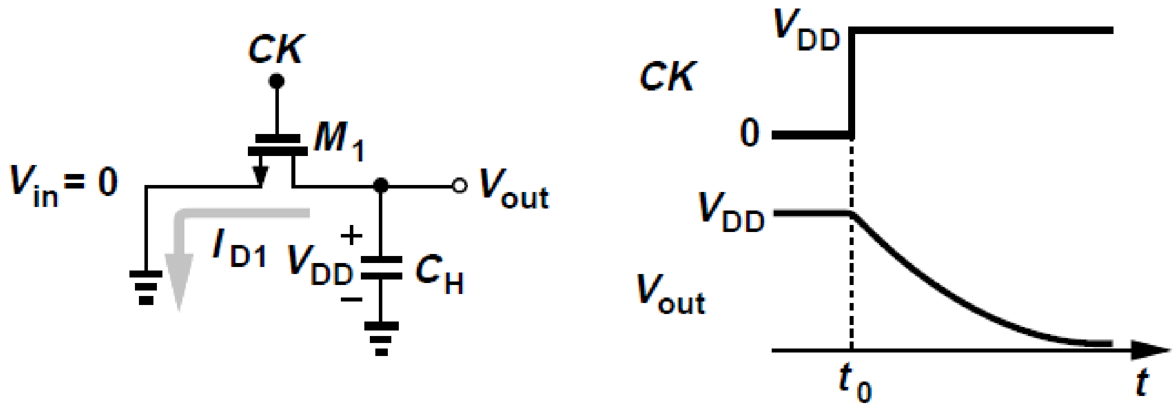


(a)



(b)

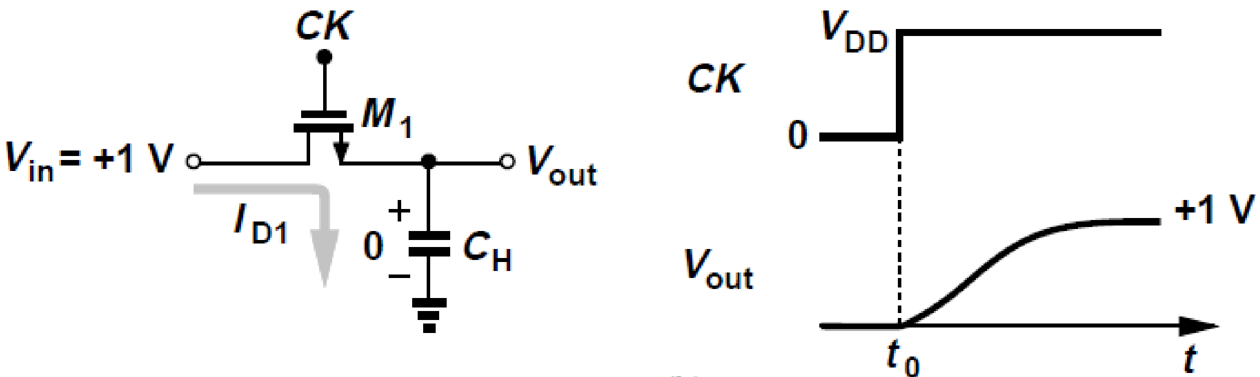
MOSFETS as Switches



(a)

- *CK* goes high at $t = t_0$
- Assume $V_{in} = 0$ and capacitor has initial voltage V_{DD}
- At $t = t_0$, M_1 is in saturation and draws current
- As V_{out} falls, at some point M_1 goes into triode region
- C_H is discharged until V_{out} reaches zero
- For $V_{out} << 2(V_{DD} - V_{TH})$, transistor is an equivalent resistor

MOSFETS as Switches

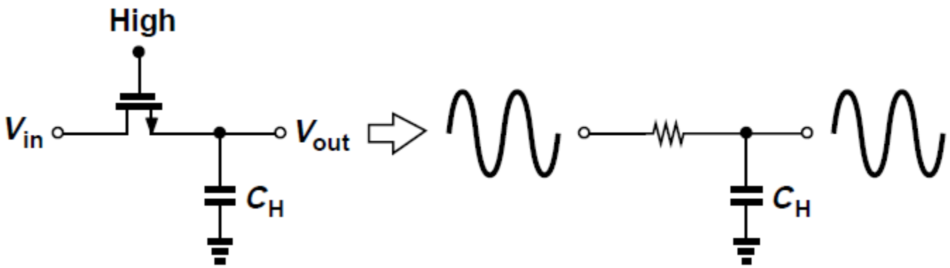


(b)

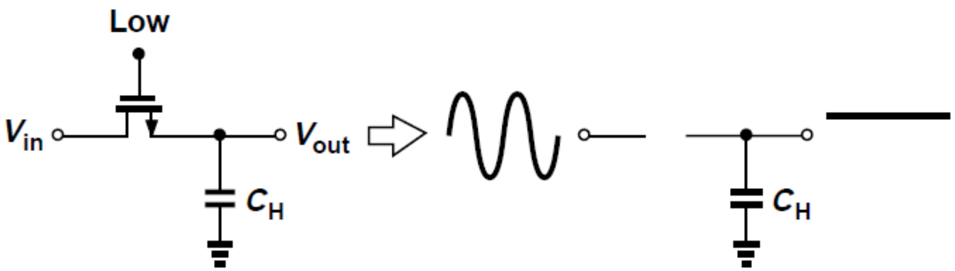
- If V_{in} = +*1 V*, $V_{out}(t = t_0)$ = +*0 V* and V_{DD} = +*3 V*
- Terminal of M_1 connected to C_H acts as source, and the transistor turns on with V_{GS} = +*3 V* but V_{DS} = +*1 V*
- M_1 operates in triode region and charges C_H until Vout approaches +*1 V*
- For $V_{out} \approx$ +*1 V*, M_1 exhibits an on-resistance of

$$R_{on} = [\mu_n C_{ox}(W/L)(V_{DD} - V_{in} - V_{TH})]^{-1}$$

MOSFETS as Switches



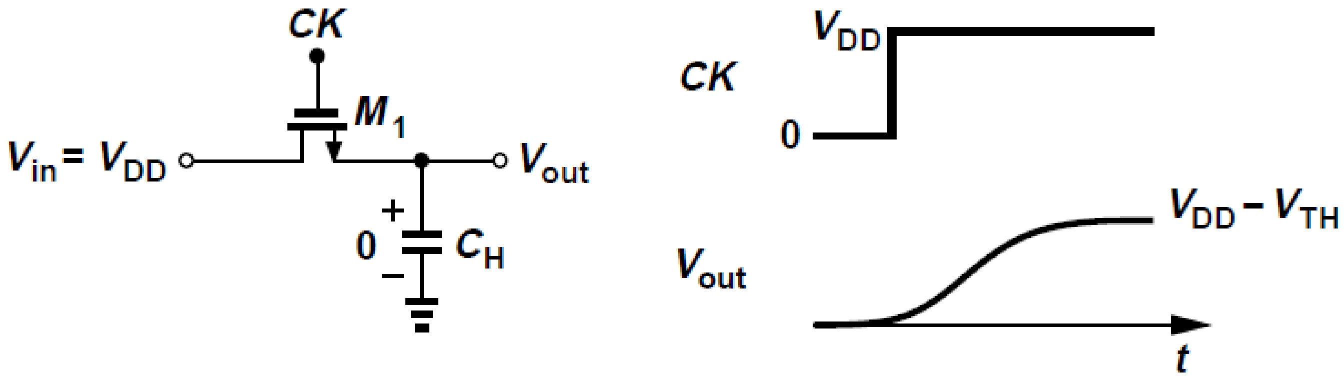
(a)



(b)

- **When switch is on [Fig. (a)], V_{out} follows V_{in}**
- **When switch is off [Fig. (b)], V_{out} remains constant**
- **Circuit "tracks" signal when *CK* is high and "freezes" instantaneous value of V_{in} across C_H when *CK* goes low**

MOSFETS as Switches



- Suppose $V_{in} = V_0$ instead of +*1 V*
- M_1 is saturated and we have:

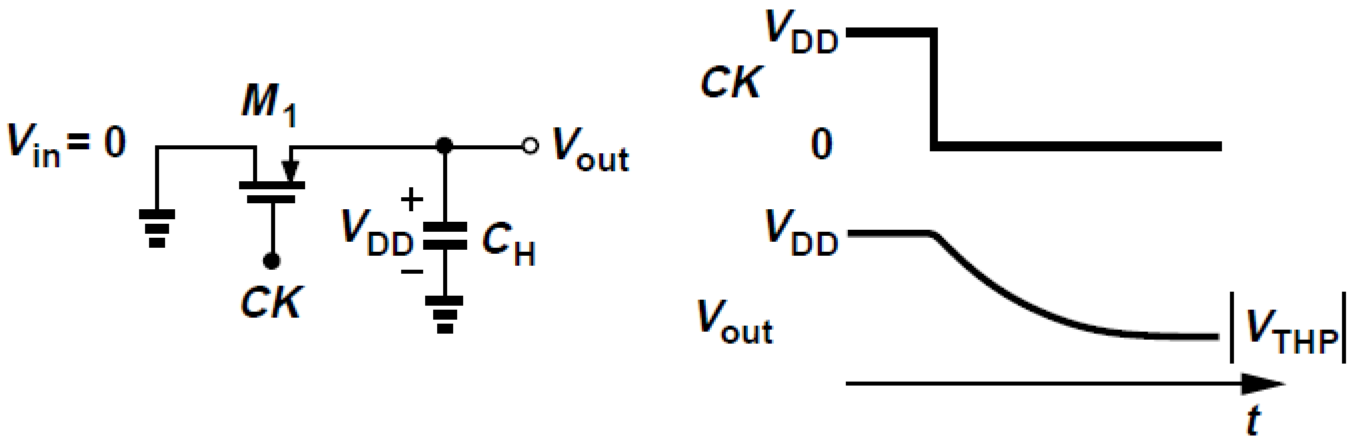
$$\begin{aligned} C_H \frac{dV_{out}}{dt} &= I_{D1} \\ &= \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{out} - V_{TH})^2 \end{aligned}$$

- Solving,

$$V_{out} = V_{DD} - V_{TH} - \frac{1}{\frac{1}{2}\mu_n \frac{C_{ox}}{C_H}\frac{W}{L}t + \frac{1}{V_{DD} - V_{TH}}}$$

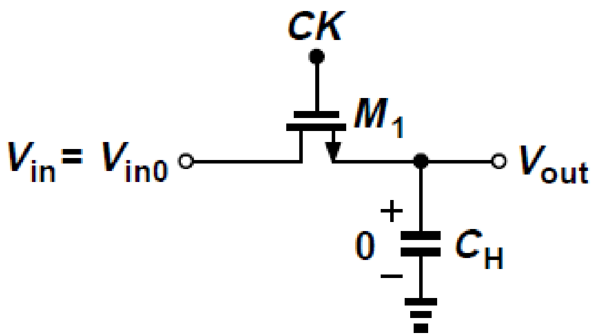
- As $t \rightarrow \infty$, $V_{out} \rightarrow V_{DD} - V_{TH}$ so NMOS cannot pull up to V_{DD}

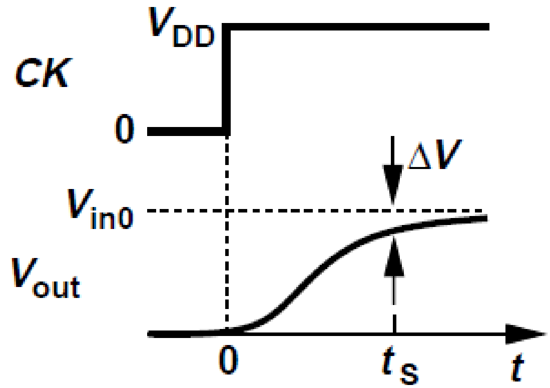
MOSFETS as Switches



- Similarly, PMOS transistor fails to operate as a switch if gate is grounded and drain senses an input voltage of $|V_{THP}|$ or less
- On resistance rises rapidly as input and output levels fall to $|V_{THP}|$ above ground

MOSFETs as Switches: Speed Considerations

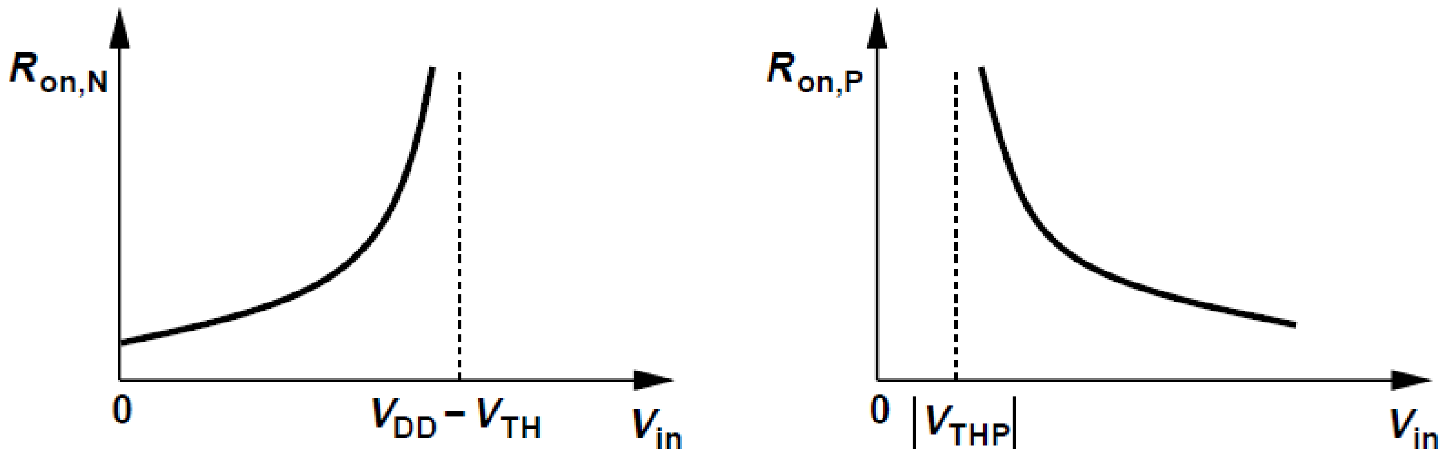




- Measure of speed is the time required for output to go from zero to the maximum input level after switch turns on
- Consider output settled within a certain "error band" ΔV around final value
- If output settles to *0.1%* accuracy after t_s seconds, then $\Delta V/V_{in0} = 0.1\%$
- After $t = t_s$, consider source and drain voltages to be approximately equal

MOSFETS as Switches: Speed Considerations

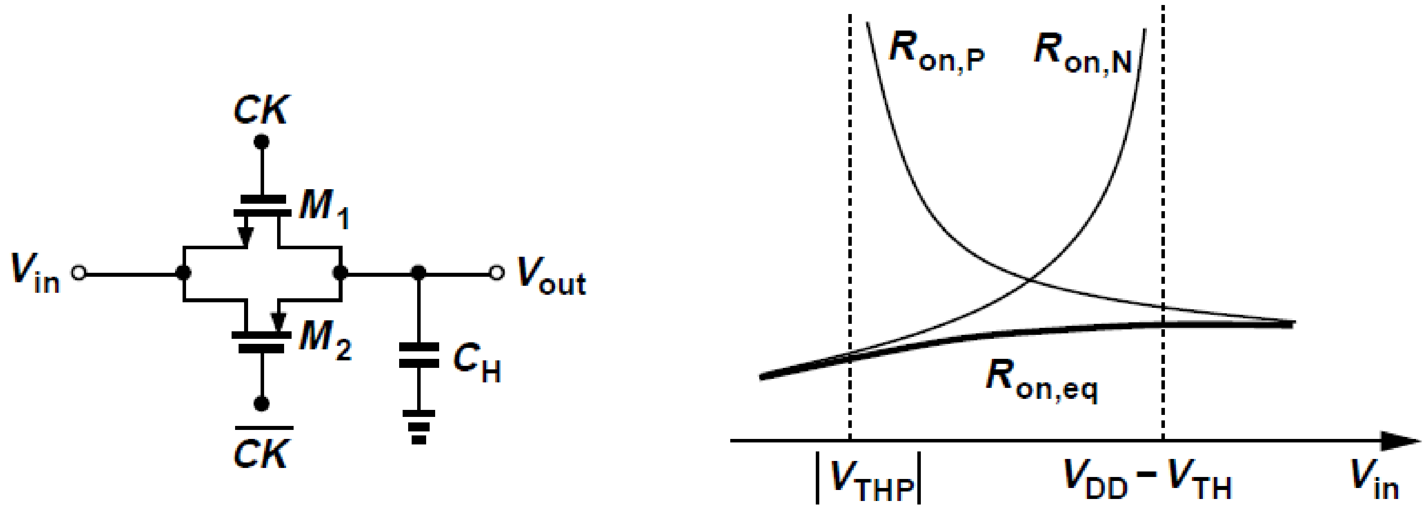
- **Sampling speed is given by two factors: switch on-resistance and sampling capacitance**
- **For higher speed, large aspect ratio and small capacitance are needed**
- **On-resistance also depends on input level for both NMOS and PMOS**



(a) (b)

MOSFETS as Switches: Speed Considerations

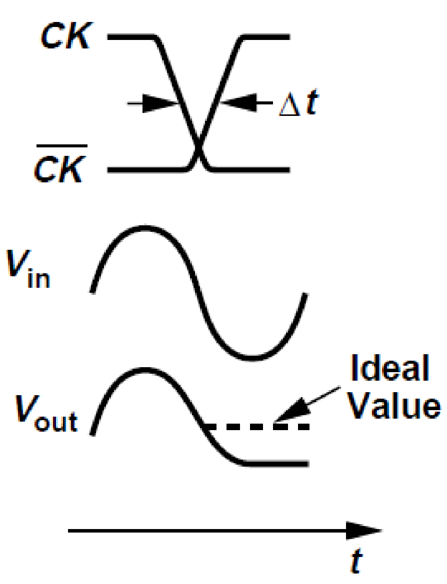
- To allow greater input swings, we can use “complementary” switches, requiring complementary clocks [Fig. (a)]
- Equivalent on-resistance shows following behavior [Fig. (b)], revealing much less variation

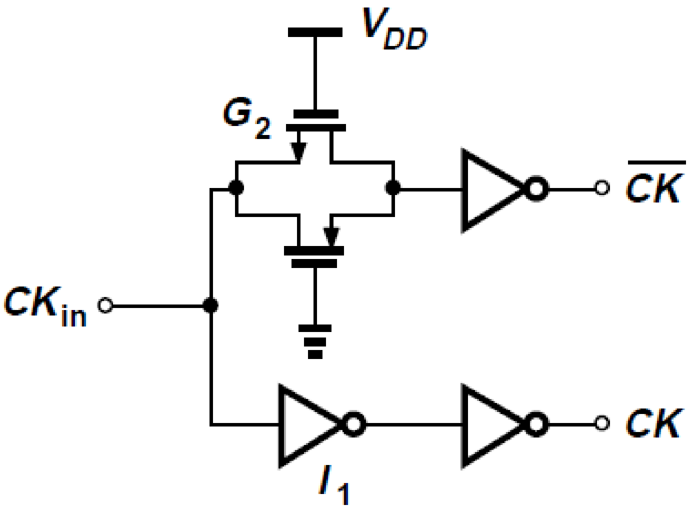


(a) (b)

MOSFETS as Switches: Speed Considerations

- **For high speed signals, NMOS and PMOS switches must turn off simultaneously to avoid ambiguity in sampled value**
- **If NMOS turns off Δt seconds before PMOS, output tends to track input for the remaining Δt seconds, causing distortion**
- **For moderate precision, circuit below is used to provide complementary clocks**

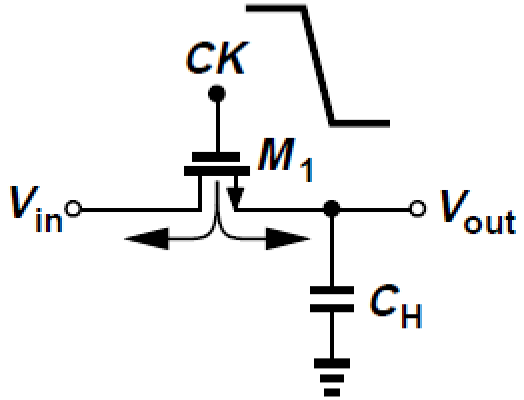




MOSFETS as Switches: Precision Considerations

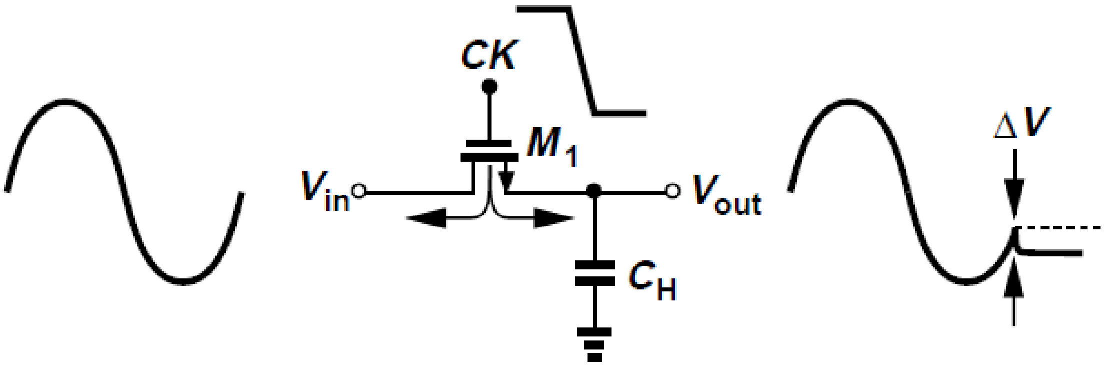
- **Speed trades with precision**
- **<u>Channel Charge Injection</u>:**
- **For MOSFET to be on, a channel must exist at the oxide-silicon interface**
- **Assuming $V_{in} \approx V_{out}$, total charge in the inversion layer is**

$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{TH})$$



- **When switch turns off, Q_{ch} exits through the source and drain terminals ("channel charge injection")**

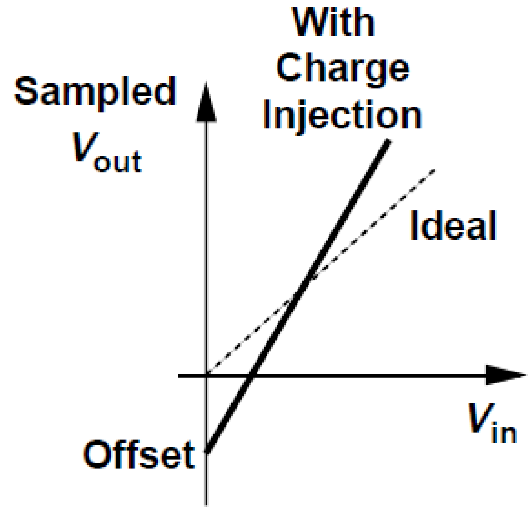
MOSFETS as Switches: Precision Considerations



- Charge injected to the left is absorbed by input source, creating no error
- Charge injected to the right deposited on C_H, introducing error in voltage stored on capacitor
- For half of Q_{ch} injected onto C_H, error (negative pedestal) equals

$$\Delta V = \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{2C_H}$$

MOSFETs as Switches: Precision Considerations



- **If all of the charge is deposited on C_H,**

$$V_{out} \approx V_{in} - \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{C_H}$$

$$V_{out} = V_{in}\left(1 + \frac{WLC_{ox}}{C_H}\right) - \frac{WLC_{ox}}{C_H}(V_{DD} - V_{TH})$$

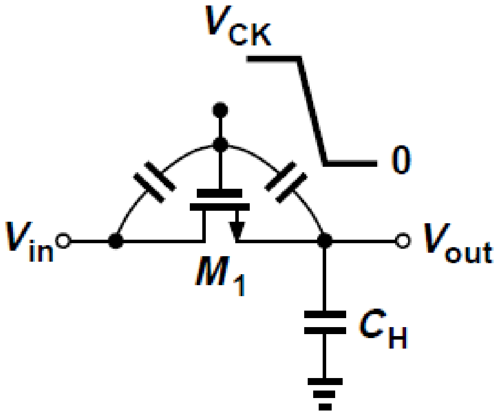
- **Since we assume Q_{ch} is a linear function of V_{in}, circuit exhibits only gain error and dc offset**

MOSFETS as Switches: Precision Considerations

- <u>Clock Feedthrough</u>:
- MOS switch couples clock transitions through C_{GD} or C_{GS}
- Sampled output voltage has error due to this give by

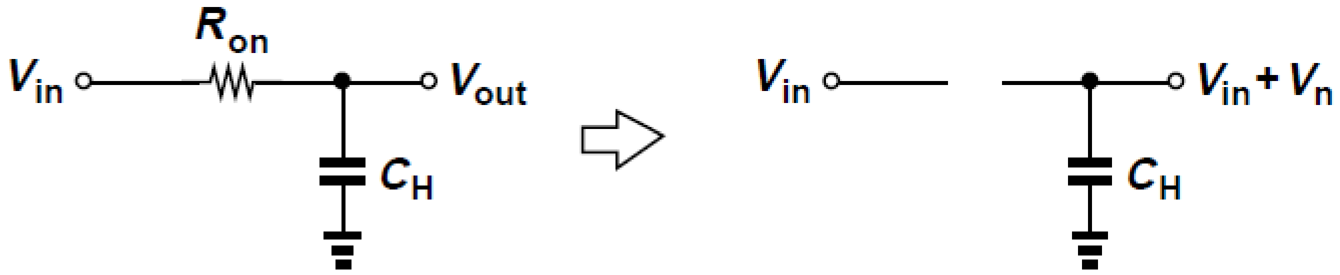
$$\Delta V = V_{CK} \frac{WC_{ov}}{WC_{ov} + C_H}$$

- C_{ov} is the overlap capacitance per unit width
- Error ΔV is independent of input level, manifests as constant offset in the input/output characteristic

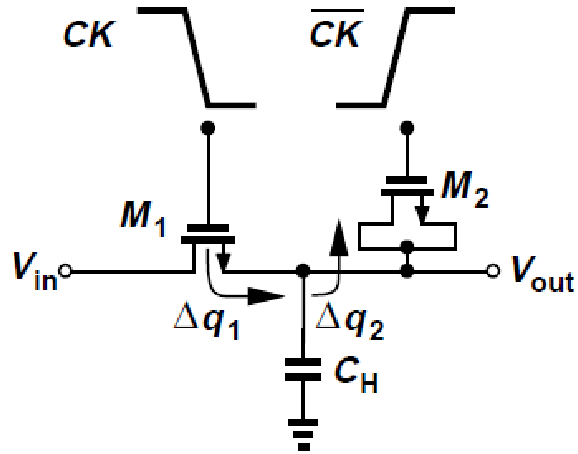


MOSFETS as Switches: Precision Considerations

- **<u>kT/C Noise</u>:**
- **Resistor charging a capacitor gives a total RMS noise voltage of** $\sqrt{kT/C}$.
- **On resistance of switch introduces thermal noise at output which is stored on the capacitor when switch turns off**
- **RMS voltage of sampled noise is still approximately equal to** $\sqrt{kT/C}$.



Charge Injection Cancellation

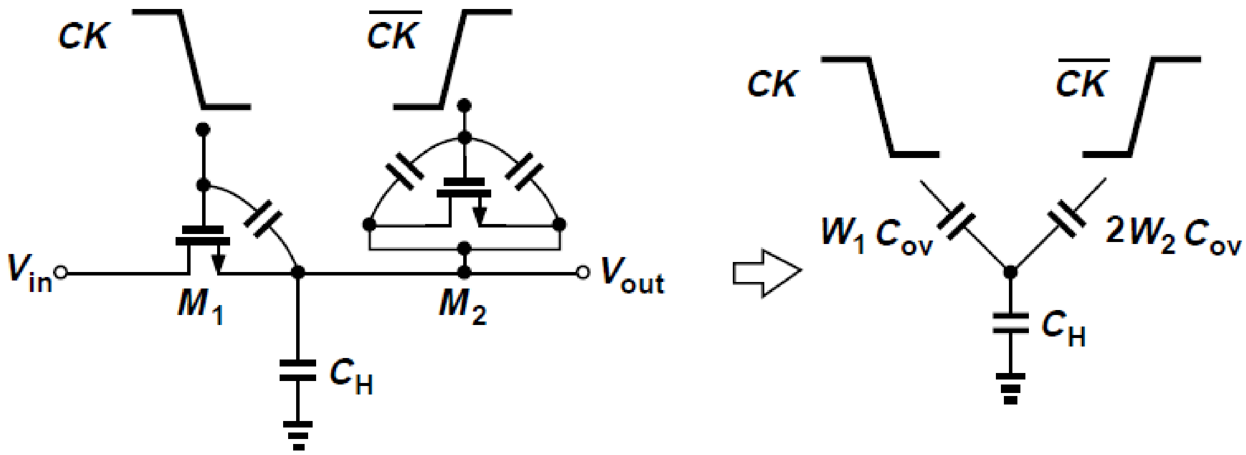


- Charge injected by main transistor removed by a dummy transistor M_2
- M_2 is driven by $\overline{CK}$ so that after M_1 turns off and M_2 turns on, channel charge deposited by M_1 on C_H is absorbed by M_2 to create a channel
- If $W_2 = 0.5W_1$, then charge injected by M_1, Δq_1 is equal to that absorbed by M

$$\Delta q_1 = \frac{W_1 L_1 C_{ox}}{2}(V_{CK} - V_{in} - V_{TH1})$$

$$\Delta q_2 = W_2 L_2 C_{ox}(V_{CK} - V_{in} - V_{TH2})$$

Charge Injection Cancellation

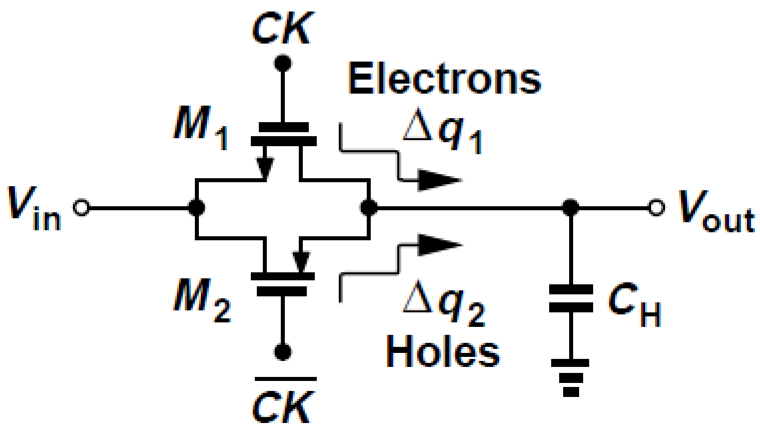


- If $W_2 = 0.5W_1$ and $L_2 = L_1$, effect of clock feedthrough is suppressed
- Total change in V_{out} is zero because

$$-V_{CK}\frac{W_1C_{ov}}{W_1C_{ov}+C_H+2W_2C_{ov}}+V_{CK}\frac{2W_2C_{ov}}{W_1C_{ov}+C_H+2W_2C_{ov}}=0$$

Charge Injection Cancellation

- **Incorporate both PMOS and NMOS devices so that opposite charge packets injected cancel each other**



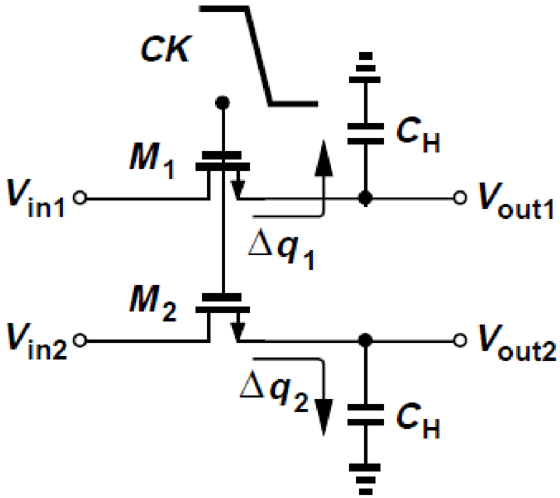
- **For Δq_1 to cancel Δq_2, we must have**

$$W_1 L_1 C_{ox}(V_{CK} - V_{in} - V_{THN}) = W_2 L_2 C_{ox}(V_{in} - |V_{THP}|)$$

- **Cancellation occurs for only one input level**
- **Clock feedthrough is not completely suppressed since C_{GD} of NFETs is not equal to that PFETs**

Charge Injection Cancellation

- Charge injection appears as a common-mode disturbance, may be countered by differential operation

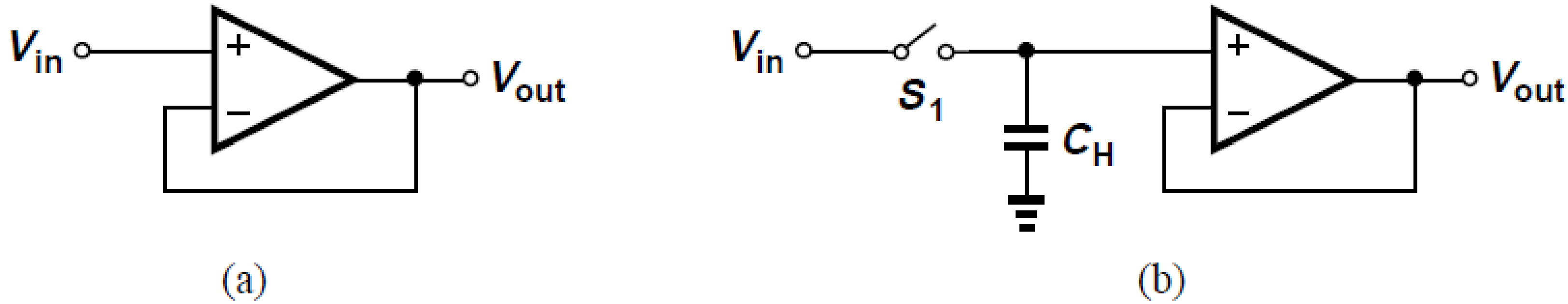


∀ $\Delta q_1 = \Delta q_2$ only if $V_{in1} = V_{in2}$, thus overall error is not suppressed for differential signals

- Removes constant offset and nonlinear component

$$\begin{aligned}\Delta q_1 - \Delta q_2 &= WLC_{ox}[(V_{in2} - V_{in1}) + (V_{TH2} - V_{TH1})] \\ &= WLC_{ox}\left[V_{in2} - V_{in1} + \gamma\left(\sqrt{2\phi_F + V_{in2}} - \sqrt{2\phi_F + V_{in1}}\right)\right]\end{aligned}$$

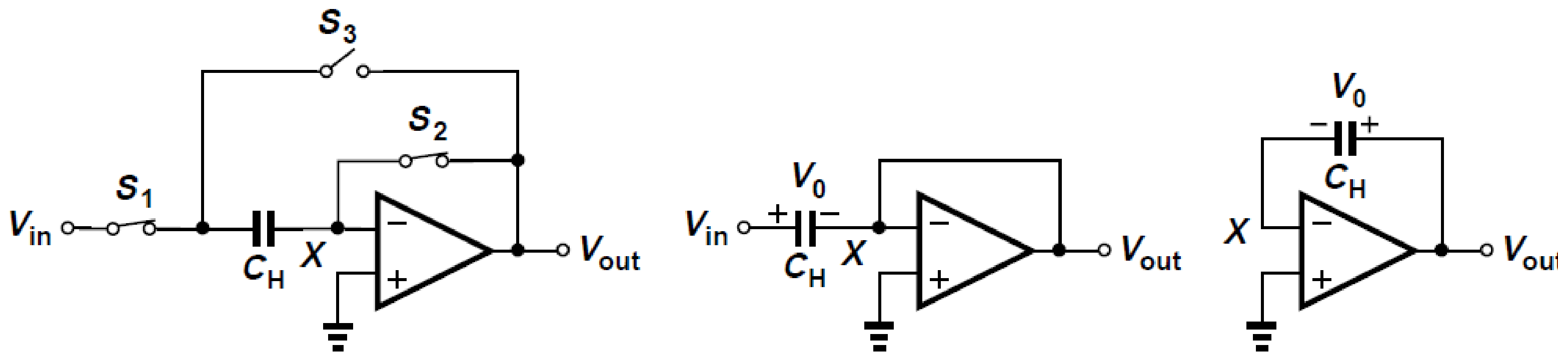
Unity-Gain Sampler/ Buffer



- **For discrete-time applications, unity-gain amplifier [Fig. (a)] requires a sampling circuit [Fig. (b)]**
- **Accuracy limited by input-dependent charge injected by S_1 onto C_H**

Unity-Gain Sampler/ Buffer

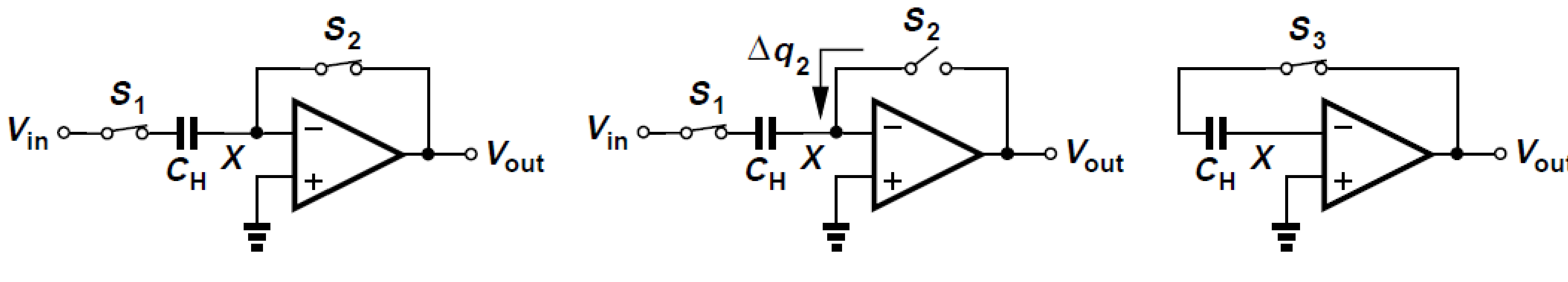
- Consider the topology shown in Fig. (a)



(a) (b) (c)

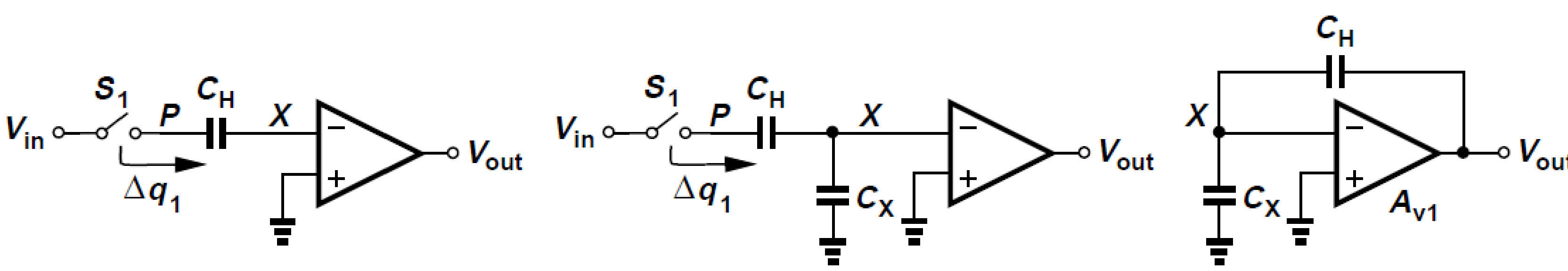
- In sampling mode, S_1 and S_2 are on, S_3 is off yielding circuit in Fig. (b)
- Thus, $V_{out} = V_X \approx 0$, and the voltage across C_H tracks V_{in}
- At $t = t_0$, when $V_{in} = V_0$, S_1 and S_2 turn off and S_3 turns on, yielding circuit of Fig. (c) [amplification mode]
- Op amp requires node X is still a virtual ground, V_{out} rises to approximately V_0 → "frozen" for processing by subsequent stages

Unity-Gain Sampler/ Buffer



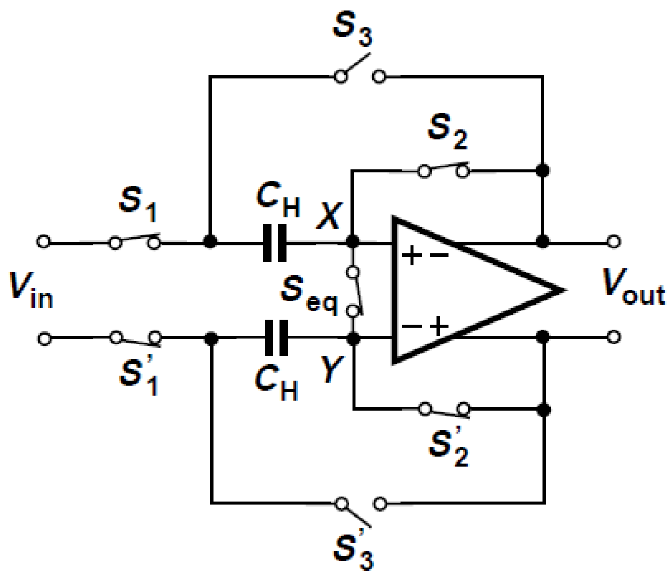
(a) (b) (c)

- S_2 turns off slightly before S_1 during transition from sampling mode to amplification mode
- Charge injected by S_2, Δq_2 is input-independent and constant, producing only an offset
- After S_2 turns off, total charge at node X stays constant and charge injected by S_1 does not affect output voltage



(a) (b) (c)

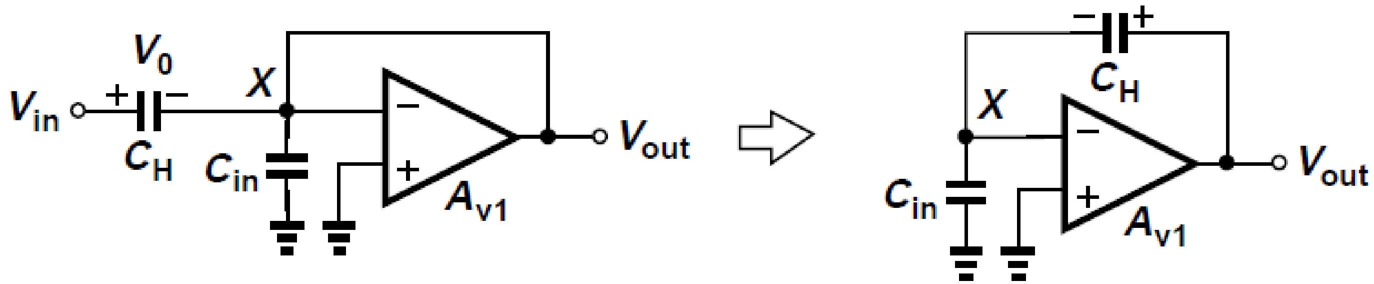
Unity-Gain Sampler/ Buffer



- **Input-independent charge injected by S_2 can be cancelled by differential operation as shown**
- **Charge injected by S_2 and S_2' appears as common-mode disturbance at nodes *X* and *Y***
- **Charge injection mismatch between S_2 and S_2' resolved by adding another switch S_{eq} that turns off slightly after S_2 and S_2', equalizing the charge at nodes *X* and *Y***

Unity-Gain Sampler/ Buffer

- **Precision Considerations**:
- **Assume op-amp has a finite input capacitance C_{in} and calculate output voltage when circuit goes from sampling to amplification mode**



- **It can be shown from the above fig. that**

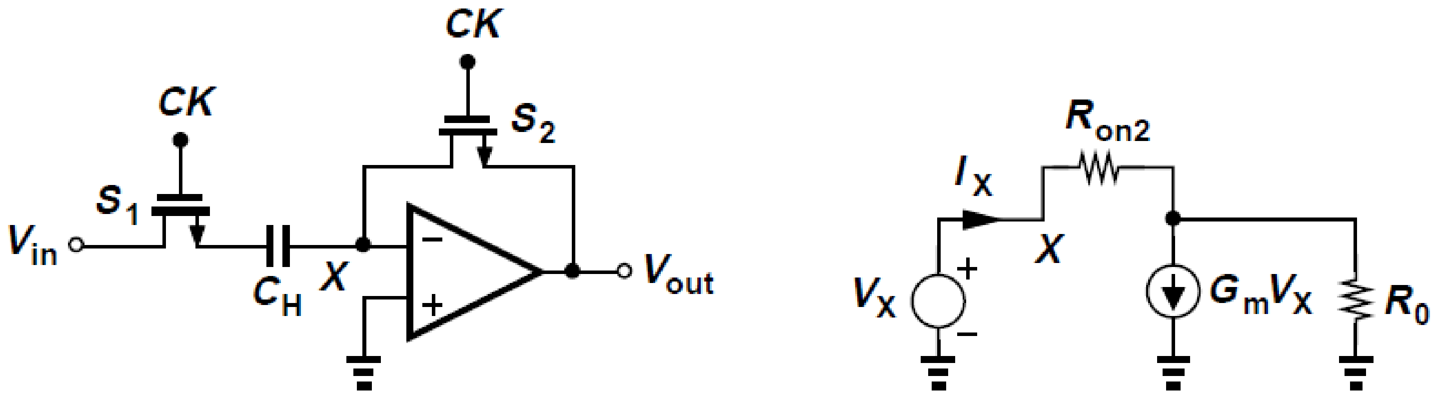
$$V_{out} = \frac{V_0}{1 + \frac{1}{A_{v1}}\left(\frac{C_{in}}{C_H} + 1\right)}$$

$$\approx V_0\left[1 - \frac{1}{A_{v1}}\left(\frac{C_{in}}{C_H} + 1\right)\right]$$

- **Circuit suffers from gain error of approximately** $-(C_{in}/C_H + 1)/A_{v1}$

Unity-Gain Sampler/ Buffer

- **<u>Speed Considerations</u>:**
- **In sampling mode, circuit appears as in Fig. (a)**



(a) (b)

- **Use equivalent circuit of Fig. (b) to find time constant in sampling mode**
- **Total resistance in series with C_H is R_{on1} and the resistance between X and ground, R_X**

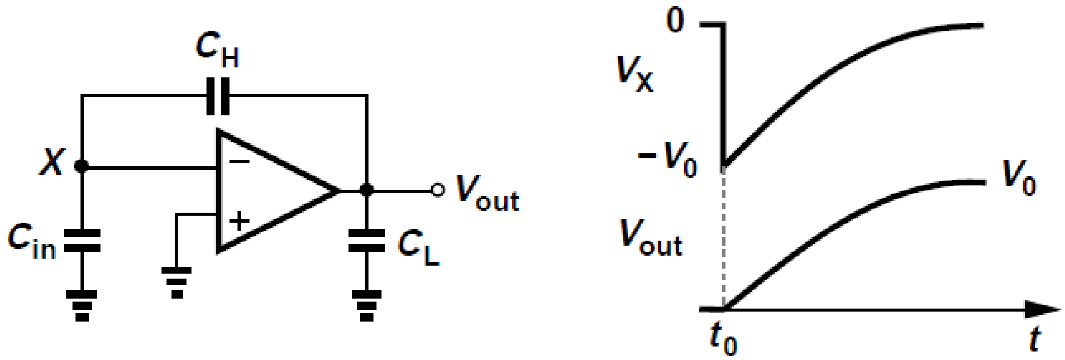
$$R_X = \frac{R_0 + R_{on2}}{1 + G_m R_0}$$

Unity-Gain Sampler/ Buffer

- **Since typically** $R_{on2} \ll R_0$ **and** $G_m R_0 \gg 1$**,** $R_X \approx 1/G_m$
- **Time constant in sampling mode is thus**

$$\tau_{sam} = \left(R_{on1} + \frac{1}{G_m}\right) C_H$$

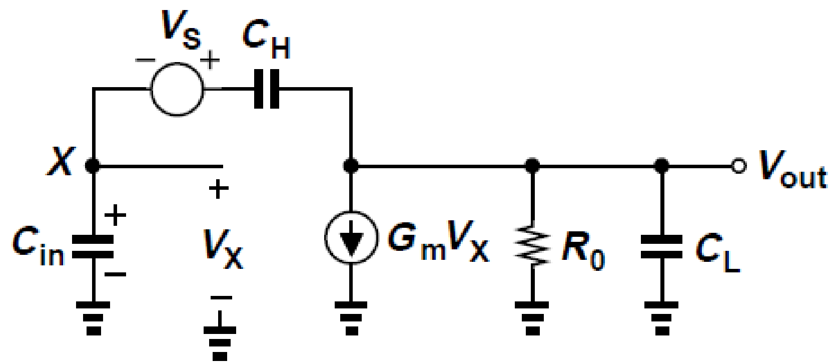
- **Consider circuit as it enters amplification mode**



- **Circuit must begin with** $V_{out} \approx 0$ **and eventually produce** $V_{out} \approx V_0$
- **For relatively small** C_{in}**, voltages across** C_L **and** C_H **do not change instantaneously so that** $V_X = -V_0$ **at the beginning of amplification**

Unity-Gain Sampler/ Buffer

- **Represent charge on C_H by a voltage source V_S that goes from zero to V_0 at $t = t_0$, while C_H carries no charge itself**



- **The transfer function $V_{out}(s)/V_{in}(s)$ can be obtained as**

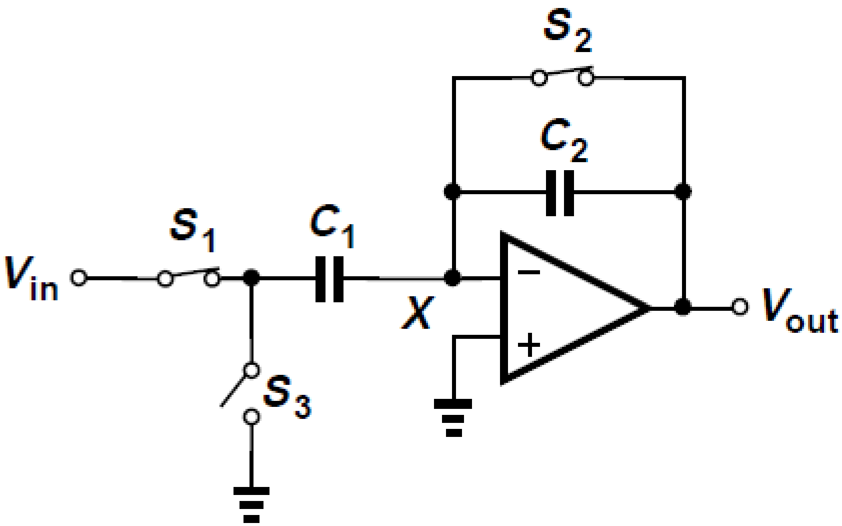
$$\frac{V_{out}}{V_S}(s) = \frac{(G_m + C_{in}s)C_H}{(C_L C_{in} + C_{in}C_H + C_H C_L)s + G_m C_H}$$

- **This response is characterized by a time constant independent of op-amp output resistance**

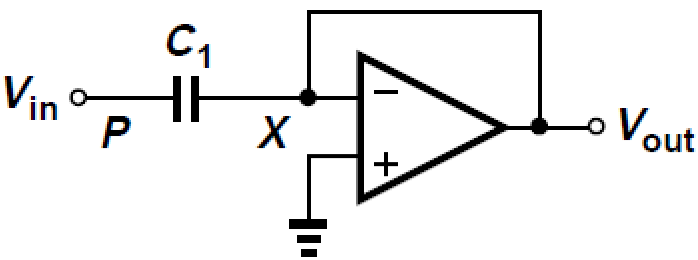
$$\begin{aligned}\tau_{amp} &= \frac{C_L C_{in} + C_{in}C_H + C_H C_L}{G_m C_H} \\ &= \frac{1}{G_m}\left[C_{in} + \left(1 + \frac{C_{in}}{C_H}\right)C_L\right]\end{aligned}$$

Noninverting Amplifier

- In non-inverting amplifier of Fig. (a), in sampling mode, S_1 and S_2 are on while S_3 is off, creating a virtual ground at X and allowing voltage across C_1 to track V_{in} [Fig. (b)]



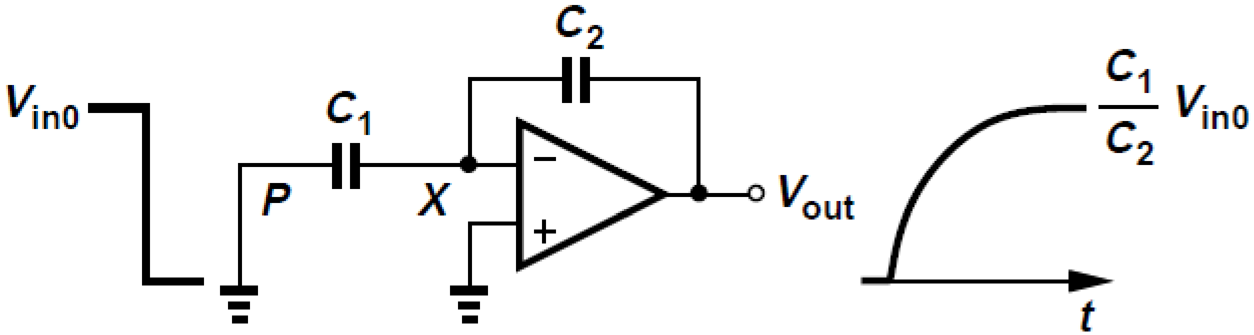
(a)



(b)

Noninverting Amplifier

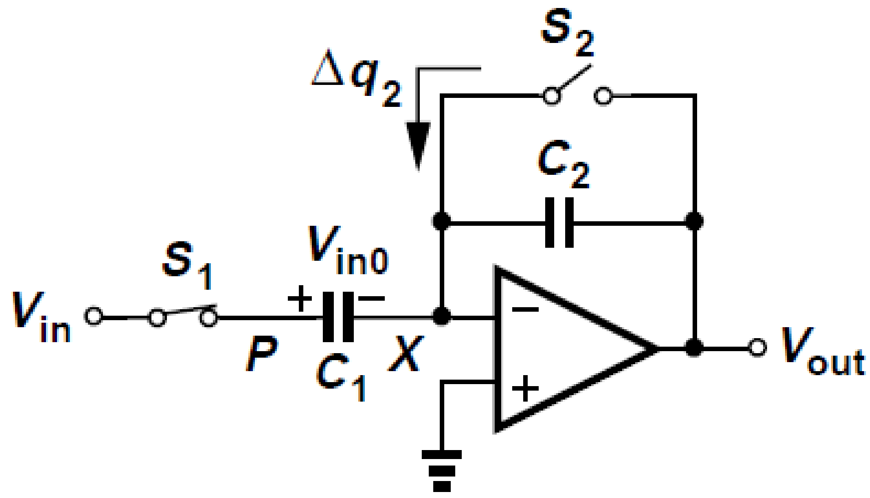
- At the end of sampling mode, S_2 turns off first, injecting a constant charge Δq_2 onto node X, after which S_1 turns off and S_3 turns on [Fig. (c)]
- Since V_P goes from V_{in0} to 0, output voltage changes from 0 to approximately $V_{in0}(C_1/C_2)$, providing a gain of C_1/C_2
- Called a "noninverting amplifier" since output polarity is the same as V_{in0} and the gain can be greater than unit



(c)

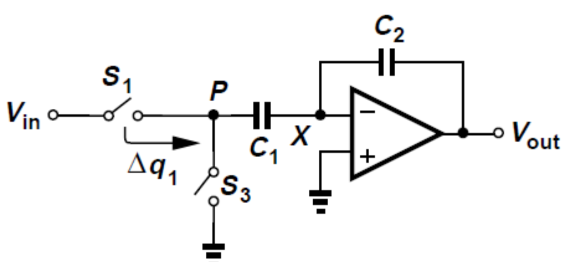
Noninverting Amplifier

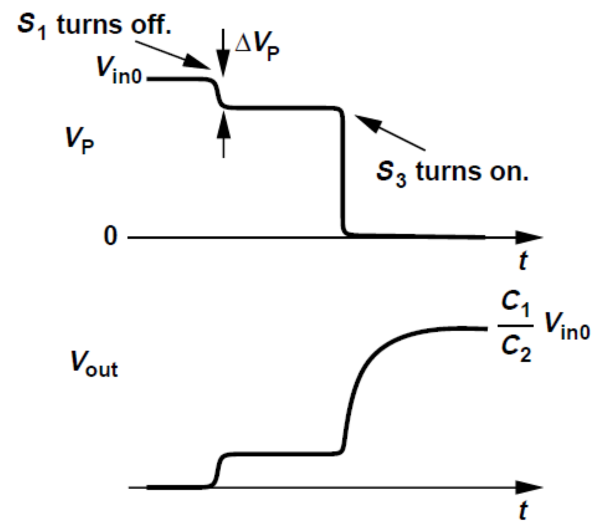
- **Noninverting amplifier avoids input-depending charge injection by turning off S_2 before S_1**
- **After S_2 is off, total charge at node X remains constant, making the circuit insensitive to charge injection of S_1 or charge "absorption" of S_3**



Noninverting Amplifier

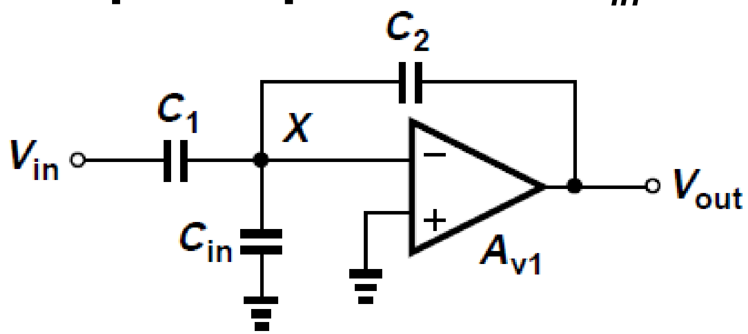
- Charge injected by S_1, Δq_1 changes voltage at node P by $\Delta V_P = \Delta q_1/C_1$ and output voltage by $-\Delta q_1 C_1/C_2$
- After S_3 turns on, V_P becomes zero so overall change in V_P is $0 - V_{in0} = -V_{in0}$, producing overall change in output of $-V_{in0}(-C_1/C_2) = V_{in0}C_1/C_2$
- V_P goes from V_0 to 0 with a perturbation due to S_1
- Since output is measure after node P is connected to ground, charge injected by S_1 does not affect final outpu





Noninverting Amplifier

- **<u>Precision Considerations</u>:**
- **Calculate actual gain if op amp has finite open-loop gain of A_{v1} and input capacitance C_{in}**



$$\left|\frac{V_{out}}{V_{in}}\right| \approx \frac{C_1}{C_2}\left(1 - \frac{C_2 + C_1 + C_{in}}{C_2} \cdot \frac{1}{A_{v1}}\right)$$

- **It can be shown that**

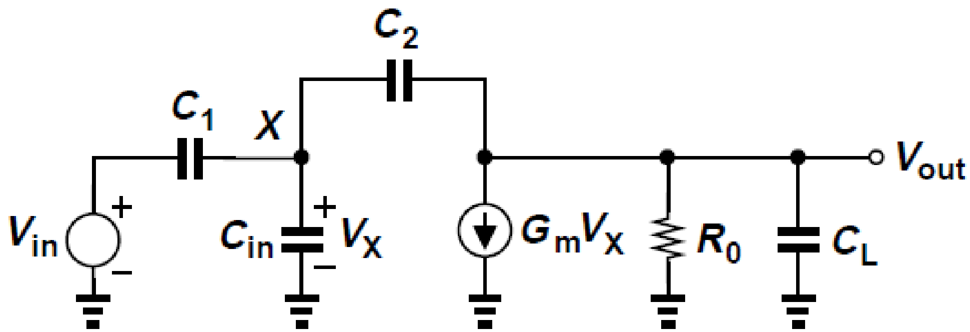
$(C_2 + C_1 + C_{in})/(C_2 A_{v1})$

- **Amplifier suffers from a gain error of**

Gain error increases with the nominal gain C/C

Noninverting Amplifier

- **<u>Speed Considerations</u>:**
- **Consider equivalent circuit in amplification mode [Fig. (a)]**



(a)

- **It can be shown for a large $G_m R_0$ that**

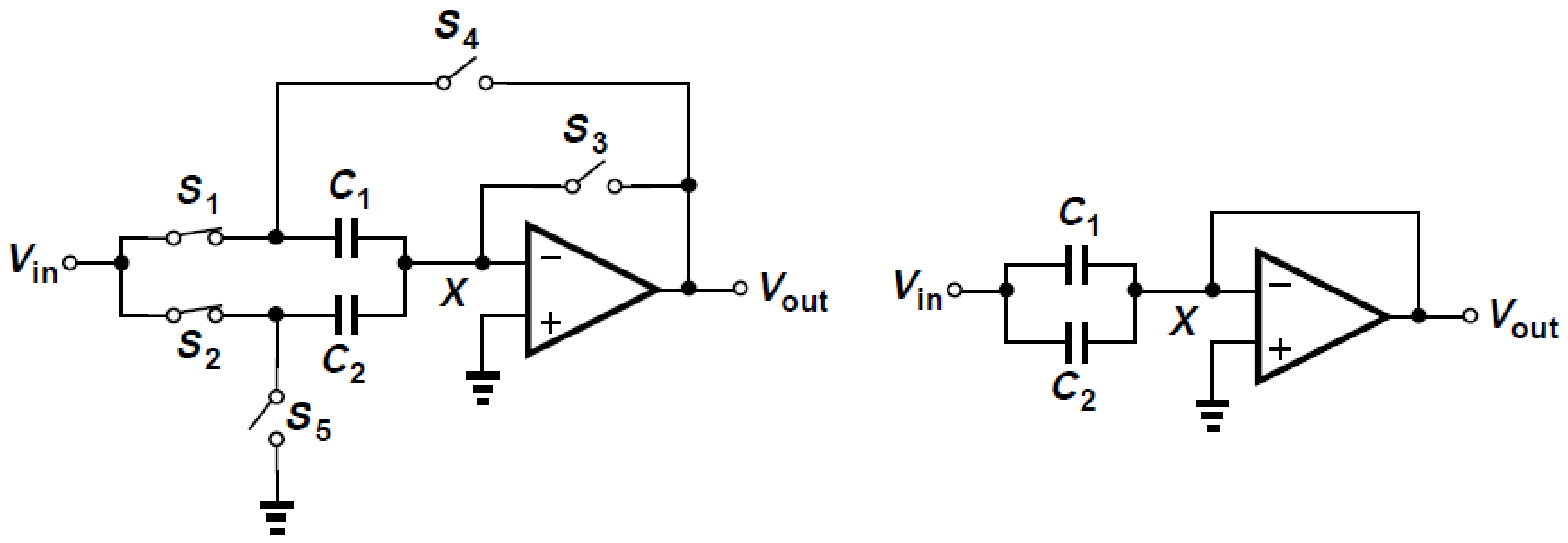
$$\frac{V_{out}}{V_{in}}(s) \approx \frac{-C_{eq}\dfrac{C_1}{C_1 + C_{in}}(G_m - C_2 s)R_0}{R_0(C_L C_{eq} + C_L C_2 + C_{eq} C_2)s + G_m R_0 C_2}$$

- **This gives a time constant of**

$$\tau_{amp} = \frac{C_L C_{eq} + C_L C_2 + C_{eq} C_2}{G_m C_2}$$

Precision Multiply-by-Two Circuit

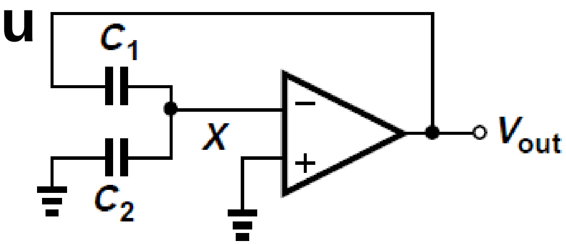
- **Topology shown in Fig. (a) provides a nominal gain of two while achieving higher speed and lower gain error**



(a) (b)

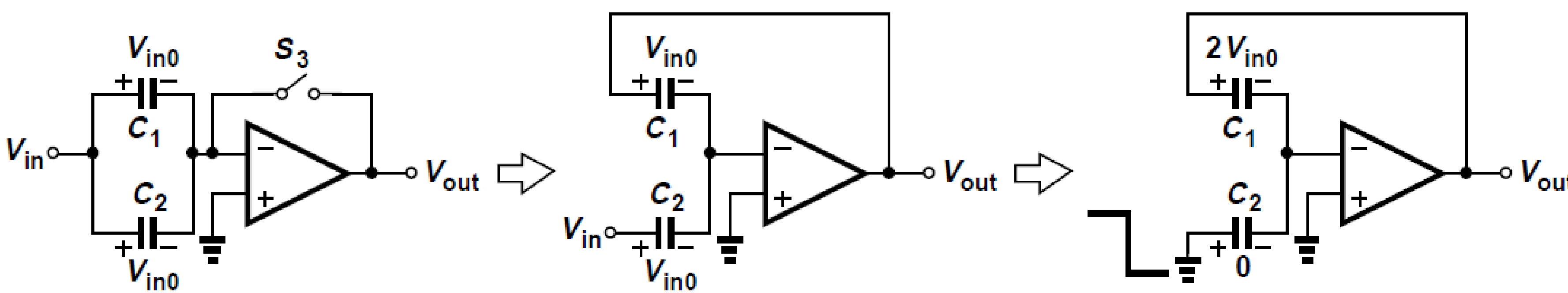
- **Incorporates two equal capacitors $C_1 = C_2 = C$**
- **In sampling mode [Fig. (b)], node X is a virtual ground, allowing voltage across C_1 and C_2 to track V_{in}**

Precision Multiply-by-Two Circuit

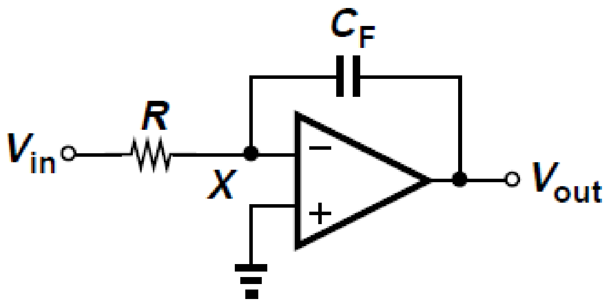
- **During transition to amplification mode [Fig. (c)], S_3 turns off first, placing C_1 around op-amp and left plate of C_2 is grounded**
- **At the moment S_3 turns off, total charge on C_1 and C_2 equals $2V_{in0}C$ and since voltage across C_2 approaches zero in amplification mode, final voltage across C_1 and hence outpu** 

$2V_{in0}$

(c)

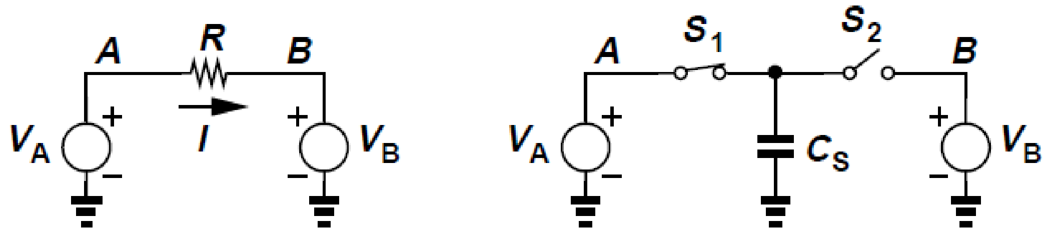


Switched-Capacitor Integrator



- **Output of a continuous-time integrator can be expressed as**

$$V_{out} = -\frac{1}{RC_F}\int V_{in}dt$$



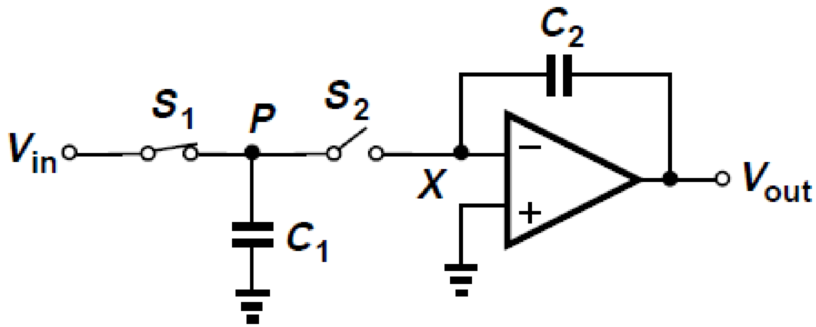
(a) (b)

- **In Fig. (a), resistor *R* carries a current of *(V_A – V_B)/R***
- **In circuit of Fig. (b), C_S is alternately connected to nodes *A* and *B* at a clock rate f_{CK}**
- **Average current flowing from *A* to *B* is the charge moved in one clock period**
- **Can be viewed as a resistor of value** $(C_S f_{CK})^{-1}$

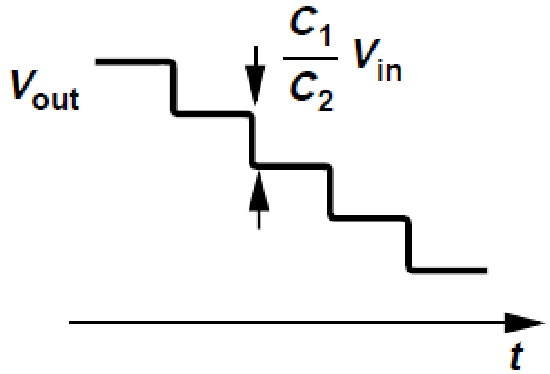
$$\overline{I_{AB}} = \frac{C_S(V_A - V_B)}{f_{CK}^{-1}}$$

$$= C_S f_{CK}(V_A - V_B)$$

Switched-Capacitor Integrator



(a)



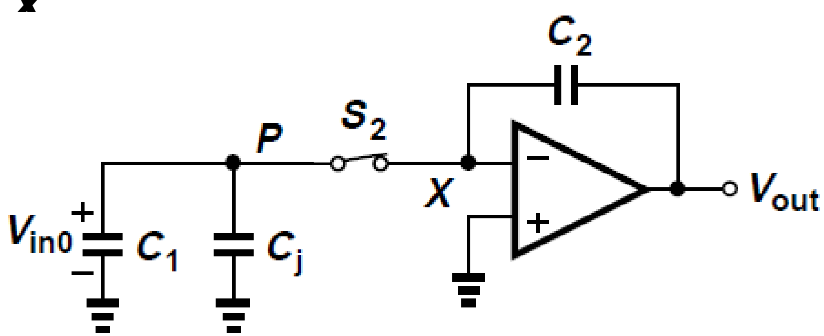
(b)

- **Fig. (a) shows discrete-time integrator**
- **In every clock cycle, C_1 absorbs a charge equal to C_1V_{in} when S_1 is on and deposits it on C_2 when S_2 is on**
- **If V_{in} is constant, output changes by $V_{in}C_1/C_2$ every clock cycle [Fig. (b)]**
- **Final value of V_{out} after clock cycle can be written as**

$$V_{out}(kT_{CK}) = V_{out}[(k-1)T_{CK}] - V_{in}[(k-1)T_{CK}] \cdot \frac{C_1}{C_2}$$

Switched-Capacitor Integrator

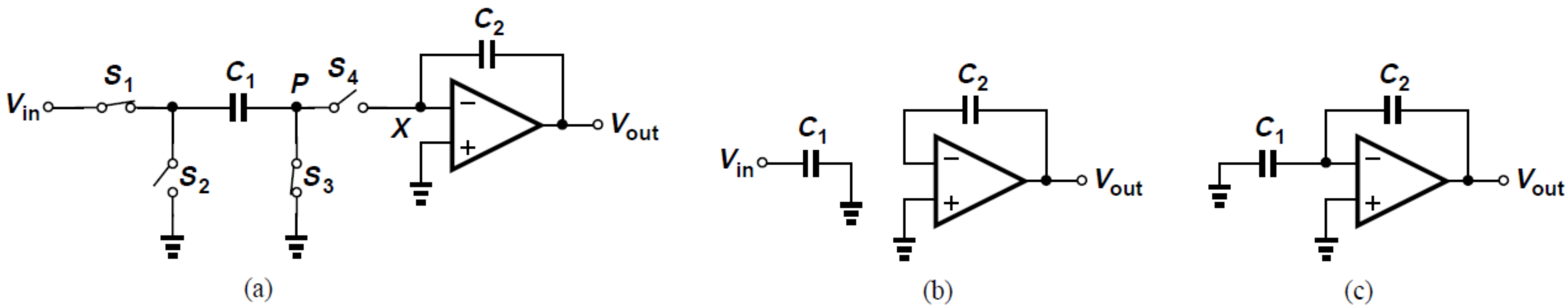
- **Input-dependent charge injection of S_1 introduces nonlinearity in output voltage**
- **Nonlinear capacitance at node P resulting from source/drain junctions of S_1 and S_2 leads to a nonlinear charge-to-voltage conversion when C_1 is switched to X**



- **Charge stored on the total junction capacitance, C_j is not equal to $V_{in0}C_j$, but rather equal to**

$$q_{cj} = \int_0^{Vin0} C_j dV.$$

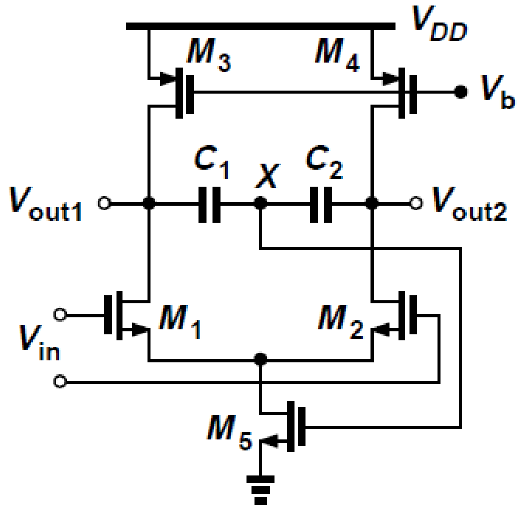
Switched-Capacitor Integrator



- Circuit of Fig. (a) resolves the issues in the simple integrator
- In sampling mode [Fig. (b)], S_1 and S_3 are on, S_2 and S_4 are off, allowing voltage across C_1 to track V_{in} while op amp and C_2 hold previous value
- In the transition to integration mode, S_3 turns off first, injecting a constant charge onto C_1, S_1 turns off next, and subsequently S_2 and S_4 turn on
- Charge stored on C_1 is transferred to C_2 through the virtual ground node

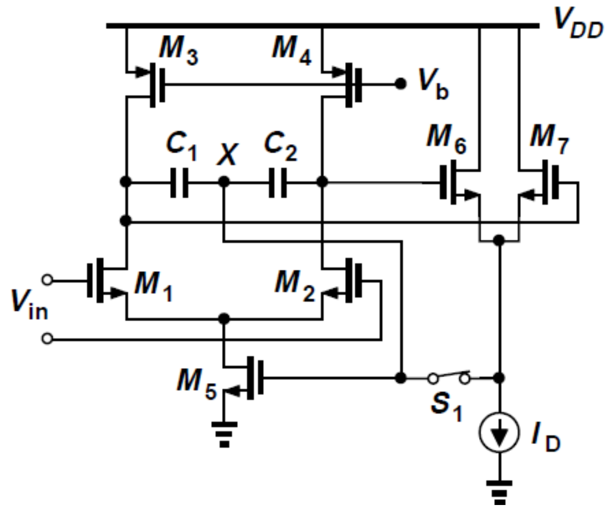
Switched-Capacitor Common-Mode Feedback

- In switched-capacitor common-mode feedback, outputs are sensed by capacitors rather than resistors



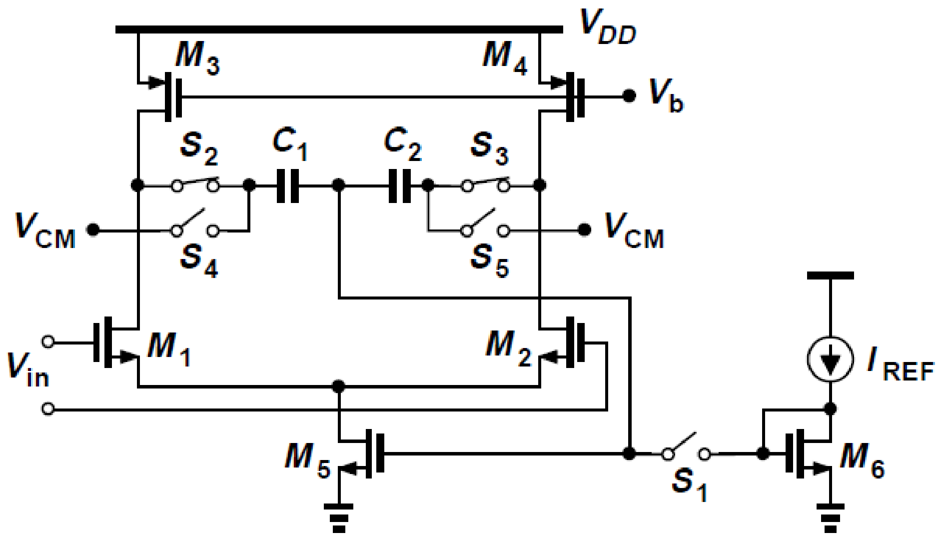
- In circuit above, equal capacitors C_1 and C_2 reproduce at node X the average of the changes in each output voltage
- If V_{out1} and V_{out2} experience a positive CM change, then V_X and I_{D5} increase, pulling V_{out1} and V_{out2} down
- Output CM is V_{GS2} plus voltage across C_1 and C_2

Switched-Capacitor Common-Mode Feedback



- Voltage across C_1 and C_2 defined as shown above
- During CM level definition, amplifier differential input is zero and S_1 is on
- M_6 and M_7 act as a linear sense circuit since their gate voltages are nominally equal
- Circuit settles such that output CM level is equal to $V_{GS6,7} + V_{GS5}$
- At the end of this mode, S_1 turns off, leaving a voltage equal to $V_{GS6,7}$ across C_1 and C_2

Switched-Capacitor Common-Mode Feedback



- For more accuracy in CM level definition, above circuit may be used
- In the reset mode, one plate of C_1 and C_2 is switched to V_{CM} while the other is connected to the gate of M_6
- Each capacitor sustains a voltage of $V_{CM} - V_{GS6}$
- In the amplification mode, S_2 and S_3 are on and the other switches are off, yielding an output CM level of $V_{CM} - V_{GS6} + V_{GS5}$, which is equal to V_{CM} if I_{D3} and I_{D4} are copied properly from I_{REF} so that $V_{GS5} = V_{GS6}$