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OrCAD Capture User Guide

Product Version 16.5
May 2011

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Before you begin

Welcome

OrCAD® Capture (henceforth referred to as Capture) is a schematic design tool set for the Windows environment. With Capture, you can draft schematics and produce connectivity and simulation information for printed circuit boards and programmable logic designs.

Capture is fully integrated in a number of different tool suites, including OrCAD PSpice, and PCB board layout tool set. Refer to OrCAD Product Installation Guide for Windows for information on hardware and software requirements.

How to use this guide

This guide is designed to make the most of the advantages of onscreen books. The table of contents, index, and cross references provide instant links to the information you need. Just click on the text and jump.

If you find printed paper helpful, print only the section you need at the time. When you want an in-depth tutorial, print the example. When you want a quick reminder of a procedure, print the procedure.

Symbols and conventions

Our documentation uses a few special symbols and conventions.

Notation	Examples	Description
Bold text	**Import Measurements**, **Modified LSQ,** **PDF Graph**	Indicates that text is a menu or button command, dialog box option, column or graph label, or drop-down list option
Icon graphic		Shows the toolbar icon that should be clicked with your mouse button to accomplish a task
Lowercase file extensions	.aap, .sim, .drt	Indicates a file name extension

Using Capture

OrCAD Capture can be used by designers to create schematics and produce connectivity and simulation information for printed circuit boards and programmable logic designs. You can use OrCAD Capture to create designs for other EDA applications by choosing to set up a PSpice project, PCB project, or programmable logic project when you start a new project. You can set your user preferences for the appearance of all designs on your system, and set up design options for each particular project or design you create.

Capture provides standard libraries that can be used to design schematics. You can also create your own library.

In Capture, you can drag and drop schematic folders and pages in the project manager in the session window. You can place parts and pins in Capture's schematic editor, then connect the parts with buses, wires, off-page connectors, and more. Use a multitude of Capture tools to edit the design, including the part editor, the Edit menu and the pop-up menu. Create your own parts and part packages, or use the standard libraries provided with Capture.

The property editor of Capture shows you properties of all or selected parts in your schematic design one page at a time. You can use the property editor to add, change, or delete user properties and property values in your own custom filter for any design.

Capture also includes verification and reporting, printing, and netlisting features for your schematic page, folder, or entire design.

For more information about	See
OrCAD Capture	Capture User's Guide
OrCAD Capture messages	Capture Messages Reference Guide
Libraries	OrCAD Supplied Libraries Reference Guide
Toolbar commands and shortcut keys	OrCAD Capture Quick Reference
PSpice simulations	PSpice User's Guide
PCB design	Allegro PCB Editor User Guide
PCB design cycle	OrCAD Flow Tutorial

Related documentation

In addition to this guide, you can find technical product information on the Cadence website www.cadence.com/orcad. The table below

describes the types of technical documentation provided with Capture.

This documentation component . . .	Provides this . . .
This guide— OrCAD Capture User Guide	A comprehensive guide for understanding and using the features available in OrCAD Capture.
Help system (automatic and manual)	Provides comprehensive information for understanding the features in Capture and using them to perform schematic capture. Capture provides help in two ways: context-sensitive help and manual help. Context-sensitive help displays help topics that are associated with your current activity when you press the F1 key or click the Help button on the active dialog box or window within the Capture workspace and interface. It provides immediate access to information that is relative to your current task. The manual method gives you full navigational access to all topics and resources outside of the help system. Using either method, help topics include: ■ Explanations and instructions for common tasks ■ Descriptions of menu commands, dialog boxes, tools on the toolbar and tool palettes, and the status bar ■ Glossary terms ■ Reference information
Online interactive tutorial	A series of self-paced interactive lessons. You can practice what you've learned by going through the tutorial's specially designed exercises that interact directly with Capture. You can start the tutorial by choosing Learning Capture from the Help menu.

This documentation component . . .	Provides this . . .
OrCAD Capture Quick Reference Card	Concise descriptions of the commands, shortcuts, and tools available in Capture

1

Basic elements of Capture design

This chapter covers:

- “Processing your PCB design” on page 41
- “Instances and occurrences” on page 43
- “Flat vs. hierarchical designs” on page 45
- “Using orthogonal drag” on page 49
- “Non-Linear Editor (Fisheye)” on page 52
- “PCB Editor 3D Footprint Viewer” on page 53
- “Part packaging” on page 57
- “Programmable logic projects” on page 59
- “Working with multiple windows” on page 61
- “Auto recovery” on page 64
- “Moving around in the editors” on page 66
- “Capture directory map” on page 89
- “Capture configuration” on page 91
- “Intertool communication” on page 93

Processing your PCB design

The PCB design process typically involves placing and connecting parts; specifying how they're to be packaged; uniquely identifying them; adding information for simulation, synthesis, board layout,

purchasing, or other external functions; and incorporating information from external functions.

Once you finish a first pass at placing and connecting parts, use the commands on the Tools menu in the project manager to complete the process. Click on the command names in the figure for information about the tool commands.

As shown in the figure, you use Annotate, Design Rules Check, and Cross Reference to package the parts in your design and make sure there are no unconnected parts, unwanted connections, or other invalid design conditions. In practice, you might run these tools several times before moving on to the next phase.

Note: Generally, you should run Design Rules Check to verify your design before you generate a netlist. This allows for more efficient netlist creation, and you can concentrate on netlist-specific problems if they should occur during the Create Netlist process. Design Rules Check warns you if certain conditions exist in your design. The severity of the specific problem may prevent completion of the design. Other conditions are subject to your judgment, and may be of no consequence. Once you are satisfied with the results of design tests like Design Rules Check, then proceed with the creation of a netlist.

You can add properties or change their values at any point, and there are several ways to do this. If you want to change the value of one or two properties, just edit them on the schematic page. To edit properties on many parts at the same time, use Update Properties or Capture's built-in spreadsheet editor (from the Edit menu, choose Browse and then Parts). If you're more comfortable editing in a full-featured spreadsheet or database program, use Export Properties to write design data out and Import Properties to read the changes back in.

Once you're satisfied with your design, use Create Netlist to create a netlist in any of the formats supported by Capture. This is often the point at which you use Bill of Materials to create a list of parts used in the design.

Instances and occurrences

This section gives you an overview of instances and occurrences, then discusses:

"Effects of applying edits to a part" on page 44

"Preferred modes for design processing" on page 44

"How Capture uses instance and occurrence properties" on page 45

It is important to understand the concept of part instances and part occurrences when using Capture to create your schematic designs.

A part instance is a part you have placed on a schematic page. A part occurrence is created each time the part instance occurs in a schematic that is within the design hierarchy. So, for example, placing a part on a schematic page in your design creates both an instance and an occurrence. You can assign properties to the part instance, in which case the property (and its associated value) will "shine through" to each part occurrence unless the value is specifically replaced by a value on an individual part occurrence. The Property editor window graphically illustrates the state of instance and occurrence properties.

Note: Logical and physical view properties from Capture v7.2 (and older) versions map logical view properties into instances, and physical view properties into occurrences.

The instance property values shines through to the occurrence as long as the occurrence property values have not been edited in any way. When you explicitly edit an occurrence property value or when Capture modifies it via one of its tools, the occurrence values overrides the instance value. Only the occurrence value will be placed in the netlist.

If you...	**The result will be...**
place a part on an unused page in your design	only instance properties on that part.
place one part in the root schematic	one set of instance properties and one set of occurrence properties on that part.

do not modify the occurrence properties on an object	instance properties will "shine through" on the occurrence. The instance properties themselves may be shining through from the library definition (or design cache if the two differ
edit a part in a library	no affect on the part in any project. Use the Update Cache command or Replace Cache command to bring library changes into a design.

Effects of applying edits to a part

You can edit part instances in the schematic page editor by selecting a part instance and choosing the Part command from the Edit menu. Once you finish editing the part instance, you can apply the changes to every occurrence in the design by clicking the Update All button, or to just the single (current) part instance by clicking the Update Current button.

Update All replaces the old part in the design cache with the newly edited part and breaks the link with the original library.

Update Current creates a new part in the design cache. The new part has no link to the original library.

In either case:

1. The edited part doesn't exist in a library, so the only way to place a copy of it is to use the Copy and Paste commands on the schematic page editor's Edit menu.
2. It has no link with the original library, so it's not affected by the Update Cache command. To restore its link with the original library, you must choose the Replace Cache command from the project manager's Design menu. For more information, see Replacing a part.

Preferred modes for design processing

Capture determines and recommends a preferred mode for processing your design based on the type of project flow, type of design with respect to complex or simple hierarchy, and whether occurrence properties already exist on the design.

The Cross Reference Parts dialog box is an example of where you can choose to use instances or use occurrences as the preferred mode.

Use instances	It is best to use instances if you are in an FPGA, PSpice, or digital simulation project, or if your design does not have occurrence properties.
Use occurrences	It is best to use occurrences if your design has at least one schematic used multiple times or a schematic from an external library. Using occurrences is also the preferred mode if the design already has some occurrence properties.

How Capture uses instance and occurrence properties

The type of property you update or use in Capture depends on the type of project in which you are working. If you are working with an FPGA project or a PSpice project, Capture allows you a choice, but defaults to update instances when you use the Annotate, Update Properties or Export Properties commands. It is best that you use instances to create Cross Reference and Bill of Materials reports, as well.

When you work with a PCB or schematic project, it is best to update occurrences when you use the Annotate, Update Properties, and Export Property commands. In these projects, Capture also uses occurrences to create reports with Cross Reference and Bill of Materials.

Note: While modifying occurrence properties, open only one occurrence at a time.

The EDIF 2 0 0, VHDL, and Verilog netlist formats generate true hierarchical netlists. Capture uses the instance property values on nets and parts when it generates a netlist for a design with one of these formats. All other netlist formats in Capture produce flat netlists and use occurrence property values.

Flat vs. hierarchical designs

This section covers:

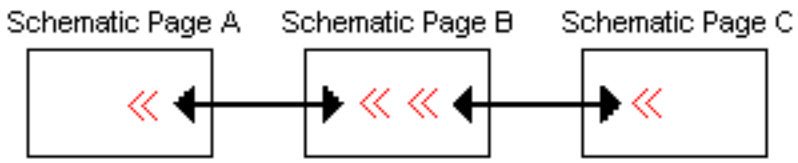
“Flat designs” on page 46

“Hierarchical designs” on page 47

Designs in Capture (even HDL- or EDIF-only designs) generally conform to one of three design structures: flat, simple hierarchy, or complex hierarchy.

Flat designs

For schematic designs, flat designs are structures in which the output signals of one schematic page connect directly to the input signals of another schematic page in the same schematic folder though off-page connectors.



A flat design has no hierarchy (no hierarchical blocks, hierarchical ports, hierarchical pins, or parts with attached schematic folders). All schematic pages in a flat design are contained within a single schematic folder. Regardless of the number of schematic pages in a flat design, all parts appear at the same level of hierarchy in the Hierarchy tab.

Since you must manage all of the interconnections between the pages of a flat design using the names assigned to the off-page connectors, it is best to keep a flat design relatively small.

For VHDL models, flat designs are implemented in a single entity/architecture pair. The entire functionality of the design unit is described within the VHDL architecture. For example:

```
architecture behavior of Dtype is
begin
  process (ck)
  begin
  if (ck = '1') and ck'event then
  q <= d;
  end if;
  end process;
end behavior;
```

Hierarchical designs

This gives you an overview of hierarchical designs, then discusses:

“Simple hierarchies” on page 47

“Complex hierarchies” on page 48

You can manage both schematic and VHDL design resources in a hierarchical manner. That is, you can create schematic pages containing hierarchical blocks or parts with schematic or VHDL implementations. The hierarchical block symbol (or part with an attached schematic page or model) in the schematic page editor is the primary mechanism you use to extend the scope of the design. Use hierarchical blocks to partition the major functional regions of your design using a block diagram.

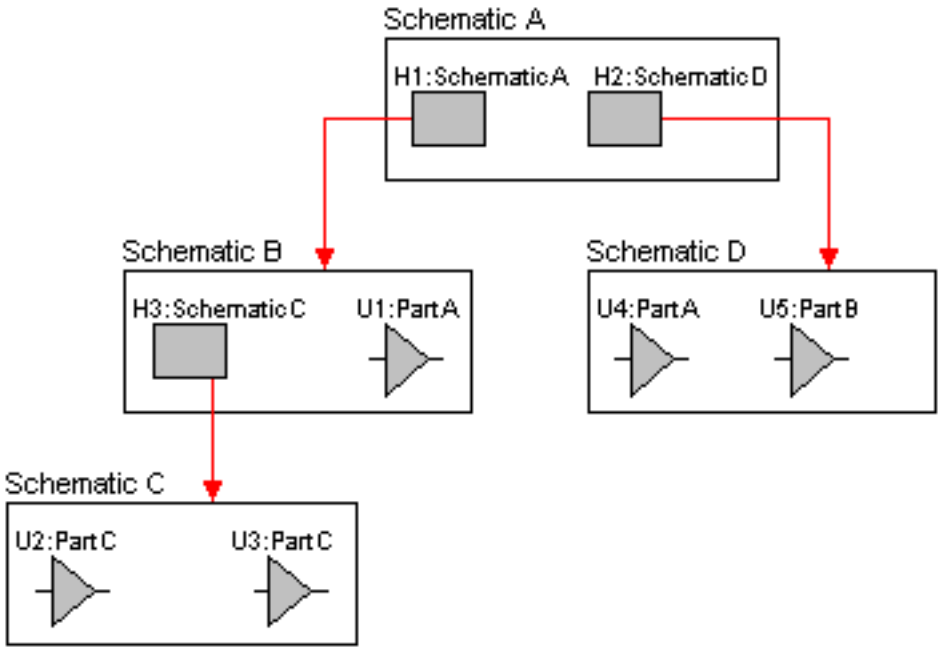
Any schematic page can contain combinations of hierarchical blocks or parts that refer to other schematics or VHDL source files. This nesting structure can be many levels deep. VHDL source files may only instantiate VHDL models; you cannot refer to a schematic folder from within a VHDL source file.

The schematic folder or VHDL entity at the top of a hierarchy, which directly or indirectly refers to all other modules in the design, is called the root module. In the project manager's file tab, the root module has a backslash on its folder icon. The root module folder, as well as any other module folder, can contain as many schematic pages or VHDL models as you require. Capture also supports a combination of flat and hierarchical structures such that a schematic folder containing multiple schematic pages may be associated with a hierarchical block or part.

Simple hierarchies

A one-to-one correspondence between hierarchical blocks or parts and the schematic, EDIF or VHDL implementations they reference is

called a simple hierarchy. The picture below is an example of a simple hierarchy typical of most PCB designs in Capture.

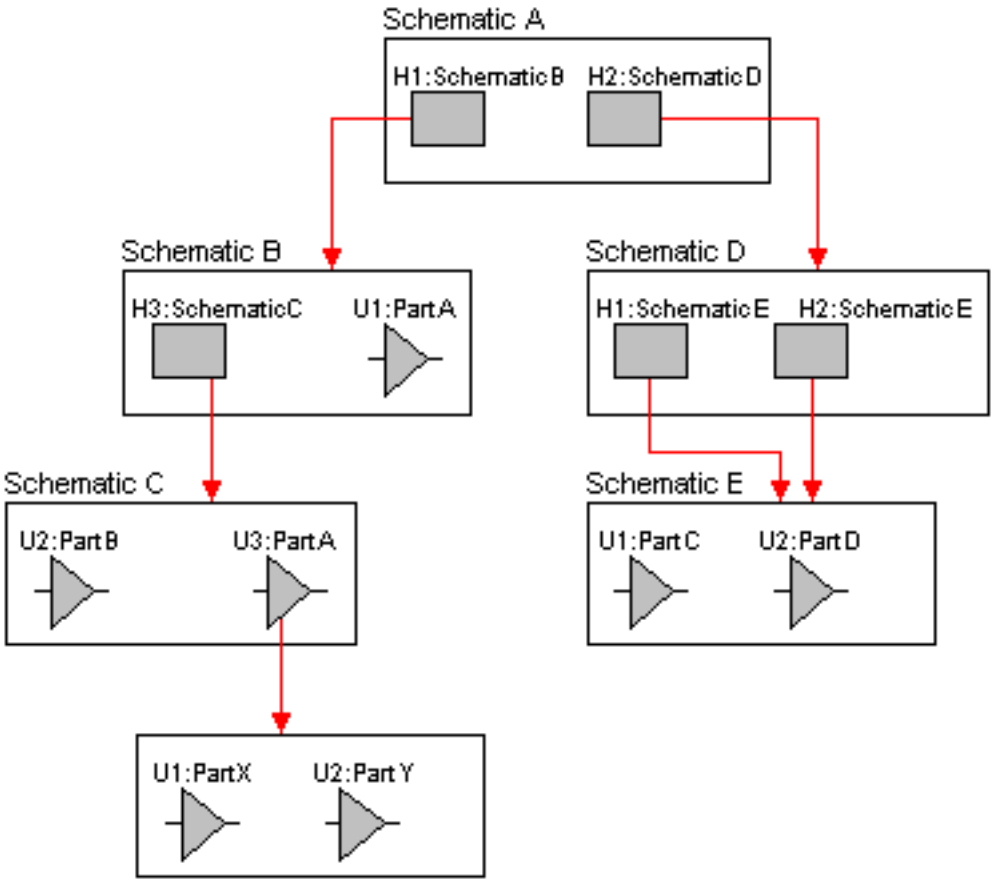


In a simple hierarchy, each hierarchical block or part with an attached schematic folder or VHDL model represents a unique design module. The project manager's hierarchy tab displays a simple hierarchical design as a tree of schematic pages.

Complex hierarchies

A complex hierarchy is one that includes a many-to-one correspondence between the hierarchical blocks or parts and their implementations (schematic, EDIF, or VHDL). The picture at right is an example of a complex hierarchy typical of most programmable logic designs in Capture. As shown in the picture, two hierarchical

blocks (H1 and H2 on schematic D) reference the same schematic (schematic E).



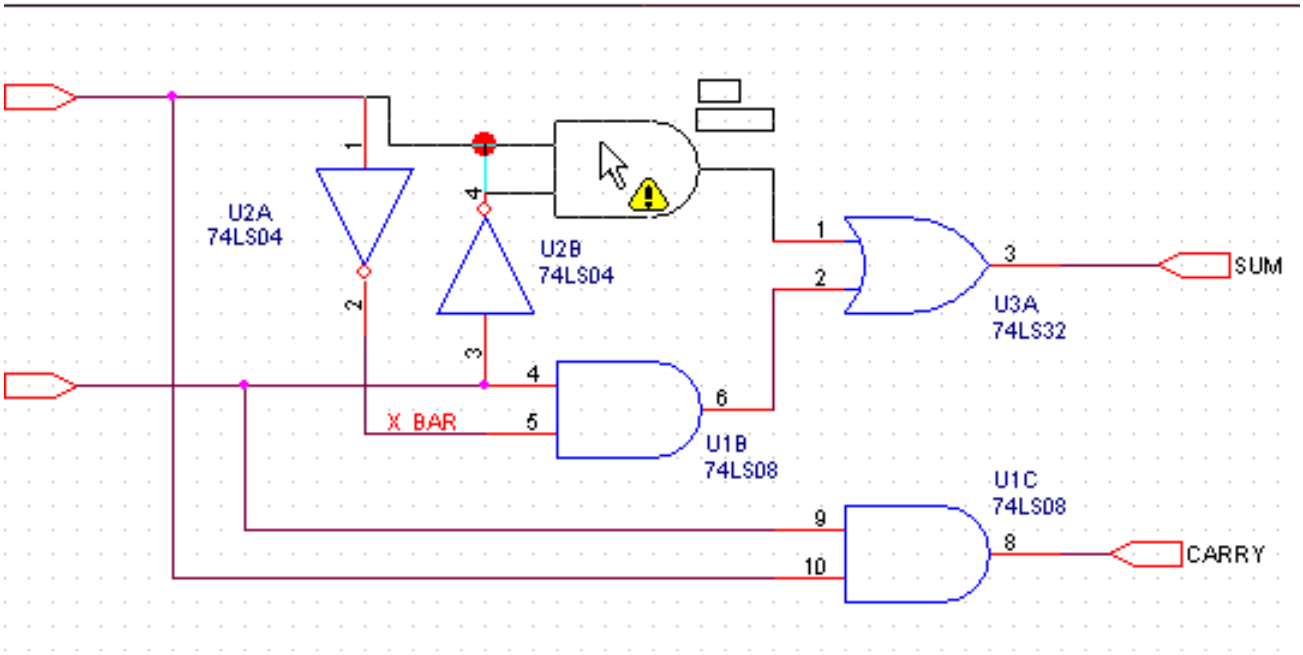
Using orthogonal drag

Connectivity and orthogonal drag

Connectivity, of course, is of vital importance to an electronic design. Therefore, it is important to understand how connectivity is maintained when you move objects on a schematic page.

Capture draws wires that maintain connectivity with a moved object in a stair step (orthogonal) fashion. When you reposition an object, connectivity may be affected.

Capture warns you of connectivity changes as you drag the object by placing markers at the connectivity change points visible on the page. At the same time, the cursor changes to an exclamation point as shown in the following schematic, and the status line warns of net connectivity changes.



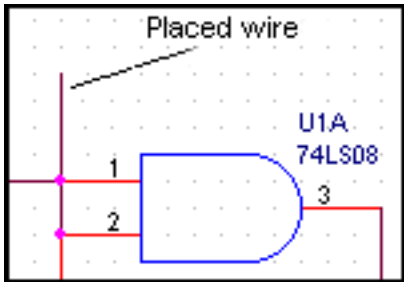
Because some connectivity changes may not be visible on screen, most connectivity changes for which you see an alert are documented in the session log.

Capture automatically places junctions to create electrical connections at "T" intersections where wires abut and do not cross. Also, Capture places a junction for you where a wire crosses a pin.

Note: Before you edit a design created in an earlier version of Capture in Capture Release 9.1, you should run a Design Rules Check to show where Capture will place junctions in your design. If you do not want electrical connections at "T" intersections and on pins where wires cross, you can adjust the design as necessary using an earlier version of Capture before you edit in Capture Release 9.1.

In Capture Release 9 and earlier, you could place wires in the following manner and Capture would not automatically place junctions for you at "T" intersections or pins.

In Capture Release 9 and earlier, you could place wires in the following manner and Capture would not automatically place junctions for you at "T" intersections or pins.



If you complete the operation, connectivity change warnings will appear in the session log as shown below.

```
----------------------------------------------------
The following 2 points have been identified as net
connectivity change
points from the last operation
----------------------------------------------------
(2.60, 1.80)
(2.60, 2.00)
```

The orthogonal drag feature eliminates most unintentional disconnects. As such, Capture will no longer warn you of some connectivity changes caused by dragging objects. If you drag the end of a wire or wire segments that are connected to pins or net symbols, they will disconnect. If you drag wire-to-pin or wire-to-net symbol disconnects back into place, you will see connectivity change indicators. Wire-to-wire connections stretch to maintain connectivity, and junctions maintain connections when you drag wire segments, objects, or entire nets.

The following table shows when Capture provides a connectivity change alert:

Object Type	Drag	Place	Pasting	Resizing
Part	Yes	Yes	Yes	N/A
Hierarchical Block	Yes	No	Yes	N/A
Wire	Yes	Yes	Yes	Yes

Bus	Yes	Yes	Yes	Yes
Net Symbol	Yes	Yes	Yes	N/A
Bus Entry	Yes	No	Yes	N/A

Non-Linear Editor (Fisheye)

The Fisheye feature in Capture allows you work on a schematic in a non-linear mode. The two basic features include the Fisheye focus and the Dynamic Fisheye View mode.

Fisheye focus

Fisheye focus allows you to set focus to specific objects on your schematic. Setting the Fisheye focus to one or more objects on the schematic ensures that these objects display in a magnified view. As this happens, the other visible objects are not moved off the page but demagnified. This ensures that you still have a view of the page, but with selected focus.

Dynamic Fisheye view

In the Dynamic Fisheye view, as the mouse hovers over an object it is immediately magnified. This functions the same as the Fisheye focus mode but in a completely dynamic manner. Also, you can work in both modes simultaneously. Setting focus to one or more objects and then switching on the dynamic mode to pan across the rest of the page.

Miscellaneous

The Fisheye mode is page specific and not design specific. Also, moving in and out of the Fisheye mode will retain the state of the previous mode. You can use all the zoom operations in addition to the focus feature of the Fisheye. All Capture features are available while in this mode.

The Capture find functionality can be used in conjunction with the Fisheye feature. Finding an object on the page will set the focus to

the object. If you press Shift + F11 (shortcut) will immediately set the Fisheye focus for the selected object.

Eye Magnification (Fisheye Zoom)

In the Fisheye mode, you can set a Fisheye (non-linear) zoom (that is independent of the standard linear zoom). This feature is used in conjunction with the Set Fisheye focus and the Dynamic Fisheye View modes to further zoom into or zoom out of the schematic in a non-linear manner.

PCB Editor 3D Footprint Viewer

The PCB Editor 3D Footprint viewer provides a three dimensional view of the footprint symbol of a selected part on the schematic or the part editor. Along with the footprint symbol, the viewer also displays pin numbers and pin names.

Footprint Viewer

When you select to view the footprint of a part, the footprint viewer displays the three dimensional view of PCB associated footprint. In the footprint viewer, selecting the footprint or a pin on the footprint queries for and displays the part or pint information at the top of the viewer.

If you select a pin on the schematic or part editor, the corresponding pin in the viewer is selected. Also, the pin details are displayed in the viewer.

Note: The viewer is available from within the schematic, the part editor or CIS Explorer.

Note: To view the 3D footprint in the CIS Explorer window, you need to first enable the Footprint Viewer toolbar by choosing View - Toolbar - Footprint Viewer from the menu. Then choose the Show footprint viewer button to display the 3D Footprint Viewer.

Footprint Views

The PCB footprint in the viewer can be viewed from different perspectives. The Footprint Viewer toolbar provides shortcuts to the following standard views:

- Top
- Bottom
- Front
- Back
- Left
- Right
- Isometric (the angles between the projection of the x, y, and z axes are all the same, or 120°)

Besides the standard views, the footprint viewer provides a completely dynamic viewing capability. If you hold down and drag the left mouse button on the viewer, you can change the footprint to any conceivable angle or view.

Measure Tool

This tool allows you to measure distances across the footprint canvas. Since the viewer is a three dimensional viewer, so the measure tool allows you to measure within the same axis plane on the view or across axes.

Axis View

The axis view displays the x, y and z axis in the bottom left corner of the viewer. As you change the perspective of the footprint the perspective of the axis changes. This is enables you to identify the current propitiate of the footprint. The axis view especially useful when you use the mouse to change the view out of the standard views.

Footprint Selection Order

When viewing a footprint of a part, the footprint viewer selects the footprint to be displayed in the following order of preference:

- PCB Footprint property defined on the part instance
- PCB Footprint defined in the CIS table, if the part is a linked database part.
- PCB Footprint property defined in the package properties of the part.

If none of the above properties/values is found, the viewer displays a blank canvas with an error in the session log.

Footprints not displaying in the 3D viewer

If you are not able to view footprints in the 3D viewer, you can verify the following settings on your Capture installation.

PCB Footprint property

For the footprint to display in the viewer, you need to ensure that a valid PCB Footprint property is defined for the part.

Capture.ini

Allegro Footprints section in the Capture.ini.

The variables in this section define the directory locations for the psm and pad files. The psm file is used by the PCB Editor 3D Footprint Viewer to display the 3D footprint. Also, the pad file is used by the Viewer to display the pin information in the viewer. For details on creating and editing the variables (including the Allegro Footprint variables) in the Capture.ini see the OrCAD Capture Quick Reference.

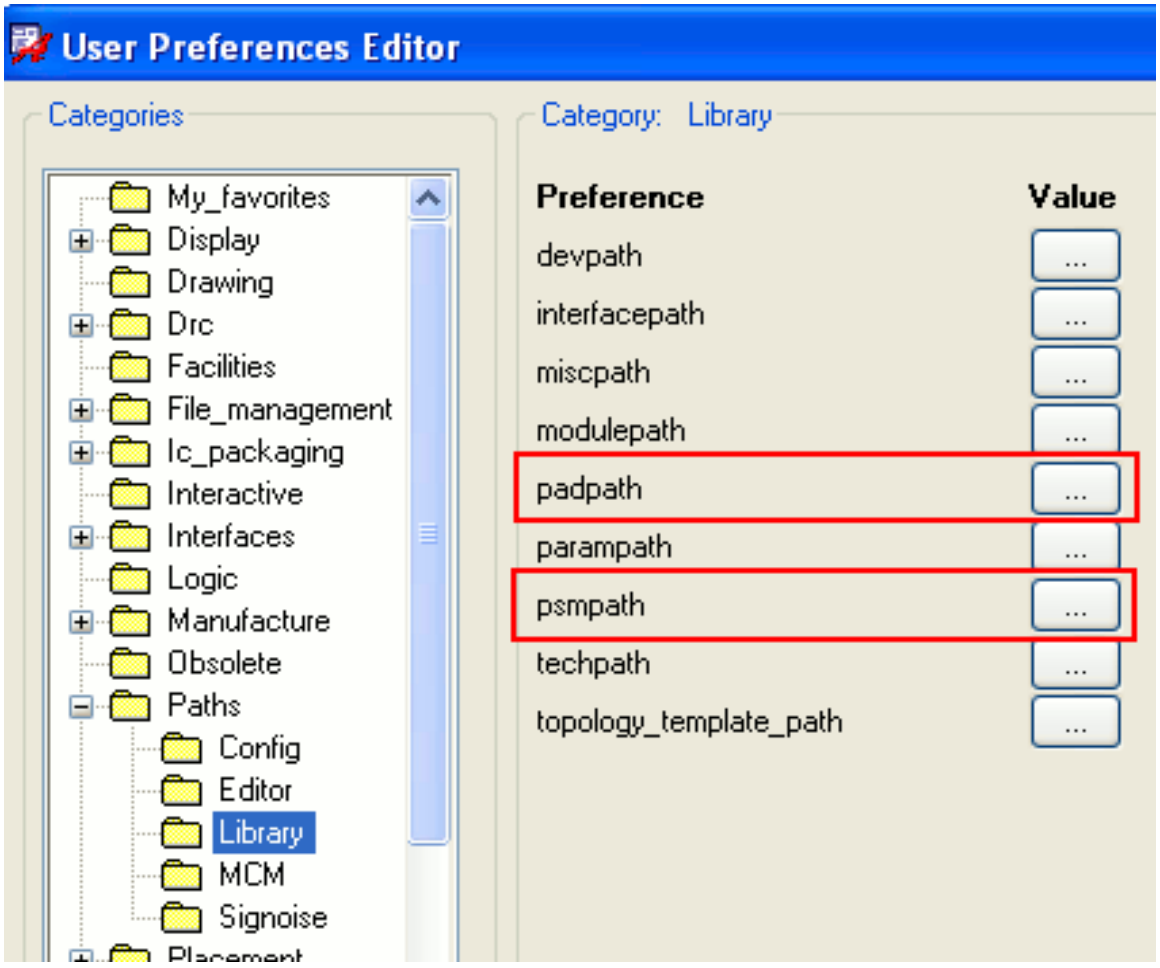
PCB env file variables

The PCB env file contains two variables psmpath and padpath. These variables define the psm and pad file paths on your Capture

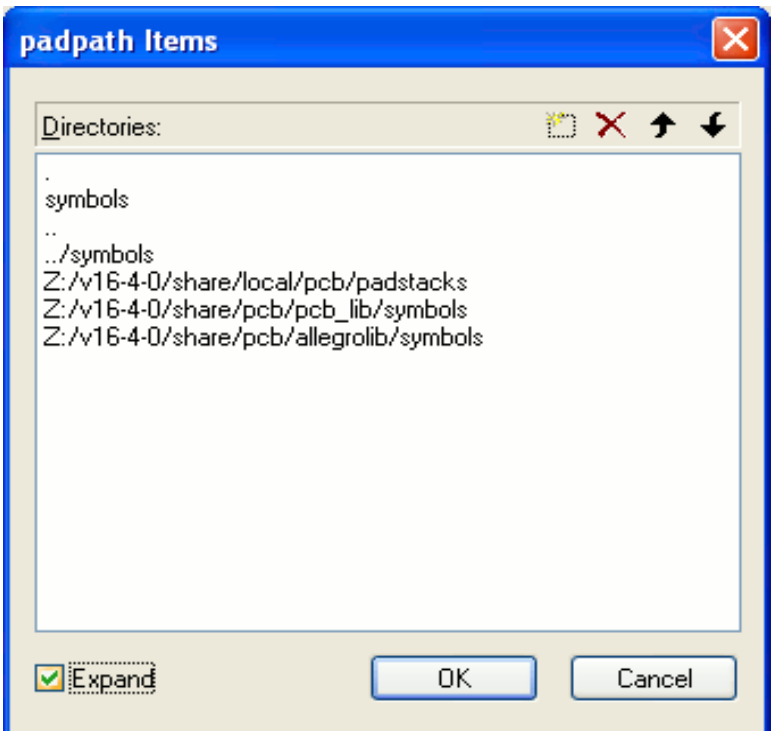
installation. To view footprints in the 3D view, you need to ensure that these variables point to valid psm and pad file paths.

To set / update the psmpath and padpath in the PCB env

1. Click Start - Run to open the Windows Run dialog box.
2. Type enved and press Enter.
3. The User Preference Editor displays.
4. In the Categories tree, go to Paths - Library.



5. To specifiy the path (or paths) for the pad file, click the Value button to the right of padpath.



6. You may need to click the Expand checkbox, in the padpath Items dialog box, to view the pad paths currently defined.
7. To specify a new path, click the New (Insert) button.

Similarly, use the psmpath Items dialog box to add / update the path to the psm files.

Part packaging

About part packaging

Parts are the basic building blocks of a design. For PCB designs, part may represent one or more physical components; or it may represent a function, a simulation model, or a text description for use by an external application. The part's behavior is described somehow, whether by a SPICE model, an attached schematic folder, HDL statements, or other means.

Parts in PCB designs usually correspond to physical objects—gates, chips, connectors, and so on—that come in packages of one or more parts. "Multiple-part packages" are physical objects that comprise more than one part.

Each logical part has graphics, pins, and properties that describe it. As you place the parts in a package to suit your design requirements, Capture maintains the identity of the part package for back annotation, netlisting, bills of materials, and processes that require it. Parts inherit this information from the package.

You specify packaging information when you create a part. You can also change it in the part editor (from the View menu, choose package; then, from the Options menu, choose the Package Properties command.

The parts in a package may have different pin assignments, graphics, and user properties. If all the parts in a package are identical except for the pin names and numbers, the package is homogeneous. If the parts in a package have different graphics, numbers of pins, or properties, the package is heterogeneous. For example, a hex inverter is homogeneous: the six inverters are identical, except for their pin numbers. A relay, which has a normally opened switch, a normally closed switch, and a coil, is heterogeneous: the three physical parts differ in graphics, number of pins, and properties.

When you place a part on a schematic page, you actually create an instance of the part. A part instance is like a "snapshot" of the part in the library; that is, it inherits all the properties of the library part. Once a part instance is on the schematic page, you can edit the properties of that instance without changing the properties of any other instance. The instance values of those properties supersede the values of any identical properties that exist on the library part. For more information, see Instances and occurrences.

When using multiple-part packages in your design, you must either make all shared pins visible and connect them to power and/or ground nets, or you must make them all invisible, in which case they are connected according to their pin names. See Making power pins visible for more information.

Related topics

For information about...	Click this topic...
The hierarchical structure of designs.	Flat vs. hierarchical designs
The distinction between part instances and part occurrences.	Instances and occurrences
Part connectivity on a schematic.	Using orthogonal drag
Designing a CPLD or an FPGA with Capture.	Programmable logic projects
Using Capture's "window" environment effectively.	Working with multiple windows
Retrieving lost information after a system crash or power outage.	Auto recovery
Becoming effective in using the various editor windows available in Capture.	Moving around in the editors
Establishing connectivity for power and ground pins in a part package.	Making power pins visible
The default directory structure for Capture.	Capture directory map
Communication between Capture and other EDA tools.	Intertool communication
Setting up your Capture work environment.	Capture configuration

Programmable logic projects

Capture also provides a method for developing FPGA/CPLD devices. A schematic folder can represent the internal logic of a programmable device such as an FPGA or CPLD. The schematic folder can contain silicon-vendor provided primitive and macrofunction symbols, as well as user-created macrofunction symbols.

FPGA and CPLD vendors (Actel, Lattice, Xilinx, and so forth) provide a CAE Interface Package containing symbols that provide you with the building blocks to create a structural design description of an FPGA or CPLD, and simulation models so a functional and timing-based simulation can be performed on the design.

You can merge design modules created in a hardware description language like VHDL or OHDL with the design description with some vendors. External View or Properties can record the file name of the module.

Capture's netlist tool creates reports of the project and any HDL modules in a standard format such as EDIF or OrCAD INF. FPGA place-and-route tools or CPLD device-fitters read the design netlist and implement the logic into the physical constraints of the device.

You can also use the FPGA Export Dialog Box to specify settings for FPGA parts that you want to generate. You can then export a FPGA part using the FPGA Export Dialog Box. FPGA flow is supported in the PCB Editor flow from Capture. When you swap pins in PCB Editor for a FPGA component, the swapped pins can be backannotated to the Capture design. You can then export the design with the swapped pins. You can also specify reserved pins (Input, Bidirectional and Output) in the FPGA component using the FPGA Export Dialog Box. This dialog box is invoked from the FPGA Export dialog box.

When you select Output Reserve Pins, the reserve pin assignment made in the Reserve Pin dialog will appear in the output tcl file. Not selecting this option does not remove the assignments, they do not appear in the tcl file.

Tip

When you choose *Place – Swap – Pins* in PCB Editor and click on a pin of a FPGA component, all the swappable pins are highlighted.

Note: Making reserve pin assignments is currently supported for Altera devices.

Working with multiple windows

This section gives you an overview of working with multiple windows, then tells you how:

- "To open a window on the active document" on page 62
- "To open a window on another document" on page 62
- "To switch to a different open window" on page 62
- "To switch to the project manager for the active document" on page 62
- "To save all open windows" on page 63
- To specify Session Log and Project Manager as Docked, Floating, or MDI Child on page 63
- To close all open windows on page 64

In Capture, each document that you open is in a separate window. You may open as many windows as your computer's resources allow. For example, if you wish to work with three schematic pages or three parts, each opens in its own window. If you are working simultaneously with several projects, each opens in its own project manager window.

Note: All the open documents are tabbed windows. You can right-click the tabs to restore, minimize, maximize, save or close the windows. You can also right-click on the title bar of the Session Log and Project Manager to set them as docked, floating or MDI child windows.

Sometimes it is useful to have more than one view of a document. You might display different areas of the document at different zoom scales, or copy items from one location to another. Capture maintains and displays the selection set across all views of a part or schematic page.

For example, you might open a schematic page and use the New Window command to open the schematic page in a second window. You could then shrink the second window and use the Zoom, then the All commands, to create a bird's eye view of the schematic page. Anything you select in the bird's eye view window is also selected in

the original window. In the original window, you use the Zoom, then the Selection commands to zoom in on selected objects.

Another way to get a different view of your document is to use the window's splitter bars to split your view, then move objects across the splitter bar and place wires, buses, arcs, and polylines that span the splitter bar. This is very useful for working on large schematic pages.

The Capture work environment is windows based. That is, all documents or schematics appear in their own windows when open for editing.

To open a window on the active document

➤ Choose *Window – New Window*.

To open a window on another document

➤ Choose *File – New*.

or

➤ From the File menu, choose the name of a recently used file.

In Capture, the windows in which you work have headings based upon the name of the open document.

To switch to a different open window

➤ Click the tab for the window. Alternatively, press `CTRL+TAB`

or

➤ From the Window menu, choose the window that you wish to make active.

Tip

Mouse-over a tab to see the name of the window as tool tip.

To switch to the project manager for the active document

➤ Click the Project Manager button on the toolbar.

Note: Click the tab for the project manager if the window is open. Mouse-over the tabs to identify the Project Manager window.

You can right-click the Project Manager title bar to specify the Project Manager to be docked to the main window.

To save all open windows

➤ From the project manager, choose *File – Save All*. All designs or libraries that have been modified are saved.

Note: When you save a project, Capture automatically creates a backup with a .DBK file extension. When you save a library, Capture automatically creates a backup with a .OBK file extension. If you save only a schematic page or a part, no backup is generated.

To specify Session Log and Project Manager as Docked, Floating, or MDI Child

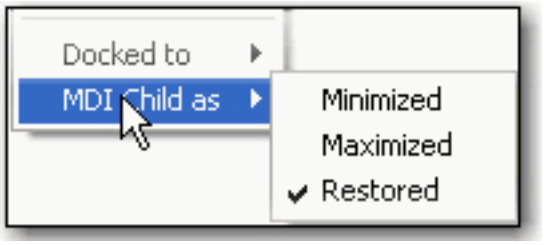
Right- click the title bar of the Session Log or Project Manager windows to specify them as *Docked*, *Floating*, or *MDI Child* window.

You can right-click the title bar and select *Docked to*, which gives the following options to dock your window:

- *Top*
- *Left*
- *Bottom*
- *Right*

Similarly, you can right-click the title bar and select *MDI child*, which gives the following options to specify the size of the window:

- *Minimized*
- *Maximized*
- *Restore*



To close all open windows

Choose *Windows - Close All Windows* to close all open windows.

Auto recovery

This section gives you an overview of auto recovery, then discusses:

"Auto recovering files" on page 65

"Restoring auto recovered files" on page 65

Capture's auto recovery feature was designed to protect you from losing work as a result of a system crash or power outage. Capture automatically saves the state of the open design and library files at the end of each interval set in the Miscellaneous tab of the Preferences dialog box. Capture removes autosaved files from your system when a project is closed and when you exit Capture normally. The Preferences dialog box appears when you choose *Tools – Preferences*.

Auto recovery is not an automatic saving feature intended to replace the Save commands. If you intentionally exit Capture without first saving your changes, they will be lost. Auto recovered files are automatically deleted when you exit Capture normally.

Auto recovering files

Capture maintains a file called FILES.ASL in the \WINDOWS\TEMP directory that has a list of all design and library files that have been opened. Capture updates FILES.ASL when a project is opened or closed. If your system goes down without exiting Capture, FILES.ASL has a list of design and library files that were open for editing when the system failure occurred.

Auto recovery works on a timer that you can set to specify how often (if at all) you want Capture to auto recover the currently open and modified design and library files. The frequency can be from five minutes to every 120 minutes (2 hours). When the interval is reached, Capture examines all open design and library files. If a file that is part of the project is open for editing, Capture examines it to see if it has been modified since the last auto recovery. If it has, it is saved to the \WINDOWS\TEMP directory.

If the project itself has been modified, or one of its files was auto recovered, the project itself is saved to the \WINDOWS\TEMP directory. When this happens, the auto recovered version of the project file is updated such that the path of any auto recovered designs or libraries change to point to the \WINDOWS\TEMP directory. Any paths of ".\" are changed to point to the directory the project was loaded from. You can then open the project from the \WINDOWS\TEMP directory with all paths pointing to the correct place: the \WINDOWS\TEMP directory for those files that were auto recovered, and the original location for those files that were not modified and therefore not auto recovered.

When a project is closed, all auto recovered files in the \WINDOWS\TEMP directory for that project are deleted.

Restoring auto recovered files

When you start Capture, it checks for the FILES.ASL file. If Capture finds the file, it reads it. If Capture exited abnormally the last time it was used, and there are design and library files listed in FILES.ASL, Capture opens the design and library files from their original locations. Capture then appends "(Restored)" to the project manager's title to indicate that the project was loaded as a result of a previous system failure.

Capture also looks for design and library files that were auto recovered to the \WINDOWS\TEMP directory. If any are present, Capture opens them, changes their name to a default name (like PROJECT1), adds "(Restored)" to their project manager's titles, removes the filename and directory from the project manager window, and marks the project as modified.

Capture then looks in the project for any files that reference the \WINDOWS\TEMP directory. Any files that do are auto recovered to the Windows temporary directory, are opened, their filenames and directories are removed from their project manager windows, and they are marked as modified.

Moving around in the editors

This section covers:

- "Scrolling" on page 67
- "Panning" on page 68
- "Moving to a location, reference, or bookmark" on page 69
- "Zooming in" on page 70
- "Zooming out" on page 71
- "Zooming to a specific scale" on page 72
- "Changing the zoom factor" on page 72
- "Viewing the entire schematic page or part" on page 72
- "Viewing a specific area" on page 73
- "Centering the view" on page 74
- "Refreshing the display" on page 75
- "Setting a bookmark" on page 75
- "Using Fisheye" on page 76
- "Using the PCB Editor 3D Footprint Viewer" on page 78
- Customizing toolbars on page 82
- Customizing Commands on page 84

- Docking Toolbars on page 85

Capture comes complete with a number of editors, including a text editor with certain features for creating VHDL models, a schematic editor, and a part editor. These editors mostly function in accordance with the general standards that one might expect in a Windows-based tool. However, there are certain unique traits (particularly with regard to zooming and scrolling) that distinguish the Capture editors from other Windows editors.

In order to understand how each feature of the various editors works in Capture, refer to the various topics mentioned in this workflow.

Scrolling

In Capture, you can scroll up or down, or to the left or the right, to focus on a different portion of the active window. Even though some objects on the Place menu are attached to your pointer while you're placing them, you can still scroll.

- Click on either side of the scroll button to scroll the panning distance in the corresponding direction—up or down using the vertical scroll bar, right or left using the horizontal scroll bar.
- Click on the up, down, right, or left arrow to scroll one grid unit in the corresponding direction.
- Drag the horizontal or vertical scroll button to scroll the window dynamically.
- Press PAGE UP to scroll the panning distance up.
- Press PAGE DOWN to scroll the panning distance down.
- Press CTRL+PAGE UP to scroll the panning distance to the left
- Press CTRL+PAGE DOWN to scroll the panning distance to the right.
- Roll the mouse wheel up and down to scroll through vertically in the schematic page editor and property editor.
- Hold down the SHIFT key and roll the mouse wheel up and down to scroll through horizontally in the schematic page editor and property editor.

- Click the mouse wheel button and drag the mouse wheel:
  - To the right or left in the property editor and schematic page editor to scroll horizontally.
  - Up or down in the property editor and schematic page editor to scroll vertically.

Panning

When performing an action while the left mouse button is depressed (moving an object, drawing a selection area, and so forth) you can pan the display region by moving the cursor to the border of the active window. You can configure the distance by which the display changes (the panning distance) during a pan.

If you want to pan the display region while not performing any action (only for viewing), you can use the Scroll mouse button. Click on the scroll button and a Pan cursor appears. Now move the mouse anywhere across the page to pan the display area. As you move close to the edge of the display area, the area out of display will move into display.

To change the display region

1. While drawing, placing, or moving objects, or while drawing a selection area, move the pointer to the edge of the window. If there is more of the schematic page or part to display, the window scrolls in the corresponding direction.

To configure panning distance

1. Choose *Options – Preferences*, then choose the Pan and Zoom tab.
2. In the Scroll Percent text box, enter the percent of the window's horizontal or vertical dimension by which the display will scroll. Note that you can specify separate values for the schematic page editor and the part editor.
3. Click OK.

Moving to a location, reference, or bookmark

You can use the Go To command to move to specific locations (either grid coordinates, references or bookmarks) in a particular editor. The X and Y coordinates of your pointer's current location appear on the right-hand side of the status bar. Grid references appear on the left and upper edges of the schematic page in the schematic page editor.

To move to a specific location

1. Choose *View – Go To*.
2. Select the Location tab.
3. Enter the X and Y values, select the Absolute option, then click OK. The coordinates are measured in inches or metric units, depending on what you specified in the Page Size tab of the Design Template / Design Properties dialog box. Your pointer moves to the new coordinates.

To move a specific distance

1. Choose *View – Go To*.
2. Select the Location tab.
3. Enter the X and Y values that you want the pointer to move, select the Relative option, then click OK. The jump distance is measured in inches or metric units, depending on what you specified in the Page Size tab of the Design Template / Design Properties dialog box. Your pointer moves the specified distance.

To move to a specific grid reference

1. Choose *View – Go To*.
2. Choose the Grid Reference tab.
3. Enter the horizontal and vertical information corresponding to the grid reference, then click OK.

To move to a specific bookmark

1. Choose *View – Go To*.

2. Choose the Bookmark tab.
3. Enter the name of the bookmark, then click OK.

Zooming in

In the schematic page editor and the part editor, you can zoom in to look closely at a particular area. When you press I to zoom in, Capture centers your view on the current pointer position, if possible. If the pointer is outside the window, or if you choose the Zoom In command or toolbar button, Capture centers your view on any selected objects. Otherwise, Capture zooms in on the center of the active window.

You can also zoom into a specific object on the page by using the right mouse button. Click on a blank area close to the object and keeping the mouse button pressed drag the area over the part you want to zoom into. The area is zoomed into as soon as you release the mouse button. The zoom factor is 3.

To zoom in

1. Choose *View – Zoom*, then choose the Zoom In command. The current zoom scale is multiplied by the zoom factor. So, for example, a zoom factor of 2 causes the image to appear twice as large and displays half the area of the previous view.

Note: In the property editor and schematic page editor, hold down the CTRL key and roll up the mouse wheel to zoom in.

To change the zoom factor

1. Choose *Options – Preferences*, then choose the Pan and Zoom tab.
2. In the Zoom Factor text box, enter the new zoom factor. Note that you can specify separate values for the schematic page editor and the part editor.
3. Click OK.

Shortcut

Toolbar:

Keyboard: I

Zooming out

In the schematic page editor and the part editor, you can change your viewing perspective to increase the portion of the schematic page or part that is visible.

To zoom out

1. Choose *View – Zoom*, then choose the Zoom Out command. The current zoom scale is divided by the zoom factor. So, for example, a zoom factor of 2 causes Capture to halve the image size and show twice the area of the previous view.

Note: In the property editor and schematic page editor, hold down the CTRL key and roll down the mouse wheel to zoom out.

To change the zoom factor

Note: At certain zoom scales, Capture substitutes filled rectangles for text that is too small to appear. These placeholders are for display only—the text prints correctly.

1. Choose *Options – Preferences*, then choose the Pan and Zoom tab.
2. In the Zoom Factor text box, enter the new zoom factor. Note that you can specify separate values for the schematic page editor and the part editor.
3. Click OK.

Shortcut

Toolbar:

Keyboard: O

Zooming to a specific scale

To view a part or schematic page at a specific scale

1. Choose *View – Zoom*, then choose the Scale command.
2. Select a preset scale or enter a custom scale, then click OK.

Changing the zoom factor

When you zoom in or out, the zoom scale is multiplied or divided by a zoom factor that you can set to suit your needs. Furthermore, you can set one zoom factor for the schematic page editor and another for the part editor.

To change the zoom factor

1. Choose *Options – Preferences*, then choose the Pan and Zoom tab.
2. Enter the new zoom factor, then click OK.

Viewing the entire schematic page or part

You can view the entire part or schematic page at once. For a schematic page, Capture uses the dimensions set in the Page Size tab in the Schematic Page Properties dialog box.

1. Choose *View – Zoom – All*. The entire schematic page or part is reduced to fit the window.

Shortcut

Toolbar:

Related topics

For information about...	Click this topic...

Scrolling around the schematic with the scroll bars.	Scrolling
Panning around the viewable area while performing a task.	Panning
Moving to a location, reference, or bookmark.	Moving to a location, reference, or bookmark
Zooming in.	Zooming in
Zooming out.	Zooming out
Zooming to a specific scale.	Zooming to a specific scale
Viewing a specific area.	Viewing a specific area
Centering the view.	Centering the view
Refreshing the display.	Refreshing the display
Changing the zoom factor.	Changing the zoom factor
Setting a bookmark.	Setting a bookmark

Viewing a specific area

To view an area of the part or schematic page

1. Choose *View – Zoom – Area*. The pointer appears as a magnifying glass.
2. Move the pointer to one corner of the rectangular area to enlarge.
3. Press and hold the left mouse button as you move the pointer to the opposite corner of the rectangular area.
4. Release the mouse button. The selected area fills the window.

Shortcut

Toolbar:

Related topics

For information about...	Click this topic...
Scrolling around the schematic with the scroll bars.	Scrolling
Panning around the viewable area while performing a task.	Panning
Moving to a location, reference, or bookmark.	Moving to a location, reference, or bookmark
Zooming in.	Zooming in
Zooming out.	Zooming out
Zooming to a specific scale.	Zooming to a specific scale
Viewing the entire schematic page or part	Viewing the entire schematic page or part
Centering the view.	Centering the view
Refreshing the display.	Refreshing the display
Changing the zoom factor.	Changing the zoom factor
Setting a bookmark.	Setting a bookmark

Centering the view

In Capture, you can center the view on your pointer or you can focus the view on a specific object.

To center the view on a specific object

1. Select objects or an area.
2. Choose *View – Zoom – Selection*. The display scrolls so that the selected objects or selected area is in the center of the window. The zoom factor does not change.

To center the view on your pointer

1. Move the pointer over the area you want to be centered, then press SHIFT+C or just C.

Refreshing the display

To refresh the display

1. Choose *View – Zoom*, then choose the Redraw command.

Shortcut

Keyboard: F5

Setting a bookmark

If you find that you need to return repeatedly to a specific area of a schematic page, or if you need to direct attention to a particular location, a bookmark is very convenient. When you set a bookmark, you assign it a name. You can then use the Go To command to return to the location, and you can use the bookmark name to direct another member of your team to the location.

Note: The Go To command is always available on the right mouse button context-sensitive menus in the part editor and schematic page editor. The Go To command, with the Relative option selected, is particularly useful for precise placement and spacing.

To place a bookmark

1. From the Place menu, choose the Bookmark command.
2. Enter the name of the bookmark, then click OK.
3. Position the pointer where you want to place the bookmark and click the left mouse button. The bookmark appears in the selection color.
4. Choose End Mode from the right mouse button pop-up menu.

5. Click an area where there are no parts or objects to deselect the bookmark.

To rename a bookmark

1. Select the bookmark.
2. Choose *Edit – Properties*. The Edit Bookmark dialog box appears.
3. Enter a new name in the text box, then click OK.

Using Fisheye

You can use the Fisheye mode to zoom into only specific objects on your schematic. In the Dynamic Fisheye mode, the schematic will zoom into focus areas as the mouse pointer moves over the page.

Fisheye view

To use the Fisheye features of Capture, you need to switch into the Fisheye mode.

To switch to the Fisheye mode

1. Right-click on the page.
2. Choose the Fisheye view menu item.

Fisheye focus

You can set the Fisheye focus to selected objects on your schematic, causing only these objects to zoom while the rest of the viewable area remain in view but is zoomed out.

To Set the Fisheye focus

1. Select one or more objects on the page. (Use Ctrl + Click to select multiple objects).
2. Right-click on the page.
3. Choose the Set Fisheye Focus menu item.

Shortcut

Keyboard: Shift + F11

To Remove the Fisheye focus

1. Right-click on the page.
2. Choose the RsSet Fisheye Focus menu item.

Shortcut

Keyboard: Ctrl + Shift + F11

Fisheye Dynamic Focus Mode

In the Dynamic Fisheye focus, the focus of the page shifts as you move the mouse pointer across the page. As the mouse pointer hovers over a part of the page, only that part of the page comes into focus. The focus area is magnified while the rest of the viewable area loses relative magnification.

To Set the Fisheye Dynamic focus mode

1. Right-click on the page.
2. Choose the Fisheye Dynamic Focus Mode menu item.

Shortcut

Keyboard: Q

Non-Linear Zoom

While in the Dynamic Fisheye mode, you can further zoom into or zoom out of the view to get higher or lower zoom factor as you pan across the page.

The magnification factor ranges from a minimum of 2 to a maximum of 10.

To zoom in (non-linear)

Press Ctrl + + (Ctrl and plus key combination)

To zoom out (non-linear)

Press Ctrl + - (Ctrl and minus key combination)

Using the PCB Editor 3D Footprint Viewer

You can use the footprint viewer to view from multiple angles a three dimensional view of the associated PCB footprint of a part. You can also query for and view details of the footprint and the pins on the part.

Viewing a PCB Footprint

1. Left-click on the part for which you want to view the PCB footprint.

   You can view the 3D footprint of a part on the schematic editor or the part editor.

   You can also view the 3D footprint for a selected part in Capture CIS Explorer window.

2. Right-click on the part.
3. Choose Show Footprint menu item.

The footrpint viewer opens with the three dimensional view of the part displayed.

Note: If the footprint information for the part is not available, the viewer displays a blank canvas with an error in the session log. See Footprint Selection Order.

Querying for part or pin details

When you view the footrpint of a part in the footrpint viewer, you also have access to the footprint information of the part and the pins on the part.

1. Click the footprint of the part in the viewer.

   The details of the part footrpint are queried and displayed at the top of the viewer.

2. Click a pin on the footprint.

   The details of the pin are queried and displayed at the top of the viewer.

Mapping schematic or part editor pins with footprint

1. View a part footprint in the footprint viewer.
2. Click a pin on the part (in the schematic or part editor).

   The corresponding pin is selected on the footprint in the viewer.

   Also, the pin details are queried and displayed at the top of the viewer.

Toggle Footprint Viewer

You can toggle the footprint viewer between show and hide mode by using the Show footprint viewer button.

Note: This switch only hides the viewer. So the footrpint remains on the canvas in the hide mode.

Shortcut

Toolbar:

Standard Footprint Views

You can view the PCB footprint from a pre-defined set of standard angles using the buttons on the Footprint Viewer toolbar: top, bottom, front, back, left, right and isometric view. Click here to see the Footprint Viewer toolbar description.

Non-Standard Footprint Views

The Footprint Viewer toolbar contains shortcuts that allow you to view the PCB footprint in standard views. However, the footrpint viewer provides the feature of viewing the footprint from any possible angle or view. To view from any non-standard angle you need to use the mouse in the footrpint viewer.

1. Left-click on the footprint viewer and hold the left mouse button down.
2. Move the mouse button within the viewer.

As you move the mouse button, the footprint rotates within the viewer.

Note: From any non-standard view position, you can always use the toolbar view buttons to go back to any standard view.

Moving the footprint

You can move (reposition) the footrpint anywhere within the viewer canvas.

1. Click the footprint on the canvas.
2. Keeping the Shift key pressed, drag the footrpint to any point on the canvas.

View Axis

When you are in a non-standard view position, you may need to identify the actual angle or preoperative of the footprint. This may not always be very easy to identify simply by looking at the view. To easily view the probative of the footprint, switch to the View Axis mode. The x, y and z axes are displayed in the same perspective as the footprint.

Shortcut

Toolbar:

Measure Tool

Use the measure tool to measure any distance on the footprint viewer canvas. An added feature to this tool is that is allows you to measure across different axis. This means that you can rotate the tool to any standard or non-standard view and use this tool to measure distances between any two points.

1. Select the Measure Tool on the Footprint Viewer toolbar.
2. Click the start point of the distance you want to measure.
3. Click the end point.

   The distance (in microns) displays at the top of the viewer. Also, as you move the mouse from the start point to the end point, a ruler displays (and extends with the mouse movement) on the canvas between the start and end points.
4. To reposition either the start or end point of the ruler, click on the point to reposition.

   Notice a wireframe appears at the point you clicked.
5. Click the wireframe and reposition the start or end point of the ruler.

   You can move this point back and forth along the same direction to measure in the line. You can also move the this point in any other direction (on any axis) to measure in other directions or even across axis.
6. Click the other end of the ruler to make this end also movable.

   Now you can reposition either ends of the ruler.

Shortcut

Toolbar:

Note: If you place the ruler on the canvas, the ruler view will change as you change the view of the footprint either using the standard or non-standard viewing.

Footprint Viewer Zoom

Use the zoom buttons on the Footprint Viewer toolbar to zoom the footprint on the canvas.

Zoom In Shortcut

Toolbar:

Zoom Out Shortcut

Toolbar:

Zoom Fit Shortcut

Toolbar:

Note: If you are using a scroll mouse, you can use the scroll wheel to zoom in and out of a footprint on the canvas.

Customizing toolbars

Toolbar settings can be saved in settings schemes.

To change the display of toolbars

To create a new toolbar

To add buttons to toolbars

To remove buttons from toolbars

To reset toolbars to their default settings

To change the display of toolbars

1. From the Tools menu, choose Customize. Alternatively, right-click the menu bar and choose Customize.
2. Click the Toolbars tab.
3. In the Toolbars list, select the toolbars you want to display.

4. Select any of the following options:
   - ❑ Select Show Tooltips to enable Tool Tips.
   - ❑ Select Cool Look to make the toolbar buttons appear flat.
5. Click OK to apply changes and close the dialog box.

OR

1. From the View menu, Choose Toolbar.
2. From the list of toolbars, chose the toolbar to display.

OR

1. Right-click on the menu bar.
2. From the context menu, select the toolbar you want to display.

To create a new toolbar

1. From the Tools menu, choose Customize.
2. Click the Toolbars tab.
3. Click New.
4. In the text box that appears, type a name for the toolbar, then click OK.

   The name of the new toolbar appears in the Toolbars list.
5. Click OK to apply changes and close the dialog box.

Note: The Customize command is also available from the View - Toolbars menu.

Tip

You can also create a new toolbar by dragging a button from the Customize dialog box to any open area on the workspace.

To add buttons to toolbars

1. From the Tools menu, choose Customize.

2. Click the Commands tab.
3. In the Categories list, click a category to display related toolbar buttons in the Buttons frame.
4. Under Buttons, click a button to display a description of its function in the Description frame.
5. To add the selected button to a toolbar, drag it from the Customize dialog box to any toolbar displayed in the program window.
6. Click OK to apply changes and close the dialog box.

To remove buttons from toolbars

1. Drag the button you do not want from the toolbar to the Customize dialog box.

To reset toolbars to their default settings

1. From the Tools menu, choose Customize.
2. Click the Toolbars tab.
3. Click Reset.
4. Click OK to apply changes and close the dialog box.

Note: Changes are applied only to the currently selected toolbar.

Customizing Commands

To customize commands:

1. Choose Tools - Customize. Alternatively, right-click menu bar and choose Customize.
2. Click the Commands tab
3. Select a Menu name from the Categories list

   The buttons for the selected Menu item are displayed in the Buttons box. Select a button to view its description in the Description box.

4. Drag a button and place it in the toolbar

Docking Toolbars

The toolbars in Capture can be docked or made floating. This gives the flexibility of placing the toolbar anywhere on the screen. You can place a floating toolbar even outside the application area.

To make a toolbar floating, double-click on the toolbar area (ensure you do not click on any of the toolbar buttons).

To dock a floating toolbar, double-click on its title bar.

To move a toolbar

To move a floating toolbar, click on the title bar and keeping the left mouse button down, drag the toolbar.

You can also right-click on the title bar and choose the Move option. Now you can use the keyboard arrow keys to move the toolbar.

To hide a toolbar

To hide the toolbar, click on the close (X) button on the right side of the title bar.

You can also hide the toolbar by right-clicking the title bar and choosing the Hide option.

Searching in Capture

The find functionality in Capture is available through the Find toolbar. This contains a text box, the Find button, the Find options pop-up list, the Find next button and the Find previous button.

Find text box

Find button

Find options

Find Next

Find Previous

Find WindowSession Log Search Results

Searching a Design Hierarchy

Find text box

In the Find text box, you enter the text to search. You can use the ? (question mark) wildcard character to denote one wildcard or the * (asterisk) to denote any number of characters.

Find button

Click the Find button to run the search.

Find options

This is a multiple selection pop-up list. It contains the search options that you can set to narrow down or broaden your search. This includes all the searchable object types on your schematic. So if you want to search only for parts, ensure that all the other objects types are unselected. Since it is a multiple select list, you can select multiple object types to search.

Find Next

After the search is complete and if the search returned more than one result, use this button to select the next item in the search list. The next find object will be selected on the open page. Or the page containing the next item is opened with the item selected.

Find Previous

After the search is complete and if the search returned more than one result, use this button to select the previous item in the search list. The previous find object will be selected on the open page. Or the page containing the previous item is opened with the item selected.

Find Window

After the search is complete and if it returned at least one result the result is displayed in the Find window. This is a tabbed dockable window. Each result of the search will display as one line item in the window.

A result line item contains other information besides the search object reference. This includes the page and schematic and properties specific to object types.

If the search returns multiple object types, each type will display in a different tab in the window.

This window can be set as dockable or floating by double-clicking on the title bar. In the docked mode, use the pin icon to alternate the window from pinned to unpinned. In the unpinned state, the Find window remains docked but slides in and out of view as you move the cursor over the window icon.

You can use this list to quickly navigate to an item by double-clicking on the item in the list.

You can also open the Browse Spreadsheet window or save the search results in HTML format.

Browse Spreadsheet window

You can open the Browse Spreadsheet window for a selected part in the Find window.

1. Right-click on a search line item.
2. Choose Edit Properties

   The Browse Spreadsheet window displays the editable part properties.

Save as HTML

You can also save your search results in HTML.

1. Right-click on a search line item.
2. Choose Save as HTML.

A message displays with the location and name of the exported HTML. The location is the directory of the current design.

Session Log Search Results

The session log displays a log of the search results. This log contains the hit count of the object types for each object selected in the Search options pop-up list. It also logs the pages that were searched.

Searching a Design Hierarchy

The find functionality in Capture allows you to search at different levels of the design hierarchy:

- Design Level

  a. In the Project manager, right-click on a design and choose Find.

  b. In the Find text box, type the search string and press Enter.

  The search results displayed in the Find window include all objects found within the entire design.

- Folder Level:

  a. In the Project manager, right-click on a folder and choose Find.

  b. In the Find text box, type the search string and press Enter.

  The search results displayed in the Find window include all objects found within the selected folder.

- Page Level:

  a. In the Project manager, right-click on a schematic page and choose Find.

  b. In the Find text box, type the search string and press Enter.

  The search results displayed in the Find window include all objects found on the selected page.

  OR

a. Open the schematic page to search and choose Find from the Edit menu.

Alternatively, use the Ctrl + F keyboard shortcut.

b. In the Find text box, type the search string and press Enter.

The search results displayed in the Find window include all objects found on the selected page.

- Multiple Object selection.

a. In the Project manager, use the Ctrl + mouse click combination to select multiple objects.

You can select multiple folder or multiple pages or any combination of folders and pages.

a. Right-click on the selection and choose Find.

b. In the Find text box, type the search string and press Enter.

The search results displayed in the Find window include all objects found within the selected items in the design hierarchy.

Capture directory map

Capture directory contents

CAPTURE.EXE	The Capture executable. It appears in the OrCAD Desktop program group as Capture.

CAPTURE.INI	Capture's initialization file. You can specify a new location for Capture to create and modify the .INI file. Use one of the following command lines to specify the new location of the .INI file:
	`CAPTURE -I directory`
	`CAPTURE /I directory`
	where path is the directory where the .INI is located. For example:
	`CAPTURE -I C:\CAPTURE`

*.EXE, *.PIF, *.DLL, and *.NT	Executable files, program information files, and other files required by Capture.
Library directory	Contains the Cadence-supplied library files (.OLB), including the CAPSYM.OLB symbol library.
Netforms directory	Contains the netlist format files used by Capture.
Samples directory	Contains sample designs.
Tutorial directory	Contains: CAPTUTOR.EXE, Capture's tutorial, which appears in the OrCAD Desktop program group as Learning Capture. .PDFs, the help files associated with the tutorial. MSVBVM60.DLL, Visual Basic run-time DLL. CAPTURE.LRN, additional file created when you run the tutorial. Keeps track of learner progress.

Capture file types

*.BCF	Binary SDT configuration file, used in translation.
*.BOM	Bill of materials report file.
*.CFG	SDT configuration file, used in translation.
*.CIR	SPICE netlist file.
*.DBK	Design backup file.
*.DRC	Design rules check file.
*.DSN	Design file.
*.DSF	VST Model netlist file.
*.EDN	EDIF netlist file.
*.ERR	DSN2MNL error text file.
*.EXP	Export property file.
*.INC	Bill of materials include file.

*.INF	VST file.
*.INS	Netlist creation file.
*.LIB	Layout or SDT library file.
*.MAP	SPICE map file.
*.MNL	Layout netlist file.
*.NET	Netlist file for most netlist formats.
*.OBK	Library backup file.
*.OLB	Library file.
*.OPJ	An OrCAD project file. It contains references to all other files included in the project.
*.PIP	Netlist creation file.
*.PLD	OHDL netlist file.
*.RES	Netlist creation file.
*.RPT	Update properties report file.
*.SCH	SDT schematic folder file.
*.SWP	Gate and pin swap file.
*.TXT	Session log text file.
*.UPD	Update properties file.
*.V	Verilog netlist file.
*.VHD or *.VHO	VHDL file.
*.XNF	XNF netlist file.
*.XRF	Cross reference file.

Capture configuration

Establishing the configuration for Capture requires that you determine the scope of each configuration setting. Capture provides different levels of configuration. Using commands on the Options menu, you can:

- Customize the working environment specific to your system (set preferences in the Preferences dialog box).
- Create default settings for new designs (with the Design Template command). These settings stay with the design even if it is moved to another system with different preferences.
- Override design template settings in individual designs (with the Design Properties command command) or individual schematic pages (with the Schematic Page Properties command).
- Create default settings for new parts (set part properties using the Part Properties command).
- Override default properties on individual parts (set package properties using the Package Properties command).

No matter where you are in Capture, the Options menu always has a Preferences command and a Design Template command. In addition, the Options menu contains a command specific to the current active window. For example, the project manager's Options menu contains the Design Properties command, while the schematic page editor's Options menu contains the Schematic Page Properties command.

The settings in the Preferences dialog box determine how Capture works on your system, and persist from one Capture session to the next. However, if you pass a design to another person, that person doesn't inherit your Preferences settings. This means that you can set colors, grid display, pan and zoom, and other things to your liking, and they won't change, even if you work on a design created on someone else's system.

The Design Template / Design Properties dialog box determines the characteristics of all the designs created on your system. Because a new design inherits characteristics from the current design template, it's a good idea to check the design template settings before you create a new design.

Once you begin working on a design, you can customize its particular characteristics by choosing the Design Properties command from the Options menu when you are in the project manager, or the Schematic Page Properties command when you are in the schematic page editor.

Similarly, you use the Part Properties command and the Package Properties command on the part editor's Options menu to set default part properties and customize those settings for individual parts.

Intertool communication

Capture is designed to communicate interactively with the Cadence PCB board layout tools.

Using Capture with the PCB board layout tools

Capture can communicate with the PCB board layout tools (like PCB Editor) directly using a form of intertool communication (ITC). With PCB Editor, cross probing displays corresponding parts and nets as well as individual pins.

You use a netlist to create a new board by communicating design information between the PCB board layout tool and Capture. Capture also generates report files that are compatible with the layout. You can back annotate your design to incorporate changes made to a board design in your layout tool.

For more information about using the PCB board layout tool (like PCb Editor), see the online help for these tools.

2

Opening a project

This chapter covers:

- "Opening a project" on page 95
- "Starting a new project" on page 95
- "Opening an existing project" on page 127
- "Working with the project manager" on page 130
- "Working with schematic pages" on page 139
- "Closing a project" on page 150

Opening a project

A project in Capture generally refers to the collection of design file, part libraries, report files, and other associated materials that exist, as a set, within the Capture environment.

Starting a new project

This section covers:

"Using the project wizard" on page 96

"Setting project preferences" on page 99

"Setting up the design template" on page 110

Whenever you start a new project, you can define it as a PCB, Programmable Logic, or PSPICE project. Or, barring that, you can leave the project definition unspecified in order to build schematics

that are not associated with a particular medium. Capture's project wizard facilitates project creation.

Using the project wizard

A project file (.OPJ) is a container for the design file (.DSN). There can be only one design file in a project. The project file stores pointers for interacting with the design file and other referenced files, and outputs reports associated with the design file.

The project file can also contain libraries, VHDL files, and information from the various Tools dialog boxes.

When the project is first created, the project manager creates a design file with the same name as the project. It also creates a schematic folder within the design file, and a schematic page within the folder. You can create a new design to replace the design created by the project manager. See Creating a new design.

Project types

Capture includes project wizards that provide an easy method for creating specific project types, complete with library and simulation resources.

- Analog or mixed signal circuit for designs to be used with OrCAD PSpice.
- PC board for designs to be used with PCB board layout tools.
- Programmable logic project for designs that may include Verilog or VHDL models as part of the structure. Projects of this nature will often use simulation and synthesis tools as part of the design flow. When you create a programmable logic project, certain folders are added to the project. These are discussed in Working with the project manager.
- Schematic. Select this type of project if none of the other project types apply. Using this option, Capture creates a basic project containing only the design file.

Note: The project types available to you will depend upon which OrCAD programs you have installed. As a minimum, you will have the option to create a PC board or Schematic project type. Be sure to specify the appropriate type when you are creating your project.

To create a project with the project wizard

Capture includes project wizards that provide an easy method for creating specific project types, complete with library and simulation resources.

1. Choose *File – New*, then choose the Project command. The New Project dialog box appears.
2. Type a name for your new project in the name text box.

Note: Do not specify a dot (.) in the project name.

3. Use the browse button to select a new directory.
4. Select a project type in the Create a New Project Using group box, and click OK.

Continue with the steps below that are appropriate for the type of project you are starting.

Note: The project types available to you will depend upon which OrCAD programs you have installed. As a minimum, you will have the option to create a PC board or Schematic project type.

Note: While using the Save As dialog box to rename the project name, do not specify a dot (.) in the project file name.

Schematic (no simulation)

1. Click the Finish button.

Programmable logic project

1. Select the logic vendor and target family for the project (for example, Altera MAX5 Family).
2. Specify the VHDL models to be used as library models for the project. You can use the default models, provided by Capture, or your own custom VHDL models.
3. Click the Finish button.

Analog or mixed signal project

1. Select the vendor part symbol libraries that you wish to include in your project, and click the Add button.
2. Click the Finish button.

PC board project

1. Select the Enable project simulation check box if you intend to have simulation capabilities in your PCB design. If you selected Enable project simulation, go to step 2. Otherwise, go to step 3.
2. Select the type of simulation resources you want to include.
   - ❑ Analog or mixed signal
   - ❑ VHDL-based
   - ❑ Verilog-based
3. Click Next.
4. Continue with the steps below that are appropriate for the simulation resource you chose.

Analog or mixed signal simulation

1. Select a PSpice symbol library you want to include in your project and click the Add button (or double-click the library name). Continue this step until you have chosen all the libraries you want.
2. Click the Finish button.

VHDL-based simulation

1. Select the PCB part symbol libraries you want to include in your project, and click the Add button.
2. Click the Next button.

Select the VHDL model libraries that you want to include in your project, and click the Add button.

1. Click the Finish button.

Note: Typically, referenced projects are FPGA projects that you want to include in your PCB project. This is useful for board simulation that

includes the appropriate timing and functionality information for an FPGA that is included in your printed circuit board.

Note: Some symbol libraries do not have corresponding simulation models.

Setting project preferences

This section covers:

- "Setting colors for objects on the schematic page" on page 101
- "Controlling the grid display" on page 101
- "Setting pan and zoom" on page 105
- "Defining selection options" on page 106
- "Setting miscellaneous options" on page 106
- "Setting Text editor options" on page 110

You set project preferences by using the Preferences dialog box. The settings in the Preferences dialog box determine how Capture works on your system, and persist from one Capture session to the next because they are stored in the Capture initialization (.INI) file on your system. If you pass projects to others, they won't inherit your preference settings. This means you can set colors, grid display options, pan and zoom options, and so on to your liking and be assured that your settings will remain, even if you work on a project created on another system.

Once you begin working on a project, you can customize its particular characteristics by choosing Design Properties from the Options menu when you are in the project manager, or Schematic Page Properties when you are in the schematic page editor.

Colors/Print

Set up colors for objects such as off-page connectors, hierarchical blocks and ports, text, title blocks, and so on, and

specify which objects will be printed or plotted. You can also change the background color and the color of the grid.

Grid Display

Select dots or lines for your grid, and whether to display or print your grid. You can select whether to have your pointer snap to grid as you place objects. You can set these options independently for the schematic page editor and the part editor.

Pan and Zoom

Define how you want autoscrolling to work, and what the zoom factor should be. You can set these options independently for the schematic page editor and the part editor.

Select

Define whether you want to select objects enclosed by a selection rectangle or objects inside and intersecting a selection rectangle, the maximum number of objects to display at high resolution while dragging, and whether to show the tool palette. You can set these options independently for the schematic page editor and the part editor.

Miscellaneous

Define the default fill, line style and width, and color for graphic objects, define the font used in the project manager and session log, render TrueType fonts with strokes (for printing and plotting), and set whether to auto recover your project and how often. In addition, you can enable intertool communication, which is the method that Capture uses to communicate with other OrCAD software, such as PCB Editor.

Text Editor

Define which (if any) VHDL keywords are highlighted, and the font and tab settings used within the text editor.

Setting colors for objects on the schematic page

You control the color in which schematic page objects display by using the Colors/Print tab in the Preferences dialog box.

1. Choose *Options – Preferences*, then choose the Colors/Print tab.
2. Click the left mouse button on the color of an item. The color palette window opens.
3. Select a new color. Click OK to dismiss the color palette.
4. Click OK.

Note: The color that you select for Title Block is also the color used for borders and grid references.

Graphics objects (lines, polylines, and arcs) use the colors specified by Miscellaneous tab. If the color options in the Miscellaneous tab are set to Default color, then Capture uses the color specified for graphics by the Colors/Print tab.

Controlling the grid display

Grid spacing is expressed as a fraction of pin-to-pin spacing, as follows:

1/*n*

where
n = an integer with a value of 1, 2, 5, or 10

So, for example, a setting of 1/2 specifies that the grid spacing on the schematic page is set to exactly half the specified pin-to-pin spacing.

Note: This setting applies only to the schematic page grid, *not* to the part and symbol grid.

To control the grid

You can control whether Capture displays a grid independently in the schematic page editor and the part editor, and whether the grid uses dots or lines. You can also specify whether the pointer snaps to grid in each editor. Additionally, you can now specify whether the drawing

objects, like Line, Polyline, Text, Rectangle, Ellipse, Arc, and Picture can be placed on fine grid.

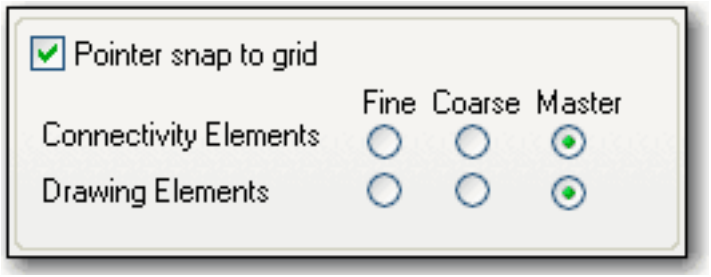
1. Choose *Options – Preferences*, then choose the Grid Display tab.
2. For the schematic page editor and the part editor, specify:
   - ❑ Whether to display the grid.
   - ❑ Whether the grid uses dots or lines.
   - ❑ The grid spacing (that is, the space between each point on the grid).
   - ❑ Whether the pointer snaps to grid as you place objects.

   Note: The pointer by default snaps to the grid for connectivity and drawing objects.
3. Click OK.

Customizing placement and movement of objects on the schematic

OrCAD Capture now enables you to customize the placement and movement of connectivity (part, symbol) and drawing objects (Line, Polyline, Text, Rectangle, Ellipse, Arc, and Picture) on coarse and fine grid in the schematic editor. You can use the options (see figure below) provided in the Grid Display tab of the Preferences dialog box to complete this task.

Note: These settings apply only to the schematic page grid; *not* to the part and symbol grid.



Note: The settings are saved in the CAPTURE.INI file and it is used whenever you start the next Capture session.

The connectivity and drawing objects can be individually configured to follow either coarse or fine grid. The following scenarios describe the usage of the above options:

If...	Then...
The *Master* option is selected for both Connectivity and Drawing Elements and the *Pointer snap to grid* check box is not selected	The connectivity and drawing objects can be placed and moved only on the fine grid.
The *Master* option is selected for both Connectivity and Drawing Elements and the *Pointer snap to grid* check box is selected	The connectivity and drawing objects can be placed and moved only on the coarse grid.
The *Master* option is selected for Connectivity Elements and the Fine option is selected for Drawing Elements and the *Pointer snap to grid* check box is not selected	The connectivity and drawing objects can be placed and moved only on the fine grid.
The *Master* option is selected for Connectivity Elements and the Fine option is selected for Drawing Elements and the *Pointer snap to grid* check box is selected	The connectivity objects can be placed and moved on the coarse grid and the drawing objects on the Fine grid.
The *Fine* option is selected for both Connectivity and Drawing Elements and the *Pointer snap to grid* check box is either selected or not selected	The connectivity and drawing objects can be placed and moved only on the fine grid.
The *Coarse* option is selected for both Connectivity and Drawing Elements and the *Pointer snap to grid* check box is either selected or not selected	The connectivity and drawing objects can be placed and moved only on the coarse grid.
The *Fine* option is selected for Connectivity Elements and the Coarse option is selected for Drawing Elements, and the *Pointer snap to grid* check box is either selected or not selected	The connectivity objects can be placed and moved on the fine grid and the drawing objects on the coarse grid.
The *Coarse* option is selected for Connectivity Elements and the Fine option is selected for Drawing Elements, and the *Pointer snap to grid* check box is either selected or not selected	The connectivity objects can be placed and moved on the coarse grid and the drawing objects on the Fine grid.
The *Coarse* option is selected for Connectivity Elements and the Master option is selected for Drawing Elements, and the *Pointer snap to grid* check box is selected	The connectivity and drawing objects can be placed and moved only on the coarse grid.

If...	Then...
The *Coarse* option is selected for Connectivity Elements and the Master option is selected for Drawing Elements, and the *Pointer snap to grid* check box is not selected	The connectivity objects can be placed and moved on the coarse grid and the drawing objects on the fine grid.
The *Master* option is selected for Connectivity Elements and the Coarse option is selected for Drawing Elements, and the *Pointer snap to grid* check box is not selected	The connectivity objects can be placed and moved on the fine grid and the drawing objects on the coarse grid.
The *Master* option is selected for Connectivity Elements and the Coarse option is selected for Drawing Elements, and the *Pointer snap to grid* check box is selected	The connectivity and drawing objects can be placed and moved only on the coarse grid.

Note: However, if your selection contains both connectivity and drawing objects then precedence will be given to option set for Connectivity Elements.

Note: Ensure that the *Pointer snap to grid* check box is selected and the Connectivity Elements is set to Coarse while placing connectivity objects. Otherwise, your part pins may be placed on the fine grid, making it difficult to connect them properly.

You can configure Capture to hide the grid or display it as dots or lines, and to constrain the pointer to the grid.

To specify grid style, spacing and visibility

Choose *Options – Preferences* command, then choose the Grid Display tab.

Choose the grid style and spacing, and click the left mouse button on the Displayed or Printed option to change the visibility.

or (to set grid visibility only)

Choose *View – Grid*. The visibility of the grid toggles on or off.

To change snap to grid

1. Choose *Options – Preferences*, then choose the Grid Display tab.
2. Select or clear the Pointer snap to grid option.

or

➤ Press CTRL+T.

Setting pan and zoom

Pan

When you hold the left mouse button down and move the pointer near the edge of the window while, the display scrolls to a different region of the document. This change is called panning. This only works if the full schematic is being displayed larger than screen.

The Auto Scroll Percent setting determines the percentage of the screen that changes when panning.

Zoom

When you zoom in or out, the view changes by the zoom factor.

To configure zoom factor and auto scroll percent

1. Choose Options – Preferences, then choose the "Pan and Zoom tab" on page 1150.
2. For the schematic page editor and the part editor, set these options:
3. Zoom Factor. Enter an integer to indicate the magnification or reduction of the objects shown in the window when you zoom in or zoom out. This number is a multiplier for each time you zoom in or out.
4. Auto Scroll Percent. Enter the percent of the window's horizontal or vertical dimension by which the display will scroll when the

pointer approaches the edge of the window with an object attached.

5. Click OK.

Defining selection options

You can specify whether objects are selected when the selection border intersects them or if the objects are selected only when they are completely enclosed in the selection area.

You can also change the maximum number of objects displayed at high resolution while dragging, and set tool palette visibility in both the schematic page editor, and the part and symbol editor.

To define selection options

1. Choose *Options – Preferences*, then choose the Select tab.
2. For the schematic page editor and the part editor, set these options:
   - Area Select. Specify whether to select objects that are inside and intersecting the selection border or only objects that are fully enclosed by the selection border.

     Note: If the Fully Enclosed option is selected and you select an object on a schematic page, make sure that you select the object along with its name and number. Otherwise, the object does not get selected.
   - Maximum number of objects to display at high resolution while dragging. If you drag more objects than you specify here, you will see rectangular placeholders for the objects as you drag them.
   - Show Palette. Select this check box to make the tool palette visible; deselect it to make the tool palette invisible.
3. Click OK.

Setting miscellaneous options

Using the Miscellaneous tab you can:

- specify the default fill, line style and width, and color for graphics objects.
- define the font used in the project manager and session log.
- render TrueType fonts with strokes (for printing and plotting).
- set whether to enable auto recovery for your project and how often.
- enable intertool communication (the method that Capture uses to communicate with other OrCAD software, such as OrCAD PSpice and the PCB layout tools).

Fill Style

Specifies a fill pattern for rectangles, ellipses, and polygons.

Line Style and Width

Specifies both line style and line width for lines, polylines, rectangles, ellipses, and arcs.

Color

Specifies the color of lines, rectangles, and ellipses in the schematic page editor.

Note: This color is not the default color, but can be set to use the default color. This option does override the default color. However, changing this setting won't change the color of objects already placed in the schematic page editor.

Polylines and arcs use the default color of objects set in the Colors tab.

Note: You can change the fill style, line and width style, and color on individual objects using the Properties command on the Edit menu.

Project Manager and Session Log

Specifies the font for the project manager and session log. If you click on this box, a standard Windows Font dialog box for font selection

appears. This option is neither a schematic page nor a part editor option.

Enable intertool communication

Enables intertool communication with other OrCAD products such as PSpice or the PCB layout tool. For more information about intertool communication, see Intertool communication. This option is not specific to either the schematic page editor or the part editor.

Text Rendering

The text rendering options affect how text on a schematic page appears on your screen, and how it is printed or plotted. The Render TrueType fonts with strokes option displays text as a series of lines, connected to resemble the outlines of the corresponding TrueType letters or numbers they represent.

Enabling the Fill text option causes the text outlines to be filled in.

Auto Recovery

You can specify any interval between five minutes and 120 minutes. When the time interval is up, any design, library, or VHDL file in your project that hasn't been saved, or has been modified since the last save, is saved as a temporary file (with an .ASP extension) in the WINDOWS/TEMP/AUTOSAVE directory.

When you close your project normally, the /AUTOSAVE directory and temporary files are deleted. In cases of power outages or system crashes, however, the temporary files are saved. When you restart Capture, it loads the auto recovered files, showing "Restored" in their title bars. You must use the Save As command and provide a filename to have an auto recovered file overwrite the original file.

Note: Auto recovery is not an automatic saving feature. If you intentionally exit Capture without first saving your changes, they will be lost. Auto recovered files are automatically deleted when you exit Capture normally.

To set miscellaneous options

1. From the Options menu, point to Preferences, then choose the Miscellaneous tab.
2. For the schematic page editor and the part editor, set these options:
   - Fill Style. Select the fill pattern to be used when drawing rectangles, ellipses, and closed shapes drawn with the polyline tool.
   - Line Style and Width. Select the line style and width used for lines, polylines, rectangles, ellipses, and arcs.
3. For the schematic page editor, set this option:
   - Color. Select the color used for graphic objects (rectangles, ellipses, and closed polylines).
4. Set the following options:
   - Project Manager and Session Log. Select a font for display text in the project manager and session log. If you select this option, a standard Windows dialog box for font selection appears. Select a font, style, and size from the dialog box, then click OK.
   - Text Rendering. The text rendering options affect how text on a schematic page appears on your screen, and how it is printed or plotted.
   - Auto Recovery. Select whether to enable auto recovery for your project and, if so, the interval between saves. You can specify any interval between five minutes and 120 minutes. When the time interval is up, any design, library, or VHDL file in your project that hasn't been saved, or has been modified since the last save, is saved as a temporary file (with an .ASP extension) in the WINDOWS/TEMP/AUTOSAVE directory.
   - Auto Reference. Select whether to enable automatic annotating of reference designators when parts are placed.
   - Intertool Communication. Select whether to enable intertool communication (also known as ITC), so that you can test and display design information using other OrCAD software (such as the PCB layout tool and PSpice) in conjunction

with Capture. Capture processes its tools faster when intertool communication is not selected.

5. Click OK.

Setting Text editor options

Capture's text editor options include automatic highlighting of VHDL keywords, comments, or quoted strings. You can enable or disable the highlighting feature, and set the text editor font and tab spacing.

1. Choose *Options – Preferences*, then choose the Text Editor tab.
2. Set these options:
   - ❑ Syntax Highlighting. Select the color to use to highlight VHDL keywords, comments, and quoted strings. You can choose a different color for each.
   - ❑ Current Font Setting. Click Set to change the font setting for the text editor to values other than those displayed.
   - ❑ Tab Spacing. Set the tab spacing for the text editor.
3. Check the Highlight Keywords, Comments, and Quoted Strings option to have those VHDL items highlighted in the text editor. The colors used to highlight these items are the ones set in the Syntax Highlighting group box.

   Note: The Highlight Keywords, Comments, and Quoted Strings option must be enabled for Capture to use the syntax highlighting options.
4. If you want to reset the text editor options to the Capture default values, click the Reset button.
5. Click OK.

Setting up the design template

This section covers:

■ "Defining fonts for new designs" on page 112

■ "Defining the title block" on page 113

- "Setting up a page" on page 118
- "Defining the grid reference" on page 119
- "Specifying the default hierarchy option for new projects" on page 120
- "Setting compatibility with OrCAD's Schematic Design Tools" on page 121

You set the design template using the Design Template / Design Properties dialog box. The Design Template dialog box determines the default characteristics of all the projects created on your system. Because a new project inherits characteristics from the current Design Template settings, it's a good idea to check the settings before you create a new project.

The options that you define in the Design Template dialog box are the default settings for all new projects, and for schematic pages you add to an existing project.

Fonts

You can define the fonts for schematic page objects that contain text, such as part references and values.

Title Block

You can specify the text to appear in title block fields, as well as the path and filename of the library containing the title block. This affects new projects, as well as new schematic pages in existing projects.

Page Size

You can specify whether inches or millimeters are used as the unit of measure, the width and height of a schematic page, and the spacing between pins.

Grid Reference

For horizontal and vertical border grid references, you can set the number of border grid references to display in either direction,

whether the grid references are alphabetic or numeric, whether they increment or decrement across the schematic page, and how wide grid reference cells are. You can also make the border, grid references, and title block visible or invisible. This affects new projects.

Hierarchy

For hierarchical blocks and part instances that have their Primitive property set to Default, you can specify if you want Capture to treat each as primitive (cannot descend into attached schematic folders) or nonprimitive (can descend into attached schematic folders).

SDT Compatibility

You can specify which Capture properties map to which OrCAD Schematic Design Tools (SDT) part fields when saving a project in SDT format.

Defining fonts for new designs

You can define the fonts assigned to the text associated with different schematic page objects in new designs. The fonts specified here do not affect existing designs.

Note: To change the fonts for an existing project, use the Fonts tab in the Design Properties dialog box. You can access this dialog box by choosing Design Properties from the project manager's Options menu.

To assign fonts for new designs

Note: The default fonts were selected for optimal compatibility with SDT. Changing these fonts may result in less than optimal text sizes for translated projects.

1. From the Options menu, choose the Design Template command, then choose the Fonts tab.
2. Click the left mouse button on the font of an item. A standard Windows font dialog box appears.

3. Select a font, font style, and size. Click OK to dismiss the font dialog box.
4. Click OK.

Defining the title block

There are two types of title blocks: default and optional. Capture places one default title block—which you specify on the Title Block tab in the Design Template / Design Properties dialog box in the lower right corner of each new schematic page. You may place any number of optional title blocks anywhere on the schematic page, using the Title Block command on the Place menu.

Default title block

You specify the information that goes into the default title block in the Title Block tab of the Design Template dialog box. Capture places a default title block in the lower right corner of each schematic page (if a library and title block name is specified), and places the information you enter in the text fields in the Title Block tab into the title block.

This information is also used in reports created by the commands on the Tools menu. It affects new projects, as well as new schematic pages in existing projects.

You can set the default title block to be visible or invisible on an existing schematic page by changing the setting in the Grid Reference tab in the Schematic Page Properties dialog box.

Capture provides default title block symbols in the CAPSYM.OLB library.

Not all of the available default title blocks provide the same information. For example, TitleBlock0 doesn't provide any properties for the organization name and address, while TitleBlock5 provides the organization name property and all five of the address properties. You must specify which title block you want for the default in the Design Template.

The default title block properties that are set in the Design Template dialog box are as follows:

Cage Code: Specifies the Cage Code.

Design Create Date: Specifies the date of creation for the design.

Design Create Time: Specifies the time of creation for the design.

Design File Name: Specifies the path and file name of the design file.

Design Modify Date: Specifies the date of the last modification to the design.

Design Modify Time: Specifies the time of the last modification to the design.

Design Name: Specifies the name of the design.

Doc: Specifies the document number.

Name: Specifies the name of the title block.

OrgAddr1: Specifies the first line of the organization's address.

OrgAddr2: Specifies the second line of the organization's address.

OrgAddr3: Specifies the third line of the organization's address.

OrgAddr4: Specifies the fourth line of the organization's address.

OrgName: Specifies the organization’s name.

Page Count: Specifies the number of schematic pages in the design.

Page Create Date: Specifies the date of creation for the schematic page.

Page Create Time: Specifies the time of creation for the schematic page.

Page Modify Date: Specifies the date of the last modification to the schematic page.

Page Modify Time: Specifies the time of the last modification to the schematic page.

Page Number: Specifies the number of the schematic page. The page number determines when it will be printed in relation to the other schematic pages of the design.

Page Size: Specifies the page size of the schematic page, as was set at creation time.

RevCode: Specifies the revision.

Schematic Create Date: Specifies the date of creation for the schematic.

Schematic Create Time: Specifies the time of creation for the schematic.

Schematic Modify Date: Specifies the date of the last modification to the schematic.

Schematic Modify Time: Specifies the time of the last modification to the schematic.

Schematic Page Count: Specifies the number of schematic pages in the given schematic.

Schematic Page Number: Specifies the order of the schematic page within the schematic.

Source Library: Specifies the path and file name of the library from where the title block was placed.

Symbol Library: Specifies the name of the symbol for the title block in the Source Library.

Title: Specifies the title.

You can add the following property to display system generated information:

Path Name: Specifies the hierarchical blocks leading from the root to the child using the Name Property for each hierarchical block in the path.

You can use the property editor to add the following property to display the hierarchical path of the schematic on an instance of a title block:

Schematic Path: Displays the full hierarchical path to the schematic visible and printable on the page.

Note: You can create custom title blocks and store them in a library using the New Symbol command from the project manager's Design menu. If you specify the name of the custom library and title block in the Symbol group box of the Design Template's Title Block tab, the custom title block appears in the lower right corner of each new schematic page.

Optional title block: You can place any number of optional title blocks anywhere on the schematic page using the Title Block command on the Place menu. Optional title blocks display information that you define as property values for the title block symbol.

To choose a title block and define the text it contains

1. Choose *Options – Design Template*, then choose the Title Block tab.
2. In the Text group box, enter the information you want to appear in the title block.
3. In the Symbol group box, enter the path and filename of the library containing the title block.

   The Library Name text box can be left blank if you are using title block from the CAPSYM.OLB library and CAPSYM.OLB has not been moved to a different directory from where it was installed.

   If you are using a custom title block, then put the full path and file name for the library in the Library Name text box. You can use the Browse button to locate a previously-defined custom title block.
4. Enter the exact name of the title block into the Title Block Name text box. Symbol names are case sensitive and space sensitive.
5. Click OK.

Note: You can create custom title blocks and store them in a library using the New Symbol command from the project manager's Design menu. If you specify the name of the custom library and title block in the Symbol group box of the Design Template's Title Block tab, the custom title block appears in the lower right corner of each new

schematic page.

For Capture to automatically place the information you entered in the text fields into your custom title block, you must give your custom title block the appropriate properties.

You can use the Design Template command of the Options menu to specify information for the default title block. In addition, you can edit title block information in the schematic page editor.

To edit title block information

1. Select the information string on the title block that needs to change.
2. Choose *Edit – Properties*. The Display Properties dialog box appears.
3. Replace the old information with the new and click OK. The schematic page editor appears with the new information in the title block.

or

1. Select the title block, and choose *Edit – Properties*. The property editor appears.
2. Place the cursor in the cell of the property you want to change, and enter the new value.
3. Click Apply, and close the property editor. The schematic page editor appears with the new information in the title block.

To edit title block information on multiple pages

1. Select the design file in the project manager.
2. Choose *Edit – Browse – TitleBlocks*. Click OK to dismiss the Browse Properties dialog box.
3. In the Browse window, select the name or names of the schematic pages that contain the title blocks you want to edit.
4. Choose *Edit – Properties* or press CTRL+E. The Browse spreadsheet editor appears. Use the Browse Spreadsheet to edit properties on one or more schematic pages at a time.

To change the display of title block information

1. Select the information string on the title block that needs to change.
2. Choose *Edit – Properties*.
3. In the Display Properties dialog box, choose the Change button. The Fonts dialog box appears.
4. In the Fonts dialog box, change the display properties, and click OK twice.

Shortcuts

Double-click on the information string to display the Display Properties dialog box, or double-click on the title block to display the Properties dialog box.

Setting up a page

For new projects, you can specify the default unit of measure, the default width and height of schematic pages, and the spacing between pins. The value you enter in the Pin-to-Pin Spacing text box defines how close together pins are placed in the part editor. It also defines the grid spacing.

Changing from Inches to Millimeters resets the page sizes to their defaults; therefore, if you make any changes to the standard page size dimensions, then change the units, the page size changes are not translated between the two types of units.

To set up the schematic page size

1. Choose *Options – Design Template*, then choose the Page Size tab.
2. In the Units area, select the default unit of measure for new projects. This setting only affects the schematic page editor, not the part editor.

   Note: Changing from Inches to Millimeters resets the page sizes to their defaults; therefore, if you make any changes to the standard page size dimensions and then change the units, the

page size changes are not translated between the two types of units.

3. Select the default schematic page size for new projects. For each schematic page size (A, B, C, D, E, and Custom if the unit of measure is Inches; or A4, A3, A2, A1, A0, and Custom if the unit of measure is Millimeters) you can specify the width and height. The values that you enter in the Width and Height text boxes become the dimensions for each page size. You cannot change these dimensions for individual schematic pages, although you can select a different page size, or choose to define a custom size.

4. In the Pin-to-Pin Spacing text box, specify the default spacing between pins. The value you enter in this text box defines how close together pins are when you place a part on a schematic page. It also defines the grid spacing (the space between grid dots or grid lines). You cannot change this value for existing projects or individual schematic pages.

   Note: Part size will vary when copying and pasting parts between pages with different pin-to-pin spacings.

5. Click OK.

Defining the grid reference

You set the border's grid references to display either horizontally or vertically, alphabetically or numerically, incrementally or decrementally across the schematic page, and the width of their cells. You can also make the border, grid references, and title block visible or invisible on the screen and on schematic pages you print.

The settings affect new projects.

Note: You can change these settings for existing schematic pages. Choose Schematic Page Properties from the schematic page editor's Options menu, then choose the Grid Reference tab in the Schematic Page Properties dialog box.

To define the grid reference

1. Choose *Options – Design Template*, then choose the Grid Reference tab.

2. Specify the number of border grid references, whether they are alphabetic or numeric, whether the grid references increment (Ascending) or decrement (Descending) across the schematic page, and how wide the grid reference cells are.

   Note: The size of the Grid Reference font is tied to the width.

3. For the border, title block, and grid reference, select Displayed to have the item display on the screen or Printed to have the item appear on schematic pages you print. Select ANSI grid references to display the grid references in accordance with ANSI standards (see the glossary entry ANSI).

4. Click OK.

Specifying the default hierarchy option for new projects

For hierarchical blocks and part instances that have their Primitive property set to Default, you can specify if you want Capture to treat each as primitive (cannot descend into attached schematic folders) or non-primitive (can descend into attached schematic folders).

The Primitive and Nonprimitive options only affect new projects.

Note: This setting affects how the options on the Tools menu process projects.

To define the default hierarchy option

1. Choose *Options – Design Template*, then choose the Hierarchy tab.

2. For hierarchical blocks and parts, select Primitive or Nonprimitive. All hierarchical blocks and part instances that have their Primitive property set to Default will use the setting selected here.

3. Click OK.

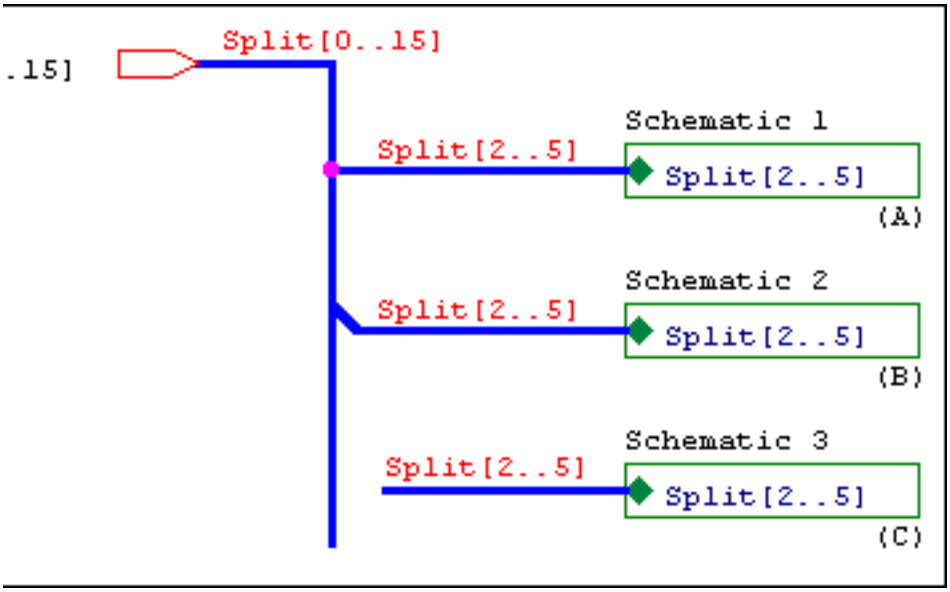
Note: You can change the hierarchy option for existing projects using the Hierarchy tab in the Design Properties dialog box. Choose Design Properties from the project manager's Options menu.

Setting compatibility with OrCAD's Schematic Design Tools

Capture uses the SDT compatibility options in the Design Template / Design Properties dialog box when you save a Capture design in SDT format. Capture sets the SDT compatibility options in the Design Properties dialog box when you open an SDT schematic folder (.SCH) file in Capture.

Capture uses a slightly different set of connectivity rules than SDT. The following cases explain the differences:

Case 1



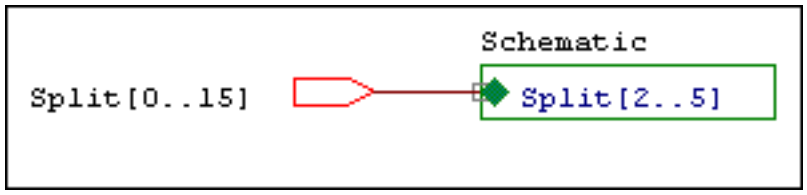
The bus is split with like members connecting before and after the split.

Situation A	The bus is split using a junction.
SDT	Yes
Capture	No—buses connected through a junction must contain the same number of signals.

Situation B	The bus is split using a bus entry.
SDT	Yes
Capture	Yes

Situation C	The bus is split without any visible connection, but is connected through name.
SDT	Yes
Capture	Yes

Case 2

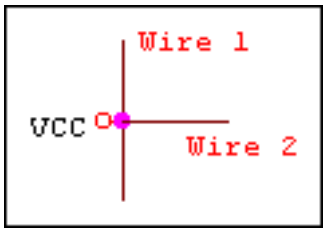


The hierarchical port connects to the hierarchical block through a wire.

SDT	Yes

Capture	No—wires in Capture are for single signals only.

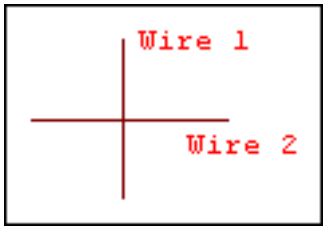
Case 3



The wire connects to the power symbol.

SDT	No
Capture	Yes

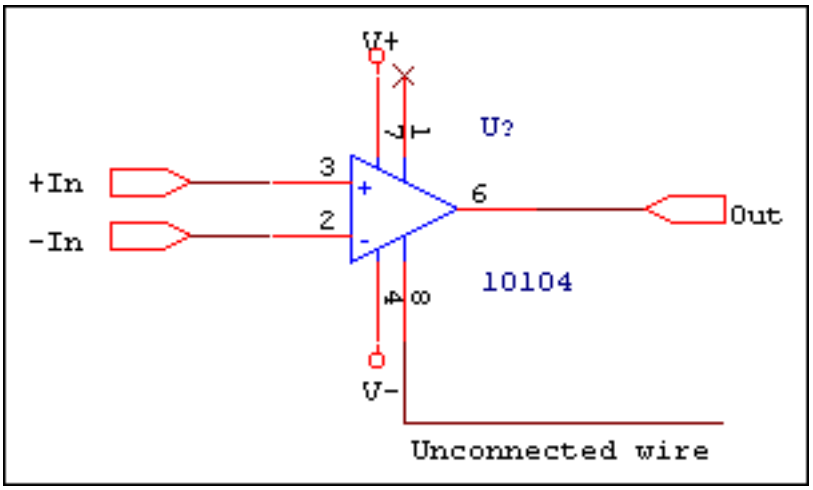
Case 4



Wire 1 connects to Wire 2 through a label hotpoint.

SDT	Yes
Capture	No—wires are connected only if they connect through a junction, or if they share an alias.

Case 5

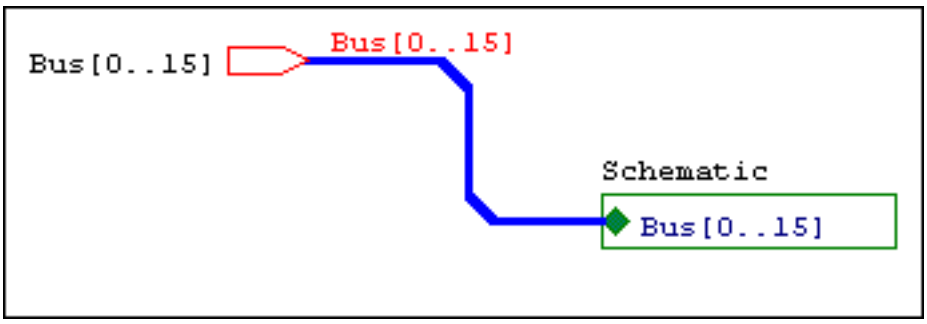


The hanging wire connected to a pin causes a single node net in netlists.

SDT No

Capture Yes

Case 6

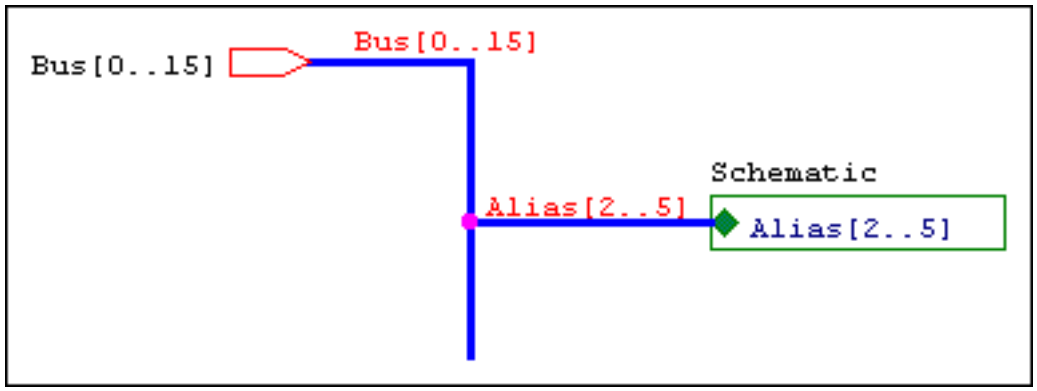


Buses routed through bus entries are connected to the target object.

SDT Yes

Capture	No—you should not use bus entries to route a bus to its target. Use the left mouse button to create turns in the bus route.

Case 7



Unlike bus members are connected.

SDT	No
Capture	Yes

You can specify which properties Capture stores in the eight SDT part fields when saving a project in SDT format. You can also use the part fields for mapping netlists that use part field information.

Note: To change the part field to property mapping for existing projects, use the SDT Compatibility tab in the Design Properties dialog box. (from the project manager's Options menu, choose Design Properties)

To set up compatibility with OrCAD's Schematic Design Tools

When you create a new design, the SDT compatibility options are inherited from the design template. Follow these steps to set up the design template for SDT compatibility:

1. Choose *Options – Design Template*, then choose the SDT Compatibility tab.

2. For each Capture property you want mapped to an SDT part field, specify the part field to contain the property value.
3. Click OK.

Changing the SDT compatibility options for a single design

When you save a design in SDT format, Capture uses the SDT compatibility options in the Design Properties dialog box. Follow these steps to change a design's SDT compatibility options:

1. With the program manager active, select the Design folder.
2. Choose *Options – Design Properties*, and choose the SDT Compatibility tab.
3. Specify the properties you want to map to the SDT part fields for the active design.

Translating part fields from SDT to Capture properties

Capture translates SDT part fields into properties. If you want to change the user property names before translation, follow these steps:

1. Open the design's SDT.CFG file in any text editor.
2. Locate the lines that specify the part field names, and change them to suit your needs.
3. Save your changes, and exit the editor.

Translating Capture properties to SDT part fields

You can specify properties for Capture to translate into SDT part fields by following these steps:

1. Choose *Options – Design Properties*, and then select the SDT Compatibility tab.
2. Specify the properties you want to map to the SDT part fields.

Opening an existing project

Once you have created a project in Capture, all library and schematic information defined therein, as well as any other included files, is recognized as being part of that project. When you open the project, all such data is automatically associated with it.

To open an existing project

1. From the File menu, choose the Open command. A standard Open dialog box appears.
2. If the project you want to open is not listed in the File name text box, do one or more of the following:
3. In the Look in drop-down list, select a new drive or directory.
4. In the File name text box, enter a portion of the file name—you can use the standard "*" and "?" wildcard characters.
5. Select the project or type the name in the File name text box, then click OK. The project opens in a project manager window.

Shortcut

Toolbar:

To open a recently used project

1. From the File menu, choose the project either by name or by number. The project opens in a project manager window.

Conversion of old analog projects to new project format

When you open an analog project created in Capture version 9.2.3 or older versions, the Update Old Project wizard appears.

The Update Old Project wizard allows you to convert your project to the Capture 10.0 format. Converting your analog project to the Capture 10.0 format has the following benefits:

- Capture 10.0 introduces a new directory structure for analog projects that makes it easier to manage the files for the project.
- You can use the new simulation profile features in Capture 10.0 if your project is in the Capture 10.0 format. For more information on the new simulation profile features, see the PSpice online help.

Important

Once you convert your project to the new format, you cannot open the project in the new format in Capture version 9.2.3 or older versions. You can create the project in the new format in a different location so that you have a backup of the project created in Capture 9.2.3 or older versions.

Important

Before you convert a project to the new format, ensure that the schematic names do not have the / (forward slash) or the \ (backward slash) character. If you do not do this, the conversion will fail. To rename a schematic that has the / or \ character in its name, select the schematic name in the Capture Project Manager and choose Rename from the Design menu.

To convert a project to the new format

1. Select the Convert the Project option to convert the project to the new project format.
2. Select the Retain Old Project check box to retain the project in its original location and create the project in the new format in a different location. Otherwise, the project in new format will overwrite this project.

   Note: You can open the old project in Capture 9.2.3 or older versions.
3. Click Next if you selected the Retain Old Project check box.
4. The Select New Project Path dialog box appears.
5. Type the location where you want the project in the new format to be created in the New Project Path text box.

6. Click Finish.
7. The Conversion Summary dialog box appears displaying the location of the new project and the new directory structure for the project.
8. Click Save to save the details of the conversion process in a file named `<projectname>_convert.txt` in the directory where the project in the new format is created.
9. Click Close.
10. The project in the new format is opened in Capture.

To automatically convert projects to the new format

1. Select the Convert the Project option to convert the project to the new project format.
2. Select the Retain Old Project check box to create project in new format in a different location. Otherwise, the project in new format will overwrite this project.
3. Select the Do not ask me this question again check box.

Any analog project created using version Capture 9.2.3 or older versions that you open in Capture 10.0 will be automatically converted to the new format.

Note: If you had selected the Retain Old Project check box, you will have to specify the location for the project in the new format in the Select New Project Path dialog box.

Later on, if you want to disable automatic conversion of old analog projects to the new project format, delete the entry given below that exists in the `[PSPICE]` section of the PSPICE.INI file.

- CONVERTDESIGN=CONVERT

  Or

- CONVERTDESIGN=CONVERT_AND_RETAIN

The PSPICE.INI file is located in the `/tools/pspice` directory under your installation directory.

To cancel conversion of the project to the new format

➤ Select the None option and click Finish if you do not want to convert the project to the new format.

The project in the old format is opened in Capture.

If you do not want to be prompted again to convert any analog project to the new format, do the following:

1. Select the None option
2. Select the Do not ask me this question again check box and click Finish.

Later on, if you want to enable conversion of old analog projects to the new project format, delete the following entry that exists in the `[PSPICE]` section of the PSPICE.INI file located in the `/tools/pspice` directory under your installation directory:

```
CONVERTDESIGN=NOCONVERT
```

Working with the project manager

This section covers:

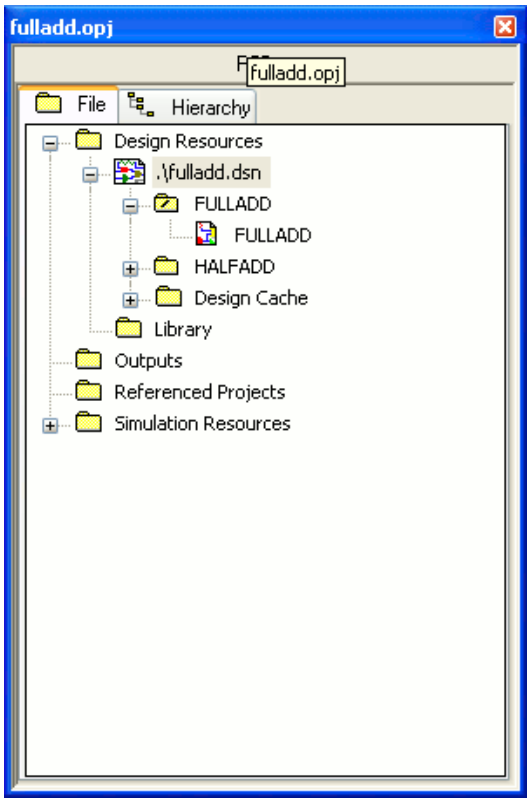
- "Moving and copying" on page 133
- "Adding a file to the project" on page 134
- "Deleting a file from the project" on page 135
- "Replacing and updating the cache" on page 136
- "Annotating a Design" on page 137
- "Searching for Schematic Objects" on page 138
- "Changing a Project Type" on page 138
- "Opening Containing Folder" on page 139

The project manager appears in the Capture session frame whenever you open or create a project. Use the project manager to collect and organize all the resources you need for your project throughout the design flow. These resources include schematic design files, part libraries, netlists, VHDL or Verilog models,

simulation models, timing files, stimulus files, and any other related information.

One design for one project

Each project may contain one design (.DSN). The design may consist of any number of schematic folders, schematic pages, or VHDL or Verilog models, but must have a single root module. The root module is the module that is defined as the top-level entity for the design. That is, all other modules in the design are referenced within the root module.



Views

The project manager provides two views of a project.

- File
- Hierarchy

File tab

The file tab is organized into folders and displays all the files included in the project. These files may include VHDL models, netlists, schematic pages, simulation models, stimulus files, or any other files that contain information related to the project.

For example, the File tab for a programmable logic project will include the following folders:

Preroute - a folder for functional simulation that stores prerouted design resource files.

Synthesis - a folder that contains post-synthesis netlists generated by a synthesis tool.

Postroute - a folder that contains postroute simulation resources, included timing annotated netlists.

The file view is shown in the illustration above.

Hierarchy tab

The Hierarchy tab shows the hierarchical relationship among the various design modules. A design module is a structural block, typically represented as a distinct hierarchical entity, that defines the functionality of a particular portion of your design. A design module in Capture can be a VHDL or Verilog model or a schematic folder.

Each instantiation of a particular module appears in the hierarchy view as part of a hierarchical "tree." The hierarchical view of the design is derived from the files that exist in the Design Resources folder.

Project manager behavior

Within the project manager, you can expand or collapse the structure you are viewing by clicking on the plus sign or minus sign to the left of a folder. A plus sign indicates that the folder has contents that are not currently visible; a minus sign indicates that the folder is open and its contents are visible, listed below the folder.

When you double-click on a schematic folder, Capture displays the schematic pages within that folder. If the folder is a VHDL model, Capture displays each defined entity in that model. If the folder is a Verilog model, Capture displays each defined module in the model.

When you double-click on a schematic page, a VHDL entity, or Verilog model, you open that object in an appropriate editor. For example, double-clicking on a VHDL entity opens the VHDL model file at the location of that entity definition in Capture's VHDL editor.

Each project you open has its own project manager window. You can move or copy folders or files between projects by dragging them from one project manager window to another (as well as from the Windows Explorer). If you close a project manager window, you close the project.

Moving and copying

You can use the standard Windows drag-and-drop operation to move or copy schematic folders, schematic pages, and libraries in the project manager windows. If you wish to copy rather than move, press and hold the CTRL key while you drag the entity.

Alternatively, you can use the Cut / Copy & Paste context menu options that are available when you right-click on schematic folders, schematic pages, and libraries.

If you move a part that has a part alias, the part alias also moves. In the context of dragging and dropping, a symbol behaves just as a part does—as shown in the table below, a symbol can be dragged from a design or a library and dropped in another library.

A document that is open in an editor, or one that contains any open elements, cannot be moved.

Documents can be moved as indicated in the following table:

Drag from . . .	Part	Schematic Page	Schematic Folder
Design to design		X	X
Design to library	X	X	X

Schematic folder to schematic folder		X	
Library to design			X
Library to library	X		X

1. If you are moving or copying a folder or page, verify that:
   a. for a folder, no Capture editor is open on any document in the schematic folder.
   b. for a page, that it is not open in any Capture editor.
2. Open both projects in their respective project managers.
3. Select the schematic folder, page, library, or symbol that you want to move or copy, then drag (pressing the CTRL key to copy) the selection to the destination project manager entity.
4. For both projects, from the File menu, choose Save All.

Note: If you copy or move a document from one design or library to another, you should save the destination design or library immediately. If you do not, you may lose data if you open the moved document in the schematic page editor or part editor and then close the editor without saving the document.

Note: Deleting schematic folders, schematic pages, parts and symbols is permanent. You cannot use the Undo command to bring back deleted items from the project manager.

Note: If you move or copy a parent schematic folder or schematic page from one project into a second project, Capture remembers the name and directory of the file containing the child schematic folder or folders. This information is stored in the Attach Implementation dialog box for each hierarchical block and nonprimitive part.

Adding a file to the project

Typically, the files you add to your project will be files that have specific functions in the design process. For example, you might add a standard delay file to provide timing information for simulation with NC VHDL or some other simulation tool. However, you can add any files you want to a project, including documentation files (perhaps a

functional specification) or waveform files (to show the results of a simulation).

To add a file to the project

1. In the project manager, select the folder to which you want to add a file.
2. Choose *Edit – Project*. The Add File to Project Folder dialog box displays.
3. Select the file you want to add and choose the Open button. The file is added to the project.

Or

1. Drag the file from the Windows Explorer into the folder in the project manager.

Note: You can also add files to your project interactively. When you create a design using the New command on the File menu, it is placed in the project manager's Design Resources folder.

Deleting a file from the project

You can delete files from your project just as you would delete files in Windows Explorer. That is, just select the file and press the Delete key.

Note: You cannot delete schematic pages or schematic folders if those schematic pages (or schematic pages within those folders) are currently open in Capture. You must first close the schematic pages in question.

Note: Deleting schematic folders, schematic pages, parts and symbols is permanent. You cannot use the Undo command to bring back deleted items from the project manager.

To delete a file from the project

1. In the project manager, select the file you want to delete.
2. Press the Delete key. The file is removed from the project.

Note: You cannot delete schematic pages or schematic folders if those schematic pages (or schematic pages within those folders) are currently open in Capture. You must first close the schematic pages in question.

Note: Deleting schematic folders, schematic pages, parts and symbols is permanent. You cannot use the Undo command to bring back deleted items from the project manager.

Replacing and updating the cache

When you place the first instance property of a part in a project, a copy of the part is created in the design cache. The design cache stores one copy of every part used in the design. (You can think of it as an embedded library.) All instances of the part normally refer to this copy in the design cache.

A cache part also retains a link to the library part on which it is based, so you can update or replace all of the parts in the design cache to synchronize them with the parts in the libraries.

The project manager updates the display of the design cache every time you open the cache. Just click on the design cache icon to close or open the design cache.

Using the Replace Cache and Update Cache commands

When you use the Update Cache command or the Replace Cache command with the option to preserve schematic part properties, the part retains all instance and occurrence properties. This means you will not lose any changes made to pin properties after the part was placed, including those made by the Back Annotate or the Annotate tools.

The Replace Cache and Update Cache commands are quite similar. However, there are a couple of significant differences between the two commands.

You can modify a part's link to the library (part name, path, and library) with Replace Cache, but not with Update Cache. Update cache only brings in new data when the path has changed.

Another difference is that if the path and library names do not change, Replace Cache reloads the part definition into the design. However, if Update Cache finds that the part name and the library names are the same, it does not bring in part changes.

Replacing parts in a design

If you need to replace a part in your project, you could open the schematic page editor to find and delete each instance of the part, then place the replacement part. If your design includes many instances of this part, you can more easily achieve the same end with the Replace Cache command.

Restoring parts in a design

When you delete a part, you also delete all of its properties. When you use the Replace Cache command to restore the part, the properties of the part instance are attached to the replacement part, but the pin properties are not restored.

You can also use the Replace Cache command if you want to undo edits to a part on a schematic page and restore the part's link to its library.

Finding libraries of origin

If you need to know a part's library of origin, you can select the part in the project manager, then select Replace Cache from the Design menu. The part name and the library and path are listed in the Replace Cache dialog box. Click the Cancel button to return to the project manager.

Discover the library of origin for multiple parts by selecting them in the project manager and choosing Cross reference from the Tools menu.

Annotating a Design

You can use the Annotate command on the right-click menu of the Project Manager to annotate your design.

Selecting this option will invoke the Annotate dialog box Annotate dialog box.

Searching for Schematic Objects

You can use the Find command on the right-click menu of the Project Manager to search for objects in your project.

Selecting this option will invoke the Find toolbar with the focus set to the Find text box.

Changing a Project Type

When you create a project Using the project wizard, you select the project type from the New Project dialog box. You can choose from the following list of project types:

- Analog or Mixed / AD
- PC Board Wizard
- Programmable Logic Wizard
- Schematic (default)

However, after you create the project with the specific project type, you can use the Change Project Type command to change the project type.

When you use this command, the Select Project Type dialog box appears. This contains the name and location of the design. To change the project type, select a type from the Associate Project To option group.

To access this command, right-click on the design in the Project Manager and choose Change Project Type from the menu.

Note: The Select Project Type dialog box also appears if you open a design in Capture that does not have an associated project. You then select the project type and Capture creates the project file (.opj) of the specific project type.

Opening Containing Folder

You can use the Open Containing Folder command on the right-click menu of the Project Manager to open the file system folder that contains the selected project.

Working with schematic pages

This section covers:

- "Moving schematic pages between schematic folders" on page 139
- "Dragging and dropping folders and pages" on page 142
- "Renaming a schematic or part" on page 143
- "Attaching a schematic folder" on page 144
- "Opening a schematic page" on page 147
- "Defining schematic page characteristics" on page 147
- "Creating a multiple-page schematic folder" on page 149
- "Switching between open schematic pages" on page 149

Moving schematic pages between schematic folders

You use schematic folders to organize a design, grouping schematic pages in ways that make the most sense for your purposes. If you change your mind, you can easily transfer schematic pages from one schematic folder to another. You can also place copies of pages in several schematic folders.

If one of your projects has one or more schematic pages that solve a problem in a second project, you can transfer the pages from one project to another, or you can place copies in both projects. Because all schematic pages must be contained in a schematic folder, a schematic folder to hold the pages must exist in the second project before you can place the pages.

If you are working in one project and you want to use one or more schematic folders that are in another project, you can transfer schematic folders from one project to another, or you can create a copy for use in multiple projects. You cannot, however, move or copy a schematic folder into the design cache of any design.

If a document in a schematic folder is open in an editor, the document cannot be moved or copied.

To move schematic pages from one schematic folder to another

1. Verify that the pages are not open in the schematic page editor or the spreadsheet editor.
2. In the project manager, select the schematic pages you wish to move.
3. Choose *Edit – Cut*. If you wish to have a copy of the pages in both schematic folders, choose the Copy command.
4. Select the schematic folder that will hold the pages.
5. Choose *Edit – Paste*.

or

1. Verify that the pages are not open in the schematic page editor or the spreadsheet editor.
2. Select the schematic pages that you wish to move, then drag them to the appropriate schematic folder. If you wish to have a copy of the pages in both schematic folders, press and hold CTRL while you are dragging.

To move schematic pages from one project to another

1. Verify that the schematic pages are not open in the schematic page editor.
2. Open a project and select the schematic pages you wish to move.
3. Choose *Edit – Cut*. If you wish to have a copy of the pages in both projects, choose Copy.
4. Open the project in which you want to use the schematic pages.

5. Select the schematic folder that will hold the pages.
6. Choose *Edit – Paste*.
7. Choose *File – Save All*. Do this for both projects.

or

1. Verify that the schematic pages are not open in the schematic page editor.
2. Open both projects in their respective project managers.
3. Drag and resize the two project manager windows so that each is visible.
4. Select the schematic pages that you want to move, then drag them to the appropriate schematic folder in the second project manager window. If you want to have copies of the pages in both projects, press and hold CTRL while you are dragging the pages.
5. Choose *File – Save All*. Do this for both projects.

Note: If you copy or move a document from one design or library to another, you should save the destination design or library immediately. If you do not, you may lose data if you open the moved document in the schematic page editor or part editor and then close the editor without saving the document

Note: Deleting schematic folders, schematic pages, parts and symbols is permanent. You cannot use the Undo command to bring back deleted items from the project manager.

Note: If you move or copy a parent schematic folder or schematic page from one project into a second project, Capture remembers the name and directory of the file containing the child schematic folder or folders. This information is stored in the Attach Implementation dialog box for each hierarchical block and nonprimitive part.

To move a schematic folder from one project to another

1. Verify that no Capture editor is open on any document in the schematic folder.
2. In the project manager, select the schematic folder or folders you wish to move.

3. Choose *Edit – Cut*. If you want to have a copy of the schematic folder in both projects, choose Copy instead.
4. Open the project in which you want to paste the schematic folder or folders.
5. Select the filename.DSN folder, then from the Edit menu, choose Paste.
6. Choose *File – Save All*. Do this for both projects.

or

1. Verify that no Capture editor is open on any document in the schematic folder.
2. Open both projects in their respective project managers.
3. Drag and resize the two project manager windows so that each is visible.
4. Select the schematic folder or folders that you wish to move, then drag the schematic folder or folders to the filename.DSN folder in the second project manager window. If you wish to have a copy of the schematic folder in both projects, press and hold CTRL while you are dragging the folder.
5. From the File menu, choose Save All. Do this for both projects.

Dragging and dropping folders and pages

You can use the standard Windows drag-and-drop operation to move or copy Capture documents in the project manager windows. If you wish to copy rather than move, you press and hold the CTRL key while you drag the document.

If you drag a part that has a part alias, the part alias also moves. In the context of dragging and dropping, a symbol behaves just as a part does—as shown in the table below, a symbol can be dragged from a design or a library and dropped in another library.

A document that is open in an editor, or one that contains any open elements, cannot be dragged.

Documents can be dragged as indicated in the following table:

Drag from . . .	Part	Schematic Page	Schematic Folder
Design to design		X	X
Design to library	X	X	X
Schematic folder to schematic folder		X	
Library to design			X
Library to library	X		X

Note: If you copy or move a document from one design or library to another, you should save the destination design or library immediately. If you do not, you may lose data if you open the moved document in the schematic page editor or part editor and then close the editor without saving the document.

Renaming a schematic or part

In Capture, the windows in which you work have headings based upon the name of the open document. You can simplify your search through a set of open windows by not using identical names for several documents.

When you create a new part, symbol, schematic folder, schematic page, project, or library, you can specify a name or accept the unique name Capture assigns it.

To rename a schematic page, symbol, or part

1. In the project manager, select the document you wish to rename.
2. Choose *Design – Rename*.
3. In the dialog box that appears, enter the new name and click OK. The name change takes effect immediately.

To rename a schematic folder

1. In the project manager, select the schematic folder you wish to rename.
2. Choose *Design – Rename*.
3. In the dialog box that appears, enter the new name and click OK. The name change takes effect immediately.

To rename a design or library

1. Use the Windows Explorer to rename the design or library file.

To save a design or library under a different filename

1. Open the project manager window for the design or library.
2. Choose *File – Save As*.
3. Enter the new filename in the File Name text box, then click OK.

Note: Renaming a library in this manner breaks the links between the library and parts selected from it, so the Update Cache command does not work. Such libraries also are not listed in the CAPTURE.INI file for configuration.

Attaching a schematic folder

You attach a schematic folder to extend net connections between schematic folders. The attached schematic folder is the child schematic folder in a hierarchy.

A schematic folder can be attached to a nonprimitive library part, a nonprimitive part instance on a schematic page, or a hierarchical block.

To attach a schematic folder to a new hierarchical block

1. Open the schematic page editor on the parent page.
2. Choose *Place – Hierarchical Block*.
3. Assign a name to the hierarchical block.

4. In the Implementation Type drop-down list, select Schematic View.
5. In the Implementation Name text box, enter the name of the child schematic folder.
6. If the child schematic folder is not in the current design, specify the path and library where the schematic folder is located.
7. Click OK.

To attach a schematic folder to a new part

1. Create a new part.
2. Click the Attach Implementation button. The Attach Implementation dialog box appears.
3. In the Schematic text box, select Schematic View from the Type drop list box.
4. Specify the name of the child schematic folder in the Name text box.
5. If the child schematic folder is not in the current design, specify the path and library where the schematic folder is located.
6. Click OK twice.

To attach a schematic folder to an existing hierarchical block or part

1. Select the hierarchical block or part on the parent schematic page, and then choose Properties from the Edit menu. The property editor appears.
2. Click the Implementation Type property cell, and choose Schematic View from the drop-down list.
3. Click the Primitive property cell, and select No from the drop-down list. With this setting you can ascend and descend the hierarchy.
4. Enter a name in the Implementation property cell.

5. If the child schematic folder is not in the current design, specify the path and library where the schematic folder is located using the Browse button in the Implementation Path property cell.
6. Click Apply, and close the property editor.

It is recommended that, rather than editing parts in libraries provided by OrCAD, you copy the part and make the changes in a custom library. If you do edit a library provided by OrCAD, it is important that you assign a new library name (from the File menu, choose Save As) so that your changes are not overwritten when you update or upgrade your software.

Note: Be careful not to create recursion in your design. Capture cannot prevent recursion, and the Design Rules Check command does not report it.

Note: If you attach external schematic folders or other files to hierarchical blocks in a design or parts in a library, be sure to include the attachments when you pass the design or library to a board fabrication house or to another engineer. Attached schematic folder and other files are not carried along automatically when you copy or move a part, schematic folder, or schematic page to another library, design, or schematic folder. Only the “pointers” to the attached schematic folders and files—that is, their names and the names of the designs or libraries that contain them—are carried along.

Note: Attached files work much like their counterparts in mail—they do not provide an alternative definition of the part (as do attached schematic folders).

Note: If you attach a schematic folder to a homogeneous part, it is attached to each part in the package, not the package itself. You cannot attach a schematic folder to a heterogeneous part.

Note: When you attach a schematic to a part or a hierarchical block, you can specify a full path and filename in the Library text box. So, although you can specify a library that hasn’t been saved, you should not try to descend into the attached schematic folder until the library that contains the schematic folder has been saved.

Note: If you don’t specify a full path and filename in the Library text box, Capture expects to find the attached schematic folder in the same design as the part of the hierarchical block to which it is attached. If the specific schematic folder doesn’t exist in either the

design or library, Capture creates the schematic folder when you descend hierarchy on the part or hierarchical block.

Note: For compatibility with future versions of Windows, Capture preserves the case of the path and filename as you specify them in the Library text box.

Opening a schematic page

The only limit to the number of schematic pages you may have open is the resources available to your computer. When you open an existing schematic page, it initially occupies a single window. A new project occupies two windows initially.

To open an existing schematic page

1. Open the design that contains the schematic page, as described in Opening an existing Capture design.
2. In the project manager, double-click on the schematic folder to display the schematic pages.
3. Double-click on the schematic page. The schematic page opens in the schematic page editor.

To create a schematic page

1. In the project manager, select the schematic folder to which the new page belongs.
2. Choose *Design – New Schematic Page*.
3. Specify a name for the new schematic page, and click OK.

Note: In Capture, the windows in which you work have headings based upon the name of the open document.

Defining schematic page characteristics

Using the design template, you can establish schematic page characteristics for an entire project; you can also override these defaults and establish characteristics for a particular schematic page

using the Schematic Page Properties or Design Properties command.

Capture will create a schematic page size to suit your printer or plotter. You can choose from five standard page sizes or specify a custom size.

The default title block symbol, default title block information, border, and grid references can all be established for each project. Title block visibility can be specified for the entire project or for each schematic page.

To define grid references for new designs and schematic pages

1. Choose *Options – Design Template*, then choose the Grid Reference tab.
2. Make selections for the horizontal and vertical grid references and then click OK to dismiss the Design Template dialog box. Until you change the Grid Reference tab, any designs or schematic pages you create reflect these selections.

To change grid references for an existing page

1. Open the schematic page editor for the schematic page.
2. Choose *Options – Schematic Page Properties*, then choose the Grid Reference tab.
3. Make selections for the horizontal and vertical grid references and then click OK to dismiss the Schematic Page Properties dialog box. The selections are reflected in the active schematic page.

To define schematic page size for new designs and schematic pages

Choose *Options – Design Template*, then choose the Page Size tab.

Select Inches or Millimeters as your unit of measure.

Select a page size.

1. If you choose inches, the choices are A, B, C, D, E, and Custom.
2. If you choose millimeters, the choices are A4, A3, A2, A1, A0, and Custom.

Enter a value for pin-to-pin spacing, and click OK to dismiss the Design Template dialog box. Until you change the Page Size tab, any designs or schematic pages you create reflect these selections.

Creating a multiple-page schematic folder

1. In the project manager, select the project root.
2. Choose *Design – New Schematic*. The New Schematic dialog box.
3. Enter the name for the schematic folder and click OK. The schematic folder name is listed in the project manager.
4. Select the new schematic folder and from the Design menu, choose New Schematic Page. The New Page in Schematic dialog box appears.
5. Enter the name for the schematic page and click OK. The page name is listed below the schematic folder name.
6. Repeat steps 4 and 5 for each page of the schematic folder.
7. Place off-page connectors, hierarchical ports, hierarchical pins, and hierarchical blocks to establish connectivity between schematic pages.

Note: In Capture, the windows in which you work have headings based upon the name of the open document.

Switching between open schematic pages

1. Click anywhere on the schematic page editor window that holds the schematic page.

or

1. Choose the name of the schematic page from the Window menu.

or

1. Double-click on the page in the project manager.

Closing a project

When the project manager window is active, you can close a project without quitting Capture, or you can close and save your project as you quit.

To close a project

1. From the project manager's File menu, choose Close Project.

   When you close a project, a dialog box displays, asking if you want to save your changes.

3

Opening and developing part libraries

This chapter covers:

- "Adding a library to your project" on page 152
- "Creating a library" on page 153
- "Opening a library" on page 155
- "Editing a library" on page 157
- "Closing and saving a library" on page 208

A library is a file that stores parts, symbols, title blocks, schematic folders or schematic pages. Capture provides more than 80 libraries; in addition, you can create additional custom libraries. If you edit a library provided by Capture, you should give it a custom name so that you will not copy over your changes when you receive updated libraries.

You can, for example, create a library to hold all your programmable logic device, or to hold schematic folders that you use often. There is no need to create a library for a particular project, because the design cache holds all the parts and symbols used in the project.

Note: Schematic folders and schematic pages cannot be created in a library, but can be copied or moved to a library from a project. Schematic folders and schematic pages can also be edited in a library.

Because a library is a file, you can work with it in the Windows File Manager as well as in Capture.

It is recommended that, rather than editing parts in libraries provided by OrCAD, you copy the part and make the changes in a custom library. If you do edit a library provided by OrCAD, it is important that

you assign a new library name (from the File menu, choose Save As) so that your changes are not overwritten when you update or upgrade your software.

Note: When you save a project, Capture automatically creates a backup with a .DBK file extension. When you save a library, Capture automatically creates a backup with a .OBK file extension. If you save only a schematic page or a part, no backup is generated.

Note: If you move a library after you place a part, the connection between the part and its library is broken. In this case, the Update Cache command will not find the library; you'll need to use the Replace Cache command and specify the new path to the library.

Adding a library to your project

When you add a library to your project, you make all the parts contained therein available for placement on schematic pages.

To add an existing library to your project

1. From the File menu, choose Open. The Open dialog box appears.
2. Select the library you wish to open. If the library file is not listed, do one or more of the following:
   - ❑ In the Look in drop list box, select a new drive, a new directory, or both.
   - ❑ In the Files of type box, select the type of file you wish to open.
3. Choose the Open button. The project manager window opens; the library parts appear in the project manager.

Note: If you open an SDT library, Capture prompts you to save the library.

To add a recently-used library to your project

➤ From the File menu, choose the name of the library you want to add.

Note: If you edit a library provided by OrCAD, it is important that you assign a new library name so that your changes are not overwritten when you upgrade or update your software.

Note: If you move a library after you place a part, the connection between the part and its library is broken. In this case, the Update Cache command will not find the library; you'll need to use the Replace Cache command and specify the new path to the library.

Creating a library

Libraries store parts, symbols, custom title blocks, as well as schematic folders and the schematic pages contained in them. With Capture, you can have as many libraries as you wish to suit any purpose, and you can specify the name and storage location of your library. Each library is available to each project.

Library size is limited only by the amount of space on your system's hard disk; however large libraries take longer to load. If speed becomes an issue, consider creating several smaller libraries, instead.

Note: Schematic folders and schematic pages cannot be created in a library, but can be copied or moved to a library from a project. Schematic folders and schematic pages can also be edited in a library.

Populating a new library

When you create a new library, the project manager adds it to the project, but it is empty. To populate the library, you can create your own parts, or you can move or copy parts from another library. See Moving parts or symbols between libraries for details.

To create a new library from the project manager

1. From the File menu point to New, then select Library. Capture adds a Library folder and a Library Cache folder to the project.
2. Name the new library by right-clicking on the new library icon and saving it with the file name and location you want.

3. Populate the library by moving or copying files from other libraries. See Moving parts or symbols between libraries for details.

To create a new library

➤ From the File menu, choose the New command, select Capture Library, and click OK. If you have a project manager window currently open at the time, Capture adds the library to the project. Otherwise, Capture creates a new project for the library.

To rename a library

1. In the project manager, select the library.
2. From the File menu, choose Save As.
3. Enter a name in the File Name text box. OLB is the recommended extension for library files.
4. Click OK to return to the project manager.

or

➤ Use the Windows Explorer.

To specify the storage location for a library

1. In the project manager, select the library.
2. From the File menu, choose the Save As command.
3. Select the drive and directory in which you want to store the library.
4. Click OK to return to the project manager.

Note: In Capture, the windows in which you work have headings based upon the name of the open document.

Note: If you move a library after you place a part, the connection between the part and its library is broken. In this case, the Update Cache command will not find the library; you'll need to use the Replace Cache command and specify the new path to the library.

Opening a library

When you open a library, you make its contents available for editing with the part editor.

To open a library

1. From the File menu, choose Open. The Open dialog box appears.
2. Select the library you wish to open. If the library file is not listed, do one or more of the following:
3. In the Look in drop list box, select a new drive, a new directory, or both.
4. In the Files of type box, select the type of file you wish to open.
5. Choose the Open button. The project manager window opens; the library parts appear in the project manager.

Note: If you open an SDT library, Capture prompts you to save the library.

To open a recently used library

Note: If you open an SDT library, Capture prompts you to save the library.

➤ From the File menu, choose the name of the library you want to open.

Note: If you edit a library provided by OrCAD, it is important that you assign a new library name so that your changes are not overwritten when you upgrade or update your software.

Note: If you move a library after you place a part, the connection between the part and its library is broken. In this case, the Update Cache command will not find the library; you'll need to use the Replace Cache command and specify the new path to the library.

Shortcut

Tool palette:

Creating a library with sheetpath parts

Once you have set up your design, follow these guidelines for processing it:

- Set your design's part primitivity to default on the Hierarchy tab of the Design Properties dialog box when updating part references. This prevents Capture from annotating the schematic folders stored in your library.
- Set your design's part primitivity to nonprimitive on the Hierarchy tab of the Design Properties dialog box when you create a netlist. This allows Capture to descend the hierarchy into the schematic folders stored in your library.

When you translate a design from SDT to Capture, any sheetpath parts become non-primitive parts that descend into another schematic folder. This schematic folder is also contained in the Capture design. When you translate an SDT library with references to other schematics, Capture translates these schematics and stores them in the library.

You can set up your Capture design to act similar in regards to sheetpath parts.

Note: Before you translate an SDT library containing sheetpath parts, the SDT.CFG file must be present in the directory where translated library will be saved.

The PLIB line in SDT.CFG should contain the valid path where the source libraries are present.

Note: Capture cannot translated compressed SDT files. You need to decompress all compressed SDT files.

To set up a design to emulate sheetpath part behavior

1. Translate the SDT design.
2. Translate the SDT library that contains the sheetpath parts.
3. In the design, remove all schematic folders that correspond to the sheetpath part schematics.

4. Open the schematic pages with the translated sheetpath parts, and select all of these parts.
5. From the Edit menu, choose the Properties command. The property editor appears.
6. Click in the Implementation Path field for one of the parts.
7. Enter the name and path of the library containing the schematic folder emulating the sheetpath part.
8. Click the Apply button.
9. Select another part, and repeat steps 6 through 8 until all of the necessary parts have attached schematic folders.

Editing a library

This section covers:

- "Populating a new library" on page 153
- "Creating parts and assigning properties" on page 157
- "Moving parts or symbols between libraries" on page 200
- "Updating part properties in a library" on page 201
- "Copying a schematic page to a library" on page 202
- "Copying a schematic folder to or from a library" on page 204
- "Copying a part from the design cache to a library" on page 207

Editing a part library includes assigning properties and, perhaps, assigning schematic pages as part definitions. There are also a number of considerations involved when moving or copying parts to and from libraries and setting the design cache for your project.

Creating parts and assigning properties

This section covers:

- "Defining heterogeneous and homogeneous parts" on page 159
- "Creating a part body" on page 160

- "Creating a part convert" on page 174
- "Creating a part alias" on page 175
- "Creating a new part from spreadsheet" on page 176
- "Assigning properties to the part" on page 180
- "Creating a package" on page 189
- "Editing parts in a library" on page 197

In Capture, you can create a part and add it to a new or existing library. The part may be a single part or a multiple-part package. It can contain graphics, which must be inside the part body border, as well as IEEE symbols and text, which can be either inside or outside the part body border. For any part that you create, you can also create a part convert.

Creating a part involves three processes: defining the part in the Part Properties dialog box (including defining the part package as either heterogeneous or homogeneous), defining the part body, and placing pins on the part body.

Note: If you edit a library provided by OrCAD, it is important that you assign a new library name so that your changes are not overwritten when you upgrade or update your software.

Note: Deleting schematic folder, schematic pages, parts, and symbols is permanent. You cannot use the Undo command to bring back deleted items from the project manager.

Note: The size of a part or a symbol is limited to 32 by 32 inches.

Note: When you save a project, Capture automatically creates a backup with a .DBK file extension. When you save a library, Capture automatically creates a backup with a .OBK file extension. If you save only a schematic page or a part, no backup is generated.

Note: You can use an existing part as a model for a new part by moving a copy of the part to a second library and then editing the copy. If you wish to have the new part in the original library, rename the new part, then move it to the original library.

Note: In Capture, the windows in which you work have headings based upon the name of the open document.

Note: If you move a library after you place a part, the connection between the part and its library is broken. In this case, the Update Cache command will not find the library; you'll need to use the Replace Cache command and specify the new path to the library.

Defining heterogeneous and homogeneous parts

Parts usually correspond to physical objects—gates, chips, connectors, and so on—that come in packages of one or more parts. Think of these packages as physical parts and the parts you place on a schematic page as logical parts. Physical parts that comprise more than one logical part are sometimes referred to as multiple-part packages. For simplicity, Capture usually refers to both as parts.

Logical parts in a package may have different pin assignments, graphics, and user properties. If all the logical parts in a package are identical except for the pin names and numbers, the package is homogeneous. If the logical parts in a package have different graphics, numbers of pins, or properties, the package is heterogeneous. For example, a hex inverter is homogeneous: the six inverters are identical, except for their pin numbers. A relay, which has a normally opened switch, a normally closed switch, and a coil, is heterogeneous: the three physical parts differ in graphics, number of pins, and properties.

To create a heterogeneous part in a library, open the library and choose New Part from the Design menu. Enter the part name, set the number of parts in the package, and select Heterogeneous in the Package Type group box. Enter the PCB Footprint if you wish to assign one to the part at this time. Click the OK button, and Capture will give you the logical part with reference designator U?A. Draw your part body, add your pins. To get to the B package choose Next Part from the View menu, or press CTRL+N. Capture displays the U?B part for you to edit. Again, draw your part body and add your pins. Repeat this process until all your logical parts are created.

After creating the logical parts of your heterogeneous part in the library you need to assign a unique property to each one. For example, create a property named PACKAGE.

Note: Do not use GROUP as the name for this property. This may cause problems while annotating your design for a PCB Editor tool, like Allegro PCB Editor. The GROUP property is used in PCB Editor for a specific purpose.

To create this property do this, double-click on the empty space beside the logical part to get the User Properties dialog box. Choose the New button, type in PACKAGE into the Property box and a 1 in the Value box. Click twice to attach that property to the logical part. Add this new property to each logical part in your package (part A, B, C, and so forth). Save your library with the new part in it.

Open your schematic and place the A, B, C (and so on) logical parts of your heterogeneous parts appropriately in your design. After you place each logical part, double-click on the part to get the property editor. Edit the value of the PACKAGE property shown in the spreadsheet. Leave the Value of 1 on that property for each logical part of the first set you place; assign a Value of 2 to each logical part in the second set, assign a Value of 3 to each logical part in the third set, and so on. Capture uses this value to group the heterogeneous parts correctly when assigning reference designators.

When you get ready to annotate the design you add that property name to the combined property string in the Annotate dialog box. Capture will use this property and the assigned values to annotate the parts correctly in the design. To do this, go to the project manager window, select the design name, and choose Annotate from the Tools menu. Select Update entire design, select Unconditional reference update (select Incremental if you have already partially annotated your design), and type in {PACKAGE} into the Combined property string box. This gives you a combined property string like {Value}{Source Package}{PACKAGE}. When you click OK, Capture then assigns the appropriate reference designators to all your parts in the design including the heterogeneous parts.

Note: Do not manually change the reference designators of heterogeneous parts for a complex hierarchical design. In case you want to change the reference designator for a part placed in the schematic page, delete it, and add it again. This way all the occurrences will get updated correctly.

Creating a part body

This section gives you an overview of creating a part body, then how:

- "To connect a pin to a non-rectangular part body" on page 168
- "To change the snap-to-grid option" on page 169

- "To set a default line style" on page 169
- "To define a default fill" on page 169
- "To edit line style or fill style of a placed object" on page 169
- "To draw an object" on page 170
- "To place a pin" on page 170
- "To place an array of pins" on page 172
- "To add comment text to a part or a schematic page" on page 173
- "To edit text display properties" on page 174

When you create a new part, the part editor opens with an empty, rectangular part outline (the part body border) visible. The part body border expands to accommodate the graphic elements of the part body, and pins are constrained to the part body border.

If you want to change the size or shape of the part body border, you can select the border and drag the selection handles until the part body border appears as you want it.

Pins, when you place them, are constrained to the part body border. If the edge of the part body coincides with this border, the pins are directly attached to the part body, but if the part body is inside this border, you must draw a line from the pin to the part body. You may place individual pins, or you may place an array of pins.

You define the part body using the tools available on the tool palette. All of these tools are also available on the Place menu. Using the Selection tool, you can select a placed object for editing.

Note: You can draw part bodies thicker than pins and the rest of the part by adjusting the line style for the graphic objects you want to be thicker.

When you place a pin, you can describe it completely. To place pins, you need to be in the Part view of the part editor.

If you want to place several identical pins that are not sequentially numbered on the part body border, the Pin tool is ideal. See Placing an array of pins if you wish to create multiple identical pins that are numbered sequentially on the part body border.

When you place a pin in one view (normal or convert), Capture places an identical pin in the other view to prevent the parts from getting out of sync. The same is true about deleting pins. Changing the name of a pin in one view doesn't cause the name to change in the other. However, if you change a pin number in one view, Capture changes the pin number in the other view so the two views stay in sync.

If the part you are creating includes a series of pins that vary only in pin number, placing a pin array is very convenient. A pin array is defined by a single set of electrical characteristics. If you wish to create multiple pins with identical properties and place them so that the pin numbers and names are sequentially arranged on the part body border, this tool is ideal.

Both homogeneous and heterogeneous parts may have shared pins. A common use of shared pins is for supply (power or ground) pins, which are referred to in Capture as "power pins."

On heterogeneous parts, power pins can be visible on every part in the package. If the pins are visible, they must be placed on at least one part in the package, and that part must be placed in the design for the power connections to appear in the netlist. Invisible power pin types must also be in a part that is placed in the design for them to appear in a netlist.

On homogeneous parts, power pins appear on every part in the package. The pin names are filled in automatically, but you must specify the pin numbers. For the pins to be shared, verify that both the pin names and pin numbers are the same for every part in the package.

Note: If you place the same pin on multiple parts in a package, you can inadvertently short two nets. Use caution to avoid this problem, and always run Design Rules Check before creating a netlist.

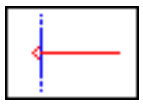
Note: Pin names are shared, but pin numbers are not.

You may have comment text, in the font of your choice, on a schematic page or a part. Use the text tool to document your schematic folder or to place the logic definition for a programmable logic device.

At certain zoom scales, Capture substitutes filled rectangles for text that is too small to appear. These placeholders are for display only—the text prints correctly.

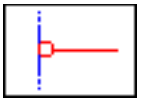
System-Defined Pin shapes

Capture provides a list of system-defined pin shapes that you can use when you create a new part or edit the pins shapes on an existing part.



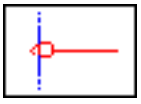
Clock

Clock symbol



Dot

Inversion bubble



Dot-Clock

Clock symbol with inversion bubble.

Line

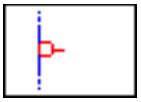
Normal pin with lead three grid units in length.

Short

Normal pin with lead one grid unit in length.

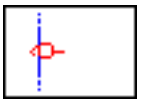
Short Clock

Clock symbol with lead one grid unit in length.



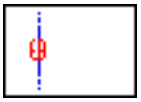
Short Dot

Inversion bubble with lead one grid unit in length.



Short Dot-Clock

Clock symbol with inversion bubble with lead one grid unit in length.



Zero length

Normal pin with lead zero grid units in length.

User-Defined Pin Shapes

You can create your own pin shapes in Capture. You can then use these pin shapes on new or existing parts.

To create a pin shape

1. Open the CAPSYM.OLB library from the following installation path: %CDSROOT%\tools\capture\library\capsym.olb.

   (see Opening a library)

2. Select the library (capsym.olb) in the Project manager and choose Design - New Symbol.

   Alternatively, you can right-click on the library (.olb) and choose New Symbol from the shortcut menu.

3. Enter a name for the new pin shape.

Note: A symbol name length cannot exceed 31 characters.

4. Choose the Pin Shape option in the Symbol type group and click OK.

   The Part Editor page opens with an empty rectangle defining the boundary of the pin shape.

5. Draw the pin shape using the available shapes on the Draw toolbar.

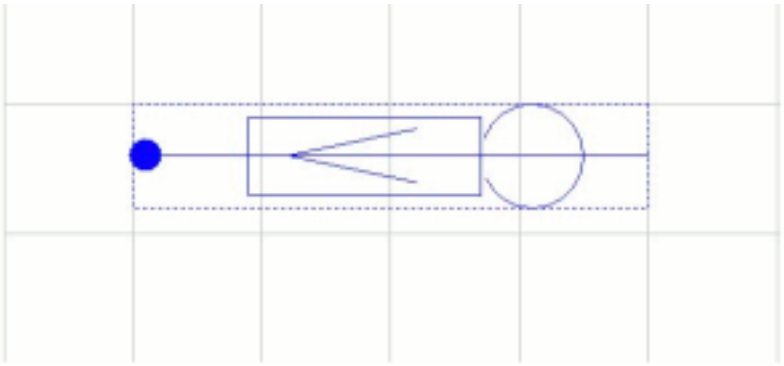
   The new pin shape is now available in the selected library.

   You can now use this pin shape by placing it on a part (see To place a pin).

Important

Please note the following when **Creating User-Defined pin shapes**:

- You can choose Line, arc, polyline, bezier curve, Rectangle, ellipse, Elliptical arc shapes to create user-defined pin shape around a dot connection point.



- The bounding box of the pin shape determines the length of the pin. If the bounding box does not completely enclose the graphics then you may see your pin offset from the boundary of the symbol. For correct adjustment, ensure the bounding box completely encloses the graphics.
- The Capture Part and Schematic Page editors require a dot connection point to be on the grid so for the pin start point to touch the body of the symbol, you must keep the end points on the grid.
- You should not draw objects enclosing the dot connection point. That may not show the pin shape correctly on the Capture Part and Schematic Page editor.
- IEEE symbols and pictures are not supported in user-defined pin shapes.

Important

Please note the following when **Adding User-Defined pin shapes** to parts in your designs:

- To place a user-defined pin shape on a part, the pin shape must be available in the CAPSYM.OLB library in the path %CDSROOT%\tools\capture\library\capsym.olb.

  If create your pin shape in a user-defined library, you need to copy that symbol into the CAPSYM.OLB library.

  Capture reads the user-defined pin shapes from the above location and populates the pin shape names in the Shape cell of the Pin Properties dialog in Part Editor.

- If you place a new part in a design which has pin shapes assigned to pins, Capture will search for the pin shapes in the CAPSYM.OLB library. When the part is placed on the design and the pin shapes are found in CAPSYM.OLB library, the pin shapes are cached to the design cache. Once you save the design, the pin-shapes will be read from design cache.

- If a pin shape is not available in the CAPSYM.OLB library the default pin shape, that is a line, will display on the part.

- If you down-grade a design containing user-defined pin shapes from any Capture version greater than 16.2 to 16.2 or any previous version, the user-defined pin shapes will be removed from the design cache. You can still open the design in 16.2 but the pins will show with default pin shape, line. However, if you open this 16.2 design in any version greater than 16.2 again, Capture will seach the CAPSYM.OLB library for the user-defined pin shapes used in the design. The pin shapes found in the library will display on the schematic. For pin shapes not found in the library, the default, line shape, will display.

- If you run the Replace cache command on a user-defined pin shape say A with B in the design, all instances of the user-defined pin shape A will be replaced with B in the design and Pin Shape property on the pins will be updated to new the pin shape value. This property is an instance override. At any time, if you want to revert to the library level pin shape value, you can use Delete property in the

Property editor and it will delete the instance override and the same will be reflected on the schematic. However, if you do an Edit part, then it will still show the part level user-defined pin shape and not the instance override that exists in the schematic.

Pin types

3 State	A 3-state pin has three possible states: low, high, and high impedance. When it's in its high impedance state, a 3-state pin looks like an open circuit. For example, the 74LS373 latch has 3-state pins.
Bidirectional	A bidirectional pin is either an input or an output. For example, pin 2 on the 74LS245 bus transceiver is a bidirectional pin. The value at pin 1 (an input) determines the active type of pin 2, as well as others.
Input	An input pin is one to which you apply a signal. For example, pins 1 and 2 on the 74LS00 NAND gate are input pins.
Open Collector	An open collector gate omits the collector pull-up. Use an open collector to make "wired-OR" connections between the collectors of several gates and to connect with a single pull-up resistor. For example, pin 1 on the 74LS01 NAND gate is an open collector gate.
Open Emitter	An open emitter gate omits the emitter pull-down. The proper resistance is added externally. ECL logic uses an open emitter gate and is analogous to an open collector gate. For example, the MC10100 has an open emitter gate.

Output	An output pin is one to which the part applies a signal. For example, pin 3 on the 74LS00 NAND gate is an output.
Passive	A passive pin is typically connected to a passive device. A passive device does not have a source of energy. For example, a resistor lead is a passive pin.
Power	A power pin expects either a supply voltage or ground. For example, on the 74LS00 NAND gate, pin 14 is VCC and pin 7 is GND. It is not a good idea to use overbars above power pin names; if you do, any netlists that you create will have invalid power pin names. Power pins are invisible.

Before you begin drawing, you may want to specify default line and fill styles because all lines and shapes you draw adopt the current line style and closed shapes adopt the current fill style. You can use a variety of line types or fill styles for any schematic page or part.

To connect a pin to a non-rectangular part body

1. Place the pin on the part body border.
2. From the Options menu, choose Preferences, then choose the Grid Display tab.
3. In the Part and Symbol Editor group box, disable the Cursor Snap to Grid option, then click OK.
4. Draw a line between the pin and the part body.
5. If the line does not look like the pin, edit the line's style and width.
6. From the Options menu, choose Preferences, then choose the Grid Display tab.
7. In the Part and Symbol Editor group box, enable the Cursor Snap to Grid option, then click OK.

Note: If you edit a library provided by OrCAD, it is important that you assign a new library name so that your changes are not overwritten when you upgrade or update your software.

Note: The size of a part or a symbol is limited to 32 by 32 inches.

To change the snap-to-grid option

➤ From the Options menu, choose the Preferences command, then choose the Grid Reference tab. You set the option separately for the schematic page editor and the part editor.

To set a default line style

1. From the Options menu, choose the Preferences command and then choose the Miscellaneous tab.
2. Click on the Line Style and Width drop box to display the options. Note that you can specify separate options for the schematic page editor and the part editor.
3. Select one of the options and click OK. Any lines or shapes you draw will have this line style.

To define a default fill

1. From the Options menu, choose the Preferences command and then choose the Miscellaneous tab.
2. Click on the Fill Style drop-down list to display the options. Note that you can specify separate options for the schematic page editor and the part editor.
3. Select one of the options and click OK. Any closed shapes you draw will have this fill style.

To edit line style or fill style of a placed object

1. Select the object.
2. From the Edit menu, choose the Properties command.
3. Select another line style or fill style in the dialog box that appears, then click OK.

To draw an object

1. From the Place menu, choose the appropriate drawing command or select the appropriate drawing tool from the tool palette.
2. Use the mouse to draw the object. To constrain the object by the orthogonality rules, press and hold the SHIFT key while you draw.

To place a pin

1. Verify that you are in the part view of the part editor.
2. From the Place menu, choose Pin. The Place Pin dialog box appears.
3. Edit the values as necessary.

   Name The name can be up to 128 characters long and may include any character. If you place multiple copies of the pin and the name ends with a numeric component, that final numeric component increments by one with each successive pin you place.

Note: If you are using Capture design with PCB Editor, make sure that the pin names do not exceed 255 characters.

Number The number can be up to 128 characters long and may include any character. If you place multiple copies of the pin and the number ends with a numeric component, the final numeric component increments by one with each successive pin you place.

Shape Select one; the choices are CLOCK, DOT, DOT CLOCK, LINE, SHORT, SHORT CLOCK, SHORT DOT, SHORT DOT CLOCKand ZERO LENGTH. If you select a pin type of POWER, the pin shape automatically is set to ZERO LENGTH.

Note: You can also specify a user-defined pin shape if the pin shape is available in the CAPSYM.OLB library

Type Select one; the choices are 3STATE, BIDIRECTIONAL, INPUT, OPEN COLLECTOR, OPEN EMITTER, OUTPUT, PASSIVE, and POWER. The Design Rules Check tool uses pin type to check electrical rules.

Width Select Scalar or Bus. If you choose Bus, the pin name must be of the form basename[m..n] where m..n specifies a range of decimal integers representing the number of bus members. For more information see Bus naming conventions.

Visibility If you are placing a power pin, you can select the Pin Visible box to cause the pin to cancel the pin's global attribute. This is useful if you want to create an isolated power net. If a power pin is visible, it must be connected to a wire. For more information see About power and ground pins or Isolating power or ground.

Note: Some netlist formats do not accept certain characters in pin names. See the description for the netlist format you want to use.

4. When you have completely defined the pin, click OK. The pin appears attached to the periphery of the part.
5. Use the mouse to move the pin to its intended location and click the left mouse button to place it. The pin appears in the selection color until you move the pointer.
6. If you want to place additional pins, repeat step 5. As you place successive pins, any final numeric component of the pin name or pin number increases by one. If you need to edit pin properties, leave the pin selected, then from the Edit menu choose Properties, make the changes in the Pin Properties dialog box, then click OK.
7. When your pins are placed, select the selection tool, or press ESC to dismiss the pin tool.
8. If the part body does not coincide with the part body border, draw a line from the pin's connection point to the part body. You may need to temporarily turn off the Snap to grid option (Options menu, Preferences command, Grid Display tab) while you draw the line.

Note: If you want an overbar over a signal name, follow each character in the name with a backslash (\).

Note: You can edit every pin in the package using the Package Properties spreadsheet editor. For more information, see Using the spreadsheet editor.

Note: You may want to use the Pin Array tool for placing large numbers of pins even though the properties or pin numbers vary. After placing the pins, you can select those you want to change, then from the Edit menu, choose Properties; this brings up the spreadsheet editor in which you can edit the properties of many pins.

Note: You cannot move pin names or pin number text when you are creating or editing a part, but you can make all the pin names on a part invisible. In the part editor, double-click within the part editor, but not on any graphic element, to bring up the Edit Part dialog box. Change Pin Names Visible from True to False.

Shortcut

Tool palette:

To place an array of pins

1. Verify that you are in the Part view of the part editor.
2. From the Place menu, choose Pin Array. The Place Pin Array dialog box appears.
3. Edit the values as necessary.

   Starting name The starting name can be up to 128 characters long and may include any character. The leftmost or upper pin of the array is assigned the starting name. If the starting name ends with a numeric component, that component increments by the increment amount from top to bottom and from left to right.

   Starting number The starting number can be up to 128 characters long and may include any character. The leftmost or upper pin of the array is assigned the starting number. If the final component of the starting number is numeric, the pin numbers change by the increment amount from top to bottom and from left to right

   Number of pins An integer

   Increment A positive or negative integer. Pin names and pin numbers that end with a numeric component are affected by the increment value. The numeric portion of the pin name or pin number changes by this amount from top to bottom or from left to right.

Pin spacing A positive value. The distance between the pins is measured in grid units.

Shape Select one; the choices are CLOCK, DOT, DOT CLOCK, LINE, SHORT, ZERO LENGTH. If you select a pin type of POWER, the pin shape automatically is set to ZERO LENGTH.

Type Select one; the choices are 3STATE, BIDIRECTIONAL, INPUT, OPEN COLLECTOR, OPEN EMITTER, OUTPUT, PASSIVE, POWER. Pin type is used by the Design Rules Check tool to check electrical rules.

Note: Some netlist formats do not accept certain characters in pin names. See the description for the netlist format you want to use.

4. When you have completely defined the array, click OK. The array is attached to the periphery of the part; the part body border automatically increases in size if necessary.
5. Use the mouse to move the array to its intended location and click the left mouse button to place it. The array appears in the selection color until you move the pointer.
6. Select the selection tool to dismiss the pin tool.
7. If the part body does not coincide with the part body border, draw a line from the pins' connection points to the part body. You may need to temporarily turn off the Snap to grid option (Options menu, Preferences command, Grid Display tab) while you draw the lines.

Shortcut

Tool palette:

To add comment text to a part or a schematic page

1. From the Place menu, choose Text.
2. Enter the text in the dialog box that appears.
3. Complete the dialog box selections; you can specify the font, color, or rotation.

4. Click OK to dismiss the dialog box. A rectangle representing the text is attached to the pointer.
5. Use the mouse to move the text. Click the left mouse button to place the text at the desired location.

Note: You can place multiple copies of the text. Just click the left mouse button at each location where you would like text. When you are through placing text, select the selection tool or press ESC.

Note: You can create multiple lines within a text object by pressing CTRL+ENTER to create the new line. This is useful for creating piped PLD commands without having to place multiple lines of text. Piped SPICE commands must be placed as separately placed lines of text.

Shortcut

Tool palette:

To edit text display properties

1. Select the text.
2. From the Edit menu, choose the Properties command.
3. In the dialog box that appears, change the font, color, or rotation, then click OK.

Shortcut

Mouse: Double-click the text you wish to edit.

Creating a part convert

You can store a part convert with a library part, then place either the normal view of the part or its convert.

To add a convert while you are creating a part

1. From the Design menu of the library's project manager window, choose New Part. The Part Properties dialog box appears.

2. In the Edit Part Properties dialog box, enable Create Convert View.
3. Fill out the rest of the dialog box and click OK. For more information, see Creating a part.
4. From View menu, choose the Convert command.
5. Use the part editor to Define the equivalent part and add the pins.
6. From the View menu, choose Package to see the convert.
7. From the File menu, choose Save.

To view a part convert

➤ From the part editor's View menu, choose Convert.

If you place the regular view of a part and you need to use the convert view instead, you can use the Graphic property in the property editor to change the view.

Creating a part alias

A part may come with several speed ratings or be made by several manufacturers. If all the variations have a common graphic and PCB footprint, you don't have to take the time and space to create and store a different library part for each variation. Instead, create a single library part and assign it multiple aliases.

To create or add a part alias

➤ From the project manager's Design menu, choose the New Part command.

or

1. From the part editor's Options menu, in package view, choose the Package Properties command.
2. Choose the Part Aliases button, then choose the New button.
3. Enter the new part alias in the Name text box, then click OK.

4. Click OK as needed to dismiss the remaining open dialog boxes.

Creating a new part from spreadsheet

You can use the New Part Creation Spreadsheet to create new parts (multi-section/single-section). The New Part Creation Spreadsheet has a spreadsheet-like interface that allows you to paste contents copied from a part data sheet to the spreadsheet.

Each row in the New Part Creation Spreadsheet corresponds to a pin while each column corresponds to properties associated with the pins. The property names are listed as the column header.

Note: Before you copy and paste part information (*pin number*, *pin name*, *pin type*, and so on) from a data sheet, make sure that you arrange the part information in the same column header format/sequence as it appears in the New Part Creation Spreadsheet.

To create a new part from spreadsheet

1. Select a library (.OLB) file that will contain the new part in the project manager.
2. Select the Design menu and choose the New Part from Spreadsheet command.

   or

   Right-click on the library file and select New Part from Spreadsheet from the pop-up menu.

   The New Part Creation Spreadsheet appears.
3. Specify a name for the new part in the Part Name text box.
4. If you want to create a multi-section part, specify the number of sections you want to have in your new part in the No. of Sections text box. The New Part Creation Spreadsheet creates single-section parts, by default.

   Note: The Section property column changes to a list box displaying the number of sections you specified in the No. of Sections text box.

Number of sections cannot be less than one.

5. Specify a part reference prefix for the part in the Part Ref Prefix text box.

6. Select Numeric or Alphabetic in the Part Numbering group. If you select Alphabetic, an alphabet (between A to Z) will be added as a suffix to the current part reference for each of the new parts. If you select Numeric, a number (between 1 and 1024) will be added as a suffix to the current part reference for each of the new parts.

   The Section property column changes based on your selection in the Part Numbering group. For example, if Alphabetic is selected, the Section property column displays “A”.

7. Specify a pin number in the Number property column.

To sort on any property, double-click its name in the column header.

8. Specify a name for the pin in the Name property column.

9. Select the type of pin from the Type property column list box.

You can select the Type cells for multiple pins simultaneously using the SHIFT+Down Arrow keys and then enter the pin type. The selected Type cells get populated with the pin type of your choice. Alternatively, you can:

- Select the Type cells for multiple pins simultaneously using the SHIFT+Left mouse button click, then press the CTRL key, and then select a pin type of your choice from the list box. The selected Type cells get populated with the pin type of your choice.
- Click the first cell of the range, and then drag to the last cell, and then enter the pin type of your choice. The selected Type cells get populated with the pin type of your choice.

(You can use these methods to make selection in the Shape, Position, and Section property column list boxes also).

10. Select a shape for the pin from the Shape property column list box.

Tip

You can hide or unhide a property column in the New Part Creation Spreadsheet. To do this, right-click the property column header you want to hide and select Hide from the pop-up menu. The selected property column will not appear now. To unhide a property column, right-click the property column header next on the right-hand side of the hidden property column and select Unhide from the pop-up menu. The hidden property column appears in the New Part Creation Spreadsheet. Alternatively, you can unhide a property column by:

- Double-clicking the column handle ( ) of the property column header.
- Dragging the column handle of the property column header.

(only the last two methods can be used to unhide a property column, which is the last column in the New Part Creation Spreadsheet).

Tip

You can change the order in which the property columns and rows appear in the New Part Creation Spreadsheet. To do this, select the property column/row header you want to move and drag and drop it to the location where you want it in the New Part Creation Spreadsheet.

11. Specify a value for a swappable (input) pin of the part in PinGroup text box.

12. Select the position where you want this pin to appear in the part for the Position property column list box.

13. Select a section number you want to associate with the pin from the Section property column list box.

Tip

You can select Section cells for multiple pins simultaneously using the SHIFT+Down Arrow keys and enter the section number. Alternatively, you can:

- Select the Section cells for multiple pins simultaneously using the SHIFT+Left mouse button click, then press the CTRL key, and then select a section number of your choice from the list box. The selected Section cells get populated with the section number of your choice.
- Click the first cell of the range, and then drag to the last cell, and then enter the section number of your choice. The selected Section cells get populated with the section number of your choice.

Tip

You can select alternate Section cells for multiple pins simultaneously using the CTRL+Left mouse button click and enter the section number.

Note: The order in which the pins appear in the spreadsheet, the pins will be added in the same order in the new part.

14. Click the Save button to save the new part. If any warnings are generated during the save operation, a message box appears asking you whether you want to view the warnings. If you want to view the warnings, click the View Warnings button. The New Part Creation Spreadsheet expands and displays a grid showing warnings messages. If you select the Continue button, the part is saved as is.

Note: Click the Hide Warnings button to hide the warning messages or Show Warnings button to display the warning messages again.

Note: If the new part you created contains one part per package then the part created would be homogeneous otherwise the part will be heterogeneous.

To add a pin

1. From the New Part Creation Spreadsheet, click the Add Pins button. The Add Pins dialog box appears.
2. Specify the number of pins you want to add in the Number of Pins text box.
3. Click OK. The desired number of blank rows gets added at the end of the current row set in the New Part Creation Spreadsheet.

To delete a pin

1. Select a row in the New Part Creation Spreadsheet.
2. Click the Delete Pins button. A message box appears asking you to confirm the deletion.
3. Click OK to confirm deletion. The selected row is deleted from the New Part Creation Spreadsheet.

Assigning properties to the part

This section covers:

- "Assigning a pin name or number" on page 181
- "Assigning a reference designator" on page 181
- "Editing part properties" on page 182
- "Assigning other properties" on page 182
- "Moving pin name and pin number text" on page 186

When you need to edit the properties of individual parts, follow the instructions below; when you need to edit properties for several parts, you can save time by using the spreadsheet editor, the Update Properties command or the Export Properties command.

Once you've added properties to a part on a schematic page, its properties no longer match the properties of the same part residing in the library. This part is unique in that it has properties assigned specifically to it that are not inherited from the library part definition.

If you add a user-defined property to one part in a homogeneous multiple-part package, all parts in the package inherit the property and its value. If you add a user-defined property to one part in a heterogeneous multiple-part package, the other parts in the package are not affected.

You can also edit properties on part packages, in which case the changes appear on every part in the package, and on every part instance.

When you are editing the properties of a library part, you use the Edit Part Properties dialog box. In this dialog box you can add or remove user-defined properties or change the values for the following properties:

- Part Value
- Part Reference
- Primitive
- Graphic
- Packaging
- PCB Footprint
- Power Pin Visibility
- User properties

Assigning a pin name or number

Pin names and numbers can be made invisible or visible on the part by changing the setting of the Pin Names Visible property or Pin Numbers Visible Property, respectively.

Assigning a reference designator

When you place parts on a schematic page, all parts of the same type are assigned the same part reference. For example, C? is assigned to all capacitors. Regardless of the ultimate purpose of your design, each part needs a unique identifier. You can assign part references by editing individual parts in the part editor, or, for PCB designs, by creating a swap file to use with the Back Annotate tool.

For uniquely identifying parts, it is more convenient to use the Annotate command on the Tools menu.

The Annotate tool assigns unique alphanumeric part references. For PCB designs, it assigns individual parts to a package and assigns unique pin numbers to each part in a multiple-part package. References are assigned in order from top to bottom and left to right; parts located at the top of the page have the lowest numerical designation. If two parts share a vertical coordinate, the part further to the left has the lower numerical designation. If you add parts after you've assigned part references, you can easily remove part reference assignment and run Annotate again.

In general, you use Annotate after you've placed all parts and before you use other Capture tools. See Generating output for an overview of the design processing tools.

You can update references incrementally, so that previously assigned part references are not changed, or you can update unconditionally.

Capture automatically updates either instances or occurrences depending upon the type of design you are working with. In general, you should update instances for FPGA and PSpice projects, and update occurrences for PCB and Schematic projects.

Editing part properties

If you have a library part that is nearly perfect, you can tailor the original part so that it suits your project. You can edit the part's properties and you can change its graphical representation or its pins.

Assigning other properties

You can assign other properties to your library parts just as you would assign them to instances or occurrences in your schematic design. See Assigning properties for more information.

To globally change the visibility of pin names or pin numbers

1. With the part open in the part editor, double-click on it to bring up the User Properties dialog box.

2. Select the Pin Names Visible property to control pin name visibility.
3. Select the Pin Numbers Visible property to control pin number visibility.
4. Set the property to FALSE to hide the pin names (or numbers).
5. Set the property value to TRUE to show the pin names (or numbers).
6. Click OK to apply the change.

To uniquely identify parts

1. In the project manager, select schematic folders or schematic pages if you want to process only a portion of the design. If you want to process the entire design, leave the schematic folders or schematic pages unselected.
2. From the Tools menu, choose Annotate. The Annotate dialog box appears.
3. Verify that the dialog box options are set the way you want them. For example, you specify whether to update the entire design or only the schematic folders or pages selected in the project manager, whether to assign part references to all parts or to only those that have not been previously updated, or whether to return all the part references to the unassigned state (such as C? or U?A). Note that if you choose the Reset reference numbers to begin at 1 in each schematic option, it is possible that part references will be duplicated within a schematic folder that contains multiple pages.
4. Click OK.

Note: If you copy a part into the Clipboard and then paste it onto a schematic page, Capture will automatically assign a unique reference designator to the pasted part when two conditions are met:

a.The Auto Reference option on the Miscellaneous tab of the Preferences dialog box is selected.

b.The pasted part has a reference designator assigned to it when it is copied to the Clipboard.

Capture assigns the reference designator, updated to the next available value (one greater than the highest value used on the schematic at that point.) If the pasted part has a default reference (for example, R?) Capture does *not* assign a unique reference designator to it.

Shortcut

Toolbar:

To edit a library part

1. Open the library containing the part.
2. In the project manager, double-click on the part. The part editor opens with the part displayed.
3. Make changes to the part body definition using graphics, text, and images.
4. Make the needed changes to pins. You can move pins after you select them or add pins. To edit pin properties, double-click on the pin.

   Note: You cannot move pin names or pin number text when you are editing a library part. You can move pin names and pin numbers only when you are editing a part instance on a schematic page. For more information, see "Moving pin name and pin number text" on page 186.
5. From the File menu, choose Save.
6. [Optional] If you want to undo all the changes you have made to a part, you can do this

Features of Editing a Part

1. **New Library Name:**

   If you edit a library provided by OrCAD, it is important that you assign a new library name so that your changes are not overwritten when you upgrade or update your software.
2. **Reuse Existign Part:**

You can use an existing part as a model for a new part by moving a copy of the part to a second library and then editing the copy. If you wish to have the new part in the original library, rename the new part, then move it to the original library.

3. **Move Library after Placing Part:**

   If you move a library after you place a part, the connection between the part and its library is broken. In this case, the Update Cache command will not find the library; you will need to use the Replace Cache command and specify the new path to the library.

To switch to a different part in the package

1. From the View menu, choose the Package command.
2. Double-click on the part you wish to edit.

OR

1. From the View menu, choose the Part command.
2. From the View menu, choose the Next Part or Previous Part command.

To edit a part instance on a schematic page in a design

1. Select the part in the schematic page editor.
2. From the Edit menu, choose the Part command. The part editor opens with the selected part displayed.
3. Edit the part to suit your needs.
4. From the File menu, choose the Close command, then select the appropriate update button. See Save Part Instance dialog box to determine which button is appropriate. The part editor window closes and the updated part appears in the schematic page editor.

Features of Editing a Part Instance on a Schematic Page

1. **Opening the Part Editor:**

When you open the part editor from the schematic page editor, the part you are editing cannot be selected on the schematic page. After you close the part editor window, the part can be selected.

2. **Moving Pin Names and Number Text:**

   You can move pin names and pin number text when you are editing a part instance on a schematic page. For more information, see "Moving pin name and pin number text" on page 186.

3. **Editing the Graphic Representation:**

   When you edit a part's graphic representation on a schematic page, you break the connection between the part and the library; if you want to reverse your edits, you use the Replace Cache command of the Design menu.

4. **Part Library Origin:**

   If you need to know a part's library of origin, you can select the part in the project manager, then select Replace Cache from the Edit menu. The part name and the library and path are listed in the dialog box that appears. Click the Cancel button to return to the project manager.

5. **Multiple Part Library Origin:**

   You can discover the library of origin for multiple parts by Creating a cross reference report.

Moving pin name and pin number text

You can move pin names and pin numbers only when you are editing a part instance on a schematic page. For more information, see "To edit a part instance on a schematic page in a design" on page 185.

Note: You cannot move pin names or pin number text when you are creating or editing a library part.

- To move a pin name or pin number, select the pin name or number text and drag it to the desired location.
- To reset a pin name movement, select the pin name text you had moved and from the Edit menu, choose Reset Location, then Pin Name.

- To reset a pin number movement, select the pin number text you had moved and from the Edit menu, choose Reset Location, then Pin Number.

Important

If you move pin names and pin number text when editing a part instance on a schematic page, you cannot open the design in Capture 9.2.3 and earlier versions unless you do the following:

a. Select the .DSN file in the Capture project manager.

b. From the File menu, choose Save As.

The Save As dialog box appears.

c. Select the Remove Pin Name and Number Movement check box and save the design.

Note: Selecting the Remove Pin Name and Number Movement check box will remove all the pin name and number movements you have done in the design.

You can now open the design in Capture 9.2.3 and earlier versions.

Property tables

You can choose a user-defined property from the property tables that follow and assign a value to the property for use with another tool (such as PCB Editor or Layout).

Part property name	Example value	Description
COMPFIXED	YES	If the value is YES, the part (such as an edge connector) is permanently fixed to the board.
COMPGROUP	2	An integer value that assigns the part to a group for placement. The value must be numeric, and between 0 and 100.

COMPKEY	YES	Used to designate a component as the key component in a given group. The key component is placed first, with all the other components in the group placed in proximity to it.
COMPLOC	[1000, 1000]	Part location on the board as X and Y coordinates. Use the following format [X, Y], where X and Y represent the coordinates. Both must be integers in mils or microns.
COMPLOCKED	YES	If the value is YES, the part is temporarily locked in position.
COMPROT	270.00	Part rotation in degrees and minutes counterclockwise from the orientation defined in the Layout library. Use a period (.) to separate degrees and minutes.
COMPSIDE	BOT	Determines which side of a board a part will reside on, TOP or BOT.
FOOTPRINT	DIP24	An explicit definition of the footprint name to attach to the component.
FPLIST	DIP24\400	Comma-delimited list of alternate footprints to attach to components, to ease switching between footprints.
GATEGROUP	1	Identifies gate swapping restrictions within a component. To be swapped, two gates must belong to the same gate group.
PARTNUM	489746	A customer part number that is generally unique for each customer and identifies the exact part, including manufacturer and case type.
PARTSHAPE	74LS04	A generic part number (such as 74LS04 or CK05) that represents a certain part throughout the industry, but may not identify the manufacturer or case type. If no footprint is defined, or the correct footprint isn't found, PARTSHAPE's value is compared to the data in SYSTEM.PRT (in ORCADWIN/LAYOUT/DATA) and the footprint listed in SYSTEM.PRT is used.

POWERPIN	YES	Defines non-wired pins (such as unusual voltages) as belonging to a particular net. POWERPIN is typically used to override the standard GND or VCC attachments to particular pins of an IC.
CONNWIDTH	10	Sets the track width, leaving MINWIDTH and MAXWIDTH at their defaults.
HIGHLIGHT	YES	If the value is YES, the net is highlighted.
MAXWIDTH	12	Sets the maximum track width.
MINWIDTH	8	Sets the minimum track width.
NETGROUP	2	Identifies grouped nets. Use this to select or color nets as a group in Layout (for editing or routing).
NETWEIGHT	60	Integer between 1 and 100 assigning relative priority to the net. The default value is 50.
PLAINLAYERS	GND	Assigns a net to a plane layer. Values are GND and POWER.
RECONNTYPE	ECL	Specifies the reconnect rules for each type of reconnect. Values are STD, HORZ, VERT, NONE, or ECL.
ROUTELAYERS	GND,PWR	Restricts the layers on which this net can route.
SPACINGBYLAYERS	TOP=13,BOT=8	Net spacing for one or more layers.
TESTPOINT	YES	If the value is YES, a test point is automatically assigned to the net.
VIAPERNET	VIA1	Via types allowed for net.
WIDTH	12	Track width value assigned to the MINWIDTH, MAXWIDTH, and CONNWIDTH properties unless overridden.
WIDTHBYLAYER	TOP=6,BOT=12	Net width for one or more layers.

Creating a package

This section covers:

- "Using the package view" on page 192
- "Editing package properties" on page 193
- "Forcing multiple parts into a single package" on page 193
- "Using part or net properties in a package" on page 193

A part or hierarchical block may have an underlying hierarchical description, such as an attached schematic folder. If it does, it's called a nonprimitive. A part or hierarchical block that has no underlying hierarchical description is called a primitive. In Capture, this characteristic is defined in a property, called Primitive, on every part instance. You can change the Primitive property as often as you like during the design process. When a part or hierarchical block is marked as primitive, all of Capture's tools treat it as such. You cannot descend into a part or hierarchical block that is marked as primitive, even if it has an attached schematic folder.

For example, you might create a part and attach a schematic folder that describes its gates and wiring, and then attach schematic folders to some of those parts to describe their transistors. Before you create a netlist for simulation, you would specify those parts as nonprimitive, so Create Netlist can descend far enough to find the transistor-level descriptions. Before you create a netlist for board layout, you would specify the parts as primitive, so Create Netlist stops at the gate-level descriptions. Bill of Materials and Cross Reference work similarly.

For part instances that have their Primitive property set to Default, you can configure Capture to treat them as either primitive or nonprimitive on a design-wide basis, using the Design Template and Design Properties commands on the Options menu. This is useful when you are describing and simulating your design at varying levels of abstraction (as in top-down design).

Note: If you attach a schematic folder to a homogeneous part, it is attached to each part in the package, not the package itself. You cannot attach a schematic folder to a heterogeneous part.

Note: When you attach a schematic folder to a part or hierarchical block, you can specify a full path and filename in the Library text box. So, although you can specify a library that hasn't been saved, you should not try to descend into the attached schematic folder until the library that contains the schematic folder has been saved.

If you don't specify a full path and filename in the Library text box,

Capture expects to find the attached schematic folder in the same design as the part of hierarchical block to which it is attached. If the specified schematic folder doesn't exist in either the design or library, Capture creates the schematic folder when you descend hierarchy on the part or hierarchical block.

For compatibility with future versions of Windows, Capture preserves the case of the path and filename as you specify them in the Library text box.

Parts usually correspond to physical objects—gates, chips, connectors, and so on—that come in packages of one or more parts. Think of these packages as physical parts and the parts you place on a schematic page as logical parts. Physical parts that comprise more than one logical part are sometimes referred to as multiple-part packages. For simplicity, Capture usually refers to both as parts.

Logical parts in a package may have different pin assignments, graphics, and user properties. If all the logical parts in a package are identical except for the pin names and numbers, the package is homogeneous. If the logical parts in a package have different graphics, numbers of pins, or properties, the package is heterogeneous. For example, a hex inverter is homogeneous: the six inverters are identical, except for their pin numbers. A relay, which has a normally opened switch, a normally closed switch, and a coil, is heterogeneous: the three physical parts differ in graphics, number of pins, and properties.

To create a heterogeneous part in a library, open the library and choose New Part from the Design menu. Enter the part name, set the number of parts in the package, and select Heterogeneous in the Package Type group box. Enter the PCB Footprint if you wish to assign one to the part at this time. Click the OK button, and Capture will give you the logical part with reference designator U?A. Draw your part body, add your pins. To get to the B package choose Next Part from the View menu, or press CTRL+N. Capture displays the U?B part for you to edit. Again, draw your part body and add your pins. Repeat this process until all your logical parts are created.

After creating the logical parts of your heterogeneous part in the library you need to assign a unique property to each one. That property can have any name (for example, PACKAGE). To do this, double click on the empty space beside the logical part to get the User Properties dialog box. Choose the New button, type in

PACKAGE into the Property box and a 1 in the Value box. Click twice to attach that property to the logical part. Add this new property to each logical part in your package (part A, B, C, and so forth). Save your library with the new part in it.

Open your schematic and place the A, B, C (and so on) logical parts of your heterogeneous parts appropriately in your design. After you place each logical part, double click on the part to get the property editor. Edit the value of the PACKAGE property shown in the spreadsheet. Leave the Value of 1 on that property for each logical part of the first set you place; assign a Value of 2 to each logical part in the second set, assign a Value of 3 to each logical part in the third set, and so on. Capture uses this value to group the heterogeneous parts correctly when assigning reference designators.

When you get ready to annotate the design you add that property name to the combined property string in the Annotate dialog box. Capture will use this property and the assigned values to annotate the parts correctly in the design. To do this, go to the project manager window, select the design name, and choose Annotate from the Tools menu. Select Update entire design, select Unconditional reference update (select Incremental if you have already partially annotated your design), and type in {PACKAGE} into the Combined property string box. This gives you a combined property string like {Value}{Source Package}{PACKAGE}. When you click OK, Capture then assigns the appropriate reference designators to all your parts in the design including the heterogeneous parts.

Note: Do not manually change the reference designators of heterogeneous parts for a complex hierarchical design. In case you want to change the reference designator for a part placed in the schematic page, delete it, and add it again. This way all the occurrences will get updated correctly.

Using the package view

In this view, you can add and edit package properties, though parts are not available for editing. Use this view if you want to add properties that are the same for all parts in the package.

All packages include the following properties:

- Name

- Alphabetic or numeric part numbering
- Homogeneous or heterogeneous type
- Number of parts per package
- Part reference prefix
- Printed Circuit Board footprint
- Aliases

Editing package properties

As with part properties, you can edit package properties in the library or on the schematic page. If you edit package properties on the schematic page, the changes affect only the parts in the project; you are, in effect, creating a new part that is not stored in a library.

Package properties are inherited by every part in the package and by every part placed on a schematic page. Packages do not support user-defined properties.

Forcing multiple parts into a single package

For PCB designs, if you need to make sure that two or more parts in your design are in the same package, you use the Update Part Reference tool. First, choose a property that all the parts share and verify that the parts all have the same value for that property, then use the Update Part Reference tool.

For example, you might have several NANDs in a schematic folder and four that are in close proximity in the final product. For each of the four NANDs, create a user-defined property named COMPGROUP and set the property's value to 1. In the Combined Property String text box in the Update Part Reference dialog box, enter {COMPGROUP}.

Using part or net properties in a package

Using properties, you can conveniently store part and net information. To change part properties on a single part (or on every instance of the part in a design), edit the part in the schematic page editor. To set part properties on every instance of the part that you

place, edit the part in the part editor. If you want to make changes to a number of parts or nets, the Update Properties command on the Tools menu is a convenient method.

You can use Update Properties to edit any properties except part value, part reference, and netname, and you can update the properties of parts in a design or in a library.

Before you run Update Properties, you create an update file. To identify the parts or nets you want to update, you specify an identifying property or combination of properties. For each identifier you use, you must create a separate update file and run Update Properties.

You can update references incrementally, so that previously assigned part references are not changed, or you can annotate unconditionally, changing all the parts across all the schematic pages processed.

Capture automatically selects to update either instances or occurrences depending upon the type of design your working with. In general, you should update instances for FPGA and PSpice projects, and update occurrences for PCB and Schematic projects.

To view all parts in a package

➤ From the View menu, choose the Package command. An image of all parts in the package appears.

To edit package properties

1. From the View menu of the part editor, choose Package.
2. From the Options menu, choose Package Properties. The Edit Part Properties dialog box appears.
3. Make your changes in the dialog box and click OK. You can change, among other things, the number of parts in the package, the PCB footprint, and the part reference prefix. The changes are reflected in the part editor, but they are not permanent until you save the design.

To edit pin-specific package properties

1. From the View menu of the part editor, choose Package.
2. From the Edit menu, choose Properties. The Package Properties dialog box appears.
3. Make your changes and click OK. Capture updates pin property information and checks for duplicate pin numbers. The Validate and Update buttons also update pin property information and check for duplicate pin numbers.

To specify ignored package pins

The IGNORE property, available for package pins, provides a method for you to specify that certain pins on a part are ignored when the part is placed on a schematic page. Pins that have the IGNORE property assigned to them do not appear on the schematic page. These pins will also not be included on the part footprint for any downstream printed circuit board layout tools. Also, note that ignored pins will not be included in any back annotation from a layout tool.

1. From the View menu of the part editor, choose Package.
2. From the Edit menu, choose Properties. The Package Properties dialog box appears.
3. Select the pins you wish to ignore, and select the IGNORE property for those pins.
4. Click OK.

To force multiple parts into a single package

1. Choose one property that the parts share and assign the same value to that property for each part. You may want to add a user-defined property to each part.
2. In the project manager, select schematic folders or schematic pages if you want to process only a portion of the design. If you want to process the entire design, leave the schematic folders or schematic pages unselected.
3. From the Tools menu, choose Annotate. The Annotate dialog box appears.

4. In the Combined Property String text box, enter the property name. The name must be enclosed in braces: "{" and "}".
5. Verify that the remaining dialog box options are set the way you want them. For example, specify, among other things, whether you are unconditionally updating all references or only those that are set to the unassigned (?) reference.
6. Click OK.

Shortcut

Toolbar:

To create a multiple-part package

1. Open the library that will hold the part.
2. From the Design menu, choose New Part. The New Part Properties dialog box appears.
3. Enter the number of parts in the package (up to 128), and specify whether they are all the same (homogeneous) or different (heterogeneous).
4. Fill in the other fields in the dialog box and click OK. The part editor opens with an empty part outline.
5. Use the graphics tools to define the part body.
6. Use the Place Pin dialog box to add pins to the part. You can share pins such as power and ground pins for each part in the package as described in Creating a shared pin.
7. If you are creating a heterogeneous package, choose Next Part from the View menu, then repeat steps 4 and 5 for each part.

or

1. If you are creating a homogeneous package, choose Next Part from the View menu, then assign pin numbers for each part.
2. From the File menu, choose Save. If you are creating the part in a new library that has not yet been saved, the Save As dialog box appears, giving you the opportunity to name the library file.

Note: If you edit a library provided by OrCAD, it is important that you assign a new library name so that your changes are not overwritten when you upgrade or update your software.

Note: After a part is created, you can add to or decrease the number of parts in the homogeneous package, even if the part starts out as a package of one. However, you can neither increase nor decrease the number of parts in a heterogeneous package.

To update part or net properties

1. Using a text editor, create an update file. See Creating an update file for further information.
2. In the project manager, select schematic folders or schematic pages if you want to process only a portion of the design. If you want to process the entire design, leave the schematic folders or schematic pages unselected.
3. From the Tools menu, choose Update Properties. The Update Properties dialog box appears.
4. Verify that the dialog box options are set the way you want them. For example, you specify, among other things, whether you are updating parts or nets, whether you want to overwrite existing property values, and the name and location for the update file.
5. Click OK.

Note: Capture preserves the case of part names and net names, but ignores the case when comparing names for electrical connection. That means you may use uppercase or lowercase letters as you wish, but you need not remember the case.

Note: Capture report files are text files and can be opened in any text editor. You may want to use the tab alignment capability of your word processor to line reports up correctly. Spreadsheets will automatically align the columns of Capture-generated report files.

Editing parts in a library

This section covers how:

- "To edit a library part" on page 198
- "To switch to a different part in the package" on page 199

- "To edit a part instance on a schematic page in a design" on page 199

If you have a library part that is nearly perfect, you can tailor the original part so that it suits your project. You can edit the part's properties and you can change its graphical representation or its pins.

To edit a library part

1. Open the library containing the part.
2. In the project manager, double-click on the part. The part editor opens with the part displayed.
3. Make changes to the part body definition using graphics, text, and images.
4. Make the needed changes to pins. You can move pins after you select them or add pins. To edit pin properties, double-click on the pin.
5. From the File menu, choose Save.

Note: If you edit a library provided by OrCAD, it is important that you assign a new library name so that your changes are not overwritten when you upgrade or update your software.

Note: You can use an existing part as a model for a new part by moving a copy of the part to a second library and then editing the copy. If you wish to have the new part in the original library, rename the new part, then move it to the original library.

Note: If you move a library after you place a part, the connection between the part and its library is broken. In this case, the Update Cache command will not find the library; you'll need to use the Replace Cache command and specify the new path to the library.

You cannot make changes to a design in the schematic page editor while you are editing a part in the part editor.

To switch to a different part in the package

1. From the View menu, choose the Package command.
2. Double-click on the part you wish to edit.

or

1. From the View menu, choose the Part command.
2. From the View menu, choose the Next Part or Previous Part command.

To delete a part in a package of a heterogeneous part

1. From the View menu, choose the Package command.
2. Select the part that you want to delete.
3. From the Edit menu, select Delete.

Caution

You cannot undo the deletion of part from a package. Once the part is deleted from a package, all information regarding the part is lost.

To edit a part instance on a schematic page in a design

1. Select the part in the schematic page editor.
2. From the Edit menu, choose the Part command. The part editor opens with the selected part displayed.
3. Edit the part to suit your needs.
4. From the File menu, choose the Close command, then select the appropriate update button. See Save Part Instance dialog box to determine which button is appropriate. The part editor window closes and the updated part appears in the schematic page editor.

Note: When you open the part editor from the schematic page editor, the part you are editing cannot be selected on the schematic page. After you close the part editor window, the part can be selected.

Note: When you edit a part's graphic representation on a schematic page, you break the connection between the part and the library; if you want to reverse your edits, you use the Replace Cache command of the Design menu.

Note: If you need to know a part's library of origin, you can select the part in the project manager, then select Replace Cache from the Edit menu. The part name and the library and path are listed in the dialog box that appears. Click the Cancel button to return to the project manager.
You can discover the library of origin for multiple parts by Creating a cross reference report.

Moving parts or symbols between libraries

You can store parts or symbols in any library you wish. You can create libraries that have a special purpose. You may wish to transfer some parts or symbols from one library to another and you may wish to store some parts or symbols in multiple libraries. If you move a part that has part aliases, the part aliases also move.

Note: A part that is open in an editor cannot be moved or copied.

To move parts between libraries

1. Verify that the parts are not open in the part editor or the spreadsheet editor.
2. In the project manager, select the parts you wish to move.
3. From the Edit menu, choose the Cut command, or if you wish to have a copy of the parts in both libraries, choose the Copy command.
4. Open the library that will hold the part and click the left mouse button in the project manager.
5. From the Edit menu, choose the Paste command.

or

1. Verify that the parts are not open in the part editor or the spreadsheet editor.
2. In the project manager, open both libraries.

3. Drag and resize the two project manager windows so that each is visible.
4. Select the parts that you wish to move, then drag them to the second library's project manager window. If you wish to have a copy of the parts in both libraries, press and hold CTRL while you are dragging.

Note: If you edit a library provided by OrCAD, it is important that you assign a new library name so that your changes are not overwritten when you upgrade or update your software.

To create a part using an existing part

1. Follow the procedure above to create a copy of the part in another library.
2. If you want to move the new part to the same library as the original:
3. From the Design menu, choose the Rename command and give the new part's a different name.
4. Follow the procedure above to drag the new part to the original library.

Updating part properties in a library

If you need specific information, like stock number or supplier, on your parts, you can add a property and set the property value in the library. Later, when you place the part in a project, the information is present; there's no need to add information to the placed part.

You can edit parts individually in the part editor, but when you wish to update properties of a number of parts, the Update Properties tool is very convenient. You can use the Update Properties tool to edit any properties except part value and part reference.

Before you run the Update Properties tool, you create an update file as described in Creating an update file. To identify the parts you wish to update, you specify an identifying property or combination of properties called a combined property string. For each combined property string you use, you must create a separate update file and run the Update Properties tool.

To update part properties

1. Using a text editor, create an update file.
2. Open the library that holds the parts you want to update.
3. From the Tools menu, choose the Update Properties command. The Update Properties dialog box appears.
4. In the Action area, select Parts.
5. Verify that the other dialog box selections are set as you want them, then click OK. Unless you select the button to Unconditionally update the property, properties that currently hold a property value are not updated.

Note: If you edit a library provided by OrCAD, it is important that you assign a new library name so that your changes are not overwritten when you upgrade or update your software.

Copying a schematic page to a library

Schematic folders and schematic pages behave almost identically in libraries as they do in designs. The primary differences are:

Schematic folders and schematic pages cannot be created in libraries. If you want to add a schematic folder or schematic page to a library, you must create it in a design and then move it over to the library. In addition to this topic, see Copying a schematic folder to or from a library for more information.

Schematic folders and schematic pages are limited to the library tool set, namely updating properties, exporting properties, and importing properties.

The Update Cache and Replace Cache commands are not available when parts are selected in the library cache.

Annotate is unavailable for parts in schematic folders contained in libraries. You should use Annotate in a schematic folder prior to moving it into a library.

You can open a library-stored schematic page in a schematic page editor, and edit it exactly the same as if you had opened it from a design; however, it is recommended that you edit a schematic page

in a design. If a schematic folder stored in a library is the child of another schematic folder in a design, the Descend Hierarchy command in the parent schematic folder opens the library containing the child schematic folder and a schematic page editor window containing the schematic page.

Note: Before editing a schematic page stored in a library, you should find out which projects call the schematic folder. Editing a library-stored schematic folder may create problems for other projects that use the library-stored schematic folder.

If you have a small circuit that you use in many projects, you can put that circuit on a separate schematic page, save it in a library, and attach it to a part that you can place in any design. It is a good idea to keep the attached schematic folder and the part in the same library.

To save a schematic page in a library, you must first move the page into a schematic folder. When you save a schematic page in a library, Capture puts the circuit's parts in the library cache.

A schematic folder or schematic page that is open in an editor cannot be moved or copied.

To save a schematic page in a library

1. Verify that the page is not open in the schematic page editor.
2. In the project manager, create a schematic folder to hold the page.
3. In the project manager, select the schematic page you wish to save, then copy or move the page into the new schematic folder. Leave the new schematic folder selected.
4. From the Edit menu, choose Copy.
5. Open the project manager for the library in which you want to store the schematic folder.
6. From the Edit menu, choose Paste.

or

1. Verify that the page is not open in the schematic page editor.

2. Open the project manager for the project and create a schematic folder to hold the page.
3. Open the project manager for the library in which you want to store the schematic folder.
4. Drag and resize the project manager windows for the project and the library so that each is visible.
5. In the project manager for the project, select the schematic page you wish to save, then copy or move the page into the new schematic folder. Leave the new schematic folder selected.
6. Press and hold CTRL while you drag the schematic folder to the project manager for the library.

Note: If you edit a library provided by OrCAD, it is important that you assign a new library name so that your changes are not overwritten when you upgrade or update your software.

Note: If you copy or move a document from one design or library to another, you should save the destination design or library immediately. If you do not, you may lose data if you open the moved document in the schematic page editor or part editor and then close the editor without saving the document.

Copying a schematic folder to or from a library

Schematic folders and schematic pages behave almost identically in libraries as they do in designs. The primary differences are:

Schematic folders and schematic pages cannot be created in libraries. If you want to add a schematic folder or schematic page to a library, you must create it in a design and then move it over to the library. In addition to this topic, see Copying a schematic page to a library for more information.

Schematic folders and schematic pages are limited to the library tool set, namely updating properties, exporting properties, and importing properties.

The Update Cache and Replace Cache commands are not available when parts are selected in the library cache.

Annotate is unavailable for parts in schematic folders contained in libraries. You should use the Annotate command in a schematic folder prior to moving it into a library.

You can open a library-stored schematic page in a schematic page editor, and edit it exactly the same as if you had opened it from a design; however, it is recommended that you edit a schematic page in a design. If a schematic folder stored in a library is the child of another schematic folder in a design, the Descend Hierarchy command in the parent schematic folder opens the library containing the child schematic folder and a schematic page editor window containing the schematic page.

Note: Before editing a schematic page stored in a library, you should find out which projects call the schematic folder. Editing a library-stored schematic folder may create problems for other projects that use the library-stored schematic folder.

If you have a circuit that you use in many projects, you can put that circuit in a separate schematic folder, save it in a library, and attach it to a part that you can place in any design. It is good design practice to keep the part and the attached schematic folder in the same library.

When you save a schematic folder in a library, Capture puts the circuit's parts in the library cache.

A schematic folder or schematic page that is open in an editor cannot be moved or copied.

To save a copy of a schematic folder as a library object

1. Verify that no Capture editor is open on any part in the schematic folder.
2. In the project manager, select the schematic folder you wish to save.
3. From the Edit menu, choose the Copy command.
4. Open the project manager window of the library in which you want to store the schematic folder.
5. From the Edit menu, choose the Paste command.
6. From the File menu, choose the Save command.

or

1. Verify that no Capture editor is open on any part in the schematic folder.
2. Drag and resize the project manager windows for the project and the library so that each is visible.
3. Select the schematic folder you wish to save.
4. Press and hold CTRL while you drag the schematic folder to the library's project manager window.
5. From the File menu of the library's project manager, choose Save.

Note: If you edit a library provided by OrCAD, it is important that you assign a new library name so that your changes are not overwritten when you upgrade or update your software.

Note: If you copy or move a document from one design or library to another, you should save the destination design or library immediately. If you do not, you may lose data if you open the moved document in the schematic page editor or part editor and then close the editor without saving the document.

To copy a schematic folder from a library to a project

1. Open the library containing the schematic folder you wish to copy in the project manager and select the schematic folder.
2. From the Edit menu, choose Copy.
3. Open the project in which you want to put the schematic folder.
4. From the Edit menu, choose Paste.
5. From the File menu, choose Save.

or

1. Open the library and the design, and from the Window menu choose the Tile Horizontally command.
2. Select the schematic folder you wish to copy.
3. Press and hold CTRL while you drag the schematic folder to the project manager window.

4. From the File menu, choose Save.

You can also attach a schematic folder to a part or hierarchical block without copying the schematic folder into the project or library, but this method affects design portability. For more information, see Attaching a schematic folder.

Copying a part from the design cache to a library

You can copy parts from the design cache to a library. This is useful if you have modified a part through the schematic page editor, and want a permanent copy of the part.

To save a design cache part in a library

1. In the project manager, open the design cache, and highlight the part you wish to save.
2. From the Edit menu, choose Copy.
3. Open the library in which you want to store the part.
4. From the Edit menu, choose Paste.

or

1. Drag and resize the project manager windows for the design and the library so that each is visible.
2. In the project manager, open the design cache, and highlight the part you wish to save.
3. Drag the part to the project manager window.

Note: If you edit a library provided by OrCAD, it is important that you assign a new library name so that your changes are not overwritten when you upgrade or update your software.

Note: If you copy or move a document from one design or library to another, you should save the destination design or library immediately. If you do not, you may lose data if you open the moved document in the schematic page editor or part editor and then close the editor without saving the document.

Closing and saving a library

Changes you make to a part are temporary until you save the part or the library using one of the commands on the File menu. When you save a library, you are saving all the parts and symbols residing in the library. If you have several parts or symbols open in the part editor, changes you have made to any of them are saved.

If the library is new and has not yet been saved, the Save As dialog box appears, giving you the opportunity to specify a drive and replace the system-generated name.

To save a part or symbol

➤ From the File menu of the part editor, choose the Save command. The active library or the library that holds the active part is saved.

To save a library

➤ From the File menu of the project manager, choose the Save command. The active library or the library that holds the active part is saved.

To rename a part

1. In the project manager, select the part.
2. From the Design menu, choose Rename. The Rename dialog box appears.
3. Enter the new name and click OK.

Note: If you edit a library provided by OrCAD, it is important that you assign a new library name so that your changes are not overwritten when you upgrade or update your software.

Note: When you attach a schematic folder to a part or hierarchical block, you can specify a full path and filename in the Library text box. So, although you can specify a library that hasn't been saved, you should not try to descend into the attached schematic folder until the library that contains the schematic folder has been saved.

If you don't specify a full path and filename in the Library text box, Capture expects to find the attached schematic folder in the same design as the part of hierarchical block to which it is attached. If the specified schematic folder doesn't exist in either the design or library, Capture creates the schematic folder when you descend hierarchy on the part or hierarchical block.

For compatibility with future versions of Windows, Capture preserves the case of the path and filename as you specify them in the Library text box.

Note: When you save a project, Capture automatically creates a backup with a .DBK file extension. When you save a library, Capture automatically creates a backup with a .OBK file extension. If you save only a schematic page or a part, no backup is generated.

4

Working with designs

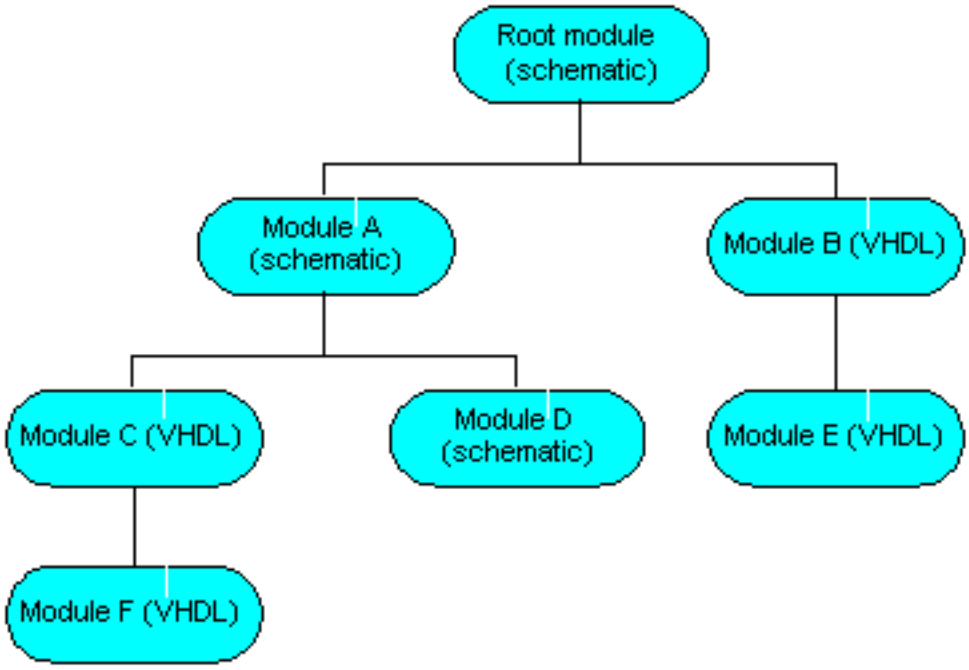
This chapter covers:

- Creating a new design on page 212
- Creating a new schematic page on page 214
- Creating a new text file on page 220
- Creating a new VHDL or Verilog file on page 220

Capture provides the means to create electronic designs in two media: as schematics or as VHDL models.

Schematic designs can include VHDL or Verilog models (one or the other, not both) as lower level hierarchical modules, but these models

can only instantiate other models (of the same type) at lower levels in the hierarchy. Consider the following illustration:



Any schematic design module can include either schematics or VHDL/Verilog models as instantiated components. However, VHDL/Verilog design modules are limited to other modules of the same type as instantiated components. Hence, if the root module of your design is a VHDL model, all lower level modules must also be VHDL models.

Note: If you haven't specified a root for your design, you cannot generate reports. Also, when folders are copied to a new design, the ROOT designation is lost and must be reestablished in the design.

Creating a new design

This section covers:

- Creating a new design file before populating the project on page 213
- Creating a new design after the project is populated on page 213

Note: There can be only one design file in a project. If you create a new design file, or move or copy a different one into the project, the project manager will ask you if you want to replace the existing design file.

Creating a new design file before populating the project

When the project is first created, the project manager creates a design file with the same name as the project. It also creates a schematic folder within the design file, and a schematic page within the folder. The schematic folder icon is marked with a backslash character (\) to signify that it is the root schematic folder.

A design file also contains a design cache, which is like an embedded library—it contains a copy of all the parts and symbols used on the schematic pages.

You can view the hierarchy using the File tab in the project manager.

You can create a new design file to replace the design created by the project manager.

Note: A new design inherits characteristics from the settings in the Design Template dialog box. You should check those settings before you create a design.

Note: While using the Save As dialog box to rename the design name, do not specify a dot (.) in the design file name.

Creating a new design after the project is populated

If you replace a current design file that contains schematic folders and pages, those folders and pages are replaced also.

Note: Though the design file and its schematic folders and pages are removed from the project, they are not deleted. The design still exists in its design file configuration, in the directory where it was saved.

In the case where you replace a current design with a newly created one, you will be replacing it with an empty design, unless you first populate the new design outside of the project.

When the project is first created, the project manager creates a design file (.DSN) with the same name as the project. If you don't want the default design file, you can replace it by moving or copying a different design file into the project, or you can create a new one.

Note: Because a new design inherits characteristics from the settings in the Design Template dialog box, you should check those settings before you create a design.

Note: There can be only one design file in a project. If you create a new design file, or move or copy a different one into the project, the project manager will ask you if you want to replace the existing design file.

To create a new design file

1. From the File menu, choose New, then choose Design.
2. The design opens in a new project manager and a new schematic page appears.

Note: Schematic folder, schematic page, part, part alias, and symbol names are case sensitive. It is possible to have a part named "XYZ" and another one named "xyz", and Capture's tools will treat the two separately.

Note: As soon as you create a new design a project file is created with the same name as the design with the .opj extension. For details of how to create a project see Starting a new project.

Creating a new schematic page

This section covers:

- Generating the schematic page on page 215
- Controlling or grid reference visibility on page 215
- Creating a custom title block on page 216
- Setting up the default title block on page 218
- Placing multiple title or revision blocks on page 219

Schematic pages are contained in schematic folders. There can be multiple schematic folders in a project and each folder can have multiple schematic pages.

Generating the schematic page

To create a new schematic page in the design

1. On the File tab of the project manager, select the schematic folder that requires a new schematic page.
2. Click the right mouse button and choose New Page from the pop-up menu. A new schematic page appears within the schematic folder you selected in step 1.

Controlling or grid reference visibility

To specify default or grid reference visibility for new designs

1. From the schematic page editor's Options menu, choose the Design Template command, then choose the Grid Reference tab.
2. In the Grid References Visible or Visible group, click the left mouse button on the Displayed or Printed option to change the visibility.

To change or grid references visibility for one schematic page

1. From the schematic page editor's Options menu, choose the Schematic Page Properties command, then choose the Grid Reference tab.
2. In the Grid References Visible or Visible group, click the left mouse button on the Displayed or Printed option to change the visibility.
3. or (for grid references only)
4. From the schematic page editor’s View menu, choose Grid References.

To specify grid reference width

1. From the schematic page editor's Options menu, choose the Schematic Page Properties command, then choose the Grid Reference tab.
2. In the Horizontal or Vertical group, enter the desired width (in inches or metric units) in the Width text box.

Creating a custom title block

Capture provides ANSI, and OrCAD title blocks in the CAPSYM.OLB library. In addition, you can create your own title block and store it in a library for future use. There are two types of title blocks:

- A default title block is placed by Capture at the lower right corner of each schematic page; information that you specify in the Title Block tab of the Design Template dialog box is incorporated into the title block fields. This information is also included in reports from Capture tools.
- You can place any number of optional title blocks at any locations you choose. The text that appears is a result of visible properties that you define when you create the symbol or after you place the title block.

When you make an optional title block, you create its graphic symbol, then define and place visible properties. When you make a new default title block, you create its graphic symbol, add one or more properties to define the information fields, then you provide the information that will appear in the fields.

The properties that define the default title block fields are as follows:

- **Doc**. Specifies the document number.
- **RevCode**. Specifies the revision.
- **Cage Code**. Specifies the Cage Code.
- **Title**. Specifies the title.
- **OrgName**. Specifies the organization name.
- **OrgAddr1**. Specifies the first line of the organization's address.

- **OrgAddr2**. Specifies the second line of the organization's address.
- **OrgAddr3**. Specifies the third line of the organization's address.
- **OrgAddr4**. Specifies the fourth line of the organization's address.
- **Page Count**. Specifies the number of schematic pages in the design.
- **Page Number**. Specifies the number of the schematic page. The page number determines when it will be printed in relation to the other schematic pages of the design.

To create a custom title block symbol

1. In the project manager, open the library in which you will store the title block symbol.
2. From the Design menu, choose the New Symbol command. The New Symbol dialog box opens.
3. Enter a name and select Title Block as the Symbol Type, then click OK. The part editor opens with an empty part boundary box.
4. Use the graphics tools to create the title block. See Creating graphics. The part boundary box will stretch to accommodate your graphic objects.

To create fields that are automatically filled on a default title block

1. With the title block graphic symbol displayed in the part editor, double-click an area where there are no objects to display the User Properties dialog box.
2. Choose the New button. The New Property dialog box appears.
3. Enter one of the properties listed above in both the Name and Value text boxes, then click OK to dismiss the New Property dialog box.
4. In the Properties dialog box, choose the Display button, then select the Visible option.

5. Click OK to dismiss the Display Properties dialog box, then click OK again to dismiss the User Properties dialog box. The part editor appears with the property representation visible.
6. Use the mouse to move the property representation to the appropriate location and click the left mouse button to place the representation. This property representation, which serves as a place holder, appears in the selection color.
7. Repeat steps 2 through 6 for each property of your title block.
8. Save the title block.

To provide information for the fields of a custom default title block

1. From the Options menu, choose the Design Template command, then choose the Title Block tab.
2. For each of the nine properties listed above that you have added to your title block symbol, enter the text that will appear in your title block.
3. Enter the library name and the distinctive name of the title block.
4. Click OK.

Note: If you edit a library provided by OrCAD, it is important that you assign a new library name so that your changes are not overwritten when you upgrade or update your software.

Note: The size of a part or a symbol is limited to 32 by 32 inches.

Setting up the default title block

In Capture, each schematic page has a default title block in the lower right corner. Title block information that you provide in the Design Template is written into the fields of the title block. You can choose the title block that Capture provides in the CAPSYM.OLB library or you can create a custom title block.

Selections that you make following these instructions are reflected in schematic pages you create subsequently, but do not affect existing schematic pages.

To specify information for title block fields

1. From the Options menu, choose the Design Template command, then choose the Title Block tab.
2. Enter the information for the nine fields that appear. This information appears in the title block and in reports generated by the Capture tools.

To select a default title block symbol

1. From the Options menu, choose the Design Template command, and then choose the Title Block tab.
2. Specify a path and library. You can use the Browse button to locate a title block.
3. Specify the name of the title block, maintaining the case of the original name.
4. Click OK to dismiss the Design Template.

Note: If Capture does not find a title block with the name you specify (the case of letters must match) in the library and path you specify, no default title block is placed.

Note: If you are using CAPSYM.OLB and you have maintained the directory structure that OrCAD provides, you can leave the Library Name text box empty.

Placing multiple title or revision blocks

Capture places a default title block at the lower right corner of every schematic page. In addition, you may place any number of optional title blocks at any location on the schematic page. Optional title blocks, unlike default title blocks, do not include information from the design template, but you can define and place visible properties on the title block.

Information placed as properties in optional title blocks will not appear in reports or netlists created by Capture; only the information in the default title block will be used.

To place optional title blocks

1. From the Place menu, choose the Title Block command. The Place Title Block dialog box appears.
2. In the Symbol text box, enter the name—you can use the standard "*" and "?" wildcard characters. Capture scans the selected libraries and lists all symbols that match the name or wildcard.
3. If the title block name is not listed, see Searching for a part in the libraries for further information.
4. Click on a title block name in the list for a preview, or double-click on it to place the title block. You can also select the title block name and click OK to place the title block.

Creating a new text file

To create a new text file from the project manager

1. From the File menu, point to New and choose Text.
2. Type in the text that you want.
3. Close the text session when you are finished. Capture asks if you want to save the text file.

   If you want to save it, enter a name and location for storage.

Creating a new VHDL or Verilog file

You can create VHDL or Verilog files as part of your design's functionality description, or as test benches for simulation with NC VHDL or some other simulator. You can also instantiate lower level VHDL or Verilog files within a VHDL or Verilog file.

Note: Any model instantiations within a VHDL or Verilog file must be of the same type (that is, VHDL or Verilog) as the parent file.

To create a new VHDL or Verilog file

There are two ways to create a new VHDL or Verilog file in Capture:

1. From the File menu, choose New, then choose VHDL File or Verilog File, as appropriate.
2. A file of the appropriate type opens in Capture's editor.

or

1. With the project manager active, choose New VHDL File or new Verilog from the Design menu. The file opens in the appropriate editor and a dialog box appears, asking if you want to add the file to the project.
2. Choose the Yes button to add the file to the project that is currently open. The Save As dialog box appears.

   Note: If you choose the No button, Capture does not add the file to your project and you must save it yourself at a later point in time.
3. Select a directory for the file and supply a filename. By default, a VHDL file's name is VHDL*n*.VHD (where n is an integer indicating the number of .VHD files created in the current session). Similarly, a Verilog file is named Verilog*n*.V.
4. Choose the Save button. Capture saves the file and places it in the Design Resources folder of your project.

5

Placing parts and pins

This chapter covers:

- "Searching for a part in the libraries" on page 223
- "Placing parts" on page 225
- "Creating hierarchical blocks" on page 228

Searching for a part in the libraries

Capture provides more than 30,000 parts in more than 80 libraries. You will find the part you need using the Place Part dialog box.

The Place Part dialog box lists the names of parts that reside in the selected libraries. You can use the Add Library and Remove Library buttons to specify the search libraries. You can filter the list of parts by typing a selective search string with wildcards or setting the filter (provided with the Filter button), and you can even browse parts graphically.

Note: The Place Part dialog is not a non-modal dockable dialog.

Note: The dialog can be pinned to keep the dialog visible at all times. Or unpinned to ensure that the dialog slides in and out of view when the mouse pointer hovers over it.

To search for a part by name

1. From the Place menu of the schematic page editor, choose the Part command. The Place Part dialog box appears.
2. In the Part text box, enter the name (you can use the standard "*" and "?" wildcard characters). Capture scans the selected libraries and lists all parts that match the name or wildcard, and that meet the criteria (if any) specified in the filter.

To browse parts graphically

1. From the schematic page editor's Place menu, choose Part. The Place Part dialog box appears.
2. Select the library or libraries you wish to browse, then select the part from the part list. The selected part appears in the preview box. You can use the up and down scroll buttons, or the arrow keys, to traverse the list and view each part in turn.

To add multiple libraries

1. From the schematic page editor's Place menu, choose Part. The Place Part dialog box appears.
2. Choose the Add Library button. The Browse File dialog box appears.
3. If the library you wish to add is not listed in the File Name box, do one or more of the following:
   - ❑ In the Look in drop list box, select a new drive, a new directory, or both.
   - ❑ In the Files of type text box, select the extension of the library you wish to search.
4. Select a library from the File Name box and click OK. The library name appears in the Libraries box of the Place Part dialog box.
5. Repeat steps 2 through 4 until all the libraries you wish to search appear in the Libraries box.

To search all libraries in a directory

1. From the schematic page editor's Place menu, choose Part. The Place Part dialog box appears.
2. Enter the name of the part to search in the Search For text box.
3. Choose the Browse button. The Browse File dialog box appears. Select the library directory to start the part search in, then choose the Open button.

   Note: Capture will search all libraries in the specified directory, but will not search sub-directories.

4. In the Part Name text box, type the name of the part to search for. Use the standard "*" and "?" wildcard characters to broaden the search.
5. Choose the Search button. Capture scans the libraries in the selected directory, and lists all parts that match the name or wildcard.
6. Select the library containing the part you want and click OK.
7. Click OK to close the Place Part dialog box.

Note: Capture preserves the case of part names and net names, but ignores the case when comparing names for electrical connection. That means you may use uppercase or lowercase letters as you wish, but you need not remember the case.

Shortcut

Tool palette:

Placing parts

Parts are stored in libraries. Capture has more than 30,000 parts in more than 80 libraries. In addition, you may wish to create your own parts in custom libraries. Some library parts have a convert as well as the normal graphical representation. Many packages contain more than one part, in which case you may need to specify which of the parts you wish to place.

The first time a part is placed, a copy of the part is created in the design cache.

To place a part

1. From the Place menu, choose the Part command. The Place Part dialog box appears. For more information, see Searching for a part in the libraries.
2. From the Parts list, select the part you wish to place. Keep the following information in mind as you select the part:

- If you wish to place a convert version of the part, select Convert in the Graphic group box.
- If the package contains more than one part, select one of the parts from the drop list in the Packaging group box. The part appears in the preview box.
- If the part is a heterogeneneous part, you need to decide which part in the package you want at this time, because you won't be able to change the part in the package after the part is placed.

Note: Whether the part is homogeneous or heterogeneous part, and you are placing multiple copies of the same part in the package, then you do not need to specify the part number at the time of placing the part. Capture will auto-increment the part numbers as you keep placing the parts on the schematic.

3. Click OK. An image of the part is attached to the pointer.

Tip

You can press F6 to change the cursor to crosshair to place the part at a specific location.90Move the part image and click the left mouse button to place the part.

4. For each instance of the part you want to place, repeat step 4.
5. Press the ESC key or select another tool to dismiss the part that's attached to the pointer.

Note: When you place a part off-grid, it remains off-grid through any cut-and-paste and drag-and-drop operations.

Note: If you place parts so that two pins meet end to end, the pins are connected.
OrCAD recommends that you connect the pins of the parts using a wire, and avoid placing parts so that two pins meet end to end. This is because, parts with direct pin to pin connections produce a system generated net name to establish the connection and:

- Capture will not allow you to assign your own net name in the place of the system generated net name.
- Searching for the system generated net name can be difficult if you are not aware of the pin to pin connection.

- If you move the parts after creating the netlist, the system generated net name might change. This may cause net name conflicts when you run backannotation.

Note: OrCAD recommends that you do not connect a power symbol directly to a power pin. Connect the power symbol to the power pin using a wire.

Note: You can place a part in the middle of a wire segment without redrawing the wire by placing the part over the wire such that two pins on the part connect with the wire segment. Then click the left mouse button over the part with the TAB key pressed until just the overlapping wire segment is selected. Finally, delete the wire segment.

Note: Do not manually change the reference designators of heterogeneous parts for a complex hierarchical design. In case you want to change the reference designator for a part placed in the schematic page, delete the part and add it again. This way all the occurrences will get updated correctly.

Note: When you place a part, make sure that the Automatically reference placed parts check box is selected in the Miscellaneous tab of the Preferences dialog box. This will ensure that the part references for the newly placed part are unique.

Placing a part from a custom part library:

1. From the Place menu, choose the Part command. The Place Part dialog box appears.
2. Click Add Library
3. Browse to the location where your custom library file (.olb) is located. Select the library and click Open. The newly added library is listed along with the other available libraries. Also, a list of parts in the library are listed under the Part List. list box
4. From the Parts List list box, select the part you wish to place. Follow steps 3 through 6 of the previous procedure to complete the procedure of placing a part from a custom part library.

Shortcut

Tool palette:

Creating hierarchical blocks

This section covers:

- "Attaching a schematic folder to a hierarchical block" on page 230
- "Creating a hierarchical block from a VHDL model" on page 233
- "Creating a hierarchical block from a Verilog model" on page 234

A hierarchical block is a representation of a schematic folder, which is attached to the hierarchical block. It provides vertical (downward-pointing) connection only. The hierarchical pins in a hierarchical block act as points of attachment for electrical connections between the hierarchical block and other connectivity objects in the attached schematic folder. A hierarchical block functions just like a part with an attached schematic folder.

Before you create or resize a hierarchical block, make sure the Snap to grid option is turned on (from the schematic page editor's Options menu, choose Preferences). If the hierarchical block is on Fine grid,

then hierarchical pins inside it are also on Fine grid—even if you change the Snap to grid setting before you place them—and it may be difficult to connect to these off-grid hierarchical pins.

A part with an attached schematic folder functions exactly as described for hierarchical blocks, and pins on such a part function exactly as described for hierarchical pins within a hierarchical block. You can use the same attached schematic folder for either method of defining a hierarchy. The only difference between the two methods is that a part with an attached schematic folder is easier to reuse. See Creating parts and assigning properties for related information.

If you choose the Descend Hierarchy command on a nonprimitive part or hierarchical block, and Capture cannot find the attached schematic folder, Capture creates a schematic folder in the active design.

Note: When you descend into an object that does not yet have a schematic folder or page associated with it, Capture creates the new schematic page and folder and gives it the same name as the hierarchical block. Because schematic names, schematic page names, part names, and symbol names are all limited to 31 characters, it is best to limit hierarchical block names to 31 characters.

When you place a hierarchical block, you must specify a reference. However, the reference need not be updated if the hierarchical block is primitive. For example, you could specify the reference to be "Halfadd?" when you place a hierarchical block. Then, when you run Annotate, the hierarchical block's reference is updated along with other parts.

If you attach an existing schematic folder to a hierarchical block, Capture automatically creates the hierarchical pins that correspond with the schematic folder's hierarchical ports. If you descend hierarchy on a hierarchical block whose schematic folder doesn't yet exist, then Capture automatically creates the hierarchical ports that correspond with the hierarchical pins of the hierarchical block.

Note: If you attach external schematic folders or other files to hierarchical blocks in a design or parts in a library, be sure to include the attachments when you pass the design or library to a board fabrication house or to another engineer. Attached schematic folders and other files are not carried along automatically when you copy or move a part, schematic folder, or schematic page to another library, design, or schematic folder. Only the "pointers" to the attached schematic folders and files—that is, their names and the names of the designs or libraries that contain them—are carried along.

Attached files work much like their counterparts in email—they do not provide an alternative definition of the part (as do attached schematic folders).

Note: When you attach a schematic folder to a part or hierarchical block, you can specify a full path and filename in the Library text box. So, although you can specify a library that hasn't been saved, you should not try to descend into the attached schematic folder until the library that contains the schematic folder has been saved.

If you don't specify a full path and filename in the Library text box, Capture expects to find the attached schematic folder in the same

design as the part of hierarchical block to which it is attached. If the specified schematic folder doesn't exist in either the design or library, Capture creates the schematic folder when you descend hierarchy on the part or hierarchical block.

For compatibility with future versions of Windows, Capture preserves the case of the path and filename as you specify them in the Library text box.

Note: The Select Entire Net command is restricted to the active schematic page—it doesn't follow hierarchical blocks, hierarchical ports, or off-page connectors across schematic folders or schematic pages. For more information, see Tracing a net.

Remember that nets on a schematic page are electrically connected by name, by alias, or by connection to a named hierarchical port or off-page connector.

Attaching a schematic folder to a hierarchical block

A hierarchical block is a representation of a schematic folder, which is attached to the hierarchical block. It provides vertical (downward-pointing) connection only. The hierarchical pins in a hierarchical block act as points of attachment for electrical connections between the hierarchical block and other connectivity objects in the attached schematic folder. A hierarchical block functions just like a part with an attached schematic folder.

Before you create or resize a hierarchical block, make sure the Snap to grid option is turned on (from the schematic page editor's Options menu, choose Preferences). If the hierarchical block is on Fine grid, then hierarchical pins inside it are also on Fine grid—even if you change the Snap to grid setting before you place them—and it may be difficult to connect to these off-grid hierarchical pins.

A part with an attached schematic folder functions exactly as described for hierarchical blocks, and pins on such a part function exactly as described for hierarchical pins within a hierarchical block. You can use the same attached schematic folder for either method of defining a hierarchy. The only difference between the two methods is that a part with an attached schematic folder is easier to reuse. See Creating parts and assigning properties for related information.

If you choose the Descend Hierarchy command on a nonprimitive part or hierarchical block, and Capture cannot find the attached schematic folder, Capture creates a schematic folder in the active design.

Note: When you descend into an object that does not yet have a schematic folder or page associated with it, Capture creates the new schematic page and folder and gives it the same name as the hierarchical block. Because schematic names, schematic page names, part names, and symbol names are all limited to 31 characters, it is best to limit hierarchical block names to 31 characters.

When you place a hierarchical block, you must specify a reference. However, the reference need not be updated if the hierarchical block is primitive. For example, you could specify the reference to be "Halfadd?" when you place a hierarchical block. Then, when you run Annotate, the hierarchical block's reference is updated along with other parts.

If you attach an existing schematic folder to a hierarchical block, Capture automatically creates the hierarchical pins that correspond with the schematic folder's hierarchical ports. If you descend hierarchy on a hierarchical block whose schematic folder doesn't yet exist, then Capture automatically creates the hierarchical ports that correspond with the hierarchical pins of the hierarchical block.

Note: If you attach external schematic folders or other files to hierarchical blocks in a design or parts in a library, be sure to include the attachments when you pass the design or library to a board fabrication house or to another engineer. Attached schematic folders and other files are not carried along automatically when you copy or move a part, schematic folder, or schematic page to another library, design, or schematic folder. Only the "pointers" to the attached schematic folders and files—that is, their names and the names of the designs or libraries that contain them—are carried along.

> Attached files work much like their counterparts in email—they do not provide an alternative definition of the part (as do attached schematic folders).

Note: When you attach a schematic folder to a part or hierarchical block, you can specify a full path and filename in the Library text box. So, although you can specify a library that hasn't been saved, you

should not try to descend into the attached schematic folder until the library that contains the schematic folder has been saved.

If you don't specify a full path and filename in the Library text box, Capture expects to find the attached schematic folder in the same design as the part of hierarchical block to which it is attached. If the specified schematic folder doesn't exist in either the design or library, Capture creates the schematic folder when you descend hierarchy on the part or hierarchical block.

For compatibility with future versions of Windows, Capture preserves the case of the path and filename as you specify them in the Library text box.

Note: The Select Entire Net command is restricted to the active schematic page—it doesn't follow hierarchical blocks, hierarchical ports, or off-page connectors across schematic folders or schematic pages. For more information, see Tracing a net.

Remember that nets on a schematic page are electrically connected by name, by alias, or by connection to a named hierarchical port or off-page connector.

To attach a schematic folder to a hierarchical block

1. From the Place menu, choose Hierarchical Block.
2. Enter a name for the hierarchical block in the Name text box.
3. Choose Schematic View as the implementation type, in the Implementation Type list box.
4. Type the name of the schematic folder in the Implementation Name text box.
5. If the schematic folder is not part of the current project, specify the path to the schematic folder in the Library or File Pathname text box.
6. Click OK.
7. Use the cursor to draw the boundaries of the hierarchical block on the schematic page. Capture creates the new hierarchical block and automatically places the hierarchical pins according to the ports that exist in the attached schematic.

   Note: Be careful not to create recursion in your design. Capture

cannot prevent recursion, and the Design Rules Check command does not report it.

Recursion causes Capture to process infinitely as it tries to expand the design, resulting in the loss of any changes you've made to your design since it was last saved.

Creating a hierarchical block from a VHDL model

In Capture, you can create hierarchical blocks from VHDL models for inclusion on your schematic page. Creating hierarchical blocks in this manner is generally termed "bottom-up" design.

To create a hierarchical block from a VHDL model

1. Open the parent schematic page in the schematic page editor.
2. From the Place menu, choose Hierarchical Block (ALT, P, H).
3. Enter a name for the hierarchical block in the Reference text box.
4. Select VHDL as the implementation type in the Implementation Type drop-down list box.
5. Type the entity name for the model in the Implementation name text box.
6. Specify the VHDL file for which you want to create a hierarchical block in the Path and filename text box. Make sure the file is a VHDL type file (*.VHD).
7. Click OK.
8. Use the cursor to draw the boundaries of the hierarchical block on the schematic page. Capture creates the new hierarchical block and automatically places the hierarchical pins according to the port list specified in the VHDL entity.

At this point, the hierarchical block is defined and ready to be "wired in" to the rest of the schematic.

Creating a hierarchical block from a Verilog model

In Capture, you can create hierarchical blocks from Verilog models for inclusion on your schematic page. Creating hierarchical blocks in this manner is generally termed "bottom-up" design.

To create a hierarchical block from a Verilog model

1. Open the parent schematic page in the schematic page editor.
2. From the Place menu, choose Hierarchical Block (ALT, P, H).
3. Enter a name for the hierarchical block in the Reference text box.
4. Select Verilog as the implementation type in the Implementation Type drop-down list box.
5. Type the module name for the model in the Implementation name text box.
6. Specify the Verilog file for which you want to create a hierarchical block in the Path and filename text box. Make sure the file is a Verilog type file (*.V).
7. Click OK.
8. Use the cursor to draw the boundaries of the hierarchical block on the schematic page. Capture creates the new hierarchical block and automatically places the hierarchical pins according to the port list specified in the module section of the Verilog file.

Note: If the port names in the Verilog model have both upper and lower case characters in their identifiers, the property Vlog_Uppercase is attached to the resulting hierarchical block. For more information about Vlog_Uppercase, see the discussion in Verilog tab.

At this point, the hierarchical block is defined and ready to be "wired in" to the rest of the schematic.

6

Establishing connectivity

This chapter covers:

- "Placing and naming wires" on page 238.
- "Auto-wiring the parts on a schematic" on page 240
- "Placing buses and bus entries" on page 247.
- "Placing power, ground, and no connect symbols" on page 255.
- "Making power pins visible" on page 260.
- "Browsing for Power Pins" on page 262.
- "Placing off-page connectors" on page 264.
- "Establishing connectivity amongst schematic pages" on page 269.
- "Using intersheet references" on page 279.
- "Working with nets" on page 290.
- "Using NetGroups" on page 299.

Establishing bus connectivity

To make connections to a bus, you label the bus, label the signals that are members of the bus, and assign an alias to each signal entering and leaving the bus. Each signal bears an alias that is within the bus range. For example, if the bus alias is ADDR[0..3], the four bus members must bear aliases ADDR0, ADDR1, ADDR2, and ADDR3.

In Capture, you can use an alias to connect a signal from one area of your schematic page to another without placing a bus between the areas.

For example, suppose you have placed the bus TIMING[1..4] on your schematic page and you want to connect it to another object at the opposite corner of the schematic page. Instead of drawing a bus from TIMING[1..4] to the other object, you can assign the alias TIMING[1..4] to the other object.

To provide a visual cue that a signal is tied to a bus, you can physically connect the signal to the bus. It is recommended that you use a bus entry for this connection. The advantage of using a bus entry is that two bus entries can be connected at the same point on a bus without connecting the signals. If two wires are run directly to a bus at the same location, the signals are connected.

Establishing wire connectivity

In Capture, you can establish connectivity either with wires or aliases.

Two perpendicular wires or buses are connected if:

- They form a "T" intersection, either by dragging an object or placing a wire.
- A junction is placed where they cross.

If they simply cross at 90 degrees, they are not electrically connected unless you manually place a junction at the intersection.

You can also use an alias to connect a signal from one area of your schematic page to another. For example, suppose you have placed a part on your schematic page and you want to connect it to another part at the opposite corner of the schematic page. Instead of drawing a wire from the first part to the second part, you can assign a single net alias to a wire connected to both parts. You can connect two crossing nets, after they have been placed, by placing a junction where they cross. For more information about placing junctions see Placing junctions.

A net can have any number of aliases plus one optional net name. The only purpose of the netname is to give highest priority to one of a net's aliases. When you assign a name to a net, you force Capture to resolve netname conflicts in favor of a particular alias.

Note: As you place buses and wires, remember the following points:

- A bus and a wire can be connected only by name.

If you begin or end a bus segment on a segment of a wire, a vertex is added to the wire and a junction appears, but the bus and wire are not electrically connected.

If you begin or end a wire segment on a segment of a bus, a vertex is added to the bus and a junction appears, but the wire and bus are not electrically connected.

- Two buses or two wires can be connected physically.

  If you begin or end a bus segment on a segment of another bus, a vertex is added to the second bus, and a junction appears—the buses are connected.

Note: If you begin or end a wire segment on a segment of another wire, a vertex is added to the second wire, and a junction appears—the wires are connected.

Note: If you place parts so that two pins meet end to end, the pins are connected.
OrCAD recommends that you connect the pins of the parts using a wire, and avoid placing parts so that two pins meet end to end. This is because, parts with direct pin to pin connections produce a system generated net name to establish the connection and:

- Capture will not allow you to assign your own net name in the place of the system generated net name.
- Searching for the system generated net name can be difficult if you are not aware of the pin to pin connection.
- If you move the parts after creating the netlist, the system generated net name might change. This may cause net name conflicts when you run backannotation.

Note: OrCAD recommends that you do not connect a power symbol directly to a power pin. Connect the power symbol to the power pin using a wire.

Note: Capture preserves the case of part names and netnames, but ignores the case when comparing names for electrical connection. That means you may use uppercase or lowercase letters as you wish, but you need not remember the case.

Placing and naming wires

This section tells you how:

To place a wire on page 238.

To place a non orthogonal wire on page 239.

To attach a wire to a net on page 239.

The purpose of wires is to create connections. When you connect a wire to a pin, Capture provides visual confirmation: the unconnected pin box on the pin disappears. If two wires cross at 90 degrees, they are not electrically connected unless you create a junction by clicking the left mouse button on one wire as you draw the other to it, or by placing a junction over two crossing wires.

When a wire forms a "T" intersection with a pin or another wire, a visible junction is shown. If the two objects don't intersect, like when a wire ends at a pin or where the next wire begins, then no junction appears.

When you place a wire, it is assigned a system-generated netname. You can replace the system-generated name by assigning an alias or a netname. If you connect a wire to an existing net, the wire assumes the name of that net.

To place a wire

1. From the Place menu, choose Wire.
2. Click the left mouse button to start the wire.

Tip

You can press `F6` to change the cursor to crosshair to start the wire from a specific location.

3. Use the mouse to draw the wire. Click the left mouse button to place a vertex and change directions. The vertex is constrained to multiples of 90 degrees.
4. If the wire ends at a pin or another wire, click the left mouse button to end the wire. The wire appears in the selection color.

or

If the wire doesn't connect to anything, double-click to end the wire.

5. Select the selection tool to dismiss the wire tool.

To place a non orthogonal wire

1. Hold down the SHIFT key while you draw the wire. There is no constraint on vertex angles.

To attach a wire to a net

1. Begin or end the wire on the net.

   or

   Click the left mouse button as you draw the wire over the net.

   or

   Create a net alias as described below, assigning the alias of the net to this wire. Within a schematic page, wires with the same name or alias are electrically connected.

As you place buses and wires, remember the following points:

- A bus and a wire can be connected only by name.

  If you begin or end a bus segment on a segment of a wire, a vertex is added to the wire and a junction appears, but the bus and wire are not electrically connected.

  If you begin or end a wire segment on a segment of a bus, a vertex is added to the bus and a junction appears, but the wire and bus are not electrically connected.

- Two buses or two wires can be connected physically.

  If you begin or end a bus segment on a segment of another bus, a vertex is added to the second bus, and a junction appears—the buses are connected.

Note: If you begin or end a wire segment on a segment of another wire, a vertex is added to the second wire, and a junction appears—the wires are connected.

Note: If you place parts so that two pins meet end to end, the pins are connected.
OrCAD recommends that you connect the pins of the parts using a wire, and avoid placing parts so that two pins meet end to end. This is because, parts with direct pin to pin connections produce a system generated net name to establish the connection and:

- Capture will not allow you to assign your own net name in the place of the system generated net name.
- Searching for the system generated net name can be difficult if you are not aware of the pin to pin connection.
- If you move the parts after creating the netlist, the system generated net name might change. This may cause net name conflicts when you run backannotation.

Note: OrCAD recommends that you do not connect a power symbol directly to a power pin. Connect the power symbol to the power pin using a wire.

Note: When you click on a wire segment, only that segment and its two handles are selected.

Note: Capture preserves the case of part names and netnames, but ignores the case when comparing names for electrical connection. That means you may use uppercase or lowercase letters as you wish, but you need not remember the case.

Shortcut

Tool palette:

Auto-wiring the parts on a schematic

To provide the connectivity on your schematic, you use the wire command to draw wires between the various object on the page. This is often a tedious and time-consuming task. To automate the task of wiring the components on a schematic page, you use the Auto-Wire feature in Capture.

This feature allows you to wire two or more points on the schematic page. It also allows you to wire multiple points on your schematic to a bus.

When wiring the parts on a page, you wire two (or more) pins on different parts or the same part (for shorting). You can create a net between two (or more) wires and you can also create a net between any number of pins and wires on a page.

This section covers the following features of Auto-wiring that allow you to connect the part pins and wires on a schematic page:

"Auto Wire two points" on page 241

"Auto-Wire Multiple Points" on page 242

"Auto-Connect to Bus" on page 243

Auto Wire two points

The auto-wire feature in Capture allows you to connect any two points (part pins and / or wires) on a schematic page.

To wire two points on a page (pin-to-pin, pin-to-wire or wire-to-wire).

1. From the Place menu, choose Auto Wire then choose Two Points.

   Or click the Auto Connect two points button on the Draw toolbar.

   Capture is now in the Auto-Wire mode. Notice the cursor changes to the Auto-Wire cursor.

2. Click the pin or wire to start the net.

   As you move the cursor across the page, notice a wire, from the start pin or wire, is formed. And the wire stretches as you move across the page.

3. Click the pin or wire to end the net.

   A wire is created between the start and end points.

4. Choose the selection tool to exit the Auto-Wire mode or go back to step 2 to Auto-Wire other pairs of pins and wires on the page.

Tip

Use this feature to short two pins on a part.

Shortcut

Draw Toolbar:

Auto-Wire Multiple Points

The Auto-Connect feature of Capture allows you to connect any number of points (pins or wires) on your schematic with an easy-to-use multi-select auto-wiring feature.

To auto-wire multiple points on a page

1. From the Place menu, choose Auto-Wire then choose Multiple Points.

   Or click the Auto Connect multiple points button on the Draw toolbar.

   Capture is now in the Auto-Wire mode. Notice the cursor changes to the Auto-Wire cursor.

2. Click the pin or wire to start the net.
3. Click the next pin or wire on the net.
4. Continue to click on as many pins or wires as required to create the complete net.

   Note: Since you are in the Multiple Point mode, you do not need to press the Ctrl key to multi-select points on the page.

   Note: Since Capture is in the Multiple Point mode a wire is not dragged as you move the cursor across the page. This is unlike the Two-Point Auto Wire mode.

5. Finally, right-click anywhere on the schematic page and choose Connect.

ALTERNATIVELY

1. Click the pin or wire to start the net.
2. Press and hold down the Ctrl key and click the next pin or wire on the route.
3. Continue to click on as many pins or wires as required to create the complete net.

   Note: You need to keep the Ctrl key pressed with each new pin or wire selected.
4. With all the pins and wires in the net selected, right-click anywhere on the schematic page and choose Connect.

Shortcut

Tool palette:

Auto-Connect to Bus

You can use the auto-wiring feature to connect the pins on a part to a bus. You can also connect pins and wires from across the page to a single bus.

In this feature, you simply need to select the pins (and wires) to connect to the bus, choose the Connect to Bus command and finally provide a net alias and all the connections to the bus are made.

To connect Part Pins and / or wires to a Bus

1. From the Place menu, choose Auto Wire then choose Connect to Bus.

   Or click the Auto Connect to Bus button on the Draw toolbar.

   Capture is now in the Auto-Wire mode. Notice the cursor changes to the Auto-Wire cursor.
2. Select any number of pins and / or wires to be connected to the bus.

   Note: Since you are in the Connect to Bus mode, you do not need to press the Ctrl key to multi-select points on the page.

3. Select the bus.

   Note: As soon as you select the bus, the wire connections between the selected points on the page and the bus are created. Notice that the bus entries for these connections are also made.

   When all the connections to the bus are made, you are prompted for the net alias.

   This net alias will be used for all the connections to the bus. So you need to provide a alias name prefix followed by a numeric range in square brackets. So that each net alias in the connections will use name prefix followed by the sequenced numeric.

   Take the example of the following alias name prefix and number range:

   AD [9-0]

   The net aliases will be named AD9, AD8, AD7 through to AD0.

   Note: If you the numeric range that you provide is greater than the number of objects to be connected to the bus, Capture will discard the un-necessary number values.

4. Enter the net alias name prefix followed by the numeric range.

All the connections to the bus are complete along with the number sequenced net aliases.

Important

The auto-connect to bus feature is extremely sensitive to the exact location of the mouse click on the objects (wires or pins) on the schematic. When you use the feature to connect wires to a bus, you need to ensure that you click at the precise end of the wires. Alternatively, when using this feature, you will find it easier to connect the bus directly to the pins on the part.

Shortcut

Tool palette:

Note: Avoid using the Auto-Connect to Bus feature if there is no grid spacing between pins on the component and the bits on the bus.

Auto-Wire to NetGroup

You can use the auto-wiring feature to connect the pins on a part to the component signals on a NetGroup wire. You can also connect pins and wires to the signals on a NetGroup block.

To auto-connect Part Pins and / or wires to a NetGroup wire

1. From the Place menu, choose Auto Wire then choose Connect to Bus.

   Or click the Auto Connect to Bus button on the Draw toolbar.

   Capture is now in the Auto-Wire mode. Notice the cursor changes to the Auto-Wire cursor.

2. Select any number of pins and / or wires to be connected to the bus.

   Note: Since you are in the Connect to Bus mode, you do not need to press the Ctrl key to multi-select points on the page.

3. Select the NetGroup wire.

   As soon as you select the NetGroup wire, the Select Nets dialog box displays the list of all the signals contained in the selected NetGroup with checkbox to the left of each signal.

4. Check on each of the signals in the NetGroup that you want to connect to the pins.

Important

In the Select Nets dialog, you need to select the specific signals within the Netgroup. This implies that selecting the NetGroup name does not ensure that signals contained within the NetGroup are connected to the pins.
ALSO
You should check only as many signals in the NetGroup wire as the number of pins or wire to which you want to connect.

To auto-connect Part Pins and / or wire to the signals in a NetGroup block

1. From the Place menu, choose Auto Wire then choose Two Points.

   Or click the Auto Connect two points button on the Draw toolbar.

   Capture is now in the Auto-Wire mode. Notice the cursor changes to the Auto-Wire cursor.

2. Click the pin or wire to start the net.

   As you move the cursor across the page, notice a wire, from the start pin or wire, is formed. And the wire stretches as you move across the page.

3. Click the NetGroup entry pin on the NetGroup block.

   A wire is created between the pin / wire and the NetGroup entry.

4. Choose the selection tool to exit the Auto-Wire mode or go back to step 2 to Auto-Wire other pairs of pins and wires on the page.

Shorting Part Pins

You often need to short the pins on a part to connect these together. Capture provides the Connect command to short multiple pins on a part.

To short pins on a part

1. Multi-select the pins to be shorted.

   You can do this by clicking on the pins to short while keeping the Ctrl keep pressed. If the pins are on one side of the part, click outside the part and drag the mouse over the pins to be shorted.

2. Right-click and choose Connect.

   All the selected pins are shorted.

Placing buses and bus entries

This section first gives you an overview of buses and bus entries and then tells you how:

"To create a bus" on page 250.

"To place a non orthogonal bus" on page 250.

"To name a bus" on page 251.

"To connect single-signal nets to a bus" on page 251.

A bus is a group of scalar signals (wires), and is never connected to a net. Once a bus acquires a valid name or alias, that name or alias defines the signals carried by the bus and connects those signals to the corresponding nets. For example, the alias A[0:3] defines a four-signal bus that connects the four bus signals A[0], A[1], A[2], and A[3] to the individual wires named A0, A1, A2, and A3. Net aliases on wires do not use brackets.

Note: You can place one pin on a part that represents all the pins for a bus. Such a pin is called a bus pin. Bus pins use the same naming convention as buses.

Note: You can use bus pins in most cases where you can use scalar pins. For example:

- Off-page connectors.
- Hierarchical ports.
- Hierarchical pins of nonprimitive parts and hierarchical blocks.

Bus pins will only work with the VHDL netlist format. No other netlist format understands them. Do not use bus pins in the following situations:

- Pins on primitive parts.
- Any design that you intend to use with PCB Editor.

Like wires, buses can acquire names and aliases by two means:

- Direct application of a valid bus name

- Electrical connection to a hierarchical port, off-page connector, or global bus pin with a valid bus name or alias

In addition to the usual rules by which netnames are resolved, bus names and aliases follow these general rules:

- If one alias defines a subset of the signals defined by another, like-named signals are connected. For example:

  Given aliases A[0..2] and A'[0..5]:

  A[0] connects to A'[0], A[1] connects to A'[1], and A[2] connects to A'[2].

- If the base names differ, or if neither alias defines a subset of the signals defined by the other, signals are connected in a bitwise manner (m to m,. . . , n to n). For example:

  Given aliases A[0..2] and A'[1..3]:

  A[0] connects to A'[1], A[1] connects to A'[2], and A[2] connects to A'[3].

  Given aliases A[0..2] and B[5..0]:

  A[0] connects to B[5], A[1] connects to B[4], and A[2] connects to B[3].

As you place buses and wires, remember the following points:

- A bus and a wire can be connected only by name.

  If you begin or end a bus segment on a segment of a wire, a vertex is added to the wire, but no junction appears—the bus and wire are not connected.

  If you begin or end a wire segment on a segment of a bus, a vertex is added to the bus, but no junction appears—the wire and bus are not connected.

- Two buses or two wires can be connected physically.

  If you begin or end a bus segment on a segment of another bus, a vertex is added to the second bus, and a junction appears—the buses are connected.

  If you begin or end a wire segment on a segment of another wire, a vertex is added to the second wire, and a junction appears—the wires are connected.

Naming conventions for a bus

A bus name must have the form basename[m..n] where m..n specifies a range of decimal integers representing the signal numbers of bus members. There are (n - m + 1) wires in the bus. You can use two periods (..), a colon (:), or a dash (-) between m and n.

Examples:

ADDR[0..31]	(32 members)
DATA[16:31]	(16 members)
CONTROL[4-1]	(4 members)
A[100..190]	(91 members)

Do not add any space between the basename and the left bracket ([), as this can cause problems during the netlist operations.

Also, note that you should not end a bus name with a numeric character (0-9), as this can cause problems during the netlist operations. Numeric characters can occur in other places in the bus name, however. For example, BUS2A will work, but BUSA2 could cause problems when you generate the netlist.

Naming conventions for a bus member

The name of a bus member must have the form basenameN where N is the bus member's signal number in the bus. The signal can have additional aliases, but it must have this name to be connected to the bus.

Also, bus members cannot have a preceding zero in their name. For example, A0 is a legal name for a bus member, but A00 is not.

Note: As you place buses and wires, remember the following points:

- A bus and a wire can be connected only by name.

  If you begin or end a bus segment on a segment of a wire, a vertex is added to the wire and a junction appears, but the bus and wire are not electrically connected.

If you begin or end a wire segment on a segment of a bus, a vertex is added to the bus and a junction appears, but the wire and bus are not electrically connected.

- Two buses or two wires can be connected physically.

  If you begin or end a bus segment on a segment of another bus, a vertex is added to the second bus, and a junction appears—the buses are connected.

  If you begin or end a wire segment on a segment of another wire, a vertex is added to the second wire, and a junction appears—the wires are connected.

Note: Capture preserves the case of part names and netnames, but ignores the case when comparing names for electrical connection. That means you may use uppercase or lowercase letters as you wish, but you need not remember the case.

To create a bus

1. From the Place menu, choose Bus.
2. Click the left mouse button to start the bus.
3. Use the mouse to draw the bus.
4. Click the left mouse button to place a vertex and change directions. The vertex is constrained to a multiple of 90 degrees.
5. Double-click to end the bus.
6. Select the selection tool to dismiss the bus tool or repeat from step 2 to place additional buses.

To place a non orthogonal bus

1. Hold the SHIFT key while you draw the bus. There is no constraint on vertex angles.

   Note: As you place buses and wires, remember the following points:

   - A bus and a wire can be connected only by name.

If you begin or end a bus segment on a segment of a wire, a vertex is added to the wire and a junction appears, but the bus and wire are not electrically connected.

If you begin or end a wire segment on a segment of a bus, a vertex is added to the bus and a junction appears, but the wire and bus are not electrically connected.

- Two buses or two wires can be connected physically.

  If you begin or end a bus segment on a segment of another bus, a vertex is added to the second bus, and a junction appears—the buses are connected.

  If you begin or end a wire segment on a segment of another wire, a vertex is added to the second wire, and a junction appears—the wires are connected.

To name a bus

1. From the Place menu, choose Net Alias. Capture displays the Place Net Alias dialog box.
2. Following the naming conventions for buses, enter the net alias in the dialog box that appears, then click OK. The bus appears in the selection color.
3. Use the mouse to move the net alias and click the left mouse button on the bus to place the net alias. The net alias appears in the selection color. The tip of the pointer must be touching the net for you to place the net alias.
4. Select the selection tool to dismiss the net alias tool. The alias is added to the alias list for the net.

Shortcut

Tool palette:

To connect single-signal nets to a bus

1. Place the bus and assign it a name.
2. From the Place menu, choose the Bus Entry command. The bus entry symbol is attached to your pointer.

3. If the entry is not at the angle you need, then from the Edit menu, choose the Rotate command to rotate the entry 90 degrees counterclockwise.
4. Use the mouse to position one end of the entry on the bus, then click the left mouse button to place the bus entry.
5. Repeat step 4 until all bus entries are placed. If you place the bus entries at regular intervals, you can simplify connecting the single-signal nets to the bus entries.
6. Place a wire to connect the first bus entry to one net, and place an alias, taking care to assign this bus member the lowest value in the bus range.
7. Select the entire wire and press CTRL and drag the wire so that it connects the next net to the bus. Note that the wire is copied to the new location and the alias value is increased by one. However, if you select only an end of the wire (and not the entire wire) and then drag the wire keeping CTRL pressed, the wire is moved to the new location along with the original alias value.
8. From the Edit menu, choose the Repeat command. The wire and the incremented alias are placed at the specified distance from the previous set.
9. Repeat step 8 for every net in the bus or repeat steps 7 and 8 as needed, then select the selection tool to dismiss the set.

Note: You can place one pin on a part that represents all the pins for a bus. Such a pin is called a bus pin. Bus pins use the same naming convention as buses.

Shortcut

Tool palette:

Placing junctions

You create junctions on wires while placing wires, or after the wires have been placed. If you are in the process of placing wires, clicking on another wire creates a junction for the two wires. Use the Place junction tool palette to place junctions on existing wires that cross each other, but don't connect.

Use junctions the same way on buses as on wires.

To create a junction while placing a wire

1. From the Place menu, choose Wire.
2. Click the left mouse button to start the wire. Click the left mouse button to change the direction of the wire as needed.
3. Move the pointer over the wire segment or wire segment vertex you want to connect with, and click the left mouse button. Capture creates a junction where the two wires meet, and ends the wire you are currently placing.

or

➤ If you are connecting with a wire or pin and continuing on across it, double-click the left mouse button when you reach the intersection. Capture creates a junction at the intersection and continues the wire you are currently placing.

To place a junction on existing wires

➤ Choose the Place junction button on the tool palette.

or

1. From the Place menu, choose Junction.
2. Move the pointer over two wires that cross, but do not connect.
3. Click the left mouse button. Capture place a junction where the two wires cross.

Note: You can place a junction on a wire and a pin to connect them when the wire runs perpendicular to the pin. Otherwise, the wire and pin are not connected.

Note: You can also specify the size of the junction dots to be placed on your schematic. The size is specified in the Miscellaneous tab of the Preferences dialog box. You can choose from Small, Medium, Large and Very Large sizes.

To select a junction

➤ Hold the SHIFT key and click to select one or more junctions.

To remove a junction

➤ Choose the Place junction button on the tool palette.

or

1. From the Place menu, choose Junction.
2. Move the pointer over the junction you want to remove.
3. Click the left mouse button. Capture removes the junction. The two wires no longer connect.

or

1. Hold the s key while you move the pointer over the junction you want to remove, and click the left mouse button to select it.
2. From the Edit menu, choose Delete.

or

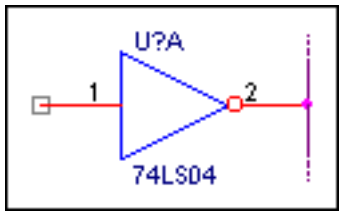
➤ Press the DELETE key. The two wires no longer connect.

Note: If the component is deleted, junction dots residing on the pin-stubs will also get automatically deleted in case that junction is not serving as a connection point to other wires/pins.

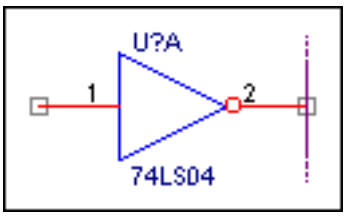
Note: When a wire is dragged, un-necessary junctions will not get created unless the drag results in more than two connections.

Shortcut

Tool palette:
Connected:



Unconnected:



Placing power, ground, and no connect symbols

This section first discusses power, ground, and no connect symbols, then tells you how:

“To place power or ground symbols” on page 256.

“To rotate power or ground symbols” on page 257.

“To create a power or ground symbol” on page 257.

“To isolate a power net to a schematic folder” on page 258.

“To isolate a power net to a schematic page” on page 258.

“To place a no connect symbol” on page 258.

“To remove a no connect symbol” on page 259.

Power and ground symbols

When you place a part that has power and ground pins, the power and ground pins of the part are automatically connected to like-named global power and ground nets of the schematic folder. This happens because, when you place the part, the power and ground pins of the part are assigned a net name that is the same as the pin name. If you need to isolate one power or ground pin from the others, you can assign it a unique net name.

Power and ground pins are invisible and global by default. This means that they are connected, on a project -wide basis, to all pins, power objects, and nets of the same name.

If you need to isolate a power or ground net, do one of the following:

- make the pin visible and connect it to another net or power object
- display the invisible power pin and connect it to a net or power object

For information on making power pins visible and on displaying invisible power pins, see Making power pins visible.

No connect symbols

The Design Rules Check tool checks for unconnected pins. If you intentionally leave a pin unconnected in a schematic page, it needs a no connect symbol. The Design Rules Check tool ignores unconnected pins with no connect symbols.

If a pin with a no connect symbol is connected to a net, the no connect symbol has no effect on the pin and becomes invisible. If the pin is later disconnected from the net, the no connect symbol becomes visible again.

No connects cannot be deleted with the Delete command.

To place power or ground symbols

1. From the Place menu, choose Power or Ground. The Place Power or Place Ground dialog box appears.

2. In the Place Power dialog box, select a power symbol and click OK.

   or

   In the Place Ground dialog box, select a ground symbol and click OK.

3. Use the mouse to move the symbol to the appropriate location and click the left mouse button. The symbol appears in the selection color.

4. Select the selection tool, or press ESC, to dismiss the power or ground tool.

5. Click an area where there are no parts or objects to deselect the symbol.

Note: To place DC ground ('0') symbols in your PSpice designs, see Placing PSpice ground 0 symbols for PSpice simulations.

Shortcut

Tool palette:

To rotate power or ground symbols

1. Select the symbol.

2. From the Edit menu, choose the Rotate command. The symbol rotates 90 degrees counterclockwise.

3. Repeat step 2 as necessary.

4. Click an area where there are no parts or objects to deselect the symbol.

To create a power or ground symbol

1. Open the library that is to hold the new symbol, and select the library in the project manager.

2. From the Design menu, choose the New Symbol command. The New Symbol dialog box appears.

3. Enter a name and select Power as the Symbol Type, then click OK. The part editor opens with an empty part boundary box.
4. Use the graphics tools to create the symbol; the part boundary box dimensions change to accommodate the graphic elements.

To isolate a power net to a schematic folder

1. Place a power symbol and attach it to a hierarchical port.

To isolate a power net to a schematic page

1. Place a power symbol and attach it to an off-page connector.

   When Capture resolves netname conflicts, the name of the off-page connector takes precedence over the name of the power object, and the off-page connector's scope is limited to the schematic folder. All pins on the same page that are connected by name or by wire to the power symbol are connected to the isolated power net.

   For example, say you want to isolate your analog and digital grounds and then connect them at one point when you make a printed circuit board. You place your analog circuitry on a separate schematic folder. On each page in the analog schematic folder, you place a ground symbol with the name GND. This implicitly connects all the pins named GND to ground. Then you connect that power symbol to an off-page connector named AGND. To connect AGND to the digital ground (GND), you can create a part whose footprint is a strip of copper with two pads, GND and AGND.

Note: When you edit a part's graphic representation on a schematic page, you break the connection between the part and the library; if you want to reverse your edits, you use the Replace Cache command of the Design menu. For more information, see Replacing a part.

To place a no connect symbol

1. Press SHIFT, X.
2. Position the mouse pointer over the pin, and click the left mouse button. The end of the pin changes from a square (unconnected) to an X (not connected).

or

1. From the Place menu, choose No Connect.
2. Position the mouse pointer over the pin, and click the left mouse button. The end of the pin changes from a square (unconnected) to an X (not connected).

or

1. Select the pin.
2. From the Edit menu, choose Properties. The property editor appears.
3. Change the filter to <All>.
4. Select the Is No Connect property.
5. Click Apply, and close the property editor.
6. Click the left mouse button in any open space on the schematic page. The end of the pin changes from a square (unconnected) to an X (not connected).

To remove a no connect symbol

1. From the Place menu, choose No Connect.
2. Position the mouse pointer over the pin, and click the left mouse button. The end of the pin changes from an X (not connected) to a square (unconnected).

or

1. Select the pin.
2. From the Edit menu, choose Properties. The property editor appears.
3. Change the filter to <All>.
4. Clear the Is No Connect property.
5. Click Apply, and close the property editor.
6. Click the left mouse button in any open space on the schematic page. The end of the pin changes from a square (unconnected) to an X (not connected).

Making power pins visible

In Capture, power and ground supply pins are referred to generically as "power pins". Normally, power pins are invisible, and global—that is, they are connected to like-named power pins, power objects, and power nets throughout the schematic folder. You can override this default connection by making a power pin visible and connecting it to a wire or other connectivity object. If you connect a power pin to a net using a hierarchical port, or off-page connector, then the pin is no longer global.

Capture can also display invisible power pins on individual part instances or throughout a design. Merely displaying an invisible power pin does not change its global nature; however, connecting a wire or other connectivity object to an invisible power pin isolates it from the design-wide (global) net. If there are duplicates of the pin in the devices of a multi-part package, then all of the pins should be made visible then wired.

To display invisible power pins

Invisible power pins always appear in the part editor. The method by which you display invisible power pins in the schematic page editor determines whether you can connect wires and other connectivity objects to them

On a part instance

1. Select the part in the schematic page editor.
2. From the Edit menu, choose Properties.
3. Find the Power Pins Visible property column on the property editor Parts tab and select the check box, then close the property editor.

Connecting a wire or other connectivity object to a power pin made visible by this method isolates that pin from the design-wide power net.

Throughout a design

1. From the project manager's Options menu, choose Design Properties.

2. In the Design Properties dialog box, choose the Miscellaneous tab.
3. Select the Display Invisible Power Pins option (for documentation purposes only).
4. Click OK.

You cannot connect to a power pin made visible by this method.

To make power pins visible

A power pin is by default connected to a global net that has the same name as the power pin. You can override this default connection by making the power pin visible by either of the methods below and connecting it to a wire or other connectivity object.

On a new part

1. From the part editor's Place menu, choose Pin.
2. In the Place Pin dialog box, change the Type to Power.
3. Verify that the Pin Visible option is selected.
4. Click OK.
5. Place the pin.

   For a power pin that is already placed, select the pin in the part editor. From the part editor's Edit menu, choose Properties. In the Pin Properties dialog box, verify that the Type is Power and that the Pin Visible option is selected, then click OK.

On a part instance

1. Select the part in the schematic page editor.
2. From the Edit menu, choose Part.
3. For each power pin you want to make visible, select the pin, then choose Properties from the Edit menu.
4. In the Pin Properties dialog box, change the Type to Power.
5. Verify that the Pin Visible option is selected.
6. Click OK.

7. When you finish, close the part editor window.
8. In the Save Part Instance dialog box, choose whether to apply your changes to all instances of the part in the design or only the selected (current) instance.
9. Click OK.

Note: When you edit a part's graphic representation on a schematic page, you break the connection between the part and the library; if you want to reverse your edits, you use the Replace Cache command of the Design menu. For more information, see Replacing a part.

Browsing for Power Pins

In Capture, power and ground supply pins are referred to generically as "power pins". Normally, power pins are invisible, and global this means they are shorted by name or they are connected to like-named power pins, power objects, and power nets throughout the schematic folder.

However, if you need to change the shorting behavior on the pins, you would need to make the visible and then work on the pin properties.

Alternatively, you can view the list of all the power pins in a schematic design and then edit the power names or define them as NC pins.

To browse the power pins in a design

1. Select the design in the Project manager.
2. On the Edit menu choose Browse - Power Pins.
3. In the Browse Properties dialog box, you can choose the mode as occurrences or instances and click OK.

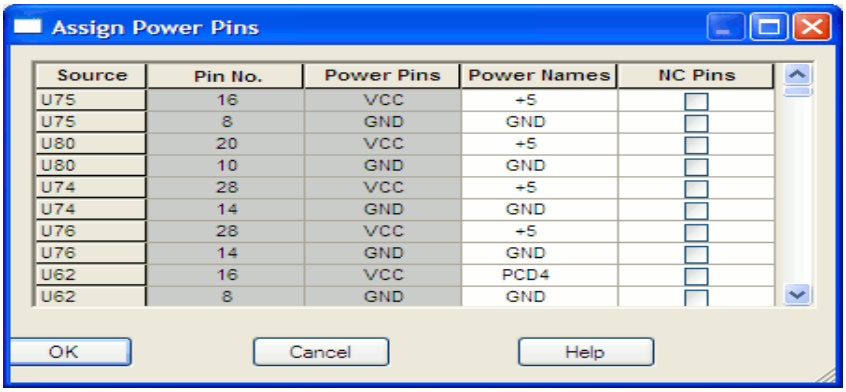
This list displays all the power pins in this design.

If you double-click on a line item in this list, you are directed to the component containing the selected power pin. However, since the pins are all invisible, you are still not able to make any changes to the pin properties.

To change the properties of a power pin

1. Click the power pin list.
2. On the Edit menu choose the Properties option (Or Press Ctrl + E).

   The list of power pins now displays in the Assign Power Pins dialog.



You can now use the Power Name property on a pin to change the shorting behavior on the pin. This implies that you can change the power name of a pin.

To change the power name of a pin

1. Pick another power name from the drop-down list on the Power Names cell of a selected Power pin.

OR

1. Type an alternative power name in the power name cell.

You can also define a power pin as an NC pin by checking the NC Pin option.

The functionality allows you to work with and change the power name and NC Pin property of power pins without having to first make the pins visible.

Note: If you set the NC Pins property of a part, the property Editor for the part will reflect this change by adding an NC_PINS property line item.

Placing off-page connectors

This section discusses placing off-page connectors, then tells you how:

- To connect schematic pages laterally (within the schematic folder) on page 264.
- To create a hierarchical port or off-page connector on page 265.

Off-page connectors provide connection between schematic pages within the same schematic folder. An off-page connector is connected by name to other off-page connectors within the same schematic folder.

Note: Like-named off-page connectors in different schematic folders are not connected.

Note: The Select Entire Net command is restricted to the active schematic page—it doesn't follow hierarchical blocks, hierarchical ports, or off-page connectors across schematic folders or schematic pages. For more information, see Tracing a net.

Note: Remember that nets on a schematic page are electrically connected by name, by alias, or by connection to a named hierarchical port or off-page connector.

Note: To connect an off-page connector to a bus, name the off-page connector with the same name and range as that of the bus. For example, to connect an off-page connector to a bus named `ABC[0:3]`, name the off-page connector as `ABC[0:3]`.

To connect schematic pages laterally (within the schematic folder)

1. From the Place menu, choose Off-Page Connector.
2. Select a symbol (standard or user-created), enter a name, and choose OK.
3. Place the symbol anywhere on the schematic page.
4. Repeat steps 1 through 3 for the other schematic pages (within the same schematic folder) you wish to connect.

The size of a part or a symbol is limited to 32 by 32 inches.

To create a hierarchical port or off-page connector

1. Open the library that will hold the new symbol.
2. From the Design menu, choose New Symbol. The New Symbol Properties dialog box appears.
3. Enter a name and select off-page connector or hierarchical port as the symbol type, then click OK. The part editor opens with an empty part boundary box.
4. Use the graphics tools to create the symbol. The symbol dimensions expand automatically to accommodate the graphics.
5. From the File menu, choose Save. If you are creating the symbol in a new library that has not yet been saved, the Save As dialog box appears, giving you the opportunity to name the library file.

Note: If you edit a library provided by OrCAD, it is important that you assign a new library name so that your changes are not overwritten when you upgrade or update your software.

Note: When you save a project, Capture automatically creates a backup with a .DBK file extension. When you save a library, Capture automatically creates a backup with a .OBK file extension. If you save only a schematic page or a part, no backup is generated.

Adding hierarchical ports

Hierarchical ports and hierarchical pins provide connection between levels of hierarchy on a schematic page.

Inside a hierarchical block, a hierarchical pin provides vertical (downward-pointing) connection only. It is connected by name to hierarchical ports on schematic pages within the attached schematic folder or to the appropriate signals in the VHDL entity port definitions. You can think of its function as bringing a net "up" from the attached implementation into the hierarchical block (but not out onto the schematic page).

Outside a hierarchical block, a hierarchical port provides vertical (upward pointing) and lateral connection. It's connected vertically to the like-named hierarchical pin inside any hierarchical block to which it is attached. It's connected laterally to like-named nets, hierarchical

ports, and off-page connectors within the same schematic folder. You can think of its function as carrying a net out of the schematic folder.

Before you create or resize a hierarchical block, make sure the Snap to grid option is turned on (from the schematic page editor's Options menu, choose Preferences). If the hierarchical block is on Fine grid, then hierarchical pins inside it are also on Fine grid—even if you change the Snap to grid setting before you place them—and it may be difficult to connect to these off-grid hierarchical pins.

A part with an attached schematic folder functions exactly as described for hierarchical blocks, and pins on such a part function exactly as described for hierarchical pins within a hierarchical block. You can use the same attached schematic folder for either method of defining a hierarchy. The only difference between the two methods is that a part with an attached schematic folder is easier to reuse. See Creating parts and assigning properties for related information.

If you choose the Descend Hierarchy command on a nonprimitive part or hierarchical block, and Capture cannot find the attached implementation, Capture creates a schematic folder or VHDL model in the active design.

If you attach an existing implementation to a hierarchical block, Capture automatically creates the hierarchical pins that correspond with the schematic folder's hierarchical ports or the VHDL models port definitions. If you descend hierarchy on a hierarchical block whose implementation doesn't yet exist, then Capture automatically creates the hierarchical ports (for schematics) or port definitions (for VHDL models) that correspond with the hierarchical pins of the hierarchical block.

Note: If you attach external schematic folders or other files to hierarchical blocks in a design or parts in a library, be sure to include the attachments when you pass the design or library to a board fabrication house or to another engineer. Attached schematic folders and other files are not carried along automatically when you copy or move a part, schematic folder, or schematic page to another library, design, or schematic folder. Only the "pointers" to the attached schematic folders and files—that is, their names and the names of the designs or libraries that contain them—are carried along.

Attached files work much like their counterparts in email—they do not

provide an alternative definition of the part (as do attached schematic folders).

Note: When you attach a schematic folder to a part or hierarchical block, you can specify a full path and filename in the Library text box. So, although you can specify a library that hasn't been saved, you should not try to descend into the attached schematic folder until the library that contains the schematic folder has been saved.

If you don't specify a full path and filename in the Library text box, Capture expects to find the attached schematic folder in the same design as the part of hierarchical block to which it is attached. If the specified schematic folder doesn't exist in either the design or library, Capture creates the schematic folder when you descend hierarchy on the part or hierarchical block.

For compatibility with future versions of Windows, Capture preserves the case of the path and filename as you specify them in the Library text box.

Note: The Select Entire Net command is restricted to the active schematic page—it doesn't follow hierarchical blocks, hierarchical ports, or off-page connectors across schematic folders or schematic pages. For more information, see Tracing a net.

Remember that nets on a schematic page are electrically connected by name, by alias, or by connection to a named hierarchical port or off-page connector.

To connect pages vertically (through a hierarchical block)

If necessary, place the hierarchical block and attach the implementation (see Creating hierarchical blocks for instructions). Complete these steps to bring the net into the hierarchical block:

1. Bring the net into the hierarchical block:
2. Select the hierarchical block.
3. From the Place menu, choose Hierarchical Pin.
4. Enter a name and choose OK.
5. Place the symbol within the boundaries of the selected hierarchical block.

This hierarchical pin is downward pointing—it is connected to any like-named hierarchical port on any schematic page in the attached schematic folder.

To finish the procedure, carry the net up to the hierarchical block:

6. Open a schematic page contained in the schematic folder attached to the hierarchical block mentioned above.
7. Make sure no hierarchical block is selected.
8. From the Place menu, choose Hierarchical Port.
9. Select a symbol, enter the name used in step 3 of the preceding sequence, and choose OK.
10. Place the symbol anywhere (except inside a hierarchical block) on the schematic page.

    This hierarchical port is upward pointing—it is connected to any like-named hierarchical pin inside any hierarchical block to which it is attached.
11. If necessary, use off-page connectors to carry the net to other schematic pages in the same schematic folder (see Placing off-page connectors for instructions).

Note: Be careful not to create recursion in your design. Capture cannot prevent recursion, and the Design Rules Check command does not report it.

Recursion causes Capture to process infinitely as it tries to expand the design, resulting in the loss of any changes you've made to your design since it was last saved.

Note: You can use the copy and paste keyboard shortcuts (CTRL+C and CTRL+V) to enter the same name in the Name text field of both dialog boxes.

To connect hierarchical ports or off-page connectors with nets

➤ Extend the net to the hierarchical port or off-page connector by placing a wire or bus.

or

1. Select the hierarchical port or off-page connector and choose Properties from the Edit menu.
2. In the Name text box or Value text box, type the name of the net, and click OK.

or

1. Select the hierarchical port or off-page connector's name and choose Properties from the Edit menu.
2. In the Name text box or Value text box, type the name of the net, and click OK.

Establishing connectivity amongst schematic pages

This section discusses establishing connectivity amongst schematic pages, then tells you how:

- To extend a net across schematic pages within a single schematic folder on page 271.
- To extend a net through a hierarchy on page 271.

In Capture, you connect schematic folders and schematic pages by extending nets between them, using off-page connectors, hierarchical blocks, and hierarchical ports. Off-page connectors carry nets between schematic pages within a single schematic folder. Hierarchical blocks and hierarchical ports carry nets between schematic folders.

A part with an attached schematic folder functions exactly as described for hierarchical blocks, and pins on such a part function exactly as described for hierarchical ports within a hierarchical block. You can use the same attached schematic folder for either method of defining a hierarchy. The only difference between the two methods is that a part with an attached schematic folder is easier to reuse. See Creating parts and assigning properties for related information.

If you choose the Descend Hierarchy command on a nonprimitive part or hierarchical block, and Capture cannot find the attached schematic folder, Capture creates a schematic folder in the active design.

The following topics describe how the connections work and how you use them:

- Creating hierarchical blocks
- Adding hierarchical ports

Note: Hierarchical ports also connect schematic pages laterally—they are connected by name to off-page connectors and hierarchical ports within the same schematic folder.

Note: The Select Entire Net command is restricted to the active schematic page—it doesn't follow hierarchical blocks, hierarchical ports, or off-page connectors across schematic folders or schematic pages. For more information, see Tracing a net.

Remember that nets of a schematic page are electrically connected by name, by alias, or by connection to a named hierarchical port or off-page connector.

Note: Capture preserves the case of part names and netnames, but ignores the case when comparing names for electrical connection. That means you may use uppercase or lowercase letters as you wish, but you need not remember the case.

When you attach a schematic to a part or a hierarchical block, you can specify a full path and filename in the Library text box. So, although you can specify a library that hasn't been saved, you should not try to descend into the attached schematic folder until the library that contains the schematic folder has been saved.

If you don't specify a full path and filename in the Library text box, Capture expects to find the attached schematic folder in the same design as the part of the hierarchical block to which it is attached. If the specific schematic folder doesn't exist in either the design or library, Capture creates the schematic folder when you descend hierarchy on the part or hierarchical block.

For compatibility with future versions of Windows, Capture preserves the case of the path and filename as you specify them in the Library text box.

To extend a net across schematic pages within a single schematic folder

1. Open the schematic page editor on a page that contains the net.
2. From the Place menu, choose the Off-Page Connector command.
3. Select a symbol and enter a name in the Name text box; then click OK.
4. Connect the off-page connector to the net, either by name or by wire.
5. For each schematic page on which the net resides (and within the same schematic folder), repeat steps 1 through 4, using the same name for each off-page connector you place.

To extend a net through a hierarchy

1. Open the schematic page editor on the parent page.
2. Place a hierarchical block, then assign a name to the hierarchical block.

   or

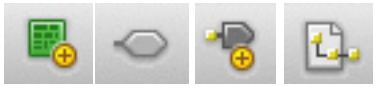
   Place a nonprimitive part.
3. If necessary, attach a schematic folder to the hierarchical block or part.
4. If you placed a hierarchical block in step 2, then from the Place menu, choose the Hierarchical Pin command and assign the pin a name.
5. Open a schematic page in the attached schematic folder.
6. Place a hierarchical port using the Hierarchical Port command with the same name of the hierarchical pin you used in step 4, then place wires to connect the hierarchical port to the net.
7. Repeat steps 4 through 6 for each hierarchical pin in the hierarchical block, or for each pin on the part.

Note: Be careful not to create recursion in your design. Capture cannot prevent recursion, and the Design Rules Check command does not report it.

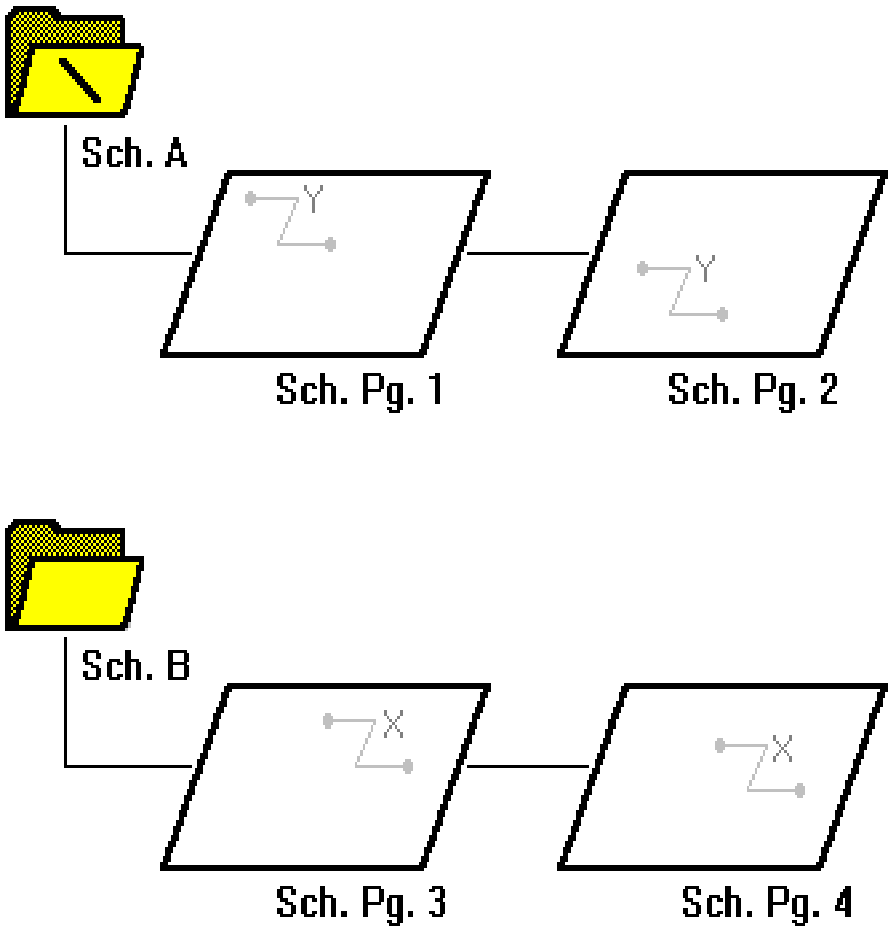
Note: If you attach external schematic folders or other files to hierarchical blocks in a design or parts in a library, be sure to include the attachments when you pass the design or library to a board fabrication house or to another engineer. Attached schematic folder and other files are not carried along automatically when you copy or move a part, schematic folder, or schematic page to another library, design, or schematic folder. Only the "pointers" to the attached schematic folders and files—that is, their names and the names of the designs or libraries that contain them—are carried along.

> Attached files work much like their counterparts in email—they do not provide an alternative definition of the part (as do attached schematic folders).

Shortcuts

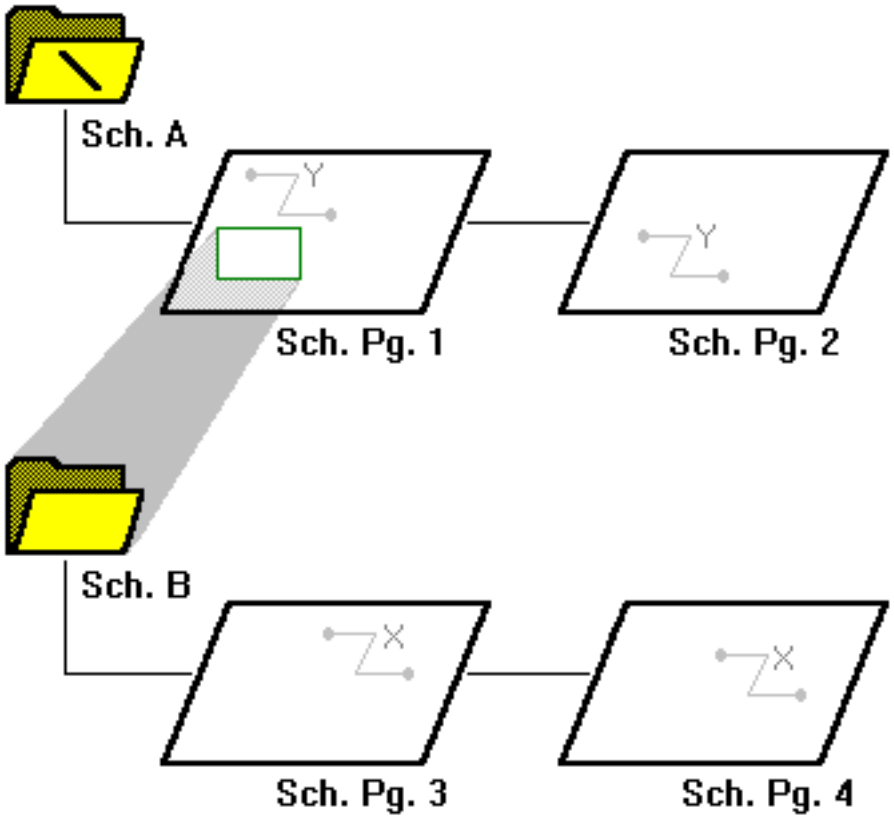
Tool palette: 

Example



This figure shows two schematic folders, A and B, with two schematic pages each. The schematic folder marked with a backslash (\) is

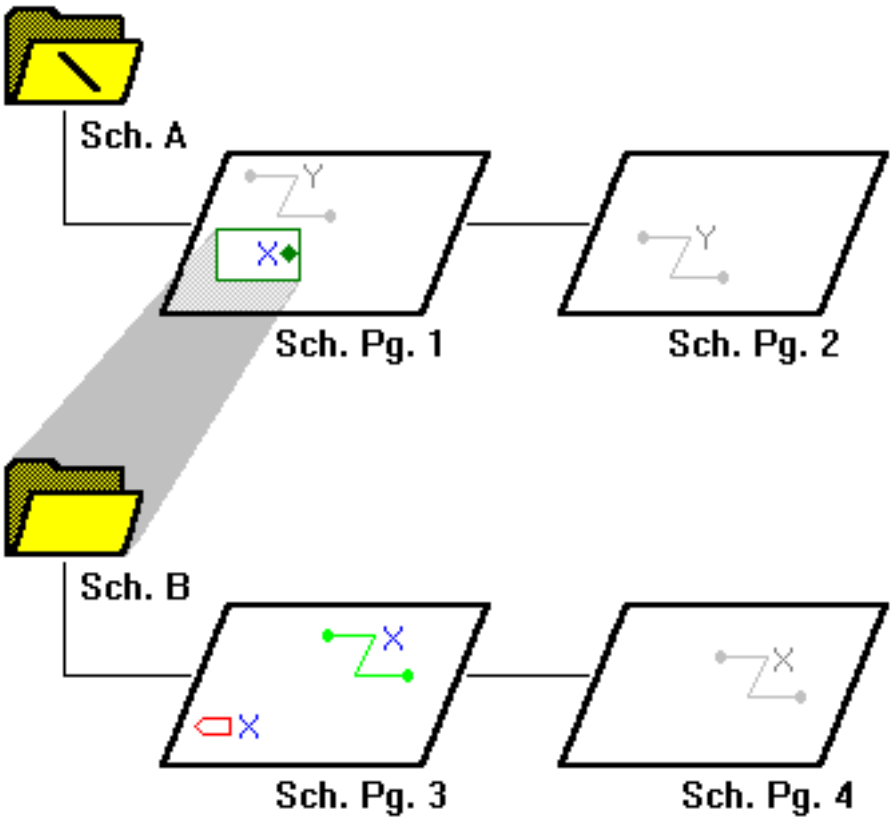
called the root schematic folder. In this demonstration, you see how to create a simple hierarchy.



To establish the hierarchy with schematic folder A "above" schematic folder B:

1. Place a hierarchical block on schematic page 1.

2. Attach schematic folder B.



To carry a net between schematic folders A and B:

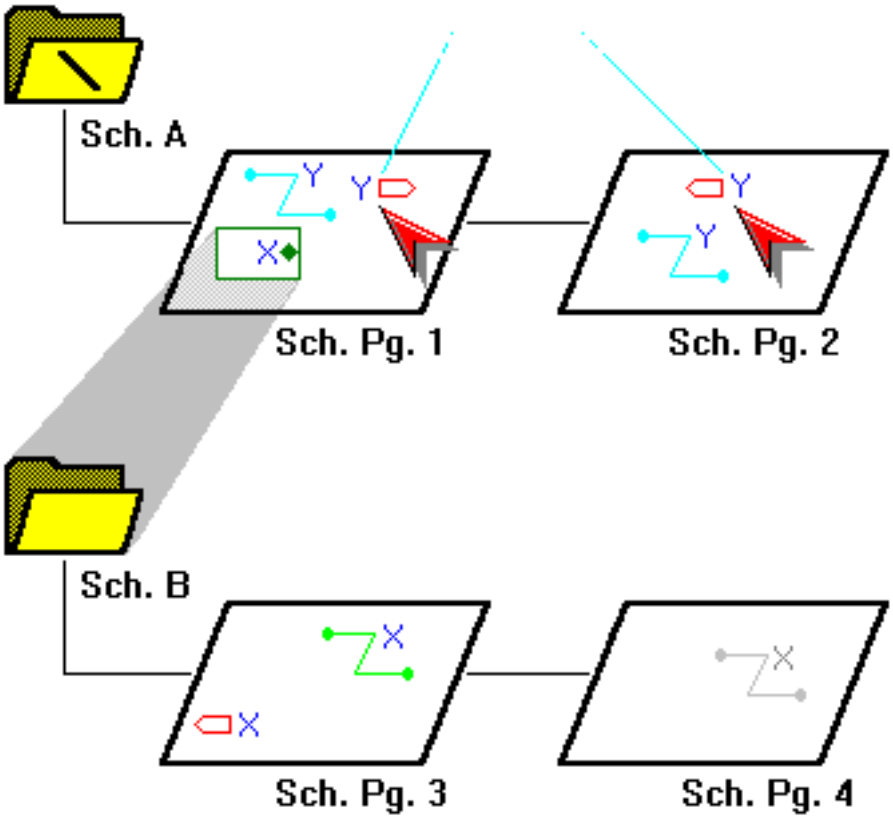
1. Select the hierarchical block on schematic page 1 and place a hierarchical pin named X inside it.

   This hierarchical pin is a point of attachment for electrical connections between the hierarchical block and other objects on schematic page 1.

2. Place a hierarchical port named X on schematic page 3.

   This hierarchical port is a point of attachment for electrical connections between schematic page 3 and other schematic

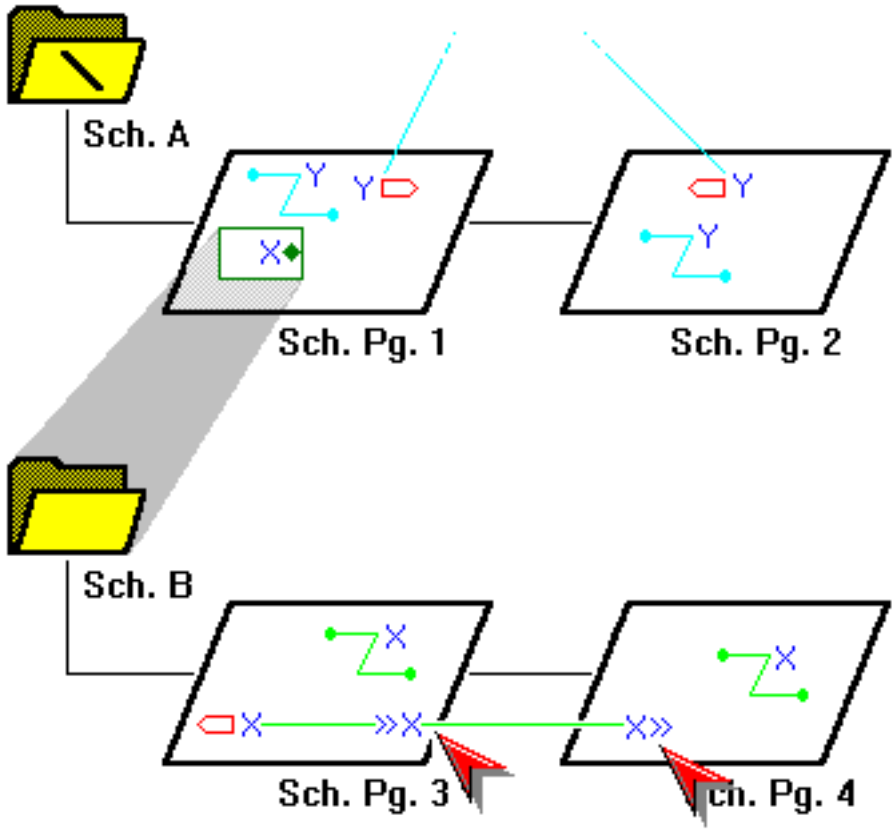
pages. It is connected by name to the hierarchical pin inside the hierarchical block on schematic page 1.



Hierarchical ports generally carry a net "up" through a hierarchy. In the root schematic folder, they usually represent external signals such as physical connectors on a PC board.

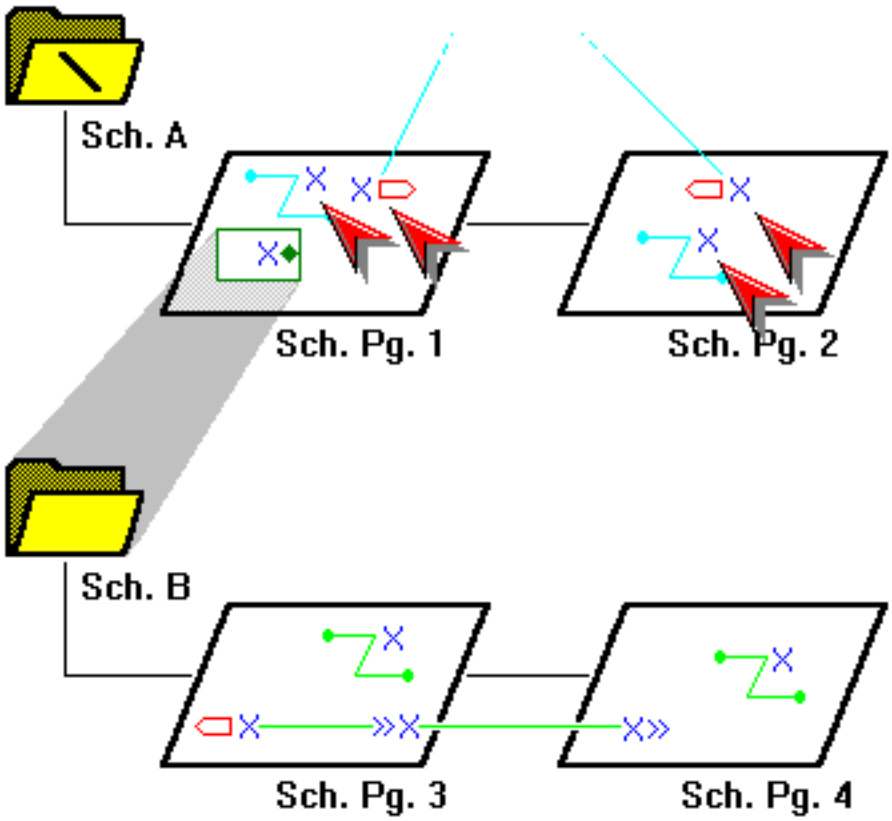
Note that hierarchical ports in schematic folder A are electrically connected by name, so any like-named connectivity objects on schematic pages 1 and 2 are part of a single net named Y. You could

make either one (but not both) of these hierarchical ports an off-page connector without affecting the electrical connections.



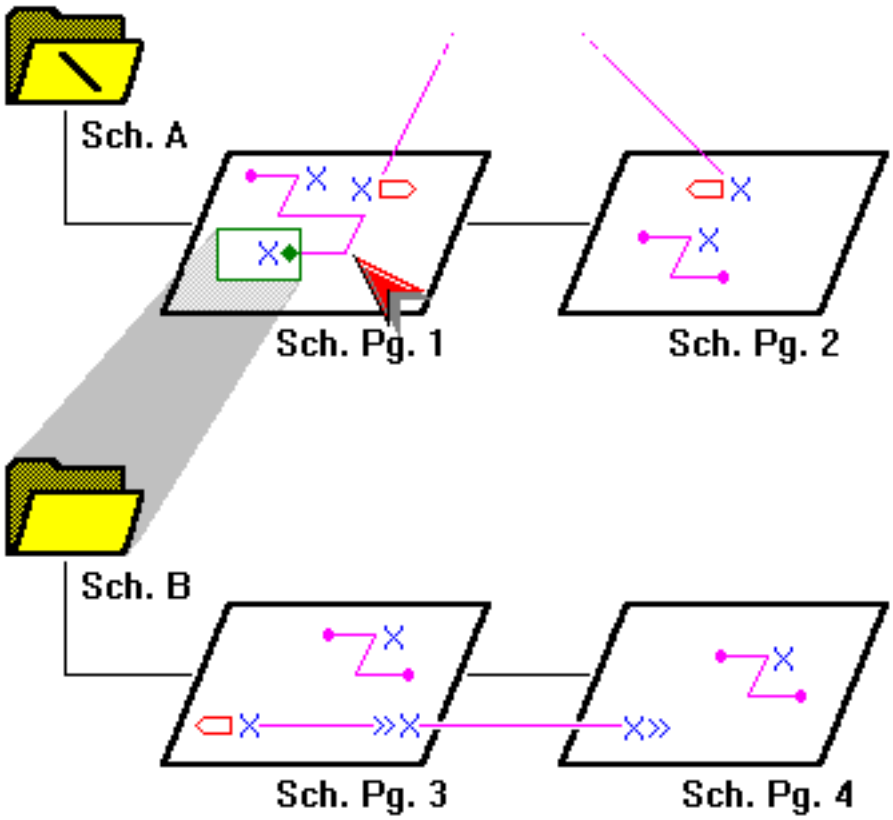
To connect the schematic pages in schematic folder B, place an off-page connector named X on both schematic pages 3 and 4. Any

like-named connectivity objects on schematic pages 3 and 4 are part of a single net named X.



To connect the X and Y nets, it is not enough simply to rename one set of objects, as shown here. Again, the hierarchical pin doesn't

bring the "green" net X out of the hierarchical block and onto the schematic page.



When you physically connect any part of the "blue" net X to the hierarchical pin inside the hierarchical block, the nets are joined.

Using intersheet references

This section introduces intersheet references in Capture, then covers the following topics:

- Intersheet references in a flat design on page 280
- Intersheet references in a hierarchical design on page 282
- Creating Intersheet references on page 283
-
- Signal Navigation in Capture on page 288

■ Reporting Intersheet References on page 288

Intersheet references indicate the source and destination of schematic page and schematic signals in your design, making it easier to trace signals and find errors in the electrical connectivity of your design. Compare this to off-page connectors, which are used for signals between schematic pages within the same schematic, or hierarchical ports, which are used for signals between schematics.

An intersheet reference for an input signal indicates all the schematic pages from which the signal originates; an intersheet reference for an output signal indicates all the schematic pages to which the signal goes.

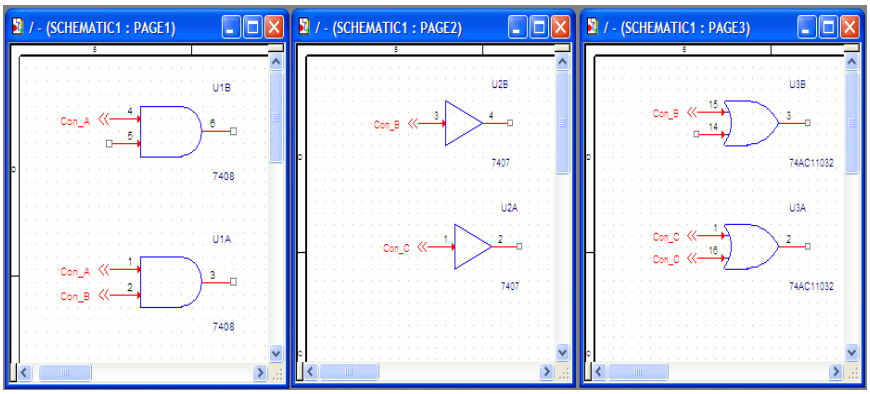
For example, an output hierarchical port with intersheet references 35, 42, and 61 indicate that the signal goes to schematic pages 35, 42, and 61.

Note: Intersheet references work with a flat design, simple hierarchy or complex hierarchy.

Intersheet references in a flat design

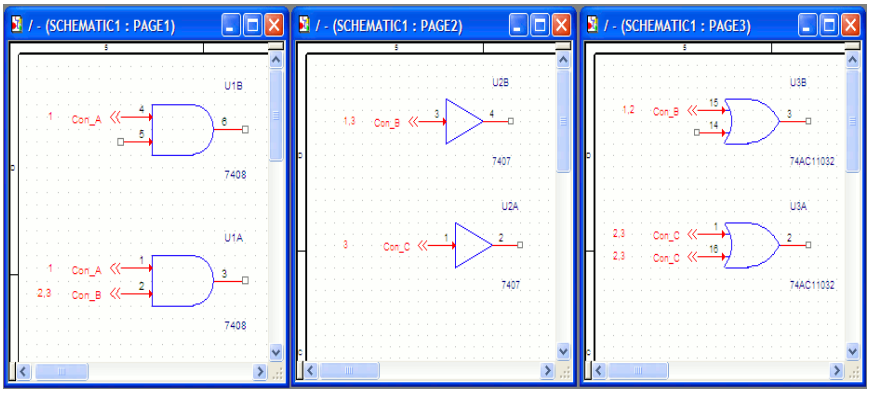
For every off-page connector on the pages of a flat design, the intersheet reference of its port will be attached to that connector.

Take the example of the following flat design that contains three pages.



Note the off-page connectors (con_A, Con_B and Con_C) used to the parts across the three pages.

Notice the output if you create intersheet references to trace the signals across the pages of this design:



Con_A:

Since the two connectors lie on Page 1, the intersheet references are defined as 1 for both connectors.

Con_B

On Page 1 the reference is defined as 2,3. This implies that the signals for this connector exist on Page 2 and Page 3.

Similarly, if you see the Con_B reference on Page 2 is 1, 3 and the reference on Page 3 is 1,2.

Con_C

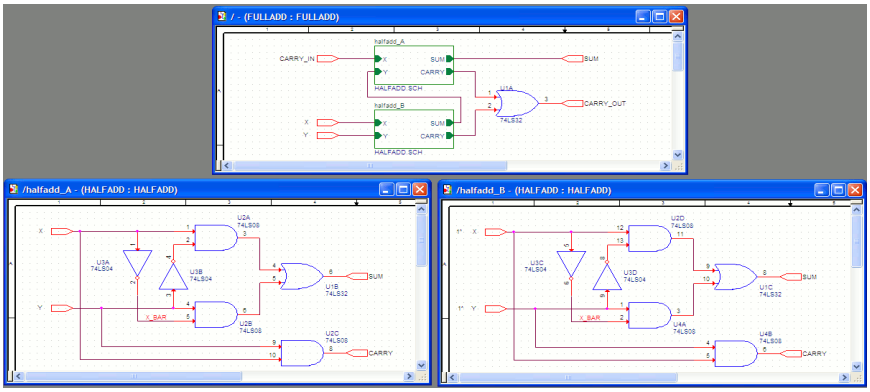
The Page 2 reference for Con_B is 3 since the signals for exist on Page 3. Now the Page 3 reference for both Con_C connectors on Page 3 show as 2,3. This implies a signal exists on Page 2. Also, another signal for this connector exists on Page 3 itself.

Note: The page numbers defined in an intersheet reference are derived from the page numbers defined in the page title block.

In a design containing a large number of pages and signals, you use signal navigation facility in Capture to navigate connected signals across pages on your design.

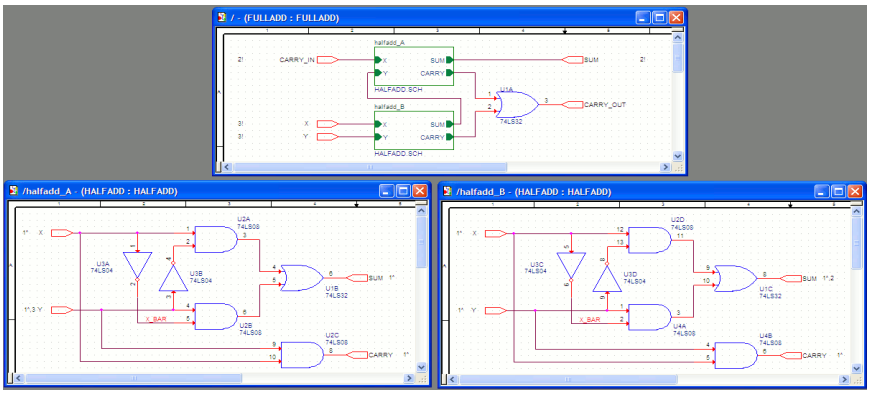
Intersheet references in a hierarchical design

Take the example of the FULLADDER design that contains two occurrences of the HALFADD hierarchical blocks.



Note that the hierarchical blocks on the FULLADD page are connected to the two HALFADD pages via hierarchical ports.

Notice the output if you create intersheet references to trace the signals across the pages of this design:



CARRY_IN (FULLADD)

The intersheet reference for the CARRY_IN port on the FULLADD page is defined as 2!. This implies that the signal for this port is on page two of the design (halfadd_A). Also, the exclamation (!) symbol implies that the connected signal exists one level lower in the hierarchy.

X (FULLADD)

The reference for the X port on the FULLADD page is defined as 3!. This indicates that the connecting signal is on page 3 (halfadd_A). And the exclamation symbol implies that the connecting signal exists one level lower in the hierarchy.

X (halfadd_A)

The intersheet reference for the X port on the halfadd_A page is defined as 1^. This indicates that the connected signal exists on page 1 (FULLADD). Also, the caret (^) symbol implies that the connecting signal exists one level higher in the hierarchy.

Y (halfadd_A)

The reference for the Y port on the halfadd_A page *1^,3* defines that one connecting signal exists on page 1 (FULLADD) and the caret symbol indicates that this signal exists one level higher in the hierarchy. The second connecting symbol exists on page 3 (halfadd_B). Similarly, the intersheet reference for the SUM port on the halfadd_B page is 1^,2.

In a complex design containing a large number of pages and signals, you use signal navigation facility in Capture to navigate connected signals across pages on your design.

Note: A port must be connected to a pin of a hierarchical block to ensure that the ^ and ! symbols will be displayed with the intersheet references for the port. These symbols will not be displayed if the port is connected to a part that is not primitive.

Creating Intersheet references

To add intersheet references

1. From the Tools menu, choose Intersheet References.

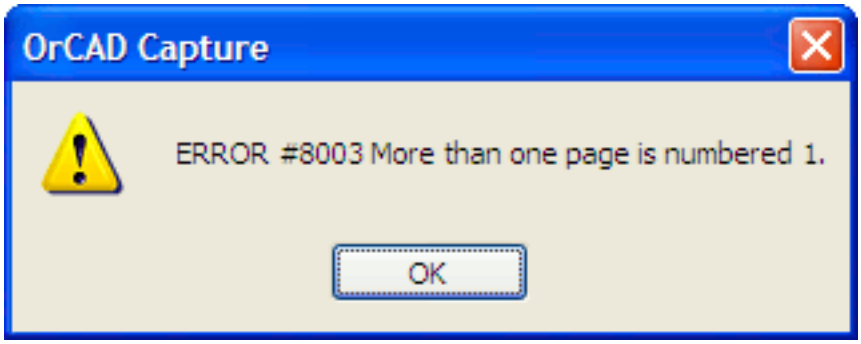
   The Intersheet References dialog box displays.

You can also access this dialog box by choosing the Annotate option on the Tools menu. Then in the Annotate dialog box select the Add Intersheet References option and click OK.

2. Select the Place On Off-Page Connectors option if you want the intersheet references placed on off-page connectors.
3. Verify that the value used for X Offset is correct. This option adjusts the horizontal spacing between the port name and the intersheet reference. Increase the value to increase the separation.
4. Select or clear the option in the Port Type Match Matrix group box as necessary to specify how port types are to match each other when creating intersheet references.
5. Click OK. Capture performs error checking on your design while it generates intersheet references.
6. To generate a report of the interesheet references of the selected design, select the View Report option and specify the name of a CSV file in which you want to create the report.

   Note: Use the Intersheet references command, with the option to generate a CSV output file, this file will be available in the Outputs folder in the Project manager.
7. If any design errors are encountered during the creation of intersheet references, a message box appears asking if you want to view the errors or warnings in the session log. Choose either the Yes button or the No button, as appropriate. If no design errors are encountered during report creation, the intersheet references are added to your design.

Note: When running the Intersheet References command you encounter the following error. This is caused if the page numbers (as defined by the Page Number property of the page title block) are duplicated. You can resolve this issue either by re-annotating your design (choose the Annotated command from the Tools menu) or by manually editing the Page Numbers on the title blocks on the pages in your design.



To remove intersheet references

1. From the Tools menu, choose Annotate. The Annotate dialog box appears.
2. Select Delete Intersheet References, and click OK. All intersheet references are removed from the design.

Guidelines for Creating Intersheet References

When generating intersheet references for a design, Capture uses a number of rules. The following set of guidelines will help you understand the details of how the intersheet references are generated and points you need to keep in mind when running this command.

1. **Same name Off-page connector and Port**

   If an off-page connector and a port on the same page have the same name, no intersheet reference will be generated if another off-page connector or port of this name does not exist on another page. Also, two warning messages will be logged for the two un-connected signals.

2. **Hanging Off-page Connectors**

   If a page contains two off-page connectors that are not connected to any pin (know as hanging off-page connectors), the intersheet references for these two off-page connector will be generated. However, if these hanging off-page connectors exist on different pages, the Intersheet references will not be

generated. Also, two warning messages will be generated for the two un-connected signals.

3. Placing Intersheet References

When placing an intersheet reference, if the net symbol is a left port or off-page connector, the IREF will be displayed to the right of the graphical lines. If the net symbol is a right port or off-page connector, the IREF will be displayed to the left of the graphical lines.

4. Zone Information for Port

The zone information will not be displayed for a port that is inherited from a hierarchical pin. However, the zone information will displayed if that signal is routed to another page.

5. Multiple Occurrence Port

If a port has multiple occurrences, then all the pages are appended to the IREF property for each occurrence of the port.

6. Bus Intersheet References

If a design has two buses and the hierarchical ports on these bus are EN2[7..0] and EN2[0..7], then one intersheet reference will be displayed for each port showing connectivity between the two buses. However, a warning will be displayed in the session log that the hierarchical port EN[7..0] appears twice on the same page.

If an off-page connector with the name A[15:0] is connected to a hierarchical port with the pin name A[0:3], then pin A0 on the hierarchical block is mapped to A15. This implies that the flatnet name for this pin is A15 and not A0.

If the off-page connector name is A[15:0], then intersheet references are generated on pages that have flatnets with names A0, A1 through A15.

If an off-page bus is placed on the top page of a design and another off-page bus on another page of the design, then the intersheet references will be generated only if the appropriate bus bits are specified on the off-page defined in the latter page of the design. To verify this, you need to open the property editor for each bus bit and check the schematic net and flatnet name defined for the bit.

7. Grid Display Option

If an off-page connector is connected to a hierarchical pin, in Intersheet References grid display option, the grid information is not displayed with the port.

8. Port Page Number Append

The port page number will be added to an off-page connector intersheet reference only when the net connected to the off-page is connected to a part pin and a is port connected to the same net on the other page.

9. Generate Intersheet References

The following matrix provides snapshot of the scenarios for Intersheet References:

Scenario	IREF Generated
Port is a bus, Bus bit is a port or net name equals to bus bit	YES
Port is a bus, Bus bit is an off-page connector or net name equals to bus bit	NO
Off-Page connector is a bus, bit is an off-page connector or net name equals to bus bit	NO
Port is a bus and bus with same name exists	YES
Off-page connector is bus and bus with same name exists	YES
Same port name exists on same page	YES
Same off-page connector name exists on the same page	YES

Signal Navigation in Capture

You can use the signal navigation feature in Capture to navigate the connected signals on a design. This feature allows you to select a signal that you want to trace. Capture then browses for all the connected signals on the design. Finally, you can select and highlight the signals from the browse list.

To find and navigate the signals on a design

1. Select the off-page connector, hierarchical port, net or bus to find its connecting signals.
2. Right-click and choose the Signals option from the pop-up menu.
3. A browse list appears with all the signals that are connected to the currently selected signal.

Object ID	Name	Page	Page Number	Schematic	Part Pin
CARRY_IN(Port)	CARRY_IN	FULLADD	1	FULLADD	halfad...
halfadd_A/X(Port)	CARRY_IN	HALFADD	2	HALFADD	U2A.1...

4. Double-click on a signal in this list to navigate to the connected signal.

Note: When you select to view the signals of a bus, the signal list contains the bus entries on the selected bus. However, the signal navigation does not connect to any bus with the same name on different pages. For example, if you choose a bus with the off-page connector defined as D[0..5] and the bus contains the bits D1 to D5, the list will display these bits. However it will not show any connectivity to another bus with the same off-page connector (D[0..5]) defined.

Reporting Intersheet References

When you create the intersheet references for a design, the Intersheet References dialog box contains an option to create a report file (in CSV format). This report file provides a complete list of all the connected signals on your design.

The following report file sample is generated from the FULLADD design.

	A	B	C	D	E	F	G	H	I	J
1	Name	Type	Page	Page Number	Schematic	PartPin	LocationX	LocationY	Zone	IREF
2	SUM	Output	FULLADD	1	FULLADD	halfadd_A.SUM	560	240	5B	5B2!
3	SUM	Output	HALFADD	2	HALFADD	U1B.6	540	200	5B	1^
4	X	Input	FULLADD	1	FULLADD	halfadd_B.X	220	340	2B	1A3!
5	X	Input	HALFADD	3	HALFADD	U2D.12,U3C.5,U4B.5	60	130	1A	1^
6	Y	Input	FULLADD	1	FULLADD	halfadd_B.Y	220	360	2C	1B3!
7	Y	Input	HALFADD	3	HALFADD	U3D.9,U4A.1,U4B.4	60	250	1B	1^
8	CARRY_IN	Input	FULLADD	1	FULLADD	halfadd_A.X	220	240	2B	1A2!
9	X	Input	HALFADD	2	HALFADD	U2A.1,U3A.1,U2C.10	60	130	1A	1^
10	CARRY	Output	HALFADD	2	HALFADD	U2C.8	520	320	5B	1^
11	CARRY	Output	HALFADD	3	HALFADD	U4B.6	520	320	5B	1^
12	CARRY_OUT	Output	FULLADD	1	FULLADD	U1A.3	560	310	5B	Property Not Present
13	SUM	Output	HALFADD	3	HALFADD	U1C.8	540	200	5B	1^,1B2
14	Y	Input	HALFADD	2	HALFADD	U3B.3,U2B.4,U2C.9	60	250	1B	1^,5B3

As an example, see the following two selected rows from the report:

4	X	Input	FULLADD	1	FULLADD	halfadd_B.X	220	340	2B	1A3!
5	X	Input	HALFADD	3	HALFADD	U2D.12,U3C.5,U4B.5	60	130	1A	1^

Name is the name of the port or off-page connector.

Type is the signal type.

Page defines the page on which the port or off-page connector exists.

Page Number are the page numbers as defined by the Page Number property of the title block on that respective page.

Schematic is the schematic folder containing the specific pages.

PartPin is the part and pin combination connected to the port or off-page connector.

LocationX is the X-axis location on the schematic page grid of the port or off-page connector.

LocationY is the Y-axis location on the schematic page grid of the port or off-page connector.

Zone is the zone location on the schematic page grid of the port or off-page connector.

IREF is the reference of the connected signal. Notice in the first item the reference is 1A3!. This means that the connected signal exists on the 1A zone of page 3 of the design and one level lower in the hierarchy.

Note: After you run the Intersheet References command, with the option to generate a CSV output file, this file will be available in the Outputs folder in the Project manager.

Working with nets

This section covers:

Net operations on page 290.

Assigning net aliases on page 293.

Tracing a net on page 295.

A net is all of the wires, buses, parts, and symbols that are logically connected via net names, net aliases, off-page connectors, and hierarchical ports.

Net operations

This section discusses net operations, then tells you how:

To find and select a net on page 291.

To edit a net's properties on page 292.

To delete a net on page 292.

A net is one or more wires that are physically connected or that have been connected by a net alias, a hierarchical port, or an off-page connector. In addition, all like-named power pins, power objects, and attached wires throughout the project constitute a net, unless they have been isolated.

You can edit a discrete wire, a wire segment, or you can edit the net as a whole. You can also easily edit or add to the properties of multiple nets. See To update part or net properties for more information.

To find and select a net

1. In the project manager, select the schematic folder or schematic pages that you wish to search.
2. From the Edit menu, choose the Browse command, and then select the Nets command from the pull right menu. The browse window displays a list of all nets by name and by alias.

   OR

   From the Edit menu, choose the Browse command, and then select the Flat Netlist command from the pull right menu. The browse window displays a list of the nets that appear in netlists.

   OR

   From the Edit menu, choose the Find command, and then type an asterisk (*) in the Text to Search text box and click the Find button. The Find window displays a list of all nets by name and by alias.
3. From the list, double-click on the name of the desired net. The schematic page editor opens with the net appearing in the selection color.
4. Press the right mouse button to display the pop-up menu.
5. From the menu, choose the Select Entire Net command. All net segments on the active page appear in the selection color.

Note: The Select Entire Net command is restricted to the active schematic page—it doesn't follow hierarchical blocks, hierarchical ports, or off-page connectors across schematic folders or schematic pages. To do this you can use the Signal Navigation in Capture or by Tracing a net

Tip

The status bar displays the net name of a selected net or wire.

Remember that nets on a schematic page are electrically connected by name, by alias, or by connection to a named hierarchical port or off-page connector.

To edit a net's properties

1. Select a segment on the net.
2. From the Edit menu, choose the Properties command. The property editor appears.
3. Change the filter to Capture.
4. Use the property editor to edit, add, or remove properties as necessary.

To delete a net

1. Select the net.
2. Press the right mouse button.
3. From the context-sensitive menu that appears, select the Select Entire Net command.
4. Press the DELETE or BACKSPACE key.

Note: As you place buses and wires, remember the following points:

- A bus and a wire can be connected only by name.

  If you begin or end a bus segment on a segment of a wire, a vertex is added to the wire and a junction appears, but the bus and wire are not electrically connected.

  If you begin or end a wire segment on a segment of a bus, a vertex is added to the bus and a junction appears, but the wire and bus are not electrically connected.

- Two buses or two wires can be connected physically.

  If you begin or end a bus segment on a segment of another bus, a vertex is added to the second bus, and a junction appears—the buses are connected.

  If you begin or end a wire segment on a segment of another wire, a vertex is added to the second wire, and a junction appears—the wires are connected.

Note: Capture preserves the case of part names and netnames, but ignores the case when comparing names for electrical connection.

That means you may use uppercase or lowercase letters as you wish, but you need not remember the case.

Assigning net aliases

This section discusses assigning net aliases, then tells you how:

To create a net alias on page 293.

To assign a netname on page 294.

To edit a net alias on page 294.

To move net alias text on page 294.

To display the net alias at multiple locations on page 295

A net is not required to have an alias, but by using an alias, you can establish connectivity.

Within a schematic page, a net with an alias is connected to any net with the same alias, or to any off-page connector, hierarchical port, or global pin with the same name.

A net alias differs from a netname in that a net can have numerous aliases, but it can have only one name. When the Create Netlist tool resolves the conflict between the various aliases attached to a net, the net alias has the highest priority; so by assigning a netname, you can determine the final name of your net.

When you place a wire, it is assigned a system-generated name. When you place a net alias on the wire, the system-generated name is replaced by the alias.

A net's alias is visible at the location where you place the alias, You may find it useful to label the net throughout your project.

To create a net alias

1. From the Place menu, choose the Net Alias command.
2. Enter the net alias text in the dialog box that appears, then click OK. A rectangle representing the net alias is attached to the pointer.

3. Use the mouse to move the net alias and click the left mouse button on the wire to place the net alias. The net alias appears in the selection color. The tip of the pointer must be touching the net for you to place the net alias.
4. Select the selection tool to dismiss the net alias tool. The alias is added to the alias list for the net.

Shortcut

Tool palette:

To assign a netname

1. Select the wire.
2. From the Edit menu, choose the Properties command. The Property editor window opens to the Schematic Nets tab.
3. Change the entry in the Name column to one of the existing net aliases and close the property editor.

To edit a net alias

1. Select the net alias.
2. From the Edit menu, choose the Properties command.
3. In the dialog box that appears, you can change the color, the font, the rotation and the alias itself.
4. Click OK to dismiss the dialog box.

To move net alias text

1. Select the net alias text on a net. An handler appears around the net alias text.
2. Drag the net alias text handler to the location (on the same net) where you want to place it.

   Note: You can not move a net alias outside of a net segment.
3. Drop the net alias handler. The net alias text appears in the new location on the net.

To display the net alias at multiple locations

1. Select the portion of net where you want the alias to be visible.
2. From the Edit menu, choose the Properties command. The property editor appears.
3. Click the New button. The Add New Property dialog box appears.
4. Assign a name, such as NAME1, to the new property. Do not assign a value at this time. Click OK to dismiss the Add New Property dialog box.
5. Select the cell of the new property, and click the Display button.
6. Select the Value Only Display Format option, and click OK.
7. Click Apply, and then close the property editor.
8. Repeat steps 1 through 7 for each location where you want the alias to appear, assigning another property name (NAME2, NAME3 . . .) at each location.
9. Use the Update Properties tool (see To update part or net properties) to assign the net's alias as the value to the properties NAME1, NAME2, NAME3 . . .

Note: Capture preserves the case of part names and net names, but ignores the case when comparing names for electrical connection. That means you may use uppercase or lowercase letters as you wish, but you need not remember the case.

Tracing a net

This section discusses tracing a net, then tells you how:

To find a net using a name on page 296.

To locate and highlight all wires of a net on a single page on page 296.

To trace a net across pages of a schematic folder on page 297.

To trace a net between schematic folders on page 297.

When you need to trace a net, you may not know all the net aliases or how many schematic pages the net touches. Using Capture, you can overcome these problems and find every portion of the net. You'll need to start with a portion of the net selected in the schematic page editor, or with a netname, an off-page connector name, or a hierarchical port name. If you start with a name, use the Power Pins command of the project manager to locate a portion of the net.

The actions involved in tracing a net can be done in any order. Typically, you locate a part of the net, highlight all portions of the net on the same schematic page, follow the net onto other schematic pages in the same schematic folder, and then follow the net into other schematic folders.

Note: You can trace a signal in a design by using the Signal Navigation in Capture.

To find a net using a name

1. In the project manager, select the schematic folder that holds the name. If you do not know which schematic folder holds this portion of the net, select all schematic folders (press CTRL while you click on a schematic folder to add it to the selection set).
2. From the Edit menu, choose the Find command. The Find toolbar displays.
3. In the Text to Search text box, enter the name, with wildcards if you wish, in the Search options drop-down list and specify that this is the name of a net, an off-page connector, or a hierarchical port.
4. Click the Search button to initiate the search. A list of all objects which match your search criteria appears in the Find window.
5. Double-click on an item in the Find window. The schematic page editor opens with the net or off-page connector or hierarchical port selected.

To locate and highlight all wires of a net on a single page

1. Click over a wire of the net to select the wire.
2. Click the right mouse button to display the pop-up menu.

3. From the menu, choose the Select Entire Net command. All wires of the net appear in the selection color. You may need to zoom out to see the entire net.

Note: The Select Entire Net command is restricted to the active schematic page—it doesn't follow hierarchical blocks, hierarchical ports, or off-page connectors across schematic folder or schematic pages. For more information, see Tracing a net.

Remember that nets on a schematic page are electrically connected by name, by alias, or by connection to a named hierarchical port or off-page connector.

To trace a net across pages of a schematic folder

1. Locate and highlight all wires of the net on one page.
2. Scan the selected net for off-page connectors and for hierarchical ports not inside a hierarchical block. For each off-page connector or hierarchical port,
   - ❑ Note the name.
   - ❑ Activate the project manager and select the current schematic folder.
   - ❑ From the Edit menu, choose the Find command.

   The Find toolbar displays with the Find text box selected.
   - ❑ In the Text to Search text box, enter the name, select Off-Page Connectors, then click the Find button. The Find window displays a list of off-page connectors with the specified name.
   - ❑ For each entry in the Find window, double-click on the entry. The schematic page editor opens with the off-page connector appearing in the selection color.
   - ❑ Repeat step 2, selecting Hierarchical Ports in the Find pop-up list on the Find toolbar.

To trace a net between schematic folders

1. Locate and highlight all wires of the net on one page.

2. Scan the selected net for hierarchical ports not inside a hierarchical block. For each port:

   - ❑ Note the name.
   - ❑ Activate the project manager and select all schematic folders except the active one.
   - ❑ From the Edit menu, choose the Find command.
   - ❑ In the Text to Search text box, enter the name, select Hierarchical Ports, then click Find. The Find window displays a list of hierarchical ports with the specified name.
   - ❑ For each entry in the Find window, double-click on the entry. The schematic page editor opens with the hierarchical port appearing in the selection color.

Note: As you place buses and wires, remember the following points:

- ❑ A bus and a wire can be connected only by name.

  If you begin or end a bus segment on a segment of a wire, a vertex is added to the wire and a junction appears, but the bus and wire are not electrically connected.

  If you begin or end a wire segment on a segment of a bus, a vertex is added to the bus and a junction appears, but the wire and bus are not electrically connected.

- ❑ Two buses or two wires can be connected physically.

  If you begin or end a bus segment on a segment of another bus, a vertex is added to the second bus, and a junction appears—the buses are connected.

  If you begin or end a wire segment on a segment of another wire, a vertex is added to the second wire, and a junction appears—the wires are connected.

Note: Capture preserves the case of part names and netnames, but ignores the case when comparing names for electrical connection. That means you may use uppercase or lowercase letters as you wish, but you need not remember the case.

Note: When you attach a schematic folder to a part or hierarchical block, you can specify a full path and filename in the Library text box. So, although you can specify a library that hasn't been saved, you

should not try to descend into the attached schematic folder until the library that contains the schematic folder has been saved.

If you don't specify a full path and filename in the Library text box, Capture expects to find the attached schematic folder in the same design as the part of hierarchical block to which it is attached. If the specified schematic folder doesn't exist in either the design or library, Capture creates the schematic folder when you descend hierarchy on the part or hierarchical block.

For compatibility with future versions of Windows, Capture preserves the case of the path and filename as you specify them in the Library text box.

Using NetGroups

This section covers:

NetGroup on page 299.

Named NetGroup on page 301.

Unnamed NetGroup on page 311.

Components of a NetGroup Block on page 315.

Netlising NetGroup Designs on page 316.

NetGroup Connectivity on page 318.

NetGroup

A NetGroup is a collection of nets. The nets in a NetGroup can be scalar, vector or a combination of both. You can create a NetGroup that consists only of nets (like a bus). You can also create a NetGroup that consists of nets (scalar and / or vector), consists of buses and consists of other NetGroups.

By definition, a NetGroup is a completely heterogeneous collection of nets. Unlike a bus, that is a homogeneous collection of nets (scalar or vector), a NetGroup provides a greater flexibility in grouping nets together.

For example, you can collect together a large number of signals on a page of a schematic into a NetGroup. You create an off-page connector and then connect all the signals on the NetGroup to the signals on another page.

Note: While a NetGroup provides greater flexibility for net grouping than a bus, there will be many situations where a bus will be a sufficient implementation of the required functionary. So care should be taken not to assume that the NetGroup completely overrides the functionality and value of a bus.

To create a NetGroup, you use the following objects (that are NetGroup-aware):

- Off-page connector
- Port
- Bus Wire
- Pin
- Global

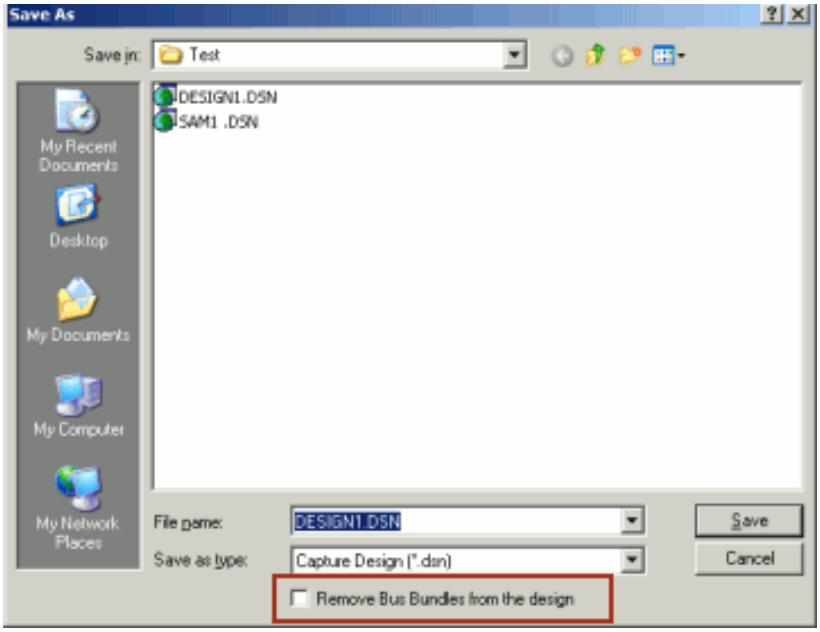
When you create a NetGroup and define a property for the NetGroup, this property is inherited by all the constituent nets of the NetGroup.

You can create two types of NetGroups, a **named** NetGroup or an **unnamed** NetGroup.

Important

When you add a NetGroup to a design, the design database version is upgraded to v16.5. This implies that the design can now not be opened in any version of Capture prior to v16.5. However, you can choose to remove all the NetGroups from a design (if you need to open the design in

a previous version), by choosing Save As from the File menu and clicking the Remove NetGroups from the design checkbox.



Named NetGroup

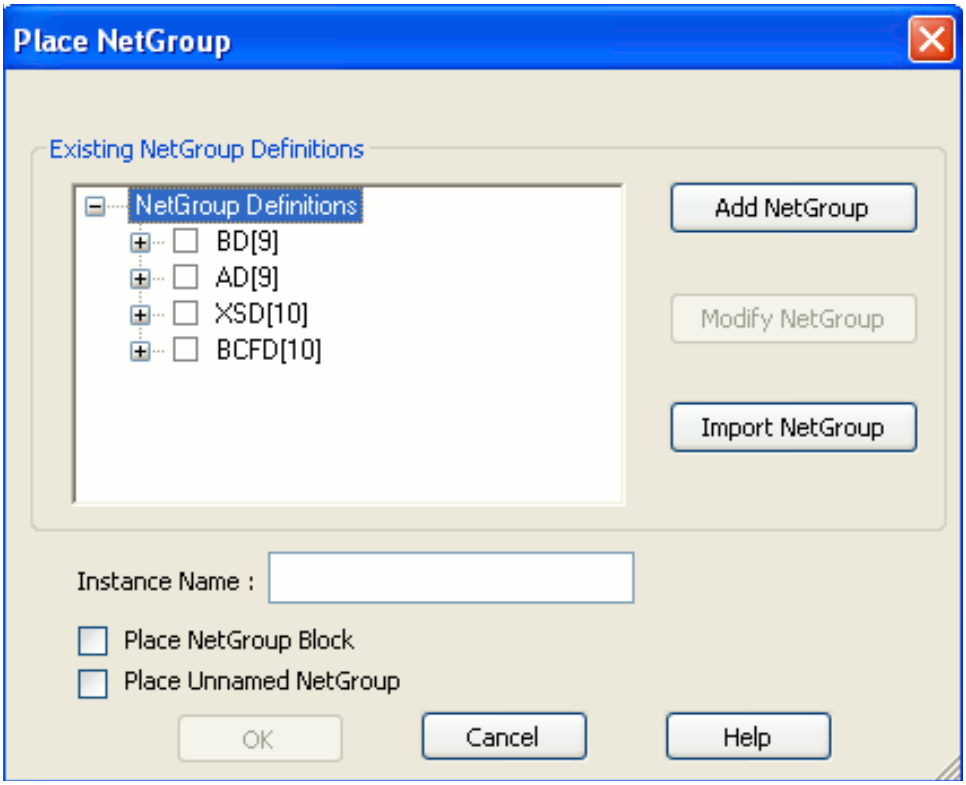
When you create a named NetGroup, you need to specify the associated NetGroup definition and then specify a name for the NetGroup. This type of NetGroup is persistent and can be instantiated across a design. The NetGroup can also be exported as a library and then instantiated and used in other designs. However, if you need to create a NetGroup for one-time use, you create an unnamed NetGroup. For details on unnamed NetGroups see Unnamed NetGroup.

To create a named NetGroup

1. Choose NetGroup from the Place menu in Capture.

   The Place / Create NetGroup dialog displays.

You use this dialog box to build associated NetGroup definitions that you can use anywhere in your design.



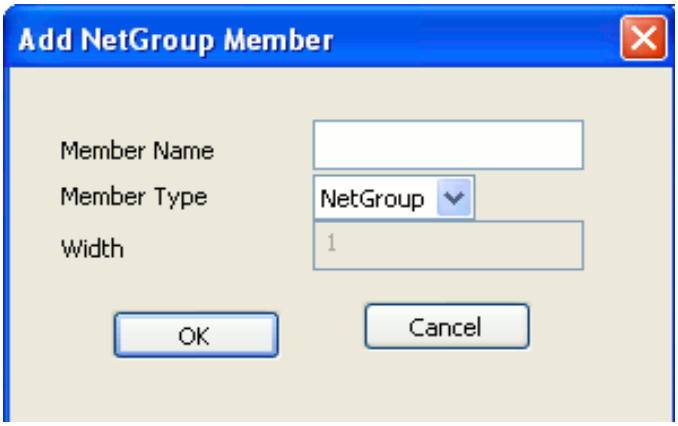
2. To specify a new associated NetGroup definition, click the Add NetGroup button.

   The Add new associated NetGroup definition dialog displays.

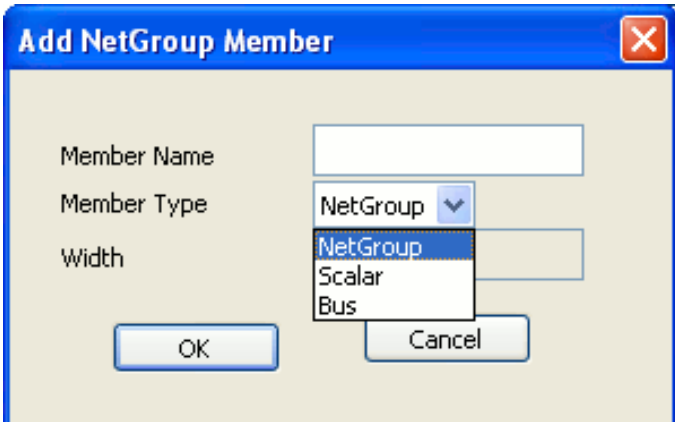
3. In the NetGroup Name text box, enter the name of the NetGroup and click Apply.
4. To add a new NetGroup member, click the Add button.

   Note: The Add button is disabled until you specify the NetGroup name and click Apply.

The Add NetGroup Member dialog displays.



You can add NetGroups, buses or scalars as members of a NetGroup.



If you add a NetGroup or a bus, you need to also specify the width of the member. For example, if you add a NetGroup named AD that contains two signals, you will specify the name as AD[0..1]. The same holds true for buses.

Note: If you add a NetGroup as a member to a NetGroup, the new NetGroup is also available for use as a NetGroup on its own. So in the New NetGroup dialog, you will see the new associated NetGroup definition.

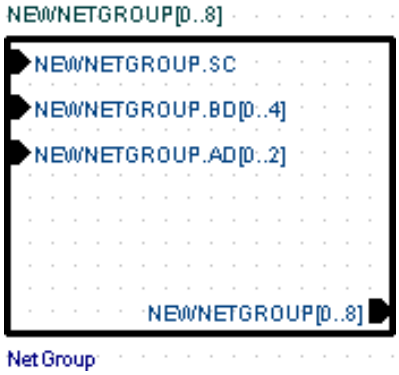
Caution

A bus or scalar signal cannot be directly added to more than one NetGroup. This implies that you cannot add the same bus or scalar to multiple NetGroups but you can add a NetGroup containing a bus or a scalar to multiple NetGroups.

In the New NetGroup dialog, you can also **rename** or **delete** existing NetGroup memebrs. You can also **move** the existing memebrs **up** and **down**.

You move the positions of the members of a NetGroup, up or down to specify the position they will appear when you place the NetGroup on a page.

So, in this example, if you want the scalar member, SC, to appear below the member BD in the block, you will need to move can either move SC down or move BD up.



To rename a NetGroup member

1. In the New NetGroup or Modify NetGroup dialog, select the NetGroup member to rename.
2. Click the Rename button.

   The Rename NetGroup Member dialog displays.
3. Type a new name for the member and click OK.

Note: When you rename a NetGroup member that is either a NetGroup or a bus, you need to ensure that you only change the name of the member. This implies, in the rename procedure, you cannot change the width of the member.

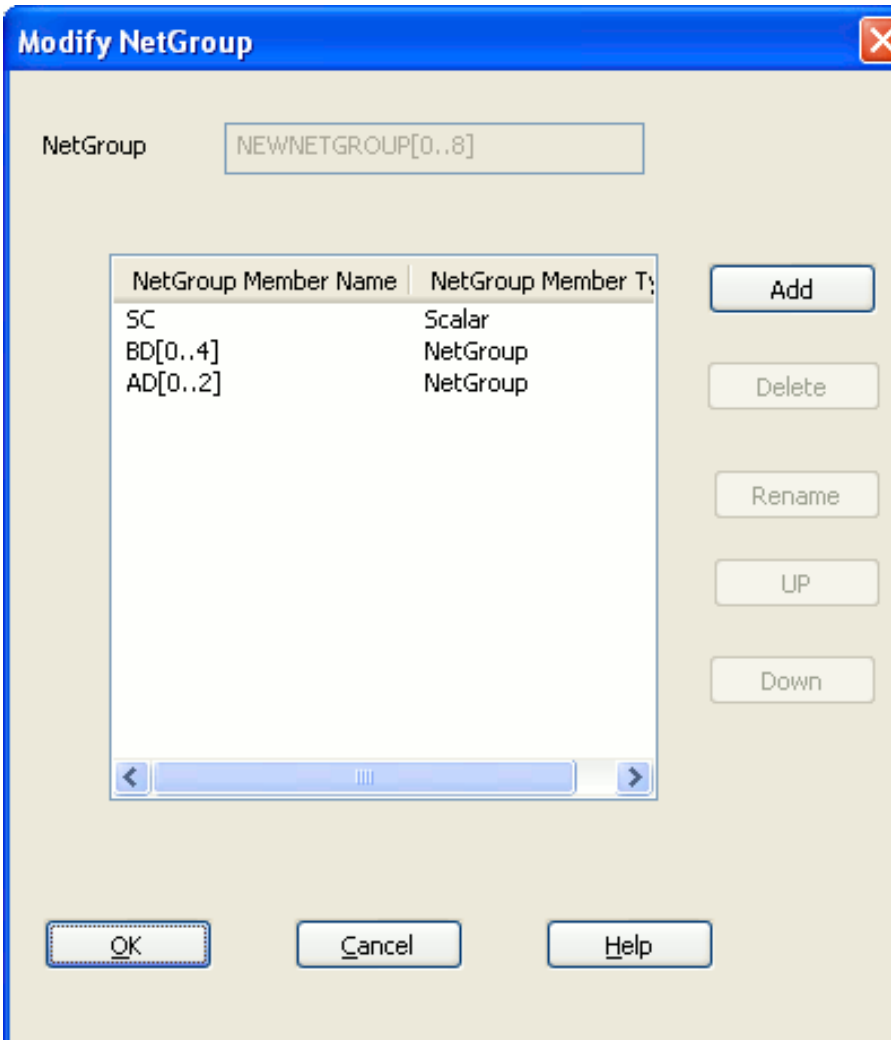
Note: When you rename a NetGroup member that is a NetGroup, you need to rename the NetGroup to the name of an existing NetGroup not already contained within the current NetGroup.

To modify a named associated NetGroup definition

1. To open the NetGroup dialog, choose NetGroup from the Place menu.
2. Click the check-mark next to the NetGroup you want to modify and click the Modify button.

   Note: You need to click the check-mark next to the name of the NetGroup. Selecting the NetGroup name will not make the

NetGroup available for edit.



When you modify an associated NetGroup definition, you can add, delete or rename members. You can also move the positions of the existing members up and down. However, you cannot change the name of the member.

Copy and Paste a NetGroup from one design to another

You can use the Capture Copy and Paste commands to copy a NetGroup from one design to another. This functionality is the same as for other schematic page objects.

When you copy a NetGroup to another design, the associated NetGroup definition is also copied. This means that if you open the NetGroup dialog, you will see the associated NetGroup definitions now available for use in the new design.

Also, if you copy and paste a NetGroup into another design and NetGroups of the same name exist in the destination NetGroup, the NetGroups in the destination design will not be overwritten.

Exporting and Importing Associated NetGroup Definitions

You can export the NetGroups defined in a design to an associated NetGroup definition Xml file. These NetGroups can then be imported and then used in any other design.

To export a NetGroup, use the XMATIC_ExportNetGroupXML Capture TCL command.

For details on Capture TCL see the Capture TCL documentation.

To import a Associated NetGroup Definition Xml

1. Open the NetGroup dialog
2. From the Place menu choose NetGroup
3. Click Import NetGroups.

   The Associated NetGroup Definitions Xml Files dialog displays
4. Enter the full path of the associated NetGroup definition Xml file or browse to and select the associated NetGroup definition Xml file and click Open.

   The NetGroups contained in the file are imported into the current design.

   You can view these definitions in the Existing associated NetGroup definitions list of the NetGroup dialog.

Note: If your run the Export NetGroup TCL command on a design only the named associated NetGroup definitions are exported. This implies that the unnamed associated NetGroup definitions are not exported to the definition file.

Placing a named NetGroup on a page

After you define a NetGroup, you can place the NetGroup on the page of the design.

You can place a named NetGroup on a page as:

- a block.
- a hierarchical port.
- an off-page connector.

To place a named NetGroup as a block

1. To place a NetGroup as a block you need to go to the NetGroup dialog box. This box is open if you have just created a new associated NetGroup definition or you can open this from the NetGroup menu item on the Place menu.

   When placing a NetGroup on a page, you have the option to place the entire NetGroup on place only selected members of the NetGroup.

2. To place the entire NetGroup on the page, click the check box to the left of the NetGroup name.

   (To place only selected members of the NetGroup, expand the NetGroup node and click the check boxes to the left of the selected members.)

   Notice, when you click the NetGroup name check box or any one of the NetGroup member check boxes, the Name field is filled with the name of the NetGroup. This is the default name given to the named NetGroup instance, and you have the option to edit this instance name.

3. To place the NetGroup as a block, choose the Place NetGroup Block check box and click OK.

   The cursor changes to a crosshair.

4. Draw a block to contain the NetGroup. This is done the same way as when drawing a hierarchical block on a page.

When you place a NetGroup as a block on a schematic page, you have the option to synchronize this block (up or down) the same way

you synchronize a hierarchical block in a design. For details about synchronizing a block see Synchronize Up command and Synchronize Down command.

To place a named NetGroup as a hierarchical port

1. To place a named NetGroup as a hierarchical port, you need go to the Place Hierarchical Port dialog.

   To open this dialog, choose the Hierarchical Port menu item from the Place menu.

2. Enter a symbol for the port.
3. To place the hierarchical port as a NetGroup port, choose the NetGroup Port check box.
4. From the drop-down list choose the NetGroup.
5. Click OK and place the port on the page.

Note: The look and feel of a NetGroup port is different from that of a hierarchical port.

Also, if you place the mouse pointer over the NetGroup port, the tooltip displays the associated NetGroup definition.

To place a named NetGroup as an off-page connector

1. To place a named NetGroup as an off-page connector, you need go to the Place Off-Page Connector dialog.

   To open this dialog, choose the Off-Page Connector menu item from the Place menu.

2. Enter a symbol for the connector.
3. To place the off-page connector a NetGroup connector, choose the NetGroup Port check box.
4. From the drop-down list choose the NetGroup.
5. Click OK and place the connector on the page.

Note: The look and feel of a NetGroup connector is different from that of a off-page connector.

Also, if you place the mouse pointer over the NetGroup connector, the tooltip displays the associated NetGroup definition.

To delete an associated NetGroup definition

A Capture TCL command is available to delete an associated NetGroup definition. See the Capture TCL documentation for details.

Unnamed NetGroup

An unnamed NetGroup allows you to create an associated NetGroup definition for one-time usage. This means that the associated NetGroup definition is built dynamically and the NetGroup cannot be further instantiated across the design.

A benefit of an unnamed NetGroup is that you first create a empty definition and then add signals as required. While, you cannot instantiate the associated NetGroup definition elsewhere in your design (or page), you can, however, copy and paste the NetGroup.

An unnamed NetGroup can contain a scalar or a bus but not another NetGroup. However, a named NetGroup can contain a scalar, a bus as well as an other NetGroup.

To create an unnamed NetGroup

1. Choose NetGroup from the Place menu in Capture.

   The Place / Create NetGroup dialog displays.

2. To specify the NetGroup as unnamed, choose Place Un Named NetGroup.

   When you click the check box, the Name box is disabled and the default unnamed NetGroup name, UNNAMEDNETGROUP, displays in the box. This is the name that is given to the NetGroup. Also, the name is un-editable.

To place an unnamed NetGroup as a block

1. To place a NetGroup as a block you need to go to the Place / Create NetGroup dialog box. This box is open if you have just created a new associated NetGroup definition or you can open this from the NetGroup menu item on the Place menu.
2. To place the NetGroup as a block, choose the Place Un Named NetGroup Block check box and click OK.

   The cursor changes to a crosshair.
3. Draw a block to contain the NetGroup. This is done the same way as when drawing a hierarchical block on a page.

When you place an unnamed NetGroup as a block on a page, the NetGroup is empty. You need to now add members to the NetGroup.

Note: You can add scalar members and buses to unnamed NetGroups.

To add a scalar member to an unnamed NetGroup

1. Select the unnamed NetGroup.
2. From the Place menu choose the Hierarchical Pin menu item.

   The Place Hierarchical Pin dialog displays.
3. Enter a name for the scalar member.
4. Specify the width as scalar by selecting the Scalar radio button in the Width group.
5. Click OK.

   The pin is attached to the cursor.
6. Place the pin on one of the edges of the unnamed NetGroup.

Note: As you keep adding members to the NetGroup, the size of the NetGroup is dynamically increased. Similarly, if you delete a member from a NetGroup the size will reduce dynamically.

To add a bus member to an unnamed NetGroup

1. Select the unnamed NetGroup.

2. From the Place menu choose the Hierarchical Pin menu item.

   The Place Hierarchical Pin dialog displays.

3. Enter a name for the bus member.

   Note: The name of the bus must also define the size of the bus.

4. Specify the width as bus by selecting the Bus radio button in the Width group.

5. Click OK.

   The pin is attached to the cursor.

6. Place the pin on one of the edges of the unnamed NetGroup.

To delete a member from an unnamed NetGroup

1. Select the member to delete and press the Delete key.

Note: As you keep deleting members from a NetGroup, the size will reduce dynamically.

Note: In the case of an unnamed NetGroup, the order of the members depends on the order in which they are added to the NetGroup.

To place an unnamed NetGroup as a hierarchical port

1. To place an unnamed NetGroup as a hierarchical port, you need go to the Place Hierarchical Port dialog.

   To open this dialog, choose the Hierarchical Port menu item from the Place menu.

2. Enter a symbol for the port.

3. To place the hierarchical port as an unnamed NetGroup port, choose the Show UnNamed NetGroup check box.

4. From the drop-down list choose the unnamed NetGroup.

5. Click OK and place the port on the page.

Note: The look and feel of a NetGroup port is different from that of a hierarchical port.

Also, if you place the mouse pointer over the NetGroup port, the tooltip displays the associated NetGroup definition.

To place an unnamed NetGroup as an off-page connector

1. To place an unnamed NetGroup as an off-page connector, you need go to the Place Off-Page Connector dialog.

   To open this dialog, choose the Off-Page Connector menu item from the Place menu.

2. Enter a symbol for the connector.

3. To place the hierarchical port as an unnamed NetGroup port, choose the Show UnNamed NetGroup check box.

4. From the drop-down list choose the unnamed NetGroup.

5. Click OK and place the connector on the page.

Note: The look and feel of a NetGroup connector is different from that of a off-page connector.

Also, if you place the mouse pointer over the NetGroup connector, the tooltip displays the associated NetGroup definition.

NetGroup Reuse (Hierarchical Part Creation)

You can reuse a NetGroup in other designs by creating a hierarchical part of the NetGroup and then instantiating the part in other designs.

To create a hierarchical part of a NetGroup

1. Open a design (or create a new design).

2. Create the NetGroup that you need to reuse.

   You can create either a named or an unnamed NetGroup.

3. Place the NetGroup as a hierchical port on a page of the design.

   For details:

   To place an unnamed NetGroup as a hierarchical port

OR

To place a named NetGroup as a hierarchical port

4. Save the design.
5. Go to the Generate Part dialog (from the Tools menu choose Generate Part).
6. In the Netlist/Source file box, enter the full path for the design. You can also browse to the design file.
7. If required, in the Netlist/Source file type drop-down, choose the Capture Schematic / Design option.
8. if required, you can change the name and destination of the library (OLB) containing the hierarchical part.
9. Click OK.

   The Split Part Section Input Spreadsheet displays.
10. Click Save.

The part is created in the library. Also, you can view the OLB file and the part in the Outputs folder in the Project manager.

If you double-click the part in the Project manager, the Part editor displays. You can also make changes to the part.

The NetGroup contained in this part is now available for use in any design.

Components of a NetGroup Block

When you place a NetGroup block on a page, the block consists of a number of different parts and definitions that are different from a hierarchical block. The parts help in using the NetGroup for connectivity. The definitions help to understand the constituent members of the NetGroup.

NetGroup Entry/Exit Pin

When you define a NetGroup, you specify members of the NetGroup. You will then need to connect signals on your page to these members. On a NetGroup block these members appear as ports and

are referred to as **NetGroup pins**. The nomenclature for a NetGroup pin is <NetGroupInstanceName>.<MemberName>.

NetGroup Pin

The benefit of a NetGroup is that you do not need to create as many exit points as the number of entry points. When you define the NetGroup, one exit point is created that holds the signals for all the entry points. This exit point is referred to as the **NetGroup entry pin**.

Note: The NetGroup port displays the NetGroup instance name and the size of the NetGroup instance.

NetGroup Wire

When you connect the entry / exit pins of the NetGroup to a wire, you are effectively connecting all the signals that constitute the NetGroup into one wire. This wire is known as the **NetGroup wire**.

Netlising NetGroup Designs

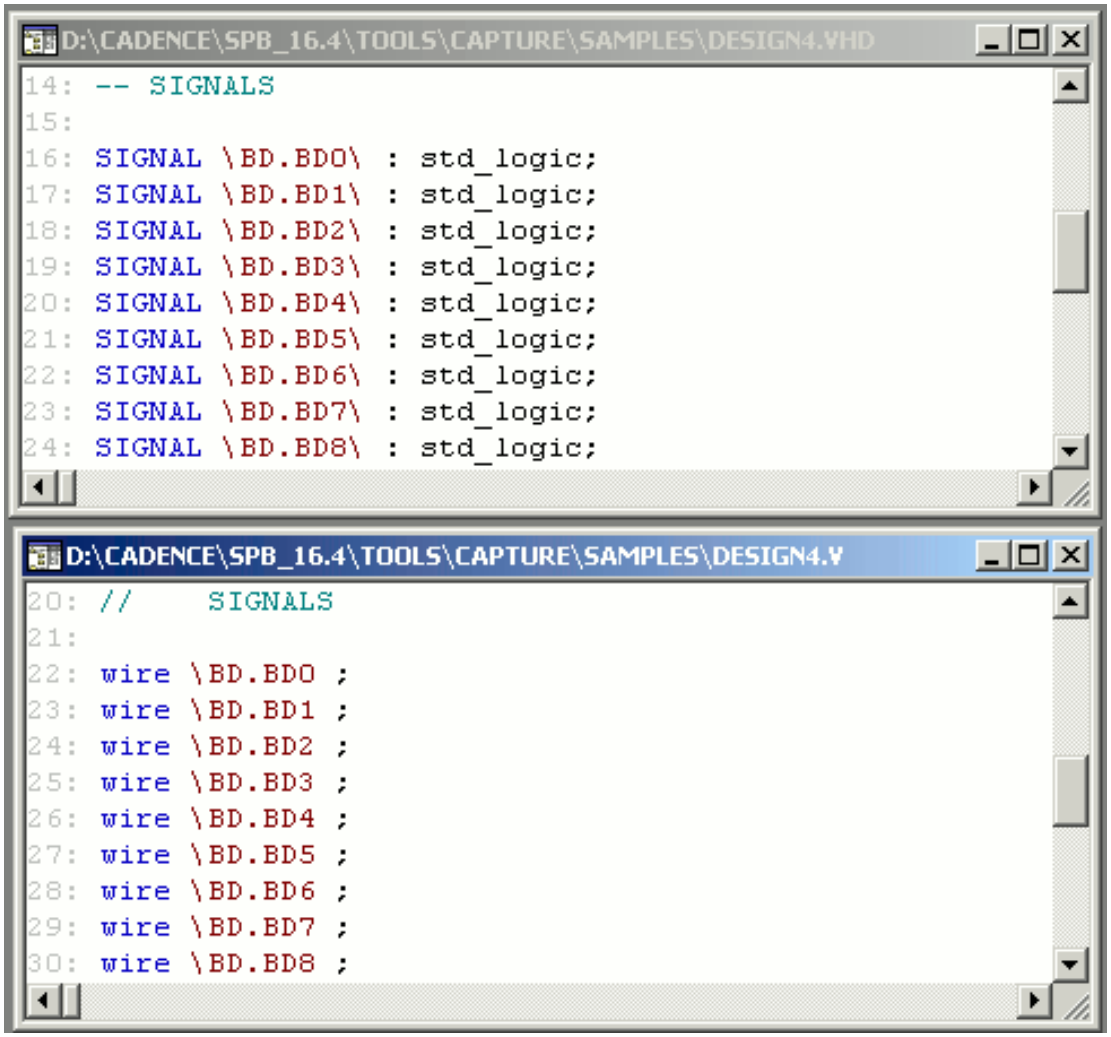
When you netlist a design, the signals in the design are mapped on the output netlilst.

A NetGroup is a hetrogeneous group of nets and hence the NetGroup as it is, cannot be translated as a NetGroup onto a netlist. The Capture netlisting command netlists the signals in a NetGroup by extracting out the signals when creating the netlist.

However, when the signal names display on the netlist, the names must also contain the name of the NetGroup. This prevents the possibility of duplicate signal names on the netlist. To define a NetGroup-signal name combination on the netlist, Capture uses <NetGroup Name><Separator><Signal Name>.

Note: The default NetGroup-signal combination, <NetGroup Name>.<Signal Name>, uses the dot notation.

For example, if you create a VHDL or Verilog netlist out of a design that contains NetGroups, the output uses the dot notation to handle the signals contained in the NetGroup.



Other Netlists

While most of the netlists generated through the Capture netlist command support the dot notation to signify NetGroup signals, some netlisters (available in the Other Netlists tab of the Create Netlist dialog) do no support the dot in a net name. To handle this, Capture

provides a TCL script (**capCorrectNetnamesONL.tcl**) that defines an alternative separator in the netlist depending on the netlister.

Formatter	Name Separator
orVstmodel.dll	_ (underscore)
orOhdlnet.dll	_ (underscore)
orPcadnlt.dll	_ (underscore)
orEdif.dll	_ (underscore)
orCbds.dll	- (hyphen)
orCalay90.dll	- (hyphen)
orCalay.dll	- (hyphen)

Tip

This TCL script runs during the netlisting procedure. This implies that if you have a custom netlister not included in Capture, and the formatter does not support the default dot separator you can update this script to specifiy an alternative separator.

NetGroup Connectivity

As the name suggests, a NetGroup allows you to NetGroup together a heterogeneous group of signals. Using this group of signals you, can easily connect together a large number of signals on a page, across pages in a design and even across a hierarchy. This section describes NetGroup connectivity using four scenarios. Two scenarios for named NetGroups and two scenarios for un-named NetGroups.

If you short a buses and NetGroups together, the order of preference depends on factors like the with of the bus or NetGroup. This preference defines the resultant object (bus or NetGroup), Winning bus, and the flat nets generated out of the short. For details (covering a set of scenarios), see Net Generation Scenarios on page 1397

Named NetGroup Connectivity on page 319.

Un-named NetGroup connectivity on page 322.

Named NetGroup Connectivity

Using named NetGroups you can connect signals across pages in a hierarchical design. You can also use named NetGroups to connect signals across page at the same level of a hierarchical design or across pages in a flat design.

Using a Named NetGroup to connect signals across a hierarchy on page 319.

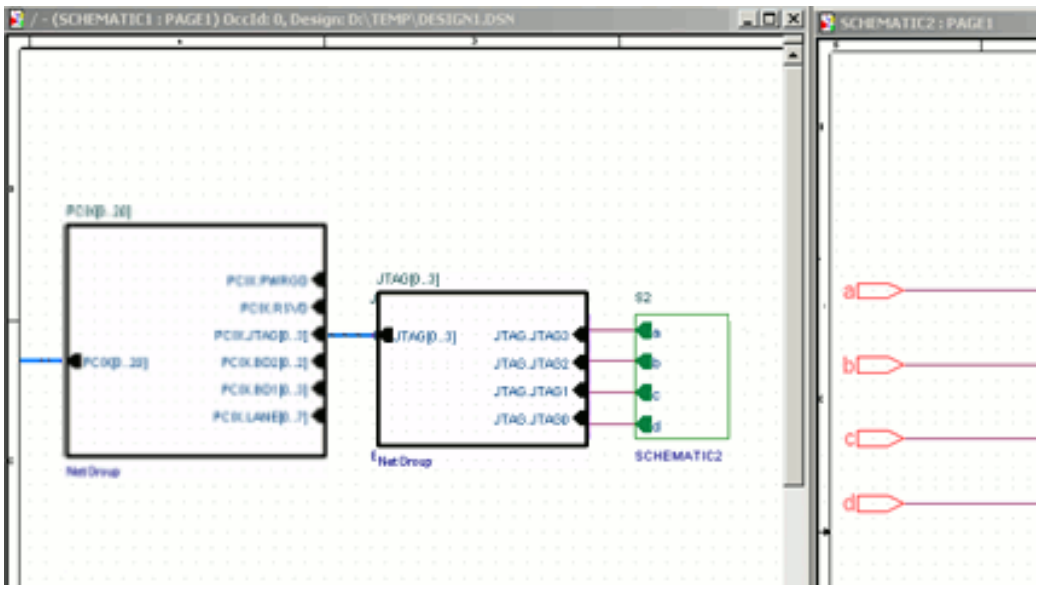
Using a Named NetGroup to connect signals across pages in a design on page 321.

Using a Named NetGroup to connect signals across a hierarchy

A NetGroup enables the connectivity of signals across the levels of a hierarchical design.

Scenario 1

In this example, the signals at the top level (SCHEMATIC1:PAGE1) of the design need to be connected to signals on the page SCHEMATIC2:PAGE1 at lower levels of the hierarchy.



1. The signals on SCHEMATIC1:PAGE1 are first tapped into a large NetGroup, PCIX, containing 19 signals. This associated NetGroup definition contains the signals of this page that need to be connected to pages across the hierarchy.

   Four signals (a, b, c & d) need to be connected from the top level to the signals on SCHEMATIC2:PAGE1.

2. These four signals are first placed in a NetGroup JTAG that is then placed, as a member, in the large NetGroup PCIX.

3. Next, the JTAG NetGroup is placed separately onto the SCHEMATIC1:PAGE1 page.

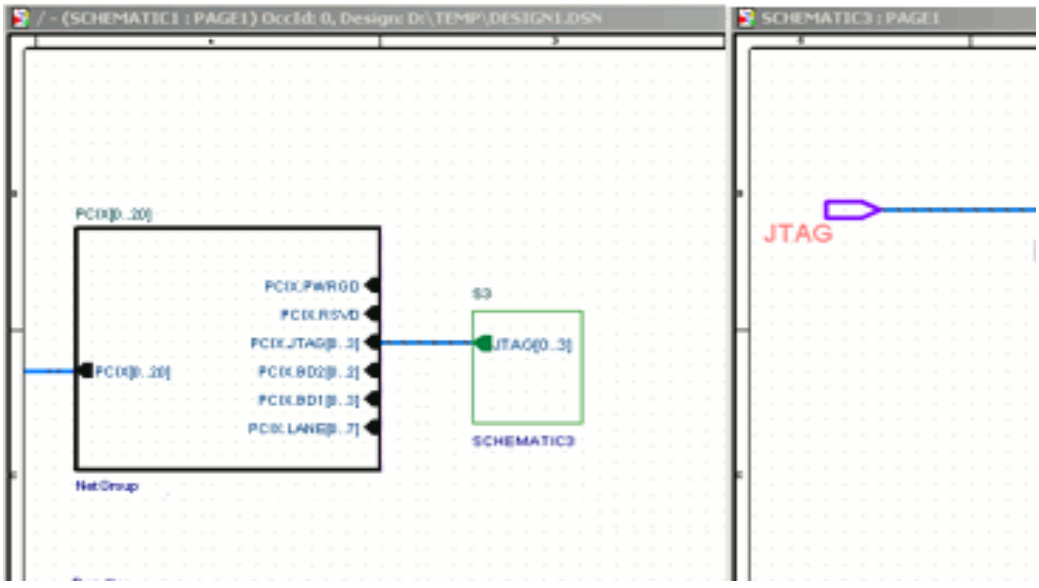
4. The PCIX.JTAG NetGroup port is connected to the separate JTAG NetGroup.

5. Each NetGroup port of the JTAG NetGroup is then connected to the corresponding ports, a, b, c & d of the hierarchical block of SCHEMATIC2.

6. Finally, on the page SCHEMATIC2:PAGE1, four off-page connectors, a, b, c & d, are created to tap out the corresponding signals from SCHEMATIC1:PAGE1.

Scenario 2

In this example, the four signals, a, b, c & d are connected to signals on SCHEMATIC3:PAGE1 using a NetGroup off-page connector.

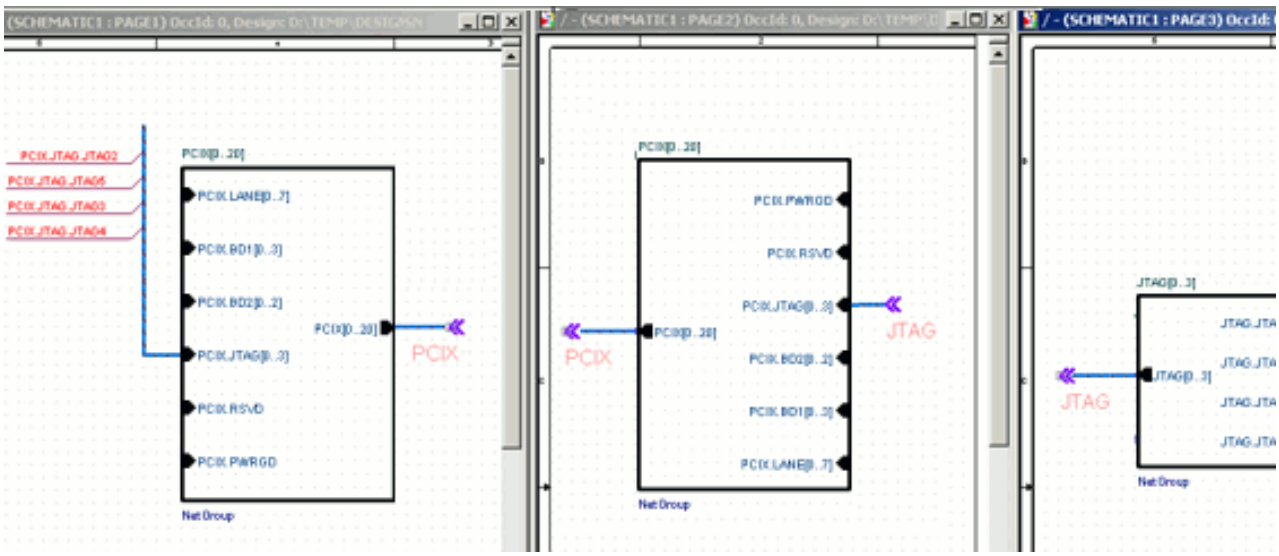


1. Again, the signals on SCHEMATIC1:PAGE1 are first tapped into a large NetGroup, PCIX, containing 19 signals.
2. In this case, the PCIX.JTAG NetGroup port is connected to the JTAG hierarchical port of the SCHEMATIC3 hierarchical block.
3. Finally, on SCHEMATIC3:PAGE1, the JTAG signals are tapped out by placing a JTAG NetGroup connector.

Using a Named NetGroup to connect signals across pages in a design

A NetGroup also increases the ease of the connectivity of signals across the pages of a design.

In this example, you will connect signals across pages in a flat design.



1. The signals on SCHEMATIC1:PAGE1 are first tapped into a large NetGroup, PCIX, containing 19 signals. This associated NetGroup definition contains all the signals of this page that need to be connected to pages across the design.

   Four signals (a, b, c & d) need to be connected from PAGE1 to PAGE3 on SCHEMATIC1.

2. On PAGE1, these signals are connected via a bus to the PCIX.JTAG NetGroup entry point.

3. The PCIX NetGroup off-page connector creates the outlet for the signals of the NetGroup.
4. Another instance of the NetGroup is placed on SCHEMATIC1:PAGE2 to tap out the signals from SCHEMATIC1:PAGE1. To build the connectivity of these signals on SCHEMATIC1:PAGE2, place a NetGroup off-page connector PCIX on the page.
5. The signals, a, b, c, and d are part of the JTAG NetGroup (included within the PCIX NetGroup). To tap out these signals, connect a NetGroup off-page connector to the PCIX.JTAG NetGroup entry in the PCIX NetGroup on SCHEMATIC1:PAGE2.
6. Next, on SCHEMATIC1:PAGE3, place an instance of the JTAG NetGroup.
7. Also, place a JTAG off-page connector to the JTAG NetGroup port.
8. Finally, tap out the signals a, b, c, and d from the NetGroup entry points to complete the signal connectivity.

Un-named NetGroup connectivity

Similar to named NetGroups, you can also use un-named NetGroups you can connect signals across pages in a hierarchical design. Again, as in named NetGroups, in un-named NetGroups, you can connect signals across page at the same level of a hierarchical design or across pages in a flat design.

Using an Un-named NetGroup to connect signals across a hierarchy on page 322.

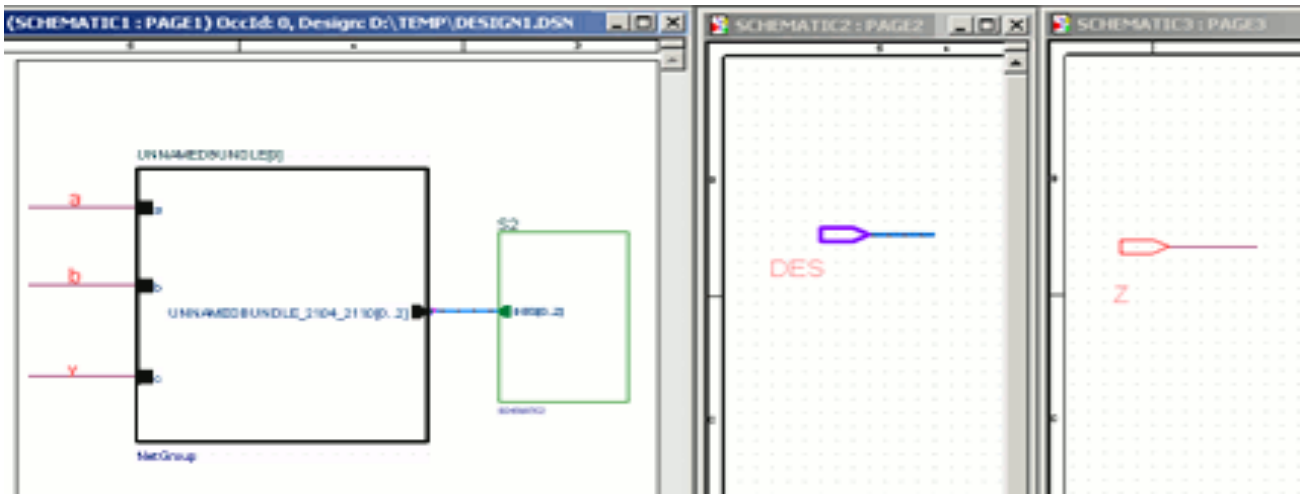
Using a Un-named NetGroup to connect signals across pages in a design on page 324.

Using an Un-named NetGroup to connect signals across a hierarchy

Along with using named NetGroups to connect signals on different levels of a hierarchical design, you can also use un-named NetGroups. We use unnamed NetGroup to group multiple signals on

the fly. This implies that we create the define (in the design) any signals we want to include in the NetGroup.

In this example, the signals, a, b, and y, at the top level (SCHEMATIC1:PAGE1) of the design are to be connected to corresponding signals on the page, SCHEMATIC3:PAGE3 at a lower level of the hierarchy.



1. An unnamed NetGroup is first placed on SCHEMATIC1:PAGE1.

   This is an empty associated NetGroup definition so we still need to add members to this NetGroup.

2. Specify three scalar members for the NetGroup. These will be used as entry points from the signals a, b, and y to the unnamed NetGroup. To this, add three hierarchical pins and name them a, b, and y.

3. Then connect the three signals to the NetGroup entry points.

4. The NetGroup port is then connected to a hierarchical port, named DES, of the SCHEMATIC2:PAGE1 hierarchical block placed on SCHEMATIC1:PAGE1.

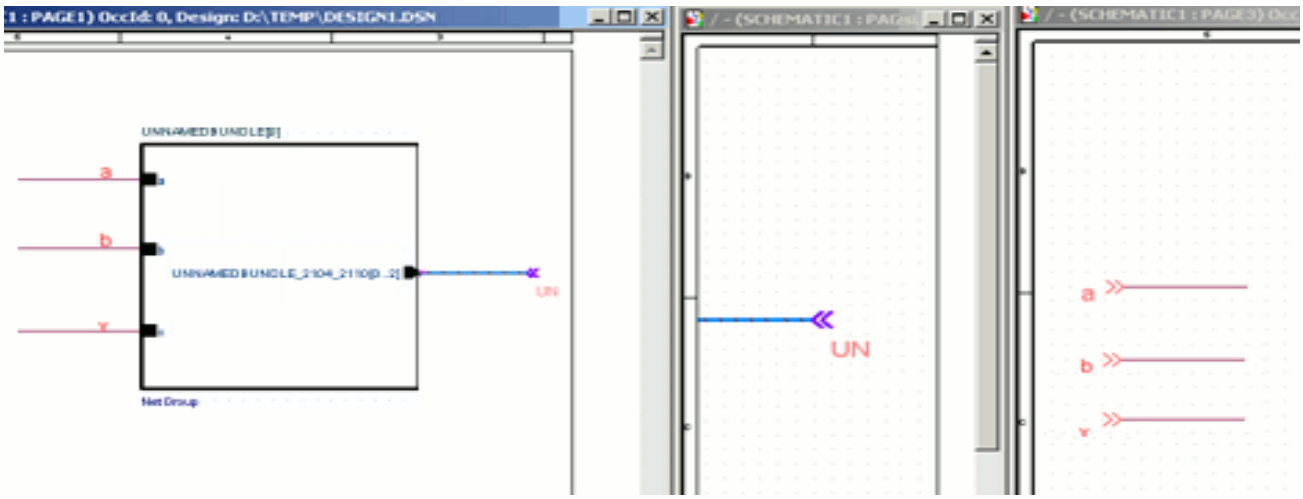
5. The NetGroup port DES is placed SCHEMATIC2:PAGE1.

6. Finally, tap the signals, a, b, and y from the NetGroup port DES on SCEMATIC3:PAGE3.

Using a Un-named NetGroup to connect signals across pages in a design

An unnamed NetGroup can also be used to connect signals across pages at the same level of a design.

In this example, the signals on SCHEMATIC1:PAGE1 of the design need to be connected to signals on SCHEMATIC1:PAGE2.



1. An unnamed NetGroup is first placed on SCHEMATIC1:PAGE1.

   This is an empty associated NetGroup definition so we still need to add members to this NetGroup.

2. Specify three scalar members for the NetGroup. These will be used as entry points from the signals a, b, and y to the unnamed NetGroup. To this, add three hierarchical pins and name them a, b, and y.

3. Then connect the three signals to the NetGroup entry points.

4. Since we are connecting signals across pages at the same level of a design, the NetGroup is connected to a NetGroup off-page connector UN.

5. To build the connectivity of these signals on SCHEMATIC1:PAGE2, place a NetGroup off-page connector UN on the page.

6. Finally, on SCHEMATIC3:PAGE3, create off-page connectors for the signals, a, b, and y.

7

Editing the design

This chapter covers:

- "Browsing a design" on page 327
- "Searching for part text and pins" on page 331
- "Replacing a part" on page 333
- "Editing Hierarchical block look and feel" on page 334
- "Manipulating objects" on page 336
- "Labeling wires and buses" on page 355
- "Editing text and graphics" on page 357
- "Editing wire and bus look & feel" on page 379
- "Editing wire and bus properties" on page 376
- "Working with macros" on page 380

Capture has a diverse and powerful set of tools that provide a method for editing the characteristics of your design.

Browsing a design

Using the project manager, you can list objects and sort them with the press of a button. This makes it easy to find, select, and edit objects.

For example, you can list the parts in your design and sort them by part reference or part value. You can list all objects by part value, then add a footprint property to all parts with the same value. When you are debugging your design, you can list all of the error markers and jump to them one by one.

In Capture, you can browse a design-wide list of all objects of one type; you can search for an object by name, or by one of its property values; and you can search a specific schematic page or an entire project.

In the project manager window, Capture will browse for the following object types:

- Parts (occurrence values only)
- Nets (occurrence values only)
- Flat netlist (nets as they appear in a netlist)
- Hierarchical ports
- Off-page connectors
- Title blocks (occurrence values only)
- Bookmarks
- DRC markers
- Variant Parts

The Find command searches for these object types or for comment text.

For information on how to use the Variant Parts option in the Find toolbar, see the *Searching for variant information on a schematic page* section of the *OrCAD Capture CIS User Guide*.

To browse a design

➤ From the Edit menu, choose Browse, then choose the browse category from the pull-right menu. For each category, the parameters given below appear in the browse window.

Parts	Reference, value, source part, source library, page
Nets	Name, netname, page, schematic folder
Hierarchical ports	Port name, page, schematic folder

Off-page connectors	Connector name, page, schematic folder
Bookmarks	Bookmark name, page, schematic folder
DRC markers	DRC error, DRC detail, DRC location, page, schematic folder

If you double-click an item in the browse window, the schematic page opens with that item selected. Or you can select several items, then choose the Properties command from the Edit menu to open the spreadsheet editor.

To display a list of parts in a library

➤ Open the library. A list of parts appears in the project manager.

or

➤ From the schematic page editor's Place menu, choose the Part command.

To display a list of parts in the design cache

➤ In the project manager, double-click on the Design Cache icon.

To list all objects of one type

1. In the project manager, select the documents you want to search. To search the entire design, select all schematic folders.
2. From the Edit menu, choose the Browse command, then choose the object type from the pull-right menu. The browse window displays a list of all objects of the selected type.
3. If you wish to display an object, double-click on the entry in the browse window. The schematic page editor opens and the object appears in the selection color.

or

➤ If you wish to edit the properties of one or more listed objects, then from the Edit menu choose the Properties command to display the spreadsheet editor.

To limit the list of objects

1. In the project manager, select the documents you want to search. To search the entire design, select all schematic folders.
2. From the Edit menu, choose the Find command. The Search toolbar displays.
3. In the Text to Search text box, enter a text string that defines the object you are searching. This could be the name, alias, or property value. You can use the standard "*" and "?" wildcard characters.

   The Search toolbar contains a drop-down list that displays the search options that allow you to further refine your search.
4. From the search options drop-down list verify that the Match Case option is as you want it.
5. From the search options drop-down list select the object type.
6. Press Enter or click the search button on the toolbar.

   The Find window displays a list of objects that meet the criteria you specified.
7. If you wish to display an object, double-click on the entry in the Find window. The schematic page editor opens and the object appears in the selection color.

   OR

➤ If you wish to edit the properties of one or more listed objects, from the Edit menu choose the Properties command to display the spreadsheet editor.

   ALSO

➤ If you wish to open the Browse Spreadsheet for a part in the Find window, right-click on the part and choose Edit Properties. The Browse Spreadsheet dialog displays.

For information on how to use the Variant Parts option in the Find toolbar, see the *Searching for variant information on a schematic page* section of the *OrCAD Capture CIS User Guide*.

Searching for part text and pins

In Capture, you can search for specific comment text on a part, or you can search for a pin by name or by one of its property values.

Using the Find command and a part property value, you can locate a part in a schematic folder or on a schematic page. In the Find toolbar, you enter a property value string and specify that you want to find a part. Capture searches all the parts to find those with a property value that matches the string. You can use question marks (?) or asterisks (*) as wildcards in the property value string.

To locate a part in a project

1. In the project manager, select the schematic folders or schematic pages you want to search.
2. From the Edit menu, choose the Find command. The Find toolbar appears.
3. In the Text to Search text box, enter the property value string for the part you seek. You must use wildcard characters (standard "*" or "?") with a truncated search. For example, to search for resistors, enter "R*".
4. Select Parts from Search options drop-down list.
5. Click the Search button to start the search.

   Parts that have a property value matching the property value string in step 3 are listed in the Find window.
6. Double-click on the part in the Find window list to open the schematic page editor with that part displayed and selected.

Note: Capture preserves the case of part names and net names, but ignores the case when comparing names for electrical connection. That means you may use uppercase or lowercase letters as you wish, but you need not remember the case.

To search for pins

1. Open the part in the part editor or open the schematic page.
2. From the *Edit* menu, choose the Find command. The Find toolbar appears.
3. Enter the pin name or a property value. You can use question marks (?) or asterisks (*) as wildcards.
4. Verify that the Match Case option is set as you want it.
5. Select *Parts Pin* as the type, then click *the Search button*.

   Parts pins that have a property value matching the property value string in step 3 are listed in the Find window.

To search for text

1. Open the part in the part editor.
2. From the Edit menu, choose the Power Pins command. The Find toolbar appears.
3. Enter the text string that you seek. You can use question marks (?) or asterisks (*) as wildcards.
4. Verify that the Match Case option is set as you want it.
5. Select Text as the object type, then click the Search button.

   The Texts matching the search string in step 3 are listed in the Find window.

Renaming and deleting part properties

Capture allows you to rename and delete a part property in every part instance that contains the property for an entire design.

To rename a part property

1. In the project manager, select the design file or the schematic page.
2. Select the Rename Part Property command from the Edit menu. The Rename Part Property dialog box appears.

3. In the Find User Property text box, type the current property name.
4. In the Replace with User Property text box, type the new property name.
5. Click OK.

To delete a part property

1. In the project manager, select the design file or the schematic page.
2. Select the Delete Part Property command from the Edit menu. The Delete Part Property dialog box appears.
3. In the Property Name text box, type the property name.
4. Click OK.

Replacing a part

If you need to replace a part in your project with another, you could open the schematic page editor to find and delete each instance property of the part, then place the replacement part. If your design includes many instances of this part, you can more easily achieve the same end with the Replace Cache command.

You would also use the Replace Cache command after you edit a part on a schematic page if you want to undo the edits and restore the part's link to its library.

When you delete a part, all of its properties are also deleted. When you use the Replace Cache command, properties of the part instance are attached to the replacement part; however, the pin properties are lost.

Note: When you use the Update Cache command or the Replace Cache command with the option to preserve schematic part properties, all instance and occurrence properties of the schematic part are retained. This means you will not lose any changes made to pin properties after the part was placed, including those made by the Back Annotate or the Annotate tools.

To replace a part throughout a design

1. From the design cache, select the part you want to replace.
2. From the Design menu, choose the Replace Cache command.
3. In the dialog box that appears, enter the name of the replacement part and the library that contains it.
4. Select the Replace schematic part properties action if you want to completely replace the part and its properties. Otherwise, use the default action to preserve schematic part properties.
5. Click OK. When the project manager appears again, double-click on the design cache to verify that the replacement part is listed instead of the original part.

Note: The Replace Cache and Update Cache commands are quite similar. However, there are a couple of significant differences between the two commands. You can modify a part's link to the library (part name, path, and library) with Replace Cache, but not with Update Cache. Update cache only brings in new data when the path has changed. Another difference is that if the path and library names do not change, Replace Cache reloads the part definition into the design. However, if Update Cache finds that the part name and the library names are the same, it does not bring in part changes.

Note: If you need to know a part's library of origin, you can select the part in the project manager, then select Replace Cache from the Design menu. The part name and the library and path are listed in the dialog box that appears. Click the Cancel button to return to the project manager.

You can discover the library of origin for multiple parts by Creating a cross reference report.

Editing Hierarchical block look and feel

When you create a hierarchical block on a schematic page, the block displays the part name and the implementation. However, you may want to add a picture to the block that acts as a visual representation of the implementation below the block.

To place a graphical object on a hierarchical block

1. Click the hierarchical block.
2. Right-click on the block and choose Edit Part from the pop-up menu.

   The block opens in the Capture Part Editor.

   From the Place menu, select any object to place on the block.

   Note: To ensure that the object is visible on the part on the schematic, place the object on the block.
3. Save the changes and close the Part Editor to return to the schematic.

To change the look and feel of a hierarchical block

1. Click the hierarchical block.
2. Right-click on the block and choose Edit Part from the pop-up menu.
3. The block opens in the Capture Part Editor.
4. From the Place menu choose rectangle.
5. Click the crosshair cursor at one corner of the block and drag the cursor to the diagonally opposite corner to cover the entire block.
6. Click to select on the rectangle you created over the block in Step 4.
7. Right-click on the rectangle (any of the edges of the block) and choose Edit Properties from the pop-up menu.
8. From the Edit Properties menu, choose the properties form the drop-down lists to apply to the block.
9. Save the changes and close the Part Editor to return to the schematic.

Note: Even after closing the Part Editor, you can undo all the changes you made to the block by using the Capture Undo command (Edit - Undo or Ctrl + Z).

Manipulating objects

This section covers:

- Moving objects on page 336
- Rotating objects on page 338
- Copying objects on page 338
- Deleting objects on page 340
- Mirroring objects on page 341
- Selecting and deselecting objects on page 341
- Graphical Operation (GOp) Locking on page 344
- Undoing and repeating on page 351

On a schematic page, you can change the location or orientation of a part, and you can use the part editor to edit the graphic representation of the part. When you edit the graphic representation on a schematic page, you make a local part that differs from the part in the library and exists only in this project; the only way to place another copy of this part is to use the Copy command on the Edit menu.

After you complete edits to the graphic representation, you close the part editor window. Capture gives you a choice of updating the single instance property, or updating all instances in the design. If you update only the single instance, Capture creates a new part in the design cache. If you update all instances, Capture replaces the library part in the design cache with your edited part.

You can also edit the part's properties. If you wish to edit the properties of several parts, use the Update Properties or Export Properties command on the Tools menu or the spreadsheet editor.

Note: When you place a part off-grid, it remains off-grid through any cut-and-paste and drag-and-drop operations.

Moving objects

You can easily change the location of objects in the schematic page editor or the part editor. Immediately after you place an object, you

need to select the selection tool or press ESC before you perform the steps below.

Note: Capture uses the location of the first pin on a part to snap to grid. If you move a part without pins, it will be on Fine grid unless you use the Cut command described below to place the part on Coarse grid.

To drag an object using the mouse

➤ Position the pointer on the object. Press the left mouse button and drag the object to the new location. Moving an object this way does not break any of its electrical connections, with the exception of pin or net symbol connections. Otherwise, electrically connected objects are rubberbanded to maintain connectivity.

Note: If you are dragging a part or wire to another location and that change will affect connectivity, Capture warns you with a changed cursor and temporary markers on your schematic. Visible and off-screen connectivity changes will be saved in the session log if you complete the operation.

To move an object using the mouse

1. Move the pointer over the object.
2. Simultaneously press ALT and the left mouse button, and then drag the object to the new location.
3. Release the mouse button. The object is placed at the new location. Nets previously connected to the object are not moved.

To move objects using the Cut command

1. Select the object or objects.
2. From the Edit menu, choose the Cut command. The object is placed on the Clipboard.
3. If the object is to be moved to another window, open that window.
4. From the Edit menu, choose the Paste command. The object is attached to the pointer.

5. Move the pointer to the location where you wish to place the object and click the left mouse button. The object appears in the selection color.
6. Click an area where there are no parts or objects to deselect the object, or press ESC.

Note: When you move an object in this manner, all occurrence properties are cleared, but instance properties are retained. See Instances and occurrences for more information.

Rotating objects

Capture objects can be rotated by 90-degree increments. Some objects, such as images, cannot be rotated.

To rotate objects

1. Select the objects.
2. From the Edit menu, choose the Rotate command. The selection set rotates 90 degrees counterclockwise. If the Rotate command does not appear on the Edit menu, the objects cannot be rotated.

Copying objects

Capture uses the Windows Clipboard to support the standard Cut, Copy, and Paste functions. You can cut, copy and paste information across schematic page or part windows. You can copy text from other Windows applications and paste it into Capture text boxes using the Clipboard. You can also copy a section of your schematic page to another Windows application.

To copy objects using the mouse

1. Select the object or objects.
2. Press and hold both CTRL and the left mouse button while you drag the object to its second location.
3. Release the left mouse button to place the copy.

Note: If you are dragging a part or wire to another location and that change will affect connectivity, Capture warns you with a changed cursor and temporary markers on your schematic. Visible and off-screen connectivity changes will be saved in the session log if you complete the operation.

Note: Copying projects using CTRL+drag causes duplicate instances, which creates problems for EDIF netlisting. If you run an EDIF netlist on a design in which you have used this method of copying objects, be sure to use instances when you annotate the design.

To copy objects using the Copy command on the Edit menu

1. Select the object or objects.
2. From the Edit menu, choose the Copy command. The object is placed on the Clipboard.
3. If the object is to be copied to another window, open that window.
4. From the Edit menu, choose the Paste command. The object is attached to the pointer.
5. Move the pointer to the location where you wish to place the object and click the left mouse button. The object appears in the selection color.
6. Click an area where there are no parts or objects to deselect the object.
7. If you want to place another copy of the object, repeat steps 4, 5, and 6 above.

To copy text or graphics into other Windows applications

1. Select the text or graphic.
2. From the Edit menu, choose Copy. The selected objects are copied to the clipboard
3. Open the other Windows application and use that application's Paste command to place the clipboard contents.

Shortcuts

Toolbar:

Deleting objects

To delete objects

➤ Select the objects and press DELETE or BACKSPACE.

or

1. Select the objects.
2. From the Edit menu, choose the Delete command.

To delete a schematic folder, schematic page, part, or symbol

1. If the schematic page (or a schematic page within the schematic folder) is currently open in Capture, close it.
2. Select the document or documents in the project manager.
3. From the Design menu, choose the Delete command.

or

1. If the schematic page (or a schematic page within the schematic folder) is currently open in Capture, close it.
2. Select the objects and press DELETE or BACKSPACE.

To delete a wire or bus segment

1. Select the segment.
2. Press the DELETE or BACKSPACE key.

To delete a net

1. Select one segment of the net.
2. Click the right mouse button. A pop-up menu appears.

3. From the pop-up menu, choose the Select Entire Net command.
4. Press the DELETE or BACKSPACE key.

Mirroring objects

Capture objects can be mirrored horizontally, vertically, or both horizontally and vertically. Some objects, such as text and images, cannot be mirrored.

To mirror objects

1. Select the objects.
2. From the Edit menu, choose the Mirror command. If the commands of the pull-right menu are not available, the objects cannot be mirrored.
3. Choose Horizontally, Vertically, or Both. The objects flip in the indicated direction.

Selecting and deselecting objects

You select objects to edit, move, or alter them in any way. You can simultaneously alter multiple objects if they are all in the selection set. Objects that are selected appear in the selection color. You can also control the selection of objects in a schematic page when you drag the mouse pointer diagonally across the schematic page.

To select an object

➤ Position the pointer on the object, then click the left mouse button or press the space bar. The object appears in the selection color. Selection handles appear along the boundary box of an object selected in the schematic page editor. If the entire object is selected, all selection handles are the same size. A large handle indicates the point at which the object is selected.

Note: When you open the part editor from the schematic page editor, the part you are editing cannot be selected on the schematic page. After you close the part editor window, the part can be selected.

Note: You can resize an object by selecting it at a single point and dragging.

To select objects that converge at a single location

➤ Click the point at which the objects converge to select all objects.

To add or remove an object from the selection set

➤ Position the pointer over the object and press CTRL while you click the left mouse button. All objects in the selection set appear in the selection color. In the spreadsheet editor, this selection method is unavailable because the selection set is limited to contiguous cells.

To control the selection of objects during a mouse-drag operation

1. From the View menu, choose the Selection Filter command.

   The Selection Filter dialog box appears.

2. Select the check box corresponding to the object that you want to be selected during the mouse-drag operation.

3. Click OK.

   The next time you drag the mouse pointer diagonally across a schematic page, only these objects will be selected in the schematic page.

To select all objects in an area

1. From the tool palette, choose the selection tool.

2. Move the pointer to one corner of the area. Press and hold the left mouse button while you drag the pointer to the opposite corner, then release the left mouse button. Every object in the selection set appears in the selection color and the set behaves as one object.

Note: You can specify whether the selection set includes all objects intersected by your selection rectangle or only those objects fully

enclosed by the selection rectangle. From the Options menu, choose the Preferences command, and then choose the Select tab.

To select an entire contiguous polyline

1. From the tool palette, choose the selection tool.
2. Press and hold the left mouse button while you drag the pointer to select an area that includes some portion of the line.

To select all objects on a schematic page or a part

➤ From the Edit menu, choose the Select All command.

To select from among overlapping objects

➤ Position the pointer over the stack and press the TAB key while you click the left mouse button. This cycles through the objects in the stack.

To select all portions of a net on one schematic page

1. Select one segment of the net. The segment changes to the selection color.
2. Click the right mouse button to display a context-sensitive menu.
3. From the pop-up menu, choose the Select Entire Net command.

To deselect the selected objects

➤ Click an area where there is no object or part, or press the ESC key. Note that a part occupies a rectangular area encompassing all its graphics and property text; this means that a part may occupy a larger area than is apparent.

Note: To deselect an object that you have just placed, you must select the selection tool before clicking the mouse or press ESC to end mode and press ESC again to deselect the object.

To change the selection color

1. From the Options menu, choose the Preferences command and then choose the Colors tab.
2. Click the left mouse button over the Selection color. The color palette window opens.
3. Select the new color and click OK to dismiss the color palette.
4. Click OK to dismiss the dialog box.

Note: When you click on a wire segment, only that segment and its two handles are selected.

Graphical Operation (GOp) Locking

A schematic page often contains a large number of different types of objects like parts, pins, buses, wires. A user often needs to perform operations like adding new objects, changing object properties, moving, creating and deleting objects. All these operations require extensive user interaction with the Capture interface. Also, with the increasing complexity of designs, the number of objects on a page and pages in a design has increased exponentially. All these issues raise the need in Capture for providing a methodology to lock the state of a design at a particular point of the design process. For example, a designer should have the ability to maybe lock the layout of a schematic page.

To address such issues, Capture includes a graphical operation locking (GOp) feature that allows you to lock objects (like components, pages, folders and even design) in a Capture project.

When you graphically lock an object, the graphical aspects of the object are locked. This implies that non-graphical aspects of an object such as its properties are still editable. For example, if you lock a part on a schematic page, you cannot delete, or move the part but you can change, say, the PCB footprint of the part.

GOp locking allows you to lock any object in a Capture design. You can lock the design, the schematic folders within the design, the pages within the schematic folders and the objects on the schematic pages.

This section covers:

- Locking and Unlocking Objects in a design on page 345
- Features of a Locked Schematic Page object on page 346
- Features of a Locked Schematic Page on page 347
- Features of a Locked Schematic Folder on page 347
- Features of a Locked Design on page 348
- Cascading and roll-up effects of Locking on page 348

Locking and Unlocking Objects in a design

You can lock (and subsequently unlock) any object in a Capture project. You can lock the objects on a schematic page, the pages in a schematic folder, the folders in a design, and the design in a project.

To lock an object in Capture

1. Select the object to lock.

   For schematic page objects, you can use the multi-select feature on the schematic page to select and lock multiple objects simultaneously.

   For Project manager objects (pages, folders and designs), you select the objects in the Project manager.

   Note: You cannot lock multiple Project manager objects simultaneously.

2. From the Edit menu choose the Lock menu item.

   Alternatively, you can right-click on the object (on the page or in the Project manager) and choose the Lock item in the pop-up menu.

   When you lock a schematic page object the look-and-feel of the object when it is selected is changed.

   When you lock a Project manager object, a lock symbol appears over the icon of the object in the Project manager.

Note: After locking (or unlocking) one or more objects on a design, the lock (or unlocked) state of the objects must be saved. For exmaple, say you lock one or more objects on a schematic page.

After locking the objects, if you close the page without saving changes, the lock state of these objects is lost.

Note: If you lock one or more objects in a design, export the design and then again import the design, all the locks on the imported design are lost.

To unlock an object n Capture

1. Select the object to unlock.

   For schematic page objects, you can use the multi-select feature on the schematic page to select and unlock multiple objects simultaneously.

   For Project manager objects (pages, folders and designs), you select the objects in the Project manager. However, you cannot unlock multiple Project manager objects simultaneously.

2. From the Edit menu choose the UnLock menu item.

Note: The lock and unlock menu items (in the Edit menu or the pop-up menu) are disabled or enabled depending on the lock state of the selected object (or objects).

Features of a Locked Schematic Page object

- The object cannot be deleted or cut.
- The object cannot be moved to another part of the page (using a cut-and-paste operation or a mouse drag operation).
- The object cannot be moved to another page (using a cut-and-paste operation or a mouse drag-and-drop operation).
- The object can be copied to another page or as another instance on the current page. However, the copied instance of the object is locked as soon as you paste it on the page.
- If the locked object is a part, the part editor for the object is inaccessible. This means that the menu option to open the part editor for a locked part is unavailable.
- The replace or update cache operations will fail if they effect a locked part. Say a design contains multiple instances of a part where some instances are locked and some are unlocked. In this

case, the replace or update cache operations on a part with multiple instances will fail if these operations effect the locked instances. This means that these operations will not update even on the unlocked part instances.

- The Update All operation on an unlocked part instance (executed in the edit part procedure) will fail if this operation effects a locked part instance. This means that this operation will not effect even on the unlocked part instances.

Since, this type of locking is graphical so you are still permitted to edit the properties of a locked part. This implies that you can open the property editor for a locked object and add, modify or delete properties on the part.

Features of a Locked Schematic Page

- The page cannot be deleted or cut.
- The page cannot be moved to another schematic folder (using a cut-and-paste operation or a mouse drag-and-drop operation).
- The page cannot be renamed.
- Schematic page objects cannot be added to the page. This implies that an object cannot be placed on a locked page using the Place command. Also, an object cannot be placed on a locked page by copying the object from another page and pasted it onto the locked page.
- The page can be copied to another folder. However, the copied page is locked as soon as you paste it to the destination folder.
- All the page objects are locked as soon as the page is locked. Also, objects on a locked page may be explicitly unlocked. For details on the cascading and roll-up effects of locking pages see the section Cascading and roll-up effects of Locking.

Features of a Locked Schematic Folder

- The folder cannot be deleted or cut.
- The folder cannot be moved to another design (using a cut-and-paste operation or a mouse drag-and-drop operation).
- The folder cannot be renamed.

- Schematic pages cannot be added to the folder.
- The make root property of a locked schematic folder cannot be modified.
- The folder can be copied to another design. However, the copied design is locked as soon as you paste it to the destination design.
- All the pages are locked as soon as the folder is locked. Also, pages in a locked folder may be explicitly unlocked. For details on the cascading and roll-up effects of locking folders see the section Cascading and roll-up effects of Locking.

Features of a Locked Design

- Schematic folders cannot be added to the design.
- All the folders are locked as soon as the design is locked. Also, folders in a locked design may be explicitly unlocked. For details on the cascading and roll-up effects of locking designs see the section Cascading and roll-up effects of Locking.
- Design operations, netlisting, annotations, DRC and permitted on a locked design. You can also simulate a locked design.

  Note: However, if you run these commands on a locked design, and this causes a graphical change in the design, Capture allows the change but it will immediately be locked onto the design.

  Say you run the DRC on a locked design (or the DRC effects locked objects in the design). If the design has any DRC errors or warnings, Capture allows the process to place the markers even on locked object of the design. However, if a marker is placed on a locked page, the marker is immediately locked and you will need to either unlock the page or the marker if you need to remove the marker.

Cascading and roll-up effects of Locking

When you lock a container object (a page, a folder, or a design), all the objects within the container are also locked. Also, this process cascades down to the lowest level object.

So, if you lock a page, all the objects on the page are locked. If you lock a folder, all the pages contained in the folder are locked. In addition, the objects on each of the pages are locked.

Note: Unlocking has the same cascading effect on a container and the objects within the container.

When you lock a container object, you can unlock specific objects within the locked container by explicitly unlocking these. However, since locking and unlocking does not cause a roll-up effect, the unlock operation does not unlock the object container.

When you lock a container object, a lock symbol appears over the container icon in the Project manager. Now, if you explicitly unlock one or more objects within the locked container, the lock symbol remains but it changes to an open lock. This indicates that the container is locked but one or more objects within the container are unlocked.

The locking operation on an object within a container is specific to the object. This implies that the lock (or unlock) operation on an object overrides the operation on the object container. Consider the example of a folder, SCHEMATIC1, containing two pages, PAGE1 and PAGE2.

1. Lock PAGE2.
2. Lock SCHEMATIC1.

   Since locking is a cascading operation, locking SCHEMATIC1 effects the lock status of its pages. In this case, since PAGE2 is assigned locked state, so the cascading operation will effect only PAGE1.

   The lock operation did not effect PAGE2 not because the page was already locked but because the lock (or unlock) state on an object overrides the locked (or unlocked) state of the container.
3. Unlock SCHEMATIC1.

   Again, due to the cascading effect of unlocking, the pages within SCHEMATIC1 are unlocked.

   However, since PAGE2 was locked specifically and not as part of the cascading lock on SCHEMATIC1, the cascading lock operation will not effect the lock state of PAGE1.

Locking (or unlocking) a container does not necessarily imply that the state of the entire contents of the container will be effected by operation. So objects within the container are assigned their own lock (or unlock) state.

Dragging entities for moving and copying

You can use the standard Windows drag-and-drop operation to move or copy schematic folders, schematic pages, and libraries in the project manager windows. If you wish to copy rather than move, press and hold the CTRL key while you drag the entity.

If you drag a part that has a part alias, the part alias also moves. In the context of dragging and dropping, a symbol behaves just as a part does—as shown in the table below, a symbol can be dragged from a design or a library and dropped in another library.

A document that is open in an editor, or one that contains any open elements, cannot be dragged.

Documents can be dragged as indicated in the following table:

Drag from . . .	Part	Schematic Page	Schematic Folder
Design to design		X	X
Design to library	X	X	X
Schematic folder to schematic folder		X	
Library to design			X
Library to library	X		X

Note: If you copy or move a document from one design or library to another, you should save the destination design or library immediately. If you do not, you may lose data if you open the moved

document in the schematic page editor or part editor and then close the editor without saving the document.

You can use the standard Windows drag-and-drop operation to move or copy schematic folders, schematic pages, libraries, and symbols between projects, in the project manager windows. If you wish to copy rather than move, press and hold the CTRL key while you drag the entity.

1. If you are moving or copying a folder or page, verify that:
   - ❑ for a folder, no Capture editor is open on any document in the schematic folder.
   - ❑ for a page, that it is not open in any Capture editor.
2. Open both projects in their respective project managers.
3. Select the schematic folder, page, library, or symbol that you want to move or copy, then drag (pressing the CTRL key to copy) the selection to the destination project manager entity.
4. For both projects, from the File menu, choose Save All.

Note: If you copy or move a document from one design or library to another, you should save the destination design or library immediately. If you do not, you may lose data if you open the moved document in the schematic page editor or part editor and then close the editor without saving the document.

Note: Deleting schematic folders, schematic pages, parts and symbols is permanent. You cannot use the Undo command to bring back deleted items from the project manager.

Note: If you move or copy a parent schematic folder or schematic page from one project into a second project, Capture remembers the name and directory of the file containing the child schematic folder or folders. This information is stored in the Attach Implementation dialog box for each hierarchical block and nonprimitive part.

Undoing and repeating

If you make a mistake, you can use the Undo command. If you change your mind again, you can use the Redo command. Undo and Redo functionality is available in the schematic editor, the part editor

and the property spreadsheet. You can use Undo/Redo for any of the following:

- Object creation/deletion activities (for example, Cut, Copy, Paste, and Place commands).
- Object manipulation (for example, Move, Resize, Rotate, and Mirror commands)
- Property value modifications.

Note: Capture creates an “undo/redo” cache as you perform commands in the schematic editor and the property editor. Note that when you perform commands in the schematic editor, the undo/redo cache for the property editor is cleared, and vice versa. Also, note that certain other operations, such as Synchronize Up/Down cause the undo/redo cache to be cleared.

Multiple undo/redo operations

Further, you can undo/redo commands in the following ways:

- sequentially, exactly one command at a time.
- by setting label states. Label state enables you to tag the schematic at different stages of design. You can later use these tags to go to a particular stage of the design and then undo/redo a number of steps that were performed at that point in the design.

For example, suppose you had performed the following actions on a schematic page:

1. Place a part.
2. Label the schematic as stage1
3. Rotate the part by 90 degrees.
4. Wire one of the pins on the part to another part on the schematic page.
5. Place another part.
6. Label the schematic as stage2.

You could then use the Undo command sequentially to return the schematic page to its state at any point in this sequence. Alternately, suppose after step 5 you decide that instead of rotating the part by 90 degree, it would make better sense to rotate the part by 270 degrees, and change the wire-pin connections as well. In such a case, instead of undoing a number of steps, you can jump to the label state stage1. This will take you to the state of the schematic described in step 1. You can then do the modifications as required.

Note: Also, note that the part editor does not include an undo/redo cache. Therefore, in the part editor, you can only undo/redo a single command.

Using Undo/Redo for designs and schematic pages

You can use Undo/Redo independently for each schematic page in your design. That is, a separate cache of undo/redo data is maintained by Capture for each schematic page.

In complex hierarchical designs, there can be more than one occurrence of a particular schematic. When editing in this environment, objects and annotations are handled by separate mechanisms.

For objects, the edits are reflected in all the pages open on different occurrences of that page. If there are two pages open on two different uses of a schematic and you move an occurrence on one page, the occurrence will also move in the second page. When the user performs an UNDO, the state of the objects is restored on all occurrence pages identically.

For annotations edits are reflected uniquely in the occurrence pages. The annotation displayed by a view is selected by filter. UNDO in this case will restore the annotation value only on the particular occurrence page
For example consider the case of a reused instance with two occurrences H1/U1 and H2/U1. This instance has different annotations for these two occurrences. When the page is open on H1/U1, the Reference Designator displays as U25; when the page is open on H2/U1, the Reference Designator displays as U72.The

behavior of UNDO will be as shown in following sequence:

Command	Undo/redo	Schematic state
Open root schematic	disabled	Schematic displayed
Open occurrences H1/U1 and H2/U1	disabled	Occurrence pages displayed
Move a component in H1/U1	Undo Move	Component moved on both H1/U1 and H2/U1
Change reference designator on H1/U1 to from U25 to U50	Undo Text (Redo disabled)	H1/U1 (only) is changed.
Change reference designator on H2/U1 from U72 to U80	Undo Text (Redo disabled)	H2/U1 (only) is changed.
Undo	Undo Text (Redo enabled)	H2/U1 reference designator returned to U72 from U80.
Undo	Undo Move (Redo enabled)	H1/U1 reference designator returned to U25 from U50.
Undo	disabled	Component moved to its previous position on both H1/U1 and H2/U1.

Clearing the Undo/Redo cache

There are a number of operations that will clear the undo/redo cache (that is, these operations cannot be undone, nor can the schematic page be returned to a state that existed previous to the execution of these operations):

- Choosing Update Current or Update all after editing a part on a schematic page
- Replace Cache, Cleanup Cache, or Update Cache
- Edit Properties through the Browse/Find commands or through third-party tools
- Annotation, back-annotation, Update properties, Import Properties, or Cross Reference operations

To undo an action

➤ From the Edit menu, choose the Undo command.

Note: Deleting schematic folder, schematic pages, parts, and symbols is permanent. You cannot use the Undo command to bring back deleted items from the project manager.

To undo an Undo command

➤ From the Edit menu, choose the Redo command.

Shortcut

Toolbar:

Labeling wires and buses

You use aliases to connect electrical objects.

To place an alias

1. From the Place menu, choose Net Alias command.

2. Enter the net alias text, following the naming conventions for buses and bus members, then click OK. A rectangle representing the alias text is attached to the pointer. The tip of the pointer must be touching the net for you to place the net alias.
3. Use the mouse to move the alias text and click the left mouse button directly on the wire or bus. The alias text appears in the selection color.
4. Select the selection tool or press ESC, to dismiss the net alias tool.

To label a series of bus members

1. Use the Repeat command to place the bus members at regular intervals.
2. On the first bus member, place one alias, taking care to assign this bus member the lowest value in the bus range.
3. Place a net alias, using the left mouse button, on each member of the series.
4. Select the selection tool, or press ESC, to dismiss the net alias tool.

Shortcut

Tool palette:

To edit net alias text

1. Select the net alias.
2. From the Edit menu, choose the Properties command.
3. In the dialog box that appears, you can change the color, the font, the rotation, or the alias.
4. Click OK to dismiss the dialog box.

To move net alias text

➤ Select the net alias text and drag it to another location.

Note: As you place buses and wires, remember the following points:

- A bus and a wire can be connected only by name.
- If you begin or end a bus segment on a segment of a wire, a vertex is added to the wire and a junction appears, but the bus and wire are not electrically connected.
- If you begin or end a wire segment on a segment of a bus, a vertex is added to the bus and a junction appears, but the wire and bus are not electrically connected.
- Two buses or two wires can be connected physically.
- If you begin or end a bus segment on a segment of another bus, a vertex is added to the second bus, and a junction appears—the buses are connected.
- If you begin or end a wire segment on a segment of another wire, a vertex is added to the second wire, and a junction appears—the wires are connected.

Note: Capture preserves the case of part names and netnames, but ignores the case when comparing names for electrical connection. That means you may use uppercase or lowercase letters as you wish, but you need not remember the case.

Editing text and graphics

This section covers:

- "Specifying text font and size" on page 358
- "Moving and rotating text" on page 359
- "Replacing text" on page 360
- "Importing text" on page 360
- "Exporting text" on page 361
- "Creating graphics" on page 361
- "Drawing lines" on page 363
- "Drawing rectangles and squares" on page 364
- "Drawing ellipses and circles" on page 365

- "Drawing arcs" on page 366
- "Drawing elliptical arcs" on page 368
- "Drawing polylines" on page 371
- "Placing images" on page 372
- "Placing OLE Objects" on page 373
- "Placing IEEE symbols" on page 375

Text and graphics in schematics are not considered electrical components. That is, they do not have any effect on the netlist generated from the schematic. Text and graphics provide a method for you to document your schematic without effecting its connectivity.

Specifying text font and size

You may want text to have a distinctive appearance, or to fit a specific space. Capture supports TrueType fonts. You can preview a sample of the selected font before you choose it. You can also select the default font that you have established in the Fonts tab of the Design Template / Design Properties dialog box.

Note: At certain zoom scales, Capture substitutes filled rectangles for text that is too small to appear. These placeholders are for display only—the text prints correctly.

To specify font

➤ If you are placing the text, then from the Place menu, choose the Text command. The Place Text dialog box appears.

or

1. If the text has already been placed, then double-click on the text. The Edit Text dialog box appears.
2. In the Font group box, choose the Change button. The Font dialog box appears.

Tip

You can select the *Symbol* font set to specify symbols, such as omega (Ω.)

3. Select a font, a font style, or a size. Sample text appears in the Sample group box.
4. Click OK to close the Font dialog box.

Shortcut

Tool palette:

Moving and rotating text

You can change the location and the orientation of comment text at any time.

To move text

1. Select the text.
2. Drag the text to the new location.
3. Click an area where there are no parts or objects to deselect the text.

To resize the text area

1. Select the text.
2. Move the pointer over one of the text's selection handles, and press the left mouse button.
3. Without releasing, drag the pointer to the new location. The text box resizes. Text wraps inside the box to fit the new shape.
4. Release the left mouse button and click an area where there are no parts or objects to deselect the text.

To rotate text

1. Select the text.
2. From the Edit menu select the Rotate command. The text rotates 90 degrees counterclockwise.
3. Repeat step 2 as necessary.
4. Click an area where there are no parts or objects to deselect the text.

Replacing text

The content of text that you place in the schematic page editor or the part editor can be easily changed. You can enter the replacement text using the keyboard, or if you wish, you may copy the replacement text from another application.

To replace text

1. Select the text you want to replace.
2. From the Edit menu, choose the Properties command. The Edit Text dialog box appears with the text highlighted.
3. Enter the replacement text or press CTRL+V to paste text from the clip board, then click OK.

Importing text

You can import text from any Windows program that copies text to the Clipboard. This is especially useful to simplify creation of a programmable logic device.

To copy text from other Windows applications

1. In the other Windows application, copy the text to the clipboard using that program's Copy command.
2. Open the Capture schematic page editor or part editor.
3. From the Place menu, choose the Text command. The Place Text dialog box appears.

4. Press CTRL+V to paste the text into the text box, then verify that the color, font, and rotation are as you want them and click OK. A rectangle representing the text is attached to your pointer.
5. Use the mouse to move the text. Click the left mouse button to place the text at the desired location.

Exporting text

You can export Capture text to any application that features the Windows Clipboard.

To export text using the clipboard

1. In Capture, select the text you wish to export.
2. From the Edit menu, choose the Properties command. The Edit Text dialog box appears.
3. Select the text, and press CTRL+C.
4. Open the other Windows application and use that application's Paste command to place the text.

Creating graphics

You can create a wide variety of graphic shapes for your parts or to add to your schematic page. You can work with the snap-to-grid option turned on or turned off. For close work, you may want to try Zooming in on your graphic. To draw very precisely, use the Go To command on the View menu.

Before you begin drawing, you may want to specify default line and fill styles because all lines and shapes you draw adopt the current line style and closed shapes adopt the current fill style. You can use a variety of line types or fill styles for any schematic page or part.

To change the snap-to-grid option

➤ From the Options menu, choose the Preferences command, then choose the Grid Display tab. You set the option separately for the schematic page editor and the part editor.

To set a default line style

1. From the Options menu, choose the Preferences command and then choose the Miscellaneous tab.
2. Click on the Line Style and Width drop box to display the options. Note that you can specify separate options for the schematic page editor and the part editor.
3. Select one of the options and click OK. Any lines or shapes you draw will have this line style.

To define a default fill

1. From the Options menu, choose the Preferences command and then choose the Miscellaneous tab.
2. Click on the Fill Style drop-down list to display the options. Note that you can specify separate options for the schematic page editor and the part editor.
3. Select one of the options and click OK. Any closed shapes you draw will have this fill style.

To edit line style or fill style of a placed object

1. Select the object.
2. From the Edit menu, choose the Properties command.
3. Select another line style or fill style in the dialog box that appears, then click OK.

To draw an object

1. From the Place menu, choose the appropriate drawing command or select the appropriate drawing tool from the tool palette.
2. Use the mouse to draw the object. To constrain the object by the orthogonality rules, press and hold the SHIFT key while you draw.

Drawing lines

You use the line tool to draw a single line. The line you draw adopts the current line style. For information on setting the line style, see Creating graphics.

If you wish to draw a line with multiple contiguous segments, the polyline tool is very convenient.

To draw a line segment

1. From the Place menu, choose the Line command.
2. Move the pointer to the line's beginning.
3. Press and hold the left mouse button while moving the mouse to draw the line.
4. Release the left mouse button to end the line. The line appears in the selection color.
5. Select the selection tool or press ESC to dismiss the line tool.
6. Click an area where there are no parts or objects to deselect the line.

or

1. From the Place menu, choose the Line command.
2. Move the pointer to the line's beginning.
3. Click the left mouse button
4. Move the mouse, and click the left mouse button again to end the line. The line appears in the selection color.
5. Select the selection tool or press ESC to dismiss the line tool.
6. Click an area where there are no parts or objects to deselect the line.

Shortcut

Tool palette:

Drawing rectangles and squares

You use the rectangle tool to create orthogonal shapes; if you wish to create a polygon, use the polyline tool.

Any rectangles or squares you create will have the current fill style and line style. For information concerning line type and fill style, see Creating graphics.

To draw a rectangle or a square

1. From the Place menu, choose the Rectangle command.
2. Move the pointer to one corner of the intended rectangle.
3. Press and hold the left mouse button while you drag the mouse. The rectangle changes shape as you move the mouse. Release the left mouse button when you have the correct shape. To draw a square, hold down the SHIFT key while you perform this step. The rectangle or square appears in the selection color.
4. Choose the selection tool or press ESC to dismiss the rectangle tool.
5. Click on an area where there are no parts or objects to deselect the rectangle.

or

1. From the Place menu, choose the Rectangle command.
2. Move the pointer to one corner of the intended rectangle and click the left mouse button.
3. Move the mouse to a new location. The rectangle changes shape as you move the mouse. Click the left mouse button when you have the correct shape. To draw a square, hold down the SHIFT key while you perform this step. The rectangle or square appears in the selection color.
4. Choose the selection tool or press ESC to dismiss the rectangle tool.
5. Click on an area where there are no parts or objects to deselect the rectangle.

Shortcut

Tool palette:

Drawing ellipses and circles

You use the ellipse tool to draw an ellipse or a full circle.

Because they are closed shapes, circles and ellipses will have the current fill style. They will also have the current line style. For information concerning line style and fill style, see Creating graphics.

For details on drawing circular or elliptical arcs see Drawing arcs and Drawing elliptical arcs.

To draw an ellipse or a circle

1. From the Place menu, choose the Ellipse command.
2. Move the pointer to an edge of the intended ellipse.
3. Press and hold the left mouse button while dragging the mouse. The ellipse changes shape as you move the mouse. Release the left mouse button when you have the correct shape. To draw a circle, hold down the SHIFT key while you perform this step. The ellipse or circle appears in the selection color.
4. Choose the selection tool or press ESC to dismiss the ellipse tool.
5. Click on an area where there are no parts or objects to deselect the ellipse.

OR

1. From the Place menu, choose the Ellipse command.
2. Move the pointer to an edge of the intended ellipse and click the left mouse button.
3. Move the mouse to a new location. The ellipse changes shape as you move the mouse. Release the left mouse button when you have the correct shape. To draw a circle, hold down the SHIFT key while you perform this step. The ellipse or circle appears in the selection color.

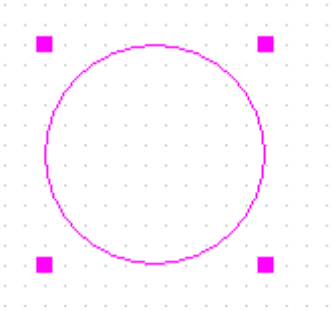
4. Choose the selection tool or press ESC to dismiss the ellipse tool.
5. Click on an area where there are no parts or objects to deselect the ellipse.

Shortcut

Tool palette:

To edit an ellipse or a circle

When you select an ellipse, four handles are made visible around the shape. Click and drag any of these handles to alter the shape.



Drawing arcs

You create a circular arc of any angle using the arc tool. Because it is a line, the arc adopts the current line style. For more information about setting line styles, see Creating graphics.

To draw elliptical arcs, see Drawing elliptical arcs.

To create a full circle, use the ellipse tool.

To draw a circular arc

1. From the Place menu, choose the Arc command.
2. Move the pointer to the center of the arc and click the left mouse button.

3. Use the mouse to establish the radius of the arc; click the left mouse button to mark the start the arc.

   The arc is drawn counterclockwise from this start point.

4. Move the mouse along the path of the circle to draw the arc and click the left mouse button to mark the end of the arc.

   The arc appears in the selection color.

5. Choose the selection tool or press ESC to dismiss the arc tool.

or

1. From the Place menu, choose the Arc command.
2. Move the pointer to the center of the arc and press the left mouse button.
3. Drag the mouse and then release the left mouse button to establish the radius of the arc and the location of the start of the arc.

   The arc is drawn counterclockwise from this start point.

4. Move the mouse along the path of the circle to draw the arc and click the left mouse button to mark the end of the arc.

   The arc appears in the selection color.

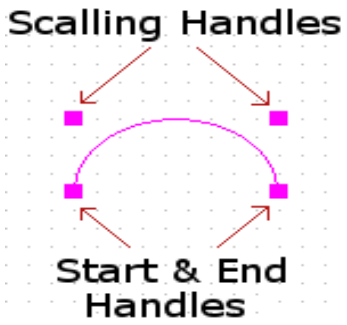
5. Choose the selection tool or press ESC to dismiss the arc tool.

Shortcut

Tool palette:

To edit an arc (circular or elliptical)

Use the start and end handles to increase or decrease the size of the arc. You the scaling handles to scale or re-shape the arc.



Drawing elliptical arcs

You create an elliptical arc of any angle using the elliptical arc tool. Because it is a line, the arc adopts the current line style. For more information about setting line styles, see Creating graphics.

To draw circular arcs, see Drawing arcs.

To create a full ellipse, use the ellipse tool.

To draw an elliptical arc

1. From the Place menu, choose the Elliptical Arc command.
2. Move the pointer to the top or bottom of the arc and click the left mouse button.
3. Move the mouse to the start point; click the left mouse button.

   The arc is drawn counter-clockwise from this start point.
4. Move the mouse along the path of the ellipse to draw the arc and click the left mouse button to mark the end of the arc.

   The arc appears in the selection color.
5. Choose the selection tool or press ESC to dismiss the arc tool.

or

1. From the Place menu, choose the Arc command.
2. Move the pointer to the top or bottom of the arc and click the left mouse button.

3. Drag the mouse and then release the left mouse button to mark the start of the arc.

   The arc is drawn counterclockwise from this start point.

4. Move the mouse along the path of the ellipse to draw the arc and click the left mouse button to mark the end of the arc.

   The arc appears in the selection color.

5. Choose the selection tool or press ESC to dismiss the arc tool.

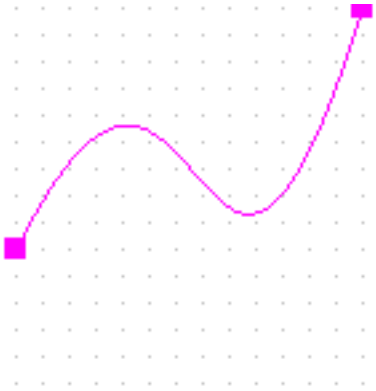
Shortcut

Tool palette:

To edit an elliptical arc see To edit an arc (circular or elliptical).

Drawing Bezier Curves

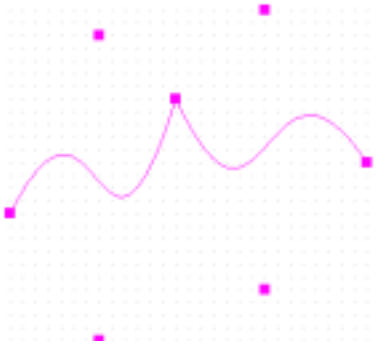
Bezier curves are defined using a start point, two control points and an end point. The two control points define the gradient of the curve. These two points control the shape of the curve. The entire curve is a blend of the four points that make up the curve.



To draw a Bezier curve

1. From the Place menu, choose the Bezier command
2. Click the left mouse button on the canvas to mark the start point of the curve.
3. Click the left mouse button to mark the first control point.

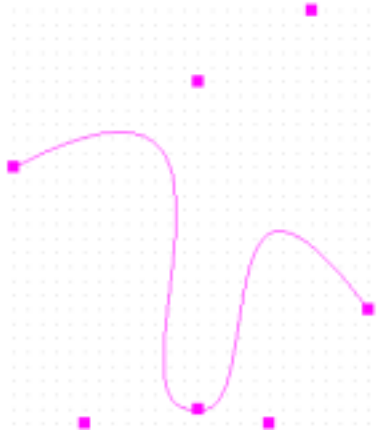
4. Click the left mouse button again to mark the second control point.
5. Click the left mouse button to mark the end point of the curve.;
6. Select the selection tool or press ESC to dismiss the Bezier curve tool.



Extending the four-point curve

After you have drawn the four points of the Bezier curve, you can mark a fifth point on the canvas. You will notice that the shape from the forth to fifth points is a straight line. Here the end point of the first curve is the start point of a second four-point curve. You can then continue to make any number of four-point Bezier curves, each starting and the end of the previous curve.

You will also notice that the point connecting two contiguous four-points curve forms a sharp edge. If required, select and move this point to smoothen out this edge. You can thus create a curve with any number of control points.



To edit a Bezier curve

1. Select and move the start or end points of the curve to alter the start or end positions of the curve.
2. Select and move the two control points of the curve to alter its gradient.

Shortcut

Tool palette:

Drawing polylines

When you wish to draw a line with multiple contiguous segments, the polyline tool is very convenient. The line you draw adopts the current line style. Polygons can be created with the polyline tool; these polygons adopt the current fill style. For information on setting the line style, see Creating graphics.

Drawing polylines behaves like placing wires. Polylines automatically default to drawing with square corners. You can draw non-orthogonal polylines simply by holding SHIFT while you draw.

To draw a polyline

1. From the Place menu, choose the Polyline command.
2. Click the left mouse button to begin drawing, click to change directions, and double-click to end the final segment. To constrain the direction changes to multiples of 90 degrees, press SHIFT. After you double-click, the polyline appears in the selection color.
3. Click an area where there are no parts or objects to deselect the polyline.
4. Select the selection tool or press ESC to dismiss the polyline tool.

To draw a polygon

➤ Follow the instructions above, ending the line with a single mouse-button click at the beginning point. The polygon adopts the current line and fill style.

Shortcut

Tool palette:

Placing images

You can create a image in another application and place it on a schematic page or library part, or in a custom title block.

To place an image

1. From the Place menu, choose the Picture command. The Open dialog box appears.
2. Select the image file. If the file is not listed in the File Name box, do one or more of the following:
   - ❑ In the Look in box, select a new drive, directory, or both.
   - ❑ In the Files of type box, select the type of file you wish to open.
3. Click OK. A rectangle representing the image is attached to the pointer.
4. Use the mouse to move the image and click the left mouse button to place the image at the desired location. If you wish to place multiple copies of the image, simply repeat this step.
5. Select the selection tool to dismiss the picture tool.

Note: Capture supports many different image file formats these include: BMP, JPEG, JPG, JPE, JFIF, GIF and PNG.

Placing OLE Objects

You can place objects of other applications on your schematic page using the OLE Object command. This allows to you embed or link an external application file into your schematic page. This provides the ability to package other files (or links to files) along with your schematic.

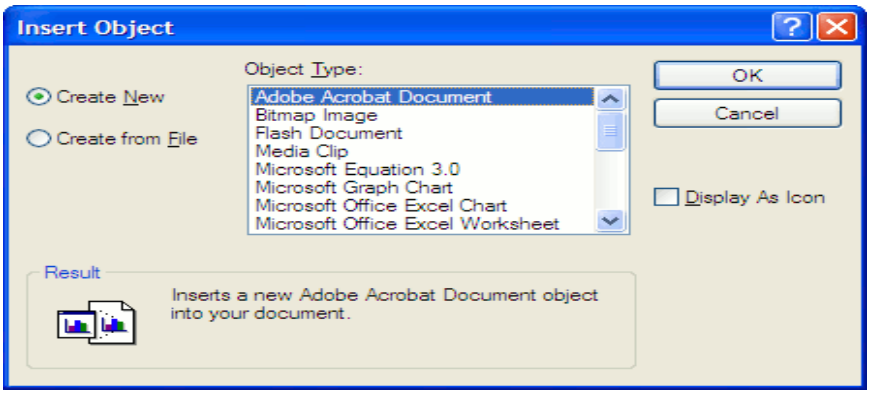
For example, you may want to embed a PDF document on a schematic page. Or you want to place and link an Excel document on a page.

Capture allows you to add an existing external file to your schematic as an OLE object. Alternatively, It allows you to add a new instance of an application file.

To place a new OLE object on a page

1. From the Place menu choose OLE Object.

   The Insert Object dialog box displays



   The Create New radio button is selected by default.

2. From the Object Type list, choose the new object type to embed on the schematic page.

Important

   Choose only object types for which you have the associated application installed on your computer.

3. Click OK.

The cursor changes into the cross-hair cursor indicating that Capture is now in the Place OLE Object mode.

4. Click the mouse button at the point where you want to start the object and drag the cursor to draw a rectangular area to contain the object.

   Notice that as soon as you release the mouse button, the Capture toolbar now includes the toolbar for the application associated with the OLE object type. For example, if you select Bitmap Image type, the Capture toolbar includes the Microsoft Paint toolbars.

   You can now make changes to the OLE object using the associated application toolbar and edit features from within Capture.

5. When you are done making changes to the new object, click anywhere on the schematic page outside the object.

   Notice now that the toolbars for the associated application are not available in Capture.

The OLE object is now embedded in your schematic page and the contents will be saved along with your schematic page.

To edit the OLE object, double-click on object in the schematic page, the associate application toolbars are included within Capture and you can now make changes to the object.

To place an existing OLE object on a page

1. From the Place menu choose OLE Object.

   The Insert Object dialog box displays

   The Create New radio button is selected by default.

2. Choose the Create From File radio option.

   You can either enter the name of the file or you can browse for the file on the file system.

   Choose the Link option to embed a reference of the file, else the file itself is embedded on your page.

Choose the Display as Icon option to display the icon for the application associated with the file.

3. Click OK.

   The cursor changes into the cross-hair cursor indicating that Capture is now in the Place OLE Object mode.

4. Click the mouse button at the point where you want to start the object and drag the cursor to draw a rectangular area to contain the object.

   Notice that as soon as you release the mouse button, the Capture toolbar now includes the toolbar for the application associated with the OLE object type. For example, if you select Bitmap Image file, the Capture toolbar will include the Microsoft Paint toolbars.

   You can now make changes to the OLE object using the associate application toolbar and edit features from within Capture.

5. When you are done making changes to the new object, click anywhere on the schematic page outside the object.

   Notice now that the toolbars for the associated application are not available in Capture. Capture is now in the schematic page editor mode.

   The file you selected is either embedded or linked on your schematic page.

   If you choose to embed a file, any changes to the original file will not be reflected on the OLE object on the schematic page. However, if you link the file, any changes you make on the OLE object on the schematic page will be reflected on the file (available on the file system). Also, any change you make on the file on the file system will be reflected on the OLE object on your schematic page.

Placing IEEE symbols

You can place IEEE symbols directly onto your schematic to represent mechanical components. Again, remember that these symbols do not have an effect when you generate a netlist for your schematic.

To place an IEEE symbol

1. From the Place menu, choose the IEEE Symbol com\mand. The Place IEEE Symbol dialog box appears.
2. From the Symbols list, select a symbol. The symbol appears in the preview box.
3. When the appropriate symbol is selected, click OK. The symbol is attached to your pointer.
4. Use the mouse to move the symbol and click the left mouse button to place the symbol.
5. Select the selection tool to dismiss the symbol tool or repeat step 4 to place additional symbols.

Shortcut

Tool palette:

Editing wire and bus properties

To drag a segment orthogonally

➤ Select the segment and drag it to the new location. The wire or bus stretches orthogonally to maintain connectivity.

To drag a segment non orthogonally

➤ Hold the SHIFT key while you select the end point and drag the wire. The selected end of the wire moves in any direction while the opposite end remains in place.

Note: When you click on a wire segment, only that segment and its two handles are selected.

Note: When you drag a part or wire to another location and that change affects connectivity, Capture flags a warning with a changed cursor ( ) and temporary markers ( ) on your schematic. Visible and off-screen connectivity changes are saved in the session log, if you complete the operation. Moreover, Capture now provides you the following UI options to control the drag operation:

- A check box named *Allow component move with connectivity changes* in the Miscellaneous tab of the Preferences dialog box.
- A toolbar button

The following describes the usage of the UI options:

- If the check box is selected or the toolbar button is in the state, then Capture will allow you to drag and place the selected part or wire on the schematic, even if it results in connectivity changes. Also, Capture will flag a warning with a changed cursor and will show the temporary markers. However, if the check box is not selected or the toolbar button is in the state, then the selected part or wire attaches to the cursor and does not get placed on the schematic, if it results in connectivity changes. Also, Capture flags only a warning with a changed cursor and does not show the temporary markers.

To move a wire or bus

1. Select the wire or bus.
2. Hold the ALT key while you move the wire or bus. The wire or bus segment breaks connectivity with the rest of the net.

Note: Moving pins connected to wires may cause wires to drag, but moving a wire always causes disconnection from pins, ports, and other objects.

To copy a wire

➤ Hold the CTRL key while you drag the wire.

To move a vertex

1. Select a wire segment next to the vertex.
2. Drag the vertex to the new location. One segment of the wire or bus stretches to the new location. The other segment breaks connectivity.

To delete a wire or bus segment

1. Select the segment.
2. Press the DELETE or BACKSPACE key.

To delete a net

1. Select one segment of the net.
2. Click the right mouse button. A pop-up menu appears.
3. From the pop-up menu, choose the Select Entire Net command.
4. Press the DELETE or BACKSPACE key.

To edit wire properties

➤ Select the wire or bus, then from the Edit menu, choose the Properties command. The property editor appears.

or

➤ Double-click on the wire or bus. Capture displays the property editor.

Note: As you place buses and wires, remember the following points:

- ❑ A bus and a wire can be connected only by name.
- ❑ If you begin or end a bus segment on a segment of a wire, a vertex is added to the wire and a junction appears, but the bus and wire are not electrically connected.
- ❑ If you begin or end a wire segment on a segment of a bus, a vertex is added to the bus and a junction appears, but the wire and bus are ***not*** electrically connected.
- ❑ Two buses or two wires can be connected physically.
- ❑ If you begin or end a bus segment on a segment of another bus, a vertex is added to the second bus, and a junction appears—the buses are connected.
- ❑ If you begin or end a wire segment on a segment of another wire, a vertex is added to the second wire, and a junction appears—the wires are connected.

Editing wire and bus look & feel

You can change the look and feel of a wire or a net on a schematic page by changing the color, line style or line width.

To edit the look and feel of a wire or bus

1. Click on a wire or bus on the page.
2. Right-click the wire or bus to display the pop-up menu.
3. Click the Edit Wire Properties option.

   The Edit Properties dialog box displays.

   The dialog box contains three drop-down lists to edit the line style, line width and color of the wire.
4. Make the required selections in the drop-down lists and click Ok.

Note: Choose the Default option in any of the drop-downs to revert the style of the wire to the OrCAD Capture default.

To edit the look and feel of a net

1. Click on a net on the page.
2. Right-click the net to display the pop-up menu.
3. Click the Edit Net Properties option.

   The Edit Properties dialog box displays.

   The dialog box contains three drop-down lists to edit the line style, line width and color of the wire.
4. Make the required selections in the drop-down lists and click Ok.

Note: Choose the Default option in any of the drop-downs to revert the style of the net to the OrCAD Capture default.

Combining wire and net look and feel

If you change the look and feel of a wire in a net and then change the look and feel of the net, the properties of the wire will override the properties of the net.

Scenario 1

Say a net contains two sections (wires).

Select one wire in the net and change the color property of the wire to Red.

The color of the other wire in the net is not effected.

Now select the net and change the color of the entire net to Blue.

The color of the second wire in the net changes to Blue. However, the color of the first net remain Red.

This is because the custom properties of a wire will override the properties of a net.

Scenario 2

Say a net contains two sections (wires),

Select one wire in the net and change the color property of the wire to Red.

The color of the other wire in the net is not effected.

Now select the net and change the color of the entire net to blue.

The color of the second wire in the net changes to Blue. However, the color of the first net remain Red.

Again, change the color of the wire to Default.

The wire color changes to Blue.

This is because the wire now inherits the color of the net.

Working with macros

This section covers:

- "Recording and saving a macro" on page 383
- "Playing a macro" on page 386
- "Creating macro shortcut keys" on page 387

- "Macro selection commands" on page 388
- "Macro editing commands" on page 392
- "Macro placement commands" on page 398
- "Macro viewing commands" on page 409
- "Macro property commands" on page 413
- "Editing VHDL and Verilog files" on page 417

Note: For more information on macro language, see Language Reference (*ENDUSER.doc*) in your Capture installation directory.

Capture's macro capability is a subset of Visual Basic for Applications. When you record macros in Capture's schematic page editor, Capture writes a .BAS file. You can edit this file later, or write your own.

Each macro must be written in a single MAIN function, and not use IF-THEN-ELSE subroutines.

Capture provides a macro command for each menu command in the schematic page editor. In some cases, a macro command cannot specify all of the values presented in the dialog box it opens. For example, you cannot add or edit properties using the PlacePart macro command.

Commands that change the active window are not available to macros. The following commands are unavailable to macros:

- Ascend Hierarchy
- Descend Hierarchy
- Edit Part (on the pop-up menu)
- Undo
- Redo

The Undo command rolls back the macro file to the start of the previous command. The Redo command repositions the file to the end of the previous command.

In a macro file, anything following a single quotation mark (') is ignored as comment text. The pause button automatically adds the following comment line:

```
'PAUSE. . .
```

Selection commands

Use the selection commands to select objects. For more information, see Macro selection commands.

Editing commands

Use the editing commands to edit selected objects. For more information, see Macro editing commands.

Placement commands

Use the placement commands to place new objects. For more information, see Macro placement commands.

Viewing commands

Use the viewing commands to access the View menu more quickly. For more information, see Macro viewing commands.

Property commands

Use the property commands to edit the properties of selected objects. For more information, see Macro property commands.

Input boxes

Use input boxes to customize your macro commands. For more information, see Macro input boxes.

Recording and saving a macro

In the schematic page editor, you can record a series of editing actions as a macro. When you record a macro, Capture assigns it a temporary name, and it is treated as a temporary macro. Temporary macros can be run during the current Capture session, but they are not saved for use in subsequent Capture sessions. You can make a temporary macro permanent by assigning it a name in the Configure Macro dialog box.

In general, you can record a macro command for each menu command available in the schematic page editor. However, because the macro commands are limited to the schematic page editor window, the following commands are unavailable:

- Ascend Hierarchy
- Descend Hierarchy
- Edit Part (on the pop-up menu)
- Undo
- Redo

The Undo command rolls back the macro file to the start of the previous command. The Redo command repositions the file to the end of the previous command.

After you record a macro, you can give it a name, a menu entry, an access key definition, and a description. Once you give a macro a name and save it, it will automatically appear in the macro name list box in the Configure Macro dialog box. The text you enter as the menu entry appears in the Macro menu, along with the macro's access key definition, if you specified one. The text you enter as the description appears in the Description text box in the Configure Macro dialog box when you select the macro name.

To record a macro

1. Click the left mouse button on the schematic page to set a location to begin recording the macro.
2. From the Macro menu, choose Record. Capture displays the macro recorder tool palette.

or

1. From the Configure Macro dialog box, choose Record.
2. Perform the series of edits that you want to record as a macro, using the three macro record buttons as necessary. The buttons perform the following tasks:
3. Use the left button to stop recording the macro.
4. Use the center button to pause recording. The pause mode is in effect until you choose the center button again.
5. Use the right button to cause a command to record in a "with dialog" mode. If a command is recorded in this mode, the value you enter while recording the macro is not saved. Instead, when the macro is run, the command displays a dialog box so that you can fill in a value. When recording the "with dialog" mode is in effect until you choose the right button again.
6. Choose the left macro record button to stop recording the macro.

To save a configured macro

1. From the Macro menu, choose the Configure command. Capture displays the Configure Macro dialog box.
2. In the Macro Name text box, enter a name for the macro.
3. Click Save. Capture displays the Macro Name dialog box.
4. If you want to assign an access key, enter an access key or key combination (for example, CTRL+7) in the Keyboard Assignment text box.

   Note: Do not assign the access key combination CTRL+ALT+DEL to a macro. Capture's macro system won't override this combination to restart your system.

   Note: Macro shortcuts may be any alphanumeric character or a function key (like F7), and may additionally use the CTRL, SHIFT, and ALT keys. For example, CTRL+SHIFT+Q and F6. For more information, see Creating macro shortcut keys.
5. If you want the macro to appear as an entry in the Macro menu, enter the appropriate text (for example, "Name Wires") in the Menu Assignment text box.

Note: You can make an access key for a macro by placing an ampersand character (&) in front of one letter in the Menu Assignment text box of the Macro Name dialog box. For example, "&Name Wires" creates the access key combination ALT, M, N to use a macro that is configured to appear as "Name Wires" in the Macro menu.

6. If you want to further describe the macro, enter the appropriate text in the Description text box.
7. Click OK. The Save As dialog box appears.
8. Select an appropriate file location and file name, then click Save.
9. In the Configure Macro dialog box, click the Close button.

To add a macro

➤ From the Macro menu, choose the Configure command. Capture displays the Configure Macro dialog box.

To remove macro

➤ From the Macro menu, choose the Configure command. Capture displays the Configure Macro dialog box.

The following macro file searches for three specific kinds of parts and adds a Cost property with a value for each one. The first line in each set finds and selects all parts of a specific type. Once the parts are selected, the second line of each set changes the value of Cost to the specified value. If the part doesn't have the Cost property, then the property is created. The final line of each set makes the value of the Cost property visible.

The first set of lines search for and edit 74LS04 type parts. The second set of lines search for and edit 74LS08 type parts. The last set of lines search for and edit 74LS32 type parts.

When this macro is configured, it will appear in the lower portion of the Macro menu. The name of the command on the menu is "Cost". In addition to being chosen from the menu with the mouse, the macro can be reached with the access keys ALT, M, O and the shortcut CTRL+1.

```
Macro commands are reserved words, and should not be used for
     macro function or procedure names.

SUB Cost

'MACROMENU &Cost
     'MACROKEY CTRL+1
     'MACRODESCRIPTION Adds a price to a known set of parts.

FindParts "74ls04", FALSE
     SetProperty "Cost", "$0.70"
     DisplayProperty "Cost", "Arial", 9, FALSE, FALSE, 48, 0

FindParts "74ls08", FALSE
     SetProperty "Cost", "$0.75"
     DisplayProperty "Cost", "Arial", 9, FALSE, FALSE, 48, 0

FindParts "74ls32", FALSE
     SetProperty "Cost", "$0.80"
     DisplayProperty "Cost", "Arial", 9, FALSE, FALSE, 48, 0

END SUB
```

Playing a macro

To play the currently selected macro

1. Click the left mouse button on the schematic page to set a starting location for your macro.
2. From the Macro menu, choose the Play command.

or

1. Click the left mouse button on the schematic page to set a starting location for your macro.
2. From the Configure Macro dialog box, choose Play.

To play a macro

1. Click the left mouse button on the schematic page to set a starting location for your macro.
2. If the macro appears in the Macro menu, choose it from the menu.

or

1. Click the left mouse button on the schematic page to set a starting location for your macro.
2. If the macro appears in the Macro menu and has an access key, press ALT, M, X where X is the letter or number corresponding to the macro command. For example ALT, M, N for a macro called "Name Wires."

or

1. Click the left mouse button on the schematic page to set a starting location for your macro.
2. If the macro has a shortcut key or keys, press the shortcut key or keys. For example, if "Name Wires" uses CTRL+F6 then press CTRL+F6.

Creating macro shortcut keys

You can make an access key for a macro by placing an ampersand character (&) in front of one letter in the Menu Assignment text

box of the Macro Name dialog box. For example, "&Name Wires" creates the access key combination ALT, M, N to use a macro that is configured to appear as "Name Wires" in the Macro menu.

You can also create a shortcut key for a macro command, using the Keyboard assignment text entry box in the Macro Name dialog box. Use the following form to assign a macro shortcut key, where **blue** indicates a required value and **red** indicates an optional value.

modifier + keydescription

The value for ***modifier*** can be one of the following:

- CTRL
- ALT
- SHIFT
- CTRL+ALT
- CTRL+SHIFT
- ALT+SHIFT

- CTRL+ALT+SHIFT

The value for ***keydescription*** can be one of the following:

- A..Z. Any alphabetic character.
- 0..9. Any numeric character.
- F1..F24. Any one function key.

The following examples are possible combinations:

- F1
- CTRL+SHIFT+5
- ALT+B

Note: Do not assign the access key combination CTRL+ALT+DEL to a macro. Capture's macro system won't override this combination to restart your system.

Note: The ESC key can be used as a shortcut key, but cannot be used in junction with any other key. For example, SHIFT+ESC is not a valid shortcut key.

Note: The keys "." and "=" do not work in macro key sequences.

Macro selection commands

The macro selection commands are:

- "FindBookmarks" on page 389
- "FindDRCMarks" on page 389
- "FindHierarchicalPorts" on page 390
- "FindNets" on page 390
- "FindOffPageConnectors" on page 390
- "FindParts" on page 390
- "FindText" on page 391
- "SelectAll" on page 391
- "SelectBlock" on page 391

■ "SelectObject" on page 392

Use the macro selection commands to find and select objects. If Capture finds multiple objects that meet the selection criteria, it places them in a rectangular selection set, and changes the CurrentLocation value to the rectangle's upper left corner. If Capture finds only one object, it selects the object and changes the CurrentLocation value to the upper left corner of the object. If no objects are found, nothing is selected, and the current location is left unchanged.

In the following macro command descriptions, **Red** indicates a decimal number value. **Blue** indicates a value of either TRUE or FALSE. **Magenta** indicates any character string.

Note: Macro commands are reserved words, and should not be used for macro function or procedure names.

FindBookmarks

FindBookmarks "*value*", *matchcase*

Function: Use this command to select bookmarks with a property name or property value that matches ***value***. If ***matchcase*** is TRUE, the search for ***value*** is case sensitive.

Example:

```
FindBookmarks "Bookmark1", TRUE
```

FindDRCMarks

FindDRCMarks "*value*", *matchcase*

Function: Use this command to select all DRC markers with a property with a value of ***value***. If ***matchcase*** is TRUE, the search for ***value*** is case sensitive.

Example:

```
FindDRCMarks "74LS32", TRUE
```

FindHierarchicalPorts

FindHierarchicalPorts "*value*", *matchcase*

Function: Use this command to select hierarchical ports with a property with a value of ***value***. If ***matchcase*** is TRUE, the search for ***value*** is case sensitive.

Example:

```
FindHierarchicalPorts "A", FALSE
```

FindNets

FindNets "*value*", *matchcase*

Function: Use this command to select all nets that have a property with a value of ***value***. If the selection consists of a single net, then CurrentLocation is set to the net's upper left vertex. If ***matchcase*** is TRUE, the search for ***value*** is case sensitive.

Example:

```
FindNets "Carry", FALSE
```

FindOffPageConnectors

FindOffPageConnectors "*value*", *matchcase*

Function: Use this command to select off-page connectors with a property name or property value that matches ***value***. If ***matchcase*** is TRUE, the search for ***value*** is case sensitive.

Example:

```
FindOffPageConnectors "A", FALSE
```

FindParts

FindParts "*value*", *matchcase*

Function: Use this command to select all part instances that have a property value that matches ***value***. If ***matchcase*** is TRUE, the search for ***value*** is case sensitive.

Example:
```
FindParts "74LS00", FALSE
```

FindText

FindText "*value*", *matchcase*

Function: Use this command to select text with a property value that matches ***value***. If ***matchcase*** is TRUE, the search for ***value*** is case sensitive.

Example:
```
FindText "a line", TRUE
```

SelectAll

SelectAll

Function: Use this command to select all objects in the page. CurrentLocation is unaffected.

Example:
```
SelectAll
```

SelectBlock

SelectBlock *X1, Y1, X2, Y2, SelectID*

Function: Use this command to select the set of objects contained in the area identified by the rectangle at the coordinates CurrentLocation + (X1, Y1) and CurrentLocation + (X2, Y2). Object selection is controlled using the rules chosen on the Select tab in the Preferences dialog box. If ***SelectID*** is TRUE, then previously selected objects remain selected. If ***SelectID*** is FALSE then previously selected objects are deselected.

Example:
```
SelectBlock -1.00, -1.00, -5.00, -5.00, TRUE
```

SelectObject

SelectObject *X*, *Y*, *SelectID*

Function:

Use this object to select the object as the CurrentLocation + (***X***, ***Y***), or deselect any currently selected objects at that location. If an object is selected, the CurrentLocation is set to the upper left corner of the object. If no object is selected at the location (***X***, ***Y***), then the selection set is empty and the CurrentLocation is set to CurrentLocation + (***X***, ***Y***). If ***SelectID*** is TRUE, then previously selected objects remain selected. If ***SelectID*** is FALSE then previously selected objects are deselected.

Example:

```
SelectObject -1.00, -1.00, FALSE
```

Macro editing commands

Macro editing commands are:

- "Copy" on page 393
- "Cut" on page 393
- "Delete" on page 394
- "Drag" on page 394
- "Duplicate" on page 394
- "MirrorHorizontal" on page 394
- "MirrorVertical" on page 395
- "Move" on page 395
- "Paste" on page 395
- "ReplacePart" on page 396
- "Rotate" on page 396
- "SetColor" on page 396
- "SetFillStyle" on page 397
- "SetFont" on page 397

- "SetHatchStyle" on page 397
- "SetLineStyle" on page 397
- "SetLineWidth" on page 398

Use the macro editing commands to edit the selected objects. Except where noted, these commands do not change an object's CurrentLocation, and do not change the selection set.

In the following macro command descriptions, **Red** indicates a decimal number value. **Blue** indicates a value of either TRUE or FALSE. **Dark Cyan** indicates an integer value. **Magenta** indicates any character string.

Note: Macro commands are reserved words, and should not be used for macro function or procedure names.

Copy

Function: Copy

Use this command to copy all selected objects to the Clipboard.

Example:

```
Copy
```

Cut

Function: Cut

Use this command to remove all selected objects from the schematic page, and place them on the Clipboard. After the operation, no objects are selected.

Example:

```
Cut
```

Delete

Delete

Function: Use this command to delete all of the selected objects, without placing them on the Clipboard. After the operation, no objects remain selected.

Example:

```
Delete
```

Drag

Drag *X*, *Y*, *dragflag*

Function: Use this command to drag all selected objects from CurrentLocation to CurrentLocation + (***X***, ***Y***). CurrentLocation is changed to CurrentLocation + (***X***, ***Y***). If ***dragflag*** is TRUE, then nets will stretch to maintain connectivity to selected parts, and remain orthogonal. If ***dragflag*** is FALSE, then select will stretch to maintain connectivity, but not remain orthogonal.

Example:

```
Drag 2.50, 3.10, TRUE
```

Duplicate

Duplicate *X*, *Y*

Function: Use this command to create a copy of the selected object at CurrentLocation + (*X*, *Y*). CurrentLocation is changed to CurrentLocation + (*X*, *Y*), and the new object is selected.

Example:

```
Duplicate -2.50, -4.60
```

MirrorHorizontal

MirrorHorizontal

Function: Use this command to mirror all selected objects horizontally.

Example: `MirrorHorizontal`

MirrorVertical

Function: MirrorVertical

Use this command to mirror all selected objects vertically.

Example: `MirrorVertical`

Move

Function: Move *X*, *Y*, *moveflag*

Use this command to move all selected objects from CurrentLocation to CurrentLocation + (***X***, ***Y***). CurrentLocation is changed to CurrentLocation + (***X***, ***Y***). If ***moveflag*** is TRUE, then nets will stretch to maintain connectivity to selected parts, and remain orthogonal. If ***moveflag*** is FALSE, then select will stretch to maintain connectivity, but not remain orthogonal.

Example: `Move 2.50, 3.10, TRUE`

Paste

Function: Paste *X*, *Y*

Use this command to paste the contents of the Clipboard to CurrentLocation + (***X***, ***Y***). CurrentLocation is changed to CurrentLocation + (***X***, ***Y***). All of the objects pasted from the Clipboard are selected.

Example: `Paste 4.00, 5.50`

ReplacePart

ReplacePart "*libname*", "*pkgname*", "*view*", "*devicedesignator*"

Function:

Use this command to change the selected parts from their normal view to their convert view, or from their convert view to their normal view. The part is specified by ***pkgname***, and the reference is specified by ***devicedesignator***. The library containing the part is specified by ***libname***. The view of the part is specified by ***view***.

Check that the library path and name specified is correct. You can use this macro to change the library, part, or both, similar to the Replace Cache command. If you do this, be certain that the new part's pin arrangement matches that of the one being replaced.

Example:

```
ReplacePart "C:\PROGRAM
FILES\ORCAD\CAPTURE\LIBRARY\TTL.OLB", "74LS08",
"74LS08.Normal", "D"
```

Rotate

Rotate

Function:

Use this command to rotate all selected objects. CurrentLocation is set to the new upper left corner of the selection set.

Example:

```
Rotate
```

SetColor

SetColor *colorID*

Function:

Use this command to set the color property to ***colorID*** for all selected objects. Objects that do not have a color property are unaffected.

Capture ColorID to RGB mapping.

Example:

```
SetColor 1
```

SetFillStyle

SetFillStyle *StyleID*

Function: Use this command to set the fill style property to ***styleID*** for all selected objects. Objects that do not have a fill style are unaffected.

Example:
```
SetFillStyle 3
```

SetFont

SetFont "*fontID*", *colorID*, *boldID*, *italicID*

Function: Use this command to set the font and font style for the selected objects. The font is specified by ***fontID***. The text's color is specified by ***colorID***. If ***boldID*** is TRUE, then the text appears as bold, otherwise it appears non-bold. If ***italicID*** is TRUE, then the text appears italicized, otherwise it appears non-italicized.

Capture ColorID to RGB mapping.

Example:
```
SetFont "Arial", 13, FALSE
```

SetHatchStyle

SetHatchStyle *StyleID*

Function: Use this command to set the hatch style property to ***styleID*** for all selected objects. Objects that do not have a fill style are unaffected.

Example:
```
SetHatchStyle 3
```

SetLineStyle

SetLineStyle *StyleID*

Function: Use this command to set the line style property to ***styleID*** for all selected objects. Objects that do not have a line style are unaffected.

Example: `SetLineStyle 2`

SetLineWidth

SetLineWidth *widthID*

Function: Use this command to set the line width property to ***widthID*** for all selected objects. Objects that do not have a line width are unaffected.

Example: `SetLineWidth 2`

Macro placement commands

The macro placement commands are:

- "PlaceArc" on page 400
- "PlaceBlock" on page 400
- "PlaceBookmark" on page 401
- "PlaceBus" on page 401
- "PlaceBusEntry" on page 401
- "PlaceEllipse" on page 402
- "PlaceGround" on page 402
- "PlaceJunction" on page 402
- "PlaceLine" on page 403
- "PlaceNetAlias" on page 403
- "PlaceNextPolygonPoint" on page 403
- "PlaceNextPolylinePoint" on page 404
- "PlaceNoConnect" on page 404
- "PlaceOffPage" on page 404
- "PlacePart" on page 405

- "PlacePicture" on page 405
- "PlacePin" on page 406
- "PlacePolygon" on page 406
- "PlacePolyline" on page 407
- "PlacePort" on page 407
- "PlacePower" on page 408
- "PlaceRectangle" on page 408
- "PlaceText" on page 408
- "PlaceTitleblock" on page 409
- "PlaceWire" on page 409

Use the macro placement commands to place objects in the schematic page editor. Some of the placement commands can be declared as WithDialog. For example, PlaceBlock can be used as PlaceBlockWithDialog. Macro commands using WithDialog prompt you to provide information, like the name of a hierarchical block, when executed.

In the following macro command descriptions, **Red** indicates a decimal number value. **Blue** indicates a Boolean value where zero means FALSE and non-zero numbers mean TRUE. **Magenta** indicates any character string. Command description variables enclosed in brackets ("**[**" and "**]**") are not used when the command is declared as WithDialog.

Note: Macro commands are reserved words, and should not be used for macro function or procedure names.

PlaceArc

PlaceArc *X1*, *Y1*, *X2*, *Y2*, *X3*, *Y3*, *X4*, *Y4*

Function:

Use this command to place an arc specified by the rectangle with the coordinates CurrentLocation + (***X1***, ***Y1***) and the CurrentLocation + (***X2***, ***Y2***). The starting point of the arc is specified by the coordinate (***X3***, ***Y3***), and is terminated at the coordinate specified by (***X4***, ***Y4***). The current location is changed to the upper left corner of the arc's defining rectangle or the coordinate (***X4***, ***Y4***).The arc becomes the only object selected.

Example:

```
PlaceArc -0.01, -1.12, 2.03, 0.92, 1.91, -0.60, 0.00, 0.00
```

PlaceBlock

PlaceBlock *X1*, *Y1*, *X2*, *Y2*, ["*libname*", "*schematicname*", "*blockname*", "*primitiveflag*"]

Function:

Use this command to place a hierarchical block defined by CurrentLocation + (***X1***, ***Y1***) and CurrentLocation + (***X2***, ***Y2***). The hierarchical block's name and reference are specified by ***blockname***. The current location is changed to the upper left corner of the hierarchical block, and the hierarchical block becomes the only selected object. If ***blockname*** is not specified, Capture will assign it a unique internal name. If ***blockname*** is specified, but not unique, the command will fail and no objects will be selected. If the hierarchical block has an attached schematic folder, it is specified by ***schematicname***. The path and library name containing the schematic folder are specified by ***libname***. The hierarchical block's primitivity is specified by ***primitiveflag***, which is set to YES, NO, or DEFAULT.

Example:

```
PlaceBlock -0.10, -0.60, 0.40, -0.30, "C:\PROGRAM
FILES\ORCAD\CAPTURE\Design\Fulladd\Fulladd.OLB", "HALFADD",
"Halfadd_A", "DEFAULT"
PlaceBlockWithDialog 0.30, -0.30, 0.80, 0.00
```

PlaceBookmark

PlaceBookmark *X*, *Y*, ["*name*"]

Function: Use this command to place a bookmark at the current location added to the offset (***X***, ***Y***). The bookmark name is specified by ***name***. The current location is changed to its current value added to the offset (***X***, ***Y***), and the bookmark becomes the only selected object.

Example:

```
PlaceBookMark 0.20, 0.00, "C:\PROGRAM
FILES\ORCAD\CAPTURE\DESIGN1.DSN", "B"
PlaceBookMarkWithDialog -1.80, 0.50
```

PlaceBus

PlaceBus *X1*, *Y1*, *X2*, *Y2*

Function: Use this command to place the first segment of a bus with the starting point at CurrentLocation + (***X1***, ***Y1***), and the endpoint at CurrentLocation + (***X2***, ***Y2***). CurrentLocation is set to CurrentLocation + (***X2***, ***Y2***). The bus becomes the only selected object.

Example:

```
PlaceBus -1.40, 1.00, 0.10, 1.00
```

PlaceBusEntry

PlaceBusEntry *X*, *Y*, *rotate*

Function: Use this command to place a bus entry at CurrentLocation + (***X***, ***Y***). If ***rotate*** is FALSE, the bus entry appears as a forward slash (/). If ***rotate*** is TRUE, then the bus entry appears as a backward slash (\). CurrentLocation is set to CurrentLocation + (***X***, ***Y***). The bus entry becomes the only selected object.

Example:

```
PlaceBusEntry -3.00, -1.00, FALSE
```

PlaceEllipse

PlaceEllipse *X1*, *Y1*, *X2*, *Y2*

Function: Use this command to place an ellipse specified by the points CurrentLocation + (***X1***, ***Y1***), and CurrentLocation + (***X2***, ***Y2***). CurrentLocation is changed to CurrentLocation + (***X2***, ***Y2***), and the ellipse becomes the only selected object.

Example:

```
PlaceEllipse 0.00, 0.00, 1.20, 1.30
```

PlaceGround

PlaceGround *X*, *Y*, ["*libname*", "*symbolname*", "*name*"]

Function: Use this command to place an instance of a ground symbol at CurrentLocation + (***X***, ***Y***). The ground symbol is specified by ***symbolname***, and is given the name ***name***. The library containing the ground symbol is specified by ***libname***. CurrentLocation is set to CurrentLocation + (***X***, ***Y***), and the ground symbol becomes the only selected object. If there is no symbol called ***symbolname*** in a library named ***libname***, then the command fails and no objects are selected.

Example:

```
PlaceGround 0.30, 0.40, "C:\PROGRAM
FILES\ORCAD\CAPTURE\LIBRARY\CAPSYM.OLB", "GND FIELD SIGNAL",
"GND"
PlaceGroundWithDialog -1.90, -0.30
```

PlaceJunction

PlaceJunction *X*, *Y*

Function: Use this command to place a junction specified by the points CurrentLocation + (***X***, ***Y***). If a junction already exists at this location, then it is removed.

Example:

```
PlaceJunction -0.10, -1.30
```

PlaceLine

PlaceLine *X1*, *Y1*, *X2*, *Y2*

Function: Use this command to place a line specified by the points CurrentLocation + (***X1***, ***Y1***), and CurrentLocation + (***X2***, ***Y2***). CurrentLocation is changed to CurrentLocation + (***X2***, ***Y2***). The line becomes the only selected object.

Example:

```
PlaceLine -0.10, 0.40, 1.20, 0.40
```

PlaceNetAlias

PlaceNetAlias *X*, *Y*, ["*alias*"]

Function: Use this command to place a net alias at CurrentLocation + (***X***, ***Y***). The name of the net alias is specified by ***alias***. CurrentLocation is set to CurrentLocation + (***X***, ***Y***). The net alias becomes the only object selected. If CurrentLocation + (***X***, ***Y***) is not a wire or bus, the command fails. If CurrentLocation + (***X***, ***Y***) is on a bus, but ***alias*** is not a valid bus name, the command fails. No objects are selected if the command fails.

Example:

```
PlaceNetAlias -3.00, -1.30, "A[1..5]"
PlaceNetAliasWithDialog 2.00, 1.00
```

PlaceNextPolygonPoint

PlaceNextPolygonPoint *X*, *Y*

Function: Use this command to add a point to the currently selected polygon. The point is specified by CurrentLocation + (***X***, ***Y***). CurrentLocation is then changed to CurrentLocation + (***X***, ***Y***), and the polygon becomes the only selected object. If a polygon is not selected, the command fails and no objects are selected.

Example:

```
PlaceNextPolygonPoint 1.30, 3.20
```

PlaceNextPolylinePoint

PlaceNextPolylinePoint *X*, *Y*

Function: Use this command to add a point to the currently selected polyline. The point is specified by CurrentLocation + (***X***, ***Y***). CurrentLocation is then changed to CurrentLocation + (***X***, ***Y***), and the polyline becomes the only selected object. If a polyline is not selected, the command fails and no objects are selected.

Example:

```
PlaceNextPolylinePoint 1.30, 3.20
```

PlaceNoConnect

PlaceNoConnect *X*, *Y*

Function: Use this command to place a no connect symbol at CurrentLocation + (***X***, ***Y***). CurrentLocation is then changed to CurrentLocation + (***X***, ***Y***). Nothing remains selected. If CurrentLocation + (***X***, ***Y***) is not located at the end of a pin, the command fails.

Example:

```
PlaceNoConnect 3.40, 5.20
```

PlaceOffPage

PlaceOffPage *X*, *Y*, ["*libname*", "*symbolname*", "*name*"]

Function: Use this command to place an instance of an off-page connector at CurrentLocation + (***X***, ***Y***). The off-page connector is specified by ***symbolname***, and is given the name ***name***. The library containing the off-page connector is specified by ***libname***. The current location is set to CurrentLocation + (***X***, ***Y***), and the off-page connector becomes the only selected object. If there is no off-page connector called ***symbolname*** in a library named ***libname***, then the command fails and no objects are selected.

Example:

```
PlaceOffPage 2.00, 1.20, "C:\PROGRAM
FILES\ORCAD\CAPTURE\LIBRARY", "OFFPAGELEFT-L", "Carry"
PlaceOffPageWithDialog -0.50, 0.00
```

PlacePart

PlacePart *X*, *Y*, ["*libname*", "*pkgname*", "*devicedesignator*", *convert*]

Function:

Use this command to place a part instance at CurrentLocation (***X***, ***Y***). The part is specified by ***pkgname***, and the reference is specified by ***devicedesignator***. The library containing the part is specified by ***libname***. If ***convert*** is TRUE, then Capture uses the part's convert view rather than the normal view. After the part is placed, it becomes the only selected item. CurrentLocation is changed to CurrentLocation + (***X***, ***Y***). This command can fail for the following reasons:

- There is no library with the name ***libname***.
- There is no package in the specified library with the name ***pkgname***.
- There is no device with the specified ***devicedesignator*** in the package.
- The ***convert*** parameter has been set to TRUE, but there is no convert for the specified device.

If the command fails, CurrentLocation changes to CurrentLocation + (***X***, ***Y***).

Example:

```
PlacePart 1.60, 0.00, "C:\PROGRAM
FILES\ORCAD\CAPTURE\DESIGN\FULLADD\FULLADD.OLB", "74LS08",
"A", FALSE
PlacePartWithDialog -1.90, -0.90
```

PlacePicture

PlacePicture *X*, *Y*, "*filename*"

Function:

Use this command to place a picture or graphic. The picture's filename and path are specified by ***filename***, and the picture's location is specified by the current location added to the offset (***X***, ***Y***). The current location is changed to the picture's location, and the picture becomes the only selected object. If the specified picture file cannot be opened, the command fails and no objects are selected.

Example:

```
PlacePicture 1.50, 0.10, "C:\Pictures\Logo.bmp"
```

PlacePin

PlacePin *X*, *Y*, ["*name*", "*pintype*", "*isbus*"]

Function:

Use this command to place a hierarchical pin on the selected hierarchical block at CurrentLocation + (***X***, ***Y***). The hierarchical pin name is specified by ***name***, and the pin type is specified by ***pintype***. If ***isbus*** is FALSE, a scalar pin is created, otherwise a bus pin is created. CurrentLocation is changed to CurrentLocation + (***X***, ***Y***), and the hierarchical pin is the only selected object. The following situations will cause the command to fail:

- CurrentLocation + (***X***, ***Y***) does not lie on the boundary of a hierarchical block.
- If is ***isbus*** TRUE and name is not a valid bus name.
- If is ***isbus*** FALSE and name is a valid bus name.

If the command fails, the current location is unaffected, and no objects are selected.

Example:

```
PlacePin 3.20, 1.20, "A[0..2]", "output", TRUE
PlacePinWithDialog 3.10, 2.20
```

PlacePolygon

PlacePolygon *X1*, *Y1*, *X2*, *Y2*

Function:

Use this command to place the first segment of a polygon. The starting point is defined by CurrentLocation + (***X1***, ***Y1***). The endpoint is defined by CurrentLocation + (***X2***, ***Y2***). CurrentLocation is changed to CurrentLocation + (***X2***, ***Y2***), and the polygon becomes the only selected object.

Example:

```
PlacePolygon 1.30, 1.30, 3.20, 2.40
```

PlacePolyline

PlacePolyline *X1*, *Y1*, *X2*, *Y2*

Function: Use this command to place the first segment of a polyline. The starting point is defined by CurrentLocation + (***X1***, ***Y1***). The endpoint is defined by CurrentLocation + (***X2***, ***Y2***). CurrentLocation is changed to CurrentLocation + (***X2***, ***Y2***), and the polygon becomes the only selected object.

Example:

```
PlacePolyline 1.30, 1.30, 3.20, 2.40
```

PlacePort

PlacePort *X*, *Y*, ["*libname*", "*symbolname*", "*name*"]

Function: Use this command to place an instance of a hierarchical port at CurrentLocation + (***X***, ***Y***). The hierarchical port is specified by ***symbolname***, and is given the name ***name***. The library containing the hierarchical port is specified by ***libname***. CurrentLocation is set to CurrentLocation + (***X***, ***Y***), and the hierarchical port becomes the only selected object. If there is no hierarchical port called ***symbolname*** in a library named ***libname***, then the command fails and no objects are selected.

Example:

```
PlacePort 0.00, 0.20, "C:\PROGRAM
FILES\ORCAD\CAPTURE\LIBRARY\CAPSYM.OLB", "PORTBOTH-L",
"High"
PlacePortWithDialog -1.50, -1.40
```

PlacePower

PlacePower *X*, *Y*, ["*libname*", "*symbolname*", "*name*"]

Function: Use this command to place an instance of a power symbol at CurrentLocation + (***X***, ***Y***). The power symbol is specified by ***symbolname***, and is given the name ***name***. The library containing the power symbol is specified by ***libname***. CurrentLocation is set to CurrentLocation + (***X***, ***Y***), and the power symbol becomes the only selected object. If there is no symbol called ***symbolname*** in a library named ***libname***, then the command fails and no objects are selected.

Example:

```
PlacePower 0.00, 1.20, "C:\PROGRAM
FILES\ORCAD\CAPTURE\LIBRARY\CAPSYM.OLB", "VCC_ARROW",
"VCC_ARROW"
PlacePowerWithDialog 0.60, 0.00
```

PlaceRectangle

PlaceRectangle *X1*, *Y1*, *X2*, *Y2*

Function: Use this command to place a rectangle specified by the points CurrentLocation + (***X1***, ***Y1***), and CurrentLocation + (***X2***, ***Y2***). The current location is changed to CurrentLocation + (***X2***, ***Y2***), and the rectangle becomes the only selected object.

Example: PlaceRectangle 1.30, 4.20, 5.40, 2.20

PlaceText

PlaceText *X1*, *Y1*, *X2*, *Y2*, ["*text*"]

Function: Use this command to place comment text in the rectangle defined by CurrentLocation + (***X1***, ***Y1***), and CurrentLocation + (***X2***, ***Y2***). The string of text is specified by ***text***. CurrentLocation is changed to CurrentLocation + (***X2***, ***Y2***), and the text becomes the only selected object.

Example:

```
PlaceText -2.10, 0.30, -1.35, 0.42, "|+ 200k 300K 200uf"
PlaceTextWithDialog -0.05, 0.68, 0.15, 0.80
```

PlaceTitleblock

PlaceTitleblock *X*, *Y*, ["*libname*", "*titleblockname*", "*name*"]

Function: Use this command to place a title block symbol at CurrentLocation + (***X***, ***Y***). The title block is specified by ***titleblockname***, in a library specified by ***libname***. The title block's name is specified by ***name***. CurrentLocation is changed to CurrentLocation + (***X***, ***Y***), and the title block becomes the only selected object. If the specified title block doesn't exist in the specified library, the command fails. If the command fails, no objects are selected.

Example:

```
PlaceTitleblock 3.40, 5.20, "C:\PROGRAM
FILES\ORCAD\CAPTURE\LIBRARY\CAPSYM.OLB", "TitleBlock0",
"TitleBlock0"
PlaceTitleBlockWithDialog -1.80, 0.50
```

PlaceWire

PlaceWire *X1*, *Y1*, *X2*, *Y2*

Function: Use this command to place the first segment of a wire with starting point at CurrentLocation + (***X1***, ***Y1***), and an endpoint at CurrentLocation + (***X2***, ***Y2***). CurrentLocation is set to CurrentLocation + (***X2***, ***Y2***). The wire segment becomes the only selected object.

Example:

```
PlaceWire -1.00, -1.00, 2.00, 2.30
```

Macro viewing commands

The macro viewing commands are:

- "GoToAbsolute" on page 410
- "GoToBookmark" on page 410
- "GotoGridReference" on page 411
- "GotoRelative" on page 411
- "ViewGrid" on page 411

- "ViewGridReference" on page 411
- "ZoomAll" on page 412
- "ZoomArea" on page 412
- "ZoomIn" on page 412
- "ZoomOut" on page 412
- "ZoomSelection" on page 413

Use the macro viewing commands to display Capture tools, go to a specific area of the schematic page, and zoom in or out of an area. Except where noted, these macro commands have no effect on the current location or the selection set.

In the following macro command descriptions, **Red** indicates a decimal number value. **Blue** indicates a Boolean value where zero means FALSE and non-zero numbers mean TRUE. **Magenta** indicates any character string.

Note: Macro commands are reserved words, and should not be used for macro function or procedure names.

GoToAbsolute

GoToAbsolute *X*, *Y*

Function: Use this command to set CurrentLocation to the coordinate (***X***, ***Y***).

Example:

```
GoToAbsolute 0.00, 1.20
```

GoToBookmark

GoToBookmark "*name*"

Function: Use this command to set CurrentLocation to the upper left corner of the bookmark specified by the name ***name***.

Example:

```
GoToBookmark "Marker1"
```

GotoGridReference

GoToGridReference "*horizontal*", "*vertical*"

Function: Use this command to set CurrentLocation to the point specified by the horizontal grid reference ***horizontal***, and the vertical grid reference ***vertical***.

Example:
```
GoToGridReference "A", "B"
```

GotoRelative

GoToRelative *X*, *Y*

Function: Use this command to set CurrentLocation to CurrentLocation + (***X***, ***Y***).

Example:
```
GoToRelative 0.00, 1.20
```

ViewGrid

ViewGrid *on*

Function: Use this command to display the grid. If ***on*** is TRUE, then the grid becomes visible. Otherwise, the grid is hidden.

Example:
```
ViewGrid TRUE
```

ViewGridReference

ViewGridReference *on*

Function: Use this command to display the grid references. If ***on*** is TRUE, then the grid references become visible. Otherwise, the grid references are hidden.

Example:
```
ViewGridReference FALSE
```

ZoomAll

ZoomAll

Function: Use this command to see the entire schematic page.

Example:
```
ZoomAll
```

ZoomArea

ZoomArea *X1*, *Y1*, *X2*, *Y2*

Function: Use this command to zoom in on the area specified by the rectangle with the coordinates the current location added to the offset (***X1***, ***Y1***), and the current location added to the offset (***X2***, ***Y2***).

Example:
```
ZoomArea 2.40, 0.50, 5.10, 1.70
```

ZoomIn

ZoomIn

Function: Use this command to zoom in at CurrentLocation. The zoom is specified by the schematic page's zoom factor.

Example:
```
ZoomIn
```

ZoomOut

ZoomOut

Function: Use this command to zoom out from CurrentLocation. The zoom is specified by the schematic page's zoom factor.

Example:
```
ZoomOut
```

ZoomSelection

ZoomSelection

Function: Use this command to zoom in on the rectangle that contains all of the objects selected on the schematic page. If nothing is selected, then the command does nothing.

Example:

```
ZoomSelection
```

Macro property commands

The macro property commands are:

- "DisplayProperty" on page 414
- "RemoveDisplayProperty" on page 414
- "RemoveProperty" on page 414
- "SetProperty" on page 415
- "GetProperty" on page 415

Use the macro property commands to add, remove, and display properties. These commands do not affect the current location or the selection set.

In the following macro command descriptions, **Blue** indicates a value of either TRUE or FALSE. **Dark Cyan** indicates an integer value. **Magenta** indicates any character string.

Note: Macro commands are reserved words, and should not be used for macro function or procedure names.

DisplayProperty

DisplayProperty "*name*", "*fontID*", *sizeID*, *boldID*, *italicID*, *colorID*, *rotate*

Function: Use this command to display the value of a property currently not visible on the selected object. The name of the property is specified by ***name***. The font for the property is specified by ***fontID***. The font size for the property is specified by ***sizeID***. If ***boldID*** is TRUE, then the property value appears in bold. If ***italicID*** is TRUE, then the property value appears in italics. The property value's color is specified by ***colorID***. The number of 90-degree rotations is specified by ***rotate***.

Capture ColorID to RGB mapping.

Example:

```
DisplayProperty "Part Reference", "Arial", 9, FALSE, FALSE,
48, 0
```

RemoveDisplayProperty

RemoveDisplayProperty "*name*"

Function: Use this command to hide a display property of an object. The property to hide is specified by ***name***.

Example:

```
RemoveDisplayProperty "Part Reference"
```

RemoveProperty

RemoveProperty "*name*"

Function: Use this command to remove the property, specified by ***name***, from the selected object or objects.

Example:

```
RemoveProperty "Location"
```

SetProperty

SetProperty "*name*", "*value*"

Function:

Use this command to change a property value or add a new property with a specified value to the selected object. The property to be changed or created is specified by ***name***. The new property value is specified by ***value***. If more than one object is selected, then all objects are affected.

Example:

```
SetProperty "Value", "74LS04"
```

GetProperty

GetProperty "*name*", "*value*"

Function:

Use this command to fetch a property value for the selected object. The parameter ***name*** specifies the name of the property to be fetched. The parameter ***value*** is the variable that will store the property value.

Example:

```
GetProperty "Cost", Temp$
```

where,

- `Cost` is the property name.
- `Temp$` is the variable that stores the property value.

Note: Make sure that the variable you define is followed by a $ symbol.

Macro input boxes

Macro input boxes create a dialog box as you execute a macro. Use input boxes if you only want to prompt the user for one variable of a macro command.

In the following macro command description, **Magenta** indicates any character string. Command description variables enclosed in brackets ("[" and "]") are optional. If a variable can be a character

string, it must be immediately followed by the dollar sign ($). These possibilities are shown in **Blue**.

InputBox$(prompt$[, [title$][, [default$], [X, Y]]])

A prompt for the input box is specified by **prompt**. The input box's title is specified by **title**. The default value for the input box is specified by **default**. The horizontal location of the input box is specified by **X**, and the vertical location of the input box is specified by **Y**.

```
Z$ = "Line Coordinates"
X1 = 0
X2 = 0
Y1 = 0
Y2 = 0
PlaceLine InputBox("What is X1?", Z$, X1), InputBox("What is
Y1?", Z$, Y1), InputBox("What is X2?", Z$, X2), InputBox("What
is Y2?", Z$, Y2)
```

Synchronizing parts

Capture gives you the power to place parts in a design, alter the parts in the library, then update the design so that all of the altered parts reflect the changes you have made in the library. You use the Update Cache command on the Design menu to do this.

When you use the Update Cache command, properties of the part are retained; however, the pin properties of the part instance are lost.

To update a part in the design cache so it matches a part in the library

1. Using the part editor, edit the parts in the library to suit your needs.
2. Open the project manager window for the design.
3. Select the parts in the project manager.
4. From the Design menu, choose the Update Cache command. The design cache and all part instances are updated to match the library parts.

Note: If you edit a library provided by OrCAD, it is important that you assign a new library name so that your changes are not overwritten when you upgrade or update your software.

Note: When you copy pages from one design or library to another, parts displayed on the copied pages may appear different due to differences in each design or library cache. If a part is not already in the destination design cache, Capture will copy it from the source design's cache. Otherwise, it will use the part already present in the destination design's cache.

Note: When you use the Replace Cache or Update Cache command, all properties of the part are retained, but the pin reflects the properties of the library part. This means you lose any changes made to pin properties after the part was placed, including those made by the Back Annotate or the Annotate tools.

Note: The Replace Cache and Update Cache commands are quite similar, but they have the following differences:

- You can have only one part selected in the design cache when you use Replace Cache; you can have multiple parts selected in the cache when you select Update Cache.
- You can modify the part's link to the library (part name, path, and library) with Replace Cache; you cannot modify the part's link with Update Cache.

Note: If you move a library after you place a part, the connection between the part and its library is broken. In this case, the Update Cache command will not find the library; you'll need to use the Replace Cache command and specify the new path to the library.

Editing VHDL and Verilog files

This section covers:

- Creating a VHDL model from a hierarchical block on page 418
- Creating a Verilog model from a hierarchical block on page 419
- Checking the syntax of VHDL or Verilog files on page 420

Capture provides editing capabilities for developing VHDL and Verilog files. You can use this capability to create functional models for design behavior, or testbenches for simulation.

Creating a VHDL model from a hierarchical block

In Capture, you can create VHDL models from hierarchical components on your schematic page. That is, you can create a hierarchical block on a schematic page, then create a VHDL model that defines its functionality. Creating VHDL models from hierarchical blocks in this manner is generally termed "top-down" design.

To create a VHDL model from a hierarchical block

1. Open the parent schematic page in the schematic page editor.
2. From the Place menu, choose the Hierarchical Block command. Capture displays the Place Hierarchical Block dialog box.
3. Assign a reference designator to the hierarchical block using the Reference text box, and choose VHDL as the implementation type in the Implementation Type drop-down list box. Type the entity name for the VHDL model in the Implementation name text box. Specify a file name for the VHDL model that will define the behavior of the hierarchical block in the Path and filename text box. The file name must be a VHDL file (*.VHD). Then, click OK. Capture returns to the schematic page editor.
4. Use the cursor to draw an outline for the block. Press the left mouse button at one corner of the desired area, drag the cursor to the opposite corner, and release the left mouse button. Capture places the outline of the block on the schematic page.
5. With the new hierarchical block selected, choose the Place Hierarchical Pin button from the tool palette. Capture displays the Place Hierarchical Pin dialog box.
6. Assign a name to the pin, specify pin type and width, then click OK. Do not move the cursor outside of the schematic page editor window before completing the next step.
7. Move the cursor to the desired location in the hierarchical block and click the left mouse button to place the pin on the block, then choose End Mode from the right mouse button pop-up menu.
8. Repeat steps 5 through 7 to place additional hierarchical pins as needed.
9. With the hierarchical block selected, click the right mouse button and choose Descend Hierarchy from the pop-up menu. Capture

generates a VHDL model template for the block, using the hierarchical pins as port names.

10. Enter the functional description for the block in the model architecture.

11. Close the VHDL editor. When Capture prompts you to save the changes to the file, click OK to save the changes.

At this point, the hierarchical block is defined and ready to be "wired in" to the rest of the schematic.

Creating a Verilog model from a hierarchical block

In Capture, you can create Verilog models from hierarchical components on your schematic page. That is, you can create a hierarchical block on a schematic page, then create a Verilog model that defines its functionality. Creating models from hierarchical blocks in this manner is generally termed "top-down" design.

To create a Verilog model from a hierarchical block

1. Open the parent schematic page in the schematic page editor.

2. From the Place menu, choose the Hierarchical Block command. Capture displays the Place Hierarchical Block dialog box.

3. Assign a reference designator to the hierarchical block using the Reference text box, and choose Verilog as the implementation type in the Implementation Type drop-down list box. Type the module name for the Verilog module in the Implementation name text box. Specify a file name for the Verilog model that will define the behavior of the hierarchical block in the Path and filename text box. The file name must be a Verilog file (*.V). Then, click OK. Capture returns to the schematic page editor.

4. Use the cursor to draw an outline for the block. Press the left mouse button at one corner of the desired area, drag the cursor to the opposite corner, and release the left mouse button. Capture places the outline of the block on the schematic page.

5. With the new hierarchical block selected, choose the Place Hierarchical Pin button from the tool palette. Capture displays the Place Hierarchical Pin dialog box.

6. Assign a name to the pin, specify pin type and width, then click OK. Do not move the cursor outside of the schematic page editor window before completing the next step.
7. Move the cursor to the desired location in the hierarchical block and click the left mouse button to place the pin on the block, then choose End Mode from the right mouse button pop-up menu.
8. Repeat steps 5 through 7 to place additional hierarchical pins as needed.
9. With the hierarchical block selected, click the right mouse button and choose Descend Hierarchy from the pop-up menu. Capture generates a Verilog model template for the block, using the hierarchical pins as port names.
10. Enter the functional description for the block in the model architecture.
11. Close the editor. When Capture prompts you to save the changes to the file, click OK to save the changes.

At this point, the hierarchical block is defined and ready to be "wired in" to the rest of the schematic.

Checking the syntax of VHDL or Verilog files

You can check the syntax of VHDL or Verilog files using the appropriate Check Syntax command. The tool checks the syntax in all VHDL or Verilog files selected in the project manager window.

Note: You must have a project open to use the Check Syntax command. Error reporting for the tool requires some project resources that are not available unless a project is open.

To check the syntax of VHDL files

1. In the project manager window, use the left mouse button to select the VHDL file for which you want to check the syntax. You can select multiple files using the CTRL key.
2. From the Edit menu, choose the Check VHDL syntax command. The Check Syntax tool finds the first error in the file, and highlights it, so that you can fix it.

3. To continue checking the file, choose the Check VHDL syntax command from the Edit menu again.

Shortcuts

Pop-up menu: Check Syntax

To check the syntax of Verilog files

1. In the project manager window, use the left mouse button to select the Verilog file for which you want to check the syntax. You can select multiple files using the CTRL key.
2. From the Edit menu, choose the Check Verilog syntax command. The Check Syntax tool finds the all errors in the file, and highlights them, so that you can fix them. Further, Capture opens a text file, VAN.TXT, that contains details on all errors in the netlist.

Shortcuts

Pop-up menu: Check Syntax

Setting and using schematic states

At times during the design process, you may want to experiment with different “what if?” scenarios to determine the best implementation for your purposes. Capture provides a method to do this with “label states.”

Label states allow you to define different states for a schematic page, perform edits, and then return to the defined state of the schematic before the editing occurred.

Each schematic page can have its own set of label states. Further, each schematic page has two label states “Start” and “End” that are implicit.

Label states are identified with a unique label consisting of 1 to 5 alphanumeric characters.

Note: Since “Start” and “End” are default label states for each schematic page, any label states that you define cannot use the identifiers “Start” or “End” as labels.

Also, note that labels are not case-sensitive. Thus “stateA” and “STATEA” are considered identical by Capture.

To set a label state

1. From the edit menu, choose Label State, then choose Set. The Set Label State dialog box appears.
2. Enter a name for the label.

Note: Labels must be 1 to 5 characters long, and must be unique per schematic page. the labels “start” and “end” are reserved and cannot be assigned.

3. Click OK. At this point, the state of the schematic is labeled.

To go to a schematic state

1. From the edit menu, choose Label State, then choose Goto. The Goto Label State dialog box appears.
2. Enter the label for the state to which you want to return.
3. Click OK. Capture returns you to the labeled state of the schematic, removing any edits that occurred in the interim.

To delete a label state

1. From the edit menu, choose Label State, then choose Delete. The Delete Label State dialog box appears.
2. Enter the label for the state that you want to delete.
3. Click OK. The label state is removed and you can no longer return to it with the Goto Label State dialog box.

Note: You cannot delete the default “start” and “end” label states.

8

Assigning properties

Capture uses properties to describe objects. Imagine a brown, ceramic capacitor that measures 6 millimeters in height. Type, color, and height are properties, while ceramic, brown, and 6 millimeters are property values. Every Capture object is made up of such name-and-value pairs.

Note: Beginning with Capture Release 9.1, property names are not case sensitive. If you have a legacy design that contains two properties with the same name, Capture will append _# to one of two properties, where # is the counting number that makes the name unique on the object.

Inherent and user-defined properties

Some properties, called inherent properties, are an essential part of an object; others, called user-defined properties, are not used by Capture, but may be used by another tool. For example, if you want to include the supplier and the price per hundred for the objects on your schematic pages, you create two user-defined properties for the objects. You can add as many user-defined properties to objects as you like, and you can remove user-defined properties when you find that you don't need them. Graphic objects such as lines, ellipses, and rectangles do not support user-defined properties.

Creating and adding properties

When you create a user-defined property with the Edit Part Properties dialog box, you can make the property name visible and specify the font and location of the property value text, even before you specify the property value. The property name acts as a placeholder until you supply the property value.

When you add a user property to an existing object using the property editor, you can assign the property value at the time you create the new property or later. The additional benefit to using the property editor is the flexibility with which you can edit all properties on an object or group of objects on a schematic page.

Once you've added properties to a part on a schematic page, its properties no longer match the properties of the same part residing in the library. This part on the schematic page is unique, in that it has properties assigned specifically to it that are not inherited from the library part definition.

The property editor window shows you all available properties in the new single view. You can use the tabs to edit properties of all selected objects from the property editor. The property editor also displays all library definitions, instance properties, and occurrence properties for an object.

Properties in the design cache

When a part is first placed on a schematic page, a copy of the part and its library properties is put into the design cache from the library. A few of the library properties, such as PCB Footprint and Value, are also copied as instance properties onto the placed part. The rest of the library properties “shine through” from the cache to the instance and occurrence of the part property.

“Shine through” is indicated by hash marks in the cell. In the property editor, you can assign an instance or occurrence value, creating an instance or occurrence property. This instance or occurrence property then will override the shine-through definition.

Instance property

An instance property is a user property applied to the placed instance of a part or symbol in the design. This includes PCB Footprint, Value, and Name properties of each placed part or symbol in a design. This is the same as the user properties displayed and editable from the Capture v7.2 Logical view.

An instance property will "shine through" to all occurrences of that instance unless it is overridden by occurrence properties that you

have edited. A change using any of the tools, like Annotate, also may update the instance property.

Occurrence property

An occurrence property is a user property applied to a particular occurrence of a placed instance of a part or symbol in a design. This is the same as the user properties displayed and editable from the Capture v7.2 Physical view.

The spreadsheet will expand to display occurrence properties if values are different from the instance shine through value; otherwise, the rows are hidden from view. To quickly hide or display all the occurrence properties, press and hold the CTRL key while clicking on one of the plus (+) symbols in the property editor.

Note: If you are working on multiple occurrences of a block, Capture provides a Save message only while closing the last occurrence. It is recommended you work on only one occurrence at a time.

Combined property strings

With many of the tools in Capture, such as Create Netlist and Annotate, you use combined property strings to convey information to the tool or to limit the tool's action.

A combined property string consists of one or more property names, enclosed in braces, and can also contain literal text. Capture combines the values of the named properties with any literal text to create a string. An example is:

```
{Value}{Reference}
```

where "Value" and "Reference" are property names. Using this combined property string and a part with a part value of 74LS32 and a part reference of U?A, Capture creates the string:

```
74LS32U?A
```

You can include spaces and other characters in the combined property string, as in this example:

```
Part: {Value} ({Reference})
```

Using this combined property string and the same part, Capture creates the string:

```
Part: 74LS32 (U?A)
```

Different tools use combined property strings in different ways. For example, Annotate uses one to compare parts—if one part's combined property string matches another part's combined property string, it packages the parts together.

Note: Bill of Materials and other commands on the Tools menu that generate an output file based on a combined property string may produce errors if you include extra curly braces.

Note: You can include tabs in combined property strings, so that the output file can be manipulated in a spreadsheet or database application. Tabs also help format report files, such as those created by the Bill of Materials command.

Note: Wherever you want to have a tab in the output file, insert the characters \t (a backslash and a lowercase "t") in the combined property string.

Certain properties can be edited, but not removed. These are called inherent properties, and are listed in the table below.

Object type	Properties
Arcs	Line style and width, color
Bookmarks	Name
Images (pictures)	(None)
Bus entries	ID, net name
Buses	(None)
DRC markers	(None)
Ellipses	Fill style, line style and width, color
Ground symbols	Name
Hierarchical pins	Name, pin type, pin width
Hierarchical ports	Name, pin type
Hierarchical blocks	Color, implementation path, implementation type, implementation, name, primitive, part reference, value

IEEE symbols	(None)
Junctions	(None)
Lines	Line style and width, color
Net aliases	Alias name, color, rotation, font
No connect objects	(None)
Off-page connectors	Name
Pictures (images)	(None)
Pins in part editor	Name, number, width, shape, type
Pins in schematic page editor	Is no connect, name, net name, number, order, swap ID, type
Polygons	Fill style, line style and width, color
Polylines	Line style and width, color
Power symbols	Name
Rectangles	Fill style, line style and width, color
Title blocks	Design create time, design file name, design modify time, design name, page create date, page modify date, page size, schematic create date, schematic modify time, schematic name, schematic page count, schematic page number, source library, source symbol
Text	Text content, color, rotation, font
Visible properties	Value (of most properties), visibility, color, font, rotation
Wires	ID, net name

Using the property editor

This section covers:

- "Defining properties" on page 370
- "Editing properties" on page 372

- "Importing part and pin properties" on page 376
- "Exporting part and pin properties" on page 377
- "Removing part reference assignments" on page 384

You can display the property editor by one of the following methods:

- Select one object, such as a design, or a combination of objects, such as a combination of schematic(s) and/or pages, right-click on the selection and select Edit Object Properties.
- Selecting items on a schematic page, then choosing Properties on the Edit or pop-up menu.
- Double-clicking on an item in the schematic page editor.

Using the property editor, you can edit properties for instances or occurrences of the following objects:

- Parts (including hierarchical blocks)
- Nets (including constituent nets within buses)
- Pins
- Title blocks
- globals
- Ports
- Aliases

To browse and edit properties for an entire design, see the Browse spreadsheet editor.

Each column in the property editor is a property. Each row is an instance or occurrence. Occurrence rows appear in yellow below their associated instance row. They only appear if you expand the instance by clicking the plus sign (+) to the left of the instance name, or if an occurrence property of an object is different from the instance. The cells in the property editor show the property values for each instance or occurrence. If a white cell contains hash marks, the corresponding property does not have an instance value causing the library definition of the property to "shine through" to the instance. If a yellow cell contains hash marks, the corresponding property does

not have an occurrence value, causing the instance value to "shine through" to the occurrence.

The properties that appear in the property editor depend on the items selected in the schematic page. Also, these properties depend on the tab selection at the bottom of the property editor. For example, if the Parts tab is active, the properties for selected parts appear in the property editor.

Note: When you first start the property editor, all instance properties appear. Occurrence properties appear only if they have their own values assigned to them (independent of the instance property values).

You can also constrain the set of displayed properties by using the filters available in the drop-down list in the upper right of the property editor. A number of filters are available. These filters are sets of properties that are typically useful for particular project types. For example, the Actel Designer Part/Net Properties filter includes properties that are useful for constraining a PLD project for integration with Actel Designer software. The <Current properties> filter causes the property editor to display all properties that currently exist for the selected item.

When editing properties in the property editor, remember these key points:

- Property values that are applied to instances will "shine through" to all occurrences of those instances, unless an occurrence has a value (independent of the instance value) for a particular property.
- Occurrence property values override instance property values.
- When you delete an instance property, that property will no longer "shine through" to its occurrences.
- Deleting a property value from an occurrence causes the instance property value to "shine through" to that occurrence.
- Library definitions will "shine through" to the instance and occurrence of the object only if the instance or occurrence value is unedited.

The Property editor window

The property editor window appears when you select some combination of parts, nets, pins, title blocks, aliases and globals in the schematic page editor, and then choose Properties from the Edit menu or choose Edit Properties from the pop-up menu. You can use the property editor window to edit part, net, pin, title block, global, port, and alias properties. The property editor displays all library definitions, instance properties, and occurrence properties for an object.

New Column or New Row

Displays the Add New Column or Add New Row dialog box, depending on the property editor orientation, to add a new property column or row. The property is added to a single object if a single cell is selected or to several objects if several cells are selected. To add a property to more than one object, either shift-select the cells or select an entire row/column by clicking on the property name. To add the property to an object, you must enter a property value for a given object.

Note: If no cell is selected on the sheet, then the value field is not activated in the Add New Column or Add New Row dialog box and the user is unable to add a new property unless the user manually enters values for the new fields in the property spreadsheet.

Apply

Applies the changes in the property editor to the schematic page. The Apply button does not dismiss the property editor. You can also apply the changes to the schematic page by closing the property editor.

Display

Displays the Display Properties dialog box to set the display option of the selected property and its value. You cannot display properties of an occurrence property using the Display Properties dialog box.

Delete Property

Deletes the editable property from the selected object or objects. (Properties that are not editable appear in italics.) If you select all of a property's cells and click the Delete Property button, the property will be removed from the selected objects but will remain in the filter. This is indicated by the hash marks that appear in the cell.

Filter by

Specifies a filter by which to view the objects. Use the property editor filter to constrain the available properties. For example, the Capture filter displays common schematic capture properties available to most parts, while the Capture-Allegro filter displays the properties needed to send a design to Allegro PCB Editor.The Layout filter displays properties needed to send a design to OrCAD Layout. For information about the Allegro PCB Editor properties, see document *Allegro Platform Properties Reference* guide (*propref.pdf*).

You can view all the properties available on the objects in the property editor by selecting the <Current properties> filter from the drop-down list.

Another example of constraining properties is using the *Allegro_Signal_Flow_Routing.* This filter setting lets you view signal flow properties, such as PROPAGATION_DELAY, RELATIVE_PROPAGATION_DELAY, RATSNEST_SCHEDULE, and DIFFERENTIAL_PAIR in the Flat Nets tab.

Column Value Editor

Displays and allows change of value in selected column. As a result, you do not need to resize the column widths to be able to view values that are larger than what can be accommodated in a column.

Parts

Displays the parts of the selected objects. The Parts tab includes hierarchical blocks.

You can use the Parts tab on the property editor to add and delete property instances and occurrences and to change their values.

Note: All property editor tabs provide one row of property information per instance or occurrence.

The Graphic property column provides the option to toggle the display of the part between Normal and Convert view. When you click the Graphic cell, a down arrow appears indicating a drop-down list. You can change the graphic's appearance on the schematic by clicking the down arrow and selecting a different view.

Schematic Nets

Displays the schematic nets of the selected objects. This tab includes constituent nets within buses.

Pins

Displays the pins of the selected objects. This tab includes hierarchical pins in hierarchical blocks.

Title Blocks

Displays the title blocks of the selected objects.

With the Title Blocks tab selected, you can add a property to the Title Block instance on a schematic page that will display the full hierarchical path to the schematic.

Globals

Displays selected globals for simultaneous editing of multiple names.

Ports

Displays source symbol, source library, and type of port. Provides for simultaneous editing of multiple ports.

Aliases

Displays color, font, name, and rotation of net aliases. Use the Aliases tab to edit multiple aliases at one time.

Rows and columns

In the property editor, each row displays an instance or an occurrence of an object. Instance rows appear with a white background. Occurrences appear in yellow below their associated instance row. Occurrence rows automatically appear when one or more of the occurrence property values are different from the instance property values.

Each column is a placeholder that you can use to add properties. The cells in the property editor show the property values for each instance or occurrence. A cell with hash marks in indicates that the property does not exist on the object that the cell represents. You can add a value by clicking inside the cell, typing the value, and pressing ENTER or clicking the Apply button. A property value in italics is a read only property cannot be edited.

Tip

Roll the mouse wheel up and down to scroll through vertically in the Property Editor.

Tip

Hold down the CTRL key and roll the mouse wheel to zoom in and zoom out.

Tip

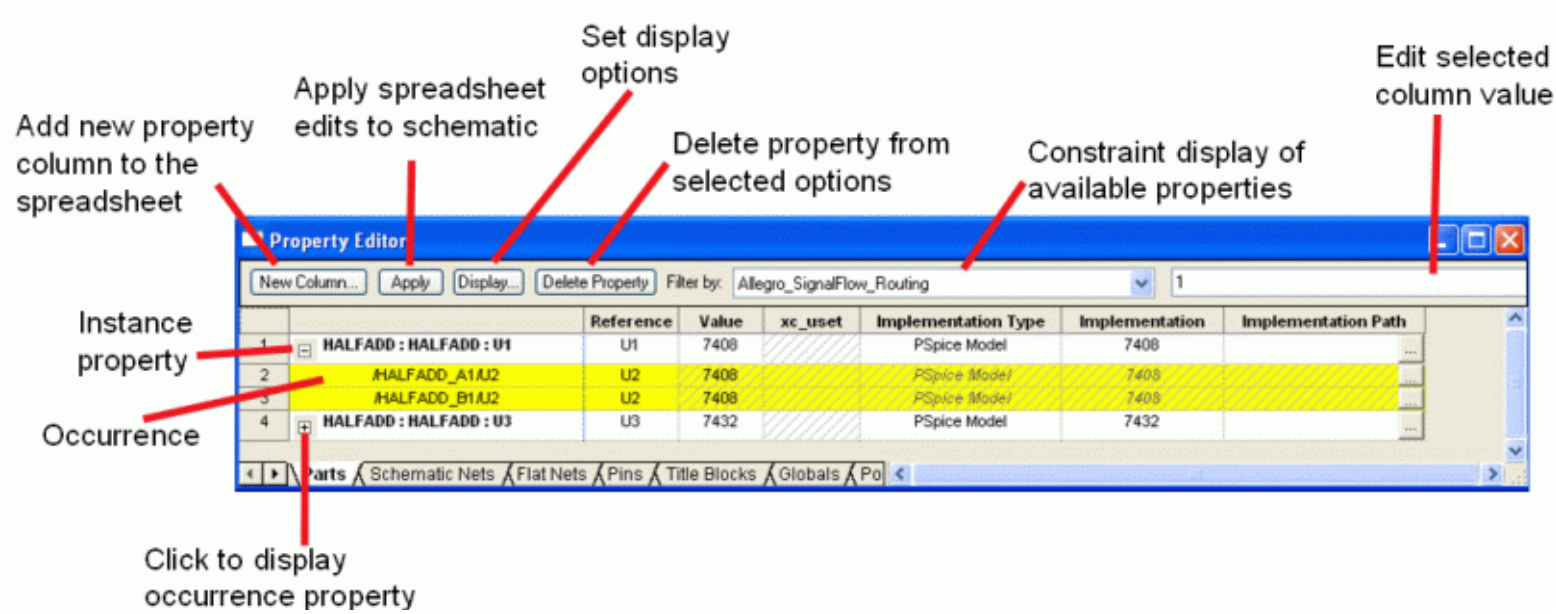
Hold down the SHIFT key and roll the mouse wheel up and down to scroll through horizontally in the Property Editor.

Tip

Click the mouse wheel button and drag the mouse wheel:

- To the right or left in the Property Editor window to scroll horizontally.

- Up or down in the Property Editor window to scroll vertically.



Changing the appearance of the property editor

You can edit the properties of a group of similar objects using a spreadsheet editor. The property editor is a spreadsheet editor you can use to edit instances or occurrence properties.

Any changes you make to the property editor spreadsheet appearance, such as sorting or moving columns or pivoting the spreadsheet, are saved to PREFPROP.TXT when you close the property editor window. The next time you open to that particular tab in that particular filter, you will see your last settings. This does not apply to any changes you make to the spreadsheet appearance while in the <Current properties> filter.

To pivot the property editor spreadsheet

1. Right-click the empty cell in the top-leftmost position of the spreadsheet.
2. From the pop-up menu, choose Pivot.

or

➤ Double-click the empty cell in the top-leftmost position of the spreadsheet.

- ❑ The default orientation of the spreadsheet shows property columns and instance and occurrence rows. You can add a new property by selecting the New Column button and entering a property name.
- ❑ If you pivot the spreadsheet, instances and occurrences appear in columns across the top, and properties appear in rows. This may be advantageous if your selected object or objects have several properties.

Note: The Find command searches down columns in the spreadsheet, regardless of the spreadsheet orientation.

To display or hide all occurrence properties with a single key stroke

➤ Press and hold the CTRL key while clicking on one of the plus (+) symbols in the leftmost column.

If you press and hold the CTRL key while clicking on a dash (-) symbol in the left column, all the occurrences collapse so that you only see the instance properties of your design.

To move columns in the property editor

1. Click the title cell of the column you want to move.
2. Release the left mouse button.
3. Click the title cell of the column again and drag the column to the new location.

Note: If the spreadsheet is pivoted, use these steps to move rows.

To sort columns in the property editor

1. Right-click on the column heading. A pop-up menu will appear.
2. Select Sort Ascending or Sort Descending.

or

➤ If the spreadsheet is not pivoted, double-click on the column heading to toggle the sort order between ascending and descending.

To change column widths in the property editor

1. Move the cursor to the right edge of the title cell of the column you want to resize.
2. When the down arrow changes to a double-sided arrow, click and drag the column edge.

Note: You can hold down the shift key while dragging the column edge to resize all columns to the same width. When the property editor is pivoted, these changes are saved on the tab and filter you were using

To create a new column or row in the property editor

1. In the schematic page editor, select the object or objects for which you want to create the property.
2. On the Edit menu, choose the Properties command. Capture displays the property editor.
3. Click the New Column/New Row button. Capture displays the Add new column or row dialog box.
4. Enter a name for the new property and click OK. Capture adds a new column or row to the property editor. Adding values in the cells of that column or row adds the property to selected objects.

To edit a property value

1. In the property editor, select the cell or group of cells that contain the value you want to change.
2. Right-click and choose Edit from the pop-up menu. The Edit Part Properties dialog box appears.
3. Type in the new value and press ENTER. Note that changing an instance property value causes that value to "shine through" to all occurrences of the instance that do not have a value independent of the instance.

Note: You cannot delete some property values that have particular significance to the design. Properties that are not editable appear in Italics.

To globally edit a property value on selected objects

1. In the property editor, click the top-leftmost cell to select the entire spreadsheet.
2. Right-click and choose Edit from the pop-up menu.
3. Select a property cell in the Edit Part Properties dialog box spreadsheet.
4. Type the new value and then click OK. The new property value appears on the spreadsheet for all selected objects.

Using the Filters menu in the property editor

The property editor filter is a powerful editing tool with which you can show or hide properties on selected objects. You can use the pop-up Filters menu on the spreadsheet to view the status of a property or edit columns, tabs, or the entire property editor spreadsheet.

You can add, delete, or change any filter except the <Current properties> filter. The <Current properties> filter displays all properties as undefined until you create or select another filter.

When you create a new filter, all properties appear undefined, just as in the <Current properties> filter. If you click the right mouse button on a column heading in the spreadsheet and point to Filters on the popup menu, you will see that each property is Undefined, and the filter specifies to Show Undefined.

The first four choices on the Filter menu apply to the appearance of a particular tab and column.

Show

The selected column will always appear when you use this filter, unless the filter is inverted.

Hide

The selected column will never appear when you use this filter, unless the filter is inverted.

Optional

The selected column will only appear if the property exists on one or more objects when you use this filter.

Undefined

The selected property is not defined. It is neither included in nor excluded from the filter.

You can control the display of undefined properties on individual tabs of the property editor with the next two choices on the Filters menu. Select any combination of the two.

Show Undefined

Specifies that any undefined property columns that are selected will appear when you use this filter. However, if you also select Invert Filter, these same selections will not appear.

Defined properties appear at the beginning of the spreadsheet (toward the left side) when you select Show Undefined.

Invert Filter

Specifies to show hidden property columns when you use this filter. Conversely, it will hide any property columns that you have specified to show. For example, if a property is optional and does not exist on any objects, you can use Invert Filter to show the property.

The last two menu choices affect all tabs on the property editor.

Add Filter

Specifies to add a new filter to all tabs. The default of a new filter is to show all properties as undefined.

Remove Current Filter

Specifies to delete the filter that displays in the Filter by list box from the list. You cannot undo this operation.

Your results will be more reliable if you use the property editor Filters menu to make changes rather than editing the PREFPROP.TXT file manually.

Changes to the filters are saved to PREFPROP.TXT when you close the spreadsheet. If you need to retrieve the original version, you can copy PREFPROP.TXT from the OrCAD installation CD in the Capture directory.

You can use the property editor filter to narrow the scope of properties it displays. Because you can have hundreds of properties assigned to your parts, nets, pins, and title blocks, it is more efficient to view only the properties you want to see. Capture provides a template that defines the properties that appear if you are targeting your design for PSpice or a board layout tool.

To use the property editor filter

1. From the schematic page, choose Select All command from the Edit menu.
2. Click the right mouse button and choose the Edit Properties command from the pop-up menu. The property editor appears.
3. Click the Parts tab to display all the properties of the parts you selected.
4. Click the Filter by drop-down list down arrow to expand the list of filters, then select a filter.
5. If you chose PCB Editor, for example, the displayed properties change to include those properties you might want to apply to your parts for use in a PCB netlist.
6. Enter a value into one of the cells and click Apply. The property and new values apply to your part.

To create a new filter in the property editor

1. Click the right mouse button on any column heading in the spreadsheet.
2. Point to Filters in the pop-up menu and choose Add Filter.
3. Type the new filter name in the Add Filter dialog box and click OK.

The new filter will be saved in PREFPROP.TXT when you close the property editor.

To edit a filter

1. Expand the Filter by drop-down list by clicking the down arrow.
2. Select a filter. The appearance of the properties on the spreadsheet may change when you change the filter.
3. Click the right mouse button on any column heading and point to Filters on the pop-up menu.
4. Use the Filters menu to change the property definitions and appearance on the spreadsheet.

Using the spreadsheet editor

The properties of a group of similar objects can be edited using a spreadsheet editor. Capture provides three spreadsheet editors for editing properties. The spreadsheet editors are the property editor, the browse spreadsheet editor, and the package properties spreadsheet editor.

The property editor

Use the property editor from the schematic page editor to edit properties for instances or occurrences of the following objects:

- Parts (including hierarchical blocks)
- Nets (including constituent nets within buses)
- Pins

- Title blocks
- globals
- Ports
- Aliases

Tip

Roll the mouse wheel up and down to scroll through vertically in the Property Editor.

Tip

Hold down the CTRL key and roll the mouse wheel to zoom in and zoom out.

Tip

Hold down the SHIFT key and roll the mouse wheel up and down to scroll through horizontally in the Property Editor.

Tip

Click the mouse wheel button and drag the mouse wheel:

- To the right or left in the Property Editor window to scroll horizontally.
- Up or down in the Property Editor window to scroll vertically.

The Browse spreadsheet editor

You can display the Browse spreadsheet editor from the Edit menu of the project manager, schematic page editor, or the part editor.

You can edit the following properties using the Browse command from the Edit menu in the project manager:

- Hierarchical ports
- Off-page connectors
- DRC markers

- Bookmarks
- Parts (including hierarchical blocks)
- Net (including constituent nets within a bus) occurrences
- Pin properties
- Title block occurrences
- Flat nets

In the schematic page editor, you can edit the following properties in the Browse spreadsheet by using the Properties command from the Edit menu:

- Off-page connectors
- DRC markers
- Bookmarks

From the part editor (while in Part View), you can edit the following properties using the Browse spreadsheet:

- Pin properties

The Browse spreadsheet editor browses the entire design for the objects you select, then displays their properties. Each property appears as a column heading in the spreadsheet. Each row is an object located by the editor.

It is important to note that, in the Browse spreadsheet editor you can edit only occurrences. The only exception being in the part editor, where you can only edit instances. To edit instance properties, you must use the property editor.

The Package Properties spreadsheet editor

Use the Package Properties spreadsheet editor to edit package properties of pins.

You can edit package properties using the Package Properties spreadsheet editor. The Package Properties spreadsheet editor is available in the part editor while in Package View. Use the Properties command on the Edit menu to display this spreadsheet. The spreadsheet displays all the package information on pins.

The Package Properties spreadsheet editor is similar to the Browse spreadsheet editor with the following differences:

The Package Properties spreadsheet editor doesn't have New or Remove buttons. You cannot add properties to a package, or remove existing properties.

The Package Properties spreadsheet has an Update button and a Validate button.

The Package Properties spreadsheet displays all of the pins in the package, regardless of what is selected in the part editor.

The package Properties spreadsheet displays two properties that do not show up in the Browse spreadsheet editor. These properties are PinGroup and Ignore.

Update

Use this to update the properties of all the pins in the package. This button is useful if you change a property on one pin, and need to change this property on the same pin in the other parts of the package. For example, say you have a four-part package. Each part in the package has a pin named IN. If you change this pin from a passive pin to an input pin in the A package part, you could use this button to update the type property for the IN pin in the B, C, and D package parts. The Update button updates all pins at once, without requiring that you click OK.

Validate

Use this button to check for duplicate pins. For example, suppose you have a pin 1, and then change another pin to pin 1. Using this button would detect the duplicate. This button checks for duplicate pin numbers, without requiring that you click OK.

To create a new property in the Browse spreadsheet editor

1. In the first column of the Browse spreadsheet, select the object or occurrence for which you want to create the new property.
2. From the Edit menu, choose Properties. Capture displays the object in a new Browse spreadsheet window.

3. Click New. Capture displays the New Property dialog box.
4. Enter a name and value for the new property, then click OK. Capture adds the property to the object or occurrence and displays the property in the original Browse spreadsheet.

To copy a value from one property to another property in the Browse spreadsheet editor

1. In the first column of the Browse spreadsheet, select the object or occurrence that has the property with the value you want to copy.
2. From the Edit menu, choose Properties. Capture displays the object in a new Browse spreadsheet window.
3. Select the cell that contains the value you want to copy.
4. Click Copy.
5. Select the cell that you want to contain the copied value.
6. Click Paste. Capture pastes the value into the selected cell.

Note: You can use the CTRL + C keys to copy a value from a cell and the CTRL + V keys to paste onto another cell in the Browse spreadsheet editor. Also, you can use the CTRL+ INSERT keys to copy a value from a cell in the Browse spreadsheet editor and paste it onto a cell in Microsoft Excel worksheet or use the SHIFT+ INSERT keys to paste values copied from Microsoft Excel onto a cell in the Browse spreadsheet editor.

To remove a user-defined property in the Browse spreadsheet editor

1. In the first column of the Browse spreadsheet, select the object or occurrence that has the property you want to remove.
2. Select the column heading for the property you want to remove.
3. Click Remove. Capture removes that property from the object.

Note: Some properties cannot be removed as they are essential for creating a netlist. You can only remove user-defined properties.

Note: If you remove a property from an occurrence for which there is a defined instance property, the occurrence property is not removed, but rather the instance property value "shines through" to the occurrence. To remove an instance property, you must use the property editor.

To replace property values

1. Select the objects whose properties you wish to edit. Note that the objects must be of the same type (for example, all pins or all hierarchical ports); otherwise, the Properties command is grayed out.
2. From the Edit menu, choose Properties. The Browse spreadsheet appears.
3. Double-click on a cell holding the value you wish to replace, then enter the new value.
4. Click the copy button.
5. Select the cells that are to receive the placement value.
6. Click the Paste button. The replacement value appears in the selected cells.
7. Click the OK button to close the Browse spreadsheet.

Defining properties

All objects are described by properties to which you can assign values to suit your needs. In addition, you can add to the set of properties for the object types listed below.

- Parts
- Hierarchical blocks
- Pins on library parts
- Buses
- Wires

For nets, you actually select a wire segment and add a property, but the property exists on the net rather than on the individual wire segment.

Note that you cannot add properties to graphic objects, bookmarks, IEEE symbols, no-connect objects, net aliases, power and ground symbols, off-page connectors, hierarchical ports, or bus entries.

You can add a property and specify the color, visibility, and font of the property text without assigning a value. The property name, which serves as a placeholder, appears next to the object and is enclosed in braces.

To add a user-defined property

1. Select a pin in the Part Editor.
2. From the Edit menu, choose the Properties command. The Pin Properties dialog box appears.
3. Click the User Properties button. The User Properties dialog box appears.
4. Click the New button. The New Property dialog box appears.
5. Enter a name for the new property. You may assign any name you wish, except that property names cannot be duplicated on a single object.
6. Enter a value for the new property.

or

1. Wait until another time to assign a value. Until then, Capture displays the property name, in braces, as a placeholder.
2. Click OK to close the New Property dialog box.
3. If you wish to make the property text visible, choose the Display button to open the Display Properties dialog box where you can specify visibility, color, rotation, and font. Complete your selections, then click OK.
4. Click OK twice to close the remaining dialog boxes.

or

➤ Use the property editor, as described in Using the property editor.

or

1. Use the Export Properties command to create a property file.
2. Edit the property file.
3. Use the Import Properties command to apply your changes.

Editing properties

All objects in Capture have attributes, or properties. Examples include the type of object (such as text, wire, or title block), part reference, color, font, and visibility. Some properties, called inherent properties, are essential to Capture—you cannot remove these inherent properties, though you can change the values of some of them. Other properties, called user-defined properties, may be used by external tools—they are not used by Capture, so you can add and modify these user-defined properties to suit your needs.

For information on editing the properties of a set of objects, see aUsing the spreadsheet editor. If you want to edit the properties of a part, see Assigning properties to the part.

Note: Except for occurrence properties, the schematics of externally-referenced libraries and designs should not be edited. You should view them as read-only designs. Trying to edit, then save, these designs from within your schematic can introduce errors such as duplicate reference designators and other problems.
When saving schematics with externally-referenced libraries or designs, occurrence properties are saved but altered instance values are not. If you want to change externally-referenced libraries or designs you should first close the referencing design. Then, open the referenced library or design, make the necessary changes, and save and close the referenced library or design. At this point, you can reopen the original design and reference the modified design.

To edit an object's properties

1. Double-click on the object.

2. Change the properties in the dialog box or spreadsheet editor that appears, then click OK or Apply.

or

1. Select the object.
2. From the Edit menu, choose the Properties command.
3. Change the properties in the dialog box or spreadsheet editor that appears, then click OK or Apply.

To edit the properties of a pin

1. In the part editor, select the pin.
2. From the Edit menu, choose Properties. The Pin Properties dialog box appears.
3. Change the properties.
4. Click OK to close the Pin Properties dialog box.

or

1. In the schematic page editor, select the pin.
2. From the Edit menu, choose Properties. The property editor appears.
3. Change the properties.
4. Click Apply, and close the property editor.

Note: Property changes made from the schematic page editor are limited to FLOAT and no-connect properties.

To edit the properties of multiple pins

1. In the part editor, hold the Ctrl key while you click to select each pin.
2. From the Edit menu, choose Properties command. The Browse spreadsheet appears.
3. Change the properties.
4. Click OK to close the Browse spreadsheet.

To edit properties associated with a net, wire, or bus

1. In the schematic page editor, select the net, wire, or bus.
2. From the Edit menu, choose Properties. The property editor appears.
3. Change the properties.
4. Click Apply, and close the property editor.

To edit properties associated with comment text

1. Select the text you want to edit.
2. From the Edit menu, choose Properties. The Display Properties dialog box appears.
3. Make the changes you want to the text, or its font, rotation, color, and visibility, then click OK.

To add a property to a part

1. Double-click on the part. The property editor appears.
2. Click the New button. The Add New Property dialog box appears.
3. Enter a name and value for the new property and click OK. You may enter any name you want, except that property names cannot be duplicated on a single object.
4. Click Apply, and close the property editor.

To change the visibility of property text

1. Double-click on the object. The property editor appears.
2. Select the property, then click the Display button. The Display Properties dialog box appears.
3. Select the appropriate Display Format option, and click OK.
4. Click Apply, and close the property editor.

To edit the name of a property

1. Double-click on the object. The property editor appears.
2. Select the property, edit its name in the Name property cell.
3. Click Apply, and close the property editor.

To delete a property

1. Double-click on the object. The property editor appears.
2. Select the property and click the Delete Property button. Only user-defined properties can be removed.
3. Click Apply, and close the property editor.

Note: To delete an occurrence property from a flat net, replace the property value with <null> in the property file. When you import the file, the property will be deleted. You cannot export instance properties using this method.

Importing part and pin properties

After you create a property file using the Export Properties command, you can use a spreadsheet, database, or word processing application to edit property values or to add or delete properties. See Assigning properties to the part for important information about the format and contents of a property file.

Note: Capture does not import all part and pin properties. So if a property is exported using the Export Properties command, it does not imply that you can change it's value and then import the change back into the part or pin. The thumb rule is that any property that is editable in the Property Editor in Capture and is exported can be imported. For example, the pin type property of a pin is exported by the Export command. However, if you EDT the value in the export file and import the file back into Capture, the pin type does not change.

Note: When you import the edited properties, Capture expects to find the schematic pages and parts unchanged. After you export properties, do not edit the project or library from which the properties were exported until after you import the changed properties. If you do, the Import Properties command will fail, and you will have to export and edit the properties again.

Note: It is a good idea to update (annotate) part references before you export properties.

Because various popular spreadsheet and database applications behave differently, Capture can import properties with or without enclosing quotation marks around each field in the property file. The fields must be tab-delimited, though—all other characters, including commas and leading and trailing spaces, are treated as part of a field's text. Be sure your spreadsheet or database program can save in this format.

Note: You can change reference designators by editing the Part References column of the property file.

Note: If Capture finds errors in the property file, the project or library remains unchanged. There is no risk that some parts will be changed and others not.

Note: The Import Properties command allows you to update the pin-type, pin-numbers and user-defined pin properties of the part.

Note: EXP files exported from version 16.2 cannot be imported in previous versions of Capture. However, EXP files exported from previous versions will import correctly in 16.2.

To import part properties or part and pin properties

1. Open the project with the design or library holding the parts.
2. From the Tools menu, choose the Import Properties command. The Import Properties dialog box appears.
3. Select the property file. If the property file is not listed, do one or more of the following:
4. In the Look in drop-down list box, select a new drive, a new directory, or both.
5. In the Files of type box, select the type of file you wish to open.
6. Click OK to apply the properties.

Note: If you edit a library provided by OrCAD, it is important that you assign a new library name so that your changes are not overwritten when you upgrade or update your software.

While importing or exporting a design, make sure that the property values do not contain a quote ' " ' symbol.

Exporting part and pin properties

The Export Properties and Import Properties commands provide a means to edit properties of parts and pins in a spreadsheet or database program, or in a text editor that preserves tab characters. You first export the properties to a property file, edit the property file in the application of your choice, then import the edited properties. See Editing Property Files below for important information about the format and contents of a property file.

Note: When you import the edited properties, Capture expects to find the schematic pages and parts unchanged. After you export properties, do not edit the project or library from which the properties were exported until after you import the changed properties. If you do, the Import Properties command will fail, and you will have to export and edit the properties again.

Note: It is a good idea to update (annotate) part references before you export properties.

Because various popular spreadsheet and database applications behave differently, Capture can import properties with or without enclosing quotation marks around each field in the property file. The fields must be tab-delimited, though—all other characters, including commas and leading and trailing spaces, are treated as part of a field's text. Be sure your spreadsheet or database program can save in this format.

Note: You can change part references by editing the References column of the property file.

Note: The Export Properties command outputs the device information for the part. So if a homogenous part has 2 sections, it will output information corresponding to both the sections. These sections can recognized in the EXP file through designator prefix.

Note: Pin-numbers will be output for each device/section of the part.

For a design, you can export all parts or just the parts in selected schematic folders and schematic pages. For a library, you can export all parts or just selected parts, but you cannot export part aliases. If you export and edit properties of a part that has aliases, the aliases reflect the changes.

You cannot select parts in the design cache or library cache for export.

You can add comments to document a property file; any text to the right of a semicolon (;) is ignored by the Import Properties tool.

Editing property files

When you export properties, Capture creates a tab-delimited list of keywords, identifiers, and properties, each of which is enclosed in double quotation marks. You can edit this file in a spreadsheet or database program, or even in a text editor (as long as the editor doesn't convert the tabs to spaces). Depending on which tool you use, you may see the property file as rows and columns of cells or fields or as lines of text.

The property file starts with a line identifying the document as either a design or library. Most subsequent lines begin with a keyword and an identifier.

Do not make changes in the ID, Net Name, and Net ID fields in the property file (*.exp). The changes will not reflect in your design when you use the Import Properties command***.***

Note: Making certain changes to the property file will cause the column headers and fields to be out of sync and invalidate your design You must not:

- change or delete the first line.
- delete the first field in any line.

- delete a field from a HEADER line without also deleting the corresponding fields from subsequent lines.

You can make these changes...	**with these results.**
Add a field to a HEADER line and subsequent lines (add a column).	This adds a property and pins with a value in this field. The name of the property is the string in the HEADER line. The value assigned to the part or pin is the string in the corresponding field. If the corresponding field is empty, Capture adds a property with no value and displays the property name as a placeholder.
Change a property value to <null>.	This deletes any existing property.
Delete a field from a HEADER line and subsequent lines (delete a column).	This has no effect on any part or pin. Deleting columns for properties you don't want to change may make the property file easier to edit. If you delete a field from a HEADER line without also deleting the corresponding fields from subsequent lines, Capture reports an error when you import the property and does not process any changes.
Change the value of a field.	Resets the value of the property on the object to which it refers.

The following table illustrates what happens when a part or pin has a property or does not have a property when a field is in various conditions:

Condition	**Part or pin has the property**	**Part or pin does not have the property**
Field is not <null>	Property value changes to specified value.	Property is added with specified value.
Field is <null>	Removes existing property.	Object is not affected.

Field is empty	Capture shows {Property Name} as place holder (when the property is visible).	Capture shows {Property Name} as place holder when the property as visible).

Capture property files contain the following keywords:

DESIGN	Identifies the property file as describing a project; specifies the path and filename of the project; identifies the mode active when the properties were exported.
LIBRARY	Identifies the property file as describing a library; specifies the path and filename of the library.
HEADER	Lists all the properties for the parts and pins in the design.
PAGE	Identifies the current schematic page.
PART	Identifies the current part and lists its properties. A column without a value signifies that the property does not apply to the part, or that no value is assigned.
PIN	Identifies a pin on the current part and lists its properties. A column without a value represents either a missing property or a property with an empty string for the value. A column without a value signifies that the property does not apply to the pin, or that no value is assigned.
SYMBOL	Identifies a symbol and lists its properties. A column without a value signifies that the property does not apply to the symbol, or that no value is assigned.

Note: It is a good idea to update (annotate) part references before you export properties.

Because various popular spreadsheet and database applications behave differently, Capture can import properties with or without enclosing quotation marks around each field in the property file. The fields must be tab-delimited, though—all other characters, including commas and leading and trailing spaces, are treated as part of a field's text. Be sure your spreadsheet or database program can save in this format.

To export part properties or part and pin properties

1. Open the project with the design or library holding the parts.
2. For a design, select the schematic folders or schematic pages containing the part you want to export.

or

1. For a library, select the parts to export.
2. From the Tools menu, choose Export Properties command. The Export Properties dialog box appears.
3. In the dialog box, specify whether the property file is to include the entire design or a selected portion, whether you want to export properties for pins as well as parts or flat nets, and whether you want to export instance or occurrence properties.
4. Before you click OK in the dialog box, note the location of the export file in the Export File text box.
5. Click OK to create the property file.

Note: If you edit a library provided by OrCAD, it is important that you assign a new library name so that your changes are not overwritten when you upgrade or update your software.

While importing or exporting a design, make sure that the property values do not contain a quote ' " ' symbol.

For projects

Capture reports a part once for each place it is used in the design. One HEADER line applies to the entire project.

Note: This abbreviated sample of a property file is formatted for presentation. As plain text, the columns do not actually line up as shown. In a spreadsheet or database program, fields may wrap or appear to be truncated.

```
"DESIGN" "C:\CAPTURE\SAMPLES\4BIT.DSN" "PHYSICAL"
"HEADER" "ID" "Part Reference" "Value"
"PART" "32" "fulladd_1" "FULLADD"
"PIN" "0{X}"
```

```
"PIN" "1{Y}"
"PIN" "2{SUM}"
"PIN" "3{CARRY_IN}"
"PIN" "4{CARRY_OUT}"
"PART" "152" "fulladd_4" "FULLADD"
"PIN" "0{X}"
"PIN" "1{Y}"
"PIN" "2{CARRY_OUT}"
"PIN" "3{CARRY_IN}"
"PIN" "4{SUM}"
"PART" "272" "fulladd_3" "FULLADD"
"PIN" ...
 :
"PART" "392" "fulladd_2" "FULLADD"
"PIN" ...
 :
"PART" "54" "halfadd_B" "HALFADD"
"PIN" ...
 :
"PART" "103" "halfadd_A" "HALFADD"
"PIN" ...
 :
"PART" "69" "U?" "74LS04"
"PIN" ...
 :
"PART" "74" "U?" "74LS08"
"PIN" ...
 :
"PART" "80" "U?" "74LS04"
"PIN" ...
 :
"PART" "85" "U?" "74LS32"
"PIN" ...
 :
"PART" "174" "halfadd_B" "HALFADD"
"PIN" ...
 :
"PART" "223" "halfadd_A" "HALFADD"
"PIN" ...
 :
"PART" "189" "U?" "74LS04"
"PIN" ...
 :
"PART" "194" "U?" "74LS08"
"PIN" ...
 :
"PART" "200" "U?" "74LS04"
"PIN" ...
 :
"PART" "294" "halfadd_B" "HALFADD"
"PIN" ...
 :
"PART" "343" "halfadd_A" "HALFADD"
"PIN" ...
 :
"PART" "309" "U?" "74LS04"
"PIN" ...
 :
"PART" "314" "U?" "74LS08"
"PIN" ...
 :
```

```
"PART" "414" "halfadd_B" "HALFADD"
"PIN" ...
 :
"PART" "463" "halfadd_A" "HALFADD"
"PIN" ...
 :
"PART" "429" "U?" "74LS04"
"PIN" ...
 :
```

For libraries

Capture reports each part in the library.

Note: This abbreviated sample of a property file is formatted for presentation. As plain text, the columns do not actually line up as shown. In a spreadsheet or database program, fields may wrap or appear to be truncated.

```
"LIBRARY" "C:\CAPTURE\SAMPLES\INTEL.OLB"
"HEADER" "ID" "Part Reference"
"PART" "80186.Normal"
"PIN" "X1"
"PIN" "X2"
"PIN" ...
 :
"PART" "80188.Normal"
"PIN" "X1"
"PIN" ...
 :
"PART" "80286.Normal"
"PIN" ...
 :
"PART" "80287.Normal"
"PIN" ...
 :
"PART" "8031.Normal"
"PIN" ...
 :
"PART" "8032.Normal"
"PIN" ...
 :
"PART" "80386.Normal"
"PIN" ..
 :
"PART" "80386SX.Normal"
"PIN" ...
 :
```

Removing part reference assignments

If you want to incrementally update a design in which some of the schematic pages have already been updated, you can use the

Annotate command to remove part references from those schematic pages.

To remove part references

1. In the project manager, select schematic folders or schematic pages if you want to process only a portion of the design. If you want to process the entire design, leave the schematic folders or schematic pages unselected.
2. From the Tools menu, choose Annotate. The Annotate dialog box appears.
3. In the Action group box, select Reset part references to "?," select other options as appropriate, then click OK.

Shortcu

Toolbar:

9

Scripting Support

This chapter covers:

- “Introducing Scripting in Capture” on page 461
- “Using the Capture Command window” on page 461
- “Creating a Capture TCL Script” on page 464
- “Executing a Capture TCL script” on page 467

Introducing Scripting in Capture

OrCAD Capture includes a scripting functionality that allows you to execute a Capture command through a command prompt. Capture also provides the facility to store and later replay the command.

Every Capture command is logged in the form of a TCL script command. This command that logged is registered with a TCL interpreter. When the command is played back, Capture uses the TCL interpreter to retrieve the command and execute it in Capture. However, this process is completely abstracted from the Capture. This makes logging and replaying of a set of commands an intuitive and simple task.

The user resources are then better utilized to actually identify the type of script (set of steps) that is required for a specific task.

Using the Capture Command window

The Capture environment includes a Command window. You use this window to execute a TCL command. Also, when you perform an operation (function) in Capture, the associated command is

registered with the TCL interpreter and the command is logged in the Command window.

To Open the Command window

1. Right-click on the Capture menu bar.
2. Choose Command Window from the short-cut menu.

The Command window displays with the capture> prompt.

Note: Any operation you perform in Capture is registered with the TCL interpreter and logged by Capture even if the Command window is closed.

Registering and Logging TCL Commands

When you perform an operation in Capture, the associated command is registered with the TCL interpreter and the command is logged in the Command window.

Menu Commands

In Capture, you perform operations that include menu commands. These commands are logged with the TCL interpreter as menu commands.

For example, to open a new design you choose File - New - Design.

As soon as you complete the menu selection, the associated command is registered with the TCL interpreter and the command is logged in the command window as:

```
Menu "File::New::Design"
```

Similarly, the command to open the part editor for a selected part on a schematic is:

```
Menu "Edit::Part"
```

Notice, when you perform any operation that is associated with a Capture menu, the associated command syntax includes the text Menu followed by the menu selection.

You can use this procedure to easily identify the TCL command associated with any operation in Capture.

Page Editor Commands

You can also log and register any operation in a schematic page.

For example, if you select or un-select all the objects on a schematic page, the associated TCL commands are:

```
SelectAll
```

```
UnSelectAll
```

Similarly, the following command will place a wire with the co-ordinates of the start point at 1, 3 and end point at 6, 3:

```
PlaceWire 1 3 6 3
```

Project Manager Commands

You can log and register command for operations performed on the Project manager.

For example, the following command will select the project item with the name Page1:

```
SelectPMItem "Page1"
```

The command to open a page Page1 in the schematic folder BENCH is:

```
OPage “Page1” “BENCH”.
```

Similarly, to identify a command, you perform the required operation in the Project Manager and the command in logged in the Capture Command window.

Executing a TCL Command

You use the Command window in Capture to execute a TCL Command.

To execute a TCL Command in the Command window, you simply type the command in the Command window and press Enter.

If an error occurs in executing the command, the error message displays in the Command window.

Note: All TCL commands are case-sensitive.

Note: Besides the Capture TCL commands, you can also execute all the native TCL commands from the Capture Command window.

For example, the following native TCL command returns the absolute path of the current (present) working directory:

pwd

And to change the working directory, use:

cd

Creating a Capture TCL Script

You can create a Capture TCL script manually, in any text editor, or by executing the series of steps in Capture. and allowing Capture to record the associated commands.

When you allow Capture to record TCL commands corresponding to the Capture commands, you can create a:

TCL Script for all Capture commands on page 464

TCL script for specific Capture commands on page 466

TCL Script for all Capture commands

When you perform an operation in Capture, the associated TCL command is registered with the TCL interpreter. The command is logged to a Capture TCL file. In addition, the command displays in the Capture Command window.

To enabled logging each command that you execute in Capture to a TCL script file, you need to execute the SetOptionBool command in the Capture Command window.

```
SetOptionBool Journaling TRUE
```

This is because, the TCL logging feature in Capture is disabled, by default.

Also, if you are in the TCL command logging mode, you can view each executed Capture command in the Command window. Use the SetOptionBool command to enable viewing of the corresponding TCL command for each Capture command in the Command window.

```
SetOptionBool DisplayCommands TRUE
```

If you enable the display of TCL commands, the TCL commands, for each Capture command, are displayed in the session log. However, one Capture command corresponds, in some cases, to a set of multiple TCL commands. Also, the Capture operation is performed only after the corresponding TCL commands are displayed in the session log. This implies that if a Capture command corresponds to a number of TCL commands, this may cause a delay in completing the Capture command. To avoid this display, you can turn off the display functionality using the SetOptionBool command using the FALSE argument.

```
SetOptionBool DisplayCommands FALSE
```

For this reason,command display in the Command window is disabled, by default.

Location of the TCL file

If you enable TCL logging in Capture (using the SetOptionBool command), a TCL file, for each Capture session, is created in the Temp\CAPTURELOG directory.

The location of the Temp directory is defined in the following order of preference:

- The path specified by the TMP environment variable
- The path specified by the TEMP environment variable
- The path specified by the USERPROFILE environment variable
- The Windows directory

This directory contains the Capture TCL file OrCaptureLogFile.captcl along with support files required to execute the script.

Capture Dialog settings in TCL

When you perform an operation in Capture that involves a dialog box (like Options - Preferences), the Capture TCL logging feature saves the complete dialog settings to an Xml file. This file is placed in the same location as the current session TCL file.

For example, to annotate a design you use the Annotate dialog box.

The associated TCL command for this operation is:

Menu "Tools::Annotate" | DialogBox "OK" "C:/Temp/CAPTURELOG/Wed_Nov_18_14_34_45_2009/Packaging_6.xml"

Notice that an Xml file is one of the arguments in the TCL command. Also, notice the location of the Xml file is the same as the location of the current Capture session TCL file.

Note: The location of the CAPTURELOG directory in the above example is C:\Temp. However this may change depending on the conditions as described in the Location of the TCL file section.

TCL script for specific Capture commands

When you turn on TCL script logging, the TCL commands for every Capture command that you execute are logged to the TCL session file. However, you can also create a TCL script with a specific set of Capture commands.

To create a script of a set of Capture commands

1. Right-click in the Capture Command window and choose Clear All.
2. Perform the Capture steps for which you want to record the corresponding TCL commands.
3. After completing the set of Capture steps, right-click in the Command window and choose Save.

4. In the Save TCL Script dialog, specify the name and location of the script.

Note: The resultant script also includes the final steps to save the TCL file. You can open the script in a text editor to edit any extra steps that may have been recorded.

If you save a specific set of Capture commands, any support files required to execute these commands are not saved along with this script. For example, the dialog settings that are saved to an Xml will not be saved along with the script. See Capture Dialog settings in TCL. In this case, the settings Xml is saved to the session TCL file location. For details see Location of the TCL file.

Executing a Capture TCL script

After creating a Capture TCL script (for details see Creating a Capture TCL Script), you can execute the script to replay the set of commands defined in the script. You can execute a TCL from the Capture Command window or from the Windows Command line.

Execute TCL script in Capture on page 467

Execute TCL script in Windows on page 468

Execute TCL script in Capture

You can execute a TCL script directly from the Capture Command window by the source command.

```
source <Script Path and Name>
```

For example, to execute the script, D:\Cadence\tclsamples\selectObjs.tcl

```
source D:/Cadence/tclsamples/selectObjs.tcl
```

Note: To specify a file location in a TCL command argument, you need to use the / (forward slash) path separator.

Alternatively, if you use the \ (backward slash) path separator, you can enclose the argument in curly braces to ensure that argument is treated as a literal.

```
source {D:\Cadence\tclsamples\selectObjs.tcl}
```

Important

If a script file path contains spaces, you need to enclose the path in double-quotes. Also, you must use the / (forward slash) path separator and exclude the curly braces.

If you execute a TCL script in Capture that contains errors, the script exists after it encounters the first error and the error is displayed in the Capture session log. Also, you can use the ? alias to get details of the last TCL error. This implies that if you type ? in the Command window and press Enter, the last error encountered by the TCL interpreter will be displayed in the Command window.

Execute TCL script in Windows

You can execute a TCL script directly from the Windows command line. This implies that you do not need to need to open Capture to execute the script.

In this case, you need to pass the script name and path as a command line argument to Capture. This will ensure that Capture will open and all the steps defined in the script will execute.

To execute the script from the command line:

```
capture <Script Path and Name>
```

Note: After the script executes, it opens as a text file in edit mode in Capture.

The path separator rules to execute TCL script from the Windows command line are the same as the rules for executing a script from the Capture command window. For details see Execute TCL script in Capture

Tip

You can create nested TCL scripts by including the TclScript command to call a TCL script from within another TCL script.

10

Functional simulation

This chapter covers:

- "Compiling vendor simulation libraries" on page 472
- "Selecting the configuration for functional simulation" on page 473
- "Setting the simulation mode for functional simulation" on page 474
- "Starting NC VHDL for functional simulation" on page 475

In the typical FPGA flow, functional simulation provides a method for verifying the logic of your design without regard for timing constraints. That is, the simulation determines that the design produces outputs that coincide with applied inputs irrespective of gate or propagation delays, and that, therefore, the logic of the design is correct.

Functional simulation occurs before the actual implementation of the design (before synthesis and place-and-route).

If you determine that the design logic does not produce expected results, you can return to the design creation stage to correct any logic problems before committing the design to timing-specific gates.

The Cadence FPGA flow uses NC VHDL as the simulation tool for functional simulation.

For information specific to using the Capture tool suite with your particular vendor, please refer to the technical documents located on the Cadence web site: http://www.cadence.com/orcad.

Compiling vendor simulation libraries

In order to simulate your design with NC VHDL, you must compile the simulation library that corresponds to the target technology. For example, if the target technology for your design is Xilinx XC9500, in order to simulate the design, you must compile the Xilinx UNISIM libraries.

Note: You need only compile your simulation libraries once. If you have compiled a particular simulation library previously, you can skip this procedure. However, if you update your vendor libraries, or if you obtain a new version of NC VHDL, you must recompile the simulation libraries.

To compile the simulation library for the target vendor

1. From the Tools menu, choose Compile vendor libraries. Capture displays the NC VHDL Library Compilation dialog box.
2. In the list box, select the set of libraries that corresponds to the target technology of your design.

   Note: Legacy programmable logic projects (that is, projects created with a version of Capture previous to version 14.2) that include schematic components from the Xilinx XC4000E library, must use the OrCAD XC4KE VHDL libraries for simulation. However, Xilinx XC4000E schematics created with Capture version 14.2 (or any later versions), or schematics that have been modified to include the new Xilinx XC4000E part symbols, must use the UNISIM VHDL libraries for simulation.
3. If desired, select the Run display in session log option to include the results of the compilation in Capture's session log.
4. In the CMD Path text box, type (or browse for) the path to, and name of, the command file that contains the compile options for the vendor library.
5. Click the Compile button. Capture then compiles the simulation libraries.

The target vendor may include options for the compilation. You can specify any such options in the command file associated with the simulation libraries. An example command file, for Xilinx XC4000E libraries, is illustrated below:

```
echo off
rem -- File name: C_x4ke.bat
rem --
rem -- DESCRIPTION
rem -- This is a batch file to compile Xilinx XC4000E
prerouted simulation models
rem -- Two files will be compiled in Cadence NC VHDL Desktop
simulator:
rem -- 1> .\FPGA_LIB\library\xilinx\x4ke\x4ke.vhd
rem -- 2> .\FPGA_LIB\library\xilinx\x4ke\x4ke_m.vhd
rem --
rem -- The compiled library will be named: x4kelib
rem --
rem -- Before running this file, please made sure that Cadence
NC VHDL Desktop simulator
rem -- was installed.
rem --
rmdir /S /Q .\sim_lib\x4kelib
mkdir .\sim_lib\x4kelib
echo on
ncvhdl -v93 -work x4kelib -log ncvhdl.log -messages
.\Xc4000e\x4ke.vhd .\Xc4000e\x4ke_m.vhd
```

Selecting the configuration for functional simulation

When you select the Preroute configuration for simulation, Capture creates a VHDL netlist of your design as it currently exists in the project manager and stores it in the Preroute folder. This netlist does not include timing information, and uses unit/delay for all components in the design. The purpose of functional simulation, as the name implies, is to verify logical functionality of the design without accounting for the timing of specific components or net delays.

To select the configuration for functional simulation

1. From the Picflow menu, choose the Simulate command. Capture displays the Select Simulation Configuration dialog box.
2. Select Preroute in the selection window. This indicates that you want to simulate your design functionality, without timing considerations.
3. Click OK. Capture generates a VHDL netlist of your design and stores it in the Preroute folder of the project manager, then displays the NC VHDL Preroute Simulation dialog box
4. Specify either interactive or batch mode for the NC VHDL session.

5. Click the Setup button. Capture displays the NC VHDL Preroute Simulation Setup dialog box.
6. Complete the dialog box as described in Starting NC VHDL for functional simulation.

Setting the simulation mode for functional simulation

When you select the simulation mode, choose the method that best provides for your needs. That is, if you want to experiment with different simulation resolutions, or run the simulation for different run times, choose Interactive mode. If you have already developed a simulation session that covers your design, and have saved it in a batch file, choose Batch mode.

Note: For information and hints on creating an NC VHDL batch file, see NC VHDL batch files.

To set the simulation mode to interactive for functional simulation

1. In the NC VHDL Preroute Simulation dialog box, choose the Use Interactive option.
2. Click the Setup button. Capture displays the NC VHDL Preroute Simulation Setup dialog box, from which you can start NC VHDL.

To set the simulation mode to batch for functional simulation

1. In the NC VHDL Preroute Simulation dialog box, choose the Specify Batch File option.
2. Enter the path to, and name of the batch file in the text box. For information on creating a batch file, see NC VHDL batch files.
3. Click the Setup button. Capture displays the NC VHDL Preroute Simulation Setup dialog box, from which you can start NC VHDL.

Starting NC VHDL for functional simulation

NC VHDL is the Cadence VHDL simulation tool suite that provides the means by which you can simulate your Capture design for both functional simulation (sometimes called functional verification) and timing simulation. For the specifics of working with NC VHDL, please refer to your NC VHDL documentation.

To start NC VHDL in interactive mode

1. In the Simulation tab (NC VHDL) of the NC VHDL Preroute Simulation Setup dialog box, in the Options area, set the paths to, and names of, your HDL.VAR file and Log directory.
2. In the Flow options area, specify the particular options you want to run in the NC VHDL session. These include:

   Compile: Specify that NC VHDL compile your design for simulation. This is a prerequisite for actually performing the simulation. You can provide command line options for the compile in the Command Options text box, by entering them exactly as you would from the command line.

   Note: You must also have compiled the simulation models that correspond to the target vendor library before you can simulate your design. See Compiling vendor simulation libraries for more information.

   Elaborate: Specify that NC VHDL perform elaboration (the process of mapping your design to machine code that NC VHDL can interpret) on your design. This is a prerequisite for actually performing the simulation. You can provide command line options for the elaboration in the Command Options text box, by entering them exactly as you would from the command line.

   Simulate: Run the simulation in interactive mode. You can provide command line options for the simulation in the Command Options text box, by entering them exactly as you would from the command line.

   Note: You need only compile and elaborate your design once. After that, when you start NC VHDL, you can skip the Compile and Elaborate steps, provided that the design has not changed

since your last simulation run.

3. In the Sim Vision launch area, specify the particular options you want to run in the NC VHDL session. These include:

   Start Sim Vision: Causes NC VHDL to display its user interface in a new window on the screen. If you do not choose this option, NC VHDL runs in the background using the command options you have specified for Compile, Elaborate, and Simulate. In effect, this is similar to running NC VHDL in batch mode, but rather than using a batch file, NC VHDL uses the options specified in the NC VHDL dialog box.

4. Enter Interactive Mode: Causes NC VHDL to set simulation time to 0 and await your inputs in order to run the simulation. This option is only available if you have selected the Start Sim Vision option.

5. Choose the Testbench tab (NC Verilog) tab, and specify whether you want to generate a new testbench for your design, include an existing testbench, or not include a testbench in the current NC VHDL session.

   Note: If you choose None (that is, if you specify that no testbench should be included), you cannot simulate your design, since testbenches provide the stimulus. In general, you should only choose None when you want to compile and/or elaborate your design without simulating it.

6. Click OK. Capture returns to the NC VHDL Preroute Simulation dialog box.

7. Click Run to start the simulation session.

11

Synthesis and place-and-route

This chapter covers:

- "Synthesis with Synplify" on page 477
- "Place-and-route using the vendor tool set" on page 478

After you have checked your design for behavioral compliance (using functional simulation), the next step is to implement it using timing-specific components from your vendor library. This is accomplished in two major steps:

Synthesis (including optimization), where any HDL modules in the design are implemented using vendor components and then optimized using logic optimization algorithms;

Place-and-route, where the design is mapped to a particular device from the target vendor.

Capture uses Synplicity's Synplify tool to perform synthesis and optimization, and uses the place-and-route tool specific to the target vendor for device mapping.

For information specific to using the Capture tool suite with your particular vendor, please refer to the technical documents located on the Cadence web site: http://www.cadence.com/orcad.

Synthesis with Synplify

When you perform synthesis on your design, Synplify creates a structural (gate level) representation of all the schematic and VHDL components of your design. This structural representation is in the form of an EDIF netlist that you can then use an input for the vendor place-and-route tool.

Synplify also optimizes your design as part of the synthesis process. The optimization removes extraneous logic while maintaining any hierarchical boundaries for the design.

To perform synthesis and optimization on your design with Synplify

1. From the PICFlow menu, choose the Synthesize command. Capture saves a VHDL netlist of the design and stores it in the Synthesis folder of the project manager, then displays the Synthesis Option dialog box.
2. Choose Interactive Mode if you want to run Synplify interactively.

or

1. Choose Batch Mode, if you want to run Synplify in batch mode and have a batch file that specifies the parameters for the synthesis session.
2. Select the Create Synplify Project option if you want to create a new Synplify project for this simulation run. Alternately, you can leave this option unselected and specify an existing Synplify project in the text box. However, a Synplify project must exist in order to run Synplify. Any Synplify project is created and stored in the Synthesis directory (of the project manager).
3. Click Run. Capture invokes Synplify according to the parameters you set.

Place-and-route using the vendor tool set

The tool suite that Capture invokes for the place-and-route process depends on the target technology you have chosen for your programmable logic project. Of course, you must have installed the tool suite appropriate to the target technology in order for Capture to start the tool.

Each vendor has a unique tool suite that performs place-and-route for designs that use its technology. The following table provides an (incomplete) list of possible tool suites that correspond to some

vendor technologies. This is not a complete list. Contact your vendor for information on the exact tool suite your require.

Vendor	Tool suite
Actel	Actel Designer
Altera	MAX+PLUS II
Xilinx	Design Manager

To initiate place-and-route for your design

1. From the PICFlow menu, choose the P&R command. Capture displays the Enter EDIF Netlist Location dialog box.
2. Enter the path to, and name of, the EDIF netlist that resulted from the synthesis run.
3. Click Run. Capture starts the vendor tool appropriate to the target technology of your design.

12

Timing simulation

This chapter covers:

- "Selecting the configuration for timing simulation" on page 482
- "Setting the simulation mode for timing simulation" on page 482
- "Starting NC VHDL for timing simulation" on page 483
- "Generating a part (for FPGA projects)" on page 485

Timing simulation provides a method for you to check your design to be sure that the timing properties of the components in the target vendor do not change the functionality of your design. That is, timing simulation allows you to be sure that propagation delays and other factors (setup times, capacitance, hold times, and so on) are within the tolerance levels of your design such that they do not affect the design's logic.

Timing data is generally included in your design during the place-and-route process and takes the form of a standard delay file (SDF) or an annotated VHDL netlist. These files are generated by your vendor's place-and-route tool.

The Cadence FPGA flow uses NC VHDL as the simulation tool for timing simulation.

For information specific to using the Capture tool suite with your particular vendor, please refer to the technical documents located on the Cadence web site: http://www.cadence.com/orcad.

Selecting the configuration for timing simulation

When you select the Postroute configuration for simulation, Capture creates a VHDL netlist of your design as it currently exists in the project manager and stores it in the Postroute folder. Capture includes any SDF file associated with the design in the Postroute folder, as well.

To select the configuration for timing simulation

1. From the Picflow menu, choose the Simulate command. Capture displays the Select Simulation Configuration dialog box.
2. Select Postroute in the selection window. This indicates that you want to simulate the timing of your design using post-place-and-route, vendor-specific delays.
3. Click OK. Capture generates a VHDL netlist of your design and stores it in the Postroute folder of the project manager, then displays the Place and Route Settings dialog box dialog box.
4. Specify the paths for the place-and-route netlist and standard delay file created by your vendor place-and-route tool, then click OK. Capture displays the NC VHDL Simulation dialog box.
5. Specify either interactive or batch mode for the NC VHDL session.
6. Click the Setup button. Capture displays the NC VHDL Simulation Setup dialog box.
7. Complete the dialog box as described in Starting NC VHDL for timing simulation.

Setting the simulation mode for timing simulation

When you select the simulation mode, choose the method that best provides for your needs. That is, if you want to experiment with different simulation resolutions, or run the simulation for different run times, choose Interactive mode. If you have already developed a

simulation session that covers your design, and have saved it in a batch file, choose Batch mode.

Note: For information and hints on creating an NC VHDL batch file, see NC VHDL batch files.

To set the simulation mode to interactive for timing simulation

1. In the NC VHDL Simulation dialog box dialog box, choose the Use Interactive option.
2. Click the Setup button. Capture displays the NC VHDL Postroute Simulation Setup dialog box, from which you can start NC VHDL.

To set the simulation mode to batch for timing simulation

1. In the NC Verilog Simulation dialog box, choose the Specify Batch File option.
2. Enter the path to, and name of the batch file in the text box. For information on creating a batch file, see NC VHDL batch files.
3. Click the Setup button. Capture displays the NC VHDL Postroute Simulation Setup dialog box, from which you can start NC VHDL.

Starting NC VHDL for timing simulation

NC VHDL is the Cadence VHDL simulation tool suite that provides the means by which you can simulate your Capture design for both functional simulation (sometimes called functional verification) and timing simulation. For the specifics of working with NC VHDL, please refer to your NC VHDL documentation.

To start NC VHDL in interactive mode

1. In the Simulation tab (NC VHDL) of the NC VHDL Postroute Setup dialog box, in the Options area, set the paths to, and names of, your HDL.VAR file and Log directory.
2. In the Flow options area, specify the particular options you want to run in the NC VHDL session. These include:

- Compile: Specify that NC VHDL compile your design for simulation. This is a prerequisite for actually performing the simulation. You can provide command line options for the compile in the Command Options text box, by entering them exactly as you would from the command line.

  Note: You must also have compiled the simulation models that correspond to the target vendor library before you can simulate your design. See Compiling vendor simulation libraries for more information.

- Elaborate: Specify that NC VHDL perform elaboration (the process of mapping your design to machine code that NC VHDL can interpret) on your design. This is a prerequisite for actually performing the simulation. You can provide command line options for the elaboration in the Command Options text box, by entering them exactly as you would from the command line.

  Note: In order to include an SDF file in the simulation, you must specify the path to, and name of the SDF file in the Command Options text box for the elaboration. The specific option is as follows:

  -sdf_cmd_file *directory/sdf_filename*

- Simulate: Run the simulation in interactive mode. You can provide command line options for the simulation in the Command Options text box, by entering them exactly as you would from the command line.

Note: You need only compile and elaborate your design once. After that, when you start NC VHDL, you can skip the Compile and Elaborate steps, provided that the design has not changed since your last simulation run.

3. In the Sim Vision launch area, specify the particular options you want to run in the NC VHDL session. These include:

   - Start Sim Vision: Causes NC VHDL to display its user interface in a new window on the screen. If you do not choose this option, NC VHDL runs in the background using the command options you have specified for Compile, Elaborate, and Simulate. In effect, this is similar to running NC VHDL in batch mode, but rather than using a batch file,

NC VHDL uses the options specified in the NC VHDL dialog box.

- Enter Interactive Mode: Causes NC VHDL to set simulation time to 0 and await your inputs in order to run the simulation. This option is only available if you have selected the Start Sim Vision option.

4. Choose the Testbench tab (NC VHDL), and specify whether you want to generate a new testbench for your design, include an existing testbench (perhaps the same testbench you used for functional simulation), or not include a testbench in the current NC VHDL session.

   Note: If you choose None (that is, if you specify that no testbench should be included), you cannot simulate your design, since testbenches provide the stimulus. In general, you should only choose None when you want to compile and/or elaborate your design without simulating it.

Generating a part (for FPGA projects)

Once you have created the final programmable logic netlist, you can generate a part for your project. This part represents the FPGA/CPLD component that is the result of the programmable logic design flow.

"Introduction" on page 485

"To generate a part for your FPGA" on page 486

"Supported Vendor Pad and Pin file formats" on page 489

Introduction

Capture reads a variety of PLD vendor pin reports to create library parts for the Capture schematic system. Most PLD vendor pin reports (Actel, Vantis, Lattice, Lucent, OrCAD SPLD, and Xilinx formats) describe the pin number, signal name, and direction (or mode) of a package pin programmed by the place-and-route process. When you create a new part with the Generate Part command, Capture creates a new schematic library (OLB) and part based on the pins defined in the report file. You can also define multiple sections for the part based

on I/O Bank information present in the .pin or .pad files by selecting the Create multi-section part option in the FPGA Options dialog box. If you want to have separate power/GND symbols, you can use the Separate Symbols for Power/NC pins options to achieve that goal. The Power/NC pin limit will create the Power/GND symbols based on the set limit and will generate a new symbol if the limit is exceeded. You can now also assign auto-pingroup values to the pins in a given section. Pins can be grouped together according to I/O Bank or pins with compatible I/O Standards within an I/O Bank. Pins are sorted alphabetically by name, with input type pins located on the left and output or bidirectional pins on the right.

Generate part can create new parts or update the pin numbers of an existing library part with the Update pins on existing part in library option, which allows for engineering change orders (ECOs) from a programmable logic project to update the part of the system schematic.

The most common Implementation type used with the parts created from PLD vendor pin reports is type <none> or Project to create a hierarchy of projects for system simulation.

Capture can read an EDIF netlist or VHDL or Verilog model created by 3rd-party EDA tool or intellectual property (IP) provider to create library parts for a programmable logic project. Most 3rd-party synthesis and module generators describe the port name and mode of the signals that interface to the EDIF netlist, VHDL model, or Verilog model.

Note: To create a pin on a symbol using the Generate Part utility, the pin must have a pin to port mapping in the pin file.

To generate a part for your FPGA

1. From the Tools menu in the project manager, choose the Generate Part command. Capture displays the Generate Part dialog box.
2. Specify the final, fitted netlist in the Netlist File Name text box. Use the Browse button to locate the netlist file, if necessary. When you select a netlist with the Browse button, Capture places default values in the Part Name and Part Library Name text boxes, and automatically selects a Vendor File Type according to the file extension of the netlist file.

3. If necessary, enter a name and library for the part in the appropriate text boxes.
4. Specify that the part is a new part or that you want to update pins on an existing part in the library with the appropriate radio button.
5. Specify ascending or descending order for the part pins.
6. If you want to specify additional pins for the part, select the appropriate button and enter the number of pins in the Number of pins text box.

   By default, the part generator creates a part with a number of pins equal to the number of input and output ports in the netlist file. However, if you are using a specific device for your FPGA/CPLD component, you may want to specify the number of pins on that device, if it differs from the number of netlist ports. This is especially true if you plan to use the part on a PCB schematic page.
7. If necessary, select the Vendor File Type for the netlist file from the drop-down list box.
8. If you specified a “raw” pin-out file in step 1, specify an implementation type, name, and file for the part.

   The most common implementation type used with the parts created from PLD vendor pin reports is either <none> or Project (which creates a hierarchy of projects for system simulation). Implementation types signify the following:

   - <none> Primitive library part.
   - EDIF Non-primitive library part. Contents defined by an EDIF netlist generated by a third-party EDA tool.
   - Project Primitive library part. Associated with the Simulation Resources of a programmable logic project for system-level simulation.
   - Schematic View Non-primitive library part. Contents defined by a schematic folder/page.
   - VHDL Non-primitive library part. Contents defined by a VHDL model.
   - Verilog Non-primitive library part. Contents defined by a Verilog model.

The table below illustrates typical combinations of vendor file type and implementation types.

Vendor file type	Implementation type
Actel Pin	[<none>|Project]
Altera Pin	[<none>|Project
AMD/MINC JEDEC	[<none>|Project]
APD BGA/Die-Text File	[<none>|Project]
EDIF Netlist	[EDIF|<none>|Project]
Lattice Pin	[<none>|Project]
Lucent Pad	[<none>|Project]
OrCAD SPLD Pad	[<none>|Project]
Verilog Netlist	[<none>|Project|Verilog]
VHDL Netlist	[<none>|Project|VHDL]
Xilinx M1 Pad	[<none>|Project]
Xilinx Pin	[<none>|Project]
XNF Netlist	[<none>|Project]

Note: You can also use the Actel Pin File format to create a part for your Atmel project by modifying the Atmel pin file.

9. Click *FPGA Setup* to open the FPGA Options dialog box.

   a. In the *General* tab, specify the settings for the symbol, pins, and pin swap.

   b. In the *Pin Defaults* tab, specify the default settings for pin direction and shape. Additionally, you can modify the pin-shape for low-asserted pins.

   c. Click *OK* to close the FPGA Options dialog box.

10. Click *OK*. Capture generates a library with the file partname.OLB and references it in the project manager's Outputs folder.

Note: Selecting *Create multi-section part* in the general tab

of FPGA Setup dialog box will open Split Part Section Input Spreadsheet when you close the Generate Part dialog box. You can use this spreadsheet to modify the part.

You can use the part you generate with the Generate Part command to represent the actual component (FPGA or CPLD) in schematics for other projects (including PCB designs). When you use the Generate Part command, Capture creates a part file (with a .OLB extension) and references it in the Outputs folder of the project manager.

Supported Vendor Pad and Pin file formats

Capture CIS supports the pad and pin file formats from the following vendors:

- **Actel Pin File**.

  For the following series:

  - 3200DX
  - ACT1
  - ACT2

- **Altera Pin File**.

  For the following series:

  - Quartus II
  - Maxplus II

- **Lattice Pin File**
- **Lucent ORCA Pad File**
- **Xilinx Pad and Pin Files**.

  For the following series:

  - Virtex
  - Spartan

13

Board-level simulation

This chapter covers:

- "Choosing an HDL for board simulation" on page 491
- "Starting NC VHDL or NC Verilog for board-level simulation" on page 492

Board-level simulation provides a method for you to simulate your entire PCB design (including any programmable logic devices created as FPGA projects in Capture) before migrating it to your board layout tool. You can create a test bench to provide stimulus and a design netlist for board-level simulation (only) with either VHDL or Verilog, by specifying one or the other in the Board Simulation tab of the Preferences dialog box.

Choosing an HDL for board simulation

You can use either VHDL or Verilog as the hardware development language for board simulation. When you simulate your PCB design, Capture creates a netlist, in the HDL that you specify, and uses it as the design source for the simulation.

Note: Be sure that, when you choose an HDL for board simulation, you choose an HDL that does not conflict with the elements of your design. That is, if your design includes Verilog components, you must choose Verilog as the board simulation HDL. Mixed Verilog/VHDL designs are not supported in this release of Capture.

To choose an HDL for board simulation

1. Choose the Preferences command from the Options menu. Capture displays the Preferences dialog box.
2. Select the Board Simulation tab.

3. Select either Verilog or VHDL as the hardware development language to be used for board simulation.

   Note: Be sure that, when you choose an HDL for board simulation, you choose an HDL that does not conflict with the elements of your design. That is, if your design includes Verilog components, you must choose Verilog as the board simulation HDL. Mixed Verilog/VHDL designs are not supported in this release of Capture.

4. Click OK.

Starting NC VHDL or NC Verilog for board-level simulation

NC VHDL and NC Verilog, collectively, comprise the NC Desktop simulation tool set that OrCAD provides. This tool set provides the means by which you can simulate your Capture design at the board level. For the specifics of working with the NC Desktop tools, please refer to your NC Desktop documentation.

Note: Be sure that, when you choose an HDL for board simulation (as describe in Choosing an HDL for board simulation), you choose an HDL that does not conflict with the elements of your design. That is, if your design includes Verilog components, you must choose Verilog as the board simulation HDL. Mixed Verilog/VHDL designs are not supported in this release of Capture.

Starting NC VHDL or NC Verilog for board-level simulation

1. Choose the Board simulation command from the Tools menu. Capture displays the NC Verilog Simulation dialog box or the NC VHDL Simulation dialog box, depending on the option you specified in the Board Simulation tab of the Preferences dialog box.

   Note: Be sure that, when you choose an HDL for board simulation (as describe in Choosing an HDL for board simulation), you choose an HDL that does not conflict with the elements of your design. That is, if your design includes Verilog components, you must choose Verilog as the board simulation HDL. Mixed Verilog/VHDL designs are not supported in this release of Capture.

2. Choose the Use Interactive option.

   or

   Choose the Specify batch file option, and enter the path to, and name of the batch file in the text box.

3. Click Setup. Capture displays the NC VHDL Simulation Setup dialog boxor the NC Verilog Simulation Setup dialog box, depending on the option you specified in the Board Simulation tab of the Preferences dialog box.

4. In the Simulation tab (NC Verilog), in the Options area, set the paths to, and names of, your HDL.VAR file and Log directory.

5. In the Flow options area, specify the particular options you want to run in the simulation session. These include:

   - Compile: Specify that the simulator compile your design for simulation. This is a prerequisite for actually performing the simulation. You can provide command line options for the compile in the Command Options text box, by entering them exactly as you would from the command line.
   - Elaborate: Specify that the simulator perform elaboration (the process of mapping your design to machine code that the simulator can interpret) on your design. This is a prerequisite for actually performing the simulation. You can provide command line options for the elaboration in the Command Options text box, by entering them exactly as you would from the command line.
   - Simulate: Run the simulation. You can provide command line options for the simulation in the Command Options text box, by entering them exactly as you would from the command line.

   Note: You need only compile and elaborate your design once. After that, when you start the simulator, you can skip the Compile and Elaborate steps, provided that the design has not changed since your last simulation run.

6. In the Sim Vision launch area, specify the particular options you want to run in the simulation session. These include:

   - Start Sim Vision: Causes the simulator to display its user interface in a new window on the screen. If you do not

choose this option, the simulator runs in the background using the command options you have specified for Compile, Elaborate, and Simulate. In effect, this is similar to running in batch mode, but rather than using a batch file, the simulator uses the options specified in the dialog box.

- Enter Interactive Mode: Causes the simulator to set simulation time to 0 and await your inputs in order to run the simulation. This option is only available if you have selected the Start Sim Vision option.

7. Choose the Testbench tab, and specify whether you want to generate a new testbench for your design, include an existing testbench, or not include a testbench in the current simulation session.

   Note: If you choose None (that is, if you specify that no testbench should be included), you cannot simulate your design, since testbenches provide the stimulus. In general, you should only choose None when you want to compile and/or elaborate your design without simulating it.

8. Choose the Model Compilation tab. The options available on this tab depend on the HDL you have selected for the simulation: VHDL or Verilog.

9. Complete the options on this dialog box as desired.

10. Click OK. Capture returns to the Preroute Simulation dialog box for VHDL or Verilog. This returns you to the NC VHDL Simulation Setup dialog boxor the NC Verilog Simulation Setup dialog box depending on the option you specified in the Board Simulation tab of the Preferences dialog box.

11. Click Run to start the simulation session.

14

Generating output

This chapter covers:

- “Annotating your design” on page 495
- “Generating reports” on page 512
- “Printing and plotting” on page 525
- “Generating netlists” on page 534
- “Generating library parts” on page 549

Capture is capable of producing a number of different reports that pertain to your design and includes full printing and plotting capabilities for schematics and parts.

Before you produce output from your design, you must annotate it so that each part or instance has a unique reference designator and to generate net names for all electrical connections in your design. After you have accomplished that (via annotation) you can run reports to check electronic design rules, designate gates, pins, or packages for swapping (in the board layout tool), print or plot, and create netlists.

Annotating your design

This section covers:

“Customizing part references in a design” on page 496

“Back annotating” on page 500

“Forward annotating schematic information” on page 502

“Designating pins, gates, or packages for swapping” on page 502

“Choosing the Annotate Sequence” on page 506

"Creating an update file" on page 508

"Creating a combined swap and update file" on page 510

By annotating your design (that is, by assigning reference designators and net names to unnamed parts and electrical connections in your design) you provide the means by which to pass it "downstream" to other layout design tools (PCB Editor, for example) that take it beyond the schematic capture phase of the design. Possible downstream applications include PCB layout tools, simulators, or logic optimizers.

Customizing part references in a design

You can customize the way Capture assigns part references in your design. You can specify a range of part reference values that Capture will use to annotate a schematic page or a hierarchical block in your design. Use the Annotate dialog box to complete this task.

Important

This functionality works independently from the existing annotation behavior of Capture.

Schematic page-wise and hierarchical block-wise annotation

In schematic page-wise annotation (recommended for flat design), you can set a part reference range for each schematic page that exists in the root schematic folder of your design. All schematic pages in the root schematic folder are displayed in a grid in the Annotate dialog box in the following format: *Schematic_Folder_Name:Schematic_Page_Name*.

In hierarchical block-wise annotation (recommended for hierarchical design), you can set a part reference range for each hierarchical block that exists in root schematic folder of your design. All hierarchical blocks in the root schematic folder are displayed in a grid in the Annotate dialog box in the following format: *Schematic_Folder_Name:Hierarchical_Block_Name*.

If you set the design for schematic page-wise or hierarchical block-wise annotation and also use the:

- Incremental reference update option, then all the part references in your design are updated incrementally within the specified part reference range. However, this does not affect the already annotated parts in your design.
- Unconditional reference update option, then all part references in your design are updated unconditionally from the start value specified in the part reference range.

Additionally, Capture will flash error and warning messages, if it encounters any invalid operation while using this functionality. For example, same part reference range for more than one schematic pages or hierarchical blocks in your design, parts in your design that are outside the specified part reference range.

To perform schematic page-wise or hierarchical block-wise annotation

1. In the project manager, select the design file, schematic folder, or a schematic page.

Note: Capture currently does not support specifying of part reference range for a portion of the design, for example, a specific schematic page or a schematic folder. You should specify a part reference range for all the schematic pages or hierarchical blocks in your design.

2. From the Tools menu, select the Annotate command. The Annotate dialog box appears.

Caution

To perform regular annotation, see "To uniquely identify parts" ***on page 183.***

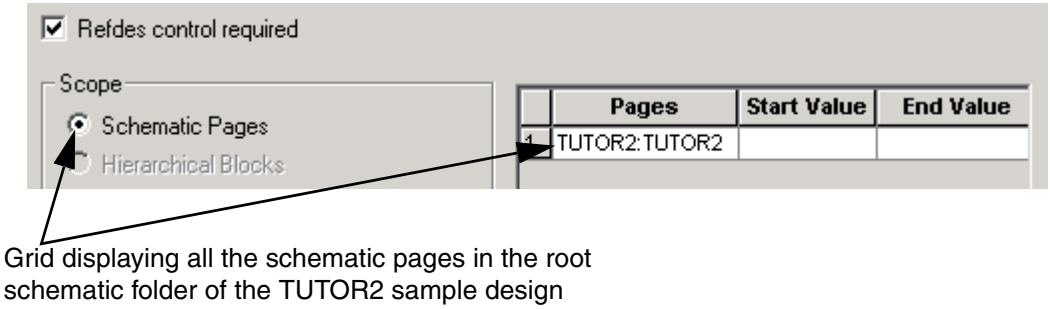
3. Select the *Refdes control required* check box, if you want to specify a part reference range for each schematic page or a hierarchical block in your design. The Scope options in the dialog box changes to Schematic Pages and Hierarchical Blocks. Also, a grid appears on the right-hand side of the dialog box displaying all the schematic pages or hierarchical blocks in the root schematic folder of your design depending on whether your design is a flat design or a hierarchical design (see figure: Annotate Dialog Box - Refdes control required).

Note: The Hierarchical Blocks option is not available, if there are no hierarchical blocks in the root schematic folder of your design.

The grid is divided into rows and columns. Each row has a number, a schematic page name or a hierarchical block name, and cells to specify Start and End values for the part reference range (see figure: Annotate Dialog Box - Refdes control required).

For example, the *TUTOR2.dsn* sample design, which is a flat design contains a schematic page defined at the root level of the design. When you select the Refdes control required check box, then the grid displays the following entry in the Pages column: *TUTOR2:TUTOR2*, where the first *TUTOR2* is the root schematic folder name and the second *TUTOR2* is the schematic page name (see figure: Annotate Dialog Box - Refdes control required).

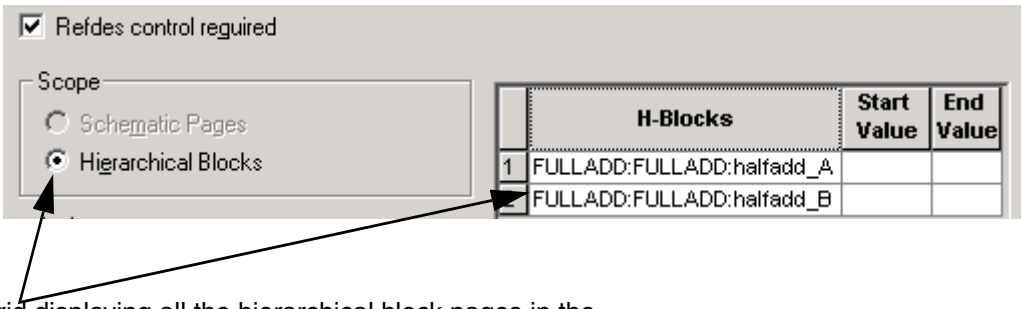
Figure 14-1 Annotate Dialog Box - Refdes control required



Grid displaying all the schematic pages in the root schematic folder of the TUTOR2 sample design

Let's take the example of a hierarchical design. The *FULLADD.DSN* sample design, which is a hierarchical design contains two hierarchical blocks defined at the root level of the design. When you select the Refdes control required check box, then the grid displays the following two entries in the H-Blocks column: *FULLADD:FULLADD:halfadd_A* and *FULLADD:FULLADD:halfadd_B*, where *FULLADD* is the root schematic folder name and *FULLADD:halfadd_A* and

FULLADD:halfadd_B are the reference to the root-level hierarchical blocks in the design (see figure).



Grid displaying all the hierarchical block pages in the root schematic folder of the FULLADD sample design

Note: The grid displays only the schematic pages or hierarchical blocks on the root schematic of the design.

4. Enter a numeric value greater than 0 in the Start Value and End Value columns corresponding to each schematic page name or the hierarchical block name.

Tip

Use the Tab key to move from the Start Value column to End Value column.

Tip

You can also use the Arrow keys to move around in the grid.

Tip

You can use the column handle ( ) to resize the rows and columns in the grid.

Tip

A valid range must have both the Start and End Values and the End Value must be greater than the Start Value.

5. Specify all other desired settings in the Annotation dialog box.

6. Click OK. Part references in each schematic page or hierarchical block get updated according to the range specified for each schematic page or hierarchical block in the Annotate dialog box.

Note: Capture saves the annotation preferences for the project when you click OK. These settings will be used whenever you open the project the next time.

Note: If you are using the Refdes control required option for a project, then the Auto reference placed part option in the Miscellaneous tab of the Preferences dialog box will not honor the range specified in the grid.

Note: If any changes are made to the root schematic of a design, then all the part reference range values specified in the grid for the design will be lost. However, this does not affect the already annotated parts in the design.

Back annotating

When you need to transfer packaging information to your schematic folder from other EDA tools, use the Back Annotate tool. When you need to back annotate properties, use the Update Properties tool (see To update part or net properties on page 197). Using Back Annotate, you can import changes created by external tools such as PCB layout packages. Capture uses a simple file format to provide support for gate swapping, for pin swapping, and for changing or adding properties on parts, pins, or nets. If the external tool creates a back annotation file, edit the file to match the format described in Creating a swap file.

You might use Back Annotate if, after you've completed your schematic design and while you are routing a printed circuit board, you discover that you could greatly reduce via count, track length, or routing complexity by exchanging two of the gates or pins on a part. You could then use your board layout application to rewire the board, exchanging the connections of U1A and U1B. To ensure that your schematic design reflects the changes, you use a text editor to create a swap file, then run the Back Annotate command. The next time you look at the design, you see that U1A and U1B have traded places.

To back annotate

Back annotating board file information to your schematic design is a matter of creating a report file and reading it back into Capture.

To back annotate schematic information

1. After you have made changes to the design in the layout tool, choose Reports from the File menu. The Generate Reports dialog box appears.
2. If you re-annotated the names of parts, or altered parts or nets, choose OrCAD Backannotation File (.SWP) to create a combined swap and update file. Click OK to create the report.
3. From the project manager's Tools menu, choose Back Annotate. The Backannotate dialog box appears.
4. Use the Browse button to find the file (.SWP) you created in step 2, then click OK. Capture updates the schematic design.

To back annotate part packaging information

1. Using a text editor, create a swap file. See Designating pins, gates, or packages for swapping for instructions.
2. In the project manager, select schematic folders or schematic pages if you want to process only a portion of the design. If you want to process the entire design, leave the schematic folders or schematic pages unselected.
3. From the Tools menu, choose Back Annotate. The Back Annotate dialog box appears. Select the tab (either PCB Editor or Layout) that is appropriate to your downstream PCB tool.
4. Verify that the dialog box options are set the way you want them. For example, the name and location for the netlist directory and the swap file.
5. Click OK.

Shortcut

Toolbar:

Forward annotating schematic information

If you make changes to your board design in Capture, you can bring those changes into PCB Editor. In addition, you must save your Capture design before you can create a netlist.

To forward annotating schematic information from Capture

Capture includes functionality with which you can forward annotate your schematic data such that it can be included in a PCB Editor board design.

1. Open the design for which you are going to create a netlist.
2. From the Tools menu, choose Create Netlist.
3. In the Create Netlist dialog box, choose the PCB Editor tab.
4. In the Input Board File box, enter a name for the input file using a .BRD file extension.
5. In the Output Board File box, enter a name for the output file using a .BRD file extension.
6. Click OK to close the Create Netlist dialog box and create the .BRD file.

Designating pins, gates, or packages for swapping

This section covers:

“Creating a swap file (.SWP)” on page 503

“CHANGEREF” on page 504

“GATESWAP” on page 504

“PINSWAP” on page 504

“CHANGEPIN” on page 505

When you need to transfer packaging information to your schematic folder from other EDA tools, use the Back Annotate tool. When you need to back annotate properties, use the Update Properties tool (see To update part or net properties). Using Back Annotate, you can

import changes created by external tools such as PCB layout packages. Capture uses a simple file format to provide support for gate swapping, for pin swapping, and for changing or adding properties on parts, pins, or nets. If the external tool creates a back annotation file, edit the file to match the format described inCreating a swap file (.SWP).

You might use Back Annotate if, after you've completed your schematic design and while you are routing a printed circuit board, you discover that you could greatly reduce via count, track length, or routing complexity by exchanging two of the gates or pins on a part. You could then use your board layout application to rewire the board, exchanging the connections of U1A and U1B. To ensure that your schematic design reflects the changes, you use a text editor to create a swap file, then run the Back Annotate command. The next time you look at the design, you see that U1A and U1B have traded places.

Creating a swap file (.SWP)

For PCB designs, a swap file is a text file containing old and new part references for use with the Back Annotate command. Swap files are typically created by another application, such as PCB Editor. You can also create a swap (.SWP) file using any text editor that saves files in ASCII format. The file can include comments; the Back Annotate tool ignores any text to the right of a semicolon.

In a swap file, each line (unless preceded by a semicolon) causes one action. The elements of each line may be separated with any number of space or tab characters. In general, the first element of the line specifies the type of swap. If no swap type is specified, CHANGEREF is assumed. The other swap types are GATESWAP and PINSWAP.

When you are creating a swap file, include only the changes from the present state of the design to the state you want it to have. For example, you might place a part as U1 in the design, and change it in a PCB layout package first to U2, then to U3. The swap file should reflect the change from U1 to U3; do not include the intermediate step involving U2.

For gate swaps, make sure that the gates being swapped are of the same type. If they are not, you may get incorrect results.

For pin swaps, an additional element—the part reference—must be specified before the old and new values, as shown in the following example. Pin swap is limited to pins of the same type and shape on the same part. For example, you can swap data pins on U5B, but you cannot swap a pin on U5C.

CHANGEREF

Changes the specified part's reference.

Examples

```
CHANGEREF U1 U2 ; Change part reference U1 to U2
CHANGEREF U1A U1B ; Change part reference U1A to U1B
U1C U2B ; Change part reference U1C to U2B
```

GATESWAP

Swaps the specified parts or packages. If U1 and U2 are multiple-part packages, then all the devices in U1 will change to U2, and vice versa—U1A, U1B, and U1C change to U2A, U2B, and U2C, respectively; U2A, U2B, and U2C change to U1A, U1B, and U1C, respectively.

Examples

```
GATESWAP U1 U2 ; Change part U1 to U2 and
  ; part U2 to U1
GATESWAP U1A U1B ; Swap gates A and B on U1
GATESWAP U1C U2B ; Swap gates U1C and U2B
```

Note: Back Annotate *does not* check part types before performing the specified swap. If you swap gates between parts of different types (as shown in the following example), you may see unwanted results in your design.

GATESWAP U1C U2B ; Swap gates U1C and U2B

PINSWAP

Swaps two pins on the specified part. Only pins of the same type and shape on the same part can be swapped. The pins are identified by name or number. Pin names must be enclosed in double quotation

marks. PINSWAP can be used multiple times on the same pins in a swap file.

Examples

```
PINSWAP U5B "D0" "D1" ; Swap the pins named D0 and D1 on U5B
PINSWAP U3 5 6 ; Swap pins 5 and 6 on U3
```

CHANGEPIN

Changes the first pin with the second pin. Only pins of the same type and shape on the same part can be swapped. The pins are identified by name or number. Pin names must be enclosed in double quotation marks. CHANGEPIN can only be used once on each pin in a swap file.

Examples

```
CHANGEPIN U5B "D0" "D1" ; Changes pin D0 to D1 on U5B
CHANGEPIN U3 5 6 ; Changes pin 5 to pin 6 on U3
```

To designate pins, gates, or packages for swapping

To specify that pins, gates, or packages in your PCB design are eligible for swapping (in order, to improve board routing) follow these steps.

1. Using a text editor, create a swap file. See Creating a swap file (.SWP) for instructions.
2. In the project manager, select schematic folders or schematic pages if you want to process only a portion of the design. If you want to process the entire design, leave the schematic folders or schematic pages unselected.
3. From the Tools menu, choose Back Annotate. The Back Annotate dialog box appears.
4. Verify that the dialog box options are set the way you want them. For example, you specify whether you want to process the entire design or only the selected schematic folders or schematic pages, and the name and location for the swap file.
5. Click OK.

Shortcut

Toolbar:

Example

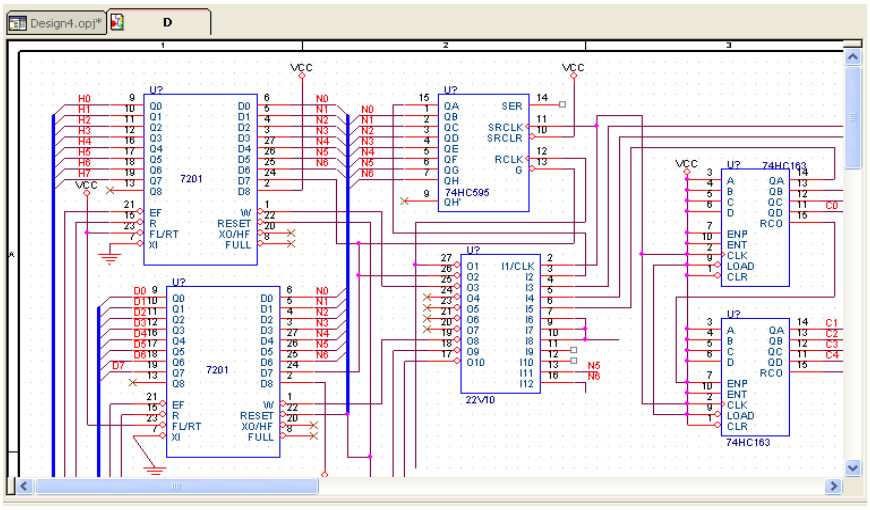
```
CHANGEREF U1 U2 ; Change part reference U1 to U2
CHANGEREF U1A U1B ; Change part reference U1A to U1B
  U1C U2B ; Change part reference U1C to U2B
GATESWAP U1 U2 ; Change part U1 to U2 and part U2 to U1
GATESWAP U1A U1B ; Swap gates U1A and U1B
PINSWAP U7 1 2 ; Swap pins 1 and 2 on U7
PINSWAP U5B "D0" "D1" ; Swap the pins named D0 and D1 on U5B
PINSWAP U3 5 6 ; Swap pins 5 and 6 on U3
```

Choosing the Annotate Sequence

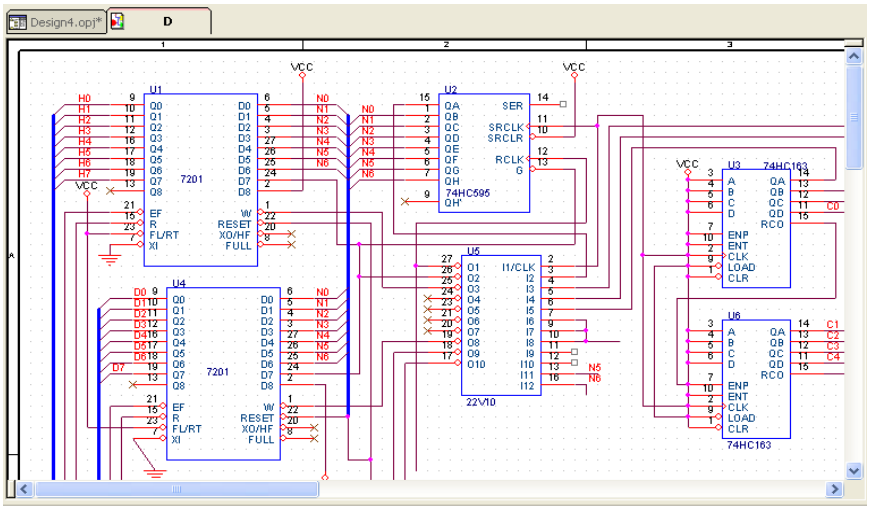
You can choose the sequence in which the components of your design are annotated.

The Annotation Sequence list contains three options that you can use to decide the sequence in which the objects on your design are annotated - Default, Left to Right & Top to Bottom.

To differentiate between the way these sequences work on a design, we will use the example of a dense design that contains a number of large components clustered together.

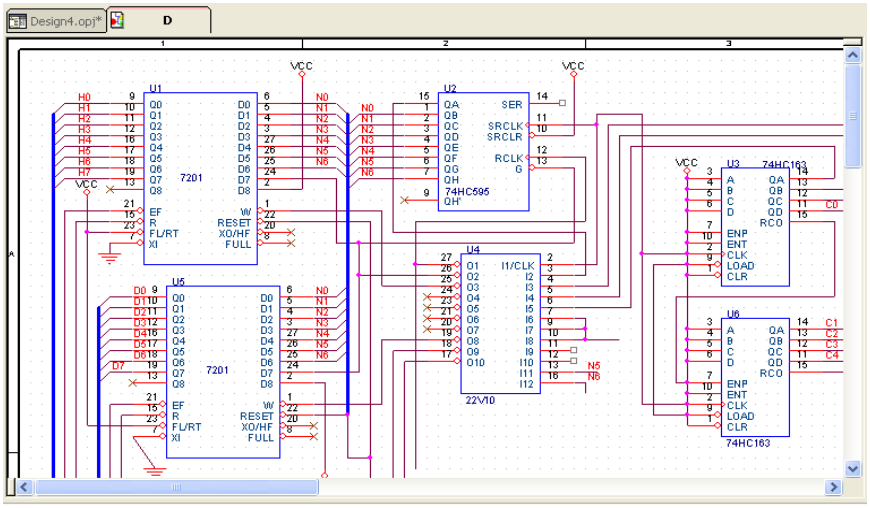


If we run the annotate command on this design using the Default option the results are as follows:



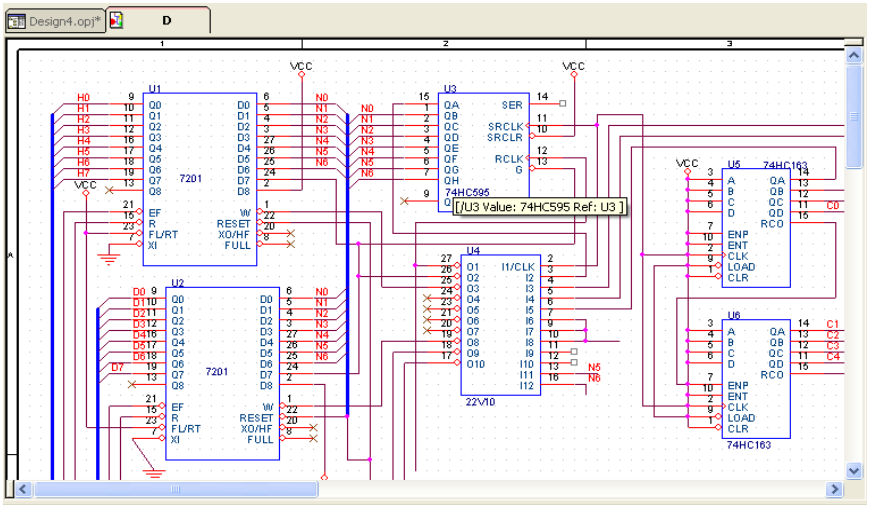
Notice the sequence of annotation of the components on the design.

Next, we will select the Left - Right option and annotate the design again.



The annotation procedure using this option scans the page grid from left to right one grid line at a time. Then moving downwards to the next grid line. In effect, the sequence is left to right and top to bottom.

We will now annotate the design using the Top - Bottom option.



In this case, the procedure scans the pages from top to bottom on grid line at a time. Then moving towards the left of the screen.

Creating an update file

The update file is used by the Update Properties tool to determine which objects to change, which of the objects' properties are affected, and what values those properties receive. You can create an update (.UPD) file using any text editor that saves files in ASCII format. The file can include comments; any text to the right of a semicolon is ignored by the Update Properties tool.

Strings in the update file (except for comments) must be enclosed in quotation marks and cannot exceed 124 characters. You can use spaces and tab characters to format the update file in rows and columns, as shown in the example below.

The first line of the update file is a header line. It starts with a combined property string that identifies which properties to compare. In the example, only the Net Name property is compared. The other strings on the first line specify which properties to update when a match is found. The rest of the file contains lines for each match string to be compared and the values to be recorded in the updated properties.

In the following example, the combined property string is {Net Name}. For every object whose Net Name property value matches one of the

strings in the first column, the object's Track Width, Net Spacing, and Routing Priority properties are updated with the corresponding values. For example, every object whose Net Name property is set to VCC will be updated as follows: the Track Width property is set to 0.04, the Net Spacing property to 0.035, and the Routing Priority property to 3.

Combined property strings

With many of the tools in Capture, such as Create Netlist and Annotate, you use combined property strings to convey information to the tool or to limit the tool's action.

A combined property string consists of one or more property names, enclosed in braces, and can also contain literal text. Capture combines the values of the named properties with any literal text to create a string. An example is:

{Value}{Reference}

where "Value" and "Reference" are property names. Using this combined property string and a part with a part value of 74LS32 and a part reference of U?A, Capture creates the string:

74LS32U?A

You can include spaces and other characters in the combined property string, as in this example:

Part: {Value} ({Reference})

Using this combined property string and the same part, Capture creates the string:

Part: 74LS32 (U?A)

Different tools use combined property strings in different ways. For example, Annotate uses one to compare parts—if one part's combined property string matches another part's combined property string, it packages the parts together.

Note: Bill of Materials and other commands on the Tools menu that generate an output file based on a combined property string may produce errors if you include extra curly braces.

Note: You can include tabs in combined property strings, so that the output file can be manipulated in a spreadsheet or database application. Tabs also help format report files, such as those created by the Bill of Materials command.
Wherever you want to have a tab in the output file, insert the characters \t (a backslash and a lowercase "t") in the combined property string.

Note: Do not use {GROUP} as a property name in combined property strings. This may cause problems while annotating your design for a PCB Editor tool, like Allegro PCB Editor. The GROUP property is used in PCB Editor for a specific purpose.

Example

```
"{Net Name}" "Track Width" "Net Spacing" "Routing Priority"
"VCC" "0.04" "0.035" "3" ; Any text to the right
"CLK" "0.01" "0.025" "1" ; of a semicolon is
"CLR" "0.01" "0.025" "3" ; ignored by the
"RESET" "0.01" "0.025" "3" ; Update Properties
"GND" "0.04" "0.035" "2" ; tool.
```

Note: Except for the header line, update files for Capture have the same format as the update files used by Update Field Contents in SDT. Once you add the appropriate header line, you can use an SDT update file without modification to change individual property values using Update Properties. You can also build on an SDT update file for a more elaborate property update, because Capture can update multiple properties in a single pass.

Do not create an empty string (two consecutive double quotation marks without intervening characters) in the header line. Update Properties reports an empty string as an error.

Creating a combined swap and update file

You can create a file that combines swap file and update file information. Run Back Annotate to use a combined swap and update file. Swap and update files should have the same .SWP file extension as normal swap files.

A swap and update file is divided into sections. Each section uses the following general form:

```
.label utility-name utility-parameters
section-information
```

```
.End
where:
```

label

Specifies the name of a section. A label can be any string combination of letters and numbers, but must always start with a dot (.).

utility-name

Specifies the utility Capture uses for the section. The acceptable utilities are: Flags, GateAndPinSwap, and UpdateProperties.

- **Flags** - The flags section marks the view of the design, and the design name and path.
- **GateAndPinSwap** - A section using this utility behaves the same as a Back Annotate file.
- **UpdateProperties** - A section using this utility behaves the same as an Update Properties file.

utility-parameters

Specifies the parameters of the utility for the section. All utility parameters only apply to the UpdateProperties utility.

- **Parts** - Specifies that only parts are updated. If both Parts and Nets are specified as parameters, Nets overrides Parts.
- **Nets** - Specifies that only nets are updated. If both Parts and Nets are specified as parameters, Nets overrides Parts.
- **OnlyStuffEmpties** - Specifies that only empty properties are updated. If a property already contains a value, then it is not modified. If this parameter is not specified, UpdateProperties unconditionally updates all properties.
- **UppercaseCombined** - Specifies that a case insensitive match is to be attempted when comparing the match string with the combined property string.

- **UppercaseStuffString** - Specifies that the update string will be changed to upper case before updating the property, but after string matching.

section-information

Specifies the actions the utility performs for the section. If the utility is GateAndPinSwap, these lines use the normal Gate and Pin Swap file format. If the utility is UpdateProperties, these lines use the normal Update Properties file format. If the utility is Flags, the section contains the following lines:

```
View = design-view
DesignName = path
```

where *design-view* is either Logical or Physical, and *path* specifies the design file name and path. In Capture Release 9 and later, the Logical design-view corresponds to instances, and Physical corresponds to occurrences.

Example

```
.Label1 Flags
  View = Physical
  DesignName = C:\ORCADWIN\CAPTURE\DESIGN\FULLADD.DSN
End
.Label2 GateAndPinSwap
  GateSwap R1 R2
  PinSwap R3 "1" "2"
  ChangeRef R4 R10
End
.Label3 UpdateProperties Parts
  "{Part Reference}" "Notes"
  "R10" "This used to be R4"
  "R3" "Notice pins 1 and 2 are swapped"
  "R1" "This used to be R2"
  "R2" "This used to be R1"
End
.Label4 UpdateProperties Nets
  "{Net Name}" "Trace Width"
  "VCC_WAVE" "0.040"
  "GND Power" "0.040"
End
```

Generating reports

This section covers:

"Creating an include file" on page 513

"Creating a bill of materials" on page 514

"Creating a cross reference report" on page 517

"Creating a placement report" on page 518

"Creating a Find result report" on page 519

"Browsing DRC markers" on page 524

Capture can generate many different reports necessary to the electronic design process.

Note: If you haven't specified a root for your design, you cannot generate reports.

Creating an include file

You can use an include file to have the Bill of Materials command add information that's not in the schematic folder to the final bill of materials. You can create an include (.INC) file using any text editor that saves files in ASCII format.

The first line of the include file is a header. The bill of materials is normally keyed to the part value, so the first line begins with a pair of single quotes with no spaces or other characters between them. The rest of the first line contains any information you want to include to make the file and the bill of materials more readable—this usually consists of headers for the values in the rest of the file.

The rest of the file contains a separate line for each part. Each line must begin with the property value (as specified in the Combined property string text box within the Include File group box in the Bill of Materials dialog box) enclosed in single quotes. Following the property value (and on the same line) is the information that you want added to the bill of materials. You can separate the part value from additional information by inserting any number of spaces or tab characters—Capture will align the first non-blank character in each line when it creates the bill of materials report.

You must separate the items in the Combined property string text box in the Bill of Materials dialog box exactly as they are separated in the

include file. For example, if you use a space to separate the part values, descriptions, and part orders, then the combined property string should look like this:

{Value}

Note: Note that screws, washers, and other hardware appear in a bill of materials, but not in a netlist. Netlists include only objects with pins.

Example

```
''     DESCRIPTION             PART ORDER CODE
'1K'   Resistor 1/4 Watt 5%    10000111003
'4.7K' Resistor 1/4 Watt 5%    10000114703
'22K'  Resistor 1/4 Watt 5%    10000112204
'1uF'  Capacitor Ceramic Disk  10000211006
'.1uF' Capacitor Ceramic Disk  10000211007
```

Note: Include files for Capture have the same format as the include files used by Create Bill of Materials in OrCAD's SDT 386+. You can use an SDT 386+ include file without modification to create a bill of materials in Capture.

Creating a bill of materials

A bill of materials is a composite list of all the elements you need for your PCB design. Using the Bill of Materials command, you can create a standard tab-delimited part list, or you can create a custom bill of materials showing properties that you specify. With either of these formats, you can add information about any part by merging an include file with your bill of materials. A standard bill of materials includes the item, quantity, part reference, and part value.

Capture automatically elects to use either instances or occurrences for generating reports, depending upon your type of design. In general, you should use instances for FPGA and PSpice projects, and use occurrences for PCB and Schematic projects.

To create a bill of materials

You can create non-electrical parts—such as screws, washers, and sockets—that will appear in a bill of materials report but not in a netlist because the non-electrical parts don't have pins. Any part without pins is considered non-electrical.

You can specify any header information you want. The header of a bill of materials usually contains information such as the design name, date, document number, revision code, report name, page number, and the time the report is created. If the Header text box contains only a single space character, the header is left blank.

Note: Bill of Materials and other commands on the Tools menu that generate an output file based on a combined property string may produce errors if you include extra curly braces {}.

Note: Capture report files are text files, and can be opened in any text editor. You may want to use the tab alignment capability of your word processor to line reports up correctly. Spreadsheets will automatically align the columns of Capture-generated report files.

1. In the project manager, select schematic folders or schematic pages if you want to process only a portion of the design. If you want to process the entire design, leave the schematic folders or schematic pages unselected.
2. From the Tools menu, choose the Bill of Materials command. The Bill of Materials dialog box appears.
3. Verify that the dialog box options are set the way you want them. For example, you specify whether you want to process the entire design or only the selected schematic folders or schematic pages, and the name and location for the report file. (If you want to customize the information contained in the bill of materials report, see To create a custom bill of materials below.)
4. Click OK.

To merge information from an external database

1. Create an include file (see Creating an include file for instructions).
2. Perform the steps in To create a bill of materials above and set these additional options in the Bill of Materials dialog box.
   - ❑ Select the Merge an include file with report option.
   - ❑ Specify a combined property string.
   - ❑ Specify the path and name of the include file.

To create a custom bill of materials

1. Perform the steps in *To create a bill of materials* above and set these additional options in the Bill of Materials dialog box:
   - In the Header text box, enter the column headings you want in the report. If you leave the Header text box blank, there are no column headings in the report.
   - In the Combined property string text box, enter the names of the properties you want in the report. If you want the property values separated by literals, include the literals in the text box. See Defining properties for more information.

Shortcut

Toolbar:

Example

Note: The Bill of Materials command generates report files with .BOM extensions.

1 Bit Full Adder Hierarchy (COMPLEX) Revised: March 31, 1999 OrCAD

Bill Of Materials March 31, 1995 16:50:31 Page 1

Item	Quantity	Reference	Part
1	1	U1	74LS32
2	3	U2	74LS08
		U2	74LS08
		U2	74LS08
3	2	U3	74LS04
		U3	74LS04

To import the bill of materials in Microsoft Excel

1. Select the Open in Excel check box.

2. Click OK.

   The bill of materials is displayed in the Microsoft Excel spreadsheet.

Creating a cross reference report

The Cross Reference tool creates a report, indexed by schematic page, of all parts with their part references, part names and libraries. You may specify that the report also list the unused parts in multiple-part packages and the coordinates of all parts.

Capture automatically selects to use either instances or occurrences for generating reports depending upon the type of design your working with. In general, you should use instances for FPGA and PSpice projects, and use occurrences for PCB and Schematic projects.

To create a cross reference report

1. In the project manager, select schematic folders or schematic pages if you want to process only a portion of the design. If you want to process the entire design, leave the schematic folders or schematic pages unselected.
2. From the Tools menu, choose the Cross Reference command. The Cross Reference Parts dialog box appears.
3. Verify that the dialog box options are set the way you want them. For example, you specify, among other things, whether you want to process the entire design or only the selected schematic folders or schematic pages, whether the parts are sorted by part value or by part reference, and the name and location for the report file.
4. Click OK.

Note: Capture report files are text files and can be opened in any text editor. You may want to use the tab alignment capability of your word processor to line reports up correctly. Spreadsheets will automatically align the columns of Capture-generated report files.

Note: The path listed in the Library column of the Cross Reference report represents where the part placed was found when it was

originally placed. If you change machines, move or delete the library, or rename the part, the information in the report won't correspond to the current path and file name.

Shortcut

Toolbar:

Example

Note: The Cross Reference command generates report files with .XRF or .CSV extensions.

```
1 Bit Full Adder Hierarchy (COMPLEX) Revised: March 31, 1995
OrCAD
Design Name: C:\CAPTURE\DESIGN\FULLADD.DSN
Cross Reference March 31, 1995 16:15:54 Page 1
```

Item	Part	Reference	SchematicName	Sheet	Library
1	74LS04	U3A	HALFADD	1	C:\WINDOWS\TEMP\TTL.OLB
2	74LS04	U3B	HALFADD	1	C:\WINDOWS\TEMP\TTL.OLB
3	74LS08	U2A	HALFADD	1	C:\WINDOWS\TEMP\TTL.OLB
4	74LS08	U2B	HALFADD	1	C:\WINDOWS\TEMP\TTL.OLB
5	74LS08	U2C	HALFADD	1	C:\WINDOWS\TEMP\TTL.OLB
6	74LS32	U1B	HALFADD	1	C:\WINDOWS\TEMP\TTL.OLB

Creating a placement report

You can generate a report of the X and Y locations of the placements of the parts on a schematic.

This report, generated as a .CSV file, provides the following details of the parts:

- the reference designator
- the part name
- the schematic name

- the sheet number
- the file system location of the part library
- the X co-ordinate location
- the Y co-ordinate location

To Create a Placement report

1. You can create this report at any level of a design hierarchy: design, folder or page. So you need to select the appropriate level of the hierarchy in the part manager.
2. Right-click on the Project manager.
3. Point to the Reports item in the pop-up menu and choose the Export Placement item.

   The Placements.csv file is created at the same file system location as the current design and simultaneously opened for viewing.

Note: While the report is generated at any level of the design hierarchy, you can also multi-select parts of the hierarchy to generate the report. For example, you can select multiple pages to generate a placement report of only the parts on the selected pages.

Creating a Find result report

You can create a report for the results of the Find command. This report can be output in either CSV or HTML format.

Also, when you run the Find command to search for different types of objects, the search results appear in different types of the Find window. In this case, you can export the data from each tab.

To create a Find result report

1. Execute the Find command.
2. Right-click on any line item in the Find window.
3. From the pop-up menu, choose, Save as HTML or Save as CSV.

   A pop-up dialog displays the file system location of the report.

4. Click OK to close the dialog.

Note: The report does not open when you run the command. You need to go to the specified location and open the report in the associated application.

Running DRC ERC

The Design Rules Check tool scans schematic folders to verify that a design conforms to design rules; it generates a report of error and warning messages and places markers on the schematic page to help you locate problems. You can specify the conditions that cause error or warning messages. The Design Rules Check tool is ideal for catching problems such as bus contention or shorted power pins before you run simulation or synthesis tools.

Optional checks performed by Design Rules Check include off-grid parts; connected aliases, hierarchical ports and off-page connectors; unconnected wires, pins, ports, and off-page connectors; identical part references; type mismatch parts; and constructs that are not portable to SDT.

Note: Generally, you should run Design Rules Check to verify your design before you generate a netlist. This allows for more efficient netlist creation, and you can concentrate on netlist-specific problems if they should occur during the Create Netlist process. Design Rules Check warns you if certain conditions exist in your design. The severity of the specific problem may prevent completion of the design. Other conditions are subject to your judgment, and may be of no consequence. Once you are satisfied with the results of design tests such as Design Rules Check, proceed with the creation of a netlist.

When you run the Design Rules Check tool, any errors are marked on your schematic pages. Warnings are also marked if you select the option to Create DRC markers for warnings. You can display a list of the markers in the browse window, and you can search for specific errors or warnings.

Each time you run the Design Rules Check tool, any existing markers are removed. This means that you are always looking at the latest results. You can remove all markers from your schematic pages by running Design Rules Check and selecting the option to Delete existing DRC markers.

When you run the Design Rules Check tool, Capture creates a report (.DRC) of warning and error messages. You can view the report in a text editor. These messages also appear in the session log.

In addition to the report, the Design Rules Check tool places error markers on the schematic pages, and places warning markers if you select the Create DRC markers for warnings option in the dialog box.

To setup and run the design rules check

The Design Rules Check tool scans schematic folders to verify that a design conforms to design rules; it generates a report of error and warning messages and places markers on the schematic page to help you locate problems.

1. In the project manager, select schematic folders or schematic pages if you want to process only a portion of the design. If you want to process the entire design, leave the schematic folders or schematic pages unselected.
2. From the Tools menu, choose the Design Rules Check command. The Design Rules Check dialog box appears, open to the Design Rules Check tab.
3. Verify that the Check design rules option is selected, and that the rest of the dialog box options are set the way you want them. For example, you specify whether you want to process the entire design or only the selected schematic folders or schematic pages, what is to be included in the report, and a path and name for the report file. You also choose if you want to check for electrical and / or physical design rules.
4. Choose the Electrical Rules tab. This tab provides the options for the different electrical rules that you can test on your design. It also provides options for the reports that you can view.
5. Choose the Physical Rules tab. This tab provides the options for the different physical rules that you can test on your design. It also provides options for the reports that you can view.
6. Choose the ERC Matrix tab. Each cell in the matrix refers to an electrical connection between the signal types that intersect in the cell. If a cell contains a "W," Design Rules Check generates a warning message when it encounters the specified connection. An "E" in a cell tells Design Rules Check to generate an error

message. If you leave a cell empty, Design Rules Check issues no warnings.

7. Change the settings in the matrix as necessary by placing your pointer over a cell and clicking the left mouse button to change from "W" to "E" to empty and back to "W." An error marks a condition that must be fixed, while a warning marks a condition that may or may not be acceptable in your design.

8. Click OK.

Note: If you run a Design Rules Check on a single schematic page, Capture checks all pages in the entire schematic folder —not just the page you have selected— which ensures that all nets on the schematic page are valid.

If you select the Check hierarchical port connections option, Capture also checks the attached schematic folders.

Note: Capture report files are text files and can be opened in any text editor. You may want to use the tab alignment capability of your word processor to line reports up correctly. Spreadsheets will automatically align the columns of Capture-generated report files.

Shortcut

Toolbar:

Example

Note: The Design Rules Check command generates report files with .DRC extensions.

```
Design Rules Check

---------------------------------------
Checking Schematic: FULLADD
---------------------------------------
Checking Electrical Rules
ERROR: [DRC0004] Possible pin type conflict halfadd_A,SUM
Output Connected to Bidirectional Port

Checking for Unconnected Wires

Checking Pin to Port Connections
WARNING: [DRC0013] Port has no matching pin in part instance
above Z
WARNING: [DRC0013] Port has no matching pin in part instance
above Z

Checking for Duplicate References
```

```
Checking for Compatibility with SDT

Reporting Ports
  X
  Y
  CARRY_IN
  CARRY_OUT
  SUM

Reporting Globals
  VCC
  GND

Reporting Net Names
  N00032
  N00030
  N00028
  Y
  X
  SUM
  CARRY_IN
  GND
  VCC
  CARRY_OUT

---------------------------------------
Checking Schematic: HALFADD
---------------------------------------
Checking Electrical Rules
ERROR: [DRC0004] Possible pin type conflict U2A,O Output
Connected to Input Port
WARNING: [DRC0005] Unconnected pin U2A,I1

Checking for Unconnected Wires
WARNING: [DRC0007] Net has no driving source N00041
WARNING: [DRC0006] Net has fewer than two connections N00041

Checking Pin to Port Connections

Checking for Duplicate References
WARNING: [DRC10] Duplicate reference U2A

Checking for Compatibility with SDT
ERROR: [DRC0025] The comment graphic is not a single dashed
line I00042
ERROR: [DRC0025] The comment graphic is not a single dashed
line I00052

Reporting Ports
  X
  Y
  Z
  CARRY
  SUM

Reporting Globals
  VCC
  GND

Reporting Net Names
  Z
  N00067
  X
  N00041
  N00035
  X_BAR
```

```
Y
CARRY
SUM
N00007
GND
VCC
```

Browsing DRC markers

When you run the Design Rules Check tool, any errors are marked on your schematic pages. Warnings are also marked if you select the option to Create DRC markers for warnings. You can display a list of the markers in the browse window, and you can search for specific errors or warnings.

Each time you run the Design Rules Check tool, any existing markers are removed. This means that you are always looking at the latest results. You can remove all markers from your schematic pages by running Design Rules Check and selecting the option to Delete existing DRC markers.

When you run the Design Rules Check tool, Capture creates a report (.DRC) of warning and error messages. You can view the report in a text editor. These messages also appear in the session log.

In addition to the report, the Design Rules Check tool places error markers on the schematic pages, and places warning markers if you select the Create DRC markers for warnings option in the dialog box.

To browse DRC markers

1. In the project manager, select the schematic folder or schematic page you wish to browse.
2. From the Edit menu, choose the Browse command, then choose the DRC Markers command. A list of DRC markers appears in the browse window.
3. Double-click on any item in the list. The schematic page editor opens with the marker displayed and highlighted.

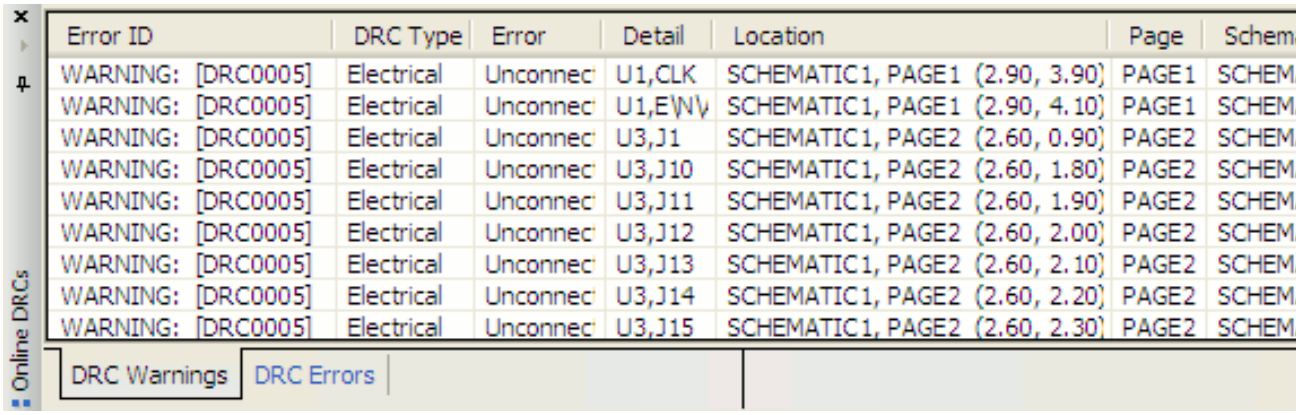
Check and Save

After you run the design rule check at least once on a design, you can then use the Check and Save command. This command executes the Design Rules Check on the current set of design rules that you define in the Design Rules Check dialog box.

To run the Check and Save command

1. Click the File menu.
2. Choose the Check and Save option.

   The Online DRCs window displays two tabs with the listings of the DRC errors and warning generated from the DRC check.



3. Double-click on a error or warning in the listings to go to the DRC marker on the specific schematic page.

Note: You need To setup and run the design rules check at least once before using the Check and Save command.

Printing and plotting

This section covers:

"Setting up a printer or plotter" on page 526

"Setting print options for objects on the schematic page" on page 527

"Printing documents" on page 528

"Printing or plotting a schematic page" on page 529

"Previewing print output" on page 531

"Printing or plotting a part" on page 532

"Scaling a print or plot" on page 533

Whether you wish to send output to a printer, a plotter, or an encapsulated PostScript file, you work with the standard Windows dialog boxes. Capture can send output to any driver that Windows supports.

In the Print dialog box, you make choices for a print job. The choices you establish are used for previewing and for creating output. Each time you open the Print dialog box to request a print job, all choices will be reset to the default settings.

For additional information on printing and plotting, see your Windows documentation.

Note: At certain zoom scales, Capture substitutes filled rectangles for text that is too small to appear. These placeholders are for display only—the text prints correctly.

To print or plot

1. Open the schematic page, part, or symbol you wish to print.
2. From the File menu, choose the Print command.

Setting up a printer or plotter

This section also covers:

"Special considerations for plotters" on page 527

"Plotter pen colors" on page 527

There are some considerations you should take into account when printing or plotting from Capture.

Special considerations for plotters

Plotters do not support bitmaps directly. If you are sending Capture output to a plotter, your bitmaps will not be plotted.

The Capture setup command may not give you access to all your plotter's setup options. For access to additional printer settings, use the Printers icon in the Windows Control Panel.

Many plotters do not have drivers that ship with Windows. If you do not see the plotter you are looking for in the list of available drivers, contact your plotter manufacturer and ask for a Windows driver. If your plotter will emulate HPGL, an alternative solution is to use the HPGL driver.

Plotter pen colors

The plotter driver maps your color choice to the closest available pen color as established in your plotter driver configuration. See your plotter's driver setup and documentation for more details. For access to additional printer settings, use the Printers icon in the Windows Control Panel.

To set up a printer or plotter

1. From the Print dialog box, choose the Setup button to select a different printer or plotter or to change printer settings.
2. If you need to set up your printer or plotter, see the documentation that accompanies the printer or plotter. For access to additional printer settings, use the Printers setting on the Start menu.

Setting print options for objects on the schematic page

You can specify various options for determining how specific objects on the schematic page are printed.

To define if an object is printed or plotted

1. From the Options menu, point to Preferences, then choose the Colors/Print tab.

2. Select the check box located beside the color block for the object that you want to be able to print or plot. Clear the check box if the object is not to be printed or plotted.

Note: Objects are always displayed on your screen, regardless of the setting of their check boxes.

Printing documents

Documents can be printed as indicated in the following table:

Document to print	From project mgr.	From schematic page editor	From part editor	From text window
Single schematic page	Yes	Yes	---	---
Multiple schematic pages	Yes	---	---	---
Entire schematic folder	Yes	---	---	---
Single part or symbol	Yes	---	Yes	---
Multiple parts and symbols	Yes	---	Yes (a)	---
Entire package	Yes	---	Yes (b)	---
Text	Yes (c)	---	---	Yes

Notes

(a) Multiple-part package in package view, only.

(b) In package view.

(c) Not including the session log.

To print multiple documents

1. In the project manager, select the documents you wish to print by holding down CTRL and clicking on the name with the left mouse button.
2. From the File menu, choose the Print command.
3. Choose either to print the highlighted text or the entire document.
4. Click OK to begin. The "Printing" message appears. Capture prints the window.

Note: When printing a multi-page schematic, make sure that the pages do not have multiple Title Blocks with different page numbers. Otherwise, the pages will not be printed in the correct order. If you change the page numbers in the Title Blocks manually, then make sure that the Do not change the page number checkbox is checked in the Annotate dialog box.

To print from a text editor window

1. Open the text editor window from which you wish to print.
2. From the File menu, choose the Print command.
3. Choose either to print the highlighted text or the entire document.
4. Click OK to begin. The "Printing" message appears. Capture prints the window.

Shortcut

Toolbar:

Printing or plotting a schematic page

With the schematic page editor active and open to a specific schematic page, you can create a print or a plot of that page. You can also print a page from the project manager.

Windows normally sets the printer to Portrait mode. You can use the Print Preview command to check output before sending it to the printer or plotter.

Behavior of offsets in printing and plotting

Your entire schematic page will be output to the printing or plotting device, regardless of the use of offsets. The following rules define the number of output pages that will be printed or plotted:

- The device and its driver determine the dimensions of the printed page area.
- The number of pages is calculated from the physical dimensions of the schematic page and the driver-provided area dimensions.
- A positive offset shifts the entire schematic page to the right in the X direction, and down in the Y direction. Additional pages are output as necessary so the entire schematic is printed. No truncation takes place.
- A negative offset shifts the schematic page left, and up. The effect of a negative offset will be to start the drawing on a “previous” page. Previous pages are “prepended” so drawing can start at the starting portion of the schematic. No truncation takes place.

Only the number of pages required to print or plot the schematic page will be printed. Extra “blank” pages are omitted.

Note: When printing a multi-page schematic, make sure that the pages do not have multiple Title Blocks with different page numbers. Otherwise, the pages will not be printed in the correct order. If you change the page numbers in the Title Blocks manually, then make sure that the Do not change the page number checkbox is checked in the Annotate dialog box.

To print or plot one page

➤ If you are working in the schematic page editor, open the window for the page you wish to print.

or

1. If you are working in the project manager window, then select the schematic page.
2. From the File menu, choose the Print command. The Print dialog box opens.
3. Select the scale, the print quality, and the number of copies, then click OK.

Shortcut

Toolbar:

Previewing print output

Using the Print Preview command, you can make sure that your schematic folder or schematic page is complete and that its appearance is what you want before you commit it to paper.

To preview print output

1. In the project manager window, select the documents you wish to print or plot.

   or

   Select the entire design or library you wish to print or plot.

   or

   Open the single part or schematic page you wish to print or plot.
2. From the File menu, choose Print Preview. The Print dialog box appears.
3. Edit the values as necessary.
4. Click OK to begin. The "Printing Now" message appears and after a moment, the Print Preview window opens. If the document requires multiple printer pages, scroll through them using the scroll bar.
5. Use the Previous page and Next page buttons to look at additional printer pages of the document.

6. To zoom in, move the magnifier pointer to a specific area and click the left mouse button.
7. When you finish, choose the Close button to dismiss the Print Preview window.

Be prepared to wait if you attempt to print multiple pages or parts. Depending on the number and size of the pages or parts you are previewing, Capture may require extra time to display the selection.

To preview print output from a text editor window

1. Open the text editor window you wish to print or plot.
2. From the File menu, choose the Print Preview command. The window displays the Print Preview and Print Setup dialog boxes.
3. Use the window's vertical scroll bars to view the other pages, if the document extends beyond one page.
4. When you finish, choose Print Preview from the File menu to return the text editor window to its normal editing state.

Printing or plotting a part

With the part editor active and open to a specific part, you can create a print or a plot of that part. You can also print a part from the project manager.

To print or plot a part

1. Select the part in the project manager window.

   or

   Open the part you wish to print.
2. From the File menu, choose the Print command. The Print dialog box opens.

3. Select the scale, the print quality, and the number of copies, then click OK.

To print or plot a multiple-part package

1. Select the part in the project manager window.

   or

   Open the part, and from the View menu choose the Package command.

2. From the File menu, choose the Print command. The Print dialog box opens.
3. Select the scale, the print quality, and the number of copies, then click OK.

Shortcut

Toolbar:

Scaling a print or plot

You can manually scale or have Capture automatically scale prints and plots to fit the paper size you choose.

Behavior of offsets in printing and plotting

Your entire Schematic Page will be output to the printing or plotting device, regardless of the use of offsets. The following rules define the number of output pages that will be printed or plotted:

The device and its driver determine the dimensions of the printed page area.

The number of pages is calculated from the physical dimensions of the schematic page and the driver-provided area dimensions.

A positive offset shifts the entire schematic page to the right in the X direction, and down in the Y direction. Additional pages are output as necessary so the entire schematic is printed. No truncation takes place.

A negative offset shifts the schematic page left, and up. The effect of a negative offset will be to start the drawing on a “previous” page. Previous pages are “prepended” so drawing can start at the starting portion of the schematic. No truncation takes place.

Only the number of pages required to print or plot the schematic page will be printed. Extra “blank” pages are omitted.

To scale a print or a plot of a schematic page or part

1. From the File menu, choose Print. The Print dialog box appears.
2. Select one of the three radio buttons in the Scale box.
   - The Auto scale option scales each schematic page to fit a single sheet of paper.
   - The Scale to page size option scales your schematic pages to the page size you select in the Scale to size box. This will result in multiple sheets of paper if you select a sheet size larger than your printer paper.
   - The Scale by factor option scales your schematic pages to a factor of your choice. The acceptance range of factors is 0.100 to 10.000.
3. If you select the Scale to sheet size option above, the Scale to size list becomes available. Your schematic page is scaled to the sheet size you select. This will result in multiple sheets of paper if you select a sheet size larger than your printer paper.
4. Click OK to send the image to the output device.

Shortcut

Toolbar:

Generating netlists

This section covers:

“Creating a netlist” on page 540

“Creating a flat netlist” on page 540

"Creating a hierarchical netlist" on page 541

"Customizing the hierarchical netlist" on page 542

"Creating subcircuit netlists" on page 543

"Specifying an alternate netlist template" on page 545

"Using SUBPARAM" on page 545

Generating netlists generally occurs after you place parts, update part references, and check for design rule violations. You can choose from more than 30 industry-recognized netlist formats. Your choice of netlist format is determined by the application that you intend to use.

The EDIF 2 0 0, VHDL, PSpice and Verilog netlist formats generate true hierarchical netlists. When a design is netlisted with one of these formats, the instance property values on nets and parts are used. All other netlist formats in Capture produce flat netlists, and use occurrence property values.

If you have translated a design with multiple schematic folders, use Annotate (and check for duplicate references) before netlisting.

Note: Generally, you should run Design Rules Check to verify your design before you generate a netlist. This allows for more efficient netlist creation, and you can concentrate on netlist-specific problems if they should occur during the Create Netlist process. Design Rules Check warns you if certain conditions exist in your design. The severity of the specific problem may prevent completion of the design. Other conditions are subject to your judgment, and may be of no consequence. If you are satisfied with the results of design tests such as Design Rules Check, then proceed with the creation of a netlist.

Note: Design Rules Check uses the decision matrix located in the ERC Matrix tab located in the Design Rules Check dialog box. It also uses a set of pre-determined rules, which are part of the executable code.

Note: Use Design Rules Check as a guide to verify the integrity of your design. It is only a guide. It is possible to generate a valid netlist even if Design Rules Check reports errors.

Note: The value, if any, you create for the PCB footprint depends on the particular netlist format you want to produce. Different

applications require netlists with different types of PCB footprints. If you do not specify this property, the PCB footprint will be set to the part value.

Netname resolution

When you are creating schematic pages, you can assign a variety of aliases to signals that are ultimately connected, but the netlist needs exactly one name for each net.
If Create Netlist encounters multiple names for a single net, higher priority aliases override lower priority aliases. Priority is determined by the source of the name, ranked as follows:

Lowest:	System-generated names Aliases Power object names Off-page connectors Hierarchical port names
Highest:	Named nets

Any remaining conflicts among netnames are resolved according to the following rules:

- The netname closest to the "root" of the project takes precedence over those further away.
- If the net is a bus, the net alias assigned to the greatest number of bus members has highest priority.
- Among netnames of equal precedence, priority follows alphabetical order.

As you can see, a net may change names several times as Create Netlist works. For example, the net may start with an alias of Battery on one page, be renamed ToBattery from an off-page connector, change again to become DC as a port is encountered, and finally change to BatteryBackup when Create Netlist finds a named net closer to the root schematic folder. Once the netlist is created, you can select any piece of the net anywhere in the design and see the net's name as it is recorded in the netlist (BatteryBackup), not as it appears at that particular location.

Combined property strings

A combined property string consists of one or more property names, enclosed in braces, and can also contain literal text. Capture combines the values of the named properties with any literal text to create a string. An example is:

{Value}{Reference}

where "Value" and "Reference" are property names. Using this combined property string and a part with a part value of 74LS32 and a part reference of U?A, Capture creates the string:

74LS32U?A

You can include spaces and other characters in the combined property string, as in this example:

Part: {Value} ({Reference})

Using this combined property string and the same part, Capture creates the string:

Part: 74LS32 (U?A)

PACK_SHORT Property

Capture includes a PACK_SHORT property that lets you map one logical pins to two or more physical pins. Take the example of an SMA connector. It has one signal pin and 4 shielding pins connected to Ground. The standard Capture symbol has only one visible Ground pin. So what is required is to short all 4 GND pins in the Allegro netlist with the net which is connected to the visible GND pin.

To do this, you can either add the other three Ground pins as NC or with a different netname depending on whether they have been added as invisible or visible with zero stub length.

Alternatively, you can use the PACK_SHORT property in Capture to hide the PACK_SHORT pins or make them visible with zero length pin stub.

Using this property, multiple groups of pins, each group having two or more pins, can be shorted.

Syntax:

```
PACK_SHORT=(<group1>)(<group2>)[<group3>]
```

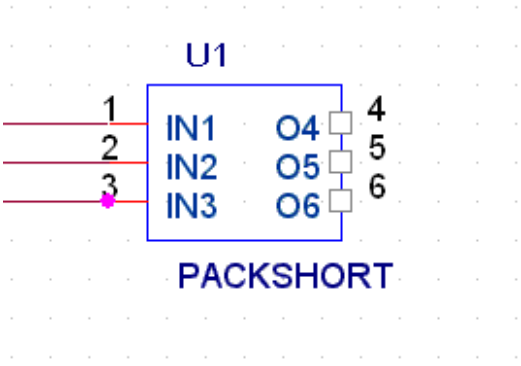
Where: <group> indicates (logicPin1, logicPin2 ... [logicPinN])

Example

Consider the assignment, PACK_SHORT = (A1, B1, Y1) (A2, B2) shorts together. The nets attached to logic pins A1, B1, and Y1 are shorted with each other and the nets attached to pins A2 and B2 are shorted with each other.

The PACK_SHORT property is implemented so you can either hide the pins to be shorted by checking the ignore checkbox in Package Properties dialog box or you can make them zero length pins and show them as unconnected as illustrated.below.

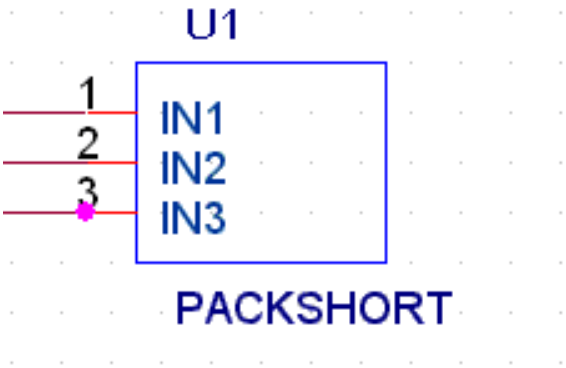
Method 1:



The above part has O4, O5 and O6 added as PACK_SHORT pins (IN1,O4,O5,O6) which will inherit the pin IN1 net set as zero-length but their stub will still be visible. If you instantiate the this part and generate an Allegro netlist, IN1, O4, O5 and O6 will inherit the same net.

If IN1 is left unconnected, all PACK_SHORT pins will be marked as NC.

Method 2:



If you have chosen to hide the pins to be shorted by checking the Ignore checkbox in Package properties and also defined those pins as part of the PACK_SHORT property, the hidden pins will be written to the netlist. Also, its net will be inherited from the master pin which is visible on the symbol instance.

You can also use the PACK_SHORT property in conjunction with the PSpiceOnly property to specify shorting for nets attached to the instance. If a PACK_SHORT device is connected with two different nets across the PACK_SHORT pins, the net connected to the first pin defined in PACK_SHORT property will be written to the netlist.

Reference

OrCAD provides a number of netlist format files. You choose a netlist format in the Create Netlist dialog box.

- PCB Editor tab
- EDIF 2 0 0 tab
- INF tab
- Layout tab
- PSpice tab
- SPICE tab
- Verilog tab
- VHDL tab

- Other tab

Note: The Capture netlist format files are not the same as those shipped with SDT 386+. It is important that you keep both versions of the netlist format files installed if you plan on using both Capture and SDT 386+. Capture netlist formats files are supplied as .DLL files, while SDT netlist format files are provided as .EXE files.

Creating a netlist

To create a netlist

1. In the project manager, select the design file for which you want to create a netlist.
2. From the Tools menu, choose the Create Netlist command to display the Create Netlist dialog box.
3. Select a tab corresponding to the netlist format you want to use.
4. In the Netlist File text box, enter a name for the output file. If the selected format creates an additional file (such as a map file or pinlist file), enter the filename in the appropriate text box.
5. If necessary, set the Part Value and PCB Footprint combined property strings to reflect the information you want in the netlist. For more information about combined property strings, see Combined property strings.
6. If necessary, set other format-specific options in the Options group box.
7. Click OK to close the Create Netlist dialog box and create the netlist.

Creating a flat netlist

To create a flat netlist

1. In the Capture project manager, select the design file (.DSN) you want to netlist.

2. From the Tools menu, choose Create Netlist to display the Create Netlist dialog box.
3. Select the PSpice tab.
4. Under the Options frame, leave all the check boxes blank.
5. In the Use Template list box, select the netlisting template(s) you wish to apply. See how to specify an alternate netlist template below.
6. Check whether you want to place DRC markers for Errors and Warnings.
7. In the Netlist File text box, type a name for the output file, or click the Browse button to assign a filename.
8. If desired, click the View Output check box to display the netlist after it has been generated.
9. Click OK.

Creating a hierarchical netlist

To create a hierarchical netlist

1. In the Capture project manager, select the design file (.DSN) you want to netlist.
2. From the Tools menu, choose Create Netlist to display the Create Netlist dialog box.
3. Select the PSpice tab.
4. Under the Options frame, click Create Hierarchical Format Netlist.
5. Click Settings to customize the format of the hierarchical netlist.
6. Click Create Subcircuit Format Netlist to specify how subcircuits will be netlisted.
7. In the Use Template list box, select the netlisting template(s) you wish to apply.
8. Check whether you want to place DRC markers for Errors and Warnings.

9. In the Netlist File text box, type a name for the output file, or click the Browse button to assign a filename.
10. If desired, click the View Output check box to display the netlist after it has been generated.
11. Click OK.

Customizing the hierarchical netlist

You can also customize the format of the subcircuit definition and reference text in the netlist. These settings, once defined, persist and will apply to all subsequent PSpice netlists whether the netlist is invoked from the Tools menu in the project manager or directly from within the schematic editor. Of course, you can always change the settings in the Settings dialog box.

Two groups of settings are saved: PSpice and "Layout versus Schematics" (or LVS). Having two groups makes it easy to switch between netlisting for PSpice and netlisting for an LVS compatible format. You can specify which group of settings is active for the netlister by using the Products list box.

Note: The settings you define are project specific. If you want to save the settings globally, click the Save as Default Project Settings button.

To customize the hierarchical netlist

1. In the PSpice tab of the Create Netlist dialog box, under the Options frame, click Create Hierarchical Format Netlist.
2. Click Settings, then enable or specify the following options, as desired:
3. Click OK.

Passing parameters to subcircuits

Hierarchical netlists have the advantage of allowing parameters to be passed from the top level schematic to any subcircuit schematics. To take advantage of this feature, you must use the SUBPARAM part in the SPECIAL.OLB library.

To learn more about setting up parameterized subcircuits for hierarchical netlists, click Using SUBPARAM.

Note: Hierarchical netlists do not support cross-probing from a subcircuit, nor do they support Probe markers in a subcircuit. Cross-probing only works on the top-level (root) schematic.

Creating subcircuit netlists

You can specify how subcircuits in a hierarchical design are processed and defined in the simulation netlist.

You cannot directly simulate a subcircuit netlist; it defines a model that can be called by another circuit being simulated. The models of parts in the PSpice libraries such as op amps and regulators, which have multiple constituent components, are implemented as subcircuits.

A subcircuit implementation may consist of a single schematic, or a hierarchy of schematics.

To create a subcircuit format netlist

1. In the Capture project manager, select the design file (.DSN) you want to netlist.
2. From the Tools menu, choose Create Netlist to display the Create Netlist dialog box.
3. Select the PSpice tab.
4. Under the Options frame, click Create Subcircuit Format Netlist, then click one of the following options, as desired:
   - Descend: This generates a definition of a hierarchical design that includes the top level circuit as well as its subcircuits. (This option is only available if Create Subcircuit Format Netlist is enabled.) If the Create Hierarchical Format Netlist is not checked, then this option combination is equivalent to creating a flat netlist.
   - Do Not Descend: This generates a definition of a hierarchical design that includes only the top level circuit, without any of its subcircuits. (This option is only available if

Create Hierarchical Format Netlist and Create Subcircuit Format Netlist are enabled.)

To define a subcircuit

1. Place hierarchical ports on the top level of the subcircuit for each node that interfaces to the circuit that will use it. (You should place all such ports on a single page of a multi-page schematic.)
2. Add a sequence property to each port, assigning values of 1, 2, and so forth. When you select the Create Subcircuit Netlist Format option on the PSpice tab of the Create Netlist dialog box, it generates a header line of the form:

   .SUBCKT LM317 IN ADJ OUT

   The example above comes from a schematic with ports named IN, ADJ, and OUT. The three ports were assigned Sequence property values of 1, 2 and 3 respectively.

To use this subcircuit in another schematic

1. Place a hierarchical symbol, or draw a hierarchical block.
2. Set the Implementation Type to PSpice Model and the Implementation to LM317. The symbol or block must be primitive and have a PSpice Template such as the following:

   ```
   X^@REFDES %IN %ADJ %OUT @MODEL
   ```

   The PSpice netlister, under guidance of the PSpiceTemplate, produces a line of the form:

   ```
   X_U1 INNET ADJNET OUTNET LM317
   ```

   INNET, ADJNET and OUTNET refer to the IN, ADJ, and OUT ports of the defining circuit. Because the correspondence is by position, the port order in the subcircuit definition must match the net order in the reference. The order in which netnames appear in the reference is controlled by the PSpiceTemplate property. As mentioned above, the Sequence property added to each port determines the order in which port names appear in the subcircuit definition.

   For more information on the use of subcircuits, see the section on the .SUBCKT command in the online *PSpice Reference Manual*.

Specifying an alternate netlist template

OrCAD provides a number of netlist format files. You choose a netlist format in the Create Netlist dialog box.

- PCB Editor tab
- EDIF 2 0 0 tab
- INF tab
- Layout tab
- PSpice tab
- SPICE tab
- Verilog tab
- VHDL tab
- Other tab

Note: The Capture netlist format files are not the same as those shipped with SDT 386+. It is important that you keep both versions of the netlist format files installed if you plan on using both Capture and SDT 386+. Capture netlist formats files are supplied as .DLL files, while SDT netlist format files are provided as .EXE files.

To specify an alternate netlist template

1. In the Capture project manager, select the design file (.DSN) you want to netlist.
2. From the Tools menu, choose Create Netlist to display the Create Netlist dialog box.
3. Select the PSpice tab.
4. In the Use Template list box, add the name of the template you want to use.

Using SUBPARAM

You can pass parameters from the top-level schematic to a subcircuit schematic using the SUBPARAM part. This allows you to explicitly

define the properties and default values to be used during netlisting and simulation.

Any part in the subcircuit (child) schematic can reference the properties in its PSPICETEMPLATE. The PSpice subcircuit mechanism supports parameterizing:

- constants specified on device statements
- model parameters
- expressions consisting of constants
- parameters
- functions

To set up parameter passing to a subcircuit using SUBPARAM

1. Make the subcircuit your active schematic page in the Capture schematic page editor.
2. From the Place menu, choose the Part command.
3. Select the part SUBPARAM from the PSpice library SPECIAL.OLB and place it on the subcircuit.
4. With the SUBPARAM part still selected, from the Edit menu, choose Properties.

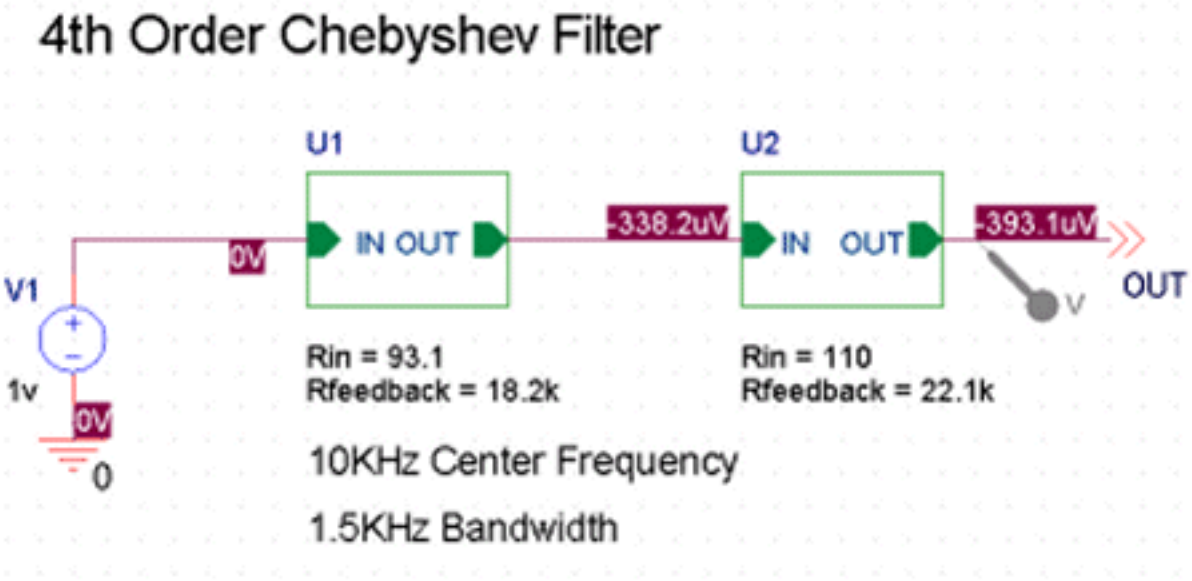
   The property editor appears.
5. In the spreadsheet, on an instance-by-instance basis, define the names and default values for the properties that can be changed.

   To view property names and values at the same time, select a property cell, and click the Display button. When the Display Properties dialog box appears, check Name and Value format for Display Format, then click OK.
6. In the top-level schematic, use the property editor to edit the properties of the hierarchical part or block that references the subcircuit (child) schematic so they match the properties you defined in Step 5.

Example

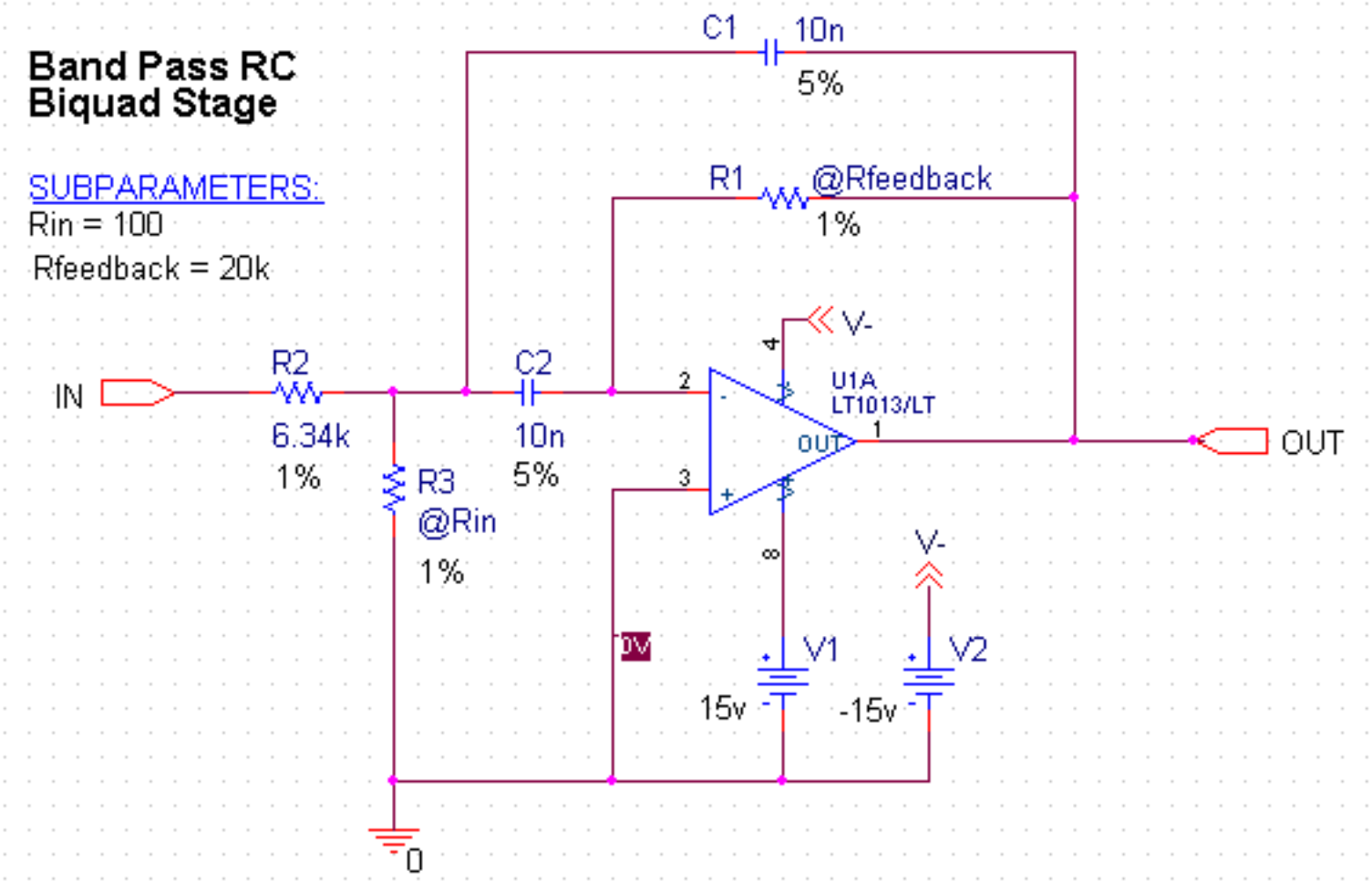
This fourth-order Chebyshev filter schematic illustrates how the SUPARAM part may be used to pass design parameters from a top-level (parent) schematic to a subcircuit (child) schematic in a hierarchical design.

In the top-level schematic, you explicitly define the parameter values you want to pass to a subcircuit. In this case, the parameters and their corresponding values for the U2 subcircuit are Rin = 110 and Rfeedback = 22.1k.



Descending into the hierarchy of the U2 subcircuit, you see the Rin and Rfeedback parameters listed with their corresponding default

values of 100 and 20k, respectively, in the SUBPARAM part (under SUBPARAMETERS).



Notice the Rin and Rfeedback values are preceded with @ symbols, indicating that these parameters are substituted with values passed down from the top-level schematic.

Here is the hierarchical netlist generated in Capture for this design:

```
* source HISTO
V_V1 N00023 0 AC 1v
X_U1 N00023 N00030 OneStage PARAMS: RIN=93.1 RFEEDBACK=18.2k
X_U2 N00030 OUT OneStage PARAMS: RIN=110 RFEEDBACK=22.1k

.SUBCKT OneStage IN OUT PARAMS: RIN=100 RFEEDBACK=20k
V_V2 V- 0 -15v
R_R2 IN N00024 R_R2 6.34k
.model R_R2 RES R=1 DEV=1%
R_R1 N00034 OUT R_R1 {Rfeedback}
```

```
.model R_R1 RES R=1 DEV=1%
R_R3 0 N00024 R_R3 {Rin}
.model R_R3 RES R=1 DEV=1%
C_C1 N00024 OUT C_C1 10n
.model C_C1 CAP C=1 DEV=5%
C_C2 N00024 N00034 C_C2 10n
.model C_C2 CAP C=1 DEV=5%
X_U1A 0 N00034 N00594 V- OUT LT1013/LT
V_V1 N00594 0 15v
.ENDS
```

Here, the U2 and U1 subcircuits are referenced in the source (top-level) circuit as X_U1 and X_U2 with the explicit values defined for the parameters that are passed to from the top-level. A .SUBCKT models both the U1 and U2 subcircuits and the default parameters are listed as placeholders. When PSpice simulates the design, the parameters passed from the top-level circuit are the ones used in the subcircuits.

Generating library parts

This section covers:

"Generating a part from a PSpice model library" on page 549

"Generating a part from a schematic or library" on page 550

Generating a part from a PSpice model library

You can use the Generate Part dialog box to create a part that has pins matching all the hierarchical ports on the root schematic of the design for design reuse. If a destination library file doesn't exist, Capture creates a library part file (.OLB) that contains the newly generated part and a copy of the top-level schematic. The new .OLB appears in the project manager Outputs directory along with the new part and schematic. The new part has a reference back to the design where the source schematic resides so that when you descend the hierarchy from the placed part, it will open the source schematic from the destination library.

Note: To create a pin on a symbol using the Generate Part utility, the pin must have a pin to port mapping in the pin file.

To generate a part from a PSpice model library

1. From the Tools menu, choose Generate Part to open the Generate Part dialog box.
2. In the Netlist/source file text box, enter the path and name of the file you want to use to generate the part, or click the Browse button to browse for it. Be sure to change the Files of type in the Browse File dialog box to PSpice Model Library Files (*.cir, *.net, *.lib).
3. Select the Implementation name from the drop-down list box in the Implementation options. If more than one model is available, you can choose one from the drop-down list, or you can keep the default setting of <ALL> that appears in the Implementation name and the Part name text boxes. Choosing <ALL> will create a part from all available models.
4. In the Destination part library text box, you can choose to accept the default path and file name, enter the path and name of the file you want to use for the new library, or click the Browse button to search for another one.
5. Click OK. The Microsim Schematics to Capture Translator translates a single model or all of the models in the library for reuse in Capture.

Generating a part from a schematic or library

You can use the Generate Part dialog box to create a part that has pins matching all the hierarchical ports on the root schematic of a design and use the design as a reuse module.

If a destination library file doesn't exist, Capture creates a library part file (.OLB) that contains the newly generated part and a copy of the top-level schematic (if the Copy schematic to library option is selected). The new .OLB appears in the project manager Outputs directory along with the new part and schematic. The new part has a reference back to the design where the source schematic resides so that when you descend the hierarchy from the placed part, it will open the source schematic from the destination library.

To generate a part from a schematic design for reuse

1. In the project manager, click to select a schematic folder from which you want to create a part. The schematic can be in a design (.DSN) file or a library (.OLB) file.

   Note: The design file you use for the source must contain ports or the Generate Part operation will fail.

2. From the Tools menu, choose Generate Part. Capture fills in default settings in the Generate Part dialog box.

3. Browse to change the Netlist/source file or keep the default settings. You can generate a part from an external design or from the current design in the active project manager window.

4. Select the Netlist/source file type. For example, choose Capture/Schematic Design if you are generating a design reuse module.

5. Keep the default Part name or enter another name from the design.

   - If the source design has more than one schematic and no schematic is selected or if more than one schematic is selected, the Part name setting defaults to the root schematic.
   - If the source design is not opened in the current project manager window, its root schematic will be the default Part name.

6. Browse to change the Destination part library or keep the default settings. The default setting creates a new .OLB file that matches the name of the source .DSN file. If the source design is a library (.OLB), the default part library name will be the same name as the source file.

7. Set the new part's Primitive property using the Primitive radio buttons. The default value is No. You can descend from the placed part to its schematic if the Primitive is set to No. For a design reuse module check Default.

8. Select the Copy schematic to library check box if you want to include a copy of the schematic in the new .OLB file along with the new part. This option is unavailable if the source and destination files are the same.

If you are generating a design reuse module, do not check the Copy schematic to library option. If you do, you will lose occurrence properties which are critical in the design reuse module. Also, checking this option will overwrite the custom library, so make sure to specify an used library name unless you intend to overwrite.

9. Click OK.

   Note: If the source schematic is copied and becomes locally available in the library, the implementation path is the same as the destination library. If the source schematic is not copied, the implementation path is the same as the source design or library.

To reuse an existing hierarchical design

1. Create a new project or open a working design.
2. In the project manager from the Tools menu, choose Generate Part.
3. Use the Browse button to pick a source design file that has a reusable design and is useful in the working design.
4. Select the schematic to reuse.
5. Enter a resulting library name or keep the default.
6. Select the Copy Schematic to Library Check box and click OK to create a part.
7. Select the schematic page editor window to place instances of the part to reuse its schematic design.
8. Click OK.

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Using Capture with PCB Editor

This section will help you understand Capture-PCB Editor flow and use it effectively.

Capture offers full integration with Cadence® PCB Editor tool suite, allowing you to use all of Capture schematic design capabilities to enter your PCB projects, then export the information to PCB Editor for layout and routing.

Capture-PCB Editor design flow

Like any other PCB design flow, Capture-PCB Editor flow involves the following steps:

1. Preparing a Capture Design
2. Creating the board file (Netlisting)
3. Placing and routing the board
4. Synchronizing the design file with the changes done in the board file
5. List of Unsupported Capture-PCB Flow field values
6. Netlist Formats (Other Netlists)

You will learn more about these steps in this section.

Preparing your design for use with PCB Editor

Preparing a design for PCB Editor is similar to designing any other design flow. The steps involved in preparing a Capture design for use with PCB Editor:

1. Preparing libraries
2. Placing components and wiring them up
3. Annotating the design
4. Assigning properties (attributes)

The first step in preparing a design is to prepare a design library. When you prepare a design library, you must ensure that you have added all PCB Editor related properties to the design.

PCB Editor has a predefined set of default properties for different components, functions, nets, and pins. You can add custom properties to this default set by defining them in PCB Editor using the Property Definitions command, accessed from PCB Editor's Setup menu. In order for any property to be passed from Capture to PCB Editor, the property name must be found in Updating the PCB Editor configuration file specified from the Setup dialog box in Capture. So, if you add a custom property in PCB Editor, you must also add the property in Capture as well as in the configuration file.

How properties are netlisted from Capture to PCB Editor

Not all properties in Updating the PCB Editor configuration file show up as properties in PCB Editor. Some of these properties are used in generating portions of the netlist PST*.DAT files.

In PCB Editor, component properties (package properties in Capture) take precedence over function properties (part properties in Capture). So in the netlist, a package property value is used if both a part and package have values for the same property. Capture always uses the occurrence values in the netlist.

Package (component) properties, which are found in the PSTCHIP.DAT andPSTXPRT.DAT netlist files, can be viewed in PCB Editor using the Show Element command on a component. For

example, PCB Editor has defined VALUE as a Component Definition property so it appears under this heading in the Show Element dialog box. Other properties such as CLASS or JEDEC_TYPE are also listed.

Part (function) properties are found in the PSTXPRT.DAT file and can appear as Component Definition properties if they are predefined in PCB Editor and if you list them in the [ComponentDefinitionProps] section of the configuration file. Function properties are listed in the [functionprops] section of the configuration file.

Net properties appear in the PSTXNET.DAT/PSTXPRT.DAT file under the NET_NAME section.

Preparing libraries for Capture to PCB Editor flow

Capture supports two types of components that can be added to a library, single-section packages and multi-section packages. A single-section package contains a single logical part in it, while a multi-section consists of multiple logical parts. A multi-section package can be further categorized as:

- Homogenous package - If all the logical parts in a package are identical except for the pin names and pin numbers, the package is homogeneous.
- Heterogeneous package - If the logical parts in a package have different graphics, pin numbers, or properties, the package is heterogeneous.

Similarly, PCB Editor also supports two types of components, single-section parts and multi-section parts. Single section parts consist of only single sections, while multi-section parts consist of multi-sections which can be categorized as:

- Symmetrical parts - This part consists of a package that has the same logical pin list across all the sections/functions of the package.
- Asymmetrical parts - This part consists of a package that has a different logical pin list across all the sections of the package.
- Split parts - This part consists of a package in which pins are split across multiple sections. You may split a large-sized part that may not fit in a single schematic page into multiple sections

based on your specifications and can place different sections in different schematic pages. You may also want to partition a large part based on its functionality and use sections individually. For example, you may like to create different sections for pins with same voltage rating.

The basic difference between an asymmetrical and split part is that a split part does not have any relation among its sections where an asymmetrical part has common pins across multiple sections.

Note: Logical pinlist: A unique set of pin names on each part per package is called the logical pinlist of the part.

Note: Physical pinlist: A list of physical pin numbers associated with logical pin names.

Single-section parts in PCB Editor map to single-section packages in Capture. Symmetrical parts in PCB Editor map to homogeneous packages in Capture, while asymmetrical parts and split parts both map to heterogeneous packages.

Besides the difference in types of components they support, Capture and PCB Editor also differ the way they read component information. Capture understands component information in .OLB format, whereas PCB Editor understands these in a specific file format - PSTCHIP.DAT, which is a readable ASCII file. The PSTCHIP.DAT file contains information about the different components used in a particular design. This file is generated by the Capture-PCB Editor Netlister from a design file.

Guidelines for preparing libraries for Capture-PCB Editor flow

- Limit part and pin names to 31 characters.
- Use only upper case characters for part/symbol names, reference designators, and pin names
- Do not use special characters to assign part names, reference designators, or pin names
- Do not use duplicate names for pins other than power pins
- For multiple power pins with the same pin name, do not make some pins as visible and others as invisible
- Do not use “0” as a pin number

Creating a split part

A split part is a multi-sectioned package. You may need to section a part for different reasons:

- Your design may include parts that have thousands of pins. Such large-sized part may not fit in a single schematic page. To handle such parts, you can split them into multiple sections based on your specification and can place different sections in different schematic pages. This will ease designing.
- You want to partition a large part based on its functionality and use sections individually. For example, you may like to create different sections for pins with same voltage rating.

Capture allows you to split a part using the Split Part Section Input Spreadsheet.

To split a part

1. Select the part that you want to split from the Library folder in the project manager.

   Note: You need to select a single-sectioned part from a library. You can split a multi-sectioned part only when it has already been split using the Split Part Section Input Spreadsheet.

2. Select the Tools menu and choose the Split Part command.

   or

   Right-click on the selection and choose Split Part from the pop-up menu.

   The Split Part Section Input Spreadsheet appears displaying all the pins and their corresponding properties for the selected part.

   Note: The Part Name and Part Ref Prefix fields display the name of the selected part and its part reference. These fields are view-only.

3. Select Numeric or Alphabetic in the Part Numbering group. If you select Alphabetic, an alphabet (between A to Z) will be added as a suffix to the current part reference for each of the split parts. If you select Numeric, a number (between 1 and 1024) will be

added as a suffix to the current part reference for each of the split parts.

The Section property column changes based on your selection in the Part Numbering group. For example, if Alphabetic is selected, the Section property column displays “A”.

Tip

Resize the Split Part window by dragging the borders as per your requirement.

4. Specify the number of sections you want to have in the split part in the No. of Sections text box. The Section property column changes to a list box displaying the number of sections you specified in the No. of Sections text box.

Caution

Number of sections cannot be less than one.

Note: If you select alphabetic numbering, then you can create up to a maximum of 26 sections only. If you select numeric numbering, then you can create up to a maximum of 1024 sections.

5. Click on a Section cell for a specific pin and select a section number from the list box.

   or

   Click on a Section cell and enter the new section number.

   The selected Section cell displays the new section number.

Tip

You can select Section cells for multiple pins simultaneously using the SHIFT+Down Arrow keys and enter the section number. Alternatively, you can:

- Select the Section cells for multiple pins simultaneously using the SHIFT+Left mouse button click, then press the CTRL key, and then select a section number of your choice from the list box. The selected Section cells get populated with the section number of your choice.

- Click the first cell of the range, and then drag to the last cell, and then enter the section number of your choice. The selected Section cells get populated with the section number of your choice.

Tip

You can select alternate Section cells for multiple pins simultaneously using the CTRL+Left mouse button click and enter the section number.

Tip

To sort on any property, double-click its name in the column header.

Note: The order in which the pins appear in the spreadsheet, the pins will be added in the same order in the split part.

6. Click the Save button to save the changes to the current part. If any warnings are generated during the save operation, a message box appears asking you whether you want to view the warnings. If you want to view the warnings, click the View Warnings button. The Split Part Section Input Spreadsheet expands and displays a grid showing warnings messages. If you select the Continue button, the split part is saved as is.

   Note: Click the Hide Warnings button to hide the warning messages or the Show Warnings button to display the warning messages again.

   Note: Use Save As to retain the original part and save the changed part as a new part in the same library.

Note: If the number of Sections specified in the Split Part Section Input Spreadsheet is greater than one, then the resulting part will be of heterogeneous package type.

Tip

You can hide or show a property column in the Split Part Section Input Spreadsheet. To do this, right-click the property column header you want to hide and select Hide from the pop-up menu. The selected property column will not appear now. To show a property column, right-click the

property column header next on the right-hand side of the hidden property column and select Unhide from the pop-up menu. The hidden property column appears in the Split Part Section Input Spreadsheet. Alternatively, you can show a property column by:

- Double-clicking the column handle ( ) of the property column header.
- Dragging the column handle of the property column header.

(only the last two methods can be used to show a property column, which is the last column in the Split Part Section Input Spreadsheet).

Note: You can change the order in which the property columns and rows appear in the Split Part Section Input Spreadsheet. To do this, select the property column/row header you want to move and drag and drop it to the location where you want it in the Split Part Section Input Spreadsheet.

Note: You can use standard copy and paste feature to copy all data from the Split Part Section Input Spreadsheet to MS Excel. You can later use the MS Excel file for archiving or documentation. It is recommended that you avoid using MS Excel to paste information into the Split Part Section Input Spreadsheet.

Adding pins to Split Part Section Input Spreadsheet

You can add more pins to the Split Part Section Input Spreadsheet. The pins are added at the end of the current set of pins. The pins numbers for the added pins is generated automatically.

To add a pin

1. From the Split Part Section Input Spreadsheet, Click the Add Pins button. The Add Pins dialog box appears.
2. Specify the number of pins you want to add in the Number of Pins text box.
3. Click OK. The required pins are added at the end of the current pin set in the Split Part Section Input Spreadsheet.

   Note: All the pins added are populated with default property

values. The default value for the Section property column is 1.

Deleting pins from Split Part Section Input Spreadsheet

You can delete pins along with their corresponding properties in the Split Part Section Input Spreadsheet.

Once you delete a pin from the Split Part Section Input Spreadsheet, you cannot retrieve it later.

To delete a pin

1. Select a row in the Split Part Section Input Spreadsheet.
2. Click the Delete Pins button. A message box appears asking you to confirm the deletion.
3. Click OK to confirm deletion. The selected row containing the pin information is deleted from the Split Part Section Input Spreadsheet.

Viewing split part properties

When you split a part, Capture assigns the following properties to it:

- `SWAP_INFO`—This property is assigned to each section and its value is determined by the number of sections you specified in the No. of Sections text box in the Split Part Input Spreadsheet. For example, if you split a part into 3 sections then all the 3 sections will be assigned the `SWAP_INFO` property with value (S1+S2+S3).
- `SPLIT_INST=TRUE`

Saving a multi-section split part will remove any existing SPLIT property. Instead, it will add the SPLIT_INST property.

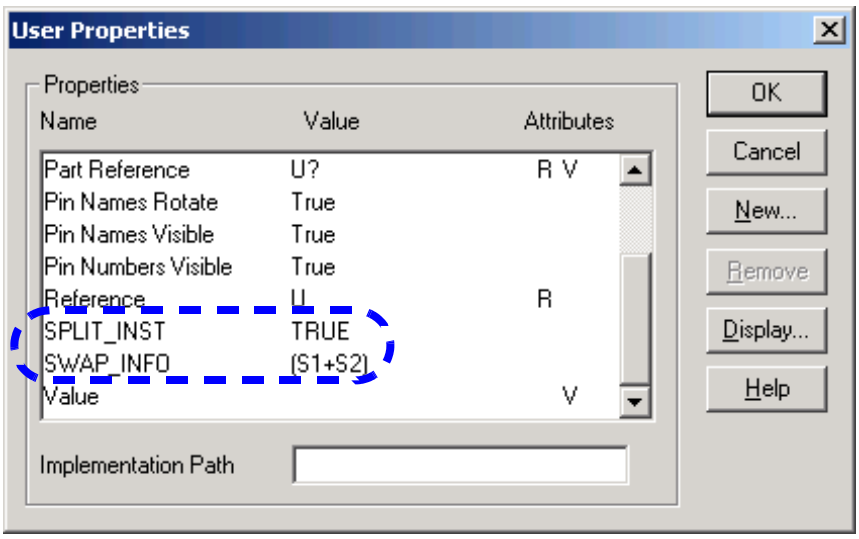
Caution

Saving a multi-section split part will overwrite any existing SWAP_INFO property value with the value (S1+S2+S3+...Sn), where n is the number of Sections specified.

Note: Ensure that you use '(' and ')' brackets for defining single sections also. For example, If you have a split part having 6 sections (S1 to S6) and wish to add the SWAP_INFO property such that swapping happens only between sections S5 and S6. In that case you need to add the SWAP_INFO value as (S1), (S2), (S3), (S4), (S5+S6).

To view split part properties

1. Double-click a split part from the Library folder in the project manager. The Part editor window appears.
2. Select the Options menu and choose Part Properties. The User Properties dialog box appears. The following figure shows a split part with the two properties assigned to it.



Note: The SWAP_INFO and SPLIT_INST properties appear in the User Properties dialog box for only those parts, which are heterogeneous.

Viewing split part package and package properties

A split part is a multi-sectioned package. You can view a split part in package view.

To view split part package

➤ From the part editor, select the View menu and choose the Package command. An image of all the sections in the package appears.

Note: You can also double-click a split part from the Library folder in the project manager to open the part editor window.

Note: The part reference for each of the sections contain a suffix entry. For example, J?A, J?B, and J?C, where A, B, C are the section numbers.

To view split part package properties

1. From the part editor, select the View menu and choose the Package command.
2. Select the Options menu and choose the Package Properties command.

   The Edit Part Properties dialog box appears. The Multi-Part Package group displays the properties for your split part package, like parts per package, package type, and part numbering.

Assigning properties in Capture for use in PCB Editor

If a property is found in the configuration file, then a value will only be found in the netlist if a value for that property exists on the part in Capture. You can add these properties to the library part themselves and then place the parts in the design.

Note: Using PCB Editor properties. If you want more specific information about definitions, uses, typical values, syntax, examples, and samples for PCB Editor properties, then see the *PCB Systems Properties Reference* installed with PCB Editor software. To view this manual, click the Windows Start menu, choose the Programs menu item, then select the Cadence Help item from the Cadence PSD 16.0

list. A browser window is launched and the *PCB Systems Properties Reference* may be found in the list of documents presented.

Using the POWER_PINS property

This property is specific to the Capture-PCB Editor design flow.

When you generate a part in Part Editor you can define the nets for the power pins on the part. For example, you can define the pins 1, 3 and 7 on the VCC net and 2, 4, 5 and 6 on the GND net. However, Capture also allows you to override these assignments for a part at the schematic level by using the POWER_PINS property.

To use the POWER_PINS property

1. Open the Property editor for the selected part
2. Click New Row.

   The Add New Row dialog displays.
3. In the Name text box, type POWER_PINS.
4. In the Value text box, type the power pins assignment.

   Example 1:

   To assign the pins 4, 5 and 7 to the VCC net. the power pins assignment is defined as:

   (VCC:4,5,7)

   Example 2:

   To assign the pins 4, 5 and 7 to the VCC net and the pins 16, 18, 21 to the GND net. the power pins assignment is defined as:

   (VCC:4,5,7;GND:16,18,21)

Capture does not support duplicate name properties. So, in Example 2, you must define the VCC power pins assignment and the GND power pins in the same POWER_PINS property. To do this, use the semi-colon to differentiate between the assignments.

Note: The power pin assignments that you perform through the POWER_PINS property are defined at the schematic level. This means these changes will not be reflected on the part. So if you open the selected part in the Part Editor, the pin assignments will not be reflected here. However, in the Capture - PCB Editor flow, the POWER_PINS property on the part will take precedence over the part instance pin assignments.

Using the POWER_GROUP property

This property is specific to the Capture-PCB Editor design flow.

Normally, Capture connects invisible power pins to a default power net that shares a name with the pin. POWER_GROUP is a special (component definition) property that can be defined in the schematic (rather than the library) that lets you assign a value to the invisible power pins on a component. POWER_GROUP gives you the ability to have different values for the power net used on a particular design, instance or occurrence. You use this property whenever you want to reassign the net name for invisible power pins on the component.

The POWER_GROUP property is used to change the net name attached to a particular invisible power pin(s). POWER_GROUP is a part property that circumvents the need to edit the pin properties for each invisible power pin on a particular component.

POWER_GROUP can be assigned with a unique value for multiple occurrences in the design. Multiple occurrences of a part can have different values for the POWER_GROUP property, allowing you to control power net connections at the occurrence level.

With the POWER_GROUP property added to parts with invisible power pin(s), you can overwrite power pins with the new power pin name at the instance level. If this property is used, POWER_GROUP is added to your combined property string so that you can annotate correctly.

The POWER_PINS property determines the power net in your design, to which invisible pins are connected. In order to connect multiple (invisible) power pins to the same net, you assign the POWER_GROUP property to each component that includes these pins.

Using the ALT_SYMBOLS property

The ALT_SYMBOLS property lets you specify a list of alternate Footprint names that can be used to substitute the primary Footprint during interactive placement in PCB Editor. The syntax of the ALT_SYMBOLS is as follows:

```
ALT_SYMBOLS '(Subclass:Symbol,...;Subclass:Symbol,...)'
```

where, Subclass can either be TOP (or T) for top layer, or BOTTOM (or B) for bottom layer and Symbol can be standard PCB Editor or APD footprint name.

You can assign an ALT_SYMBOLS property to a package or component either at the library level or at the instance level. For example, you can assign the component 7400 the following ALT_SYMBOLS value, T:dip14_3;B:dip14_3

Using the SWAP_INFO property

To enable pin swaps across sections of split (heterogeneous) parts in PCB Editor, a SWAP_INFO property has been introduced in PCB Editor.

Note: In Capture 9.2.3, the SPLIT property provided a method for swapping pins between parts of a heterogeneous package. From Capture 10.0, we recommend that you use the SWAP_INFO property as it provides the same functionality with better features. In Capture 10.5, the SPLIT property has been renamed to SPLIT_INST.

In existing designs, please do not replace the SPLIT property with the SWAP_INFO property. The SPLIT property converts parts as flat parts whereas the SWAP_INFO property leaves the part as a split part. On an existing design, replacing the SPLIT property on a component package with the SWAP_INFO property will change its definition from a flat part to a split part. This will cause component rip-offs in the board file.

The SWAP_INFO property defines a logical group of parts of a package in a heterogeneous (split) part. This allows two pins having

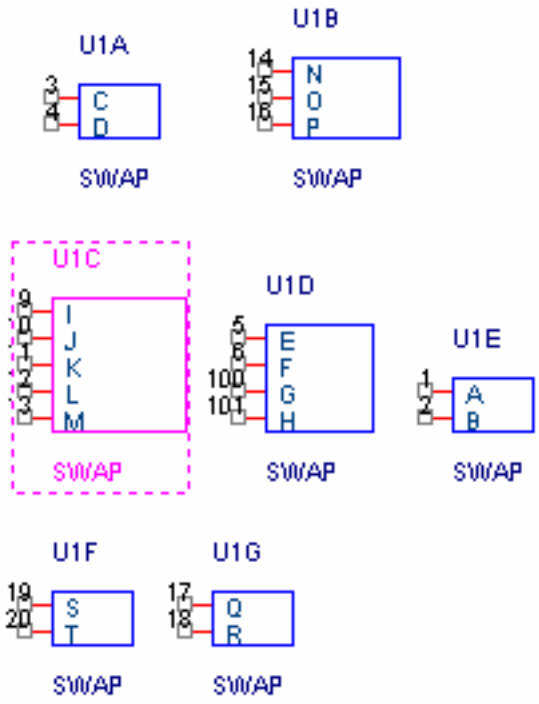
the same PIN_GROUP property to be swapped within a logical group, regardless of the physical availability of the pin in the given part of the package.

The SWAP_INFO property is defined under the [ComponentDefinitionProps] section in the allegro.cfg file. The swap information is written into body section of the primitive of the pstchip.dat file. PCB Editor reads the SWAP_INFO property in the pstchip.dat file and accordingly allows pin swaps across sections.

Note: If you have a customized PCB Editor configuration file (Allegro.cfg) for your Capture PCB Editor netlister, you need to add the following entry under the [ComponentDefinitionProps] section in the Allegro.cfg file:

```
[ComponentDefinitionProps]
SWAP_INFO=YES
```

The usage of the SWAP_INFO property is described using a split part.



The above figure shows the example of a heterogeneous (split) part having seven parts-per-package. Let us assume that parts with the reference designators:

- U1A and U1B, form one logical section
- U1C, U1D and U1E, form the second logical section, and
- U1F and U1G, form the third logical section

In this scenario the value of the SWAP_INFO property on all the parts of the package will be defined as:

```
(S1+S2),(S3+S4+S5),(S6+S7)
```

The logical section (S1+S2) indicates that a pin in section S1 is swappable with a pin in section S2, provided they have the same PIN_GROUP value. Therefore, pin 3 of S1 can be swapped with pin 14 of S2 if they have the same PIN_GROUP value.

In a SWAP_INFO syntax, the logical and physical sections are separated by a (+) sign.

Note the following when you use the SWAP_INFO property:

- You must assign the SWAP_INFO property to all parts in the heterogeneous package for which you want to perform pin swapping.
- There must not be any duplicate pins on any of the parts in the heterogeneous package if they are to receive the SWAP_INFO property.
- Ensure that you name the sections as (S1+S2+ S3+…S*n*). If you use any other notation for naming the sections, the SWAP_INFO property will not work.
- Ensure that you use ‘(‘ and ‘)’ brackets for defining single sections also. For example, If you have a split part having 6 sections (S1 to S6) and wish to add the SWAP_INFO property such that swapping happens only between sections S5 and S6. In that case you need to add the SWAP_INFO value as (S1), (S2), (S3), (S4), (S5+S6).
- The SWAP_INFO property does not function for homogeneous parts. No DRC errors will be reported if the SWAP_INFO property is assigned to a homogeneous part.

- DRC errors will not be reported if there are syntax or semantic errors in the value of the SWAP_INFO property.

Using the SPLIT_INST property

The SPLIT_INST property provides a method for swapping pins between parts of a heterogeneous package. You can assign it to a part in a library, or to an instance in a design.

Note: When you assign the SPLIT_INST property to a part at the library or instance level, all lower level occurrences of that part (on the schematic) inherit the property.

The SPLIT_INST property has two possible values: TRUE and FALSE (default). Assigning a value of TRUE to the SPLIT_INST property on the parts of a heterogeneous package indicates that the netlister treats the package as a flat part, thus allowing pin swapping between the parts of that package.

When you use the SPLIT_INST property, be aware of the following points:

- You must assign the SPLIT_INST property to each part in the heterogeneous package for which you want to perform pin swapping.
- The SPLIT_INST property does not function for homogeneous parts (nor will the Design Rules Check tool detect an error if SPLIT_INST is assigned to a part that is part of a homogeneous package).
- There must not be any duplicate pins on any of the parts in the heterogeneous package if they are to receive the SPLIT_INST property.
- Cross-probing will not function on pins of parts that have the SPLIT_INST property assigned to them. You can work around this by cross-probing the connected nets rather than the pins.

To assign properties in Capture for use in PCB Editor

There are several ways to make property assignments if the parts are already placed in your design:

- In the schematic design editor, select the part to which properties are to be added, then right-click and choose Edit Part from the pop-up menu to activate the part editor. Choose the Part Properties command from the Options menu to add properties such as PCB Footprint and CLASS. After modifying the part and closing the User Properties window, click the Update All button when you close the property editor window to make sure the properties are propagated to every like part in the design. You can use the Capture-Allegro filter in the Property Editor to view typical properties that may be assigned in Capture to be used in Allegro PCB Editor. (This list of properties comes from the PREFPROP.TXT file, placed in your Capture folder during installation). For information about the Allegro PCB Editor properties, see document *Allegro Platform Properties Reference* guide (*propref.pdf*).

- Modify your parts in the library and then use the Replace Cache command on the Design menu with the Preserve schematic part properties option. If you don't have the original library, you can create a library and copy the parts from the design cache to the new library, then modify the parts in the new library.

- Add or edit properties manually in the property editor. You can access the property editor by double-clicking on the part or selecting a part and then choosing Edit Properties from the pop-up menu. If you change the occurrence values on the part, occurrence values are used instead of the values found in the library. If you haven't changed the occurrence values, then the values are those from the original library.

- Use the Update Properties command from the Tools menu with an update (.UPD) file which adds properties and corresponding values to one or more components.

Note: PCB Footprint. In order to correctly map a logical package to the physical board environment, you must specify a PCB Footprint for each and every part in your design. PCB Editor must have a valid PCB Footprint property for each part so the netlister can assign this property in the PSTCHIP.DAT file as the JEDEC_TYPE. This includes mechanical parts in your design (although, in this case, you can use a "dummy" value for the PCB Footprint property. In Capture 10.0, the Capture-PCB Editor flow, like other PCB flows, also allows you to use the combined property string to pass user-defined properties as PCB Footprint property for PCB Netlist generation. This enhancement gives you the flexibility of defining a user-defined PCB

Footprint property specifically for the PCB Editor flow. As a result, you can define different PCB Footprint properties for different PCB flows.

Note: Property string. You can use the Bill of Materials tool to see whether you have added a PCB Footprint to every part in your design. You can also just append the property name to the combined property string.

Note: Part name. The part name found between single quotation marks in the PSTCHIP.DAT file is just the value of the DEVICE property present. If there is no a DEVICE property on the part, then the part name is a made by combining the values of the Source Package, PCB Footprint and other properties that may be found in the [ComponentDefinitionProps] section of the configuration file. The part name string is a concatenation of these properties, with each value separated by an underscore character. By changing the order of component definitions properties in Allegro.cfg you can change the concatenation order.

Note: User-defined property names are case sensitive. If you have problems seeing properties netlisted or back annotated, check the spelling and the case of the property names. Also, all properties in PCB Editor are in upper case.

Note: Pin level property transfer between Capture and PCB Editor. You can also pass pin level properties between Capture and PCB Editor using a configuration file. This ensures seamless transfer of pin level constraints between Capture and PCB Editor. In the earlier versions of Capture, there was no way pin level properties could be transferred back and forth from Capture and PCB Editor and had to be manually specified at both ends. For example, now you can specify a property say, NO_SHAPE_CONNECT to a schematic pin. PCB Editor, on finding this property, will ensure that no connection is created between the pin (that passes through a shape with the same net) and a shape.

Note: Packaging of multi-section parts. During netlisting, multi-section, heterogeneous parts are treated as single-section parts. For multi-section parts, all sections must have the same values for the properties listed under [ComponentInstanceProps] in Updating the PCB Editor configuration file. For example, ROOM is a component instance property, so if you add {ROOM} to the combined property string when you annotate, then sections with differing ROOM properties will not be packaged together.

You can separate or combine component instances in a multi-section parts just by specifying distinguishing properties in the combined property string. Check the configuration file to identify the component instance properties currently available.

Note: If you are planning to back-annotate your design from Capture, do not modify the schematic in Capture while working on the design in PCB Editor.

To perform pin swapping between parts in a heterogeneous package

Note: Please refer to Defining heterogeneous and homogeneous parts for an explanation of heterogeneous parts and packages.

PCB Editor allows function/section swapping depending on the logical pin list on the function/section. This plays a key role when you create asymmetrical parts. If you have used invisible pins in a Capture design, these pins are not used by PCB Editor while deciding swappable sections. That is, body sections do not play any role in section swapping. PCB Editor calls each section as a function. A function is made with only logical pin list and any two functions that have same logical pin list are swappable in PCB Editor.

In the Capture-PCB Editor flow (only) you can perform pin swapping between parts in a heterogeneous package by using the SWAP_INFO or the SPLIT_INST property. This is useful when you are working with parts that have large pin counts (such as BGA parts). For information about the SWAP_INFO and the SPLIT_INST property, see Using the SWAP_INFO property on page 566 and Using the SPLIT_INST property on page 569. You can assign the SWAP_INFO or the SPLIT_INST property to a part at the library level (recommended) or at the instance level.

Note: When you assign the SPLIT_INST property to a part at the library or instance level, all lower level occurrences of that part (on the schematic) inherit the property. This is the only occasion in which a property at a higher level overrides properties at lower levels.

To avoid using visible power pins in the Capture-PCB Editor flow

1. Create a part with invisible power pins.

2. Place the part in your design. By default, Capture connects any power pins on the part to the corresponding global nets. So, for example, if the part included (invisible) power pins VCC, VDD, GND, and AGND, each of these would be connected to a corresponding global net of the same name.

3. In order to change the default power connections, select the part and add the POWER_GROUP property to reassign the connections for any of the power pins. So, for example, to change the connection for VDD to VCC, you would add the POWER_GROUP property as follows:

   ```
   POWER_GROUP VDD=VCC
   ```

   (To change the value of this property, open the Property spreadsheet, then go to the Capture-PCB Editor Property filter and enter “VCC=VDD” as the value of the POWER_GROUP property).

   In this example, pins in the netlist that would have been assigned to the VDD net are instead assigned to VCC and the netlister correctly reflects this change into the netlist.

Note: The POWER_GROUP property is handled at the individual net level. So, if you have a part that includes power pins VCC, VDD, VPP, AVCC, GND, AGND, you can reassign one, some, or all of these depending on your requirements. For example:

```
POWER_GROUP : VCC=AVPP; GND=HGND
POWER_GROUP : AGND=GND
```

Reassigning power pin connections

When reassigning nets, Capture uses precedence rules for the POWER_GROUPS property in the same way they are used for other component definition properties. Therefore, when a higher level property value overrides property values at a lower level, even if there are multiple occurrences at the lower level, each of these occurrences is replaced by the higher-level properties.

For example, assume you have an instance with various power signals VCC, VDD, VPP, and VSS. If you want all these signals to be shorted to VCC, then assign the following POWER_GROUP property in the Attribute form of the Property Spreadsheet:

```
POWER_GROUP = VDD=VCC;VPP=VCC;VSS=VCC
```

This results in the following assignments:

On the part	On the schematic instance	In the PSTCHIPS.DAT file
Pin numbers 14,28 = VCC Pin numbers 13,12=VDD Pin numbers 10,11 =VPP Pin numbers 8,9=VSS Pin numbers 7,21 =GND	POWER_GROUP= VDD=VCC; VPP=VCC; VSS=VCC	POWER_PINS='(VCC:14,28,13,12,10,11,8,9)'; POWER_PINS='(GND:7,21)';

Note: The POWER_PINS property is an PCB Editor property that defines the various power nets for layout purposes. The value of POWER_PINS is derived from the value of the POWER_GROUP property when you create an PCB Editor netlist for your design.

Using the IGNORE_PROP property to ignore the DEVICE property on your design

In cases where your design library includes the DEVICE property (an anachronism from previous releases), you can avoid having to remove the property from each part in your library by employing the IGNORE_PROP property. To ignore the DEVICE property on a complete design, define IGNORE_PROP as an environmental/system variable and assign it a value of "DEVICE."

Note: As with all environmental variables, IGNORE_PROP is specific to a system login. You must have administrative privileges to define IGNORE_PROP as a system variable for your system. Also, you must restart Capture in order to read the new environmental variable settings.

Assigning “no connect” pins for PCB Editor

In a schematic page, if you leave a pin unconnected, it needs a no connect symbol. You should always connect a no connect symbol to open pins for better readability of the design. The Design Rules Check tool ignores unconnected pins with no connect symbols.

If a pin with a no connect symbol is connected to a net, the no connect symbol has no effect on the pin and becomes invisible. If the pin is later disconnected from the net, the no connect symbol becomes visible again.

The number of pins specified in the PSTCHIP.DAT file must equal the number of pins specified in the PCB Editor footprint. The total number of pins found in PSTCHIP.DAT includes regular pins, power pins, and NC (no-connect) pins if present. If you have numbered through-hole pins or non-electrical pins on the board then you must do one of the following to the part in your design:

- Add a NC property to the part. For the value of the NC property, use the pin numbers of the non-electrical pins separated by commas. For example, if you had an 8-pin footprint with the two through-holes being pins 7 and 8, then you would have a 6-pin part on your design with an NC property containing the value of 7,8.
- Place a No Connect symbol on pins that you don't want to be connected to anything. If you look in the property editor you will see a check for the Is No Connect property on the pin. In the design, you will see an X symbol on the pin. So, for the previous example you would have an 8-pin part in your design with No Connect on pins 7 and 8.

Note: You will get an error message if there are missing pins on a symbol. After adding a No Connect property on a part, use the Update Cache command to update the part in your design (if you realize that the part is missing pin numbers).

- Don't connect any nets to the non-electrical pins on the part. So, in the two options above, you would have an 8-pin part with nothing connected on pins 7 and 8.

Note: Do not do a combination of these three options on the same part or the netlister will issue a fatal error.

Note: All pins that are not connected to a net (whether with a No Connect symbol, or otherwise) appear in the PSTXNET.DAT file, as nets with the name "NC." Therefore, you should avoid the net alias "NC" in your design. The NC property discussed in the first option, above, appears in the PSTCHIP.DAT file in the NC_PINS line rather than being added to the NC net in PSTXNET.DAT/PSTXPRT.DAT. Therefore, all pins connected to the NC net are unconnected on the PC board.

You have to account for unconnected pins of multi-section parts, such as mounting holes of multi-row connectors. To do so, however, you do not want to make the part heterogeneous with the mounting holes as pins on one section or distributed among the sections. Instead, make the part homogeneous and add a NC property to each section of the part, with the same pins listed for the NC property on all sections. In the part editor, you can add an NC property to each part in turn by choosing Previous Part from the View menu and placing the same NC property on all sections.

Note: During netlisting, multi-section, heterogeneous parts are treated as single-section parts.

Assigning "no connect" power pins for PCB Editor

When you take your design to the board, by default, all powers pins will be shorted together (all VCC pins are shorted and all GND pins are shorted). This means that on your board you will need to route all the power pins. In the case of large pin devices (like FPGAs), this can be a tedious and time-consuming task.

To overcome this, you can select the power pins on your design that you want to router and then set all the other power pins as NC pins. This ensures that you then only need to route the power pins that are not set as NC pins.

Since you design may potentially have a large number of schematic folder and pages, Capture allows you to specify the NC pin command for power pins at multiple levels of the design. At the design level, you can view the list of the power pins in the entire design. You can also select and view the power pins at schematic folder level, schematic page level or even down to the level of one or more selected objects on a schematic page.

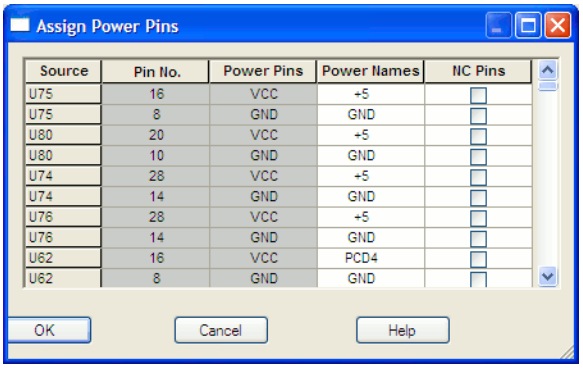
You can only specify the power pin command to invisible power pins.

To specify a power pin as an NC pin at the design, folder or page level

1. In the Project manager select the design, schematic folder or schematic page that contains the power pins you need to set as NC.

2. From the Tools menu choose Assign Power Pins to view the list of invisible power pins.

   The Assign Power Pins dialog displays listing all the invisible power pins in the object (or objects) selected in the Project manager.



   By default, all the pins in the list appear with the NC Pins as checked.

   Note: If the selected object contains no invisible power pins, a warning is displayed in the Session window.

3. To specify a power pin for use on the board, un-check the NC Pins option and click OK.

Note: If you un-check the NC Pin option for a line item in the power pin list, notice that the power name for the pin displays in the Power Names list.

Tip

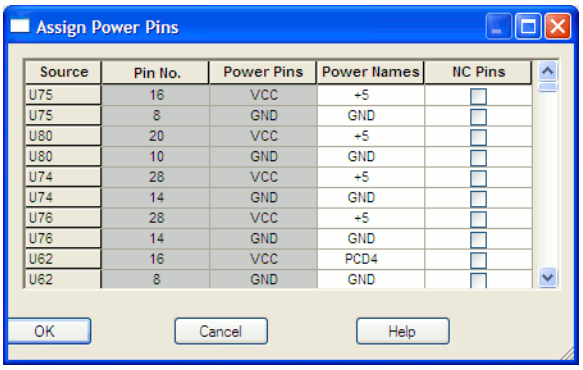
After you specify the NC Pin command for the power pins on a object, open the Property Editor for the object. Notice, the property NC_PINS includes a comma separated list of all NC power pins in the object.

Note: You can also open the Assign Power Pins dialog for objects selected in the Project manager by choosing Browse - Power Pins from the Edit menu. Then select a line item in the power pin list and choose Properties from the Edit menu.

To specify a power pin as an NC pin at the object level in a schematic page

1. Select an object on the schematic page
2. On the schematic page select the object (or objects) that contains the power pins you need to set as NC.
3. Right-click and choose Assign Power Pins to view the list of invisible power pins.

   The Assign Power Pins dialog displays listing all the invisible power pins in the object (or objects) selected on the schematic page.



4. To specify a power pin for use on the board, un-check the NC Pins option and click OK.

Updating the PCB Editor configuration file

The configuration file specifies net, part (function), and component instance and component definition properties. This mapping determines what properties may be netlisted from Capture to PCB Editor or back annotated from PCB Editor to Capture. If a Capture property is not included in the configuration file it is not passed to PCB Editor. Similarly, if an PCB Editor property is not listed in the file, it does not get back annotated to Capture.

The configuration file is divided into four sections, written in a Windows.INI format.

- **ComponentDefinitionProps** PCB Editor component definition properties, output in PSTCHIP.DAT file
- **ComponentInstanceProps** PCB Editor component instance properties, output in PSTXPRT.DAT file
- **netprops** PCB Editor net properties and all pin level properties, output in the PSTXNET.DAT file.
- **functionprops** PCB Editor function properties, output in the PSTXPRT.DAT file

You can have many different configuration files. All you need do is specify which file you want to use in the Setup dialog box.

Using an alias for an old property

You can use an alias in the configuration file to map an old PCB Editor property into a new one. Here are some example PCB Editor properties where this would be appropriate:

Old property name	New property name
ASSIGN_TOPOLOGY	ELECTRICAL_CONSTRAINT_SET
DELAY_RULE	PROPAGATION_DELAY
MATCHED_DELAY	RELATIVE_PROPAGATION_DELAY
TOPOLOGY_TEMPLATE	ELECTRICAL_CONSTRAINT_SET

The TOPOLOGY_TEMPLATE_REVISION property is obsolete and therefore ignored. If you have a previous PCB Editor design that uses DELAY_RULE, for example, you can change the line in the configuration file from

```
PROPAGATION_DELAY=YES
```

to

```
DELAY_RULE = PROPAGATION_DELAY
```

With an alias, you can have two different names for equivalent properties, one for Capture and one for PCB Editor. In the above

example, DELAY_RULE properties get passed into the netlist as PROPAGATION_DELAY properties. You would include one of the above lines or the other in your configuration file. Alternatively, you could modify your design to use PROPAGATION_DELAY rather than DELAY_RULE.

Note: User-defined property names are case sensitive. PCB Editor properties consist of all capitalized letters.

Note: The component definition properties VALUE, ALT _SYMBOL, JEDEC_TYPE, and CLASS are not back annotated since they cannot be changed in PCB Editor.

Note: Do not use NO after the = sign for a property. NO becomes the property alias. If you do not want a property to be passed, you must delete it from the configuration file.

Note: Some properties listed in the configuration file are not applicable in all versions of PCB Editor. Including these properties in the configuration file is not a problem since they would not be used.

Note: A list of typical properties used with PCB Editor may be found in the Capture-PCB Editor filter of the property editor. This filter is built on the PREFPROP.TXT file, which is copied to your Capture directory during installation.

This sample is ALLEGRO.CFG, the default configuration file installed with Capture. In this file, if a value after the = sign were to be other than YES it would specify an alias under which the property will be output instead of its real name.

```
[ComponentDefinitionProps]
ALT_SYMBOLS=YES
CLASS=YES
PART_NUMBER=YES
TOL=YES
VALUE=YES
POWER_GROUP=YES

[ComponentInstanceProps]
GROUP=YES
ROOM=YES
VOLTAGE=YES

[netprops]
```

```
ASSIGN_TOPOLOGY=YES
BUS_NAME=YES
CLOCK_NET=YES
DIFFERENTIAL_PAIR=YES
DIFFP_2ND_LENGTH=YES
DIFFP_LENGTH_TOL=YES
ECL=YES
ECL_TEMP=YES
ELECTRICAL_CONSTRAINT_SET=YES
EMC_CRITICAL_NET=YES
IMPEDANCE_RULE=YES
MATCHED_DELAY=YES
MAX_EXPOSED_LENGTH=YES
MAX_FINAL_SETTLE=YES
MAX_OVERSHOOT=YES
MAX_VIA_COUNT=YES
MIN_BOND_LENGTH=YES
MIN_HOLD=YES
MIN_LINE_WIDTH=YES
MIN_NECK_WIDTH=YES
MIN_NOISE_MARGIN=YES
MIN_SETUP=YES
NET_PHYSICAL_TYPE=YES
NET_SPACING_TYPE=YES
NO_GLOSS=YES
NO_PIN_ESCAPE=YES
NO_RAT=YES
NO_RIPUP=YES
NO_ROUTE=YES
NO_TEST=YES
PROBE_NUMBER=YES
PROPAGATION_DELAY=YES
RELATIVE_PROPAGATION_DELAY=YES
ROUTE_PRIORITY=YES
SHIELD_NET=YES
SHIELD_TYPE=YES
STUB_LENGTH=YES
SUBNET_NAME=YES
TS_ALLOWED=YES
VOLTAGE=YES
VOLTAGE_LAYER=YES
```

```
[functionprops]
GROUP=YES
HARD_LOCATION=YES
NO_SWAP_GATE=YES
NO_SWAP_GATE_EXT=YES
NO_SWAP_PIN=YES
ROOM=YES

[pinprops]
NO_DRC=YES
NO_PIN_ESCAPE=YES
NO_SHAPE_CONNECT=YES
NO_SWAP_PIN=YES
PIN_ESCAPE=YES
```

Assigning pins for swapping in PCB Editor

If you want to do pin swaps in PCB Editor and then back annotate those changes, you must set up the pin properties in Capture first. Pin swap specifications will be produced only if the Swap Id properties are set correctly on pin-swappable parts.

To do this, you can open the part in the library or select the part of interest in your design. Then, from the Edit menu, choose the Part option. From the View menu, choose Package, then from the Edit menu, choose Properties.

In the Properties spreadsheet set the PinGroup value to 1 for each swappable (input) pin of the part. If you have a multi-section part you only have to set the PinGroup value for one section; the part editor adds the same value for all the other sections automatically. For example, on a 7400, set the PinGroup to 1 for pins 1 and 2. Leave the other PinGroup values blank and they are filled in automatically when you click the update all button. (PinGroup = 1 for pins 1, 2, 4, 5, 8, 9, 11, and 12.)

When you select a pin and edit its properties, the value shows as the Swap Id property. The default value is –1, meaning the pin is not swappable. Therefore you must add the PinGroup property to enable pin swapping for your part if you want to be able to swap pins. Swap Id value of 0 and greater than 0 in the property editor mean that the

pin is swappable. If you made a pin swappable, and later decide to remove the swappability of the part, then you just delete the PinGroup property in the property editor. You can see which pins are swappable in the PSTCHIP.DAT file by looking for the PIN_GROUP line under the pin name.

Using the SWAP_INFO property

To enable pin swaps across sections of split (heterogeneous) parts in PCB Editor, a SWAP_INFO property has been introduced in PCB Editor.

Note: In Capture 9.2.3, the SPLIT property provided a method for swapping pins between parts of a heterogeneous package. From Capture 10.0, we recommend that you use the SWAP_INFO property as it provides the same functionality with better features. In Capture 10.5, the SPLIT property has been renamed to SPLIT_INST.

In existing designs, please do not replace the SPLIT property with the SWAP_INFO property. The SPLIT property converts parts as flat parts whereas the SWAP_INFO property leaves the part as a split part. On an existing design, replacing the SPLIT property on a component package with the SWAP_INFO property will change its definition from a flat part to a split part. This will cause component rip-offs in the board file.

The SWAP_INFO property defines a logical group of parts of a package in a heterogeneous (split) part. This allows two pins having the same PIN_GROUP property to be swapped within a logical group, regardless of the physical availability of the pin in the given part of the package.

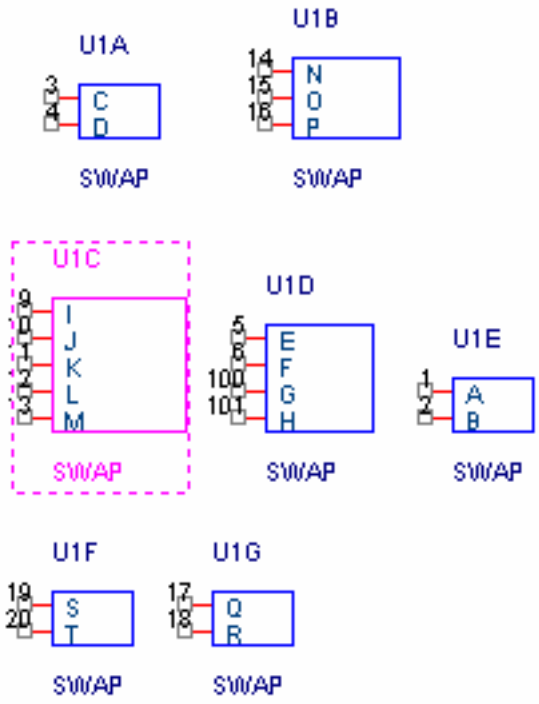
The SWAP_INFO property is defined under the [ComponentDefinitionProps] section in the allegro.cfg file. The swap information is written into body section of the primitive of the pstchip.dat file. PCB Editor reads the SWAP_INFO property in the pstchip.dat file and accordingly allows pin swaps across sections.

Note: If you have a customized PCB Editor configuration file (Allegro.cfg) for your Capture PCB Editor netlister, you need to add

the following entry under the [ComponentDefinitionProps] section in the Allegro.cfg file:

```
[ComponentDefinitionProps]
SWAP_INFO=YES
```

The usage of the SWAP_INFO property is described using a split part.



The above figure shows the example of a heterogeneous (split) part having seven parts-per-package. Let us assume that parts with the reference designators:

- U1A and U1B, form one logical section
- U1C, U1D and U1E, form the second logical section, and
- U1F and U1G, form the third logical section

In this scenario the value of the SWAP_INFO property on all the parts of the package will be defined as:

```
(S1+S2),(S3+S4+S5),(S6+S7)
```

The logical section (S1+S2) indicates that a pin in section S1 is swappable with a pin in section S2, provided they have the same PIN_GROUP value. Therefore, pin 3 of S1 can be swapped with pin 14 of S2 if they have the same PIN_GROUP value.

In a SWAP_INFO syntax, the logical and physical sections are separated by a (+) sign.

Note the following when you use the SWAP_INFO property:

- You must assign the SWAP_INFO property to all parts in the heterogeneous package for which you want to perform pin swapping.
- There must not be any duplicate pins on any of the parts in the heterogeneous package if they are to receive the SWAP_INFO property.
- Ensure that you name the sections as (S1+S2+ S3+…S*n*). If you use any other notation for naming the sections, the SWAP_INFO property will not work.
- The SWAP_INFO property does not function for homogeneous parts. No DRC errors will be reported if the SWAP_INFO property is assigned to a homogeneous part.
- DRC errors will not be reported if there are syntax or semantic errors in the value of the SWAP_INFO property.

Using the SPLIT_INST property

Note: In Capture 10.5, the SPLIT property has been renamed to SPLIT_INST.

The SPLIT_INST property provides a method for swapping pins between parts of a heterogeneous package. You can assign it to a part in a library, or to an instance in a design.

Note: When you assign the SPLIT_INST property to a part at the library or instance level, all lower level occurrences of that part (on the schematic) inherit the property.

The SPLIT_INST property has two possible values: TRUE and FALSE (default). Assigning a value of TRUE to the SPLIT_INST property on the parts of a heterogeneous package indicates that the

netlister treats the package as a flat part, thus allowing pin swapping between the parts of that package.

When you use the SPLIT_INST property, be aware of the following points:

- You must assign the SPLIT_INST property to each part in the heterogeneous package for which you want to perform pin swapping.
- The SPLIT_INST property does not function for homogeneous parts (nor will the Design Rules Check tool detect an error if SPLIT_INST is assigned to a part that is part of a homogeneous package).
- There must not be any duplicate pins on any of the parts in the heterogeneous package if they are to receive the SPLIT_INST property.
- Cross-probing will not function on pins of parts that have the SPLIT_INST property assigned to them. You can work around this by cross-probing the connected nets rather than the pins.

Some of the other pin properties used in Capture for pin and gate swapping are:

NO_SWAP_COMP property

The NO_SWAP_COMP property defined on a component instance ensures that while swapping the component, the symbol associated with the component does not get swapped. This property takes a boolean value. Make sure that you set the value of this property to TRUE.

NO_SWAP_GATE property

The NO_SWAP_GATE property defined on a reference designator or a function designator (gate) specifies the functions within the component that cannot be swapped. The function remains fixed in its current slot in the component. This property takes a boolean value. Make sure that you set the value of this property to TRUE. For more information on this property, see the *Allegro PCB and Package User's Guide*.

NO_SWAP_GATE_EXT property

The NO_SWAP_GATE_EXT property defined on a function designator ensures that the function is not swapped with a function from another component. However, the function can be swapped among slots within its current component. This property takes a boolean value. Make sure that you set the value of this property to TRUE.

NO_SWAP_PIN property

The NO_SWAP_PIN property defined on a reference designator, function designator (gate), or a pin ensures that the pins on the component or function are not swapped either interactively or automatically. This property takes a boolean value. Make sure that you set the value of this property to TRUE.

When you add this property at the instance level in Capture, you need to add the following entry under the [ComponentInstanceProps] section in the Allegro.cfg file:

```
[ComponentInstanceProps]

NO_SWAP_PIN=YES
```

The above entry contains the properties that you add to the components in Capture.

Netlisting to PCB Editor

The Capture netlister generates the board file and three PCB Editor-compatible netlist files:

- PSTCHIP.DAT This file contains a description for each different type of part used in the design. The netlister extracts this information from properties on occurrences.
- PSTXNET.DAT This connectivity file, also referred to as the flat list or expanded net list, contains each net, its properties, its attached nodes, and node properties. The list is ordered by physical net name.
- PSTXPRT.DAT This file, also referred to as the expanded parts list, contains a list of physical parts and lists each reference

designator and the sections assigned to it, ordered by reference designator and section number.

For sample files and details on the file formats, click on the file links above. Also, information about Preparing your design for use with PCB Editor may be helpful in setting up your Capture design for Netlisting to PCB Editor or planning ahead for back annotation once you have completed a board layout in PCB Editor.

You can generate the board file by switching on the Netrev option in the PCB Editor tab of the Create Netlist dialog box.

Note: An error will be generated during netlisting if a part has an invisible power pin and the device property for the part has Power Pins Visible checked.

To access the dialog box from the Tools menu, choose Create Netlist.

Important

The OrCAD Capture product in the OrCAD PCB Designer Basics suite has the following capability limitations for creating a PCB Editor netlist:

- You cannot create a PCB Editor netlist for a design that has more than 500 components and/or 2000 pins.
- The PCB Editor netlister is the only netlister available with this suite.
- High-speed signal flow properties such as, PROPAGATION_DELAY, RELATIVE_PROPAGATION_DELAY, RATSNEST_SCHEDULE, and DIFFERENTIAL_PAIR in your design are not transferred to the PCB Editor board. For more information on high-speed signal flow properties, see Assigning signal flow properties.

The OrCAD PCB Editor Basics product in the OrCAD PCB Designer Basics suite has the following capability limitations:

- Your board can have up to four layers only.
- You cannot save a board that has more than 500 components and/or 2000 pins.

- You cannot save a board, if the design logic imported is more than 500 components and/or 2000 pins.

Note: When you netlist your design, you can choose to open the output board (.brd) file in a layout application immediately after the design is netlisted.

You can choose to open the board in any one of the following layout applications:

- Allegro PCB Editor
- Allegro Package Designer
- Cadence SiP
- OrCAD PCB Editor.

Suppress electrical and netlisting warnings during PCB Editor netlisting

The PCB Editor tab in the Create Netlist dialog contains a Setup button that opens a Setup dialog.

- You can use this dialog to ignore the following electrical warnings during netlisting:
  - PROPAGATION_DELAY
  - RATSNEST_SCHEDULE
  - RELATIVE_PROPAGATION_DELAY
  - DIFFERENTIAL_PAIR
  - NET_SPACING_TYPE
  - NET_PHYSICAL_TYPE
  - ELECTRICAL_CONSTRAINT_SET
  - RATSNEST_SCHEDULE
  - VOLTAGE
  - MIN_LINE_WIDTH
  - MIN_NECK_WIDTH
  - MATCHED_DELAY

- You can also choose to suppress netlist (ALG*) warnings during netlist. To do this you need to enter the warning (for example ALG0051) you want to suppress in the Suppress Warnings text box and click Add to add the warning to list of warnings to be suppressed.

Cross probing and cross selection between Capture and PCB Editor

After creating the board file, you place and route the board. This includes placing the parts in PCB Editor/Allegro SI/PCB Editor, APD and routing the nets. Sometimes, you may also require to swap pins or sections/functions to make routing easier. You can select the components from the Select elements for placement list in the Placement dialog box and then place them directly on the board. You can also place the components directly from the Capture schematic design. This feature is called cross probing. Between Capture and PCB Editor, there are two cross probing functions: *cross highlighting* and *cross selection*.

Cross probing between PCB Editor and Capture uses Intertool Communication (ITC). In Capture, you make this connection by selecting the Miscellaneous tab of the Preferences dialog box. You can reach this dialog box from the Options menu by choosing the Preferences menu item.

Note: The cross probe function works only in the Interactive Place mode of PCB Editor.

Note: Both the backslash (\ ) and underscore (_) characters in net names interfere with cross probing. Also, the design name must not contain period (**.**).

Cross highlighting between Capture and PCB Editor

Cross highlighting applies to three different types of objects: parts, nets and pins. Here are the general rules of cross probing:

- If PCB Editor is in highlight mode, you can select an object in PCB Editor, and the corresponding logical element in Capture is highlighted.

- If PCB Editor is in dehighlight mode, when you dehighlight a physical object, the corresponding logical element is dehighlighted in Capture. Deselecting an element in Capture dehighlights the corresponding element in PCB Editor.
- In Capture, when you select a component, its corresponding physical part is only highlighted in PCB Editor *if you are in PCB Editor highlight mode*. Otherwise, selection in Capture has no effect in PCB Editor, unless you are using cross selection.

The following tables show how highlighting and dehighlighting work between the two tools.

Selecting in Capture	Result in PCB Editor
Select a part	Highlights the corresponding component
Select a wire	Highlights all trace segments in the net
Select a pin	Highlights the corresponding pad

Deselecting in Capture	Result in PCB Editor
Deselect a part	Dehighlights the corresponding component
Deselect a wire	Dehighlights all trace segments in the net
Deselect a pin	Dehighlights the corresponding pad

Highlighting in PCB Editor	Result in Capture
Highlight a component	Highlights all parts in the corresponding package
Highlight a net	Highlights the entire corresponding flat net
Highlight a pad	Highlights the corresponding pin

Dehighlighting in PCB Editor	Result in Capture
Dehighlight a component	Dehighlights all parts in the corresponding package
Dehighlight a net	Dehighlights the entire corresponding flat net
Dehighlight a pad	Highlights the corresponding pin

Cross selecting between Capture and Allegro PCB Editor

If you are placing parts in PCB Editor (using the *Manually* option from the Place menu) then select one or more parts in Capture and the corresponding parts will be selected in the Placement dialog box in PCB Editor. This option is only available when PCB Editor is active (running) and Intertool Communication (ITC) is enabled in Capture.

Important

If you select a part/pin/signal in PCB Editor that has been deleted from Capture design, a warning message will be printed in the Session log of Capture.

Note: The cross probe function works only in the Interactive Place mode of PCB Editor.

To initiate cross probing between Capture and PCB Editor

1. In Capture, from the Options menu, choose Preferences. Capture displays the Preferences dialog box.
2. Select the Miscellaneous tab.
3. Activate the Enable Intertool Communication option.
4. Click OK.
5. When you export the netlist for your design into PCB Editor, cross-probing will be enabled.

Note: The cross probe function works only in the Interactive Place mode of PCB Editor.

Locking Components during Cross-Probing

When you cross probe between Capture and PCB Editor, you need to keep selecting components in your design to place them on your board.

In many cases, you create elaborate design with a large number of components and intricate connectivity. So when you keep selecting the components and nets on your design, you might inadvertently shift a component. This shift, in some cases, might even cause issues of connectivity.

To avoid shifting a component during the cross-probe operation, you can temporarily lock the component. This ensures that the component is locked to the canvas and cannot be moved.

However, this is a temporary locking operation and the lock status of the object is lost as soon as you click anywhere on the page or on another object. To create a persistent lock on a component you need to use the Graphical Operation (GOp) Locking feature in Capture.

Back annotation from PCB Editor

The Back Annotate dialog box appears when you choose Back Annotate from the Tools menu after selecting the design folder of a Capture project. The back annotation process generates a Capture-compatible swap file, which is based on the differences between the logical view (PST*.DAT netlist files) and the physical view (*VIEW.DAT files of board changes).

You use back annotation to synchronize the design file with the changes done in the board file. Changes in the PCB Editor board need to be back annotated to the Capture schematic to ensure the physical board design is consistent with the logical schematic design.

The Back annotation process includes the following steps:

1. Generating feedback files (*VIEW.DAT files) - A utility called genfeedformat generates board file information in four files named compview.dat, pinview.dat, netview.dat, and funcview.dat. These four files are also called *VIEW.DAT files.
2. Generating PCB Editor netlist files (PST* files) - Capture- PCB Editor netlister generates netlist files (PST* files) again. This step

is necessary to check if any changes are made in the Capture design after board file creation.

3. Generating the swap file (.swp file) - Capture-PCB Editor netlister runs in the Feedback mode and generates the swap files by comparing netlist files with feedback files.

4. Updating the design with swap information - Capture updates the design based on the information in the swap file.

While generating *VIEW.DAT files, the PCB Editor Export Logic utility (genfeedformat.exe) uses the pxlBA.txt file to decide which properties need to be written into the *VIEW.DAT files. The pxlBA.txt sets up the properties that are back annotated from the PCB Editor board file.

When you create an PCB Editor netlist (forward mode), the pxlBA.txt file is generated and is stored in the same location as the PST*.DAT files. When you back annotate a design (backward mode), the pxlBA.txt file is generated again and is stored in the same location as the .BRD file (board file).

If PCB Editor is not installed on the same system as Capture, you can use the Export Logic command of PCB Editor on the system where PCB Editor is installed. By default, PCB Editor picks the pxlBA.txt file from the location where the board file resides. If the pxlBA.txt file does not exist at the board file location, PCB Editor picks it from the standard PCB Editor installation path, which is <PCB Editor_Installation_Dir>/share/pcb/text/views. However, this pxlBA.txt file may not have all the properties that you want to back annotate to Capture and some of the properties may get annotated as deleted or with a null value. To avoid this problem, you must copy the pxlBA.txt file generated by Capture to the board file location, before running the Export Logic command from PCB Editor.

PCB Editor back annotation includes property changes, additions and deletions; changes to part reference designators; and gate (function) and pin swaps. Here are some details:

Pin swaps

Interchanges two pin numbers. For example, pin 6 could become pin 9. Pin 9 would become pin 6 in the process. On the board, the net is just routed to a different pin, since the order of the pins on the physical IC cannot be changed. On the schematic, the pin numbers will visually switch places.

Gate swaps

Switches or interchanges two gates, or functions. For example, a 74LS00 has four NAND gates: U1A, U1B, U1C, and U1D. You can swap U1A with U1B or any other of the NAND gates in the package.

Reference changes

You can change reference designators, U1 to a value of ST1, for example. If the part is a multi-package, then U1A through U1D, would become ST1A through ST1D.

Properties defined or changed in PCB Editor are back annotated to Capture, provided the properties are listed in the configuration file.

Just as occurrence values are always used in the PCB Editor netlist, these values are also the ones replaced or updated in the back annotation process. Instance values are neither netlisted nor back annotated unless the instance value is the same as the occurrence value.

If you double-click on the part to invoke the part editor on the schematic page the occurrence values are the ones in the yellow rows below the instance values (white rows).

Property changes

Back annotation from PCB Editor only uses CHANGEREF and PINSWAP format lines in the .SWP file for pin and gate swaps and reference designator changes. The properties are back annotated in a separate section.

If a net name is renamed in the physical design (on the PCB Editor board) and net properties are added or edited, the net name does not back annotate to Capture, even though the properties do.

To get around this naming discrepancy between the physical layout and schematic designs, you should rename the net in Capture, then netlist the design to PCB Editor. The net names then correspond and properties may be passed without a problem.

Setup button

Click this button to open the Setup dialog box where you can set up, edit and view information about the configuration file used for netlisting and back annotating property information between Capture and PCB Editor. You can also specify the number of backup files to keep in your design directory.

Generate Feedback Files

Select this option to generate the *VIEW.DAT back annotation files from the specified PCB Editor Board File. These files are listed under the project manager. Selecting this option is equivalent to using the Export Logic command in PCB Editor.

This option is only available if you have PCB Editor installed.

If this option is unselected, then make sure the * VIEW.DAT files are saved in the same directory as PST*.DAT netlist files for your design.

PCB Editor Board File

Accept the path and file listed or navigate to the PCB Editor board (.BRD) file that contains previously-imported netlist information and the design changes you want to back annotate. This is the same board file used to create feedback files (*VIEW.DAT files) need for generating the .SWP file during back annotation.

By default, the name of your design (with a .BRD extension) in the allegro subfolder is used, unless you have run a previous back annotation. In this case, the field contains the file previously entered. If the file in this field is not valid, back annotation cannot proceed and Capture issues an error message.

Back annotation from PCB Editor only uses CHANGEREF and PINSWAP format lines in the .SWP file for pin and gate swaps and reference designator changes. The properties are back annotated in a separate section.

Browse to the directory where you have your PST*.DAT files. This is also the location where the * VIEW.DAT files will be placed after being extracted from the board.

Netlist Directory

The default directory is the allegro subfolder for your design. If you have run a previous back annotation on the current .DSN design, the netlist directory for that back annotation is the default. A netlist directory must be specified for back annotation to proceed.

It is critical that the original design not be modified before attempting to back annotate. Otherwise, errors can result when comparing the netlist files with the *VIEW.DAT board files.

Output File

Specifies the path and file name for the .SWP file that is saved after back annotation. By default the file name is DESIGN_NAME.SWP unless you have previously run a back annotation on the current design. In this case the default output file is the name given to the previous output file.

Back Annotation

Update Schematic. Select this option if you want the Capture schematic design to be updated with back annotation information from the .SWP file. Selecting this check box lets you review the back annotation details. This option is selected by default.

If you don't select this check box, you can still use the Layout tab later to back annotate the generated .SWP file to Capture. You might choose this option, for example, if you wanted to view the SWP file before actually back annotating. In this case, you can also select the check box later in the Allegro tab when you rerun the back annotation.

View Output (.SWP) File. Select this option if you want the .SWP file to be automatically opened and available for viewing and editing in a Capture text window after the .SWP file is generated. You can also close the file and re-open it from the project manager. This check box is not selected by default.

Note: PCB Editor back annotation allows you to do the following:

- Perform more than one back annotation in a row without netlisting in-between, once you have made an initial netlisting.
- Netlist occurrence values for user-added properties.

- Back annotate parts with added connections or properties that are not used, including unwired parts and those that could be used in the future.
- Back annotate properties and their values to components, pins, and nets using a configuration file.
- Back annotate numeric and alphabetic reference designators for multi-section parts.
- Check the Capture session log for errors

Best practices for Capture-PCB Editor design flow process

Best practices for Capture design for PCB Editor

- Avoid using parenthesis " ( ) " in schematic names. If you still want to use parenthesis in schematic name then make sure that you map it with a valid character while generating a netlist and do reverse mapping while generating a .swp file.
- While defining a net list alias or a net name:
  - Keep the maximum length of a net name or alias up to 31 characters.
  - Do not use lower case or special characters in a net name.
- Avoid using "Power Pins Visible" property at design level.
- Use net to connect pins
  - Leave room for assigning a net name. Pin-to-pin connection changes the net name when a user moves a component
- Run the Capture DRC command before generating PCB Editor netlist.
- Set path for PCB Editor footprint before running Netrev.
- Do not use {GROUP} as property name in combined property strings. This may cause problems while annotating your design for a PCB Editor tool, like Allegro. The GROUP property is used in Allegro for a specific purpose.

- Do not use a part in your design, which does not contain a logical pin and contains only a power pin. You will not be able to create an Allegro netlist for the design.
- Capture allows you to assign the SIGNAL_MODEL property and pass it to the back-end tool. However, you cannot use it to create XNets. You can create XNets only in Allegro PCB Editor.

Best practices for smooth back annotation

- Do not change design name, hierarchical block names, or reference designators in Capture after board files creation
- Do not edit a part from schematic in Capture after board file creation
- Do not replace cache as it changes the Source library name and part name, in capture
- Do not change the values of component definition properties in capture after board files creation
- Capture does not support electrical constraint sets (ECSets). ECSets will not be back annotated to your Capture design
- Do not change Design file/root schematic/hierarchical block names in Capture after board file creation
- Do not add or delete components to or from the schematic design immediately after the board file creation. Add or delete components after finishing the back annotation process
- Do not add any additional components in PCB Editor. Instead, add components in Capture and take them to PCB Editor
- Do not add, rename, or delete a net in PCB Editor
- Do not change the format for reference designators for parts in PCB Editor as <Alphabet(s)><Numeric><Alphabet(s)> or <Alphabet(s)>-<Alphabet(s)>
- Run PCB Editor Dbdoctor before running Back annotation by selecting the Database Check command from the Tools menu in PCB Editor
- Make backups of the original design before updating the design with the swap information in Capture

- Back annotate the design immediately after making the board file. Though it's not a mandatory step, back annotating the design before placing components helps avoid problems in back-annotation at a later stage.

Note: During back annotation, if you encounter Error *[ALG0037] Unable to read physical netlist data.* The probable reasons for this error are:

- Netlist files not found.

Or

- Unable to read the netlist file because either the path name is long or has spelling errors.

If back annotation at this stage generates an empty swap file, you can proceed with placing and routing the board file. In case any problems are detected, you must correct them in the design file and generate the board file again until an empty swap file is generated.

Design reuse models

Design reuse is the capability of defining and using design modules, in both the Capture and PCB Editor layout environments, that are compatible between both of these PCB tools. You can create modules for reuse in your design in either the Capture schematic or PCB Editor physical layout part of the design process.

Creating a reuse design

In Capture, a reuse module is either a library (.OLB) part or an externally referenced schematic design (.DSN). If the module is externally-referenced it can be a complete physical PCB design laid out on a board. Also, the corresponding schematic design will have been converted to a reuse module in Capture, which is done by choosing the Generate Reuse Module option in the PCB Editor reuse tab of the Annotate dialog box.

In PCB Editor, the source of a design reuse module is the Capture netlist. This netlist contains a set of reuse properties that are used to identify and group each of the packages within the module. After

placing and routing the board in PCB Editor, you can save the design as a reuse module by creating an MDD file

Creating and modifying multi-level reuse designs

When creating a multi-level schematic design in which you embed successive levels of reuse modules, you must take care to ensure you preserve the reuse design. In general, modifying properties from the root level of a design is *not* a problem unless the property causes a component change at a lower level.

For example, say you have a three-level design called HIGH.DSN. HIGH.DSN references MID.DSN which is a reuse module, and MID.DSN references LOW.DSN which is also a reuse module.

If you want to make design modifications that will result in changes in connectivity—such as adding or modifying a component or editing instance properties—then you must edit lower level designs first before you can see the changes reflected at higher levels. Occurrence properties however, may be changed at any level in a referenced schematic without modifying the source design. Consider the following two design scenarios. The first is a component change but the second only changes occurrence properties.

- Scenario A—Modifying LOW.DSN by adding a series terminating resistor

  a. First, open the LOW.DSN design and make the change. Afterwards, netlist the design to PCB Editor and update the PCB Editor board and reuse module from within PCB Editor.

  b. Open MID.DSN and, again, netlist the revised design with connectivity changes to PCB Editor. In PCB Editor, read in the revised LOW physical module and update the MID board and physical module.

  c. Open HIGH.DSN and generate the netlist for PCB Editor. Once the design is in PCB Editor, refresh the instances of the MID reuse module.

- Scenario B—Changing a Reference Designator in LOW.DSN from U1_1 to U444

  In this case, all you have to do is modify the higher-level occurrence tree for the component that is located in LOW.DSN.

The next time you take the netlist from HIGH.DSN into PCB Editor the individual component will get its Reference Designator updated.

Note: Except for occurrence properties, the schematics of externally-referenced libraries and designs should not be edited. You should view them as read-only designs. Trying to edit, then save, these designs from within your schematic can introduce errors such as duplicate reference designators and other problems.

When saving schematics with externally-referenced libraries or designs, occurrence properties are saved but altered instance values are not. If you want to change externally-referenced libraries or designs you should first close the referencing design. Then, open the referenced library or design, make the necessary changes, and save and close the referenced library or design. At this point, you can reopen the original design and reference the modified design.

Reuse properties

Capture assigns reuse properties to identify and distinguish the reuse parts used in simple hierarchical and complex hierarchical designs. These properties ensure that part packaging is preserved and references are renumbered in such a way that they do not conflict with each other.

REUSE_ID

This property is added to every part in a reuse design. Within a reuse design there are as many values of this property as there are packages so that each package has a unique REUSE_ID. All parts in a package have the same REUSE_ID value. Capture assigns these property values when you enable the Generate Reuse Module in the PCB Editor reuse tab of the Annotate dialog box.

REUSE_PID

If a reuse module contains another reuse module as part of its external design, then the netlister assigns a REUSE_PID value to every component in each package of the external design. The value of the REUSE_PID is the *same as* the value of the component's previous REUSE_ID. A new REUSE_ID value is then assigned to each module. This way, occurrences of the same module will have different REUSE_IDs on them, but the same REUSE_PIDs for corresponding components. Using REUSE_IDs, makes it possible for Capture to propagate changes to lower levels of a reuse module.

REUSE_NAME

The default value of the REUSE_NAME property, assigned by the netlister, is a concatenation of the design name and the schematic name coupled by an underscore character. Here is an example:

```
testmodule_schematic1
```

The REUSE_NAME property is propagated down throughout the design hierarchy to all parts below.

This value is computed by the netlister and added to the netlist. The value of this property is unique for each usage, or instance, of a reuse module. A design may have one REUSE_NAME value but many REUSE_INSTANCE values.

REUSE_INSTANCE

The REUSE_INSTANCE property is obtained from the name of the referencing hierarchical part. If a REUSE_INSTANCE property is not present, it is created as follows:

```
< REUSE_NAME >_<document ID of the referencing
hierarchical part>
```

Like the REUSE_NAME property, the REUSE_INSTANCE property is propagated down throughout the design hierarchy to all parts below.

REUSE_MODULE

PCB Editor assigns this property as a unique name to identify a physical reuse module. The property corresponds to placed and routed board in PCB Editor (.BRD file) which has been saved as an .MDD file. If this property is user-defined in Capture, it specifies the reuse module to use in PCB Editor.

To create a reuse design

1. In Capture, create the schematic that will become your reuse design.

   You can use the project wizard to set up your schematic and build the design from scratch or use library components.

2. Perform a design rules check (DRC) by selecting the .DSN file in the project manager, then choosing the Design Rules Check command from the Tools menu. This action checks for disconnected nets, no connects, off-grid objects, packaging problems, duplicate part references and other types of errors.

3. Annotate the design by choosing the Annotate command from the Tools menu. Select the Packaging tab of the Annotate dialog box and check appropriate options.

   If you do not plan to make any design changes in PCB Editor that would affect the netlist skip to step 7. Otherwise, proceed to the next step.

   Note: In step 7 there are two options you can check in the PCB Editor reuse tab Generate Reuse Modules and Renumber Design for Using Reuse Modules. By checking both of these options, you can generate a reuse design *and* annotate it at the same time, saving yourself extra steps.

4. Generate an Allegro netlist by choosing the Create Netlist command from the Tools menu; select the PCB Editor tab in the Create Netlist dialog box. Complete the appropriate options in the dialog box. Either enable the Create or Update PCB Editor Board (Netrev) option to open a .BRD design in PCB Editor during netlisting or import the netlist into PCB Editor by choosing the Import Logic command in PCB Editor.

5. In PCB Editor, place and route the physical design, then export the design logic to Capture.

6. In Capture, back annotate design changes from PCB Editor by selecting the .DSN file and choosing the Back Annotate command from the Tools menu. The Backannotate dialog appears. Select the appropriate options in the Allegro tab of the Backannotate dialog box.

7. From the Tools menu, choose the Annotate command. In the PCB Editor reuse tab of the Annotate dialog enable the Generate Reuse Module option to create a reuse module from the design.

   This step adds a unique REUSE_ID property for each package. You can view these properties in the Property editor window.

8. Netlist the design to PCB Editor, and create an .MDD reuse module in PCB Editor from the schematic reuse design.

   You complete the module creation in PCB Editor by selecting the Create Module command from the Tools menu. You are prompted to select the extents of the module and pick an origin. By doing so, you have designated an PCB Editor Module Definition File (.MDD).

   Note: See the PCB Editor online Help documentation for how to create a physical design reuse module in PCB Editor from a placed-and-routed board.

9. Repeat steps 1 through 8, as necessary, for multiple levels of design in a design reuse hierarchy.

10. Use the reuse module in a Capture design, either as a library part or as a hierarchical block.

Note: When creating design reuse modules, it is a good idea to avoid making multiple-page schematics (with off-page connectors). When trying to descend the hierarchy of a referenced design, such as a reuse module, you cannot choose which page gets opened.

Using a reuse design

Once you have generated a reuse module in Capture, you can use it in one of two ways, either by:

- Placing the module as an external design schematic (.DSN file) using the Place Hierarchical Block dialog box;

or

- Placing the module as a library part (.OLB file) using the Place Part dialog box if the part was created with the Generate Part command in Capture.

You can use a design reuse module either as an .OLB part from a library or as an external .DSN design, placed as a hierarchical block.

To place a reuse design which was created as library part

1. From the Place menu, choose the Part command. The Place Part dialog box appears.
2. Locate and select the .OLB part previously saved as a reuse design. For more information, see Searching for a part in the libraries.
3. Click OK. An image of the part is attached to the pointer.
4. Move the part image and click the left mouse button to place the part.
5. For each instance property of the part you want to place, repeat step 4.
6. Press the ESC key or select another tool to dismiss the part that's attached to the pointer.

Note: When you place a part off-grid, it remains off-grid through any cut-and-paste and drag-and-drop operations.

Note: If you place parts so that two pins meet end to end, the pins are connected.
OrCAD recommends that you connect the pins of the parts using a wire, and avoid placing parts so that two pins meet end to end. This is because, parts with direct pin to pin connections produce a system generated net name to establish the connection and:

- Capture will not allow you to assign your own net name in the place of the system generated net name.
- Searching for the system generated net name can be difficult if you are not aware of the pin to pin connection.
- If you move the parts after creating the netlist, the system generated net name might change. This may cause net name conflicts when you run backannotation.

Note: OrCAD recommends that you do not connect a power symbol directly to a power pin. Connect the power symbol to the power pin using a wire.

Note: You can place a part in the middle of a wire segment without redrawing the wire by placing the part over the wire such that two pins on the part connect with the wire segment. Then click the left mouse button over the part with the TAB key pressed until just the overlapping wire segment is selected. Finally, delete the wire segment.

Shortcut

Tool palette:

To place a reuse module as a hierarchical block

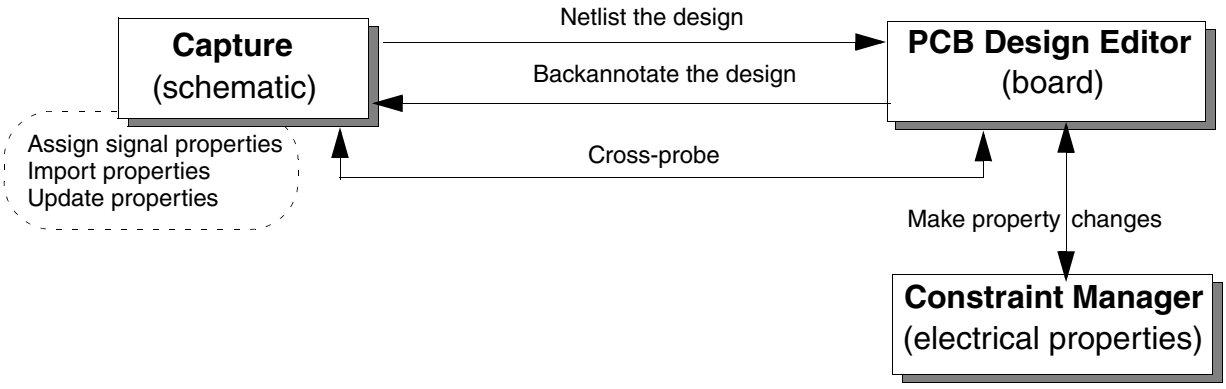
1. In Capture, place a hierarchical block on a schematic page by choosing the Hierarchical Block command from the Place menu. Reference the reuse module as an external design.
2. Annotate the design by choosing the Annotate command from the Tools menu.
3. Select the PCB Editor Reuse tab and enable the Renumber Design For Reuse Modules option. Complete the other options in the PCB Editor Reuse tab, then click OK.

Note: After placing the reuse module, if you want to synchronize your Capture schematic with its corresponding PCB Editor .MDD equivalent, you must regenerate an PCB Editor netlist from Capture. In PCB Editor, you can either update the PCB Editor board or re-import the netlist onto the PCB Editor board. This action ensures the reuse properties are incorporated into the physical reuse module. The module can now be used in any schematic or physical design as a reuse module.

Assigning signal flow properties

Modern designs often operate at sub-nanosecond edge rates. At such speed, it often becomes important to resolve timing issues early in the design cycle. When coupled with the need to reduce time-to-market, solving high-speed issues requires early identification, analysis and specification often in the schematic design phase itself. Capture is now enhanced to process high speed

electrical constraints and take them through a complete front-to-back flow.



Note: To enable cross-probing between OrCAD Capture and Constraint Manager, enable highlighting in PCB Editor. When you highlight a component in PCB Editor, PCB Editor sends cross-probing messages to OrCAD Capture. You can disable cross-probing messages in Capture by deselecting Enable Intertool Communication under Intertool Communication in the Miscellaneous tab of the Preferences dialog box.

Capture supports graphical and manual entry for assigning the following high-speed signal properties to nets:

- PROPAGATION_DELAY—This property defines the minimum and maximum propagation delay constraint between any pair of pins in a net. By assigning this property to nets, you can make the router restrict the length of interconnect to meet timing margin. This property often is best applied to a common clock sourced designed bus.

- RATSNEST_SCHEDULE—This property specifies the type of ratsnest calculation that Constraint Manager performs on the net.

  By using the RATSNEST_SCHEDULE property, you can meet a balance between time margin and noise margin. Based on your design need, you can define the configuration as MIN_TREE, MIN_DAISY_CHAIN, SOURCE_LOAD_DAISY_CHAIN, FAR_END_CLUSTER or STAR. You would find this property useful in defining the placement of receiver or driver in multi-drop buses and asynchronous signals.

- RELATIVE_PROPAGATION_DELAY—This property is an electrical constraint attached to pin-pairs on a net. It specifies a group of pin-pairs that are required to have interconnect propagation delays matching a specified delta (offset) and tolerance with respect to the target pin pair. A RELATIVE_PROPAGATION_DELAY group has a pin-pair against which all other pin-pairs in the group are compared. You can apply the RELATIVE_PROPAGATION_DELAY property to a source synchronous bus design, such as DDR interfaces.
- DIFFERENTIAL_PAIR—This property represents a pair of flat nets that will be routed in a way that the signals passing through them are opposite in sign with respect to the same reference. This ensures that any electromagnetic noise in the circuit is cancelled out.

Note: For more information about the function of signal properties, see the Cadence *Allegro Platform Properties Reference* documentation.

Note: The signal flow properties that are added in the Flat Nets tab in Capture 10.3 and later versions can be transferred to the design in Capture 10.0 (Service Pack 2) or earlier versions. To do this, open the design in Capture 10.3 or later version and select the Flat Nets Properties option in the Export Properties dialog box. Capture creates an export file (*.exp*). Now, from Capture 10.0 (Service Pack 2) or earlier version, choose the Import Properties command from the Tools menu and specify the *.exp* file in the Import Properties dialog box.

Note: In the case of flat designs, you can use the Schematic Nets or the Flat nets tab of the Property editor to manually edit the high-speed signal properties.

Understanding the Signal Property Flow

1. Make a schematic
2. Assign signal properties

   Use one of the following procedures:

   - Specifying the PROPAGATION_DELAY property on page 611

- Specifying the RELATIVE_PROPAGATION_DELAY property on page 614
- Specifying the RATSNEST_SCHEDULE property on page 618
- "Specifying the DIFFERENTIAL_PAIR property" on page 618

3. (Optional) Import properties

   If you have properties recorded in a text file in a previous session in the Property Editor, you can import those properties.

4. (Optional) Update properties

   If you have a large design and want to avoid manual property assignment, you can update properties using the update property text file.

5. Export properties

   It is a good practice to export properties to a text file. These files can be used for archival purpose and as backup in the unlikely event of accidental data corruption or deletion.

6. Perform a design rule check on the design.
7. Netlist the design
8. Open PCB Design Editor and launch Constraint Manager.

   a. Open the board file in the PCB Editor.

   b. Click *Setup - Electrical Constraint Spreadsheet* to open the Constraint Manager.

   c. Expand the *Routing* spreadsheet.

   d. Select the *Min/Max Propagation Delays* tab to view the `PROPAGATION_DELAY` property or the Relative Propagation delay tab to view the `RELATIVE_PROPAGATION_DELAY` property.

   e. Select the *Wiring* tab to view the `RATSNEST_SCHEDULE` property. This property appears in the *Schedule* column in the *Topology* section.

9. Backannotate property changes

If you make any signal property changes in Constraint Manager, you need to backannotate those changes to Capture.

a. Open the board file in the PCB Editor and open the Constraint Manager.

b. Make the desired property changes in Constraint Manager.

c. In Capture, select *Tools - Back Annotate.*

The Backannotate dialog box appears.

d. Select the Allegro tab, set different backannotation options and click *OK*.

The Progress window reports the details of backannotation.

e. Open the Property Editor and verify any changes.

Limitations of the signal property flow

The signal property flow has the following limitations:

- You cannot define extended nets.
- You cannot use multi match group power.

Specifying the PROPAGATION_DELAY property

1. Double-click the net where you want to assign the `PROPAGATION_DELAY` property.

   The Property Editor window appears.

2. Select the *Filter* as *Allegro_Signal_Flow_Routing*.

3. Select the *Flat Nets* tab.

   Based on the grid-settings, rows or columns corresponding to different properties appear.

4. Select the grid corresponding to the `PROPAGATION_DELAY` property.

5. Select the Edit menu and choose the Invoke UI command or press the CTRL+U shortcut keys.

The Propagation Delay dialog box appears.

Note: Alternatively, you can right-click on the grid corresponding to the PROPAGATION_DELAY property and select the Invoke UI command from the pop-up menu.

Note: You can also manually enter values in the grids corresponding to the PROPAGATION_DELAY property. After you enter a value in the PROPAGATION_DELAY property grid and click the Apply button, Capture performs syntax validation and if there is a syntax violation, the property is not applied and the details of the violation are appended to the Session Log.

Tip

You can use the shortcut keys CTRL+C and CTRL+V to perform standard copy/paste operations in the PROPAGATION_DELAY property grids.

Tip

You can populate multiple consecutive or nonconsecutive grids of the PROPAGATION_DELAY property at the same time. To do this, select the grids you want to populate and press the CTRL+E shortcut keys. The Edit Property Values dialog box appears. Specify the value that you want to be populated across all the selected grids in the dialog box.

6. To create a new pin-pair, click the *Add Pin Pair* ( ) button or press the ALT+A shortcut keys.

   The Create Pin Pairs dialog box appears. Select the first pin for the pin-pair, then select the second pin, and click *OK.*

   A pin-pair is created. The new pin-pair appears as a row in the Propagation Delay dialog box. You can define constraints for it.

Tip

You can use the following methods to select multiple consecutive pins in the Create Pin Pairs dialog box:

- Using SHIFT+Down Arrow keys
- Using SHIFT+Left mouse button click

- Dragging the mouse pointer diagonally across the pins appearing in the combo box to select them

Similarly, you can use the CTRL+Left mouse button click to select multiple nonconsecutive pins in the Create Pin Pairs dialog box.

7. To specify the pin-pair, select one of the following options in the *Pin Pair* field.

   - Longest/Shortest pin-pair(L:S)—To apply minimum delay to the shortest pin-pair and maximum delay to the longest pin-pair.
   - Longest/Shortest Driver/Receiver(D:R)—To apply minimum delay to the shortest driver/receiver pin-pair and maximum delay to the longest driver/receiver pin-pair.
   - All Drivers/All Receivers(AD:AR)—To apply Min/Max constraints to all driver/receiver pin-pairs.

8. Enter a value specifying the minimum allowable propagation delay/length for the pin-pairs in the *Min* field.

9. To specify the unit for minimum constraint, select one of the following options in the *Min Rule* field:

   - `DELAY` in `ns`
   - `%MANHATAN`
   - `LENGTH` in mills `(mils)`, micron (`um`), millimeter (`mm`), centimeter (`cm`), and inches (`in`)

10. Enter a value specifying the maximum allowable propagation delay/length for the pin-pairs in the *Max* field.

11. Specify the unit for the maximum constraint by selecting unit value in the *Max Rule* field. The options are:

    - `DELAY` in `ns`
    - `%MANHATAN`
    - `LENGTH` in mills `(mils)`, micron (`um`), millimeter (`mm`), centimeter (`cm`), and inches (`in`)

12. Click OK in the Propagation Delay dialog box. The PROPAGATION_DELAY property is seeded in the PROPAGATION_DELAY grid for the corresponding column.

13. Click the Apply button in the Property Editor to apply the PROPAGATION_DELAY property on the nets. Moreover, if you have manually entered the PROPAGATION_DELAY syntax, then Capture performs syntax validation and appends any syntax violations to the Session Log.

Note: To delete an existing pin-pair, select the left-most cell of the pin-pair row and click the *Delete Pin Pair* ( ) button or press the ALT+D shortcut keys.

Note: You can use the User Properties dialog box to assign the PROPAGATION_DELAY property to all the bits of a bus at the same time. Make sure that you use the correct syntax for specifying a value for the PROPAGATION_DELAY property. The syntax is:

```
<Pin_pair>:<min_value>:<max_value>
```

The pin-pairs can only be:

- L:S
- D:R
- AD:AR

Specifying the RELATIVE_PROPAGATION_DELAY property

1. Double-click the net where you want to assign the RELATIVE_PROPAGATION_DELAY property.

   The Property Editor window appears.

2. Select the *Filter* as *Allegro_Signal_Flow_Routing*.

3. Select the *Flat Nets* tab.

4. Select the grid corresponding to the RELATIVE_PROPAGATION_DELAY property.

5. Select the Edit menu and choose the Invoke UI command.

   The Relative Propagation Delay dialog box appears.

Note: Alternatively, you can right-click on the grid corresponding to the RELATIVE_PROPAGATION_DELAY property and select the Invoke UI command from the pop-up menu or press the CTRL+U shortcut keys.

Note: You can also manually enter values in the grids corresponding to the RELATIVE_PROPAGATION_DELAY property. After you enter a value in the RELATIVE_PROPAGATION_DELAY property grid and click the Apply button, Capture performs syntax validation and if there is a syntax violation, the property is not applied and the details of the violation are appended to the Session Log.

Tip

You can use the shortcut keys CTRL+C and CTRL+V to perform standard copy/paste operations in the RELATIVE_PROPAGATION_DELAY property grids.

Tip

You can populate multiple consecutive or nonconsecutive grids of the RELATIVE_PROPAGATION_DELAY property at the same time. To do this, select the grids you want to populate and press the CTRL+E shortcut keys. The Edit Property Values dialog box appears. Specify the value that you want to be populated across all the selected grids in the dialog box.

6. To specify the pin-pair, select one of the following options in the *Pin Pair* field.
   - *Longest/Shortest pin-pair*—To apply minimum delay to the shortest pin-pair and maximum delay to the longest pin-pair.
   - *Longest/Shortest Driver/Receiver*—To apply minimum delay to the shortest driver/receiver pin-pair and maximum delay to the longest driver/receiver pin-pair.
   - *All Drivers/All Receivers*—To apply Min/Max constraints to all driver/receiver pin-pairs.
7. Select the scope as global or local. Select the scope as `global` to define the RELATIVE_PROPAGATION_DELAY property between different nets of same match group. Select the scope as

`local` to define the `RELATIVE_PROPAGATION_DELAY` property between different pin-pairs of same net.

8. Enter the relative value from the target net that all nets in the group should match in the *Delta* field.

9. To specify the unit for delta, select *Delay* in `ns` or *Length* in mills `(mils)`, micron (`um`), millimeter (`mm`), centimeter (`cm`), and inches (`in`) in the *Delta Units* field.

10. Enter a value that specifies the maximum allowable propagation delay/length for the pin-pairs in the *Tolerance* field.

11. To specify the unit for Tolerance, select one of the following options in the *Tol. Units* field:

    - `%`
    - DELAY (`ns`)
    - LENGTH (`mils, mm, cm, in`)

12. To create a new pin-pair, click the *Add Pin Pair* ( ) button or press the ALT+A shortcut keys.

    The Create Pin Pairs dialog box appears.

13. Select the first pin for the pin-pair, then select the second pin, and click *OK.*

    A pin-pair is created. The new pin-pair appears as a row in the Propagation Delay dialog box. You can define constraints for it.

Tip

You can use the following methods to select multiple consecutive pins in the Create Pin Pairs dialog box:

- Using SHIFT+Down Arrow keys
- Using SHIFT+Left mouse button click
- Dragging the mouse pointer diagonally across the pins appearing in the combo box to select them

Similarly, you can use the CTRL+Left mouse button click to select multiple nonconsecutive pins in the Create Pin Pairs dialog box.

14. To delete an existing pin-pair, select the pin-pair row by clicking its left-most cell.

15. Click the *Delete Pin Pair* ( ) button or press the ALT+D shortcut keys.

16. To set a pin-pair as the target net, select the pin-pair row and click the *Set Target* ( ) button or press the ALT+S shortcut keys.

17. To delete the target status from a pin-pair, select the pin-pair row and click the *Delete Target* ( ) button or press the ALT+T shortcut keys.

18. To change the match group:

    - Select a group from the list box.
    - Type a new match group name.

    Note: Based on the match group selected, all nets contained in it will display in the *Nets Attached* box.

19. Click OK in the Relative Propagation Delay dialog box. The `RELATIVE_PROPAGATION_DELAY` property is seeded in the `RELATIVE_PROPAGATION_DELAY` grid for the corresponding column.

20. Click the Apply button in the Property Editor to apply the `RELATIVE_PROPAGATION_DELAY` property on the nets. Moreover, if you have manually entered the RELATIVE_PROPAGATION_DELAY syntax, then Capture performs syntax validation and appends any syntax violations to the Session Log.

Note: You can use the User Properties dialog box to assign the `RELATIVE_PROPAGATION_DELAY` property to all the bits of a bus at the same time. Make sure that you use the correct syntax for specifying a value for the `RELATIVE_PROPAGATION_DELAY` property. The syntax is:

For the target pin-pair:

```
<match_group>:<scope>:<pin-pair>::
```

where `<pin-pair>` has the following syntax:

```
<pin1>:<pin2>
```

For non-target pin-pairs:

`<match_group>:<scope>:<pin-pair>:<delta>:<tolerance>`

The pin-pairs can only be:

- AD:AR
- L:S
- D:R

Specifying the RATSNEST_SCHEDULE property

To specify the `RATSNEST_SCHEDULE` property:

1. Select the grid corresponding to the `RATSNEST_SCHEDULE` property.
2. Choose any of the following values:
   - MIN_TREE—Indicates that the net rat should be displayed with the minimum spanning tree algorithm. This can form Ts at pins.
   - MIN_DAISY_CHAIN—Indicates that a minimum length daisy-chain schedule is formed.
   - SOURCE_LOAD_DAISY_CHAIN—Indicates that a source-to-load ECL daisy-chain schedule is used.
   - FAR_END_CLUSTER—Automatically places a single Tpoint in a schedule at a calculated location.
   - STAR—Specifies a ratsnest similar to `FAR_END_CLUSTER` without the Tpoint added.

Note: For more information about the `RATSNEST_SCHEDULE` property, see Cadence document *Allegro Platform Properties Reference.*

Specifying the DIFFERENTIAL_PAIR property

To specify the DIFFERENTIAL_PAIR property for flat nets:

1. Right-click the design in the project manager and select Edit Object Properties. The Property Editor window appears.

2. Click the Flat Nets tab at the bottom in the Property Editor window.
3. Select the first flat net for which you want to create a differential pair.
4. Select the grid corresponding to the DIFFERENTIAL_PAIR property and specify a name for the differential pair.
5. Select the second flat net for which you want to create a differential pair.
6. Specify the same differential pair name you specified for the first net.
7. Click the Apply button. A differential pair between both the nets is created.

   Note: For more information about the DIFFERENTIAL_PAIR property, see Cadence document *Allegro Platform Properties Reference.*

Creating differential pairs between flat nets

In addition to creating a differential pair using the DIFFERENTIAL_PAIR property in the property editor, you can use the Create Differential Pair command to create a differential pair between two flat nets in your design. You can also modify or delete a differential pair from your design.

To create a differential pair

1. In the project manager, click the design file (.dsn) or a schematic page file.
2. Select the Tools menu and choose the Create Differential Pair command. The Create Differential Pair dialog box appears.
3. Select the Net option, if not already selected, from the drop-down list. All the flat nets in your design appear in All Nets column in a sorted order (all net names starting with a numeric character will be displayed first and then all net names starting with an alphabet).

   Note: To view nets of a particular type, specify the initial letters of the net in the Filter text box. All the nets of that particular type

will appear in the All Nets column. For example, if you want to view all nets starting with the letter “A”, then enter “A” in the Filter text box. All the nets starting with letter “A” will appear in the All Nets column.

4. Select a net from the All Nets column and click the button or double-click the net. The selected net appears in the Selections column.

5. Repeat step 4 for the second net. Now, both the nets appear in the Selections column.

To create a differential pair you must have two nets.

You can use the CTRL or SHIFT keys to move multiple nets to the Selections column.

To remove a net from the Selections column, select a net and click the button.

Note: In case, you add a net for which you do not want to create a differential pair and want to revert back, double-click the net in the Selections column. The net is removed from the Selections column, but is available in your design.

6. Specify a name for the differential pair in the Diff Pair Name text box.

7. Click the Create button. The differential pair is created between the selected nets. The differential pair name appears in the Selections column adjacent to the net’s name.

   Note: If the selected nets are not of the same type (for example, a power net and a non-power net) or they differ in the total number of pins in each selected net, then a message appears asking you to confirm the creation of a differential pair between the selected nets.

8. Click the Close button to close the Create Differential Pair dialog box.

For steps on how to create a differential pair using the property editor, see "Specifying the DIFFERENTIAL_PAIR property" on page 618.

Note: The `DIFFERENTIAL_PAIR` property column is automatically updated with the differential pairs you create using the Create Differential Pair dialog box.

Note: An Auto Differential pair can also be created for a bus. To do so, you need to put _n_ & _p_ as prefix and the Auto command creates differential pairs for all bits in the bus.

To view a differential pair

1. Select the Differential Pair option from the drop-down list. All the differential pairs you created in your design appear in Diff Pairs column.

Tip

To view differential pairs of a particular type, specify the initial letters of the differential pairs in the Filter text box. All the differential pairs of that particular type will appear in the Diff Pairs column. For example, if you want to view all differential pairs starting with the letter "DP", then enter "DP" in the Filter text box. All the differential pairs starting with letter "DP" will appear in the Diff Pairs column.

2. Select a differential pair from the Diff Pairs column and click the (>) button or double-click the differential pair. The Selections column will display the name of the two nets associated with the selected differential pair.

Tip

You can use the CTRL or SHIFT keys to move multiple differential pairs to the Selections column and view the nets associated with the selected differential pairs.

3. Click the Close button to close the Create Differential Pair dialog box.

To modify a differential pair

1. Select the Differential Pair option from the drop-down list. All the differential pairs you created in your design appear in Diff Pairs column.
2. Select the differential pair you want to modify from the Diff Pairs column and click the (>) button or double-click the differential pair. The selected differential pair along with the associated nets appears in the Selections column.

   Note: In case, you select a wrong differential pair for modification and want to revert back, double-click the differential pair in the Selections column. The differential pair is removed from the Selections column, but is available in your design.
3. Specify a new name for the differential pair in the Diff Pair Name text box.
4. Click the Modify button. The new differential pair name is assigned to the selected nets.
5. Click the Close button to close the Create Differential Pair dialog box.

To delete a differential pair

1. Select the Differential Pair option from the drop-down list. All the differential pairs you created in your design appear in Diff Pairs column.
2. Select the differential pair you want to delete from the Diff Pairs grid and click the (>) button. The selected differential pair along with the associated nets appear in the Selections column.

   Note: If you accidentally selected the wrong differential pair for deletion and want to revert back, double-click the nets in the Selections column. The differential pair is removed from the Selections column, but is available in your design.
3. Click the Delete button. The differential pair set on the selected nets is deleted.

   Note: When you click the Delete button, the differential pair is deleted from the Selections column and the Diff Pairs column.

4. Click the Close button to close the Create Differential Pair dialog box.

Creating differential pairs between multiple pairs of flat nets simultaneously

Instead of creating differential pairs between two nets individually, you can quickly create differential pair between multiple pairs of flat nets simultaneously.

To create multiple differential pairs simultaneously

1. In the Create Differential Pair dialog box, click the Auto Setup button The Differential Pair Automatic Setup dialog box appears displaying all the flats nets and the corresponding differential pairs in the All Nets column.

Tip

To view nets of a particular type, specify the initial letters of the net in the Filter text box. All the nets of that particular type will appear in the All Nets column. For example, if you want to view all nets starting with the letter “A”, then enter “A” in the Filter text box. All the nets starting with letter “A” will appear in the All Nets column.

2. Specify a string (numeric or alphabet) that you want to precede the differential pair name. For example, if you specify “A” in the Prefix text box, then all the differential pair names that will be created will be preceded with “A”.

3. Specify the last digit of the first net’s name in the + Filter text box. For example, all net names ending with 1.

4. Specify the last digit of the second net’s name in the - Filter text box. For example, all net names ending with 4.

5. Click anywhere inside the Differential Pair Automatic Setup dialog box.

   Capture displays a list of all differential pairs that can be created between all the nets that qualify the criteria set in the + Filter and - Filter text boxes. Also, the Differential Pair Name is preceded with the prefix specified in the Prefix text box.

The +Net and -Net grid displays the two nets associated with a differential pair.

Note: If you do not want a specific differential pair to be created, select the row containing the differential pair and click the Remove button or double-click the row containing the differential pair. The selected row disappears.

Note: If the nets forming a differential pair are of the type DP+ and DP-, the name of the differential pair is set to DP. For other pairs of nets, the name of the differential pair is of the type DPn.

6. Click the Create button. All the differential pairs displayed in the Selections column are created. For information on how to view the differential pairs, see "To view a differential pair" on page 621.

7. Click the Close button to close the Differential Pair Automatic Setup dialog box and go back to the Create Differential Pair dialog box.

List of Unsupported Capture-PCB Flow field values

You should avoid the use of the following special characters when defining **pin names**, **net names** or **signal names** in the Capture - PCB Editor flow:

- leading or trailing white spaces
- ! (exclamation mark)
- ' (single-quote)

Netlist Formats (Other Netlists)

Capture supports a number of other netlists formats. You can use these formats during netlisting by accessing the Other tab in the Create Netlist dialog.

This section describes the restrictions that are enforced in the nomenclature of different objects when using these netlist formats.

Wirelist

Netlist Condition	Error / Warning
Part Name should be less than or equal to 29 characters in length.	Warning: Name is too long
Part Reference should be less than or equal to 9 characters in length.	Warning: Reference is too long
Pin Number should be less than or equal to 7 characters in length.	Warning: Name is too long
Pin Name should be less than or equal to 15 characters in length.	Warning: Name is too long

Tango

Valid Object name Character Set:

+_/\\{}<>.‘~!@#$%^&*=? 0-9 a-z A-Z

Netlist Condition	Error / Warning
Part Name should be less than or equal to 16 characters in length.	Warning: Name is too long
Part Reference should be less than or equal to 16 characters in length.	Warning: Name is too long

Netlist Condition	Error / Warning
Signal Name should be less than or equal to 16 characters in length.	Warning: Name too long

cadNetix

Netlist Condition	Error / Warning
Part Name should be less than or equal to 17 characters in length.	Warning: Name is too long
Signal Name should be less than or equal to 16 characters in length.	Warning: Name too long
Sum of the characters of Pin Number and Part Reference should be less than or equal to 11.	Warning: Reference plus Pin Number is too long

calay/calay90

Netlist Condition	Error / Warning
Part Name should be less than or equal to 19 characters in length.	Warning: Name is too long
Part Reference should be less than or equal to 19 characters in length.	Warning: Name too long
Signal Name should be less than or equal to 8 characters in length.	Warning: Name too long

Netlist Condition	Error / Warning
Signal Name should contain only valid characters Valid Character Set: _, -, 0-9, a-z, A-Z	Warning: Name contains illegal characters.

orcbds/orcompvisn

Netlist Condition	Error / Warning
Signal Name should be less than or equal to 20 characters in length.	Warning: Name too long
Signal Name should contain only valid characters Valid Character Set: /, -, 0-9, a-z, A-Z	Warning: Name contains illegal characters.

eedesign

Netlist Condition	Error / Warning
Part Reference should be less than or equal to 8 characters in length.	Warning: Name too long

future

Netlist Condition	Error / Warning
Part Name should be less than or equal to 16 characters in length.	Warning: Name too long

hilo

Netlist Condition	Error / Warning
Signal Name should be less than or equal to 14 characters in length.	WARNING: Name is too long

mentor

Netlist Condition	Error / Warning
Part Reference should be less than or equal to 19 characters in length.	WARNING: Name is too long
Part Name should be less than or equal to 19 characters in length.	WARNING: Name is too long

multiwir

Netlist Condition	Error / Warning
Signal Name should be less than or equal to 16 characters in length.	WARNING: Name is too long
Sum of the characters of Pin Number and Part Reference should be less than or equal to 31.	WARNING: Reference plus Pin Number is too long

ohdlnet

Netlist Condition	Error / Warning
Signal Name should contain only valid characters Valid Character Set: / - 0-9 a-z A-Z **Note:** If a net name consists entirely of a dash, no warning will be given.	WARNING: Name contains illegal characters

padspcb

Netlist Condition	Error / Warning
Part Reference should be less than or equal to 16 characters in length.	WARNING: Name is too long

Netlist Condition	Error / Warning
Signal Name should be less than or equal to 47 characters in length.	WARNING: Name is too long
Part Reference should contain only valid characters Valid Character Set: ~ ! # $ % _ - = + | / . : ; <> 0-9 a-z A-Z	WARNING: Name contains illegal characters
Signal Name should contain only valid characters Valid Character Set: ~ ! # $ % _ - = + | / . : ; <> 0-9 a-z A-Z	WARNING: Name contains illegal characters

pcad

Netlist Condition	Error / Warning
Signal Name should be less than or equal to 14 characters in length.	WARNING: Name is too long

pcadnlt

Netlist Condition	Error / Warning
Signal Name should contain only valid characters Valid Character Set: +-_$ 0-9 a-z A-Z	WARNING: Name contains illegal characters

pcbii

Netlist Condition	Error / Warning
Signal Name should be less than or equal to 8 characters in length.	WARNING: Name is too long
Part Name should be less than or equal to 8 characters in length.	WARNING: Name is too long
Part Reference should be less than or equal to 8 characters in length.	WARNING: Reference is too long
Pin Number should be less than or equal to 4 characters in length.	WARNING: Name is too long
Signal Name should contain only valid characters Valid Character Set: ~ ‘ ! @ # $ % ^ & * _ - + = [ ] | ’ : ; / > < . 0-9 a-z A-Z	WARNING: Name contains illegal characters

Scicards

Netlist Condition	Error / Warning
Part Name should be less than or equal to 17 characters in length.	WARNING: Name is too long
Signal Name should be less than or equal to 16 characters in length.	WARNING: Name is too long

Netlist Condition	Error / Warning
Sum of the characters of Pin Number and Part Reference should be less than or equal to 11.	WARNING: Reference plus Pin Number is too long

Vectron

Netlist Condition	Error / Warning
Part Reference should be less than or equal to 8 characters in length.	WARNING: Reference is too long
Signal Name should be less than or equal to 12 characters in length.	WARNING: Name is too long

Pads2k

Netlist Condition	Error / Warning
Part Reference should be less than or equal to 16 characters in length.	WARNING: Reference is too long
Signal Name should be less than or equal to 47 characters in length.	WARNING: Name is too long
Reference should contain only valid characters Valid Character Set: ~ ! # $ % _ - = + | / . : ; < > 0-9 a-z A-Z	WARNING: Name contains illegal characters

Netlist Condition	Error / Warning
Signal Name should contain only valid characters Valid Character Set: ~ ! # $ % _ - = + | / . : ; < > 0-9 a-z A-Z	WARNING: Name contains illegal characters

PADSPWRP

Netlist Condition	Error / Warning
Part Reference should be less than or equal to 6 characters in length.	WARNING: Reference is too long
Signal Name should be less than or equal to 47 characters in length.	WARNING: Name is too long
Reference should contain only valid characters Valid Character Set: ~ ! # $ % _ - = + | / . : ; < > 0-9 a-z A-Z	WARNING: Name contains illegal characters
Signal Name should contain only valid characters Valid Character Set: ~ ! # $ % _ - = + | / . : ; < > 0-9 a-z A-Z	WARNING: Name contains illegal characters

PROTEL2

Valid Object name Character Set:

+_/\\{}<>.‘~!@#$%^&*=? 0-9 a-z A-Z’

Netlist Condition	Error / Warning
Part Reference should be less than or equal to 12 characters in length.	WARNING: Reference is too long
Footprint should be less than or equal to 32 characters in length.	WARNING: Footprint is too long

WINBOARD

Netlist Condition	Error / Warning
Signal Name should be less than or equal to 24 characters in length.	WARNING: Name is too long
Signal should contain only valid characters Valid Character Set: ~ ‘ ! @ # $ % ^ & * _ - + = [ ] | ’ : ; / > < . 0-9 a-z A-Z	WARNING: Name contains illegal characters

EDIF

Valid Object name Character set

_, 0-9, a-z, A-Z

pcadnlt

Valid Object name Character set

+ - _ $ 0-9 a-z A-Z

Spice

Netlist Condition	Error / Warning
Signal should contain only valid characters Valid Character Set: _ $ 0-9 a-z A-Z	WARNING: Name contains illegal characters

vstmodel

Netlist Condition	Error / Warning
Signal names must begin with one of the following prefixes: 'P', 'L', 'N' or '*P', '*L', '*N' or '~P', '~L', '~N' or "or have the name: 'IPL', 'IPH', 'ONE' or 'ZERO'.	ERROR: Illegal signal name

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Designing for other EDA applications

Capture is fully compatible with a number of other EDA tools, including PCB Editor, OrCAD Express, OrCAD PSpice, and NCVHDL. If you plan to use your Capture design in conjunction with one or more of these tools, you should keep certain guidelines in mind.

Designing for PCB Editor

Capture and PCB Editor can communicate directly using intertool communication (ITC), or indirectly using netlist and report files. Cross probing displays the corresponding parts and nets between Capture and PCB Editor.

Netlists and report files communicate design information changes between PCB Editor and Capture. Use these files to create new boards in PCB Editor, and to annotate designs in both PCB Editor and Capture.

For more information about using PCB Editor, see the online help for PCB Editor.

Note: In PCB Editor, if you modify properties on a net, which does not have a corresponding physical object (also called invisible nets) in Capture, the modified properties will not be imported during backannotation. The error messages are displayed in the sessions log.

Cross probing for PCB Editor

After creating the board file, you place and route the board. This includes placing the parts in PCB Editor/Allegro SI/PCB Editor, APD and routing the nets. Sometimes, you may also require to swap pins or sections/functions to make routing easier. You can select the components from the Select elements for placement list in the Placement dialog box and then place them directly on the board. You can also place the components directly from the Capture schematic design. This feature is called cross probing. Between Capture and PCB Editor, there are two cross probing functions: *cross highlighting* and *cross selection*.

Cross probing between PCB Editor and Capture uses Intertool Communication (ITC). In Capture, you make this connection by selecting the Miscellaneous tab of the Preferences dialog box. You can reach this dialog box from the Options menu by choosing the Preferences menu item.

Note: The cross probe function works only in the Interactive Place mode of PCB Editor.

Note: Both the backslash (\ ) and underscore (_) characters in net names interfere with cross probing. Also, the design name must not contain period (**.**).

Cross highlighting between Capture and PCB Editor

Cross highlighting applies to three different types of objects: parts, nets and pins. Here are the general rules of cross probing:

- If PCB Editor is in highlight mode, you can select an object in PCB Editor, and the corresponding logical element in Capture is highlighted.
- If PCB Editor is in dehighlight mode, when you dehighlight a physical object, the corresponding logical element is dehighlighted in Capture. Deselecting an element in Capture dehighlights the corresponding element in PCB Editor.
- In Capture, when you select a component, its corresponding physical part is only highlighted in PCB Editor *if you are in PCB Editor highlight mode*. Otherwise, selection in Capture has no effect in PCB Editor, unless you are using cross selection.

The following tables show how highlighting and dehighlighting work between the two tools.

Selecting in Capture	Result in PCB Editor
Select a part	Highlights the corresponding component
Select a wire	Highlights all trace segments in the net
Select a pin	Highlights the corresponding pad

Deselecting in Capture	Result in PCB Editor
Deselect a part	Dehighlights the corresponding component
Deselect a wire	Dehighlights all trace segments in the net
Deselect a pin	Dehighlights the corresponding pad

Highlighting in PCB Editor	Result in Capture
Highlight a component	Highlights all parts in the corresponding package
Highlight a net	Highlights the entire corresponding flat net
Highlight a pad	Highlights the corresponding pin

Dehighlighting in PCB Editor	Result in Capture
Dehighlight a component	Dehighlights all parts in the corresponding package
Dehighlight a net	Dehighlights the entire corresponding flat net
Dehighlight a pad	Highlights the corresponding pin

Cross selecting between Capture and Allegro PCB Editor

If you are placing parts in PCB Editor (using the *Manually* option from the Place menu) then select one or more parts in Capture and the corresponding parts will be selected in the Placement dialog box in PCB Editor. This option is only available when PCB Editor is active (running) and Intertool Communication (ITC) is enabled in Capture.

If you select a part/pin/signal in PCB Editor that has been deleted from Capture design, a warning message will be printed in the Session log of Capture.

Note: The cross probe function works only in the Interactive Place mode of PCB Editor.

To initiate cross probing between Capture and PCB Editor

1. In Capture, from the Options menu, choose Preferences. Capture displays the Preferences dialog box.
2. Select the Miscellaneous tab.
3. Activate the Enable Intertool Communication option.
4. Click OK.
5. When you export the netlist for your design into PCB Editor, cross-probing will be enabled.

Note: The cross probe function works only in the Interactive Place mode of PCB Editor.

Creating a new PCB Editor project from a Capture design

You can bring Capture netlist information into PCB Editor by choosing the Create or Update PCB Editor Board option in the Create Netlist dialog box. To update an existing board, you need to select the board in the Input Board File box. If the board file is open when you update the netlist file, PCB Editor automatically displays a dialog box asking if you want to load the new netlist file. If the board file is not open

when the netlist changes, PCB Editor prompts you to load the modified netlist when you re-open the board file.

To forward annotate information from Capture to PCB Editor

1. In the Capture project manager, select the design for which you are going to create a netlist.
2. From the Tools menu, choose the Create Netlist command.
3. In the Create Netlist dialog box, choose the PCB Editor tab.
4. In the Input Board File box, enter a name for the input file using a .BRD file extension.
5. In the Output Board File box, enter a name for the output file using a .BRD file extension.
6. Click OK to close the Create Netlist dialog box and create the .BRD file.

Note: Yellow triangles in the ratsnest indicate unrouted, zero-length connections (connections that lead directly from a pad on the top layer to a pad on the bottom layer). These connections need to be routed using a via.

Preparing a Capture design for PCB Editor

Preparing a design for PCB Editor is similar to designing any other design flow. The steps involved in preparing a Capture design for use with PCB Editor:

1. Preparing libraries
2. Placing components and wiring them up
3. Annotating the design
4. Assigning properties (attributes)

The first step in preparing a design is to prepare a design library. When you prepare a design library, you must ensure that you have added all PCB Editor related properties to the design.

PCB Editor has a predefined set of default properties for different components, functions, nets, and pins. You can add custom

properties to this default set by defining them in PCB Editor using the Property Definitions command, accessed from PCB Editor's Setup menu. In order for any property to be passed from Capture to PCB Editor, the property name must be found in Updating the PCB Editor configuration file specified from the Setup dialog box in Capture. So, if you add a custom property in PCB Editor, you must also add the property in Capture as well as in the configuration file.

How properties are netlisted from Capture to PCB Editor

Not all properties in Updating the PCB Editor configuration file show up as properties in PCB Editor. Some of these properties are used in generating portions of the netlist PST*.DAT files.

In PCB Editor, component properties (package properties in Capture) take precedence over function properties (part properties in Capture). So in the netlist, a package property value is used if both a part and package have values for the same property. Capture always uses the occurrence values in the netlist.

Package (component) properties, which are found in the PSTCHIP.DAT andPSTXPRT.DAT netlist files, can be viewed in PCB Editor using the Show Element command on a component. For example, PCB Editor has defined VALUE as a Component Definition property so it appears under this heading in the Show Element dialog box. Other properties such as CLASS or JEDEC_TYPE are also listed.

Part (function) properties are found in the PSTXPRT.DAT file and can appear as Component Definition properties if they are predefined in PCB Editor and if you list them in the [ComponentDefinitionProps] section of the configuration file. Function properties are listed in the [functionprops] section of the configuration file.

Net properties appear in the PSTXNET.DAT/PSTXPRT.DAT file under the NET_NAME section.

Preparing libraries for Capture to PCB Editor flow

Capture supports two types of components that can be added to a library, single-section packages and multi-section packages. A single-section package contains a single logical part in it, while a

multi-section consists of multiple logical parts. A multi-section package can be further categorized as:

- Homogenous package - If all the logical parts in a package are identical except for the pin names and pin numbers, the package is homogeneous.
- Heterogeneous package - If the logical parts in a package have different graphics, pin numbers, or properties, the package is heterogeneous.

Similarly, PCB Editor also supports two types of components, single-section parts and multi-section parts. Single section parts consist of only single sections, while multi-section parts consist of multi-sections which can be categorized as:

- Symmetrical parts - This part consists of a package that has the same logical pin list across all the sections/functions of the package.
- Asymmetrical parts - This part consists of a package that has a different logical pin list across all the sections of the package.
- Split parts - This part consists of a package in which pins are split across multiple sections. You may split a large-sized part that may not fit in a single schematic page into multiple sections based on your specifications and can place different sections in different schematic pages. You may also want to partition a large part based on its functionality and use sections individually. For example, you may like to create different sections for pins with same voltage rating.

The basic difference between an asymmetrical and split part is that a split part does not have any relation among its sections where an asymmetrical part has common pins across multiple sections.

Note: Logical pinlist: A unique set of pin names on each part per package is called the logical pinlist of the part.

Note: Physical pinlist: A list of physical pin numbers associated with logical pin names.

Single-section parts in PCB Editor map to single-section packages in Capture. Symmetrical parts in PCB Editor map to homogeneous packages in Capture, while asymmetrical parts and split parts both map to heterogeneous packages.

Besides the difference in types of components they support, Capture and PCB Editor also differ the way they read component information. Capture understands component information in .OLB format, whereas PCB Editor understands these in a specific file format - PSTCHIP.DAT, which is a readable ASCII file. The PSTCHIP.DAT file contains information about the different components used in a particular design. This file is generated by the Capture-PCB Editor Netlister from a design file.

Guidelines for preparing libraries for Capture-PCB Editor flow

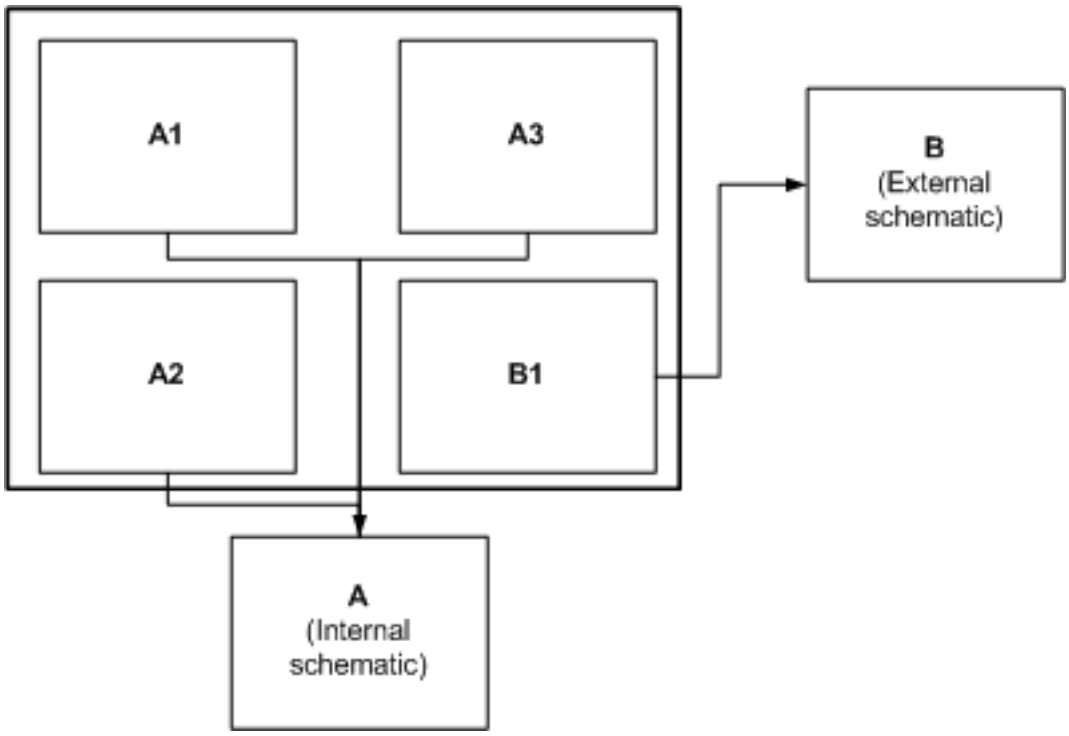
- Limit part and pin names to 31 characters.
- Use only upper case characters for part/symbol names, reference designators, and pin names
- Do not use special characters to assign part names, reference designators, or pin names
- Do not use duplicate names for pins other than power pins
- For multiple power pins with the same pin name, do not make some pins as visible and others as invisible
- Do not use “0” as a pin number

Design reuse for PCB Editor

Capture provides functionality that lets you reuse packaging and annotation information from your schematic when you rout your PCB (in the form of a PCB Editor .BRD file).

The basic concept is that you can use a the annotation information particular schematic, whether internal to the design, or as an external reference, multiple times in your PCB Editor design, and all the part

references and packaging information will be duplicated correctly with each occurrence of the reuse design in the .BRD file. Consider this example:



Suppose a design consists of multiple occurrences of two schematics:

- Schematic A is an internal schematic (that is, a schematic that is part of the design, and appears in the project manager as a folder)
- Schematic B is an external design (a schematic that is referenced by the design but that is not part of the design)

Schematic A has three occurrences in the design: A1, A2, and A3. Schematic B has one occurrence, B1. If you specify each of these schematics as “reuse schematics,” when Capture annotates the design, packaging information is assigned to parts in the design such that part packaging is contained within each occurrence of the reuse schematic.

So, in this example, when you annotate the design in Capture, no parts in A1 would share packaging with parts from A2 or A3, etcetera.

To create a reuse design

1. In Capture, create the schematic that will become your reuse design.

   You can use the project wizard to set up your schematic and build the design from scratch or use library components.

2. Perform a design rules check (DRC) by selecting the .DSN file in the project manager, then choosing the Design Rules Check command from the Tools menu. This action checks for disconnected nets, no connects, off-grid objects, packaging problems, duplicate part references and other types of errors.

3. Annotate the design by choosing the Annotate command from the Tools menu. Select the Packaging tab of the Annotate dialog box and check appropriate options.

   If you do not plan to make any design changes in PCB Editor that would affect the netlist skip to step 7. Otherwise, proceed to the next step.

   Note: In step 7 there are two options you can check in the PCB Editor reuse tab Generate Reuse Modules and Renumber Design for Using Reuse Modules. By checking both of these options, you can generate a reuse design *and* annotate it at the same time, saving yourself extra steps.

4. Generate an Allegro netlist by choosing the Create Netlist command from the Tools menu; select the PCB Editor tab in the Create Netlist dialog box. Complete the appropriate options in the dialog box. Either enable the Create or Update PCB Editor Board (Netrev) option to open a .BRD design in PCB Editor during netlisting or import the netlist into PCB Editor by choosing the Import Logic command in PCB Editor.

5. In PCB Editor, place and route the physical design, then export the design logic to Capture.

6. In Capture, back annotate design changes from PCB Editor by selecting the .DSN file and choosing the Back Annotate command from the Tools menu. The Backannotate dialog appears. Select the appropriate options in the Allegro tab of the Backannotate dialog box.

7. From the Tools menu, choose the Annotate command. In the PCB Editor reuse tab of the Annotate dialog enable the Generate Reuse Module option to create a reuse module from the design.

   This step adds a unique REUSE_ID property for each package. You can view these properties in the Property editor window.

8. Netlist the design to PCB Editor, and create an .MDD reuse module in PCB Editor from the schematic reuse design.

   You complete the module creation in PCB Editor by selecting the Create Module command from the Tools menu. You are prompted to select the extents of the module and pick an origin. By doing so, you have designated an PCB Editor Module Definition File (.MDD).

   Note: See the PCB Editor online Help documentation for how to create a physical design reuse module in PCB Editor from a placed-and-routed board.

9. Repeat steps 1 through 8, as necessary, for multiple levels of design in a design reuse hierarchy.

10. Use the reuse module in a Capture design, either as a library part or as a hierarchical block.

Note: When creating design reuse modules, it is a good idea to avoid making multiple-page schematics (with off-page connectors). When trying to descend the hierarchy of a referenced design, such as a reuse module, you cannot choose which page gets opened.

Designing for PSpice

You can use your Capture design with PSpice. The sections that follow describe how you can use a design created in Capture with PSpice.

Associating PSpice model to a Capture symbol

You can associate a PSpice model to an existing Capture symbol using the Model Import wizard.

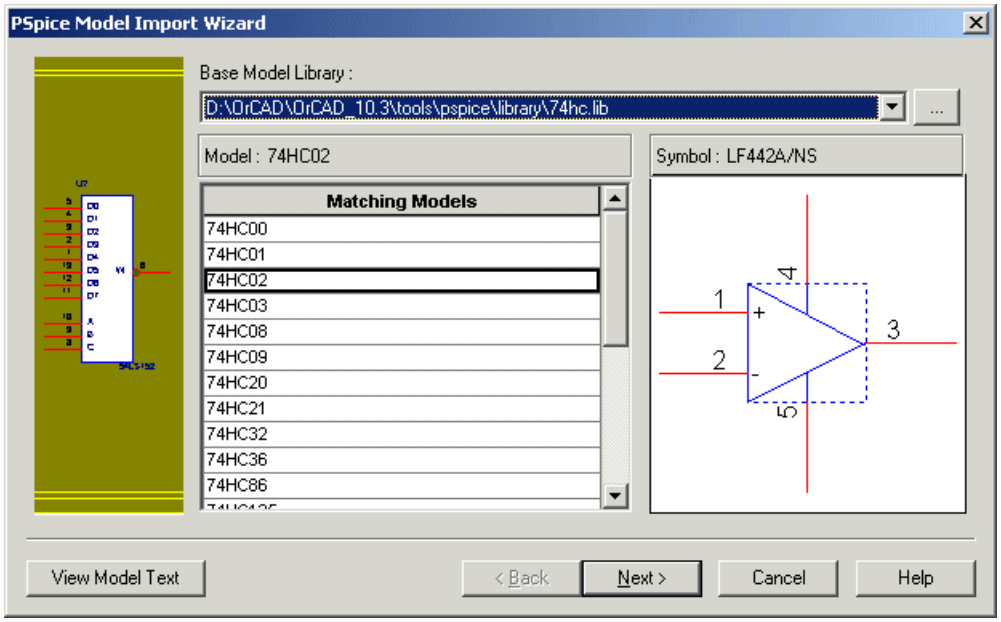
To associate a PSpice model to an existing Capture symbol

1. Open the library (`.OLB`) containing the symbol for which PSpice model is required.
2. Select the Tools menu and choose the Associate PSpice Model command.

   or

   Right-click on the library file and select Associate PSpice Model from the pop-up menu.

   The Model Import Wizard appears.



Note: If the symbol is open in Capture, the Associate PSpice Model command will appear disabled in the pop-up menu.

Important

If the selected symbol in the `.OLB` file has a Convert view, it will be ignored by the Model Import wizard. The PSpice model gets attached to the symbol in the normal view.

Caution

If you are reusing any existing symbol, you might get an warning stating that the Implementation property is already defined. Ignore the warning and click OK.

3. Specify the name and location of the library containing the required PSpice model.

   You can either select the library from the Base Model Library drop-down list box or can browse to the library location.

   Once you have selected the `.lib` file, the Model Import wizard lists the model than match the symbol, in the Matching Model list box.

4. In the Select Matching page of the wizard, choose a model from the Matching Models list box and click Next.

5. In the Define Pin Mapping page of the wizard, map each of the model terminal to a Symbol pin. The pin names on the selected symbol appear in the Symbol Pin drop-down list box.

   Note: For the mapping you may want to view the model definition. For this use the View Model Text button at the bottom-left corner of the wizard.

6. To complete the attaching a PSpice model to the selected symbol and to close the Model Import wizard, click Finish.

A message box appears indicating that the a PSpice model is now attached to the selected symbol.

Caution

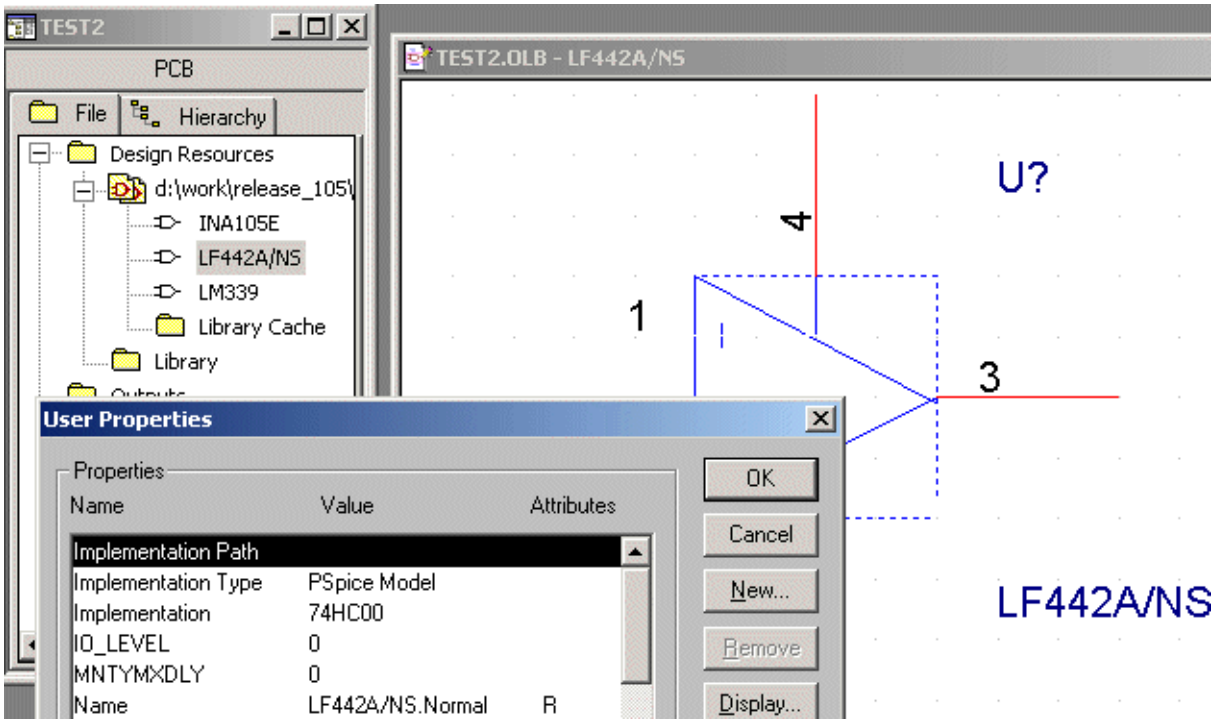
The procedure covered in this section can be used to attach PSpice models to homogeneous part symbols only.

When you use Model Import Wizard to attach a model to a symbol, following symbol properties are updated.

- Value of the IMPLEMENTATION TYPE property.
- Value of the IMPLEMENTATION property.

Tip

The value of the IMPLEMENTATION property attached to the part symbol, should match the name of the PSpice model as it appears in the .MODEL or .SUBCKT definition.



- Value of PSPICETEMPLATE property (not required for template-based models).

Simulating designs using PSpice

Capture designs are fully compatible with PSpice for simulation. This workflow provides information that will be useful for migrating your design from Capture into the PSpice environment.

If your design does not have a PSpice ground (‘0) symbol, then the analog simulation will not run on that design.

Creating a new simulation profile

A simulation profile (*.SIM) saves your simulation settings for an analysis type so you can reuse them easily.

You can create a new simulation profile from scratch or import the settings from an existing simulation profile. Importing settings from existing simulation profiles allows you to reuse the settings from other simulation profiles.

Capture version 10.0 allows you to create a new simulation profile by importing settings from a simulation profile that exists in the same project or in another project. Previous versions of Capture allowed you to import settings only from a simulation profile that exists in the same project.

Note: You can import simulation settings from a simulation profile that exists in another project only if the project in which you are creating the new simulation profile was created using Capture version 10.0.

If the project in which you are creating the new simulation profile was created using Capture version 9.2.3 or older versions, you must convert the project to the Capture 10.0 format to be able to import settings from a simulation profile that exists in another project.

To create a new simulation profile in PSpice

1. From the PSpice menu, choose New Simulation Profile. The New Simulation dialog box appears.

2. In the Profile Name text box, type a name for the profile (such as the name of the analysis type for the new profile).
3. You may want to import the simulation settings from an existing profile to the new profile. To do this, from the Inherit From drop-down list, select the profile from which you want to import the settings.

   The Inherit From drop-down list lists all the profiles existing in the current project. Click browse to select a profile from another project.

   Note: If the project in which you are creating the new simulation profile was created using Capture version 9.2.3 or older versions, you must convert the project to the Capture 10.0 format to be able to import settings from a simulation profile that exists in another project.
4. Click Create to create the profile and display the Simulation Settings dialog box.

After creating a new profile, you can edit the settings with the Edit Simulation Settings command.

Shortcut

Keyboard: ALT, S, N

Creating a simulation netlist

When generating a PSpice netlist, you can choose between two types of netlist formats:

- Flat netlist
- Hierarchical netlist

Use the PSpice tab on the Create Netlist dialog box to generate a customized PSpice netlist.

Note: While generating the netlist, if Capture does not find a PSpice ground (0) symbol in your design, then a warning message is flagged in the Session Log. You may ignore the warning, if the design will be used for running digital PSpice simulation. However, for running

analog simulation, the design must have at least one PSpice ground 0 symbol.

Viewing a simulation netlist

You can view the most recent simulation netlist for a selected design, or the current design.

To view a simulation netlist

1. In the project manager, select the design for which you want to create a netlist, or open a schematic page.
2. From the PSpice menu, choose View Netlist.

Running a simulation

You can simulate your Capture design using PSpice, provided that there are PSpice models for the parts in your design. PSpice and Capture are fully integrated.

To run a simulation

1. In the project manager, select a design to simulate, or open a schematic page.
2. In the project manager, select a simulation profile.
3. From the PSpice menu, choose Run or press the F11 function key.

PSpice does the following:

- checks design rules for your design.
- creates a simulation netlist for PSpice.
- opens PSpice using the netlist created from your design.

PSpice creates an output file (.OUT) as the simulation progresses. It contains bias point information, model parameter values, error messages, and so on. If the simulation fails, you can view the output file to see the error messages.

If the simulation completes successfully, PSpice produces a data file (.DAT). This is the file PSpice uses to display the simulation results. To see marker simulation results, the schematic must be open.

Viewing the results as the simulation progresses

You can choose to view results as a simulation progresses or after a simulation is completed.

To view results as a simulation progresses

1. From the PSpice menu, choose Edit Simulation Settings.
2. The Simulation Settings dialog box appears.
3. In Probe Window tab, select the Display Probe window check box.
4. Select the during simulation option.
5. Click OK.

Viewing the most recent simulation results

You can view the most recent simulation results for a schematic. If the schematic was simulated with more than one profile, you can choose which profile results to view.

To view the most recent simulation results

1. Open the schematic for which you want to view simulation results. You must do this to see marker results.
2. In the project manager, select the simulation profile you want to be active.
3. From the PSpice menu, choose View Simulation Results or press the F12 function key.

Viewing the output file

PSpice creates an output file (.OUT) as the simulation progresses. It contains bias point information, model parameter values, error

messages, and so on. If the simulation fails, you can view the output file to see the error messages.

To view the most recent output file

1. In the project manager, choose the simulation profile for which you want to see the output file.
2. From the PSpice menu, choose View Output File.

Editing simulation settings

Simulation profiles can be edited in Capture and PSpice.

To edit simulation settings from Capture

1. From the PSpice menu, choose Edit Simulation Settings. The Simulation Settings dialog box appears.
2. Click the tab for the settings you want to change.
3. Edit the settings and click the Apply button.
4. Repeat steps 2 and 3 until you have changed all the settings you need.
5. Click OK.

Shortcut

Keyboard: ALT, S, E

Using the FLOAT property

When preparing a circuit for simulation with PSpice, it's important that all pins for all parts are connected properly. If a pin is intentionally meant to remain unconnected, you need to use the PSpice pin property FLOAT, rather than a No Connect symbol. Otherwise, the circuit may not netlist correctly for PSpice.

The pin property FLOAT may have one of the following three values:

Value	Description
Error	The pin will not netlist. An error message will be returned when the PSpice simulation netlist is generated. Use Error when you want to be reminded that this pin is a "no connect" and should be treated in a special way. Error is the default value.
RtoGND	The pin is connected to a virtual resistor, whose opposite pin is tied to GND. The resistor has a value of 1/GMIN. This value allows the simulation netlist to be created and allows PSpice to perform the analysis. The virtual resistor will not be processed as part of a layout netlist or appear in a BOM.
Unique Net	The pin, when left unconnected, is attached to a unique node when the PSpice simulation netlist is generated. Use UniqueNet when you want the pin to remain unconnected but correspond to the Probe data associated with its part.

The FLOAT property can either be defined in the part editor when creating a new part, or you can edit a pin on an existing part Using the property editor.

To define the FLOAT property using the property editor

1. In Capture, double-click on the pin to open the property editor spreadsheet.
2. Click on the Pins tab.
3. Click New Column and type FLOAT (upper case) in the Name text box.
4. Type the property value you want to use, then click OK.
5. Click Apply or close the spreadsheet to have the changes take effect.

Placing markers

To view the markers in the simulation results, the schematic must be open.

Marker types on the Advanced command's submenu are only available after defining a simulation profile for an AC Sweep/Noise analysis.

To place markers in your design

1. From the PSpice menu, choose Markers.
2. Select the marker you want to place.
3. Drag the marker symbol attached to the cursor to the location where you want to place it.
4. Click the left mouse button to place the symbol.
5. Repeat steps 3 and 4 until you have place all of that type of symbol that you want.
6. Press the ESC key to end the marker mode, or click the right mouse button and select End Mode.

Showing, hiding, and deleting markers

You can show all, hide all, or delete all markers. Showing or hiding markers in the schematic also shows or hides the trace results in the Probe window.

To show all, hide all, or delete all markers

1. From the PSpice menu, choose Markers.
2. Select the Show All, Hide All, or Delete All option.

Note: When you move a wire which has a voltage marker placed on it, you might find that the voltage marker stays at its original place and no longer points to the wire. When you try to move the marker on the moved wire, you get the following warning message: “Voltage/digital level marker will be ignored unless connected to a wire, bus, or a pin.” To avoid this warning, after moving the wire which already has a marker placed, choose the Show All command from the Markers

submenu of the PSpice menu. This action rearranges all the markers to their corresponding node/net at the new locations.

Simulating and viewing the results of multiple profiles

You can select one profile or multiple profiles to be simulated or viewed. If you select only one profile for simulation, it is handled as though you chose the Run command. If you select one file for viewing, it is handled as though you chose the View Simulation Results command.

If you select multiple profiles, simulations for all selected profiles are performed using the simulation queue. You must then open the .DAT files to view the results.

To simulate multiple profiles

1. In the project manager, choose the simulation profiles you want to simulate.
2. From the PSpice menu, choose Simulate Selected Profile(s).

PSpice opens and processes the profiles using the simulation queue.

To view the results

1. Close the simulation queue, but leave PSpice active.
2. The Probe window is active, but no traces are visible.
3. From the PSpice File menu, choose Open.
4. Select the .DAT files that you want to view and click the Open button. A tab for each .DAT file you selected appears at the bottom of the Probe window.
5. From the PSpice Window menu, choose Display Control.
6. Select a profile for which you want to display the results.
7. Click the Restore button.
8. Repeat steps 4, 5, and 6 for all profiles you want to view.

You can then click each tab to view the displayed results.

Making a simulation profile active

To simulate a design with a specific simulation profile, or to view the most recent results of a specific simulated profile, you must activate the profile.

To activate a simulation profile

1. In the project manager, choose the simulation profile you want to activate.
2. From the PSpice menu, choose Make Active.

Designing for analog/mixed signal simulation

To simulate a Capture design with PSpice A/D, you must begin the project as an analog type intended for simulation. Existing projects in Capture cannot be simulated without special modifications. To learn how to simulate an existing project with PSpice A/D, see Simulating non-PSpice projects in the PSpice online help.

A design that is targeted for simulation has:

- parts for which there are simulation models available and configured
- sources of stimulus to the circuit

When creating designs for both simulation and printed circuit board layout, some of the parts you use are for simulation only (simulation stimulus parts like voltage sources), and some of the parts you use have simulation models that only model some of the pins of a real device.

The parts that are to be used for simulation, but not for board layout, have a SIMULATIONONLY property.

You can add this (or any) property to your own custom parts to make them simulation-only.

To create a new project for simulation

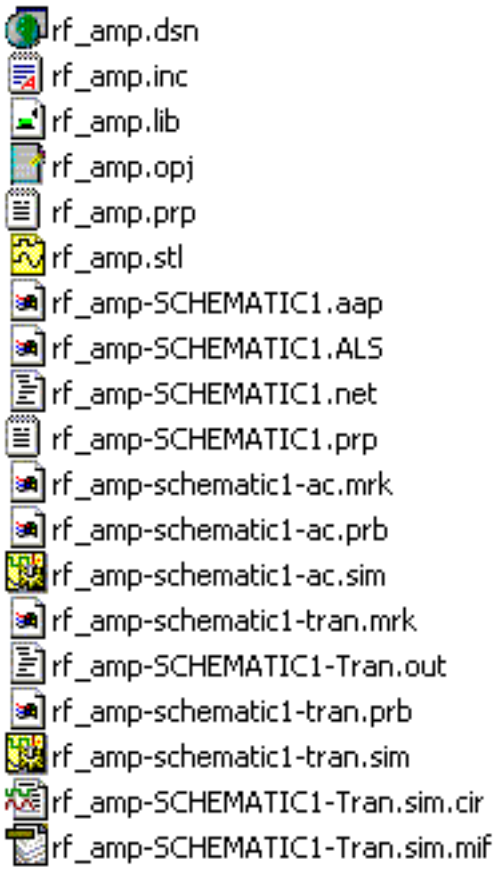
1. From the File menu in Capture's Project Manager, point to New and select Project.
2. The New Project dialog box appears.
3. In the Name text box, enter the name for the new project.
4. Under the Create a New Project Using frame, select Analog or Mixed-Signal Circuit Wizard.

   Note: You must create a project (not a design) and select the Analog or Mixed-Signal Circuit Wizard option to be able to simulate the new design with PSpice A/D.
5. In the Location text box, enter the path where you want the new project files to be stored, or use the Browse button to locate the directory.
6. Click OK.
7. Enter any special libraries to be included, if necessary, and click Finish to create the new project directory and open the schematic page editor.

New directory structure for analog projects

All files related to analog projects created using Capture version 9.2.3 or older versions were maintained in a single directory.

Figure 16-1 Directory structure for RF_AMP analog project created using Capture 9.2.3 or older versions



In the above figure, the `rf_amp` project has a design named `rf_amp.dsn`. The `rf_amp` design has a schematic named `SCHEMATIC1` and `SCHEMATIC1` has two profiles, `rf_amp-schematic1-ac.sim` and `rf_amp-schematic1-tran.sim`. The long file names make it difficult to identify files associated with the design, schematic or profile, and delete them if they are no longer required. For example, the `.sim` (simulation profile) files have the name,

`<DesignName>-<SchematicName>-<ProfileName>.SIM`

Capture 10.0 introduces a new directory structure for analog projects in which the design level, schematic level and simulation profile level PSpice files are organized in their respective directories. This makes it easier to manage the files for the project.

Note: If you open an analog project that was created using Capture version 9.2.3 or older versions in Capture 10.0, you will be prompted to convert the project to the Capture 10.0 format.

In the new directory structure all the PSpice related files for the `rf_amp` project are maintained in a directory named `rf_amp-PSpiceFiles`.

- The PSpice files related to the design are maintained in the `rf_amp-PSpiceFiles` directory. For more information, see How are files configured at the design level maintained in the new directory structure for analog projects? on page 662.
- The PSpice files related to the schematic named `SCHEMATIC1` are maintained in a sub-directory named `SCHEMATIC1` under the `rf_amp-PSpiceFiles` directory.
- The PSpice files related to the AC and Tran simulation profiles are maintained in the `AC` and `Tran` sub-directories under the `SCHEMATIC1` directory. For more information, see How are files configured at the profile level maintained in the new directory structure for analog projects? on page 664.

How are files configured at the design level maintained in the new directory structure for analog projects?

The model libraries, stimulus files and include files configured at the design level are stored in the `<projectname>-PSpiceFiles` directory. For example, the model libraries, stimulus files and include files configured at the design level are stored in the `rf_amp-PSpiceFiles` directory. The `rf_amp.stl` stimulus file in the `rf_amp-PSpiceFiles` directory is an example of a PSpice file related to the design.

You can view the paths to the model libraries, stimulus files and include files configured at the design level in the Capture Project Manager window.

Note the following:

- If you select the Retain Old Project check box when you convert an analog project that was created using Capture version 9.2.3 or older versions to the new project format, only the files configured at the design level that have the same name as the

design are copied over to the `<projectname>-PSpiceFiles` directory in the location you specified for creating the project in the new format.

The files configured at the design level that do not have the same name as the design are not copied over to the `<projectname>-PSpiceFiles` directory because they are custom files. Instead, these files are read from their original location. You can view the path to the custom files configured at the design level in the Configuration Files tab of the Simulation Settings dialog box and in the Capture Project Manager window.

For example, suppose that your design name is `rf_amp`, and you have configured the following files at the design level:

- rf_amp.inc
- decoder.lib
- rf_amp.lib
- rf_amp.prp
- rf_amp.stl

If you select the Retain Old Project check box when you convert the analog project to the new format, only the following files are copied over to the `rf_amp-PSpiceFiles` directory in the location you specified for creating the project in the new format.

- rf_amp.inc
- rf_amp.lib
- rf_amp.prp
- rf_amp.stl

The `decoder.lib` file is read from the old project location. You can view the path to the `decoder.lib` file in the Configuration Files tab of the Simulation Settings dialog box and in the Capture Project Manager window.

- When you create a new simulation profile by importing the settings from another simulation profile that exists in another project, only the simulation settings are inherited from the source simulation profile. The files configured at the design level for the source simulation profile are not copied over to the

<projectname>-PSpiceFiles directory of the project in which you are creating the new simulation profile.

How are files configured at the profile level maintained in the new directory structure for analog projects?

The model libraries, stimulus files and include files configured at the profile level are stored in a directory that has the same name as the profile. For example, the PSpice files related to the Tran simulation profile can be maintained in the Tran sub-directory under the SCHEMATIC1 directory.

An include file named <profilename>_profile.inc is created in the directory for the simulation profile. This file contains information on the model libraries, stimulus files and include files configured for that profile. For example, the Tran profile directory can contain a Tran_profile.inc include file that includes information on the decoder.lib model library, decoder.stl stimulus file and the Tran.inc include files configured for the Tran profile.

You must not delete the <profilename>_profile.inc file in the directory for a simulation profile.

Note: When you create a new simulation profile by importing the settings from another simulation profile that exists in the same project or in another project, the files configured at the profile level for the source simulation profile are copied to the directory for the new simulation profile. The files configured at the design level for the source simulation profile are not copied over to the <projectname>-PSpiceFiles directory of the project in which you are creating the new simulation profile.

What happens when I convert a project that uses a design from another project or from another location?

If you convert an analog project (created using Capture 9.2.3 or older versions) that uses a design from another project or from another location, to the new project format, the design file and all the contents of the design are copied to the current project and maintained in the new directory structure for analog projects.

What should I do if the schematic for a converted project uses FILESTIMn parts from the SOURCE library?

If you have specified only the name of the stimulus file as the value of the FILENAME property on a FILESTIMn part, you must specify the path to the stimulus file in the value for the FILENAME property on the FILESTIMn part.

Transitioning from PSpice Schematics to Capture

A number of significant changes were made to PSpice Release 9 that users of Release 8 may find difficult to understand or work with. The following information should make the transition to Release 9 easier and less confusing for those who are familiar with earlier versions of PSpice.

Note: For more detailed information about using the Schematics-to-Capture Translator, see the online guide Converting MicroSim Schematics Designs to OrCAD Capture Designs (SCH2CAP.PDF) in the \doc directory of your OrCAD installation or if you have installed the documentation to your hard disk, you can access it by choosing Cadence Help from the OrCAD Release 16.0 pull-right menu (available from the Start menu).

Note: For last minute information about moving from Release 8 to Release 9, see the PSpice Release 9.1 Release Notes. You can access this by choosing Release Notes from the OrCAD Release 9 pull-right menu (available from the Start menu).

Converting PSpice Schematics projects to Capture projects

You can translate a MicroSim Schematics Release 8 project to an OrCAD Capture project using the in Capture.

To convert a Schematics project to Capture:

1. In Capture, from the File menu, choose Import.
2. In the PSpice tab, select the source schematic, the destination project, and the PSPICE.INI file for existing settings.

3. Click OK to start the automated translation utility.

Note: For more detailed information about using the Schematics-to-Capture Translator, see the online guide *Converting MicroSim Schematics Designs to OrCAD Capture Designs* (SCH2CAP.PDF) located in the \doc directory of your OrCAD installation or if you installed the documentation to your hard disk, you can access it by choosing Cadence Help from the OrCAD Release 16.0 pull-right menu (available from the Start menu).

Note: For last minute information about the Schematics-to-Capture Translator, see the *PSpice Release 9.1 Release Notes.* You can access this by choosing Release Notes from the OrCAD Release 9 pull-right menu (available from the Start menu).

Using the PSpice Schematics “Bridge”

An interim capability referred to as the "Bridge" is now available to help users of PSpice Schematics Release 8 bridge the transition to working with OrCAD Capture and PSpice Release 9.1. The Schematics "Bridge" allows users of PSpice Schematics Release 8 to load and simulate designs with PSpice Release 9.1. This is a temporary solution for those who need to continue doing designs with Schematics while they learn to use Capture, but want to take advantage of the improvements found in PSpice Release 9.1 immediately.

PSpice Schematics vs. OrCAD Capture command reference

Use the following comparison tables to find the particular command you are familiar with in Schematics Release 8, and its corresponding command in Capture Release 9. These tables are organized according to the Release 8 menu structure.

This PSpice Schematics Release 8 command...	Is similar to this Capture schematic editor command...
New (File menu)	New command
Export (File menu)	Export Design command

Undo (Edit menu)	Undo command
Redo (Edit menu)	Redo command
SPACEBAR	Repeat command
Cut (Edit menu)	Cut command
Copy (Edit menu)	Copy command
Paste (Edit menu)	Paste command
Delete (Edit menu)	Delete command
Select All (Edit menu)	Select All command
Attributes (Edit menu)	Properties command
Symbol (Edit menu)	Part command
Flip (Edit menu)	Mirror command
Rotate (Edit menu)	Rotate command
Find (Edit menu)	Find command
Get New Part (Draw menu)	Part command Off-Page Connector command, Hierarchical Port command, No Connect command, Title Block command, Power command, Ground command
Wire (Draw menu)	Wire command
double-clicking a wire	Net Alias command
Bus (Draw menu)	Bus Entry command
Block (Draw menu)	Hierarchical Block command
drawing a wire to the edge of a block	Hierarchical Pin command
Box (Draw menu)	Rectangle command
Circle (Draw menu)	Ellipse command
Arc (Draw menu)	Arc command
Polyline (Draw menu)	Line command Polyline command
Insert Picture (Draw menu)	Picture command

Text (Draw menu)	Text command
Pop, Top (Navigate menu)	Ascend Hierarchy command
Push (Navigate menu)	Descend Hierarchy command
Select Page (Navigate menu)	Go To command
Fit (View menu)	Zoom All command
In (View menu)	Zoom In command
Out (View menu)	Zoom Out command
Area (View menu)	Zoom Area command
Entire Page (View menu)	Zoom All command
Redraw (View menu)	Redraw command
Pan–New Center (View menu)	Zoom Selection command
Toolbars (View menu)	Toolbar command or Tool Palette command
Status Bar (View menu)	Status Bar command
Editor Configuration (Options menu)	Schematic Page Properties command
New (Window menu)	New Window command
Tile Horizontal (Window menu)	Tile Horizontally command
Tile Vertical (Window menu)	Tile Vertically command

This PSpice Schematics Release 8 command...	**Is similar to this Capture project manager command...**
Pan and Zoom (Options menu)	Preferences command
Display Options (Options menu)	Preferences command
Display Preferences (Options menu)	Preferences command or Design Template command

Tips for PSpice Schematics Release 8 users

This topic contains a number of helpful tips for users of PSpice Schematics Release 8, who are learning how to work with Release 9.1. These are taken from the Release Notes for PSpice Release 9.1. Please refer to the Release Notes for the most recent, up-to-date information about PSpice Schematics, which may supersede the information presented here.

Creating a new PSpice project

Creating a new PSpice project in Capture is a matter of selecting the proper Project Wizard option and choosing whether to use an existing project file.

To create a new project:

1. From Capture's File menu, point to New and choose Project.
2. In the New Project dialog box, select the Analog or Mixed A/D option.
3. Specify a project name and location.
4. Choose the OK button. The Create PSpice Project dialog box appears.
5. Select one of the two available options: Create it based upon an existing project or Create a blank project. If you select the former option, choose a project file (.OPJ) with either the appropriate drop-down menu or the Browse button.

Note: Use the PSpice project template, *AnalogGNDSymbol.opj.* This project by default has the PSpice ground 0 symbol needed for your analog designs.

6. Click OK.

Note: You must create a project (not a design) and select the Analog or Mixed A/D option in order to be able to simulate the new design with PSpice A/D.

Note: When you create a new design for PSpice, you need to use the File > New > Project command and then select the Analog or Mixed A/D radio button. If you pick one of the other radio buttons, or

choose the File > New > Design command, you cannot add and edit profiles, place markers, or run PSpice simulations. Also, while copying PSpice designs from one directory to another, you need to copy the project file as well as the design file or else you cannot perform PSpice operations. To solve this problem, you need to create an Analog or Mixed A/D project using the File > New > Project command and then add your design to it.

Note: When you create a new PSpice project, you can use an existing design as a template for creating the new design.

Locating PSpice libraries

The PSpice part libraries (.OLB files) are located in the CAPTURE\LIBRARY\PSPICE directory, under your main installation directory. The simulation model libraries (.lib files) are located under the PSPICE\LIBRARYdirectory.

If you wish to add more PSpice part libraries to your design, you can do so by using the Place Part dialog box (from the Place menu, choose Part or use the Place Part toolbar button). Then add the library you need by selecting it from the CAPTURE\LIBRARY\PSPICE subdirectory.

Placing PSpice ground 0 symbols for PSpice simulations

For PSpice analog simulation to run, your design must have a PSpice ground (0) symbol. The CAPSYM.OLB, which is the default library in Capture now includes the PSpice ground (0) symbol. Use the ‘0’ symbol to place a PSpice ground 0 symbol in your design.

To select the '0' symbol:

1. From the Place menu, choose Ground (or use the Place Ground toolbar button). The Place Ground dialog box appears.
2. Select the CAPSYM part library from the Libraries list (if it is not already selected).

Note: You can also place the 0 symbol from the Source part library. To do this, add the Source part library to the Libraries list using the Add Library button; SOURCE.OLB is located in the

\TOOLS\CAPTURE\LIBRARY\PSPICE subdirectory under your installation directory.

3. Select the '0' symbol (if not already selected).
4. Click OK to place the PSpice ground ‘0’ symbol.

Alternately, you can place any ground symbol, double-click on it and change its name to "0".

Note: While generating the PSpice netlist, if Capture does not find a PSpice ground (0) symbol in your design, then a warning message is flagged in the Session Log. You may ignore the warning, if the design will be used for running digital PSpice simulation. However, for running analog simulation, the design must have at least one PSpice ground 0 symbol.

Note: If you are starting a new analog PSpice design, then it is recommended that you use the PSpice project template, *AnalogGNDSymbol.opj*. This project by default has the PSpice ground 0 symbol needed for your analog designs.

Descending hierarchical parts in a translated .SLB library

If you use a part in a translated library and the library is not in the same directory as your design, you will not be able to descend. As a workaround, you can edit the part in the library and clear the name of the library from the implementation cell so that it is blank.

Simulating without displaying waveforms

To simulate without displaying the waveforms

1. From the PSpice menu choose Edit Simulation Settings command the Simulation Settings dialog box appears.
2. Clear both of the following check boxes under the Probe tab:
   - ❑ Display Probe window when profile is opened
   - ❑ "Display Probe window"

Command line switches for PSpice

Command line options, such as "-i" to load a user defined initialization file (.INI), can be specified by adding the following line to the <windows_dir>\pspice.ini file:

```
[PSPICE]
PSPICECMDLINE= -i <user_dir>\<ini_file>
```

A custom .INI file can contain a configuration of PSpice library, include and stimulus files. For other command line options, see the online *PSpice A/D Reference Manual*.

Translated designs with unconnected pin errors

Translated schematics, when netlisted for PSpice, may get "unconnected pin" errors in Release 9.1. This will occur if there are voltage sources or ABM parts with outputs connected to ports, where the ports have no corresponding port with the same name. These designs will need their design cache changed to Unique Net to work correctly.

To change the design cache:

1. In Capture, select the part.
2. From the Edit menu, choose the Part command.
3. Double-click the pin.
4. Add a User Property FLOAT=UniqueNet.
5. From the File menu, choose Save.
6. Select Update All.

Change in the function of PRINT STEP

Print Step no longer needs to be specified for a transient analysis. When left at the new default value of 0, the following is used in its place:

- maximum step size if defined
  otherwise Final Time/100

PSpice uses TSTEP for the following purposes, in addition to setting print and plot intervals for the text output file:

- It's the maximum time step for circuits that have no charge storage devices or maximum step size.
- It's used to limit the maximum frequency for impulse response calculations in ABM Laplace devices and lossy transmission lines.
- It becomes the default for various parameters associated with independent source stimuli (i.e., rise time, fall time, 1/frequency, etc.) if these values are set to zero by the user.
- .FOUR uses it to specify time resolution for the old Fourier analysis, whose results are printed to the text output file. This does not affect the FFT plots in Probe.

Using the PSpiceDefaultNet property

IPIN(<pin>) attributes that are present for hidden pins in Schematics are replaced by the PSpiceDefaultNet property on power pins in Capture. When creating a part with a power pin, create the pin property:

```
PSpiceDefaultNet=<net_name>
```

The PSpiceDefaultNet pin property cannot be displayed on the schematic.

Using the @ prefix

Use the @ prefix to pass down values from the top-level schematic (parent) to a sub schematic (child). Check out the histo.opj project under <install_dir>\tools\pspice\capture_samples\anasim\histo. In the Band Pass RC Biquad Stage schematic. Notice that Rin and Rfeedback values are preceded with @ symbols, indicating that these parameters are substituted with values passed down from the top-level schematic. See "Example" on page 547.

Using global parameters in Capture

The new PARAM part works differently in releases earlier than Release 9.1. Now you just add new properties and assign them

values in the spreadsheet. They should display on the schematic and netlist as in Release 8.

Consider the following example, in which you can add a property named VAL, with value 10K:

1. From the Place menu, choose Part.
2. Place an instance of PARAM from SPECIAL.OLB.
3. Double-click it to start the spreadsheet editor.
4. Click New.
5. Type Name=VAL.
6. Click on the cell below VAL, then type in the value 10K.
7. Click Display, then Click Name=Value.
8. Click Apply.

Unlike the PARAM symbol in PSpice Schematics, there is no limit on the number of parameters you can add with one PARAM part in Capture.

Using HI and LO symbols

The HI and LO symbols for digital inputs have been renamed and moved. These can be used by choosing Place Power in Capture. $D_HI and $D_LO are now in the library \TOOLS\CAPTURE\LIBRARY\PSPICE\SOURCE.OLB under your installation directory.

Using the Run Optimizer command

With PSpice Schematics Release 8, using the Run Optimizer command from the Tools menu would load parameters into Optimizer even if Optimizer was already open.

With the PSpice Schematics "Bridge" for Release 9.1, if Optimizer is open and Run Optimizer is executed, an hourglass appears for about 5-10 seconds before a message box is displayed stating: "Unable to start application, OPTIMIZE.EXE". This message is followed by another message: "Unable to start application".

The workaround for this situation is to close Optimizer before selecting the Run Optimizer command from the Tools menu.

NRD and NRS default values for MOSFETs

Prior to PSpice Release 9, the default values for NRD and NRS in PSpice were 1.

Starting with PSpice Release 9, the default values are 0.

This change will not affect device instances with NRD and NRS specified in the netlist.

MEMUSE in the .OPTIONS ACCT report

The command MEMUSE has been removed and will no longer appear when you simulate with .OPTIONS ACCT in the netlist.

The memory usage information can be obtained from Windows.

Importing designs from OrCAD Express to Capture

The Express tool was the FPGA solution provided by OrCAD. Express gives you the tools you need to take your programmable logic device project through each phase of the design flow. With Express you get full design entry capabilities (establishment and control of design hierarchy, schematic and VHDL model development, and design rule checking) as well as simulation and debugging capabilities.

Any design file (.DSN) that you have created in Express is compatible with Capture. We recommend that to complete your FPGA design, you use our new FPGA Studio tool suite.

Although you can create designs in Capture, and import them into Express, it is not recommended that you do so. Since Express is now a "sunsetted" product, its synthesis and simulation engines are no longer supported by OrCAD.

Using Capture with OrCAD SDT

Use the information in this workflow to help translate your designs from SDT to Capture.

Opening a design created in SDT

OrCAD Capture for Windows can translate flat and hierarchical designs created in SDT Release IV and SDT 386+.

Translation turns illegal characters in part names in a library into the underscore character (_). The only currently illegal character is the period (.). All parts on a schematic page that reference illegally named parts will be renamed in the same fashion.

Translation requirements

Either an SDT.CFG file or an SDT.BCF file (Release IV) must exist in one of the following places:

- The current directory
- The directory that contains the design
- The directory specified by the ORCADPROJ environment variable

All necessary libraries (.LIB files) must be present in one of the following places:

- The current directory
- The directory that contains the design

Note: You do not need to move any files (including DOS utilities) if your design is correctly specified for SDT, to translate SDT designs into Capture.

Note: If you have changed your environment, it may be useful to keep your .LIB files in the same directory as their associated SDT.CFG and SDT.BCF files.

To translate a schematic from SDT to Capture

1. If you need to change the name of a part field, open the design's configuration file and make the necessary changes. See Translating part fields for more information.
2. Specify any user properties you want created from SDT part fields in the SDT Compatibility tab of the Design Template dialog box.
3. From the File Menu, choose Open. The Open dialog box appears.
4. In the Files of Type box, select SDT Schematic (*.SCH) or select All Files (*.*).
5. Locate the schematic by changing the drive and directory as appropriate in the Look in box.
6. Select the schematic folder and click Open.
7. In the Save Translated Design As dialog box, specify the following information:
8. In the Save in box, select a drive and directory as appropriate.
9. In the File name box, provide a name for the translated design.
10. Click Save.

Note: Before the design or library is translated, the Save As dialog box appears. Do not click Cancel unless you want to abandon the translation. If you do click Cancel, Capture will not translate the design or library.

Note: Capture changes the alignment of vertical pins in designs translated from SDT. In SDT, vertical pin numbers are to the right of the pins. In Capture, they are to the left of the pins. As a result, a design translated from SDT may be difficult to read.

The schematic folder structure of the translated design appears in the project manager.

- Any sheet parts and sheetpath parts are converted to hierarchical blocks, which you can display by choosing Descend Hierarchy on the View menu.

- Any module ports are converted to off-page connectors (for a flat design) or hierarchical ports (for a hierarchical design or a single page design).
- Any |LINK statements and comments are converted to text. Connectivity is not maintained by |LINK statements. Connectivity is maintained through off-page connectors to pages placed within the same schematic folder.

Opening a library created in SDT

OrCAD Capture for Windows can translate libraries created in SDT Release IV and SDT 386+.

Note: Translation turns illegal characters in part names in a library into the underscore character (_). The only currently illegal character is the period (.). All parts on a schematic page that reference illegally named parts will be renamed in the same fashion.

Translation requirements

These utilities must be located in one of the following areas:

- The current directory
- The design directory (if different from the current directory)
- The CAPTURE.EXE directory
- A directory specified by the ORCADPROJ environment variable

The library to be translated must be in one of the following places:

- The current directory
- The design directory (if different from the current directory)

Capture cannot translated compressed SDT files. You need to decompress all compressed SDT files.

To translate a library from SDT to Capture

1. From the File Menu, choose Open. The Open dialog box appears.

2. In the List Files of Type box, select the library type SDT Library (*.LIB) or select All Files (*.*).
3. Locate the library by changing the drive and directory as appropriate in the Look in box.
4. Select the library file to open or type the name in the File name entry box, and choose Open.
5. In the Save Translated Design As dialog box, specify the following information:
6. In the Save in box, select a drive and directory as appropriate.
7. In the File name box, provide a name for the translated design.
8. Click Save.

Note: Before the design or library is translated, the Save As dialog box appears. Do not click Cancel unless you want to abandon the translation. If you do click Cancel, Capture will not translate the design or library.

Note: Capture changes the alignment of vertical pins in designs translated from SDT. In SDT, vertical pin numbers are to the right of the pins. In Capture, they are to the left of the pins. As a result, a design translated from SDT may be difficult to read.

Note: If you move a net alias away from the wire it is linked to in Capture, and then translate the design back to SDT, the label won't be tied to the net. Its original link established in Capture won't be restored.

SDT Release IV and SDT 386+ ASCII (.SRC) libraries

Capture translates the ASCII (.SRC) file to SDT 386+ (.LIB) format, and then translates that to OrCAD Capture for Windows (.OLB) format.

The structure of the translated library appears in the project manager.

SDT Release IV binary (.LIB) libraries

Capture translates the SDT Release IV (.LIB) file to ASCII (.SRC) format. Capture then translates that to SDT 386+ (.LIB) format.

Finally, Capture translates that to OrCAD Capture for Windows (.OLB) format. Capture translates bitmap parts to vectors.

The structure of the translated library appears in the project manager.

SDT 386+ binary (.LIB) libraries

Capture translates the SDT 386+ (.LIB) file to OrCAD Capture for Windows (.OLB) format.

The structure of the translated library appears in the project manager.

Saving in SDT format

Capture can translate projects and libraries to SDT 386+ and SDT Release IV format.

Translation requirements

Capture includes the following DOS utility, which it uses to translate a design to SDT:

- COMP16.EXE

This utility must be contained in a directory specified by your AUTOEXEC.BAT's PATH statement.

Guidelines for creating an SDT-compatible design

Not all designs you make in Capture are compatible with SDT. If you want to make your Capture design SDT compatible, follow these rules:

- Do not place bus-width pins on part instances.
- Do not create heterogeneous parts.
- Do not create packages with more than sixteen parts.
- Do not create parts or part instances with more than seven user-defined properties.

- Do not put properties on wires, hierarchical ports, power or ground pins, or off-page connectors.
- Do not create hierarchical blocks with hierarchical ports on top or bottom.
- Do not use numeric pin numbers greater than 255.
- Use one title block only.
- Do not create a multiple-page schematic folder in a multiple-level project. In other words, you can use either off-page connectors or hierarchical blocks, but not both. (If you use hierarchical blocks, each must be mapped to a schematic folder containing a single schematic page.)
- Do not use graphics. (You can use lines of text characters, instead.)
- Use eight characters or fewer (not including extensions) for schematic page names.
- Do not move net aliases off of wires or buses. If you do, the wire or bus will be disconnected.

Note: Capture truncates schematic page names to eight characters. Before you save a design or library in SDT format, make sure schematic page names are unique within the first eight characters.

When you run Design Rules Check on your design with the Check SDT compatibility option selected, Capture checks for violations of these rules.

In addition to following these guidelines, an SDT.CFG file must exist in the same directory as your design or in the directory specified by your ORCADPROJ environment variable.

To save a design or library in SDT format

1. Run Design Rules Check on your design using the Check SDT compatibility option.
2. If Capture reports any errors, correct them before saving the design or library in SDT format.

3. In the Design Properties dialog box, specify which properties you want mapped to each SDT part field. For more information, see Translating part fields.
4. From the project manager's File menu, choose Save As. The Save As dialog box appears.
5. In the Save File as Type box, select either SDT 386+ or SDT Release IV (.SCH for schematic or .LIB for library).
6. Type the name in the File Name entry box, and click OK.

Translating part fields

Capture uses the SDT compatibility options in the Design Template dialog box when you save a Capture design in SDT format. Capture sets the SDT compatibility options in the Design Properties dialog box when you open an SDT schematic folder (.SCH) file in Capture.

Setting up the design template

When you create a new design, the SDT compatibility options are inherited from the design template. Follow these steps to set up the design template for SDT compatibility:

1. From the Options menu, choose Design Template, and choose the SDT Compatibility tab.
2. Specify the properties you want to map to the SDT part fields for future designs.

Changing the SDT compatibility options for a single design

When you save a design in SDT format, Capture uses the SDT compatibility options in the Design Properties dialog box. Follow these steps to change a design's SDT compatibility options:

1. With the program manager active, select the Design folder.
2. From the Options menu, choose Design Properties, and choose the SDT Compatibility tab.
3. Specify the properties you want to map to the SDT part fields for the active design.

Translating part fields from SDT to Capture properties

Capture translates SDT part fields into properties. If you want to change the user property names before translation, follow these steps:

1. Open the design's SDT.CFG file in any text editor.
2. Locate the lines that specify the part field names, and change them to suit your needs.
3. Save your changes, and exit the editor.

Translating Capture properties to SDT part fields

You can specify properties for Capture to translate into SDT part fields by following these steps:

1. From the Options menu, choose Design Properties, and select SDT Compatibility.
2. Specify the properties you want to map to the SDT part fields.

Importing and exporting designs

Capture can export designs and schematics to EDIF and DXF format, and can import designs in EDIF, PDIF and PSpice formats.

Importing EDIF designs

Capture can import graphical EDIF design files. Make sure that the .EDF file is not an EDIF netlist before importing the file.

You can specify a configuration file (*.CFG) to be used for importing. The configuration file specifies which information is carried over from the EDIF design to the Capture design. For more information on using configuration files for importing EDIF designs, see Electronic Tools Company's *EDIF2CAP (EDIF 2 0 0 to OrCAD Capture Schematic Translator) User's and Reference Manual*.

Supplied with Capture are the following sample .CFG files you can use for importing designs:

- EDI2CAP.CFG
- MENT2CAP.CFG
- VIEW2CAP.CFG

Importing PDIF designs

Capture can import PDIF designs. If Capture encounters problems while translating, check the session log. Some imported PDIF parts may not be editable in Capture. Such parts won't affect netlists.

Importing PSpice designs

Capture can import PSpice designs. If Capture encounters problems while translating, check the session log.

Exporting EDIF designs

Capture can export graphical EDIF design files. These files typically have an .EDF file extension, and should not be confused with EDIF netlists that share the same file extension. If you want to generate an EDIF netlist, use the EDIF tab on the Create Netlist dialog box, accessible through the Create Netlist command on the Tools menu.

You can specify a configuration file (*.CFG) to be used for exporting. The configuration file specifies which information is carried over from your Capture design to the EDIF design. For more information on using configuration files for exporting EDIF designs, see Electronic Tools Company's *CAP2EDIF (OrCAD Capture to EDIF 2 0 0 Schematic Translator) User's and Reference Manual*.

Supplied with Capture are the following sample .CFG files you can use for exporting designs:

- CAP2EDI.CFG
- CAP2MENT.CFG
- CAP2VIEW.CFG

Exporting DXF designs

Capture can export individual schematics to DXF output. Files are saved as .DXF files, and saved in AutoCAD's V12 file format.

Importing designs

Use the Import Design dialog box, accessible through the Import Design command, to import EDIF (*.EDF), PDIF (*.PDF) and PSpice design files.

When translating EDIF files, make sure to use only graphical EDIF design files, and not EDIF netlists. You can specify a configuration file (*.CFG) to control certain aspects of the EDIF design translation. For information on configuration files, see Using Capture with OrCAD SDT on page 676 and Electronic Tools Company's *EDIF2CAP (EDIF 2 0 0 to OrCAD Capture Schematic Translator) User's and Reference Manual*.

To import an EDIF design

1. Make sure only the project you're working with is open.
2. From the File menu, choose the Import Design command. The Import Design dialog box appears.
3. Choose the EDIF tab.
4. In the Open text box, specify the name of the .EDF file to translate, or use the Browse button to locate the file.
5. In the Save As text box, specify the name of the .DSN file to save the design as, or use the Browse button to locate a file and directory.
6. If you are using a configuration file for the translation, specify the .CFG in the Configuration file text box, or use the Browse button to locate the file.
7. Click OK. Capture translates the design, and opens it in a project manager window.

To import a PSpice Design

1. From the File menu, choose the Import Design command. The Import Design dialog box appears.
2. Choose the PSpice tab.
3. In the Open text box, specify the name of the PSpice file to translate, or use the Browse button to locate the file.
4. In the Save As text box, specify the name of the .OPJ file to save the project as, or use the Browse button to locate a directory.
5. Specify the path and filename of the PSPICE.INI file in the Schematic Configuration File text box, or use the Browse button to locate the file and directory.
6. Click OK. Capture translates the design, and opens it in the project manager window.

Note: For information on translating a schematic with hierarchical blocks, see the online help Schematics-to-Capture Translation (sch2cap.chm).

To import a PDIF design

1. From the File menu, choose the Import Design command. The Import Design dialog box appears.
2. Choose the PDIF tab.
3. In the Open text box, specify the name of the .PDF file to translate, or use the Browse button to locate the file.
4. In the Save As text box, specify the name of the .DSN file to save the design as, or use the Browse button to locate a file and directory.
5. Click OK. Capture translates the design, and opens it in a project manager window.
6. If Capture encounters problems during translation, check the session log. Some imported PDIF parts may not be editable in Capture. Such parts won't affect netlists.

Exporting designs

Use the Export Design dialog box, accessible through the Export Design command, to export EDIF (*.EDF) and DXF (*.DXF) designs and schematics.

When exporting designs to EDIF, Capture saves the files to a graphical EDIF design format, and not as an EDIF netlist. You can specify a configuration file (*.CFG) to control certain aspects of the EDIF design translation. For more information on configuration files, see Using Capture with OrCAD SDT on page 676 and Electronic Tools Company's *CAP2EDIF (OrCAD Capture to EDIF 2 0 0 Schematic Translator) User's and Reference Manual*.

You can export individual schematic pages or the entire design to DXF files in AutoCAD's V12 file format. Capture exports schematic data exactly as appears in the schematic editor, with the following exceptions:

- Parts with filled graphics are translated as outlined objects.
- Parts with overbar pin names are translated as such, but no overbar will be visible when viewing with Vcadd V2.0.
- Graphics on the schematic sheet are not translated. Only the outline of the graphic will be seen in the final DXF file.
- Properties with Do Not Display settings will not be displayed in the final DXF file.

Note: Pin name and number movement information is not exported to DXF files.

To export a design to EDIF

1. From the File menu, choose the Export Design command. The Export Design dialog box appears.
2. Choose the EDIF tab.
3. In the Save As text box, specify the name of the .EDF file to save the design as, or use the Browse button to find a file and directory.

4. If you are using a configuration file for the translation, specify the .CFG in the Configuration file text box, or use the Browse button to locate the file.
5. Click OK. Capture translates the design to a graphical EDIF design file.

To export a design to DXF

1. In the schematic page editor, choose Export Design from the File menu. The Export Design dialog box appears.

   Note: In order to export a design or schematic to DXF, you must have a schematic page from that design open and selected as the active window. Otherwise, Capture will not allow a DXF export.
2. Choose the DXF tab.
3. In the Save As text box, specify the name of the .DXF file to save the design as, or use the Browse button to find a file and directory.
4. Select the option to save the entire design or the current page, and select or clear the Include Border and Include Title Block check boxes.
5. Click OK. Capture translates the design to a DXF file.

Using Partial Design Simulation

Using the Partial Design Simulation feature, you can:

- Identify individual components of any design and simulate only selected portions
- Simulate different circuits in the design with different simulation profiles
- Create netlist of only a particular portion of the design
- Compare and merge portions of a design quickly

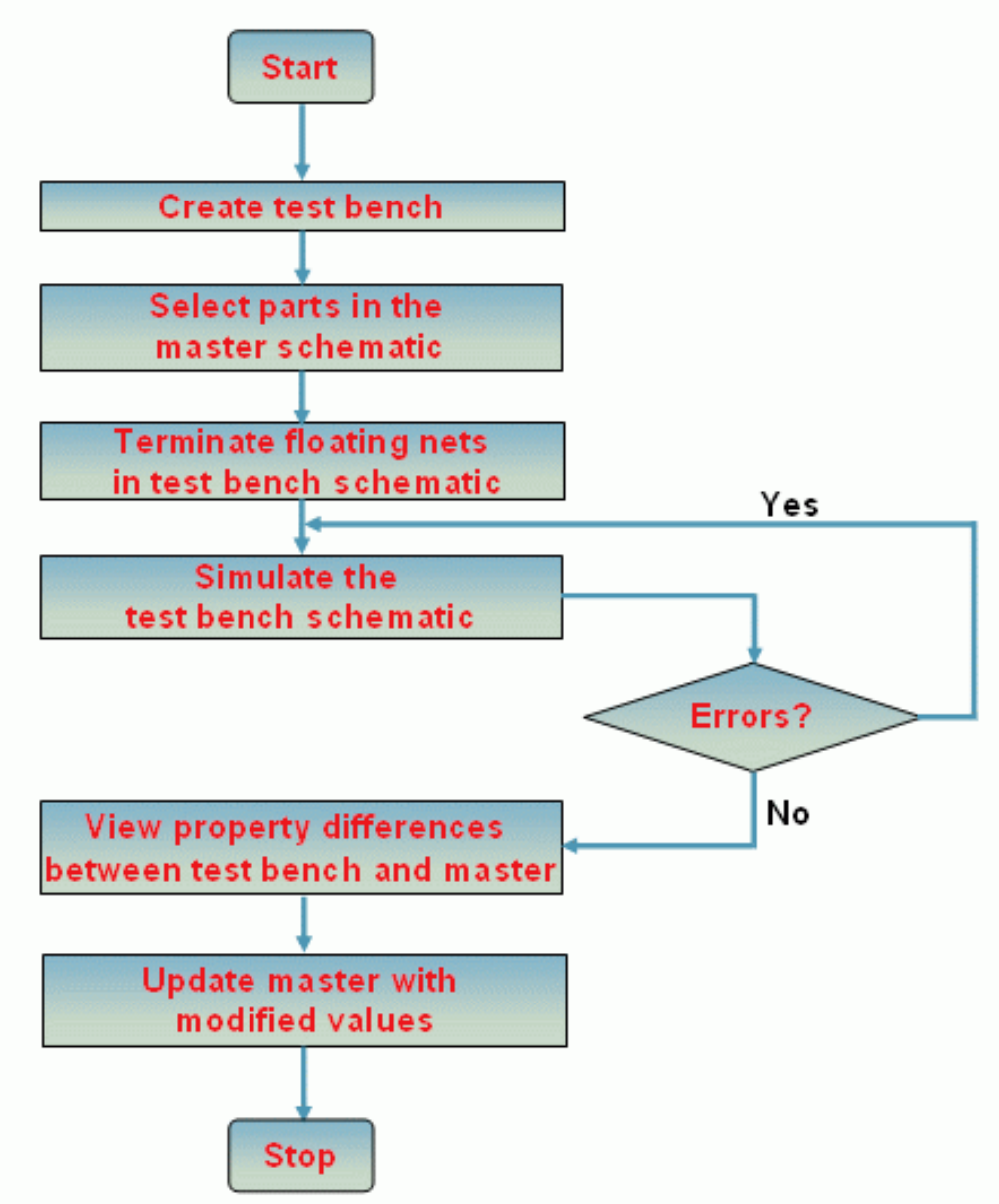
To use this feature, you select a portion called test bench of a master design. You create one or more test benches using the ToolsTest

Bench Create Test Bench menu of OrCAD Capture. The test benches are listed in the Project Manager window of the master design. You can add components from the design to a test bench by selecting them from the master schematic canvas, and then add profiles and simulate the test bench. You can also synchronize the master design with a test bench, to propagate any changes you make in the test bench design.

Note: The OrCAD Capture CIS license is required to use this feature.

You can use the Partial Design Simulation in the following flow, as shown in the figure:

1. Create a test bench
2. Select parts in the master schematic
3. Terminate floating nets in test bench schematic
4. Simulate the test bench schematic
5. View Property differences between test bench and master
6. Update master with modified values



The remaining sections explain these steps in detail.

Working with a Test Bench

A test bench is like any other new project created in Capture. When you create a test bench, it is listed under the *TestBenches* node in the project manager of the master project. All simulation profiles and

parameters or variables in the master project are copied by deafult to the test bench project. The components in the different schematics are greyed out. You can choose to activate the components to create a partial design.

You might need to add terminations and other parts to the partial design of the test bench because a test bench design must be complete in itself. You can also make edits to your test bench to prepare it for simulation by adding stimulus or simulation profiles. You can simulate a test bench even if the master design is not a PSpice project. If the master project is a PSpice project, the test bench can inherit the simulation profiles in the master project.

Creating a Test Bench

To create a Test Bench:

1. Select the DSN file in the Project Manager
2. Choose *Tools – Test Bench – Create Test Bench*

   The Test Bench Name box appears.
3. Enter a name in the *Enter Test Bench Name* field.

Tip

You can set a default test bench name by adding the *Default Test Bench Name* property in the [`TEST BENCH`] section of `capture.ini`. For example, to set the default test bench name to `MyTestBench`, add the following section in `capture.ini` :

```
[TEST BENCH]

Default Test Bench Name=MyTestBench
```

4. Click *OK*.

The test bench is added under *TestBenches* in the Project Manager. The test bench created contains all the designs in the master project.

The components in the schematic pages of the test bench are grayed out. You need to add components to the test bench to be able to work on a partial design.

Note: You can activate a test bench by right-clicking on the test bench in the Project Manager under Test Benches and choosing Make Active.

Activating Components

You can activate components in a test bench using any one of the options; context-menu for selected parts in the master design, conext-menu for selected parts in the test bench design, or from the hierarchy editor.

To activate components from the master design:

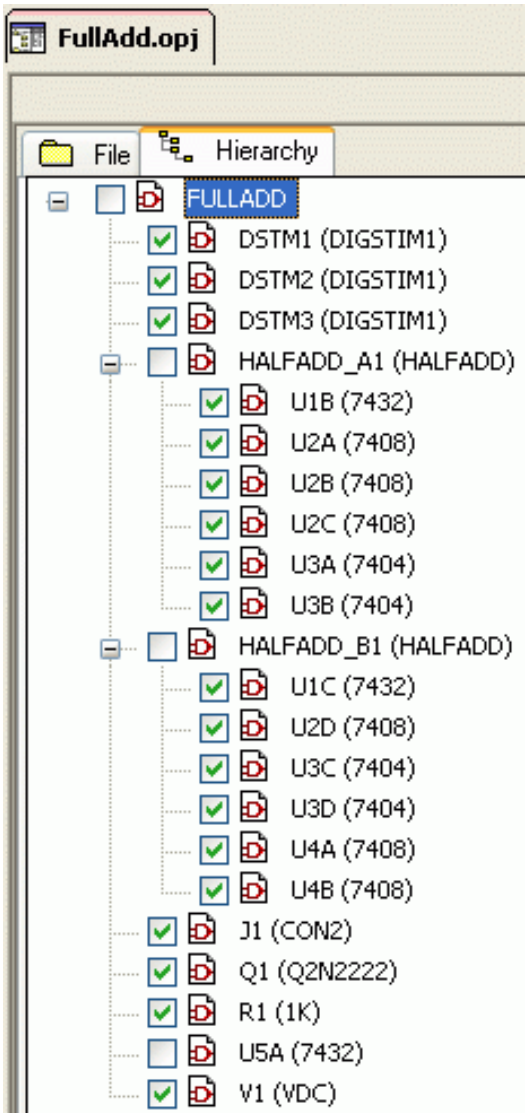
1. Select the components in the master design
2. Right-click and choose *TestBench – Add Part(s) to Active TestBench*

To activate components from the test bench design:

Select the components in the test bench design.

Right-click and choose *TestBench – Add Part(s) to Self*

To activate components using the hierarchy editor check the components to be added in the hierarchy editor of the master design, as shown in the figure.

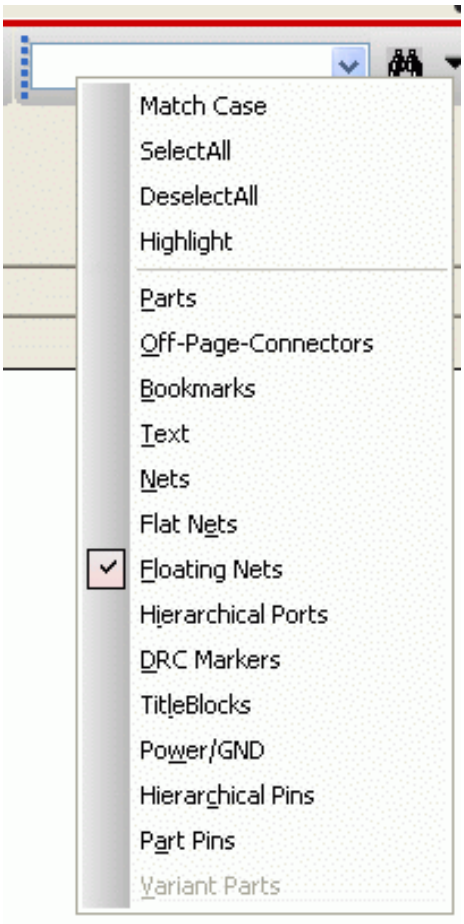


Similarly, you can inactivate a component from the test bench design from the context-menu or the hierarchy editor. Capture will ignore all components that are inactive. As a result, these inactive components will not be processed, for example, for simulation.

When you activate only a portion of the design, many nets might be floating because they are not terminated. You can easily resolve this problem by making a floating net search. To perform this search:

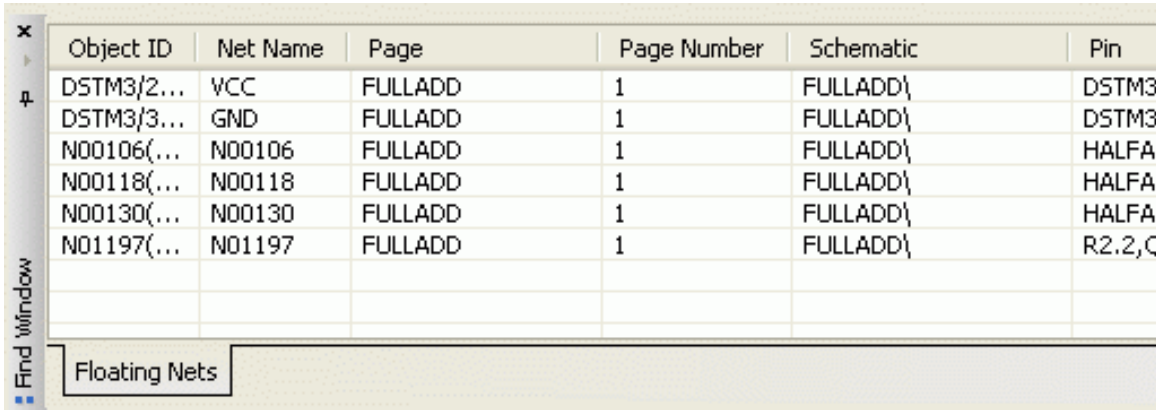
1. Select the test bench design in Capture

2. From the search menu select *Floating Nets* as shown in the figure



3. Click the Find button with the binocular shape.

   All the floating nets requiring terminators are listed in the Floating Nets tab of the Find Window



4. Double-click a row in the Find Window to select it in the design.

Comparing and Updating Master Design

You can compare the schematics in the master project and test bench to highlight the differendes using the SVS utility. This utility displays the differences and uses color code to highlight the type of change. The result window has two panels, the left panel represents the test bench. The differences listed are for the categories: unmatched object (yellow by default), missing objects (red by default), and matching objects (white in color). You can check any of the listed differences in the test bench panel, and propagate the changes to the master design. However, you cannot update a master design for missing objects.

You can click Settings ( ) to open the Settings dialog box and change the default colors in the *Color* tab. You can also filter for different objects, if you do not want them to be listed.

To compare and propagate changes:

1. Select the master DSN in Project Manager
2. Choose *Tools – Test Bench – Diff and Merge*

   The differences between the master design and the test bench design are displayed.

To update the master design with the test bench differences, check the differences you want to update in the *SVS* tab and click Accept Left ( ).

17

Saving and archiving

Capture provides functionality that allows you to easily save and archive your projects at each stage of development. This includes the ability to save designs and part libraries. You can also create a zip archive.

Saving a project, design, or library

When the project manager window is active, you can save a new or existing project, design, or library. The Save command saves all open documents referenced by the project, as well as the project itself.

Note: Except for occurrence properties, the schematics of externally-referenced libraries and designs should not be edited. You should view them as read-only designs. Trying to edit, then save, these designs from within your schematic can introduce errors such as duplicate reference designators and other problems.

When saving schematics with externally-referenced libraries or designs, occurrence properties are saved but altered instance values are not. If you want to change externally-referenced libraries or designs you should first close the referencing design. Then, open the referenced library or design, make the necessary changes, and save and close the referenced library or design. At this point, you can reopen the original design and reference the modified design.

The Save As command saves files depending on what you have selected in the project manager.

- If one or more designs or libraries are selected, you are prompted to save each file in turn.
- If no top-level folders (Design Resources or Outputs) are selected, and items other than designs or libraries are selected, the Save As command is unavailable.

- If no designs or libraries are selected in the project manager, you are prompted to save the project.

Note: When you use the Save As command, you are prompted to choose the file type from the Save As Type list in the Save As dialog box. You can choose to save the file in the current design database schema version or in a schema version that is one version prior to the application version you are currently using.

To save a new design or library

1. With the design or library selected in the project manager, from the File menu, choose Save. The Save As dialog box displays.
2. Enter a name for the design or library in the File name text box, specify a location, then choose the Save button.

The design or library is saved, and the project manager remains open. When you close the project, Capture prompts you to save the project file.

To save an existing project

➤ With the Design Resources or Output folder selected, choose Save from the File menu.

The project is saved, and remains open in the Capture session frame.

When you save a project, you are saving all the files residing in the project. If you have several pages open in schematic page editor windows, changes you have made to any of them are saved. In addition, changes made by the Capture tools are saved to disk.

To save one project

➤ From the File menu of the project manager, choose Save. If the project is new and has not yet been saved, the Save As dialog box appears, giving you the opportunity to specify a drive and replace the system-generated name.

Note: When you save a project, Capture automatically creates a backup with a .DBK file extension. When you save a library, Capture automatically creates a backup with a .OBK file extension. If you save only a schematic page or a part, no backup is generated.

A Capture a design file (.DSN) is always accompanied by a project file (.OPJ). Each time you use the Save As command from the File menu to save a design file to another name or directory, you should also use Save As for the project file. The following process saves a .DSN file and a .OPJ file into the same directory so you can continue editing the current project without altering the original files.

To save a project file along with the design file

1. In the project manager, select the design file.
2. From the File menu, choose Save As.
3. Change the drive and directory as appropriate, select the file name, then click Save.
4. In the project manager, select the Design Resources folder.
5. From the File menu, choose Save As.
6. Change the drive and directory as appropriate, select the file name, then click Save.

Shortcut

Toolbar:

Changes you make to a schematic page are temporary until you save the page or the project to disk using one of the commands of the File menu. If you save one schematic page, all of the pages in the schematic are saved. If you save a project while you have several pages open in schematic page editor windows, changes you have made to any of them are saved as well as any changes made by the Capture tools.

To save one schematic page

➤ From the File menu of the schematic page editor, choose the Save command. If the design is new and has not yet been saved, the Save As dialog box appears, giving you the opportunity to specify a drive and replace the system-generated name.

To save one design

➤ From the File menu of the project manager, choose the Save command. If the design is new and has not yet been saved, the Save As dialog box appears, giving you the opportunity to specify a drive and replace the system-generated name.

Note: When you save a project, Capture automatically creates a backup with a .DBK file extension. When you save a library, Capture automatically creates a backup with a .OBK file extension. If you save only a schematic page or a part, no backup is generated.

Archiving

You can save the project (.OPJ) and all the related files (design, library, output files, and referenced projects) in a different directory and also create a zip file of this directory for archival purposes. You can also specify any additional files or directories that you may want to be archived along with your project files. For example, you can archive external designs, global PSpice model libraries, and global include files along with your PSpice project or data sheets for the parts. For more information, see "To add additional files and directories to the archive" on page 703.

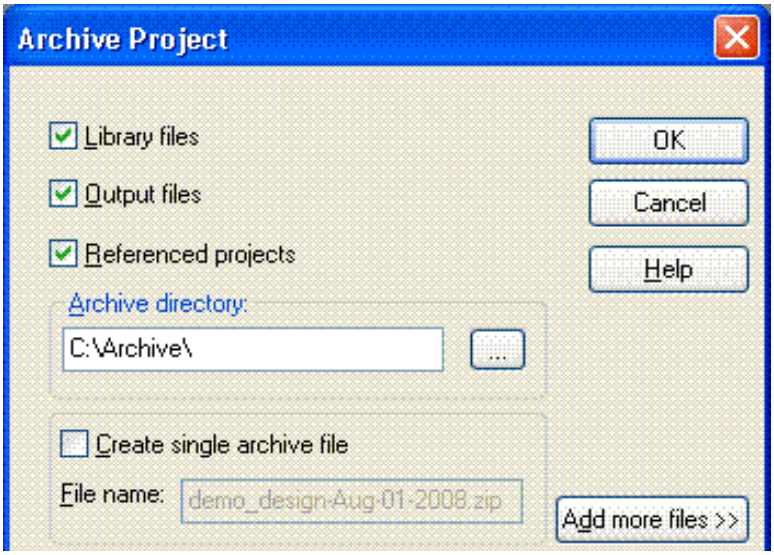
You can use the Archive Project command on the File menu to archive your project. This command will allow you to save all the files related to your project in the directory you specify for archival and zip the directory into a single zip file, which will have a *.zip* extension. You can use the WinZip software to unzip zip archives created using Capture.

Note: The path names of the files and directories in the archive file are relative to the archive directory. This implies that when the archive file is unzipped on a different machine the files and directories retain the original directory structure of the archive directory.

To archive a project

1. Make sure that the project you want to archive is active and the schematic pages for the project are not open.

2. From the File menu, choose Archive Project. The Archive Project dialog box appears.



3. Select the files you want to be archived with your project. If you do not select any of the options (Library files, Output files, or Referenced projects), Capture by default archives only your project (.OPJ) and design (.DSN) files.

   Note: For PSpice projects, the simulation profiles and local files (.LIB, .STL, .INC) will all be archived along with the project. The Output files option also archives simulation output files such as .DAT and .OUT for PSpice projects. The archiving methodology for PSpice model libraries is as follows:

   - Profile-level model libraries are archived under their respective profiles and referenced as *.\<library_name>.lib*.

     For example, when a profile; AC containing a model library *diode.lib* is archived, the *diode.lib* is copied under the directory *AC* and the simulation settings is modified as: `.\diode.lib`.

   - Design-level model libraries are archived under `.\<design_name-pspicefiles>\<design_name>\<library_name>.lib`.

     For example, when a design called *histo* containing a model library *bipolar.lib* is archived, the model library *bipolar.lib* is copied under directory

`histo-pspicefiles\histo` and the simulation settings is modified as: `.\histo-pspicefiles\histo\bipolar.lib`.

- In case of global-level model libraries:
  - a copy of model library is created under the existing *<design_name>.lib (*if exists).
  - a new *<design_name>.lib* file is created and a copy of model library is added to the *<design_name>lib* and the simulation setting is modified as design-level library.

4. Click the **...** button to find the directory to which you will save your files. The Select Directory dialog box appears.

   Note: You can also enter the relative path of the archive directory in the Archive directory text box. This path is treated as relative to the project being archived.

5. Find and select the directory in which you want your project archived and click OK. If necessary, create the directory.

6. Click OK in the Archive Project dialog box. Capture archives your project with all the selected files to the specified directory and displays information/errors in the Session Log.

Note: The working directory does not change to the newly set archive directory.

Note: The settings you specify in the Archive Project dialog box get saved in the CAPTURE.INI file. These settings are used whenever you start the next archive session.

To create a zip archive for the project

1. Make sure that the project you want to archive is active and the schematic pages for the project are not open.

2. From the File menu, choose Archive Project. The Archive Project dialog box appears.

3. Set the directory to which you want to save all project files as described in "To archive a project" on page 700.

4. Select the Create single archive file check box to activate the File name text box.
5. Specify a file name for the zip archive file in the File name text box.

   Note: The default file name for the zip archive file is <projectname-current date>. The file extension (.zip) is automatically added to the zip archive file.
6. Click OK. Capture zips all the files in the specified directory and generates a zip file with .zip extension. The Session Log displays all the events that occur during the archiving process and report whether the process completed successfully or with errors.

Note: The working directory does not change to the newly set archive directory.

Note: You can unzip the zip archive using the WinZip software.

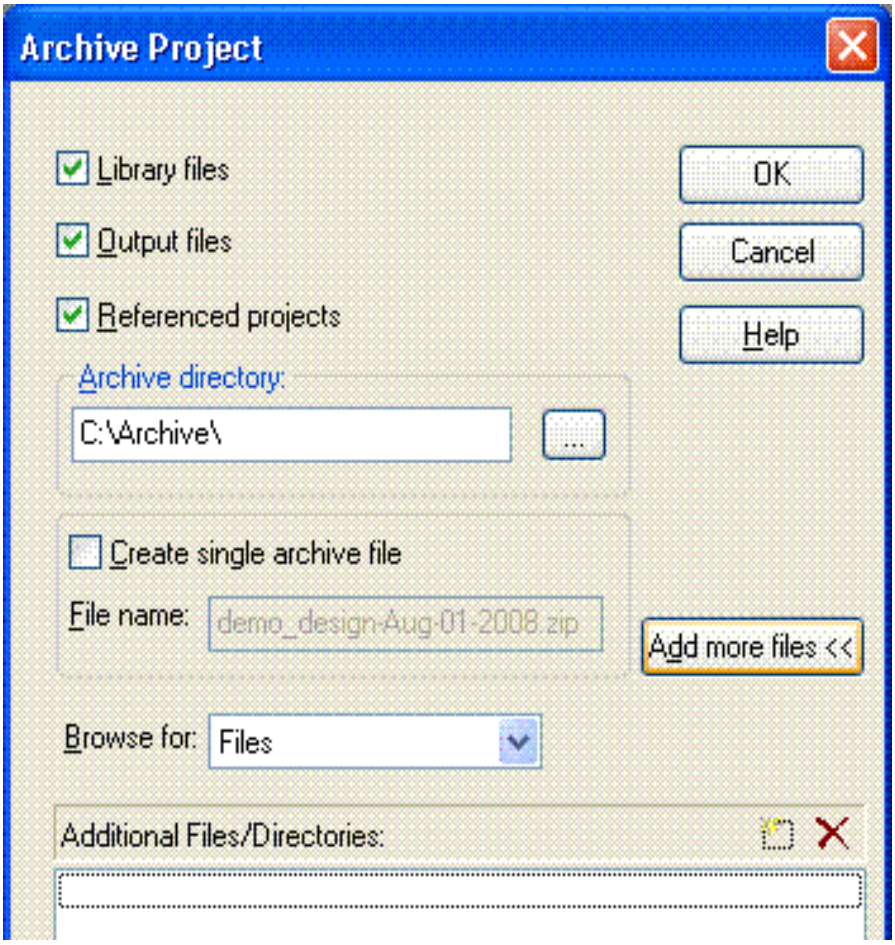
Note: Archiving to a single file with a .zip extension does not compress the contents.

To add additional files and directories to the archive

1. Make sure that the project you want to archive is active and the schematic pages for the project are not open.
2. From the File menu, choose Archive Project. The Archive Project dialog box appears.
3. Set the directory to which you want to save all project files as described in "To archive a project" on page 700.
4. Click the Add more files >> button. The Archive Project dialog box expands and displays a grid where you can add more files and directories.

   Note: Click the Add more files << button to revert the Archive Project dialog box to its default state.
5. Select an option from the Browse for list box. Select the Directories option to add directories or the Files option to add more files to your archive. The Files options is the default selection.

6. Click the button or press the Insert keyboard key. An edit box with a blinking cursor appears in the Additional Files/Directories list.



7. Click the **...** button to locate the files or directories you want to add in the archive. A file or directory selection dialog box appears depending on your selection in the Browse for list box. For example, if you selected the Directories option, then the Select Directory dialog box appears. Otherwise, the Select File (s) dialog box appears.

8. Find and select the file or directory to be added to your archive. The location path of the selected file or directory is added in the Additional Files/Directories list.

   Note: Do not enter relative path for files or directories in the Additional Files/Directories list.

Note: You can use the standard CTRL or SHIFT keys to select multiple files in the Select File (s) dialog box.

Note: You can also select multiple files by dragging the left mouse button over the files you want to select in the Select File (s) dialog box. You cannot use this method to select multiple directories in the Select Directory dialog box.

Note: If you finished adding files and want to add directories now and vice-versa, you must select an appropriate option from the Browse for list box.

Note: The Additional Files/Directories list displays information based on your selection in the Browse for list box, that is, if your selection is Directories then only the directories added to the list are displayed and vice-versa.

Note: Use the button or press the Delete keyboard key to delete the files or directories you do not want in the Additional Files/Directories list.

Note: The archiving mechanism ensures that duplicate files or directories do not get added to the Additional Files/Directories list.

9. Click OK in the Archive Project dialog box. Capture archives your project with all the selected additional files and directories to the specified directory. The working directory does not change to the newly set archive directory. For information on how to create a zip archive file, see "To create a zip archive for the project" on page 702.

Note: The files and directories you add using the Additional Files/Directories list are added to the archive directory under a separate sub-directory called *Additional files.*

Note: The archived project (.OPJ) file does not contain references to the additional files and directories added using the Additional Files/Directories list.

Note: The settings you specify in the Archive Project dialog box get saved in the CAPTURE.INI file. The settings are used whenever you start the next archive session except for the files and directories list in the Additional Files/Directories list.

18

Project manager command reference

This chapter covers:

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- “Design menu” on page 716
- “Edit menu” on page 726
- “View” on page 740
- “Tools menu” on page 745
- “PICFlow menu” on page 760
- “PSpice” on page 761
- “Advanced Analysis menu” on page 767
- “Accessories menu” on page 770
- “Options menu” on page 775
- “Window menu” on page 776
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File menu

“New command” on page 708

“Open command” on page 709

“Close Project command” on page 710

“Save command” on page 711

"Check and Save command" on page 711

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"Print Preview command" on page 713

"Print command" on page 713

"Print Setup command" on page 713

"Import Design command" on page 714

"Export Design command" on page 714

"1,2,3,4 command" on page 715

"Change Product command" on page 715

"Exit command" on page 715

New command

Available from: File menu

Function:

Use this command to create a new project, design, library, or VHDL file. Choose a command from the menu that appears:

- Project
- Design
- Library
- VHDL File
- Verilog File

The number of open windows you can have is only limited by your available system resources. You can use the Window menu to switch among open windows (see1,2.... command).

You can open an existing project, design, library, or VHDL file using the Open command on the File menu.

Note: If you click the Create document toolbar button from the project manager window, the New Project dialog box appears.

Shortcuts:

Toolbar:

Keyboard: ALT, F, N

Open command

Available from:

File menu

Function:

Use this command to open an existing project, design, library, VHDL, or Verilog file in a new window. Choose a command from the menu that appears:

- Project
- Design
- Library
- Project
- VHDL File
- Verilog File

The number of open windows you can have is only limited by your available system resources. You can use the Window menu to switch among open windows (see 1,2.... command).

You can create a new design, library, VHDL, or Verilog file using the New command on the File menu.

Note: When you click the Open button on the toolbar, a standard Windows Open dialog box appears, in which you can choose the type of file you want to open in the Files of type drop-down list. Among the listed choices are SDT Schematic (*.SCH) and SDT Library (*.LIB).

Shortcuts:

Toolbar:

Keyboard: ALT, F, O

Close Project command

Available from: File menu

Function: Use this command to close the active window. If necessary, you are prompted to save your changes.

Shortcuts: Keyboard: ALT, F, C

Save command

Available from: File menu

Function: Use this command to save the active, modified projects, designs, libraries, and VHDL files. You can save a design, library, VHDL file, or session log under a different name using the Save As command on the File menu.

Note: When you save a project, Capture automatically creates a backup with a .DBK file extension. When you save a library, Capture automatically creates a backup with a.OBK file extension. If you save only a schematic page or part, no backup is generated.

Shortcuts: Toolbar:

Keyboard: ALT, F, S or CTRL+S

Check and Save command

Available from: File menu

Function: Use this command to execute the design rules check and save the design. The design rules check is executed with the electrical design rules currently defined in the Design Rules Check dialog.

Shortcuts: Keyboard: ALT, F, N

Save As command

Available from: File menu

Function:

Use this command to save the active project, design, library, VHDL file, or session log under a different name or to save a new, unnamed project, design, library, VHDL file, or session log. You can save a design, library, schematic page, part, or session log with the Save command on the File menu.

The Save As command opens a standard Windows dialog box to save files.

Note: When you save a project, Capture automatically creates a backup with a .DBK file extension. When you save a library, Capture automatically creates a backup with a.OBK file extension. If you save only a schematic page or part, no backup is generated.

Note: When you use the Save As command, you are prompted to choose the file type from the Save As Type list in the Save As dialog box. You can choose to save the file in the current design database schema version or in a schema version that is one version prior to the application version you are currently using.

Shortcuts: Keyboard: ALT, F, A

Archive Project command

Available from: File menu

Function:

Use this command to save the project (*.OPJ) and all the related files (design (*.DSN), library (*.OLB), and referenced projects) in a different directory and create a zip archive (.zip) of this directory for archival purposes.

You can also specify any additional files or directories that you may want to be archived along with your project files.

You can include output files and library files (like *.OLB files in the Library folder and *.VHD files).

Shortcuts: Keyboard: ALT, F, H

Print Preview command

Available from: File menu

Function: Use this command to see how a schematic page or part will look when printed.

After setting the options in the Print Preview dialog box, click OK to preview the printed document. You can use the buttons at the top of the window to view different pages and to zoom in and out.

Note: Be prepared to wait if you attempt to print multiple pages or parts. Depending on the number and size of the pages or parts you are previewing, Capture may require extra time to display the selection.

Shortcuts: Keyboard: ALT, F, V

Print command

Available from: File menu

Function: Use this command to print the active schematic page, the active part, or the selected items in the project manager.

Note: When you print multiple copies, the copies are grouped by page, not sorted by copy.

Shortcuts: Toolbar:

Keyboard: ALT, F, P or CTRL+P

Print Setup command

Available from: File menu

Function: Use this command to choose a printer, paper source, and orientation before printing. The Print Setup command displays the Print Setup dialog box, a standard windows dialog box for configuring your printer or plotter. For more information on setting up printers and plotters, refer to the documentation for your configured printer driver.

Tip

Many times, the options for your printer are not available in the standard setup dialog box. If you do not find the options you need, try the printer setup in the Windows Control Panel.

Shortcuts: Keyboard: ALT, F, R

Import Design command

Available from: File menu

Function: Use this command to import EDIF, PDIF and PSpice designs. EDIF designs must be graphical EDIF designs, and not EDIF netlists. Not all imported PDIF parts may be edited in Capture. Such parts won't affect netlists.

Export Design command

Available from: File menu

Function: Use this command to export EDIF designs and DXF schematic pages. This command saves EDIF designs as graphical EDIF designs, and not EDIF netlists. DXF schematic pages are saved in AutoCAD's V12 file format.

1,2,3,4 command

Available from: File menu

Function: Use the numbers listed at the bottom of the File menu to open one of the last four projects or files. Choose the file you want to open.

Shortcuts: Keyboard: ALT, F, N (n = 1, 2, 3, or 4)

Change Product command

Available from: File menu

Use this command to select a product suite from which to open Capture without having to exit the tool.

This command is not available if you have a project open in Capture.

Function: Select the Use as default check box to set the default product suite from which Capture should check out a license each time you start the tool. If this option is selected, then the suite selection dialog box will not appear the next time you start the tool. However, if you want the suite selection dialog box to be displayed again then clear the Use as default check box in the suite selection dialog box.

Shortcuts: Keyboard: ALT, F, C

Exit command

Available from: File menu

Function:

Use this command to exit the software. If necessary, you are prompted to save your changes.

You can also exit the software by choosing the Close command on the session frame Control menu (ALT, SPACEBAR, C).

Shortcuts:

Keyboard:

ALT, F, X

ALT, SPACEBAR, C

ALT+F4

Design menu

"New Schematic Design command" on page 717

"New Schematic Page command" on page 717

"New VHDL File command" on page 717

"New Part command" on page 718

New Part from Spreadsheet command on page 719

"New Symbol command" on page 719

"Rename command" on page 720

"Delete command (Design menu)" on page 720

"Remove Occurrence Properties command" on page 721

"Make Root command" on page 721

"Replace Cache command" on page 722

"Update Cache command" on page 724

"Cleanup Cache command" on page 726

New Schematic Design command

Available from: Design menu

Function: Use this command to create a schematic folder in the active project.

You can add a new schematic page to the selected schematic folder using the New Schematic Page command on the Design menu.

Note: Schematic folder, schematic page, part, part alias, and symbol names are completely case sensitive. It is possible to have a part named "XYZ" and another one named "xyz," and Capture's tools will treat the two separately.

Shortcuts: Keyboard: ALT, D, S

New Schematic Page command

Available from: Design menu

Function: Use this command to add a new schematic page to the selected schematic folder.

You can add a new schematic folder to the active project using the New Schematic command on the Design menu.

Note: Schematic folder, schematic page, part, part alias, and symbol names are completely case sensitive. It is possible to have a part named "XYZ" and another one named "xyz," and Capture's tools will treat the two separately.

Shortcuts: Keyboard: ALT, D, P

New VHDL File command

Available from: Design menu

Function: Use this command to create a new VHDL file in the active project.

Shortcuts: Keyboard: ALT, D, V

New Verilog File command

Available from: Design menu

Function: Use this command to create a new VHDL file in the active project.

Shortcuts: Keyboard: ALT, D, V

New Part command

Available from: Design menu

Function: Use this command to create a part in the active library. Part aliases are created at the same time as the original part and show up in the library independently from the original part, but are represented in the project manager by a part icon with a horizontal line through the center. You can add part aliases to a library after the original part is created using the Package Properties command.

Note: Schematic folder, schematic page, part, part alias, and symbol names are completely case sensitive. It is possible to have a part named "XYZ" and another one named "xyz," and Capture's tools will treat the two separately.

Tip

You can use an existing part as a model for a new part by moving a copy of the part to a second library and then editing the copy. If you wish to have the new part in the original library, rename the new part, then move it to the original library.

Shortcuts: Keyboard: ALT, D, T

New Part from Spreadsheet command

Available from: Design menu

Function: Use this command to create a new part in the active library.

Shortcuts: Keyboard: ALT, D, H

New Symbol command

Available from: Design menu

Function: Use this command to create a symbol in the active library.

Note: Schematic folder, schematic page, part, part alias, and symbol names are completely case sensitive. It is possible to have a part named "XYZ" and another one named "xyz," and Capture's tools will treat the two separately.

Shortcuts: Keyboard: ALT, D, L

Rename command

Available from: Design menu

Function: Use this command to change the name of the selected schematic folder, schematic page, or part. If you rename a power or ground symbol using this command, the name is limited to 31 characters.

Shortcuts: Keyboard: ALT, D, R

Delete command (Design menu)

Available from: Design menu

Function: Use this command to delete the selected schematic folders, schematic pages, parts, and symbols that are listed in the project manager window.

Deleting schematic folders, schematic pages, parts, and symbols is permanent. You cannot use the Undo command ***to bring back deleted items from the project manager.***

Shortcuts: Keyboard:

ALT, D, D

BACKSPACE

DEL

DELETE

Remove Occurrence Properties command

Available from: Design menu

Function: Use this command to remove all the unique annotations you have placed on parts if your schematic design part references are no longer synchronized with your PCB project. To correct this problem, back annotate your PCB in PCB Editor to create a swap (.SWP) file. Then, in Capture, use Back Annotate.

Note: The following changes will be lost using this command:

- inherent properties on occurrences
- user-define properties on occurrences
- gate or pin swaps unique to the part occurrences
- occurrence properties on title blocks, pins, and nets

You can use the property editor to find occurrence properties on objects in your design.

Shortcuts: Keyboard: ALT, D, O

Make Root command

Available from: Design menu

Function: Use this command to designate the selected schematic folder as the root schematic folder of the hierarchy.

Shortcuts: Keyboard: ALT, D, M

Important

If you haven't specified a root for your design, you cannot generate reports. Also, when folders are copied to a new design, the ROOT designation is lost and must be reestablished in the design.

Replace Cache command

Available from: Design menu

Function: Use this command to replace the selected part in the design cache, based on its current definition in any library. You can also use this command to replace a selected part in the cache with a different part.

Important

When you replace a selected part in the design cache, make sure the part library is correct before you change the part name to the library part name. If more than one part is selected in the design cache, you can use the Replace Cache command to replace them, but the Part name field will not be available.

When you replace a part in the design cache, you replace all the parts in the active design that share the same part value and library. If the replaced part displays on an open schematic page, the parts on that page do not change until the page is closed and then reopened.

Note: If you select all the parts in the design cache and execute the Replace Cache command to replace parts from a new library in which one of the parts doesn't exist, the execution will quit when it gets to that part. Parts below it will not be replaced in the cache.

Using the Replace Cache dialog box, you can choose to preserve schematic part properties or replace schematic part properties.

If you select the action to **Preserve schematic part properties**, Capture brings in the graphics, pins, package properties, and part properties from the library while retaining all instance and occurrence properties of the schematic part in the design. The part reference changes to an unannotated reference (?), and the value becomes the new part name. If you look at the property editor Parts tab, you will also see that the package property value appears in the PCB Footprint property column. You will lose any changes made to the pin properties after the part was placed, including those made by the Back Annotate or the Annotate tools.

Note: Using the Preserve schematic part properties option with the Replace Cache command causes the same behavior as the default Replace Cache command in Capture Release 9 and earlier.

If you select the action to **Replace schematic part properties**, Capture brings in graphics, pins, package properties, and user properties from the library, totally replacing the schematic part in the design. Any value, PCB footprint, part reference, and instance or occurrence property defined on the schematic page will not change. Remember that instance and occurrence properties always obscure library definitions.

When you select the **Replace schematic part properties** option, the Preserver Refdes checkbox is enabled for selection. If you select this checkbox, you can preserve the reference designator of parts and/or symbols that you want to change. However, the PCB Footrpint/Package properties are updated only if the Preserve Refdes check box is unselected.

Note: The Replace Cache and Update Cache commands are quite similar. However, there are a couple of significant differences between the two commands. You can modify a part's link to the library (part name, path, and library) with Replace Cache, but not with Update Cache. Update cache only brings in new data when the path has changed. Another difference is that if the path and library names do not change, Replace Cache reloads the part definition into the design. However, if Update Cache finds that the part name and the library names are the same, it does not bring in part changes.

Tip

If you need to know a part's library of origin, you can select the part in the project manager, then select Replace Cache from the Design menu. The part name and the library and path are listed in the dialog box that appears. Click Cancel to return to the project manager.

You can discover the library of origin for multiple parts by Creating a cross reference report.

Shortcuts: Keyboard: ALT, D, C

Update Cache command

Available from: Design menu

Function:

Use this command to update the selected parts in the design cache, based on their current definitions in their original libraries. This command works when one or more parts are selected.

When you change a part in the design cache, you change all the parts in the active design that share the same part value and library. Part properties are retained, but pin properties are not. If the modified part appears on an open schematic page, the parts on that page do not change until the page is closed and reopened.

If you copy pages from one design or library to another, parts displayed on the copied pages may appear different due to differences in each design or library cache. If a part is not already in the destination design cache, Capture will copy it from the source design's cache. Otherwise, it will use the part already present in the destination design's cache.

Note: The Replace Cache and Update Cache commands are quite similar. However, there are a couple of significant differences between the two commands. You can modify a part's link to the library (part name, path, and library) with Replace Cache, but not with Update Cache. Update cache only brings in new data when the path has changed. Another difference is that if the path and library names do not change, Replace Cache reloads the part definition into the design. However, if Update Cache finds that the part name and the library names are the same, it does not bring in part changes.

Tip

If you need to know a part's library of origin, you can select the part in the project manager, then select Replace Cache from the Design menu. The part name and the library and path are listed in the dialog box that appears. Click Cancel to return to the project manager.

You can discover the library of origin for multiple parts by Creating a cross reference report.

Shortcuts:

Keyboard: ALT, D, U

Cleanup Cache command

Available from:	Design menu
Function:	Use this command to cleanup the design cache. This command removes nonexistent parts from the cache.
Shortcuts:	Keyboard: ALT, D, N

Edit menu

"Cut command" on page 727

"Copy command" on page 727

"Paste command" on page 728

"Project command" on page 729

"Properties command" on page 729

"Object Properties command" on page 731

"Browse command" on page 732

"Power Pins command" on page 737

"Rename Part Property command" on page 738

"Go To command" on page 740

"Clear Session Log command" on page 740

"Delete Part Property command" on page 739

"Replace command" on page 739

Cut command

Available from: Edit menu

Use this command to remove the selected object from the active window and put it on the Clipboard. This command is only available when an object is selected.

Function: Cutting objects to the Clipboard replaces any objects previously stored there. Use the Paste command to copy objects to another page or part, or to another Windows application that supports pasting from the Clipboard.

Note: The Cut and Copy command are unavailable in the part editor when you have one or more pins selected with other objects (such as an arcs and lines).

Toolbar:

Shortcuts: Keyboard: ALT, E, T or CTRL+X

Pop-up menu: Cut

Copy command

Available from: Edit menu

Use this command to copy a selected object to the Clipboard without removing it from the active window. This command is available only if an object is selected.

Function: Copying objects to the Clipboard replaces any objects previously stored there. Use the Paste command to copy objects to another page or part, or to another Windows application that supports pasting from the Clipboard.

Note: The Cut and Copy commands are unavailable in the part editor when you have one or more pins selected with other objects (such as arcs and lines).

Toolbar:

Shortcuts: Keyboard: ALT, E, C or CTRL+C

Pop-up menu: Copy

Paste command

Available from: Edit menu

Use this command to place any objects stored on the Clipboard into the active window. This command is unavailable if the Clipboard is empty.

Function: Pasting objects from the Clipboard does not affect the Clipboard's contents. Use Paste to copy objects to another page or part, or to another Windows application that supports pasting from the Clipboard. You can only paste text into text boxes.

Note: If you copy a part into the Clipboard and then paste it onto a schematic page, Capture will automatically assign a unique reference designator to the pasted part when two conditions are met:

1. The Auto Reference option on the Miscellaneous tab of the Preferences dialog box is selected.
2. The pasted part has a reference designator assigned to it when it is copied to the Clipboard.

Capture assigns the reference designator, updated to the next available value (one greater than the highest value used on the schematic at that point.) If the pasted part has a default reference (for example, R?) Capture does not assign a unique reference designator to it.

Toolbar:

Shortcuts: Keyboard: ALT, E, P or CTRL+V

Pop-up menu: Paste

Project command

Available from: Edit menu

Function: Use this command to add resources to your project. When you choose this command, the <Bold Sans> Add file to Project Folder dialog box (continued) appears, in which you can locate and select files to add to your project. The files are added to the folder that is currently selected in the project manager window.

This command is only available when the File tab is active in the project manager window.

Shortcuts: Keyboard: ALT, E, R

Properties command

Available from: Edit menu

Function: In the project manager, use this command to view properties about the selected document. Using the Properties dialog box, you can access information general, type, and project about the file that is currently selected in the project manager window. You can also change the file's type. A file or project must be selected in the project manager window to access the Properties command.

In the schematic page and part editors, use this command to open the property editor, where you can edit properties and other data for the selected objects.

The properties you can edit depend on the selected objects. The following lists the inherent properties you can edit and the dialog boxes in which you edit them:

Objects	Dialog Box
Arcs	Edit Graphic dialog box
Images (pictures)	Not applicable

Objects	Dialog Box
Bookmarks	Edit Bookmark dialog box
Buses Property editor	Property editor
Bus entries	User Properties dialog box
DRC markers	View DRC Marker dialog box
Ellipses	Edit Filled Graphic dialog box
Hierarchical blocks	Property editor
Hierarchical pins	Property editor
Hierarchical ports	Property editor
IEEE symbols	Place IEEE Symbol dialog box
Junctions	Not applicable
Lines	Edit Graphic dialog box
Multiple objects	Property editor or Browse spreadsheet editor
Nets (wires and buses	Property editor
Net aliases	Property editor
No connects	Not applicable
Off-page connectors	Edit Off-Page Connector dialog box
Parts	Property editor
Pictures (images)	Not applicable
Part body borders	Not applicable
Pins (part editor)	Pin Properties dialog box (part editor)
Pins (schematic page editor)	Property editor
Polygons	Edit Filled Graphic dialog box
Polylines	Edit Graphic dialog box
Power, ground	Property editor
Rectangles	Edit Filled Graphic dialog box
Text	Place Text dialog box
Title blocks	Property editor

Objects	Dialog Box
Wires	Property editor

Note: You can edit homogeneous sets of the following objects in the spreadsheet editor:

- Bookmarks
- DRC markers
- Hierarchical ports
- Nets
- Off-page connectors
- Parts
- Pins

Shortcuts:

Keyboard: ALT, E, I or CTRL+E

Mouse: Double-click on a part

Pop-up menu: Edit Properties

Object Properties command

Available from: Edit menu

Function:

Use this command to open the Property editor window for a design. You can use the property editor window to edit part, net, pin, title block, global, port, and alias properties.

This command is available only when you have selected any one of the following items in the Project manager window:

- Design file (.dsn)
- Schematic folder
- Schematic page

You can access the Edit Object Properties command from pop-up menu.

Shortcuts: Keyboard: ALT, E, O

Browse command

Available from: Edit menu

Function:

Use this command in the project manager to specify which items to search for and how to sort the results. Choose a command from the menu that appears:

- Parts command
- Nets command
- Hierarchical Ports command
- Off-page Connectors command
- Titleblocks command
- Bookmarks command
- DRC Markers command
- Flat Netlist command
- Power Pins command

You can open a schematic page or part by double-clicking on the selected item. You can also choose properties to edit and change one or more items.

Shortcuts: Keyboard: ALT, E, B

Parts command

Available from: Edit menu, Browse command

Function:

Use this command to list the parts of the selected schematic pages in the browse window. The Browse Properties dialog box gives you the option to use instances or occurrences.

You can sort the parts in the browser spreadsheet by clicking the button at the top of each column in the browse window. Capture only displays the occurrences of the parts in the browse window.

You can select single or multiple parts and edit them with the Properties command. When you edit one part, a part editor window appears. When you select multiple parts, the Browse spreadsheet editor appears.

Shortcuts: Keyboard: ALT, E, B, P

Nets command

Available from: Edit menu, Browse command

Use this command to list the nets of the selected schematic pages in the browse window. Capture only displays the occurrences of the nets in the browse window.

Function: You can select single or multiple nets and edit them with the Properties command. When you edit nets, the property editor window appears.

Double-click on a net to view it in the schematic page editor.

Shortcuts: Keyboard: ALT, E, B, N

Hierarchical Ports command

Available from: Edit menu, Browse command

Use this command to list the hierarchical ports of the selected schematic pages in the browse window. You can use this command to follow ports through a hierarchy when tracing problems in a hierarchical design.

Function: You can select single or multiple hierarchical ports and edit them with the Properties command. When you edit one hierarchical port, the Edit Hierarchical Port dialog box appears. When you select multiple hierarchical ports, the Edit Properties dialog box appears.

Double-click on a hierarchical port to view it in the schematic page editor.

Shortcuts: Keyboard: ALT, E, B, H

Off-page Connectors command

Available from: Edit menu, Browse command

Function: Use this command to list the off-page connectors of the selected schematic pages in the browse window. You can use this command to follow nets as they travel through off-page connectors to other pages.

You can select single or multiple off-page connectors and edit them with the Properties command. When you edit one off-page connector, the Edit Off-Page Connector dialog box appears. When you select multiple off-page connectors, the Browse spreadsheet editor appears.

Double-click on an off-page connector to view it in the schematic page editor.

Shortcuts: Keyboard: ALT, E, B, O

Titleblocks command

Available from: Edit menu, Browse command

Function: Use this command to list the title blocks of the selected schematic pages in the browse window. When you edit a title block, the User Properties dialog box appears. Double-click on a title block to view it in the schematic page editor.

Shortcuts: Keyboard: ALT, E, B, T

Bookmarks command

Available from: Edit menu, Browse command

Function: Use this command to list the bookmarks of the selected schematic pages in the browse window. Bookmarks are useful for marking a particular spot in your design.

You can select single or multiple bookmarks and edit them with the Properties command. When you edit one bookmark, the Edit Bookmark dialog box appears. When you select multiple bookmarks, the Edit Part Properties dialog box appears.

Double-click on a bookmark to view it in the schematic page editor.

Shortcuts: Keyboard: ALT, E, B, B

DRC Markers command

Available from: Edit menu, Browse command

Function: Use this command to list the DRC markers of the selected schematic pages in the browse window. DRC markers are placed on pages by the Design Rules Check tool. They are useful when troubleshooting your design before creating a netlist.

You can select single or multiple DRC markers and edit them with the Properties command. When you edit one DRC marker, the View DRC Marker dialog box appears. When you select multiple DRC markers, the Browse spreadsheet editor appears.

Double-click on an DRC marker to view it in the schematic page editor.

Shortcuts: Keyboard: ALT, E, B, D

Flat Netlist command

Available from: Edit menu, Browse command

Use this command to list the nets of the design, as they will appear in a netlist.

Function: You can select single or multiple nets and edit them with the Properties command. When you edit nets, the property editor window appears.

Double-click on a net to view it in the schematic page editor.

Shortcuts: Keyboard: ALT, E, B, F

Power Pins command

Available from: Edit menu, Browse command

Use this command to list the power pins in the design.

Function: You can choose the view mode as occurrences or instances from the Browse Properties dialog.

Shortcuts: Keyboard: ALT, E, B, W

Find command

Available from: Edit menu

Use this command to locate an object or string of text in a design.

The Find command supports wildcard searches. Use an asterisk (*) to match any string of characters, and a question mark (?) to match any single character.

In the schematic page editor, part editor, and project manager, the Find command will find all instances of the specified text search string. In the session log, the Find command will find the next occurrence of the specified text search string from the current position.

In the design variant schematic page, the Find command will find parts that are not present or parts with different property values attached to it.

Function:

This command can be used to search at different levels of a design folder hierarchy in the Project manager.

The search command can be executed at any of the following levels or selections of the design folder hierarchy:

- Design Level
- Folder level - For any number of selected folders within the design
- Page Level - For any number of selected pages within the design. This includes pages selected from different folders.

Note: The command also allows multi-level selection. This means you can simultaneously select folder and pages.

The search command can also be executed on an open schematic page.

Shortcuts:

Keyboard: ALT, E, F or CTRL+F

Rename Part Property command

Available from:

Edit menu

Function: Use this command to rename a part property for every placed part that includes the property for an entire design.

Note: This command is available only when you have selected the design (.DSN) or the schematic page(s) in the Project Manager window.

Shortcuts: Keyboard: ALT, E, Y

Delete Part Property command

Available from: Edit menu

Function: Use this command to delete a part property from every placed part in a design.

Note: This command is available only when you have selected the design (.DSN) or the schematic page(s) in the Project Manager window.

Shortcuts: Keyboard: ALT, E, D

Replace command

Available from: Edit menu

Function: Use this command to find and replace a particular string in a text editor window. When you choose Replace from the Edit menu, the Replace dialog box appears.

Shortcuts: Keyboard: ALT, E, E

Go To command

Available from: Edit menu

Use this command to center the view on a specific location, grid references, or bookmark. By clicking the Go To command, the Go To Line dialog box dialog box appears.

Function: **Note:** The Go To command is always available on the right mouse button context-sensitive menus in the part editor and schematic page editor. The Go To command, with the Relative option selected, is particularly useful for precise placement and spacing.

Shortcuts: Keyboard: ALT, E, G or CTRL+G

Clear Session Log command

Available from: Edit menu

Use this command to center the view on a specific location, grid references, or bookmark. By clicking the Go To command, the Go To Line dialog box dialog box appears.

Function: **Note:** The Go To command is always available on the right mouse button context-sensitive menus in the part editor and schematic page editor. The Go To command, with the Relative option selected, is particularly useful for precise placement and spacing.

Shortcuts: Keyboard: ALT, E, G or CTRL+G

View

"Toolbar command" on page 741

Toolbar command

Available from: View menu

Function: Use this command to show or hide the toolbars. This setting is stored in your .INI file and thus affects the visibility of the toolbar in subsequent sessions. You can move the toolbars anywhere on the screen by pressing the left mouse button over the toolbar, and then moving the mouse to the toolbar's new location. If the toolbar is moved to any edge of the window, the toolbar snaps into place. Otherwise, it floats on the screen wherever it is released.

If the toolbar is floating, you can hide it by choosing Toolbar from the View menu.

Shortcuts: Keyboard: ALT, V, T

Capture Toolbar command

Available from: View - Toolbar menu

Function: Use this command to show or hide the Capture toolbar. This setting is stored in your .INI file and thus affects the visibility of the toolbar in subsequent sessions. You can move the toolbar anywhere on the screen by pressing the left mouse button over the toolbar, and then moving the mouse to the toolbar's new location. If the toolbar is moved to any edge of the window, the toolbar snaps into place. Otherwise, it floats on the screen wherever it is released.

If the toolbar is floating, you can hide it by choosing Toolbar from the View menu.

For details on the toolbar buttons on this toolbar see Capture Toolbar in the OrCAD Capture Quick Reference Guide.

Draw Toolbar command

Available from: View - Toolbar menu

Function: Use this command to show or hide the Draw toolbar. This setting is stored in your .INI file and thus affects the visibility of the toolbar in subsequent sessions. You can move the toolbar anywhere on the screen by pressing the left mouse button over the toolbar, and then moving the mouse to the toolbar's new location. If the toolbar is moved to any edge of the window, the toolbar snaps into place. Otherwise, it floats on the screen wherever it is released.

If the toolbar is floating, you can hide it by choosing Toolbar from the View menu.

For details on the toolbar buttons on this toolbar see Draw Toolbar in the OrCAD Capture Quick Reference Guide.

PSpice Toolbar command

Available from: View - Toolbar menu

Function: Use this command to show or hide the PSpice toolbar. This setting is stored in your .INI file and thus affects the visibility of the toolbar in subsequent sessions. You can move the toolbar anywhere on the screen by pressing the left mouse button over the toolbar, and then moving the mouse to the toolbar's new location. If the toolbar is moved to any edge of the window, the toolbar snaps into place. Otherwise, it floats on the screen wherever it is released.

If the toolbar is floating, you can hide it by choosing Toolbar from the View menu.

For details on the toolbar buttons on this toolbar see PSpice Toolbar in the OrCAD Capture Quick Reference Guide.

FPGA Toolbar command

Available from: View - Toolbar menu

Function: Use this command to show or hide the FPGA toolbar. This setting is stored in your .INI file and thus affects the visibility of the toolbar in subsequent sessions. You can move the toolbar anywhere on the screen by pressing the left mouse button over the toolbar, and then moving the mouse to the toolbar's new location. If the toolbar is moved to any edge of the window, the toolbar snaps into place. Otherwise, it floats on the screen wherever it is released.

If the toolbar is floating, you can hide it by choosing Toolbar from the View menu.

For details on the toolbar buttons on this toolbar see FPGA Toolbar in the OrCAD Capture Quick Reference Guide.

CIS Explorer Toolbar command

Available from: View - Toolbar menu

Function: Use this command to show or hide the CIS Explorer toolbar. This setting is stored in your .INI file and thus affects the visibility of the toolbar in subsequent sessions. You can move the toolbar anywhere on the screen by pressing the left mouse button over the toolbar, and then moving the mouse to the toolbar's new location. If the toolbar is moved to any edge of the window, the toolbar snaps into place. Otherwise, it floats on the screen wherever it is released.

If the toolbar is floating, you can hide it by choosing Toolbar from the View menu.

For details on the toolbar buttons on this toolbar see CIS Explorer Toolbar in the OrCAD Capture CIS Quick Reference Guide.

Part Manager Toolbar command

Available from: View - Toolbar menu

Function: Use this command to show or hide the Part Manager toolbar. This setting is stored in your .INI file and thus affects the visibility of the toolbar in subsequent sessions. You can move the toolbar anywhere on the screen by pressing the left mouse button over the toolbar, and then moving the mouse to the toolbar's new location. If the toolbar is moved to any edge of the window, the toolbar snaps into place. Otherwise, it floats on the screen wherever it is released.

If the toolbar is floating, you can hide it by choosing Toolbar from the View menu.

For details on the toolbar buttons on this toolbar see Part Manager Toolbar in the OrCAD Capture Quick Reference Guide.

Search Toolbar command

Available from: View - Toolbar menu

Function: Use this command to show or hide the Search toolbar. This setting is stored in your .INI file and thus affects the visibility of the toolbar in subsequent sessions. You can move the toolbar anywhere on the screen by pressing the left mouse button over the toolbar, and then moving the mouse to the toolbar's new location. If the toolbar is moved to any edge of the window, the toolbar snaps into place. Otherwise, it floats on the screen wherever it is released.

If the toolbar is floating, you can hide it by choosing Toolbar from the View menu.

For details on the toolbar buttons on this toolbar see Search Toolbar in the OrCAD Capture Quick Reference Guide.

Footprint Viewer Toolbar command

Function:

Use this command to show or hide the Footprint Viewer toolbar. This setting is stored in your .INI file and thus affects the visibility of the toolbar in subsequent sessions. You can move the toolbar anywhere on the screen by pressing the left mouse button over the toolbar, and then moving the mouse to the toolbar's new location. If the toolbar is moved to any edge of the window, the toolbar snaps into place. Otherwise, it floats on the screen wherever it is released.

If the toolbar is floating, you can hide it by choosing Toolbar from the View menu.

For details on the toolbar buttons on this toolbar see Footprint Viewer Toolbar in the OrCAD Capture Quick Reference Guide.

Command Window command

Available from:

View - Toolbar menu

Function:

Use this command to open the TCL Command window in the OrCAD Capture workspace.

For details see the Command window help in the Capture User Guide.

Tools menu

"Annotate command" on page 746

"Associate PSpice Model command" on page 747

"Back Annotate command" on page 747

"Board simulation command" on page 748

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"Split Part command" on page 758

"Synch NetGroup command" on page 759

"Customize command" on page 759

Annotate command

Available from: Tools menu

Function: Use this command to update part references in the active design. You specify the scope and parameters of the update in the Annotate dialog box.

Annotate will update references for primitive hierarchical blocks. For example, you could specify the reference to be "Halfadd?" when you place a hierarchical block. Then, when you run Annotate, the hierarchical block's reference is updated along with other parts.

Shortcuts: Toolbar:

Keyboard: ALT, T, O

Associate PSpice Model command

Available from: Tools menu

Function: Use this command to associate a PSpice model with an existing Capture symbol.

Shortcuts: Keyboard: ALT, T, M

Back Annotate command

Available from: Tools menu

Function: Use this command to swap parts in a package, part references, and pins in the active design based on the contents of a swap file created by you or your PC board layout software. Capture swap files use a .SWP file extension. The purpose of back annotation is to ensure that the physical information in the board layout is consistent with the logical information in the schematic design.

There are two back annotation options, one for PCB Editor and one for Layout.

Note: Swap files are not true transaction swap files. If your a swap file contains the following lines:

```
SWAP UI U2
SWAP U2 U3
SWAP U3 U4
```

the original U1 is changed to U2. It does not change to U3 or U4, as it would in a true transaction system.

Shortcuts: Toolbar:

Keyboard: ALT, T, A

Board simulation command

Available from: Tools menu

Function: Initiates the board simulation process. This process provides a method for you to simulate your PCB designs (which may include FPGA designs, as components). You can use Verilog or VHDL to simulation your PCB designs by choosing the appropriate option in the Board Simulation tab of the Preferences dialog box.

Update Properties command

Available from: Tools menu

Function: Use this command to update properties based on an update file. This command constructs a combined property string for a part or net. Then, if that string matches a string in the update file, it replaces the specified properties of the combined property string with the update string properties. Capture update files use a .UPD file extension.

If you are updating net properties, Capture will update all of the nets in the schematic folder even if only one schematic page is selected. Capture updates all of the nets in the schematic folder because a single net can appear on more than one schematic page within the schematic folder. Capture only updates the selected schematic folders and schematic pages when updating part properties.

Tip

Capture report files are text files, and can be opened in any text editor. You may want to use the tab alignment capability of your word processor to line reports up correctly. Spreadsheets will automatically align the columns of Capture-generated report files.

Note: When back annotating from PCB Editor, an update value of "/IGNORE/" is interpreted as a property that is not to be updated. When "/IGNORE/" is found, the property in the schematic unchanged from it's previous value. For example, in the following line, the "TOL" property will not be updated for the part with a reference of "U1".

"{Part Reference}" "TOL"

"R1" "10%"

"U1" "/IGNORE/"

You can update properties of parts in libraries as well as update properties of parts in designs.

Shortcuts: Keyboard: ALT, T, U

Design Rules Check command

Available from: Tools menu

Function: Use this command to check a design for violations of design rules. Capture places DRC error markers on schematic pages as needed. You can search for the markers by using the Browse DRC Markers command on the Edit menu.

Note: Generally, you should run Design Rules Check to verify your design before you generate a netlist. This allows for more efficient netlist creation, and you can concentrate on netlist-specific problems if they should occur during the Create Netlist process. Design Rules Check warns you if certain conditions exist in your design. The severity of the specific problem may prevent completion of the design. Other conditions are subject to your judgment, and may be of no consequence. Once you are satisfied with the results of design tests like Design Rules Check, then proceed with the creation of a netlist.

Note: Design Rules Check uses the decision matrix located in the ERC Matrix tab in the Design Rules Check dialog box. It also uses a set of pre-determined rules, which are part of the executable code.

Note: Use Design Rules Check as a guide to verify the integrity of your design. It is only a guide. It is possible to generate a valid netlist even if Design Rules Check reports errors.

Tip

If you run a Design Rules Check on a single schematic page, Capture checks the entire schematic folder the schematic page is in. This ensures that all nets on the schematic page are valid.

If you select the Check hierarchical port connections option, Capture also checks the attached schematic folders.

Tip

Capture report files are text files, and can be opened in any text editor. You may want to use the tab alignment capability of your word processor to line reports up correctly. Spreadsheets will automatically align the columns of Capture-generated report files.

Shortcuts:

Toolbar:

Keyboard ALT, T, D

Create Netlist command

Available from:

Tools menu

Function:

Use this command to create a netlist from the selected design. This command displays the Create Netlist dialog box, a tabbed dialog box that you use to choose a netlist format.

If you have translated a design with multiple schematic folders, use Annotate (and check for duplicate references) before you create a netlist.

Note: Note that screws, washer, and other hardware appear in a bill of materials, but not in a netlist. Netlists include only objects with pins.

Important

Generally, you should run Design Rules Check to verify your design before you generate a netlist. This allows for more efficient netlist creation, and you can concentrate on netlist-specific problems if they should occur during the Create Netlist process. Design Rules Check warns you if certain conditions exist in your design. The severity of the specific problem may prevent completion of the design. Other conditions are subject to your judgment, and may be of no consequence. Once you are satisfied with the results of design tests like Design Rules Check, then proceed with the creation of a netlist.

Note: The value, if any, you create for the PCB footprint depends on the particular netlist format you want to produce. Different applications require netlists with different types of PCB footprints. If you do not specify this property, the PCB footprint will be set to the part value.

Tip

Capture report files are text files, and can be opened in any text editor. You may want to use the tab alignment capability of your word processor to line reports up correctly. Spreadsheets will automatically align the columns of Capture-generated report files.

Shortcuts:

Toolbar:

Keyboard: ALT, T, N

Create Differential Pair command

Available from:

Tools menu

Function: Use this command to create a differential pair between two flat nets in your design. This command displays the Create Differential Pair dialog box where you select the nets to be associated with a differential pair. You can also use the Create Differential Pair dialog box to modify or delete a differential pair.

Note: You can access this command only if you select a design file (.DSN) or a schematic page (.sch) in the project manager.

Shortcuts: Keyboard: ALT, T, F

Cross Reference command

Available from: Tools menu

Function: Use this command to create a cross-reference listing telling you where each part is located, and the library it comes from.

Tip

Capture report files are text files, and can be opened in any text editor. You may want to use the tab alignment capability of your word processor to line reports up correctly. Spreadsheets will automatically align the columns of Capture-generated report files.

Shortcuts: Toolbar:

Keyboard: ALT, T, C

Intersheet References command

Available from: Tools menu

Function: Use this command to create the interesheet references for the signals on a design. In addition, you can also generate a report for all the signals on the design.

Shortcuts: Keyboard: ALT, T, T

Bill of Materials command

Available from: Tools menu

Function: Use this command to create a summary list of all parts used in the design. You can also use an include file to add information to the bill of materials. By default, Capture include files use a .INC file extension.

Important

Reference designators should not exceed 24 characters. When Bill of Materials encounters a reference designator that is longer than 24 characters, an error occurs and the bill of materials isn't generated.

Important

Capture report files are text files, and can be opened in any text editor. You may want to use the tab alignment capability of your word processor to line reports up correctly. Spreadsheets will automatically align the columns of Capture-generated report files.

Toolbar:

Shortcuts:

Keyboard: ALT, T, B

Export Properties command

Available from: Tools menu

Function: Use this command to write the properties of the selected documents to an ASCII text file. Properties are delimited by tabs so the file is suitable for manipulation by spreadsheet or database software. You can export properties from a design or library.

For more information on property files see Exporting part and pin properties.

Important

If you add, delete, or reorder lines in a project's property file, the file cannot be imported.

If you move a PART line in a design property file created in a library property file, be sure to move all the PIN lines associated with it and keep them in the same order. Otherwise, importing the file may fail or cause unwanted changes to your project or library.

In every case, it is much safer to refrain from adding, deleting, or reordering the lines in a property file.

Note: It is a good idea to update part references before you export properties.

Because various popular spreadsheet and database applications behave differently, Capture can import properties with or without enclosing quotation marks around each field in the property file. The fields must be tab-delimited, though—all other characters, including commas and leading and trailing spaces, are treated as part of a field's text. Be sure your spreadsheet or database program can save in this format.

Shortcuts: Keyboard: ALT, T, E

Export Placement command

Available from: Project manager pop-up menu

Function: Use this command to generate a placement report for the selected levels of the current design hierarchy.

You can generate the report at any level of the hierarchy, page, folder or design. You can also generate the report at different level by multi-selecting the level in the Project manager.

Save as HTML command

Available from: Find window pop-up menu

Function: Use this command to generate a report, in HTML format, for the results of a Find command.

Save as CSV command

Available from: Find window pop-up menu

Function: Use this command to generate a report, in CSV format, for the results of a Find command.

Import Properties command

Available from: Tools menu

Function:

Use this command to import the contents of a tab-delimited property file. The imported properties may add to or supersede existing properties. The property file must be in the format used by Capture when you choose the Export Properties command from the Tools menu. You can import properties to a design or library.

For more information on property files see Exporting part and pin properties.

The Import Properties command opens a standard Windows dialog box for opening files.

Important

If you add, delete, or reorder lines in a project's property file, the file cannot be imported.

If you move a PART line in a design property file created in a library property file, be sure to move all the PIN lines associated with it and keep them in the same order; otherwise, importing the file may fail or cause unwanted changes to your project or library.

In every case, it is much safer to refrain from adding, deleting, or reordering the lines in a property file.

Note: It is a good idea to update part references before you export properties.

Because various popular spreadsheet and database applications behave differently, Capture can import properties with or without enclosing quotation marks around each field in the property file. The fields must be tab-delimited, though—all other characters, including commas and leading and trailing spaces, are treated as part of a field's text. Be sure your spreadsheet or database program can save in this format.

Note: If Capture finds errors in the property file, the project or library remains unchanged. There is no risk that some parts will be changed and others not.

Shortcuts: Keyboard: ALT, T, I

Generate Part command

Available from:

Tools menu

Function:

Use this command to create a library and an associated part that represents your design. You can use a schematic, a library containing schematics, or a netlist to generate a symbol for the project.

You can use the symbol you generate with the Generate Part command to represent the actual component (such as an FPGA or CPLD) in schematic designs or other projects. When you use the Generate Part command, Capture creates a library file (.OLB) and part based on the pins defined in the report file or schematic and references it in the Outputs folder of the project manager. If the library already exists, the new part is appended to the existing library. If the part already exists in the library, the new part replaces it.

Note: If the schematic from which you generate a part has one or more Param symbols, the entries in that symbol are placed on the resulting part as user properties. You can then overwrite default values for those properties on a specific instance or occurrence.

The Generate Part dialog box offers a number of netlist and source file types that are used to generate a part or symbol. The Capture Schematic/Design source file type uses a library or a single schematic to create the new .OLB containing the new part and a copy of the schematic for easy portability and design reuse. You can use this source type to create a design reuse module.

Capture reads a variety of PLD vendor pin reports to create library parts for the Capture schematic system. Most PLD vendor pin reports describe the pin number, signal name, and direction (or mode) of a package pin programmed by the place-and-route process. Pins are sorted alphabetically by name, with input type pins located on the left-hand side, and output or bidirectional pins on the right-hand side.

Generate part can create new parts or update the pin numbers of an existing library part with the Update pins on existing part in library option, which allows for engineering change orders (ECOs) from a programmable logic project to update the part symbol of the system schematic.

Note: To create a pin on a symbol using the Generate Part utility, the pin must have a pin to port mapping in the pin file.

Shortcuts: Keyboard: ALT, T, G

Export FPGA command

Available from: Tools menu

Function: Use this command export the selected (or all) part to export as an FPGA part.

Note: You can select a vendor family and if you want to generate if a VHDL or Verilog wrapper file.

Shortcuts: Keyboard: ALT, T, X

Split Part command

Available from: Tools menu

Function: Use this command to divide a part into multiple sections.

Note: You need to select a single-sectioned part from a library. You can split a multi-sectioned part only when it has been split already using this command.

Shortcuts: Keyboard: ALT, T, L

Assign Power Pins command

Available from: Tools menu

Function: Use this command to specify the invisible powers on the selected object (design, schematic folder, schematic page or schematic part) as NC Pins.

Shortcuts: Keyboard: ALT, T, W

Synch NetGroup command

Available from: Tools menu

Function: If a hierachical block pin in connected to a NetGroup and the width (number of contained signals) of the NetGroup is modified, use this command to synchronize the number of signals in the hierarchical pin and the NetGroup.

Customize command

Available from: Tools menu

Function: Use this command to customize the OrCAD Capture menus.

You can:

- choose the menus to show and hide.
- add or remove buttons (commands) from the menus.
- create a custom menu and add buttoms (commands) to the menu.

PICFlow menu

Note: This menu is visible and active only when the project in the active project manager window is defined as a programmable logic project.

"Compile Vendor Libraries command" on page 760

"Synthesize command" on page 760

"P&R command" on page 761

"Simulate command" on page 761

Compile Vendor Libraries command

Available from: Tools menu

Function: Use this command to initiate compilation of the vendor simulation models required to simulate your design.

Shortcuts: Toolbar

Synthesize command

Available from: PICFlow menu

Function: Use this command to initiate setup for synthesis of your FPGA design.

When you select this command, Capture starts Synplify. In the Synplify interface, you can perform synthesis on your design.

Shortcuts: Toolbar

Keyboard: ALT, P, Y

P&R command

Available from: PICFlow menu

Function: Use this command to start the place-and-route tool specific to the target vendor of your programmable logic design. Capture invokes the place-and-route tool, from which you can initiate the place-and-route procedure. You can also run the place-and-route tool in batch mode.

Shortcuts: Toolbar

Keyboard: Alt, P, B

Simulate command

Available from: PICFlow menu

Function: Use this command to initiate setup for simulation of your FPGA design.

When you execute this command, Capture displays the Select Simulation Configuration dialog box.

Shortcuts: Toolbar:

Keyboard: ALT, P, S

PSpice

"Bias Points command" on page 762

"New Simulation Profile command" on page 762

"Edit Simulation Profile command" on page 763

"Run command" on page 763

"View Simulation Results command" on page 764

"View Output File command" on page 764

"Make Active command" on page 764

"Simulate Selected Profile(s) command" on page 765

"Create Netlist command" on page 765

"View Netlist command" on page 766

"Marker List command" on page 766

"Advanced Analysis menu" on page 767

Bias Points command

Available from: PSpice menu, Bias Points submenu

From a schematic page, point to Markers on the PSpice menu.

Function: Use the commands in the Bias Points submenu to enable and disable bias point display, toggle selected bias points and to set preferences for displaying and printing bias points.

Shortcuts: Keyboard: ALT, S, B, E

New Simulation Profile command

Available from: PSpice menu

Function: You must create a simulation profile (or edit an existing one) before you can set up a PSpice simulation. Use this command to create a new simulation profile. A simulation profile (*.SIM) saves your simulation settings for an analysis type so you can reuse them easily.

After creating a new profile, you can edit the settings with the Edit Simulation Settings command.

Shortcuts:

Toolbar

Keyboard: ALT, S, N

Edit Simulation Profile command

Available from:

PSpice menu

Function:

Use this command to edit an existing PSpice simulation profile. Simulation profiles can be edited in Capture and PSpice.

Shortcuts:

Toolbar

Keyboard: ALT, S, E

Run command

Available from:

PSpice menu

Function:

After setting all the simulation parameters you need, choose Run to perform the simulation. This command automatically performs the following steps:

- checks design rules for your design.
- creates a simulation netlist for PSpice.
- opens PSpice using the netlist created from your design.

PSpice creates an output file (.OUT) as the simulation progresses. It contains bias point information, model parameter values, error messages, and so on. If the simulation fails, you can view the output file to see the error messages.

If the simulation completes successfully, PSpice produces a data file (.DAT). This is the file PSpice uses to display the simulation results.

To see marker simulation results, the schematic must be open.

Note: You can run PSpice simulations from the Capture environment by pressing the F11 function key.

Shortcuts:

Toolbar

Keyboard: ALT, S, R

View Simulation Results command

Available from: PSpice menu

Function: Use this command to view the most recent simulation results, for the active simulation profile. To see marker simulation results, the schematic must be open.

Note: You can view the simulation results from the currently active profile by pressing the F12 function key.

Shortcuts:

Toolbar

Keyboard: ALT, S, V

View Output File command

Available from: PSpice menu

Function: Use this command to view the most recent output file for the current design.

Shortcuts: Keyboard: ALT, S, W

Make Active command

Available from: PSpice menu

Function: Use this command, with the project manager active, to make the selected simulation profile the active profile. In the project manager, the simulation profile folder is in the PSpice Resources folder.

Simulate Selected Profile(s) command

Available from: PSpice menu

Use this command, with the project manager active, to simulate selected profiles.

Simulate Selected Profile(s) automatically performs the following steps:

- Checks design rules for your design.
- Creates a simulation netlist for PSpice.
- Opens PSpice using the netlist created from your design.

Function: You can select one profile or multiple profiles to be simulated or viewed. If you select only one profile for simulation, it is handled as though you chose the Run command. If you select one file for viewing, it is handled as though you chose the View Simulation Results command.

If you select multiple profiles, simulations for all selected profiles are performed using the simulation queue. You must then open the .DAT files to view the results.

See Simulating and viewing the results of multiple profiles for procedures to simulate and view multiple profiles.

Shortcuts: Keyboard: ALT, P, A

Create Netlist command

Available from: PSpice menu

Use this command to create a simulation netlist for the current design. The netlist is generated for all levels of hierarchy, starting from the top, regardless of whether you are pushed into any level of the hierarchy.

Function: In OrCAD Capture, the TEMPLATE property specifies the primitive parts' contributions to the netlist. In the process of creating the netlist, buses, connectors, and so on, are resolved. Only parts with a TEMPLATE property are included in the simulation.

During the netlist process, Capture creates several files with different extensions: The .NET file contains the netlist; the .CIR file contains simulation commands; and the .ALS file contains alias information.

Shortcuts: Keyboard: ALT, S, C

View Netlist command

Available from: PSpice menu

Function: Use this command to view the most recent simulation netlist for a selected or the current design.

Shortcuts: Keyboard: ALT, S, I

Marker List command

Available from: PSpice menu

From the Project Manager, choose Marker List from the PSpice menu.

Function: Use this command to display or hide markers in the design. The Markers dialog box displays markers that exist in the profile. An empty check box beside a marker indicates that the marker is hidden. If a marker is hidden, it will not appear in Capture but it will still exist in the profile.

Shortcuts: Keyboard: ALT, S, L

Advanced Analysis menu

"Sensitivity command" on page 767

"Optimizer command" on page 767

"Monte Carlo command" on page 768

"Smoke command" on page 768

"Export Parameters to Optimizer command" on page 769

"Import Optimizable Parameters command" on page 770

Sensitivity command

Available from: PSpice menu, Advanced Analysis submenu

If you have installed PSpice Advanced Analysis, use this command to run Sensitivity Analysis.

Function: Sensitivity analysis identifies which components have parameters critical to the measurement goals of your circuit design. See the PSpice Advanced Analysis User's Guide, for more information on the Sensitivity Analysis tool.

Shortcuts: Keyboard: ALT, S, D, S

Optimizer command

Available from: PSpice menu, Advanced Analysis submenu

Function:

If you have installed PSpice Advanced Analysis or PSpice Optimizer, use this command to optimize your design.

Optimizer is a design tool for optimizing analog circuits and their behavior. It helps you modify and optimize analog designs to meet your performance goals. For more information on the Optimizer tool, see:

- "PSpice Advanced Analysis User's Guide, if you have installed PSpice Advanced Analysis
- "PSpice Optimizer User's Guide (Capture version), if you have installed PSpice Advanced Analysis

Shortcuts: Keyboard: ALT, S, D, O

Monte Carlo command

Available from: PSpice menu, Advanced Analysis submenu

Function:

If you have installed PSpice Advanced Analysis, use this command to run Monte Carlo analysis.

Monte Carlo analysis predicts the behavior of a circuit statistically when part values are varied within their tolerance range. Monte Carlo analysis also calculates yield, which can be used for mass manufacturing predictions. See the PSpice Advanced Analysis User's Guide, for more information on the Monte Carlo analysis tool.

Shortcuts: Keyboard: ALT, S, D, M

Smoke command

Available from: PSpice menu, Advanced Analysis submenu

If you have installed PSpice Advanced Analysis, use this command to run Smoke analysis.

Function: Smoke analysis determines whether components in your design are operating within their safe operating limits. See the PSpice Advanced Analysis User's Guide, for more information on the Smoke analysis tool.

Shortcuts: Keyboard: ALT, S, D, K

Export Parameters to Optimizer command

Available from: PSpice menu, Advanced Analysis submenu

If you have installed PSpice Advanced Analysis or PSpice Optimizer, use this command to export device-level parameters to Optimizer.

Select a component on the schematic and use this command to export its device-level parameters to the Optimizer tool. The component and its parameters are added in the Parameters table.

Function: **Note:** This feature of exporting device-level parameters to Optimizer is available only if the selected component is based on PSpice-provided templates.

For more information on the Optimizer tool, see:

- PSpice Advanced Analysis User's Guide, if you have installed PSpice Advanced Analysis
- PSpice Optimizer User's Guide (Capture version), if you have installed PSpice Advanced Analysis

Shortcuts: Keyboard: ALT, S, D, E

Import Optimizable Parameters command

Available from: PSpice menu, Advanced Analysis submenu

If you have installed PSpice Advanced Analysis or PSpice Optimizer, use this command to import optimizable parameters from the component's model library as instance properties.

Select a component on the schematic and use this command to import optimizable parameters from the component's model library. The parameter names and their default values are displayed on the component instance in the schematic editor.

Function: This feature of importing optimizable parameters is available only if the selected component is based on PSpice-provided templates.

For more information on the Optimizer tool, see:

- PSpice Advanced Analysis User's Guide, if you have installed PSpice Advanced Analysis
- PSpice Optimizer User's Guide (Capture version), if you have installed PSpice Advanced Analysis

Shortcuts: Keyboard: ALT, S, D, I

Accessories menu

"Accessories commands" on page 771

"Rotate Aliases command" on page 771

"Library Verification/Correction command" on page 771

"Push Occ. Prop into Instance command" on page 772

Layout to PCB Editor command on page 773

"Export Hierarchy command" on page 774

"Export Hierarchy with Parts command" on page 774

"Mentor Netlist command" on page 774

"Mentor Netlist (to UNIX) command" on page 774

"Mentor Back Annotation command" on page 775

Accessories commands

Available from: Accessories menu

Function: You can use extensions to the OrCAD-supplied functionality of Capture if you purchase software developed by associates of OrCAD. These associates create .DLL files that address specific Capture functionality, such as customized netlisting. The associates configure their .DLL files so that they are listed as menu choices in the Accessories menu, which is available in either the project manager window or the schematic page editor window.

Rotate Aliases command

Available from: Accessories menu, aliasrot sub menu

Function: Use this command to rotate 270 degree aliases, ports, and off page connector names to 90 degrees.

Library Verification/Correction command

Available from: Accessories menu, LibCorrectionUtil sub menu

Function:

Use this command to:

- Verify and correct all the parts with missing pin numbers or duplicate pin names in a library.
- Change all lowercase pin numbers and pin names to uppercase in a library.
- Make all Power pins visible in a library.

This command launches the Library Correction Utility dialog box where you specify the name of the library that you want to correct and select the correction to be done.

Push Occ. Prop into Instance command

Available from:

Accessories menu, Transfer Occ. Prop. to Instance sub menu

Function:

Suppose that you copied a circuit or part of a circuit from design A and pasted it in design B. You might see occurrence and instance level properties with different values on the pasted parts/nets in design B. For example, the reference designators of the occurrences and instances may be different. To avoid confusion in the future you have to ensure that each part has only one reference designator by replacing the instance value of the part reference property with the occurrence value of the part reference property for each part.

Use this command to automatically:

- transfer occurrence property values of the part reference and PCB footprint properties as instance level property values.
  - remove all occurrence properties from the design, and set Capture to update instance properties when the design is back annotated.
- transfer occurrence property values of flat nets to schematic nets.

This command opens the Push Occ. properties to instance dialog box.

Cadence Tcl/Tk Utilities command

Available from: Accessories menu, Utilities sub-menu of the Cadence Tcl/Tk Utilities menu item

Function:

Use this command to launch the Tcl/Tk applications dashboard.

From the dashboard, you have access the the Cadence Tcl/Tk applications.

You can:

- launch a Tcl/Tk application.
- view the source code of a Tcl/Tk application.
- view the Cadence Tcl/Tk documentation.

Start Page command

Available from: Accessories menu, Start Page sub-menu of the Cadence Tcl/Tk Utilities menu item

Function: Use this command to go to the OrCAD Capture Start Page.

Layout to PCB Editor command

Available from: Accessories menu, Layout to PCB Editor translator sub menu

Function:

Use this command to translate Layout database files (.max) to PCB Editor board files (.brd). You can also choose to synchronize the design (.dsn) file with the generated board file (.brd).

This command opens the Layout to PCB Editor dialog box.

Export Hierarchy command

Available from: Accessories menu, Hierarchy Report submenu

Function: Use this command to generate a report that depicts the hierarchical structure of a design. This command generates a .txt file that lists all the schematics used in the design and stores the file under the Outputs folder in project manager.

Export Hierarchy with Parts command

Available from: Accessories menu, Hierarchy Report submenu

Function: Use this command to generate a report that depicts the complete hierarchical structure of a design listing all the parts that are included in the design. This command generates a .txt file that lists all the schematics along with all the parts used in the design and stores the file under the Outputs folder in project manager.

Mentor Netlist command

Available from: Accessories menu, Mentor submenu

Function: Use this command to create a netlist in Mentor Graphics format.

Mentor Netlist (to UNIX) command

Available from: Accessories menu, Mentor submenu

Function: Use this command to create a netlist in Mentor Graphics format for UNIX.

Mentor Back Annotation command

Available from: Accessories menu, Mentor submenu

Function: Use this command to back annotate Mentor board information to Capture design

Options menu

"Preferences command" on page 775

"Design Template command" on page 776

"Design Properties command" on page 776

Preferences command

Available from: Options menu

Function: Use this command to set your environment preferences for the current project (and all future projects) on your system. The options you specify affect the behavior of the software, and are saved in the .INI file.

Shortcuts: Keyboard: ALT, O, P

Design Template command

Available from: Options menu

Function: Use this command to specify default settings for new projects, designs, and schematic pages. The values specified in this dialog box do not affect existing projects or designs.

Note: To change the properties of an active design, use the Design Properties command. To change the properties of an active schematic page, use the Schematic Page Properties command. You cannot change the default title block of an active schematic page.

Shortcuts: Keyboard: ALT, O, D

Design Properties command

Available from: Options menu

Function: Use this command in the project manager to globally set design related options throughout a design.

Note: To change the properties for objects in new designs, use the Design Template command.

Shortcuts: Keyboard: ALT, O, R

Window menu

"New Window command" on page 777

"Cascade command" on page 777

"Tile Horizontally command" on page 777

"Tile Vertically command" on page 778

"Arrange Icons command" on page 778

"1,2.... command" on page 778

Close All Windows on page 779

New Window command

Available from: Window menu

Function: Use this command to create a new window, which is a copy of the currently active window. This new window is another "view" on the same data, and you can scroll the two windows to different positions.

Shortcuts: Keyboard: ALT, W, N

Cascade command

Available from: Window menu

Function: Use this command to "stack" all open Capture windows so that just their title bars are visible. The active window stays on top.

Shortcuts: Keyboard: ALT, W, C

Tile Horizontally command

Available from: Window menu

Function: Use this command to arrange open Capture windows, one above another, so that all are visible.

Shortcuts: Keyboard: ALT, W, H

Tile Vertically command

Available from: Window menu

Function: Use this command to arrange open Capture windows, one beside another, so that all are visible.

Shortcuts: Keyboard: ALT, W, V

Arrange Icons command

Available from: Window menu

Function: Use this command to arrange the icons for minimized windows across the bottom of the session frame.

Shortcuts: Keyboard: ALT, W, A

1,2.... command

Available from: Window menu

Function: Use the numbers listed at the bottom of the Window menu to view which windows are currently open, and to determine which window is active. (The active window is indicated by a check mark.) When you choose a window from this list, Capture restores that window if it was in icon form, pops it to the front of the Capture session, and makes it the active window.

Shortcuts: Keyboard: ALT, W, n (n = 1, 2, . . .)

Close All Windows

Available from: Window menu

Function: Use this command to close all open windows.

Help menu

"OrCAD Capture Help command" on page 779

"Known Problems and Solutions command" on page 780

"What's New command" on page 780

"Learning OrCAD Capture command" on page 780

"About OrCAD Capture command" on page 781

"Web Resources command" on page 781

"Documentation command" on page 783

Note: To use the context-sensitive menu commands, select one or more items, then press the right mouse button. The contents of the menu differ depending on the objects selected.

OrCAD Capture Help command

Available from: Help menu

Function: Use this command to display the Capture Help window.

Shortcuts: Toolbar:

Keyboard: ALT, H, H or F1

Known Problems and Solutions command

Available from: Help menu

Function: Use this command to display a document listing the known problems in this release of OrCAD Capture and tells you how to solve or work around these problems.

Shortcuts: Keyboard: ALT, H, K

What's New command

Available from: Help menu

Function: Use this command to display a document describing the new features and enhancements in this release.

Shortcuts: Keyboard: ALT, H, K

Learning OrCAD Capture command

Available from: Help menu

Function: Use this command to run the online, interactive tutorial.

Shortcuts: Keyboard: ALT, H, L

About OrCAD Capture command

Available from: Help menu

Function: Use this command to get the software version number, copyright information, registration number, and license information.

Shortcuts: Keyboard: ALT, H, A

Web Resources command

Available from: Project manager Help menu, or schematic page editor Help menu

Function: Use this command to link to Capture resources on the web

Shortcuts: Keyboard: ALT, H, W

Note: You can add other web resources to the displayed list by modifying your CAPTURE.INI file. Note, however, that the first resource in the list, appears as the last name in the menu. Therefore, if you want to add a web resource to the top of the list, include it in the CAPTURE.INI file as the last entry.

Source Link command

Available from: Help menu, Web Resources command

Function: Use this command to launch your web browser and visit the Cadence Customer Support web site.

Shortcuts: Keyboard: ALT, H, W, S

Education Services command

Available from: Help menu, Web Resources command

Function: Use this command to launch your web browser and visit the OrCAD web site.

Shortcuts: Keyboard: ALT, H, W, E

PCB Systems Home command

Available from: Help menu, Web Resources command

Function: Use this command to launch your web browser and visit the PCB Systems home page.

Shortcuts: Keyboard: ALT, H, W, P

OrCAD Community Site command

Available from: Help menu, Web Resources command

Function: Use this command to launch your web browser and visit the OrCAD Community web page. This page provides usable technical solutions for Windows™ based PCB design.

Shortcuts: Keyboard: ALT, H, W, O

Documentation command

Available from: In the project manager or schematic page editor, from the Help menu, choose Documentation.

Function: Use this command to launch the HTML page, which contains links to all the documentation types (manuals and online help), product tutorial, and multimedia demonstrations shipped with this product release.

Shortcuts: Keyboard: ALT, H, D

Project Manager Menu

"Change Project Type command" on page 783

"Open Containing Folder command" on page 784

Change Project Type command

Available from: In the project manager, from the Project manager menu, choose Change Project Type.

Function: Use this command to change the type of a project to any of the following project types:

- Analog or Mixed A/D
- PC Board Wizard
- Programmable Logic Wizard
- Schematic.

Open Containing Folder command

Available from: In the project manager, from the Project manager menu, choose Open Containing Folder.

Function: Use this command to open the file system folder containing the selected project..

Edit Object Properties command

Available from: In the project manager, from the right-click menu, choose Edit Object Properties.

Function: Use this command to edit the properties of project objects in the project manager.

The command is available for at the:

- design level
- folder level
- page level

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Schematic page editor and part editor command reference

This chapter covers:

- "File menu" on page 785
- "Edit menu" on page 796
- "View menu" on page 813
- "Place menu" on page 824
- "Macro menu" on page 844
- "PSpice/Markers menu" on page 846
- "Accessories menu" on page 851
- "Options menu" on page 851
- "Window menu" on page 855
- "Help menu" on page 857
- "Pop-up menu" on page 860

File menu

This section covers:

"New command" on page 786

"Open command" on page 789

"Close command" on page 791

"Save command" on page 792

"Export Selection command" on page 792

"Import Selection command" on page 792

"Print Preview command" on page 793

"Print command" on page 793

"Print Setup command" on page 794

"Print Area command" on page 794

"Import Design command" on page 795

"Export Design command" on page 795

"1,2,3,4 command" on page 795

"Exit command" on page 796

New command

Available from: File menu

Function:

Use this command to create a new project, design, library, or VHDL file. Choose a command from the menu that appears:

- Project
- Design
- Library
- VHDL File
- Verilog File

The number of open windows you can have is only limited by your available system resources. You can use the Window menu to switch among open windows (see 1,2.... command).

You can open an existing project, design, library, or VHDL file using the Open command on the File menu.

If you click the Create document toolbar button from a schematic page editor, the New Page in Schematic dialog box appears.

If you click the Create document toolbar button from the part editor, the New Part Properties dialog box appears.

Shortcuts:

Toolbar:

Keyboard: ALT, F, N

New Project command

Available from:

File menu, New command

Function:

Use this command to create a new project in Capture. Specify your project to be one of the following:

- PSpice design
- PCB design
- CPLD or FPGA
- Blank schematic project

Shortcuts:

Keyboard: ALT, F, N, P

New Design command

Available from:

File menu, New command

Function: Use this command to create one schematic folder with one schematic page, which Capture opens in the schematic page editor.

Shortcuts: Keyboard: ALT, F, N, D

New Library command

Available from: File menu, New command

Function: Use this command to create a new library (containing no parts or symbols) with a library cache folder.

Shortcuts: Keyboard: ALT, F, N, L

New VHDL File command

Available from: File menu, New command

Function: Use this command to create a new VHDL File, opened in Capture's text editor.

Shortcuts: Keyboard: ALT, F, N, V

New Verilog File command

Available from: File menu, New command

Function: Use this command to create a new Verilog File, opened in Capture's text editor.

Shortcuts: Keyboard: ALT, F, N, V

New Text File command

Available from: File menu, New command

Function: Use this command to create a new text file, opened in Capture's text editor.

Shortcuts: Keyboard: ALT, F, N, T

Open command

Available from: File menu

Function: Use this command to open an existing project, design, library, VHDL, or Verilog file in a new window. Choose a command from the menu that appears:

- Design
- Library
- Project
- VHDL File
- Verilog File

The number of open windows you can have is only limited by your available system resources. You can use the Window menu to switch among open windows (see 1,2.... command).

You can create a new project, design, library, VHDL, or Verilog file using the New command on the File menu.

Note: When you choose the Open button on the toolbar, a standard Windows Open dialog box appears, in which you can choose the type of file you want to open in the Files of type drop-down list. Among the listed choices are SDT Schematic (*.SCH) and SDT Library (*.LIB).

Shortcuts: Toolbar: s

Keyboard: ALT, F, O

Open Project command

Available from: File menu, Open command

Function: Use this command to open an existing project.

Shortcuts: Keyboard: ALT, F, O, P

Open Design command

Available from: File menu, Open command

Function: Use this command to open one schematic folder with one schematic page, which Capture opens in the schematic page editor.

Shortcuts: Keyboard: ALT, F, N, D

Open Library command

Available from: File menu, Open command

Function: Use this command to open a library (containing no parts or symbols) with a library cache folder.

Shortcuts: Keyboard: ALT, F, O, L

Open VHDL File command

Available from: File menu, Open command

Function: Use this command to open a VHDL File, opened in Capture's text editor.

Shortcuts: Keyboard: ALT, F, O, V

Open Verilog File command

Available from: File menu, Open command

Function: Use this command to open a Verilog File, opened in Capture's text editor.

Shortcuts: Keyboard: ALT, F, O, E

Open Text File command

Available from: File menu, Open command

Function: Use this command to open an existing text file in a text editor

Shortcuts: Keyboard: ALT, F, O, T

Close command

Available from: File menu

Function: Use this command to close the active window. If necessary, you are prompted to save your changes.

Shortcuts: Keyboard: ALT, F, C

If you open a part editor via the Part command on the Edit menu, modify the part, and then close it, Capture asks if you want to update the current part only, update all parts of this type in the design, discard your changes, or cancel the Close command.

Save command

Available from: File menu

Function: Use this command to save the active, modified projects, designs, libraries, and VHDL files. You can save a design, library, VHDL file, or session log under a different name using the Save As command on the File menu.

Note: When you save a project, Capture automatically creates a backup with a .DBK file extension. When you save a library, Capture automatically creates a backup with a.OBK file extension. If you save only a schematic page or part, no backup is generated.

Shortcuts: Toolbar:

Keyboard: ALT, F, S or CTRL+S

Export Selection command

Available from: File menu

Function: Use this command to export the selected objects on a schematic page to a design or library. You can later import them onto a schematic page using the Import Selection command on the File menu.

This is useful if you have portions of a schematic page that you want to use on different schematic pages.

Shortcuts: Keyboard: ALT, F, E

Import Selection command

Available from: File menu

Function: Use this command to import the contents of a file created with the Export Selection command on the File menu to the active schematic page.

Shortcuts: Keyboard: ALT, F, I

Print Preview command

Available from: File menu

Function: Use this command to see how a schematic page or part will look when printed.

After setting the options in the Print Preview dialog box, click OK to preview the printed document. You can use the buttons at the top of the window to view different pages and to zoom in and out.

Note: Be prepared to wait if you attempt to print multiple pages or parts. Depending on the number and size of the pages or parts you are previewing, Capture may require extra time to display the selection.

Shortcuts: Keyboard: ALT, F, V

Print command

Available from: File menu

Function: Use this command to print the active schematic page, the active part, or the selected items in the project manager.

Note: When you print multiple copies, the copies are grouped by page, not sorted by copy.

Shortcuts: Toolbar:

Keyboard: ALT, F, P or CTRL+P

Print Setup command

Available from: File menu

Function: Use this command to choose a printer, paper source, and orientation before printing. The Print Setup command displays the Print Setup dialog box, a standard windows dialog box for configuring your printer or plotter. For more information on setting up printers and plotters, refer to the documentation for your configured printer driver.

Tip

Many times, the options for your printer are not available in the standard setup dialog box. If you do not find the options you need, try the printer setup in the Windows Control Panel.

Shortcuts: Keyboard: ALT, F, R

Print Area command

Available from: File menu

Function: Use this command in the schematic page editor to select and set or clear a specific area to print on your schematic page. Choose a command from the menu that appears:

- Set
- Clear

Shortcuts: Keyboard: ALT, F, A

Clear command

Available from: File menu

Function: Use this command to clear a print area setting from the active schematic page. The print area setting also clears automatically when you close the schematic page.

Shortcuts: Keyboard: ALT, F, A, C

Import Design command

Available from: File menu

Function: Use this command to import EDIF, PDIF and PSpice designs. EDIF designs must be graphical EDIF designs, and not EDIF netlists. Not all imported PDIF parts may be edited in Capture. Such parts won't affect netlists.

Export Design command

Available from: File menu

Function: Use this command to export EDIF designs and DXF schematic pages. This command saves EDIF designs as graphical EDIF designs, and not EDIF netlists. DXF schematic pages are saved in AutoCAD's V12 file format.

1,2,3,4 command

Available from: File menu

Function: Use the numbers listed at the bottom of the File menu to open one of the last four projects or files. Choose the file you want to open.

Shortcuts: Keyboard: ALT, F, n (n = 1, 2, 3, or 4)

Exit command

Available from: File menu

Function: Use this command to exit the software. If necessary, you are prompted to save your changes.

You can also exit the software by choosing the Close command on the session frame Control menu (ALT, SPACEBAR, C).

Shortcuts: Keyboard:

ALT, F, X

ALT, SPACEBAR, C

ALT+F4

Edit menu

This section covers:

“Undo command” on page 797

“Redo command” on page 798

“Repeat command” on page 798

“Cut command” on page 800

“Copy command” on page 800

“Paste command” on page 801

“Delete command” on page 802

“Select All command” on page 803

"Properties command" on page 804

"Part command" on page 806

"Reset Location command" on page 807

"Mirror command" on page 808

"Rotate command" on page 810

"Find command" on page 810

"Global Replace command" on page 811

Undo command

Available from: Edit menu

Function: Use this command to reverse the effect of the last operation, if possible. In Capture, the name of this command changes, depending on what the last reversible operation was—for example, Undo Rotate or Undo Delete. You can undo and redo multiple commands to return your design to any particular state, as described in Undoing and repeating.

The Undo command applies to the following actions:

- Placing
- Deleting
- Moving
- Resizing
- Rotating
- Mirroring

Shortcuts: Toolbar:

Keyboard: ALT, E, U or CTRL+Z

Redo command

Available from: Edit menu

Function: Use this command to reverse the effect of the most recent Undo command. In Capture, the name of the command changes, depending on what the undone operation was, for example: Redo Rotate or Redo Delete. You can undo and redo multiple commands to return your design to any particular state, as described in Undoing and repeating.

The Redo command applies to the following actions:

- Placing
- Deleting
- Moving
- Resizing
- Rotating
- Mirroring

Shortcuts: Toolbar:

Keyboard: ALT, E, E or CTRL+Y

Repeat command

Available from: Edit menu

Function: Use this command to repeat the last operation on the currently selected object, when the last operation can be repeated. The name of the command changes, depending on what the last repeatable operation was—for example, Repeat Rotate or Repeat Paste. This command is most useful for placing objects and creating arrays of objects quickly.

The Redo command applies to the following actions:

- Placing
- Moving
- Resizing
- Rotating
- Mirroring

Shortcuts: Keyboard: ALT, E, R or F4

Label State commands

Set

Available from: Edit menu

Function: Use this command to specify a label for the current state of the active schematic page.

GoTo

Available from: Edit menu

Function: Use this command to specify the label of the schematic state to which you want to return.

Delete

Available from: Edit menu

Function: Use this command to specify a label state to delete.

Cut command

Available from: Edit menu

Use this command to remove the selected object from the active window and put it on the Clipboard. This command is only available when an object is selected.

Function: Cutting objects to the Clipboard replaces any objects previously stored there. Use the Paste command to copy objects to another page or part, or to another Windows application that supports pasting from the Clipboard.

Note: The Cut and Copy commands are unavailable in the part editor when you have one or more pins selected with other objects (such as an arcs and lines).

Toolbar:

Shortcuts: Keyboard: ALT, E, T or CTRL+X

Pop-up menu: Cut

Copy command

Available from: Edit menu

Use this command to copy a selected object to the Clipboard without removing it from the active window. This command is available only if an object is selected.

Function: Copying objects to the Clipboard replaces any objects previously stored there. Use the Paste command to copy objects to another page or part, or to another Windows application that supports pasting from the Clipboard.

Note: The Cut and Copy commands are unavailable in the part editor when you have one or more pins selected with other objects (such as arcs and lines).

Toolbar:

Shortcuts: Keyboard: ALT, E, C or CTRL+C

Pop-up menu: Copy

Paste command

Available from: Edit menu

Use this command to place any objects stored on the Clipboard into the active window. This command is unavailable if the Clipboard is empty.

Function: Pasting objects from the Clipboard does not affect the Clipboard's contents. Use Paste to copy objects to another page or part, or to another Windows application that supports pasting from the Clipboard. You can only paste text into text boxes.

Note: If you copy a part into the Clipboard and then paste it onto a schematic page, Capture will automatically assign a unique reference designator to the pasted part when two conditions are met:

1. The Auto Reference option on the Miscellaneous tab of the Preferences dialog box is selected.
2. The pasted part has a reference designator assigned to it when it is copied to the Clipboard.

Capture assigns the reference designator, updated to the next available value (one greater than the highest value used on the schematic at that point.) If the pasted part has a default reference (for example, R?) Capture does not assign a unique reference designator to it.

Toolbar:

Shortcuts: Keyboard: ALT, E, P or CTRL+V

Pop-up menu: Paste

Delete command

Available from: Edit menu

Function: Use this command to remove the selected object from the active window without putting it on the Clipboard. This command is available only if an object is selected.

Deleting objects does not affect the Clipboard's contents.

Shortcuts:

Keyboard:

- ALT, E, D
- BACKSPACE
- DEL
- DELETE
- Pop-up menu: Delete

Label command

Available from: Edit menu

Function:

Use this command to tag the schematic designs at different stages of development. This command is useful when you want to quickly jump to a particular state of schematic design. For example, consider the situation while developing a schematic:

1. Place a 7400 part.
2. Add the ATOD library to the design.
3. Place the 5962-8700 part on the schematic
4. Join the components.
5. Add the Discrete library to the schematic.
6. Place the 126ANS part on the schematic.

At this point you realize that instead of 5962-8700 part, the 5962-87786 part should have been used. Now, to do so, you can either undo the last three steps. Alternately, you could have used the label state option to label the schematic at different stages of design. For example, you could have set a label, say stage2, after step 2. In such a scenario, you could have used the label and jumped straight to the state of the schematic as it was after step 2, thus saving yourself a lot of effort.

Note: A label can have a maximum of 31 characters.

Shortcuts:

Keyboard:

- Set: Ctrl + Shift + F2
- Goto: Ctrl + Shift + F5
- Delete: Ctrl + Shift+ F7

Select All command

Available from: Edit menu

Function: Use this command to select all items in the active window.

Shortcuts: Keyboard: ALT, E, L or CTRL+A

Parts command

Available from: Edit menu, Browse command

Function: Use this command to list the parts of the selected schematic pages in the browse window. The Browse Properties dialog box gives you the option to use instances or occurrences.

You can sort the parts in the browser spreadsheet by clicking the button at the top of each column in the browse window. Capture only displays the occurrences of the parts in the browse window.

You can select single or multiple parts and edit them with the Properties command. When you edit one part, a part editor window appears. When you select multiple parts, the Browse spreadsheet editor appears.

Shortcuts: Keyboard: ALT, B, P

Properties command

Available from: Edit menu

In the project manager, use this command to view properties about the selected document. Using the Properties dialog box, you can access information general, type, and project about the file that is currently selected in the project manager window. You can also change the file's type. A file or project must be selected in the project manager window to access the Properties command.

Function: In the schematic page and part editors, use this command to open the property editor, where you can edit properties and other data for the selected objects.

The properties you can edit depend on the selected objects. The following lists the inherent properties you can edit and the dialog boxes in which you edit them:

Objects	Dialog box
Arcs	Edit Graphic dialog box
Images (pictures)	Not applicable
Bookmarks	Edit Bookmark dialog box
Buses Property editor	Property editor
Bus entries	User Properties dialog box
DRC markers	View DRC Marker dialog box
Ellipses	Edit Filled Graphic dialog box
Hierarchical blocks	Property editor
Hierarchical pins	Property editor
Hierarchical ports	Property editor
IEEE symbols	Place IEEE Symbol dialog box
Junctions	Not applicable
Lines	Edit Graphic dialog box
Multiple objects	Property editor or Browse spreadsheet editor
Nets (wires and buses)	Property editor
Net aliases	Property editor
No connects	Not applicable
Off-page connectors	Edit Off-Page Connector dialog box
Parts	Property editor
Pictures (images)	Not applicable

- Part body borders
- Pins (part editor)
- Pins (schematic page editor)
- Polygons
- Polylines
- Power, ground
- Rectangles
- Text
- Title blocks
- Wires

- Not applicable
- Pin Properties dialog box (part editor)
- Property editor
- Edit Filled Graphic dialog box
- Edit Graphic dialog box
- Property editor
- Edit Filled Graphic dialog box
- Place Text dialog box
- Property editor
- Property editor

Note: You can edit homogeneous sets of the following objects in the spreadsheet editor:

- Bookmarks
- DRC markers
- Hierarchical ports
- Nets
- Off-page connectors
- Parts
- Pins

Shortcuts:

Keyboard: ALT, E, I or CTRL+E

Mouse: Double-click on a part

Pop-up menu: Edit Properties

Part command

Available from:

Edit menu

Function: Use this command to open the selected part in a part editor window.

The part command edits the part in the design cache. After saving the part, you have the option to apply your changes to just one part or all parts with the same part value in the design. If you edit the one part only, a new part is created in the cache and all other parts with the same part value are left unchanged. Otherwise, the changes are applied to the part in the cache. To replace a part in the cache with another part, use the Replace Cache command.

Shortcuts: Keyboard: ALT, E, A

Pop-up menu: Edit Part

Reset Location command

Available from: Edit menu

Function: Select the pin name and pin number text you had moved in the part editor and use this command to reset the pin name or pin number text movement. Choose a command from the menu that appears:

- To reset a pin name movement, choose Pin Name
- To reset a pin number movement, choose Pin Number

For more information, see "Moving pin name and pin number text" on page 186.

Shortcuts: Pop-up menu: Reset Location

Pin Name command

Available from: Edit menu, Reset Location command

Function: Select the pin name text you had moved in the part editor and use this command to reset the pin name movement.

For more information, see "Moving pin name and pin number text" on page 186.

Shortcuts: Pop-up menu: Reset Location

Pin Number command

Available from: Edit menu, Reset Location command

Function: Select the pin number text you had moved in the part editor and use this command

to reset the pin number movement.

For more information, see "Moving pin name and pin number text" on page 186.

Shortcuts: Pop-up menu: Reset Location

Mirror command

Available from: Edit menu

Function: Use this command to mirror selected items in the schematic page editor or the part editor. Choose a command from the menu that appears:

- Horizontally
- Vertically
- Both

Note: Multiple selected objects are mirrored and rotated as a group. They do not mirror or rotate around their individual axes.

Note: Title blocks and text cannot be mirrored or rotated.

Shortcuts: Keyboard: ALT, E, M

Horizontally command

Available from: Edit menu, Mirror command

Function: Use this command to mirror selected objects from side to side (across the Y axis).

Note: Multiple selected objects are mirrored and rotated as a group. They do not mirror or rotate around their individual axes.

Title blocks and text cannot be mirrored or rotated.

Shortcuts: Keyboard: ALT, E, M, H or SHIFT+H

Pop-up menu: Mirror Horizontally

Vertically command

Available from: Edit menu, Mirror command

Function: Use this command to mirror selected objects from top to bottom and from bottom to top (across the X axis).

Note: Multiple selected objects are mirrored and rotated as a group. They do not mirror or rotate around their individual axes.

Note: Title blocks and text cannot be mirrored or rotated.

Shortcuts: Keyboard: ALT, E, M, V or SHIFT+V

Pop-up menu: Mirror Vertically

Both command

Available from: Edit menu, Mirror command

Function: Use this command to mirror selected objects both horizontally and vertically. This is equivalent to rotating the objects by 180 degrees.

Note: Multiple selected objects are mirrored and rotated as a group. They do not mirror or rotate around their individual axes.

Note: Title blocks and text cannot be mirrored or rotated.

Shortcuts: Keyboard: ALT, E, M, B

Rotate command

Available from: Edit menu

Function: Use this command to rotate selected objects counterclockwise in 90-degree increments. Selected objects rotate as a set, not as individual objects rotating in place.

Note: Multiple selected objects are mirrored and rotated as a group. They do not mirror or rotate around their individual axes.

Note: Title blocks, text, and Non-TrueType fonts cannot be mirrored or rotated.

Shortcuts: Keyboard:

- ALT, E, O
- R
- Pop-up menu: Rotate

Find command

Available from: Edit menu

Function:

Use this command to locate an object or string of text in the active window.

The Find command supports wildcard searches. Use an asterisk (*) to match any string of characters, and a question mark (?) to match any single character.

In the schematic page editor, part editor, and project manager, the Find command will find all instances of the specified text search string. In the session log, the Find command will find the next occurrence of the specified text search string from the current position.

In the design variant schematic page, the Find command will find parts that are not present or parts with different property values attached to it.

Shortcuts: Keyboard: ALT, E, F or CTRL+F

Global Replace command

Available from: Edit menu

Function:

Use this command to locate and replace an object or a string of text in the schematic editor.

The Global Replace command does not support wildcard searches.

In the schematic page editor, the Global Replace command will find all instances of the specified text search string.

Shortcuts: Keyboard: ALT, E, B

Check Verilog syntax command

Available from: Edit menu

Function:

Use this command to check the syntax of Verilog files for errors.

When you choose Check Verilog Syntax from the Edit menu (or Check Syntax from the popup menu), the Check Syntax tool finds the first error in the file and highlights it so that you can fix it. Once you fix the error, you can continue to check the file by choosing Check Syntax from the Edit menu again.

If the project manager window is active, you can check all selected Verilog files. Or, you can check an open, active Verilog file.

Note: If you check an open file that has been modified but not saved, note that you are checking the version of the file that is open, not the version of the file saved to disk.

Note: You must have a project open to use the Check Syntax command. Error reporting for the tool requires some project resources that are not available unless a project is open.

Shortcuts: Pop-up menu: Check Syntax

Check VHDL syntax command

Available from: Edit menu

Function:

Use this command to check the syntax of VHDL files for errors.

When you choose Check VHDL Syntax from the Edit menu (or Check Syntax from the popup menu), the Check Syntax tool finds the first error in the file and highlights it so that you can fix it. Once you fix the error, you can continue to check the file by choosing Check Syntax from the Edit menu again.

If the project manager window is active, you can check all selected VHDL files. Or, you can check an open, active VHDL file.

Note: If you check an open file that has been modified but not saved, note that you are checking the version of the file that is open, not the version of the file saved to disk.

Note: You must have a project open to use the Check Syntax command. Error reporting for the tool requires some project resources that are not available unless a project is open.

Shortcuts: Pop-up menu: Check Syntax

Samples command

Available from: Edit menu

Function: Use this command to display VHDL file samples in the VHDL Samples dialog box or Verilog file samples in the Verilog Samples dialog box.

Note: The VHDL samples dialog box appears if you open a VHDL file in Capture and then use this command. The Verilog Samples dialog box appears if you open a Verilog file in Capture and then use this command.

When you select a sample in the upper box, the associated sample lines appear in the lower box. Double-click on the sample type in the upper box, or select it and click OK to copy the sample into the text editor.

Shortcuts: Keyboard: ALT, E, A

View menu

This section covers:

“Ascend Hierarchy command” on page 814

“Convert command” on page 815

“Descend Hierarchy command” on page 815

“Go To command” on page 816

“Synchronize Up command” on page 816

“Synchronize Down command” on page 816

“Synchronize Across command” on page 817

"Part command (View)" on page 817

"Previous Part command" on page 817

"Next Part command" on page 818

"Normal command" on page 818

"Package command" on page 819

"Zoom command" on page 819

"Tool Palette command" on page 822

"Toolbar command" on page 822

"Status Bar command" on page 823

"Grid command" on page 823

"Grid References command" on page 823

"Selection Filter command" on page 824

"Invoke UI command" on page 824

Ascend Hierarchy command

Available from: View menu

Function: Use this command to view the parent of the active schematic page.

If the parent schematic page is open in another window, that window becomes active; otherwise, it opens in a new schematic page editor window.

You can view and traverse the hierarchy in the project manager.

Shortcuts: Keyboard: ALT, V, A or SHIFT+A

Pop-up: Click right mouse button and choose Ascend Hierarchy

Convert command

Available from: View menu

Function: Use this command to display the active part editor window's convert view. This command is available only when the parts in the package have convert views. A dot next to this command indicates that the convert view appears in the part editor.

Shortcuts: Keyboard: ALT, V, C

Descend Hierarchy command

Available from: View menu

Function: Use this command to view the schematic page. This command is available only when the selected part or hierarchical block has an attached schematic folder or file. If the attached schematic folder has not yet been created, this command creates a new page. If the child schematic folder is open in another window, that window becomes active. Otherwise, it opens in a new schematic page editor window.

You can view and traverse the hierarchy in the project manager.

Tip

Once you have attached a file and associated a text editor with it, you can use the Descend Hierarchy command to open that file. If you have an attached schematic folder as well as an attached file, Descend Hierarchy opens the schematic folder and not the file.

Shortcuts: Keyboard: ALT, V, D or SHIFT+D

Pop-up menu: Descend Hierarchy

Go To command

Available from: View menu

Function: Use this command to center the view on a specific location, grid reference, or bookmark.

Tip

The Go To command is always available on the right mouse button context-sensitive menus in the part editor and schematic page editor. The Go To command, with the Relative option selected, is particularly useful for precise placement and spacing.

Shortcuts: Keyboard: ALT, V, G or CTRL+G

Pop-up menu: Go To

Synchronize Up command

Available from: View menu / Shortcut menu

Function: Updates the hierarchical blocks with all the changes made to the hierarchical ports of the underlying schematic of the selected hierarchical block.

Shortcuts: Keyboard: Shift + U

Synchronize Down command

Available from: View menu / Shortcut menu

Function: Updates the underlying schematic with all the changes made to the hierarchical pins of the selected hierarchical block.

Shortcuts: Keyboard: Shift + O

Synchronize Across command

Available from: View menu / Shortcut menu

Function: Updates all the instances of hierarchical block at the same level of hierarchy with the changes on the hierarchical pin of the selected hierarchical block.

Shortcuts: Keyboard: Shift + C

Part command (View)

Available from: View menu

Function: Use this command to display a single part in a multiple part package. You can edit the part in this view.

Shortcuts: Keyboard: ALT, V, A

Previous Part command

Available from: View menu

Function: Use this command to view the previous part in the package. In Part view, this command displays the previous part of the package in the part editor. In Package view, this command selects the previous part in the package.

Shortcuts:

Keyboard:

- ALT, V, V
- CTRL+B
- SHIFT+TAB (PACKAGE VIEW ONLY)

Next Part command

Available from: View menu

Function: Use this command to view the next part in the package. In Part view, this command displays the next part of the package in the part editor. In Package view, this command selects the next part in the package.

Shortcuts:

Keyboard:

- ALT, V, X
- CTRL+N
- TAB (PACKAGE VIEW ONLY)

Normal command

Available from: View menu

Function: Use this command to display the active part editor window's normal view of the part. A dot next to this command indicates that the normal view appears in the part editor.

Shortcuts:

Keyboard:

- ALT, V, N

Package command

Available from: View menu

Function: Use this command in the part editor to view all the parts in a package. Parts cannot be edited in package view.

Shortcuts: Keyboard:

- ALT, V, K

Zoom command

Available from: View menu

Function: Use this command to change your view of the schematic folder or part. Choose one of the commands listed:

- In
- Out
- Scale
- Area
- All
- Selection
- Redraw

Shortcuts: Keyboard: ALT, V, Z

In command

Available from: View menu, Zoom command

Function: Use this command to zoom in on the schematic page or part. The zoom scale is multiplied by the current zoom factor.

Capture uses the following order to determine where the view of the zoom centers:

On the pointer location

On the selected item or items

In the center of the window (not the center of the schematic page or part)

Shortcuts: Toolbar:

Keyboard: ALT, V, Z, I or SHIFT+I

Pop-up menu: Zoom In

Out command

Available from: View menu, Zoom command

Function: Use this command to zoom out from the schematic page or part. The zoom scale is divided by the current zoom factor.

Shortcuts: Toolbar:

Keyboard: ALT, V, Z, O or SHIFT+O

Pop-up menu: Zoom Out

Scale command

Available from: View menu, Zoom command

Function: Use this command to zoom to a preset or user-defined scale. The new view centers on the selected objects, the pointer location, or the center of the previous view.

Shortcuts: Keyboard: ALT, V, Z, S

Area command

Available from: View menu, Zoom command

Function: Use this command to make a specific area of the document as large as will fit in the window. You define the area by dragging a rectangle around it.

Shortcuts: Toolbar:

Keyboard: ALT, V, Z, A

All command

Available from: View menu, Zoom command

Function: Use this command to view the entire document in the active window. This command uses the size of the work area, not the limits of the objects.

Shortcuts: Toolbar:

Keyboard: ALT, V, Z, L

Selection command

Available from: View menu, Zoom command

Function: Use this command to view all selected objects.

Shortcuts: Keyboard: ALT, V, Z, E

Redraw command

Available from: View menu, Zoom command

Function: Use this command to refresh the display.

Shortcuts: Keyboard: ALT, V, Z, R or F5

Tool Palette command

Available from: View menu

Function: Use this command to show or hide the tool palette. This setting is stored in your CAPTURE.INI file and thus affects the visibility of the palette in subsequent sessions.

Shortcuts: Keyboard: ALT, V, P

Toolbar command

Available from: View menu

Function: Use this command to show or hide the toolbar. This setting is stored in your .INI file and thus affects the visibility of the toolbar in subsequent sessions. You can move the toolbar anywhere on the screen by pressing the left mouse button over the toolbar, and then moving the mouse to the toolbar's new location. If the toolbar is moved to any edge of the window, the toolbar snaps into place. Otherwise, it floats on the screen wherever it is released.

If the toolbar is floating, you can hide it by choosing Toolbar from the View menu.

Shortcuts: Keyboard: ALT, V, T

Status Bar command

Available from: View menu

Function: Use this command to show or hide the status bar. This setting is stored in your .INI file and thus affects the visibility of the status bar in subsequent sessions.

Shortcuts: Keyboard: ALT, V, S

Grid command

Available from: View menu

Function: Use this command to show or hide the grid dots. You can show or hide the grid independently in each schematic page and part you have open.

You can also set the grid dots to show or hide in the Preferences dialog box.

Shortcuts: Keyboard: ALT, V, I

Grid References command

Available from: View menu

Function: Use this command to show or hide the grid references.

You can also set the grid references to show or hide in the Design Template dialog box and the Schematic Page Properties dialog box.

Shortcuts: Keyboard: ALT, V, R

Selection Filter command

Available from: View menu

Note: You can access this command only if a schematic page is open.

Function: Use this command to control the selection of objects in a schematic page during a block-select operation.

Shortcuts: Keyboard: CTRL, I or ALT, V, F

This command is also available from the schematic page editor pop-up menu.

Invoke UI command

Available from: View menu

Function: Opens the Propagation Delay dialog box or the Relative Propagation Delay dialog box while editing these properties in the Property Editor window.

This command is available only when you have selected the grid corresponding to the Propagation Delay/Relative Propagation Delay property in the Property Editor window.

You can also access the Invoke UI command by right-clicking the grid corresponding to the Propagation Delay/Relative Propagation Delay property in the Property Editor window.

Shortcuts: Keyboard: CTRL, U or ALT, E, V

Place menu

This section covers:

“Part command” on page 826

“Parameterized Part command” on page 826

"NetGroup command" on page 826

"Wire command" on page 827

"Bus command" on page 828

"Junction command" on page 830

"Bus Entry command" on page 830

"Net Alias command" on page 830

"Power command" on page 831

"Ground command" on page 831

"Off-Page Connector command" on page 831

"Hierarchical Block command" on page 832

"Hierarchical Port command" on page 832

"Hierarchical Pin command" on page 833

"No Connect command" on page 834

"Title Block command" on page 835

"Bookmark command" on page 838

"Text command" on page 838

"Line command" on page 839

"Rectangle command" on page 840

"Ellipse command" on page 840

"Arc command" on page 840

"Elliptical Arc command" on page 841

"Bezier curve command" on page 842

"Polyline command" on page 843

"Picture command" on page 843

"OleObject command" on page 844

Part command

Available from: Place menu

Function: Use this command to place a part you select in the Place Part dialog box.

In the Place Part dialog box, you choose a part by selecting libraries to view. You may view parts from both Capture and SDT libraries. If you choose a part from an SDT library, Capture translates the library for you.

Shortcuts: Tool palette:

Keyboard: ALT, P, P or press the P key

Parameterized Part command

Available from: Place menu

Function: Use this command to place a parameterized part you select in the Place Part dialog box.

Shortcuts: Keyboard: ALT, P, D

NetGroup command

Available from: Place menu

Function: Use this command to place a NetGroup on a schematic page.

Note: You also use this dialog to add or modify associated NetGroup definitions.

Shortcuts: Keyboard: Press the U key

Wire command

Available from: Place menu

Function: Use this command to place a part you select in the Place Part dialog box.

In the Place Part dialog box, you choose a part by selecting libraries to view. You may view parts from both Capture and SDT libraries. If you choose a part from an SDT library, Capture translates the library for you.

Shortcuts: Tool palette:

Keyboard: ALT, P, W or press the W key

Auto Wire Two Points command

Available from: Place menu

Function: Use this command to auto-wire two points (pins or wires) on a schematic page.

Shortcuts: Tool palette:

Auto Wire Multiple Points command

Available from: Place menu

Function: Use this command to auto-wire multiple points (pins or wires) on a schematic page.

Shortcuts: Tool palette:

Auto Wire Connect to Bus

Available from: Place menu

Function: Use this command to auto-wire any number of points on a schematic page to a bus on the page.

Shortcuts: Tool palette:

Bus command

Available from: Place menu

Function: Use this command to place a bus. When placing a bus, you click the left mouse button to start the bus. Click the left mouse button to change the bus's direction or create a junction with another bus. Double-click the left mouse button or press ESC to end the bus, and place another bus. Press ESC again to exit the bus tool.

When placing buses, you are constrained to 90-degree angles. If you want to draw non-orthogonal buses, hold the SHIFT key down while placing the bus.

You may also use the keys B and E to start and end buses.

Important

As you place buses and wires, remember the following points:

- A bus and a wire can be connected only by name.
- If you begin or end a bus segment on a segment of a wire, a vertex is added to the wire, but no junction appears—the bus and wire are not connected.
- If you begin or end a wire segment on a segment of a bus, a vertex is added to the bus, but no junction appears—the wire and bus are not connected.
- Two buses or two wires can be connected physically.
- If you begin or end a bus segment on a segment of another bus, a vertex is added to the second bus, and a junction appears—the buses are connected.
- If you begin or end a wire segment on a segment of another wire, a vertex is added to the second wire, and a junction appears—the wires are connected.

Note: Bus names and aliases have the form X[m..n].

- X represents the "basename" (how you think of the bus, perhaps)
- m..n represents the range of signals carried by the bus.

Note that m may be less than or greater than n: both A[0..3] and A[3..0] are valid bus aliases. You can use two periods (..), a colon (:), or a dash (-) to separate m and n.

Capture ignores any spaces between the basename and the left bracket ([). For example, ADDR[0..31], ADDR[0:31], and ADDR[0-31] represent the same bus.

Shortcuts:

Tool palette:

Keyboard: ALT, P, B or press the B key

Junction command

Available from: Place menu

Function: Use this command to place a junction to connect two nets, or remove a junction connecting two nets. Junctions can only connect wires to wires, or buses to buses. Junctions cannot connect wires to buses or buses to wires.

Shortcuts: Tool palette:

Keyboard: ALT, P, J or press the J key

Bus Entry command

Available from: Place menu

Function: Use this command to place a bus entry.

Shortcuts: Tool palette:

Keyboard: ALT, P, E or press the E key

Net Alias command

Available from: Place menu

Function: Use this command to place a net alias on the selected object. To quit placing net aliases, press ESC or choose the selection tool.

Shortcuts: Tool palette:

Keyboard: ALT, P, N or press the N key

Power command

Available from: Place menu

Function: Use this command to place a power symbol.

Shortcuts:
Tool palette:
Keyboard:
ALT, P, O
F

Ground command

Available from: Place menu

Function: Use this command to place a ground symbol.

Shortcuts:
Tool palette:
Keyboard:
ALT, P, G
G

Off-Page Connector command

Available from: Place menu

Function: Use this command to place an off-page connector, which connects to another page in the schematic folder, and to isolate power to a schematic folder. Net aliases of the same name connect wires to these nets.

Note: If you have single pin nets connecting to internal signals then use off-page connectors for making connections. The use of ports is recommended when you have multiple pin nets.

Shortcuts: Tool palette:

Keyboard: ALT, P, F

Hierarchical Block command

Available from: Place menu

Function: Use this command to place a hierarchical block. A hierarchical block maps to a schematic folder, not a schematic page.

If you attach an existing schematic folder to a hierarchical block, Capture automatically creates the hierarchical pins that correspond with the schematic folder's hierarchical ports. If you descend hierarchy on a hierarchical block whose schematic folder doesn't yet exist, then Capture automatically creates the hierarchical ports that correspond with the hierarchical pins of the hierarchical block.

Shortcuts: Tool palette:

Keyboard: ALT, P, H

Hierarchical Port command

Available from: Place menu

Use this command to place a hierarchical port. A hierarchical port is electrically connected by name to a hierarchical pin or signal "above" the schematic page. Hierarchical ports can connect laterally to other hierarchical ports.

Function:

If you attach an existing schematic folder to a hierarchical block, Capture automatically creates the hierarchical pins that correspond with the schematic folder's hierarchical ports. If you descend hierarchy on a hierarchical block whose schematic folder doesn't yet exist, then Capture automatically creates the hierarchical ports that correspond with the hierarchical pins of the hierarchical block.

Note: If you have multiple pin nets, use hierarchical ports for making connections. The use of off-page connectors is recommended when you have single pin nets connecting to internal signals.

Shortcuts:

Tool palette:

Keyboard: ALT, P, I

Hierarchical Pin command

Available from:

Place menu

Use this command to place a hierarchical pin. You must select a hierarchical block to use this command. Hierarchical pins can only be placed inside hierarchical blocks. A hierarchical pin is electrically connected by name to a port or signal in the schematic folder attached to the pin's hierarchical block.

Function:

If you attach an existing schematic folder to a hierarchical block, Capture automatically creates the hierarchical pins that correspond with the schematic folder's hierarchical ports. If you descend hierarchy on a hierarchical block whose schematic folder doesn't yet exist, then Capture automatically creates the hierarchical ports that correspond with the hierarchical pins of the hierarchical block.

Shortcuts:

Tool palette:

Keyboard: ALT, P, R

No Connect command

Available from: Place menu

Function: Use this command to place a no connect symbol. This object causes unused pins to be ignored by reports that show unconnected pins. Design rule checks and netlists won't report errors for pins with no connects placed on them. No connects do not affect connected pins, even if the Is No Connect property is set to TRUE. If the No Connect property is set to TRUE and the pin is unconnected, an X appears on the pin.

No connects can also be placed by setting the Is No Connect property of a pin to TRUE. No connects cannot be deleted using the Delete command. You must either set the pin property to FALSE, or connect a wire to the pin.

Shortcuts: Tool palette:

Keyboard: ALT, P, C or press the X key

Pin command

Available from: Place menu

Function: Use this command to place one or more pins on a part. A pin is placed with each click of the left mouse button. Press ESC or choose the selection tool to stop placing pins.

Shortcuts: Tool palette:

Keyboard: ALT, P, P

Pin Array command

Available from: Place menu

Function: Use this command to place an array of pins.

Shortcuts: Tool palette:

Keyboard: ALT, P, Y

Title Block command

Available from: Place menu

Function: Use this command to place optional title blocks.

You can set title block visibility in the Design Template and Schematic Page Properties dialog boxes.

There are a number of default title block properties. You can set the values for these properties with the property editor. They are:

- Cage Code: Specifies the Cage Code.
- Design Create Date: Specifies the date of creation for the design.
- Design Create Time: Specifies the time of creation for the design.
- Design File Name: Specifies the path and file name of the design file.
- Design Modify Date: Specifies the date of the last modification to the design.
- Design Modify Time: Specifies the time of the last modification to the design.
- Design Name: Specifies the name of the design.
- Doc: Specifies the document number.
- Name: Specifies the name of the title block.
- OrgAddr1: Specifies the first line of the organization's address.
- OrgAddr2: Specifies the second line of the organization's address.
- OrgAddr3: Specifies the third line of the organization's address.
- OrgAddr4: Specifies the fourth line of the organization's address.
- OrgName: Specifies the organization’s name.
- Page Count: Specifies the number of schematic pages in the design.
- Page Create Date: Specifies the date of creation for the schematic page.
- Page Create Time: Specifies the time of creation for the schematic page.
- Page Modify Date: Specifies the date of the last modification to the schematic page.
- Page Modify Time: Specifies the time of the last modification to the schematic page.
- Page Number: Specifies the number of the schematic page. The page number determines when it will be printed in relation to the other schematic pages of the design.

- Page Size: Specifies the page size of the schematic page, as was set at creation time.
- RevCode: Specifies the revision.
- Schematic Create Date: Specifies the date of creation for the schematic folder.
- Schematic Create Time: Specifies the time of creation for the schematic folder.
- Schematic Modify Date: Specifies the date of the last modification to the schematic folder.
- Schematic Modify Time: Specifies the time of the last modification to the schematic folder.
- Source Library: Specifies the path and file name of the library from where the title block was placed.
- Schematic Page Count: Specifies the number of schematic pages in the given schematic folder.
- Schematic Page Number: Specifies the order of the schematic page within the schematic.
- Symbol Library: Specifies the name of the symbol for the title block in the Source Library.
- Title: Specifies the title.

You can add the following property to display system generated information:

- Path Name: Specifies the hierarchical blocks leading from the root to the child using the Name Property for each hierarchical block in the path.

You can use the property editor to add the following property to display the hierarchical path of the schematic on an instance of a title block:

- Schematic Path: Displays the full hierarchical path to the schematic visible and printable on the page.

Note: Title blocks and text cannot be mirrored or rotated.

Shortcuts: Keyboard: ALT, P, K

Bookmark command

Available from: Place menu

Function: Use this command to place a bookmark. A bookmark is a reference point on a schematic page for finding a location.

Shortcuts: Keyboard: ALT, P, M

Text command

Available from: Place menu

Function: Use this command to place comment text on the schematic page or part. To quit placing text, press ESC or choose the selection tool.

Note: Title blocks and text cannot be mirrored or rotated.

Shortcuts: Tool palette:

Keyboard: ALT, P, T or press the T key

Pin Array command

Available from: Place menu

Function: Use this command to place an array of pins.

Shortcuts: Tool palette

Keyboard: ALT, P, Y

IEEE Symbol com\mand

Available from: Place menu

Function: Use this command to place an IEEE symbol. When you select this command, the Place IEEE Symbol dialog box appears.

Click the left mouse button to place an IEEE symbol once you have selected a symbol. Press ESC, or click on the selection tool, to quit placing the selected symbol. You can choose the Properties command from the Edit menu, or the Edit Properties command from the right mouse button pop-up menu, to change the IEEE symbol without having to quit the IEEE symbol tool.

Shortcuts: Tool palette:

Keyboard: ALT, P, E

Line command

Available from: Place menu

Function: Use this command to draw a line. To place a line, you press the left mouse button to start the line. Without releasing the left mouse button, drag the pointer to the other end point for the line. Release the left mouse button.

You may also use the keys B and E to start and end lines.

Shortcuts: Tool palette:

Keyboard: ALT, P, L

Rectangle command

Available from: Place menu

Function: Use this command to draw a rectangle. Press the left mouse button and drag the pointer to define the rectangle. To quit drawing rectangles, press ESC, or click on the selection tool.

To draw a square, hold down the SHIFT key while drawing.

Shortcuts: Tool palette:

Keyboard: ALT, P, R

Ellipse command

Available from: Place menu

Function: Use this command to draw an ellipse. Press the left mouse button and drag the pointer to define the ellipse. To quit drawing ellipses, press ESC, or click on the selection tool.

To draw a circle, hold down the SHIFT key while drawing.

Shortcuts: Tool palette:

Keyboard: ALT, P, S

Arc command

Available from: Place menu

Function:

Use this command to draw a circular arc. To quit drawing arcs, press ESC, or click on the selection tool.

When drawing an arc, click the left mouse button to place the center of the arc. Then move the pointer to increase or decrease the arc radius. Click the left mouse button a second time to set the radius size. Now move the pointer to increase or decrease the arc length. Rotate the pointer counter-clockwise to increase the arc length. Click the left mouse button again to set the arc length.

OR

Move the pointer to the center of the arc and press the left mouse button. Drag the mouse and then release the left mouse button to establish the radius of the arc and the location of one end of the arc. Use the mouse to establish the other end of the arc; click the left mouse button to accept the arc.

Shortcuts:

Tool palette:

Keyboard: ALT, P, A

Elliptical Arc command

Available from:

Place menu

Function:

Use this command to draw an elliptical arc. To quit drawing arcs, press ESC, or click on the selection tool.

When drawing an arc, click the left mouse button to place the top or bottom of the arc. Then move the pointer to increase or decrease the arc radius. Click the left mouse button a second time to set the radius size and the start point of the arc. Now move the pointer to increase or decrease the arc length. Rotate the pointer counter-clockwise to increase the arc length. Click the left mouse button again to set the arc length and the end point of the arc.

OR

Move the pointer to the top or bottom of the arc and press the left mouse button. Drag the mouse and then release the left mouse button to establish the radius of the arc and the location of the start point of the arc. Use the mouse to establish the length of the arc; click the left mouse button to accept the end point of the arc.

Shortcuts:

Tool palette:

Keyboard: ALT, P, C

Bezier curve command

Available from:

Place menu

Function:

Use this command to draw a Bezier curve. To quit drawing arcs, press ESC, or click on the selection tool.

When drawing a Bezier curve, click the left mouse button to define the start point of the curve. The click the left mouse button to define the first control point, again the left mouse button to define the second control point of the curve. Finally, click the left mouse button to define the end point of the curve.

Shortcuts:

Tool palette:

Keyboard: ALT, P, Z

Polyline command

Available from: Place menu

Function: Use this command to draw a polyline or polygon. To quit drawing polylines or polygons, press ESC, or click on the selection tool. Click the left mouse button once to place one segment of the line and start another. Double-click the left mouse button to end the line when drawing polylines, or single-click the left mouse button to end the line while drawing polygons.

When placing polylines, you are constrained to 90-degree angles. To place a non-orthogonal polyline, hold the SHIFT key down while placing the polyline.

You may also use the keys B and E to start and end polylines.

Shortcuts: Tool palette:

Keyboard: ALT, P, Y or press the Y key

Picture command

Available from: Place menu

Function: Use this command to place images on the schematic. This command displays the standard Insert Object Windows dialog box, in which you choose to create a new object or create an Ole reference for an existing object.

After you select an object, the cursor switches to the draw mode where you drag and draw an rectangular area to fit the object.

Shortcuts: Keyboard: ALT, P, U

OleObject command

Available from: Place menu

Function: Use this command to place images on the schematic. This command displays the standard Insert Object Windows dialog box, in which you choose to create a new object or create an Ole reference for an existing object.

After you select an object, the cursor switches to the draw mode where you drag and draw an rectangular area to fit the object.

Macro menu

This section covers:

"Configure command" on page 844

"Play command" on page 845

"Record command" on page 845

"User Macro 1,2,... command" on page 845

Configure command

Available from: Macro menu

Function: Use this command to configure macros. Capture can have up to 50 configured macros in memory. You can add and remove configured macros, as well as record, save, and play them with this command.

Capture uses the macro selected in the Configure Macro dialog box to play back and record over using the Play and Record commands.

Shortcuts: Keyboard: ALT, M, C or F9

Play command

Available from: Macro menu

Function: Use this command to play the macro currently selected in the Configure Macro dialog box.

Shortcuts: Keyboard: ALT, M, P or F8

Record command

Available from: Macro menu

Function: Use this command to record over the macro currently selected in the Configure Macro dialog box. Capture creates and configures a new macro if no macros are currently configured.

Shortcuts: Keyboard: ALT, M, R or F7

User Macro 1,2,... command

Available from: Macro menu

Function: Use this command to play back your macros configured to display in this menu.

Shortcuts: Keyboard: ALT, M, X or Y

The access keys may use any alphanumeric character for X. The shortcut for Y may be any alphanumeric character or a function key (like F7), and may additionally use the CTRL key. For example, CTRL+Q and F6. For more information, see Creating macro shortcut keys.

Important

Do not assign the access key combination CTRL+ ALT+ DEL to a macro. Capture's macro system won't override this combination to restart your system.

Note: You can make an access key for a macro by placing an ampersand character (&) in front of one letter in the Menu Assignment text box of the Macro Name dialog box. For example, "&Name Wires" creates the access key combination ALT, M, N to use a macro that is configured to appear as "Name Wires" in the Macro menu.

PSpice/Markers menu

This section covers:

“Markers command” on page 847

“Marker List command” on page 847

“Voltage Level command” on page 848

“Voltage Differential command” on page 848

“Current Into Pin command” on page 849

“Power Dissipation command” on page 849

“Advanced command” on page 849

“Plot Window Templates command” on page 850

“Show All command” on page 850

“Hide All command” on page 850

“Delete All command” on page 851

Markers command

Available from: PSpice menu

Use this command to place markers in the design. You can place markers in your design to indicate the points for which you want to see simulation waveforms displayed in PSpice.

You can place markers:

- before simulation to limit results written to the waveform data file, and automatically display those traces in the active Probe window.
- during or after simulation, to automatically display traces in the active Probe window.

Function: The color of the marker in Capture and its corresponding trace in the Probe window are the same. If you change the color of one or the other, its counterpart also changes.

To view the markers in the simulation results, the schematic must be open.

Marker types on the Advanced command submenu are only available after defining a simulation profile for an AC Sweep/Noise analysis.

You can also choose to show all, hide all, delete all, or list markers using this command.

Shortcuts: Keyboard: ALT, T, G

Marker List command

Available from: PSpice menu

From the Project Manager, choose Marker List from the PSpice menu.

Function: Use this command to display or hide markers in the design. The Markers dialog box displays markers that exist in the profile. An empty check box beside a marker indicates that the marker is hidden. If a marker is hidden, it will not appear in Capture but it will still exist in the profile.

Shortcuts: Keyboard: ALT, S, L

Voltage Level command

Available from: PSpice menu, Markers submenu

From a schematic page, point to Markers on the PSpice menu.

Function: Use this command to place voltage level markers on the schematic, in a location of your choice.

Shortcuts: Keyboard: ALT, S, M, V

Voltage Differential command

Available from: PSpice menu, Markers submenu

From a schematic page, point to Markers on the PSpice menu.

Function: Use this command to place voltage differential markers on the schematic, in a location of your choice.

Shortcuts: Keyboard: ALT, S, M, D

Current Into Pin command

Available from: PSpice menu, Markers submenu

From a schematic page, point to Markers on the PSpice menu.

Function: Use this command to place current into pin markers on the schematic, in a location of your choice.

Shortcuts: Keyboard: ALT, S, M, C

Power Dissipation command

Available from: PSpice menu, Markers submenu

From a schematic page, point to Markers on the PSpice menu.

Function: Use this command to place power dissipation markers on the schematic, in a location of your choice.

Shortcuts: Keyboard: ALT, S, M, P

Advanced command

Available from: PSpice menu, Markers submenu

From a schematic page, point to Markers on the PSpice menu.

Function: Use this command to place markers for AC Sweep/Noise analysis.

Note: Marker types on the Advanced command submenu are only available after defining a simulation profile for an AC Sweep/Noise analysis.

Plot Window Templates command

Available from: PSpice menu, Markers submenu

From a schematic page, point to Markers on the PSpice menu.

Function: Use this command to place a plot window template marker on the schematic. The marker will restore the associated template when you run the simulation in PSpice.

Shortcuts: Keyboard: ALT, S, M, T

Show All command

Available from: PSpice menu, Markers submenu

From a schematic page, point to Markers on the PSpice menu.

Function: Use this command to display all the markers on the schematic.

Shortcuts: Keyboard: ALT, S, M, S

Hide All command

Available from: PSpice menu, Markers submenu

From a schematic page, point to Markers on the PSpice menu.

Function: Use this command to hide all the markers on the schematic

Shortcuts: Keyboard: ALT, S, M, H

Delete All command

Available from: PSpice menu, Markers submenu

Function: From a schematic page, point to Markers on the PSpice menu.

Use this command to delete all the markers on the schematic.

Shortcuts: Keyboard: ALT, S, M, E

Accessories menu

This section covers:

"Accessories command" on page 851

Accessories command

Available from: Accessories menu

Function: You can use extensions to the Cadence-supplied functionality of Capture if you purchase software developed by associates of Cadence. These associates create .DLL files that address specific Capture functionality, such as customized netlisting. The associates configure their .DLL files so that they are listed as menu choices in the Accessories menu, which is available in either the project manager window or the schematic page editor window.

Options menu

This section covers:

"Autobackup command" on page 852

"Part Properties command" on page 852

"Package Properties command" on page 854

"Preferences command" on page 854

"Design Template command" on page 855

"Schematic Page Properties command" on page 855

Autobackup command

Available from: Options menu

Function:

Determines the frequency, location, and the number of copies of autobackup done by Capture.

The Multi-level backup Settings dialog box appears when you choose Autobackup option from the Options menu.

Enter the values for the following fields to determine the duration, number of backups, and its storage.

Backup time (in minutes) - Enables you to determine the time after which Capture will perform automatic backup.

No of backups to keep - Enables you to determine the total number of backups that will be stored.

Directory for backup - Enables you to determine the storage location for the backup

Shortcuts: Keyboard: ALT, O, B

Part Properties command

Available from: Options menu

Function:

Use this command in the part editor to set part properties. The following are the default part properties:

Implementation Path
Specifies the filename and directory to the child schematic.

Implementation Type
Specifies the implementation type. For more information about implementation types, see Attach Implementation dialog box.

Implementation
Specifies the name of the child schematic for the part.

Name
Specifies both the name and normal or convert view of the part. The part name appears to the left of the period, and the view appears to the right. This property is read-only.

Part Reference
Specifies both the part reference prefix and the reference designator. The reference designator for parts in libraries is a question mark (?), indicating a part reference that is not annotated. This property is read-only.

Pin Names Rotate
Specifies if the pin names rotate with the pins.

Pin Names Visible
Specifies if the pin names are visible in the schematic page editor. You may choose either True or False.

Pin Numbers Visible
Specifies if the pin numbers are visible in the schematic page editor. You may choose either True or False.

Reference
Specifies the part reference prefix. This property is read-only.

Schematic
Specifies the name of a part's schematic folder. This property is read-only in the part editor. It is an editable user property on parts in the schematic page editor.

Schematic Library
Specifies the name of a schematic folder's library. This property is read-only in the part editor. It is an editable user property on parts in the schematic page editor.

Value
Specifies the part value. If this is not specified when you place the part in a schematic folder, Capture uses the part name.

Note: You cannot remove a read-only property, but you can make it visible or invisible.

Shortcuts: Keyboard: ALT, O, R

Package Properties command

Available from: Options menu

Function: Use this command in the part editor to set package properties.

Note: PCB Footprint is a reserved property name. It is a package property that becomes a user property when you place a part on a design. If you want to make it visible, you must do so in the property editor. (The Display Properties dialog box appears when you click the Display button.)

Shortcuts: Keyboard: ALT, O, A

Preferences command

Available from: Options menu

Function: Use this command to set your environment preferences for the current project (and all future projects) on your system. The options you specify affect the behavior of the software, and are saved in the .INI file.

Shortcuts: Keyboard: ALT, O, P

Design Template command

Available from: Options menu

Function: Use this command to specify default settings for new projects, designs, and schematic pages. The values specified in this dialog box do not affect existing projects or designs.

Note: To change the properties of an active design, use the Design Properties command. To change the properties of an active schematic page, use the Schematic Page Properties command. You cannot change the default title block of an active schematic page.

Shortcuts: Keyboard: ALT, O, D

Schematic Page Properties command

Available from: Options menu

Function: Use this command in the schematic page editor to set schematic-page-related options.

Shortcuts: Keyboard: ALT, O, R

Window menu

"New Window command" on page 856

"Cascade command" on page 856

"Tile Horizontally command" on page 856

"Tile Vertically command" on page 856

"Arrange Icons command" on page 857

"1,2.... command" on page 857

New Window command

Available from: Window menu

Function: Use this command to create a new window, which is a copy of the currently active window. This new window is another "view" on the same data, and you can scroll the two windows to different positions.

Shortcuts: Keyboard: ALT, W, N

Cascade command

Available from: Window menu

Function: Use this command to "stack" all open Capture windows so that just their title bars are visible. The active window stays on top.

Shortcuts: Keyboard: ALT, W, C

Tile Horizontally command

Available from: Window menu

Function: Use this command to arrange open Capture windows, one above another, so that all are visible.

Shortcuts: Keyboard: ALT, W, H

Tile Vertically command

Available from: Window menu

Function: Use this command to arrange open Capture windows, one beside another, so that all are visible.

Shortcuts: Keyboard: ALT, W, V

Arrange Icons command

Available from: Window menu

Function: Use this command to arrange the icons for minimized windows across the bottom of the session frame.

Shortcuts: Keyboard: ALT, W, A

1,2.... command

Available from: Window menu

Function: Use the numbers listed at the bottom of the Window menu to view which windows are currently open, and to determine which window is active. (The active window is indicated by a check mark.) When you choose a window from this list, Capture restores that window if it was in icon form, pops it to the front of the Capture session, and makes it the active window.

Shortcuts: Keyboard: ALT, W, n (n = 1, 2, . . .)

Help menu

This section covers:

"OrCAD Capture Help command" on page 858

"Known Problems and Solutions command" on page 858

"What's New command" on page 859

"Learning OrCAD Capture command" on page 859

"About OrCAD Capture command" on page 859

"Web Resources command" on page 859

"Documentation command" on page 860

Note: To use the context-sensitive menu commands, select one or more items, then press the right mouse button. The contents of the menu differ depending on the objects selected.

OrCAD Capture Help command

Available from: Help menu

Function: Use this command to display the Help window.

Shortcuts: Toolbar:

Keyboard: ALT, H, H or F1

Known Problems and Solutions command

Available from: Help menu

Function: Use this command to display a document listing the known problems in this release of OrCAD Capture and tells you how to solve or work around these problems.

Shortcuts: Keyboard: ALT, H, K

What's New command

Available from: Help menu

Function: Use this command to display a document describing the new features and enhancements in this release.

Shortcuts: Keyboard: ALT, H, K

Learning OrCAD Capture command

Available from: Help menu

Function: Use this command to run the online, interactive tutorial.

Shortcuts: Keyboard: ALT, H, L

About OrCAD Capture command

Available from: Help menu

Function: Use this command to get the software version number, copyright information, registration number, and license information.

Shortcuts: Keyboard: ALT, H, A

Web Resources command

Available from: Project manager Help menu, or schematic page editor Help menu

Function: Use this command to link to Capture resources on the web

Shortcuts: Keyboard: ALT, H, W

Note: You can add other web resources to the displayed list by modifying your CAPTURE.INI file. Note, however, that the first resource in the list, appears as the last name in the menu. Therefore, if you want to add a web resource to the top of the list, include it in the CAPTURE.INI file as the last entry.

Documentation command

Available from: In the project manager or schematic page editor, from the Help menu, choose Documentation.

Function: Use this command to launch the HTML page, which contains links to all the documentation types (manuals and online help), product tutorial, and multimedia demonstrations shipped with this product release.

Shortcuts: Keyboard: ALT, H, D

Pop-up menu

This section covers:

“Mirror Horizontally command” on page 861

“Mirror Vertically command” on page 861

“Rotate command” on page 862

“Edit Properties command” on page 863

“Edit Part command” on page 865

“Select Entire Net command” on page 866

“Descend Hierarchy command” on page 866

"Zoom In command" on page 868

"Zoom Out command" on page 869

"Go To command" on page 869

"Delete command" on page 869

"PCB Editor Select command" on page 870

"Tooltip command" on page 871

Note: To use the context-sensitive menu commands, select one or more items, then press the right mouse button. The contents of the menu differ depending on the objects selected.

Mirror Horizontally command

Available from: Edit menu, Mirror command

Function: Use this command to mirror selected objects from side to side (across the Y axis).

Note: Multiple selected objects are mirrored and rotated as a group. They do not mirror or rotate around their individual axes.

Title blocks and text cannot be mirrored or rotated.

Shortcuts: Keyboard: ALT, E, M, H or SHIFT+H

Pop-up menu: Mirror Horizontally

Mirror Vertically command

Available from: Edit menu, Mirror command

Function: Use this command to mirror selected objects from top to bottom and from bottom to top (across the X axis).

Note: Multiple selected objects are mirrored and rotated as a group. They do not mirror or rotate around their individual axes.

Note: Title blocks and text cannot be mirrored or rotated.

Shortcuts:

Keyboard: ALT, E, M, V or SHIFT+V

Pop-up menu: Mirror Vertically

Rotate command

Available from:

Edit menu

Function:

Use this command to rotate selected objects counterclockwise in 90-degree increments. Selected objects rotate as a set, not as individual objects rotating in place.

Note: Multiple selected objects are mirrored and rotated as a group. They do not mirror or rotate around their individual axes.

Note: Title blocks, text, and Non-TrueType fonts cannot be mirrored or rotated.

Shortcuts:

Keyboard:

- ALT, E, O
- R
- Pop-up menu: Rotate

Edit Properties command

Available from:

Edit menu

In the project manager, use this command to view properties about the selected document. Using the Properties dialog box, you can access information general, type, and project about the file that is currently selected in the project manager window. You can also change the file's type. A file or project must be selected in the project manager window to access the Properties command.

Function:

In the schematic page and part editors, use this command to open the property editor, where you can edit properties and other data for the selected objects.

The properties you can edit depend on the selected objects. The following lists the inherent properties you can edit and the dialog boxes in which you edit them:

Objects	Dialog box
■ Arcs	■ Edit Graphic dialog box
■ Images (pictures)	■ Not applicable
■ Bookmarks	■ Edit Bookmark dialog box
■ Buses Property editor	■ Property editor
■ Bus entries	■ User Properties dialog box
■ DRC markers	■ View DRC Marker dialog box
■ Ellipses	■ Edit Filled Graphic dialog box
■ Hierarchical blocks	■ Property editor
■ Hierarchical pins	■ Property editor
■ Hierarchical ports	■ Property editor

IEEE symbols	Place IEEE Symbol dialog box
Junctions	Not applicable
Lines	Edit Graphic dialog box
Multiple objects	Property editor or Browse spreadsheet editor
Nets (wires and buses)	Property editor
Net aliases	Property editor
No connects	Not applicable
Off-page connectors	Edit Off-Page Connector dialog box
Parts	Property editor
Pictures (images)	Not applicable
Part body borders	Not applicable
Pins (part editor)	Pin Properties dialog box (part editor)
Pins (schematic page editor)	Property editor
Polygons	Edit Filled Graphic dialog box
Polylines	Edit Graphic dialog box
Power, ground	Property editor
Rectangles	Edit Filled Graphic dialog box
Text	Place Text dialog box
Title blocks	Property editor
Wires	Property editor

Note: You can edit homogeneous sets of the following objects in the spreadsheet editor:

- Bookmarks
- DRC markers
- Hierarchical ports
- Nets
- Off-page connectors
- Parts
- Pins

Shortcuts:

Keyboard: ALT, E, I or CTRL+E

Mouse: Double-click on a part

Pop-up menu: Edit Properties

Edit Part command

Available from:

Edit menu

Function:

Use this command to open the selected part in a part editor window.

The part command edits the part in the design cache. After saving the part, you have the option to apply your changes to just one part or all parts with the same part value in the design. If you edit the one part only, a new part is created in the cache and all other parts with the same part value are left unchanged. Otherwise, the changes are applied to the part in the cache. To replace a part in the cache with another part, use the Replace Cache command.

Shortcuts:

Keyboard: ALT, E, A

Pop-up menu: Edit Part

Select Entire Net command

Available from: Popup menu

Function: Use this command to select the entire net associated with the selected wire or bus. To select an entire net, you must first select a single wire or bus. The Select Entire Net command only works on the active schematic page.

Note: The Select Entire Net command is restricted to the active schematic page—it doesn't follow hierarchical blocks, hierarchical ports, or off-page connectors across schematic folders or schematic pages. For more information, see Tracing a net.

Remember that nets on a schematic page are electrically connected by name, by alias, or by connection to a named hierarchical port or off-page connector.

Shortcuts: Keyboard: CTRL,SHIFT,W

Pop-up menu: Select Entire Net

Descend Hierarchy command

Available from: View menu

Function: Use this command to view the schematic page. This command is available only when the selected part or hierarchical block has an attached schematic folder or file. If the attached schematic folder has not yet been created, this command creates a new page. If the child schematic folder is open in another window, that window becomes active. Otherwise, it opens in a new schematic page editor window.

You can view and traverse the hierarchy in the project manager.

Tip

Once you have attached a file and associated a text editor with it, you can use the Descend Hierarchy command to open that file. If you have an attached schematic folder as well as an attached file, Descend Hierarchy opens the schematic folder and not the file.

Shortcuts:

Keyboard: ALT, V, D or SHIFT+D

Pop-up menu: Descend Hierarchy

Update Design Hierarchy command

Available from: Pop-up menu from the Hierarchy tab in the Project manager

Function: Use this command to update the design hierarchy for the current project.

Shortcuts: Pop-up menu: Update Design Hierarchy

Show Footprint command

Available from: Popup, Show Footprint command

Function:

Use this command to open the PCB Editor Footprint Viewer for the selected schematic part.

Note: For the footprint to display in the viewer, you need to ensure that:

- a valid PCB Footprint property is defined for the part.
- the Allegro Footprints is defined in the capture.ini.
- the pcb env file contains the psmpath, padpath variables. And that both these variables are assigned valid footprint and pad file paths.

Shortcuts: Pop-up menu: Show Footprint

Zoom In command

Available from: View menu, Zoom command

Function:

Use this command to zoom in on the schematic page or part. The zoom scale is multiplied by the current zoom factor.

Capture uses the following order to determine where the view of the zoom centers:

On the pointer location

On the selected item or items

In the center of the window (not the center of the schematic page or part)

Shortcuts: Toolbar:

Keyboard: ALT, V, Z, I or SHIFT+I

Pop-up menu: Zoom In

Zoom Out command

Available from: View menu, Zoom command

Function: Use this command to zoom out from the schematic page or part. The zoom scale is divided by the current zoom factor.

Shortcuts: Toolbar:

Keyboard: ALT, V, Z, O or SHIFT+O

Pop-up menu: Zoom Out

Go To command

Available from: View menu

Function: Use this command to center the view on a specific location, grid reference, or bookmark.

Tip

The Go To command is always available on the right mouse button context-sensitive menus in the part editor and schematic page editor. The Go To command, with the Relative option selected, is particularly useful for precise placement and spacing.

Shortcuts: Keyboard: ALT, V, G or CTRL+G

Pop-up menu: Go To

Delete command

Available from: Edit menu

Function: Use this command to remove the selected object from the active window without putting it on the Clipboard. This command is available only if an object is selected.

Deleting objects does not affect the Clipboard's contents.

Shortcuts:

Keyboard:

- ALT, E, D
- BACKSPACE
- DEL
- DELETE
- Pop-up menu: Delete

PCB Editor Select command

Available from: Schematic page editor shortcut menu, when you select a component on a schematic page.

Function: Use this command to place components directly from your Capture schematic design to PCB Editor. To do this, select a component on the Capture schematic page and choose this command and then move your cursor over to the PCB Editor window, the part will be attached to the cursor and you can place it in PCB Editor.

Note: The PCB Editor Select menu option is available only when PCB Editor is active (running) and Intertool Communication (ITC) is enabled in Capture.

Shortcuts: Keyboard: select a component on the schematic page and press SHIFT+S.

Tooltip command

Available from: Schematic page editor shortcut menu, when you select the schematic part.

Note: The Tooltip menu item will not appear if you select a component on the schematic page and then invoke the pop-up menu.

Function: Use this command to toggle the display on tooltips for pins, parts and nets on the schematic page.

Shortcuts: None.

Lock command

Available from: Schematic page editor shortcut menu, when you select the schematic part.

Note: This command is disabled if the object is currently locked.

Function: Use this command to lock an object on a schematic page.

Note: You can lock one or more objects on a schematic page or you can lock all the objects in design, folder or page.

Shortcuts: None.

UnLock command

Available from: Schematic page editor shortcut menu, when you select the schematic part.

Note: This command is disabled if the object is currently unlocked.

Function: Use this command to unlock an object on a schematic page.

Note: You can unlock one or more objects on a schematic page or you can unlock all the objects in design, folder or page.

Shortcuts: None.

Save As HTML command

Available from: Find window, when you select an object in the list.

Function: Use this command to save the results of a Find operation to an HTML file. The file is saved to the save location as the current design. Also, a message, giving the name and path of the file is displayed on this command.

Shortcuts: None.

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Session log command reference

This chapter covers:

- “File menu” on page 873
- “View menu” on page 879
- “Edit menu” on page 879
- “Options menu” on page 881
- “Window menu” on page 882
- “Help menu” on page 885

File menu

“New command” on page 874

“Open command” on page 874

“Save command” on page 875

“Save As command” on page 876

“Print Preview command” on page 876

“Print command” on page 877

“Print Setup command” on page 877

“Import Design command” on page 878

“Exit command” on page 878

"1,2,3,4 command" on page 879

New command

Available from: File menu

Function:

Use this command to open a new design, library, or VHDL file. Choose a command from the menu that appears:

- Design
- Library
- VHDL File
- Verilog File

The number of open windows you can have is only limited by your available system resources. You can use the Window menu to switch among open windows (see 1,2.... command).

You can open an existing project, design, library, or VHDL file using the Open command on the File menu.

Shortcuts:

Toolbar:

Keyboard: ALT, F, N

Open command

Available from: File menu

Function:

Use this command to open an existing project, design, library, VHDL, or Verilog file in a new window. Choose a command from the menu that appears:

Design

Library

Project

VHDL File

Verilog File

The number of open windows you can have is only limited by your available system resources. You can use the Window menu to switch among open windows (see 1,2.... command).

You can open a new design, library, VHDL, or Verilog file using the New command on the File menu.

Note: When you choose the Open button on the toolbar, a standard Windows Open dialog box appears, in which you can choose the type of file you want to open in the Files of type drop-down list. Among the listed choices are SDT Schematic (*.SCH) and SDT Library (*.LIB).

Shortcuts:

Toolbar:

Keyboard: ALT, F, O

Save command

Available from:

File menu

Function:

Use this command to save the active, modified projects, designs, libraries, and VHDL files. You can save a design, library, VHDL file, or session log under a different name using the Save As command on the File menu.

Note: When you save a project, Capture automatically creates a backup with a .DBK file extension. When you save a library, Capture automatically creates a backup with a.OBK file extension. If you save only a schematic page or part, no backup is generated.

Shortcuts:

Toolbar:

Keyboard: ALT, F, S or CTRL+S

Save As command

Available from:

File menu

Function:

Use this command to save the active project, design, library, VHDL file, or session log under a different name or to save a new, unnamed project, design, library, VHDL file, or session log. You can save a design, library, schematic page, part, or session log with the Save command on the File menu.

The Save As command opens a standard Windows dialog box to save files.

Note: When you save a project, Capture automatically creates a backup with a .DBK file extension. When you save a library, Capture automatically creates a backup with a.OBK file extension. If you save only a schematic page or part, no backup is generated.

Note: When you use the Save As command, you are prompted to choose the file type from the Save As Type list in the Save As dialog box. You can choose to save the file in the current design database schema version or in a schema version that is one version prior to the application version you are currently using.

Shortcuts:

Keyboard: ALT, F, A

Print Preview command

Available from:

File menu

Use this command to see how a schematic page or part will look when printed.

Function: After setting the options in the Print Preview dialog box, click OK to preview the printed document. You can use the buttons at the top of the window to view different pages and to zoom in and out.

Note: Be prepared to wait if you attempt to print multiple pages or parts. Depending on the number and size of the pages or parts you are previewing, Capture may require extra time to display the selection.

Shortcuts: Keyboard: ALT, F, V

Print command

Available from: File menu

Function: Use this command to print the active schematic page, the active part, or the selected items in the project manager.

Note: When you print multiple copies, the copies are grouped by page, not sorted by copy.

Shortcuts: Toolbar:

Keyboard: ALT, F, P or CTRL+P

Print Setup command

Available from: File menu

Function: Use this command to choose a printer, paper source, and orientation before printing. The Print Setup command displays the Print Setup dialog box, a standard windows dialog box for configuring your printer or plotter. For more information on setting up printers and plotters, refer to the documentation for your configured printer driver.

Tip

Many times, the options for your printer are not available in the standard setup dialog box. If you do not find the options you need, try the printer setup in the Windows Control Panel.

Shortcuts: Keyboard: ALT, F, R

Import Design command

Available from: File menu

Function: Use this command to import EDIF and PDIF designs. EDIF designs must be graphical EDIF designs, and not EDIF netlists. Not all imported PDIF parts may be edited in Capture. Such parts won't affect netlists.

Exit command

Available from: File menu

Function: Use this command to exit the software. If necessary, you are prompted to save your changes.

You can also exit the software by choosing the Close command on the session frame Control menu (ALT, SPACEBAR, C).

Shortcuts: Keyboard:

ALT, F, X

ALT, SPACEBAR, C

ALT+F4

1,2,3,4 command

Available from: File menu

Function: Use the numbers listed at the bottom of the File menu to open one of the last four projects or files. Choose the file you want to open.

Shortcuts: Keyboard: ALT, F, n (n = 1, 2, 3, or 4)

View menu

This section covers:

"Toolbar command" on page 879

Toolbar command

Available from: View menu

Function: Use this command to show or hide the toolbars. This setting is stored in your .INI file and thus affects the visibility of the toolbars in subsequent sessions. You can move the toolbars anywhere on the screen by pressing the left mouse button over the toolbar, and then moving the mouse to the toolbar's new location. If the toolbar is moved to any edge of the window, the toolbar snaps into place. Otherwise, it floats on the screen wherever it is released.

If the toolbar is floating, you can hide it by choosing Toolbar from the View menu.

Shortcuts: Keyboard: ALT, V, T

Edit menu

This section covers:

"Edit menu" on page 879

"Find command" on page 880

"Clear Session Log command" on page 881

Copy command

Available from: Edit menu

Use this command to copy a selected object to the Clipboard without removing it from the active window. This command is available only if an object is selected.

Function: Copying objects to the Clipboard replaces any objects previously stored there. Use the Paste command to copy objects to another page or part, or to another Windows application that supports pasting from the Clipboard.

Note: The Cut and Copy commands are unavailable in the part editor when you have one or more pins selected with other objects (such as arcs and lines).

Toolbar:

Shortcuts: Keyboard: ALT, E, C or CTRL+C

Pop-up menu: Copy

Find command

Available from: Edit menu

Function: Use this command to locate an object or string of text in the active window.

The Find command supports wildcard searches. Use an asterisk (*) to match any string of characters, and a question mark (?) to match any single character.

In the schematic page editor, part editor, and project manager, the Find command will find all instances of the specified text search string. In the session log, the Find command will find the next occurrence of the specified text search string from the current position.

Shortcuts: Keyboard: ALT, E, F or CTRL+F

Clear Session Log command

Available from: Edit menu

Function: Use this command to clear the session log.

Shortcuts: Keyboard: ALT, E, S or CTRL+DEL

Options menu

"Preferences command" on page 881

"Design Template command" on page 882

"Product Configuration command" on page 882

Preferences command

Available from: Options menu

Function: Use this command to set your environment preferences for the current project (and all future projects) on your system. The options you specify affect the behavior of the software, and are saved in the .INI file.

Shortcuts: Keyboard: ALT, O, P

Design Template command

Available from: Options menu

Function: Use this command to specify default settings for new projects, designs, and schematic pages. The values specified in this dialog box do not affect existing projects or designs.

Note: To change the properties of an active design, use the Design Properties command. To change the properties of an active schematic page, use the Schematic Page Properties command. You cannot change the default title block of an active schematic page.

Shortcuts: Keyboard: ALT, O, D

Product Configuration command

Available from: Options menu

Function: Use this command to configure Capture for use with other products, such as PSpice. If you select a product in the Product Configuration dialog box, you will use a license for that product. Leaving a product unselected frees a license for other users in your work group.

Shortcuts: Keyboard: ALT, O, T

Window menu

"Cascade command" on page 883

"Tile Horizontally command" on page 883

"Tile Vertically command" on page 883

"Arrange Icons command" on page 884

"1,2.... command" on page 884

Close All Windows on page 884

Cascade command

Available from: Window menu

Function: Use this command to "stack" all open Capture windows so that just their title bars are visible. The active window stays on top.

Shortcuts: Keyboard: ALT, W, C

Tile Horizontally command

Available from: Window menu

Function: Use this command to arrange open Capture windows, one above another, so that all are visible.

Shortcuts: Keyboard: ALT, W, H

Tile Vertically command

Available from: Window menu

Function: Use this command to arrange open Capture windows, one beside another, so that all are visible.

Shortcuts: Keyboard: ALT, W, V

Arrange Icons command

Available from: Window menu

Function: Use this command to arrange the icons for minimized windows across the bottom of the session frame.

Shortcuts: Keyboard: ALT, W, A

1,2.... command

Available from: Window menu

Function: Use the numbers listed at the bottom of the Window menu to view which windows are currently open, and to determine which window is active. (The active window is indicated by a check mark.) When you choose a window from this list, Capture restores that window if it was in icon form, pops it to the front of the Capture session, and makes it the active window.

Shortcuts: Keyboard: ALT, W, n (n = 1, 2, . . .)

Close All Windows

Available from: Window menu

Function: Use this command to close all open windows.

Help menu

"OrCAD Capture Help command" on page 885

"Known Problems and Solutions command" on page 885

"What's New command" on page 886

"Learning OrCAD Capture command" on page 886

"About OrCAD Capture command" on page 886

"Web Resources command" on page 887

"Documentation command" on page 887

Note: To use the context-sensitive menu commands, select one or more items, then press the right mouse button. The contents of the menu differ depending on the objects selected.

OrCAD Capture Help command

Available from: Help menu

Function: Use this command to display the Capture Help window.

Shortcuts: Toolbar:

Keyboard: ALT, H, H or F1

Known Problems and Solutions command

Available from: Help menu

Function: Use this command to display a document listing the known problems in this release of OrCAD Capture and tells you how to solve or work around these problems.

Shortcuts: Keyboard: ALT, H, K

What's New command

Available from: Help menu

Function: Use this command to display a document describing the new features and enhancements in this release.

Shortcuts: Keyboard: ALT, H, K

Learning OrCAD Capture command

Available from: Help menu

Function: Use this command to run the online, interactive tutorial.

Shortcuts: Keyboard: ALT, H, L

About OrCAD Capture command

Available from: Help menu

Function: Use this command to get the software version number, copyright information, registration number, and license information.

Shortcuts: Keyboard: ALT, H, A

Web Resources command

Available from: Project manager Help menu, or schematic page editor Help menu

Function: Use this command to link to Capture resources on the web

Shortcuts: Keyboard: ALT, H, W

Note: You can add other web resources to the displayed list by modifying your CAPTURE.INI file. Note, however, that the first resource in the list, appears as the last name in the menu. Therefore, if you want to add a web resource to the top of the list, include it in the CAPTURE.INI file as the last entry.

Documentation command

Available from: In the project manager or schematic page editor, from the Help menu, choose Documentation.

Function: Use this command to launch the HTML page, which contains links to all the documentation types (manuals and online help), product tutorial, and multimedia demonstrations shipped with this product release.

Shortcuts: Keyboard: ALT, H, D

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Command Window command reference

This chapter covers:

■ “Command Window pop-up menu” on page 889

Command Window pop-up menu

“Font command” on page 889

“Background Color command” on page 890

“Text Color command” on page 890

“Save command” on page 890

“Clear All command” on page 890

Font command

Available from: Pop-up menu

Function: Use this command to change the font of the Command window

Shortcuts: None

Background Color command

Available from: Pop-up menu

Function: Use this command to change the background color of the Command window

Shortcuts: None

Text Color command

Available from: Pop-up menu

Function: Use this command to change the text color of the Command window

Shortcuts: None

Save command

Available from: Pop-up menu

Function: Use this command to save the commands in the Command window to a TCL file.

Shortcuts: None

Clear All command

Available from: Pop-up menu

Function: Use this command to clear all the commands from the Command window

Shortcuts: None

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Dialog box descriptions

The following is an exhaustive set of descriptions for the dialog boxes you may encounter while using Capture. Each description is listed alphabetically, using the dialog box title.

Add file to Project Folder dialog box

The Add File to Project Folder dialog box appears when you choose the Project command from the Edit menu.

Use this command to add files to a project. You can select multiple files to add using the CTRL key. The title bar of the dialog box displays the folder into which the files will be added (the folder currently selected in the project manager window).

Use this control...	To do this...
Look in	Browse the hierarchical drive and directory structure for your system.
File name	Select or type the name of the project or file(s) that you want to add to the Project Folder.
Files of type	Filter files by extension.

Add new column or row dialog box

The Add New Column or Add New Row dialog box appears when you click the New Column or New Row button in the property editor window.

Use this control...	To do this...
Name	Displays the name of the new property column or row to add in the property editor.
Value	Displays the value of the new property column or row to add to selected objects and in the property editor. If you enter the name of an existing property in the Name text box, its current value appears in this text box.
Always show this column/row in this filter	Select the check box to save the new column/row in the current filter. You cannot save a new column or row in the <Current properties> filter. **Note:** You can narrow your selection of objects by selecting one or more object columns/rows in the property editor before opening this dialog box. When you enter a name and value, then click OK or Apply, the property will be added to the selected objects.

New Property dialog box

The New Property dialog box appears when you click the New button in the Display Properties dialog box. The Display Properties dialog box appears when from Part editor window, you choose the Part Properties command from the Options menu.

Use this control...	To do this...
Name	Add the name of the new property column in the Part Editor.
Value	Specify an appropriate value for the new property added.

Add to Project dialog box

The Add to Project dialog box appears when you select the Library command from the File – New menu, with the focus away from the currently open schematics or the project manager. The dialog box prompts you to either add the new library to the currently open projects or to a new project.

Annotate dialog box

The Annotate dialog box appears when you choose Annotate from the Tools menu, or when you click the Annotate button on the Capture toolbar. A .DSN file must be selected first in the Capture project manager.

Use this tab...	To do this...
Packaging tab	Annotate parts and group parts together that have common characteristics. Packaging is a key step that should be done before netlisting to a PCB board design tool such as PCB Editor, Layout, or others.
PCB Editor reuse tab	Generate a reuse module or renumber the reference designators in a reuse module in Capture. Reuse modules may be netlisted then used in PCB Editor or used in Capture as library parts or as hierarchical blocks.
Layout reuse tab	Generate a reuse module or renumber the reference designators in a reuse module in Capture. Reuse modules may be netlisted then used in Layout or used in Capture as library parts or as hierarchical blocks.

Packaging tab

The Annotate dialog box appears when you choose Annotate from the Tools menu or when you choose the Annotate button on the toolbar. To annotate a design you must first select a .DSN object in the Capture project manager.

Use this control...	To do this...
Refdes control required	Check this option, if you want to specify a part reference range for each schematic page or a hierarchical block in the root-level of your design. *Important* This functionality works independently from the existing annotation behavior of Capture. *Important* If you are using the Refdes control required option for a project, then the Auto reference placed part option in the Miscellaneous tab of the Preferences dialog box will not honor the range specified in the grid. For more description about how to use this option to specify a part reference range for a schematic page or a hierarchical block, see Customizing part references in a design.
Scope ■ Update entire design ■ Update selection ■ Schematic Pages ■ Hierarchical Blocks	Specify whether to update all the part references in the design (or library), or just the selected schematic pages. **Note:** These options are available only when you select the Refdes control required check box. **Note:** The Scope options changes to Schematic Pages or Hierarchical Blocks depending on whether your design is a flat design or a hierarchical design.

Grid (for specifying part reference range)	**Note:** This grid appears only when you select the Refdes control required check box.
■ Pages or H-Blocks column	Displays all the schematic pages or hierarchical blocks in the root schematic folder of your design depending on whether your design is a flat design or a hierarchical design.
■ Start Value and End Value columns	Specify a numeric value greater than 0 in the cell corresponding to the schematic page name or hierarchical block name.

Tip

Use the Tab key to move from the Start Value column to End Value column.

Tip

You can also use the Arrow keys to move around in the grid.

Tip

You can use the column handle ( ) to resize the rows and columns in the grid.

Tip

A valid range must have both the Start and End Values and the End Value must be greater than the Start Value.

Action

Incremental reference update	If checked, Capture incrementally updates parts with a question mark in the part reference. For example, parts with reference designators of U?A will be numbered U1A, U1B, U1C, and so on. Part reference and package information is not updated on existing parts.
Unconditional reference update	If checked, Capture updates all parts in the selected schematic pages. Both part reference and package information may be updated on existing parts. Parts on different schematic pages are not packaged together.

Reset part references to “?”	Specifies to reset all the part references to "U?"
Add intersheet references	Specifies to add intersheet references to the design.
Annotation Type	Specifies the sequence in which the components on the design are annotated. The Annotation Sequence list contains three options that you can use to decide the sequence in which the objects on your design are annotated - Default, Left to Right & Top to Bottom.
Delete intersheet references	Specifies to remove all intersheet references from the design. **Note:** If your design contains multiple heterogeneous parts that are the same part in the package, you will need to update their part references after every time you reset all part references to "U?" or group them using a grouping property. For more information, see Defining heterogeneous and homogeneous parts.
Mode	Specifies to update either instances or occurrences. Capture automatically sets this option based on the project type. All designs default to use instances. If a PCB or schematic design is complex or has occurrence properties, the default shifts to occurrences. Capture recommends the preferred mode, which you can override.
Physical Packaging	Specifies the properties that must match for Capture to group parts into a single package. Value and Source Library properties are the default property string, but you can use any combination you like. **Note:** Do not use {GROUP} as a property string in combined property strings text box. This may cause problems while annotating your design for a PCB Editor tool, like Allegro PCB Editor. The GROUP property is used in PCB Editor for a specific purpose.

	For example, you might want to use Value and Voltage. Say your design uses both Tantalum capacitors and ceramic disk capacitors. First, you could assign ".01uF" to the part Value property for all the capacitors. Then, you could define a user property called "Voltage" for all capacitors in the design, and assign it the value "100V" or "25V" as appropriate. To annotate your design, type "{Value} {Voltage}" (without the quotation marks) in the Part Value property combine text box. In this example, Capture groups the parts with "C?" as the part reference, and ".01uF" as the part value, but it separates the 100V Tantalum capacitors from the 25V ceramic disk capacitors.
Reset reference numbers to begin at 1 in each page	Specify whether to number parts within the context of the schematic folder. When this option is selected, Capture begins numbering parts at 1 for every selected page. Otherwise, Capture continues numbering after the highest referenced part in the selected schematic pages.
Annotate as per PM page ordering	Specify whether to perform the annotation on the basis of order of pages/ folders in the Project Manager window. If there are multiple folders and multiple pages in each folder then the root folder is annotated first followed by its pages. Alphabetic order is followed to determine the sequence of pages in a folder.
Annotate as per page ordering in the title blocks	Specify whether to perform annotation according to numbers on the page numbers specified in the title blocks of the schematic pages.
Do not change the page number	Check this option if you have chosen to annotate as per page ordering in the title blocks option, changed the page numbers in the title blocks, but do not want to change the page ordering on reannotation.
Include non-primitive parts	Specifies whether to annotate non-primitive parts or to reset non-primitive part references to “?”. Select this option to avoid netlisting duplicate reference errors when you want to simulate a design or generate a new part.

PCB Editor reuse tab

The Annotate dialog box appears when you choose Annotate from the Tools menu or when you choose the Annotate button on the toolbar. To annotate a design you must first select a .DSN object in the Capture project manager.

Use this control...	To do this...
Function	
Generate Reuse modules	Check this to create a reuse design by assigning or re-assigning reuse properties to parts. ■ If the design does not contain reuse modules, then a REUSE_ID property is added to all elements of a part and there's a unique REUSE_ID for each part. All parts packaged together into the same part have the same, unique REUSE_ID. ■ If the design already contains reuse modules, then REUSE_PID values are generated during netlisting, and these values replace the REUSE_ID values. ■ If this option is unchecked and there are parts with REUSE_PID properties, then the values revert to their previous REUSE_ID values.
Renumber design for using reuse modules	Check this to option to annotate the current design for reuse. If only this option is checked, then the design is annotated but no REUSE_ID values are generated. **Note:** By checking both of these options, you can generate a reuse design and annotate it at the same time. You must check at least one of these two options or Capture generates an error message.
Action	
Incremental	If checked, Capture incrementally updates parts with a question mark in the part reference. For example, parts with reference designators or U?1 will be numbered U1A, U1B, U1C, and so on. Part reference and package information is not updated on existing parts.

Unconditional	If checked, Capture updates all parts in the selected schematic pages. Both part reference and package information may be updated on existing parts. Parts on different schematic pages are not packaged together. **Note:** If a design references an external design more than once, when annotated the reference designators of the reference designs are updated but keep their assigned packages. A reuse module root design can be annotated using the Packaging tab and checking the Unconditional reference update option. However, to be assured of avoiding duplicate part references in hierarchical reuse modules, you should check the Unconditional reference update option when you use the PCB Editor Reuse tab. **Note:** If your design contains multiple heterogeneous parts that are the same part in a package, you will need to update their part references after every time you reset all part references to "U?" or group them using a grouping property. For more information, see Defining heterogeneous and homogeneous parts.
Physical Packaging/Property Combine String	Specifies the properties that must match for Capture to group parts into a single package. Value and Source Library properties are the default property string, but you can use any combination you like. **Note:** Do not use {GROUP} as a property string in combined property strings text box. This may cause problems while annotating your design for a PCB Editor tool, like Allegro PCB Editor. The GROUP property is used in PCB Editor for a specific purpose.

	For example, you might want to use Value and Voltage. Say your design uses both Tantalum capacitors and ceramic disk capacitors. First, you could assign ".01uF" to the part Value property for all the capacitors. Then, you could define a user property called "Voltage" for all capacitors in the design, and assign it the value "100V" or "25V" as appropriate. To annotate your design, type "{Value} {Voltage}" (without the quotation marks) in the Part Value property combine text box. In this example, Capture groups the parts with "C?" as the part reference, and ".01uF" as the part value, but it separates the 100V Tantalum capacitors from the 25V ceramic disk capacitors.
Do not change the page number	Specify whether to renumber the schematic pages as part of the part reference update process.
Select modules to mark for reuse	From this list of all possible reuse modules, check which reuse modules you want to include in your design. These designs represent the root schematics of external designs that are referenced hierarchically. Currently, in Capture, the reuse module of a schematic must be the root of a design, and the design must be referenced externally from the referencing design. If you are simply storing circuitry in an external design, you do not have to select all the modules. However, if the external design has an accompanying PCB that has been laid out—and you want to reuse this PCB—then you have to make sure that you enable the check box for that design module. Schematics with REUSE_NAME properties are checked by default. Any module not checked has its REUSE_NAME properties removed. A module is only listed once, even if it has been referenced multiple times. Checking the box corresponding to the module includes the design in the netlist as a reuse module for every case. When multiple modules are displayed, you must select all the modules for hierarchical renumbering to work successfully.

Reuse annotation works quite differently for design reuse than it does for Capture's standard algorithm. Any parts not contained in a reuse module will first be annotated with Capture's standard annotation tool. Then, any section of the design contained within a checked reused module gets updated.

Part packaging is not determined by the annotation tool. Rather, the packaging in the original design will be used in the referencing design. The "numbering" will likely be different but all parts packaged together also end up packaged together in the referencing design.

Additionally, the parts of multi-part per package devices still fill the same slots in the package. In other words, the suffixes of the reference designators on the original PCB are still valid when used in the new PCB.

Layout reuse tab

The Annotate dialog box appears when you choose Annotate from the Tools menu or when you choose the Annotate button on the toolbar. To annotate a design you must first select a .DSN object in the Capture project manager.

Use this control...	To do this...
Action	Select the type of annotation that will occur. You must annotate the entire design at one time; you do not have the option of annotating only a portion of the Capture design.

Incremental reference update	If checked, Capture incrementally updates parts with a question mark in the part reference. For example, parts with reference designators of U?A will be numbered U1A, U1B, U1C, an so on. Part references and package information are not changed for existing parts that have already been annotated. For schematics that have been selected for reuse, Capture will also incrementally update the references of those parts that have question marks in their reference designators. However, Capture applies the same packaging information across all reuse schematics. Parts on schematics that have been marked for reuse will be packaged independent of non-reuse schematics and independent of each other.
Unconditional reference update	If checked, Capture updates all parts in the selected schematic pages. Both part reference and package information may be updated on existing parts. For reuse schematics, Capture also unconditionally updates the part references. However, Capture applies the same packaging information across all reuse schematics. **Note:** If a design contains internal reuse schematics, the packaging information is made consistent across all reuse schematics as the design is annotated. **Note:** If a design includes external reuse schematics, packaging information from the external reuse schematics is used when packaging the reuse schematic. An external reuse schematic can be a subschematic in an existing design. That is, it is not necessary that the external reuse schematic be the root schematic of a design. Be sure to avoid duplicate reference designators in the external reuse schematic. Otherwise, these references will be duplicated in the reuse schematics.

Note: Externally referenced schematics in Capture libraries are treated like internal reuse schematics because packaging information is not maintained when a Capture design is placed in a Capture library. Therefore, when annotated by Capture, it will be repackaged as if it was an internal reuse schematic.

Note: If your design contains multiple heterogeneous parts that are the same part in a package, you will need to update their part references after every time you reset all part references to "U?" or group them using a grouping property. For more information, see Defining heterogeneous and homogeneous parts.

Check the design for the following:

- Duplicate references
- Cross schematic reuse annotations
- Inconsistent reuse annotations

If you select this option, Capture performs checks against the design but does not change any reference designators. The results of the check appear in Capture's Session Log window.

Capture performs the following checks:

Duplicate references - Checks for duplicate references across schematic pages. This is similar to Capture's Tools\Design Rules Check\Report identical part references check, except that hierarchical block references are not checked.

Cross schematic reuse annotations - Checks to see if reuse schematic parts have been packaged outside of the reuse schematic.

Inconsistent reuse annotations - Checks to see that consistent number and packaging has been maintained across and within reuse schematics.

Note: The reuse annotation checks are automatically performed after running an Incremental reference update or Unconditional reference update.

Physical Packaging Property Combine String	Specifies the properties that must match for Capture to group parts into a single package. Value and Source Library properties are the default property string, but you can use any combination you like. For example, you might want to use Value and Voltage. Say your design uses both Tantalum capacitors and ceramic disk capacitors. First, you could assign ".01uF" to the part Value property for all the capacitors. Then, you could define a user property called "Voltage" for all capacitors in the design, and assign it the value "100V" or "25V" as appropriate. To annotate your design, type "{Value} {Voltage}" (without the quotation marks) in the Part Value property combine text box. In this example, Capture groups the parts with "C?" as the part reference, and ".01uF" as the part value, but it separates the 100V Tantalum capacitors from the 25V ceramic disk capacitors.
Do not change the page number	Specify whether to renumber the schematic pages as part of the part reference update process.

Select schematic (s) to mark for reuse	From the list of possible reuse schematics, check which schematics you want to be annotated to include reuse. The schematics listed can be internal or external schematics that are referenced in the design through a hierarchical object. Each schematic is only listed once, even if it has been referenced multiple times. When you select a schematic, the selection applies to all occurrences of that schematic in the design. Selecting multiple schematics indicates that you wish to have multiple levels of reuse and each reuse schematic will be independently packaged and kept separate from other reuse schematics. Selecting a schematic for reuse automatically includes all subschematics in that schematic. Reuse annotation works quite differently for design reuse than it does for Capture's standard algorithm. Any parts not contained in a reuse schematic will first be annotated with Capture's standard annotation tool. Then, any section of the design contained within a checked reuse schematic gets annotated next. Part packaging for internally referenced schematics and externally referenced schematics in Capture libraries are determined by Capture's annotation tool. For externally references schematics, the packaging in the original design will be used in the referenced design. The "numbering" will most likely be different, but all parts packaged together in the external schematic will be packaged together in the referenced design. Additionally, the parts of multi-part per package devices still fill the same slots in the package. In other words, the suffixes of the referenced designators of the original PCB are still valid when used in the new PCB.

Archive Project dialog box

The Archive Project dialog box appears when you choose Archive Project command from the File menu.

Use this control...	To do this...
Library files	**Note:** Archive library files and related files located in the Library folder of the project manager. These files include library (*.OLB) files, simulation and synthesis (*.VHD) files, *.STL files, and *.SML files. The PSpice model libraries are archived as follows: ❑ Profile-level model libraries are archived under their respective profiles and referenced as *.\<library_name>.lib*. For example, when a profile; AC containing a model library *diode.lib* is archived, the *diode.lib* is copied under the folder *AC* and the simulation settings is modified as: `.\diode.lib`.

- Design-level model libraries are archived under `.\<design_name-pspicefiles>\<design_name>\<library_name>.lib`. For example, when a design called *histo* containing a model library *bipolar.lib* is archived, the model library *bipolar.lib* is copied under folder `histo-pspicefiles\histo` and the simulation settings is modified as: `.\histo-pspicefiles\histo\bipolar.lib`.
- In case of global-level model libraries:
  - a copy of model library is created under the existing *<design_name>.lib*, if it exists
  - a new *<design_name>.lib* file is created and a copy of model library is added to the <design_name>lib and the simulation setting is modified as design-level library.

Output files	Archive output files generated by Capture's tools. For example, cross reference reports (*.XRF files) and EDIF netlists (*.EDN files) would be archived.
Referenced projects	Recursively save any projects referenced from within the current project.
Archive directory	Specify the drive and directory for the project to be archived in. Use the **...** button to display the Select Directory dialog box where you can locate and select a new drive, directory, or both.
Create single archive file	Activate the File name text box for specifying the name of the compressed archive file.
File name	Specify a name for the compressed archive file. The default name is <projectname-current date>.
Add more files	Add more files and folders to be archived.

Browse for	Specify whether you want to add more files or directories to your archive. Select the Directories option to add a directory or the Files option to add more files to your archive.
Additional Files/Directories	Specify files and directories you want to be archived. Use the **...** button to select the files and directories you want to archive.

Attach Implementation dialog box

The Attach Implementation dialog box appears when you choose Attach Implementation from the Edit Part Properties dialog box, or the New Part Properties dialog box.

Use this control...	To do this...
Implementation Type	Specify the type of implementation from one of the following: **Schematic View** Indicates that the attached implementation is a schematic. Capture automatically generates the appropriate hierarchical pins for the hierarchical block based on the hierarchical ports. **VHDL** Indicates that the attached implementation is a VHDL entity. Capture automatically generates the appropriate hierarchical pins for the hierarchical block based on the port declarations in the VHDL entity. **Verilog** Indicates that the attached implementation is a Verilog model. Capture automatically generates the appropriate hierarchical pins for the hierarchical block based on the port declarations in the Verilog model. **EDIF** Indicates that the attached implementation is an EDIF netlist. If your design includes EDIF implementations for hierarchical blocks, you must specify the hierarchical pins for the hierarchical block; Capture will not generate them from the EDIF netlist. Also, if your design includes EDIF implementations, you can simulate them, but you cannot compile or build them. **Project** Indicates that the attached implementation is a Capture programmable logic project. You must specify the hierarchical pins for the hierarchical block; Capture will not generate them. Attaching an implementation does not automatically add that file, project, or schematic folder to the project. You must specifically add the implementation to the project with the Project command.
Implementation	Specify the name of the attached object.

Implementation Path	Specify the path and name of the library or file where the attached object is located.

Assign Power Pins dialog box

The Assign Power Pins dialog box displays when you select a design or schematic folder or schematic page in the Project manager and choose Assign Power Pins from the Tools menu. The dialog box is also accessible when you select an object (or multiple objects) on a schematic page and from the right-click menu you choose Assign Power Pins.

Use this control...	To do this...
Source	Displays the name of the part containing the power pin. This field is read-only.
Pin No	Displays the pin number of the power pin. This field is read-only.
Power Pins	Displays the type of the power pin. For example, VCC, VDD, GND. This field is read-only.
Power Names	Displays the names of the power pin. For example, GND for a ground pin. +15V for a VCC pin.
Power Pin check box	Toggle the corresponding power pin as an NC pin

Back Annotate dialog box

The Backannotate dialog box appears when you choose the Back Annotate command from the Tools menu. This dialog box provides a method for back annotating PCB information from the board layout tool to Capture. Select the PCB Editor tab to backannotate from PCB Editor and the Layout tab to backannotate from Layout.

Note: To back annotate information from PCB Editor to Capture, refer to the Using Capture with PCB Editor workflow.

Use this control...	To do this...
Scope	Specify whether to process all the part references in the design or just in the selected schematic page or pages.
Mode	Specify to update either instances or occurrences. Capture automatically sets this option based on the project type. FPGA and PSpice projects default to instances, while PCB and Schematic projects default to occurrences.
Back Annotation File	Specify the swap file's path and filename. For more information about swap files, see Designating pins, gates, or packages for swapping.
Browse	Display a standard Windows dialog box for selecting the swap file.

Bill of Materials dialog box

The Bill of Materials dialog box appears when you choose the Bill of Materials command from the Tools menu.

Use this control...	To do this...
Scope	Select the scope of the bill of materials. The scope can cover the entire design, or the selected schematic folders and pages.
Mode	Include either instances or occurrences. Capture automatically sets this option based on the project type. FPGA and PSpice projects default to instances, while PCB and Schematic projects default to occurrences.
Line Item Definition	
Header	Specify a header that Capture inserts on each page. If this is left blank, Capture assumes there is no header. For example, "Item\tQuantity\tPart" creates a header that displays column entries of "Item", "Quantity", and "Part" each separated by a tab character.
Combined property string	Specify the properties that must match for Capture to group them in the bill of materials. Typically, this text box should be set to "{Value}" (without the quotation marks). To insert a tab, use the \t character sequence. For example, "{Reference}\t{Value}" prints a part's reference, a tab character, and the part's value. To create separate listings for 100V and 25V .01uF capacitors, for example, set the Part Value combined property string to "{Value} {Voltage}" (without the quotation marks), where Voltage is a user property in which you store the appropriate voltage values.

Place each part entry on a separate line	Specify that each part entry appears on a separate line in the bill of materials report file. When this option is selected, the quantity of parts sharing the same Part Value appear on one line, then each part is listed below. When this option is not selected, all the parts with the same Part Value are listed on one line.
Include File	
Merge an include file with report	Specify whether to merge an include file with the report. For more information about include files, see Creating an include file.
Combined property string	Specify a lookup string to match in the include file.
Include file	Specify the path and name of the include file.
Report	
Report File	Specify the bill of material's output file. For an example of a bill of materials report file, see Creating a bill of materials.
View Output	Open the bill of materials report file in a text editor.
Browse	Display a standard Windows dialog box for selecting files.

Browse File dialog box

The Browse File dialog box appears when you choose the Browse button from any dialog box with a Browse button.

Use this control...	To do this...
Look in	Specifies the drive and directory to locate the file in.
File name	Specifies the name of the file to look for.
Files of type	Specifies the type of files to look for.
Open as read-only	Specifies to open the file as a read-only file.

Color dialog box

The Color dialog box appears when you click on a color in the Colors tab in the Preferences dialog box.

Use this control...	To do this...
Basic colors	Shows the color of the object selected in the Colors tab. To change the color, click the left mouse button on a different color and then click OK.
Custom colors	This feature is disabled in Capture.
Define custom colors	This feature is disabled in Capture.

Configure Macro dialog box

The Configure Macro dialog box appears when you choose the Configure command from the Macro menu.

Use this control...	To do this...
Macro Name	Specify the name of a new macro or show the selected macro.
Configured Macros	See the list of configured macros.
Close	Close the Configure Macro dialog box.
Macro	
Record	Start recording the specified macro. When you choose Record, this dialog box is dismissed, and the macro tool palette appears.
Play	Play back the selected macro. When you choose Play, this dialog box is dismissed.
Add	Display the standard Windows Open dialog box to browse and open macro files.
Remove	Remove the selected macro from the Macro List.
File	
Save	Save the selected macro. If you have not saved the macro before, the standard Windows Save As dialog box appears for you to save the macro in a macro file.
Save As	Display the Macro Name dialog box for you to save the macro in a macro file.

Keyboard Assignment	Specify the keyboard assignment for the selected macro. Macros do not require keyboard assignments. Keyboard assignments are shown to the right of commands on the Macro menu. If you assign a shortcut to a macro command that is already in use by another command, the shortcut is temporarily assigned to the macro. When you remove the macro from the list of configured macros, the shortcut assignment reverts back to its original menu command.
Menu Assignment	Specify the menu name for the selected macro. All macros with menu assignments appear on the Macro menu. Macros do not require menu assignments.
Description	Provide a brief description about the selected macro.

Create Differential Pair dialog box

The Create Differential Pair dialog box appears when you choose the Create Differential Pair command from the Tools menu.

Use this control...	To do this...
Net/Differential Pair	View all the flat nets or differential pairs defined in a design.
All Nets/Diff Pair grid	Select the nets between which differential pair needs to be created.
Filter	Specify the nets you want to view in the All Nets grid. **Note:** To view nets of a particular type, specify the initial letters of the net in the Filter text box. All the nets of that particular type will appear in the All Nets grid. For example, if you want to view all nets starting with the letter “A”, then enter “A” in the Filter text box. All the nets starting with letter “A” will appear in the All Nets grid.
[>]	Move the selected nets from the All Nets grid to the Selections grid. *Tip* Double-click the selected net to move it to the Selections grid. *Tip* You can use the CTRL or SHIFT keys to move multiple nets to the Selections grid.
[<]	Remove the nets from the Selections grid. *Tip* Double-click the selected net to remove it from the Selections grid.

Diff Pair Name	Specify a name for the differential pair. **Note:** If the nets forming a differential pair are of the type DP+ and DP-, the name of the differential pair is set to DP. For other pairs of nets, the name of the differential pair is of the type DP*n*.
Selections grid	View the nets and the differential pair associated with those nets.
Create	Create a differential pair between the nets displayed in the Selections grid.
Modify	Change the differential pair name selected in the Selections grid.
Delete	Delete the selected differential pair selected from the design.
Auto Setup	Open the Differential Pair Automatic Setup dialog box to create multiple differential pairs simultaneously.
Close	Close the Create Differential Pair dialog box.

Note: An Auto Differential pair can also be created for a bus. To do so, you need to put _n_ & _p_ as prefix and the Auto command creates differential pairs for all bits in the bus. An Auto Differential pair can also be created for a bus. To do so, you need to put _n_ & _p_ as prefix and the Auto command creates differential pairs for all bits in the bus.

Note: In case of Flat Designs, DIFFERENTIAL_PAIR properties added through this dialog will be added on Schematic nets rather than flat nets.

Create Directory dialog box

The Create Directory dialog box appears when you click the Create Dir button in the Select Directory dialog box.

Use this control...	To do this...
Current Directory	Shows the current directory. The new directory will be a subdirectory to the current directory.
Name	Specify the name of the new directory to be created below the current directory.

Create Netlist dialog box

The Create Netlist dialog box appears when you choose the Create Netlist command from the Tools menu.

Use this tab...	To do this...
PCB Editor	Create the three files associated with PCB Editor netlist. For more information, see PCB Editor tab.
EDIF 2 0 0	Create an EDIF hierarchical netlist. It can include net, part, or pin properties. For more information, see EDIF 2 0 0 tab.
PSpice	Create a PSpice netlist that you want to examine or modify before running a simulation, or to create a subcircuit netlist. For more information, see PSpice tab. *Important* Before generating a PSpice netlist make sure that your design contains a PSpice ground symbol (0). Otherwise, you will not be able to use the netlist for running PSpice analog simulation on the design. For information on how to place PSpice ground symbol in your design, see Placing PSpice ground 0 symbols for PSpice simulations.
Spice	Create a Spice hierarchical netlist. It can include net, part, or pin properties. For more information, see SPICE tab.
VHDL	Create a 1076-87 or 1076-93 VHDL netlist. For more information, see VHDL tab.
Verilog	Create a Verilog netlist. For more information, see Verilog tab.
Layout	Create a netlist for use with OrCAD's Layout. For more information, see Layout tab.

INF	Create a netlist for use with OrCAD's Digital Simulation Tools 386+. For more information, see INF tab.
Other	Create an EDIF or Spice flat netlist of a simple hierarchy or a netlist using a format not represented on the other tabs. For more information, see Other tab.

PCB Editor tab

This dialog box can be reached by selecting the .DSN file and choosing Create Netlist from the Tools menu.

Before generating a PCB Editor netlist, you should complete the design by assigning properties, annotating, and running a Design Rules Check (DRC). Assigning appropriate PCB Editor properties, such as PCB Footprint, is a key part of successful netlisting.

The following rules apply to Capture elements you set up for netlisting.

1. Net names should not exceed 31 characters and the part name itself should not exceed 31 characters either.
2. The part name is made up of the DEVICE property value, if this value is present. If DEVICE is not present, then the part name is made up by combining the values of the Source Package, PCB footprint, and other component definition properties found in the [ComponentDefinitionProps] section of the configuration file. The values are concatenated, separated by an underscore character.

- While assigning value for the Device property, consider the following rules:
  - Do not use same device value for two components having different component definition properties PXL-Lite will ensure that there are no conflicts such as conflicts due to power pin visibility.
  - DEVICE property value equal to design name or schematics (root schematic or any schematic) name netrev

3. There are a few illegal characters which the netlister does not allow. The ‘ character (single quotation mark) is not allowed in

net, pin, or part names. Also, the ! (bang) character is not allowed in net names. Similarly, the @ character should not be used while naming library parts used for the PCB Editor.

Where there is an illegal character, it is substituted with an _ (underscore) character. You are warned if the name has been changed for any reason. There are a few exceptions: A ! (bang) character in net names is a fatal error. However, the \ (backslash) character in net names is not substituted because it is legal.

Note: Both the backslash (\ ) and underscore (_) characters in net names interfere with cross probing.

4. To generate unique net and physical part names, the name is truncated to 31 characters. If the name is not unique, the netlister generates a unique name by appending _1 (underscore plus the character 1). This digit is incremented until a unique name is formed. The length is always maintained within 31 characters.

5. To exclude PSpice specific parts from a PCB Editor netlisting, you need to set their PSpiceOnly property to TRUE. So, if PSpiceOnly is set to TRUE, no error is thrown for missing or zero pin numbers while netlisting.

Note: You can check the Capture session log for netlisting details and to verify that netlisting proceeded as you expected.

Note: During netlisting, multi-section, heterogeneous parts are treated as single-section parts.

Note: Both OrCAD Capture and Cadence® PCB Router products use .DSN as the extension for their design files. Keep the two different file types in separate directories to avoid the possibility of one file overwriting the other.

Note: Except for occurrence properties, the schematics of externally-referenced libraries and designs should not be edited. You should view them as read-only designs. Trying to edit, then save, these designs from within your schematic can introduce errors such as duplicate reference designators and other problems. Since Capture saves your design before netlisting, you might notice instance properties in externally-referenced designs do not get updates.

When saving schematics with externally-referenced libraries or designs, occurrence properties are saved but altered instance values

are not. If you want to change externally-referenced libraries or designs you should first close the referencing design. Then, open the referenced library or design, make the necessary changes, and save and close the referenced library or design. At this point, you can reopen the original design and reference the modified design. To learn more about preparing your design for netlisting, see additional topics on pin swapping and no-connect pins. Here are the options available in the PCB Editor tab of the Create Netlist dialog box:

Use this control...	To do this...
PCB Footprint	Specify a property name for PCB footprint using combined property string. The default property name is PCB Footprint. You can use the combined property string to pass user-defined properties as PCB Footprint property for PCB Netlist generation. This gives you the flexibility of defining a user-defined PCB Footprint property specifically for the PCB Editor flow. As a result, you can define different PCB Footprint properties for different PCB flows.
Setup button	Click this button to open the Setup dialog box where you can specify, edit, and view a configuration file. This file contains a list of properties available for mapping between Capture and PCB Editor. You can also specify the number of backup versions to be maintained for the PST*.DAT netlist files.
Create PCB Editor Netlist	Select this check box to generate a netlist in PCB Editor format which consist of the PSTCHIP.DAT, PSTXNET.DAT, and PSTXPRT.DAT files. This check box is selected by default. Selecting ensures the three PST*.DAT files are found in the project manager when the netlisting is complete, or in the directory you designate for the Netlist Files Directory. If this check box is cleared, no netlisting takes place and the Options below this check box are unavailable.

Location where the PST*.DAT files are to be saved. The default location is the directory named the last time this dialog box was invoked for the current design.

Netlist Files Directory

- If this is the first time the design is being netlisted, the default location will be an Allegro subfolder in your design directory.
- If the netlist files have been generated previously for the project, then the default is last directory used with this dialog box for a design.

Select this check box to automatically open the three PST*.DAT netlist files to be displayed in separate Capture windows for viewing and editing after netlisting is completed. The default for this option is to leave it cleared.

View Output

- If .DAT files are registered to Capture, they will open in Capture. If not, they will open in whatever program they are registered to, such as Notepad or WordPad.
- When this check box is unchecked, the PST*.DAT files will not be opened automatically, but they can be found in the project manager and in the directory specified by Netlist Files Directory.

Create or Update PCB Editor Board (Netrev)

Select this check box if you want to update or create the PCB Editor board that corresponds to the netlist you are generating. If selected the Capture design is transferred and updates the PCB Editor database. This option eliminates the need to import logic into PCB Editor.

This check box is not selected by default. The options below the check box are unavailable unless the check box is selected.

Input Board File

This board is a base (or template file) on top of which the logical schematic data is placed to create a new Output Board File. If there is a board which the netlist was previously imported to, this is the default board file. If you haven't previously selected the Create or Update PCB Editor Board option for the design, then this field is empty and the logic is imported into an empty board.

Output Board File

This is the location for a new board file. The output board uses the input board as a template and the output board receives the logical data from the design.

- If you have previously netlisted and specified an output board, this is the board file listed.
- If this is the first time the netlist has been run creating or updating a board, the name will be DESIGN_FILENAME.BRD found in an Allegro subdirectory where the design is found. If the path and board name are invalid, Capture issues an error message.

Allow Etch Removal During ECO

Select this check box if you want PCB Editor to rip up etch of already-routed tracks for parts that need re-routing as a result of Capture changes. This option is not selected by default. Selecting this can save you time by automatically removing the etch up to the closest T-connection or pin, if a pin is moved due to a part placement or circuit change.

Ignore FIXED property

Select this check box if you want PCB Editor to replace and delete symbols, rip up etch, and make other changes even if elements of your design are fixed (are assigned the FIXED property).

Create user-defined properties

Select this check box to allow the creation of property definitions from the netlist.

Place Changed Components

This option lets you choose what to do when a reference designator is assigned to a different component in Capture than what the reference designator is assigned to in the board layout.

Always PCB Editor will replace all components in the layout with new components from the netlist according to their reference designators. PCB Editor places the new component at the same X,Y location and rotation as the old part. This is the default option unless you have netlisted previously with a different option selected.

If Same Same as Always, but only if the component package symbol, value, and tolerance match the original component. If there is a difference, the old component is removed, and the new component becomes an unplaced part.

Never Changes must be made by the user. All old components that had changed reference designators are removed and new ones become unplaced.

This option lets you choose what to do when a reference designator is assigned to a different component in Capture than what the reference designator is assigned to in the board layout.

Open Board in Allegro PCB Editor Select this option if you want the Output Board File to open in PCB Editor once the netlisting is done. If PCB Editor is already open, a second session is invoked with a board open. If not selected the board will not be opened in PCB Editor regardless of whether it is running.

Open Board in APD Select this option if you want the Output Board File to open in Allegro Package Designer once the netlisting is done. If APD is already open, a second session is invoked with a board open. If not selected the board will not be opened in APD regardless of whether it is running.

Board Launching Option

Open Board in Cadence SiP Select this option if you want the Output Board File to open in Cadence SiP once the netlisting is done. If Cadence SiP is already open, a second session is invoked with a board open. If not selected the board will not be opened in Cadence SiP regardless of whether it is running.

Note: If you are using the OrCAD® PCB Designer license, Allegro® PCB Editor will not open. For such situations, you can select the Open Board in OrCAD PCB Editor option to open OrCAD PCB Editor.

Open Board in OrCAD PCB Editor Select this option if you want the Output Board File to open in OrCAD PCB Editor once the netlisting is done.

Note: High speed properties will not be transferred to the OrCAD PCB Editor board. Use "Open Board in Allegro PCB Editor" option to launch boards that import high speed properties assigned within Capture.

Do not open board file Select this option if you do not want to open the Output Board File in any of the tools.

EDIF 2 0 0 tab

Capture provides two EDIF netlist formats. The first format, provided in this tab, produces either hierarchical or flat netlist output, depending on your design structure and the active mode. The second

format produces only flat netlists, and is accessible through the Other tab in the Create Netlist dialog box.

Capture manages the hierarchy by turning pages in the schematic folder into CELLs in the main LIBRARY. These cells can then be referred to by INSTANCE where needed. Because EDIF requires a define-before-use philosophy, the hierarchy appears to be inverted in the netlist (the root schematic page is the last CELL in the main LIBRARY).

Use this control...	To do this...
Part Value	Specify the value for the Part Value in the netlist, using a combined property string. Most Part Values are specified using the following combined property string: {Value}
PCB Footprint	Specify the value for the PCB Footprint in the netlist, using a combined property string. Most PCB Footprints are specified using the following combined property string: {PCB Footprint}
Options	
Allow non-EDIF characters	Create a netlist for PCB 386+ or another EDIF reader that allows non-EDIF characters. If you select this option, the EDIF formatter does not check for legal EDIF characters.
Output pin names (instead of pin numbers)	Use pin names instead of pin numbers in the netlist. Most EDIF readers expect pin names instead of pin numbers. Do not select this option to create a netlist for PC Board Layout Tools 386+.

Do not create "external" library declaration	Create a netlist file without an EDIF external statement in the netlist file. If you do not select this option, Capture uses external statements to identify OrCAD as the source of the library parts in the netlist, but some EDIF readers do not accept external statements.
Output Designator constructs	Insert designator constructs at certain locations in the netlist. Some EDIF readers require designator constructs. Use this option if your reader requires them.
Output net properties	Output net properties in addition to the normal netlist.
Output part properties	Output part properties in addition to the normal netlist.
Output pin properties	Output pin properties in addition to the normal netlist.
Output buses as scalars	Output buses as bits in the netlist.
Netlist File	Specify the drive and directory for the netlist file.
View Output	Display the generated netlist in an editor. Before you can use this option effectively, you must associate the netlist file type with an editor using the Windows Explorer. For example, if you wanted to view a VHDL netlist in Notepad using this option, you would need to associate *.VHD files with Notepad in the File Manager.

INF tab

This format file produces .INF files for use with OrCAD's Digital Simulation Tools 386+. See the *Digital Simulation Tools User's Guide* for details.

If you attach a file to any nonprimitive part or hierarchical block, Capture treats the file as a schematic folder external to the design. When this formatter uses such an external file, it won't generate the netlist for the child .INF file. Instead, Capture assumes that this file will be supplied by someone else.

The VST netlist formatter truncates the names of child schematic folders in the hierarchical design. If the schematic folder names are too long (more than eight characters) and they match, the netlist formatter won't descend into the child schematic folder or create the netlist of the part. If you restrict the names of child schematic folders to eight characters, the netlist formatter creates .INF files for each child schematic folder as expected.

Use this control...	To do this...
Part Value	Specify the value for the Part Value in the netlist, using a combined property string. Most Part Values are specified using the following combined property string: {Value}
Netlist File	Specify the drive and directory for the netlist file.
View Output	Display the generated netlist in an editor. Before you can use this option effectively, you must associate the netlist file type with an editor using the Windows Explorer. For example, if you wanted to view a VHDL netlist in Notepad using this option, you would need to associate *.VHD files with Notepad in the File Manager.

Layout tab

This format produces .MNL files for use with Layout. Netnames have no restrictions in Layout netlists; however, it is recommended that you do not include spaces in netnames. For more information, see Layout's online help or the OrCAD Layout for Windows User's Guide.

The output .MNL files are binary files, not ASCII text files. Therefore, you are unable to read them using a text editor, such as Notepad.

Note: Don't use net names that include quotation marks. Although the Layout netlist format will create a netlist that includes the net name with quotation marks, Capture will encounter problems when

you try to back annotate your design. Capture's back annotation files (.SWP) use quotation marks to identify property values.

Use this control...	To do this...
PCB Footprint	Specify the value for the PCB Footprint in the netlist, using a combined property string. Most PCB Footprints are specified using the following combined property string: {PCB Footprint}
Options	
Run ECO to Layout	Automatically load the new .MNL netlist file in Layout. The corresponding board file must already be loaded in Layout, or it will ignore the .MNL file.
User Properties are in inches/millimeters	Specify the user property scale.
Netlist File	Specify the drive and directory for the netlist file.

Other tab

For this Netlist format...	choose this .dll...
Accel	oraccel.dll
Algorex	oralgorex.dll
AlterADF	oralteraad.dll
AppliconBRAVO	orapplbrav.dll
AppliconLEAP	orapplleap.dll
Cadnetix	orcadnetix.dll
Calay	orcalay.dll
Calay90	orcalay90.dll
Case	orcase.dll

CBDS	orcbds.dll
ComputerVision	orcompvisn.dll
Dump	ordump.dll
EDIF	oredif.dll
EEDesigner	oreedesign.dll
FutureNet	orfuture.dll
HiLo	orhilo.dll
IntelADF	orinteladf.dll
Intergraph	orintergra.dll
MultiWire	ormultiwir.dll
OHDL	orohdlnet.dll
PADS 2000	orpads2k.dll
PADS-PCB	orpadspcb.dll
PCAD	orpcad.dll
PCADnlt	orpcadnlt.dll
PCBII	orpcbii.dll
PDUMP	orpdump.dll
PLDnet	orpldnet.dll
PROTEL2	orprotel2.dll
RacalRedac	orracalred.dll
RINF	orrinf.dll
Scicards	orscicards.dll
SPICE	orspice.dll
Tango	ortango.dll
Telesis	ortelesis.dll
Vectron	orvectron.dll
VST Model	orvstmodel.dll
WinBoard	orwinboard.dll
WireList	orwirelist.dll

Note: Specify a configuration file that contains the properties to be transferred to the .ONL file.

Configuration file (sample format):

```
[ENABLESWAPDETAILS]

Swap=YES

[LIBRARY]

Part Reference=NO

Implementation Type=NO

Reference=NO

Name=NO

Part Reference=NO

Pin Numbers Visible=NO

Pin Names Visible=NO

Pin Names Rotate=NO

Number=NO

Type=NO

Long=NO

Clock=NO

Dot=NO

Order=NO

Is NO Connect=NO

Swap Id=NO

Net Name=NO

SDTSourceLibName=NO

[NET]

Name=NO

Number=NO
```

```
Swap Id=NO

Type=NO

Net Name=NO

Is Global=NO
```

The above format contains the following sections:

- `[LIBRARY]` - specify the part properties that you want to be transferred to the .ONL file in this section and set the property to YES. The property will be transferred to the .ONL file. If you do not want to transfer the property to the .ONL file, then set the property to NO.
- `[NET]` - Specify the Net properties to be transferred to the .ONL file in the [NET] section and set it to YES.
- `[ENABLESWAPDETAILS]` - This section contains a property named SWAP. Set this property to YES, if you want the properties defined under [LIBRARY] and [NET] sections to be transferred to the .ONL file. If the SWAP property is set to NO, then none of the properties defined under [LIBRARY] and [NET] sections will be transferred to the .ONL file.

PSpice tab

When generating a PSpice netlist, you can choose between two types of netlist formats:

- Flat netlist

or

- Hierarchical netlist

Use the PSpice tab on the Create Netlist dialog box to generate a customized PSpice netlist using the options described below.

Use this control...	To do this...

Create Hierarchical Format Netlist	Check this box if you want to create a hierarchical netlist; leave the box unchecked for a flat netlist. A flat netlist is generated for all levels of hierarchy, starting from the top, regardless of whether you are pushed into any level of the hierarchy. Flat netlists are most commonly used as input to PCB layout tools. The flat simulation netlist format for PSpice contains device entries for all parts on a subcircuit (child) schematic multiple times, once for each instance of the hierarchical part or block used. The hierarchical netlist preserves the hierarchical information in any subcircuit (child) schematics. It contains a single .SUBCKT definition for each child schematic. The devices in the subcircuit are therefore netlisted only once. Each instance of the hierarchical part or block is then netlisted as an instance of that subcircuit (as an “X” device). The subcircuit name corresponds to the name of the subcircuit (child) schematic. **Note:** The .SUBCKT arguments nodes, parameters, and optional nodes do not have a maximum limit.
Settings	Hierarchical netlists are especially useful to IC designers who want to perform Layout vs. Schematic (LVS) verification because they are more accurate descriptions of the true circuit. You can customize the hierarchical PSpice or LVS netlist by specifying various options in the Hierarchical PSpice Netlist Settings dialog box dialog box. To reach this dialog box, click the Settings button in the PSpice tab of the Create Netlist dialog box.

Create SubCircuit Format Netlist

A subcircuit netlist cannot be simulated directly. Rather, it is a definition of a circuit—a model—that can be called by another circuit being simulated. Use one of the following options to specify how to generate netlists for subcircuits:

- **Descend** generates a definition of a hierarchical design that includes the top level circuit as well as its subcircuits. (This option is only available if Create Subcircuit Format Netlist is enabled.) If the Create Hierarchical Format Netlist is not checked, then this option combination is equivalent to creating a flat netlist.
- **Do Not Descend** generates a definition of a hierarchical design that includes only the top level circuit, without any of its subcircuits. (This option is only available if Create Hierarchical Format Netlist and Create Subcircuit Format Netlist are enabled.)

Use Template

You can select an alternate template option to define which netlisting template property to use. The template applies to both flat and hierarchical netlists. You can specify a particular netlist template for generating netlists used by other simulation tools or for creating alternate PSpice netlists that contain different part descriptions.

In OrCAD Capture, the template property specifies how primitive parts are described in the simulation netlist. A template defines the pin order and identifies which part property values to include in the netlist. A part must have a template property to be included in the simulation. (The default template is PSPICETEMPLATE.

Place DRC markers for Errors and Warnings	When selected, this option causes DRC markers to be placed on devices and pins that cause errors in the netlist and would prevent proper simulation. After creating a PSpice netlist, you can point to Browse on the Edit menu and choose DRC Markers to create a browse spreadsheet. When you double-click on a line in the browse spreadsheet, it takes you to the erroneous part in a schematic. **Note:** The netlister does not catch all errors. The PSpice Simulator will catch some errors that the netlister misses. Use the Design Rules Check dialog box to clear the DRC markers for each successive run of the PSpice netlister. Choose Design Rules Check on the Tools menu and select Delete Existing DRC Markers in the Action section on the Design Rules Check tab.
Netlist File	This is the pathname to the file you want to use for storing your netlist.
Compatibility Mode (16.2 and Prior Releases)	In OrCAD 16.2 and prior releases, if two nets of the same name are placed on different pages of a design, the nets, in the PSpice netlist, are shorted together. However, in OrCAD 16.3 and subsequent releases, the two nets are assigned unique net names in the PSpice netlist. This causes the two nets not to be shorted together. Choose this option to create a PSpice netlist with the OrCAD 16.2 and prior release functionality.
View Output	Select this option if you want the .NET file to open automatically after the netlist is generated. The .NET file is stored in the Outputs folder of the project manager.

Important

Before generating a PSpice netlist make sure that your design contains a PSpice ground symbol (0). Otherwise, you will not be able to use the netlist for running PSpice analog simulation on the design. For information on how to place PSpice ground symbol in your design, see Placing PSpice ground 0 symbols for PSpice simulations.

SPICE tab

Use this control...	To do this...
Part Value	Specify the value for the Part Value in the netlist, using a combined property string. Most Part Values are specified using the following combined property string: {Value}
Options	
Include unconnected pins	If you select this option, Capture assigns node numbers to all unconnected pins. Node numbers for unconnected pins begin at 32767 and decrease in value. If you do not select this option and there are unconnected pins on your schematic page, they are assigned a space character and Capture displays a warning.

Use net names	If you select this option, Capture uses the node names you placed on the schematic page (via aliases and hierarchical ports) where available. Not all versions of SPICE support alphanumeric node names. Check your SPICE manual for details. If your version of SPICE does not allow alphanumeric node names, you can still give them numeric names such as "17." These numeric names do not interfere with the ones generated by Capture, since the node numbers it generates begin at 10000 (except GND, which is always 0).
PCB Footprint	Specifies the value for the PCB Footprint in the netlist, using a combined property string. Most PCB Footprints are specified using the following combined property string: {PCB Footprint}
View Output	Specifies to display the generated netlist in an editor. Before you can use this option effectively, you must associate the netlist file type with an editor using the Windows Explorer. For example, if you wanted to view a VHDL netlist in Notepad using this option, you would need to associate *.VHD file with Notepad in the File Manager.

Verilog tab

Use this control...	**To do this...**
Part Value	Specify the value for the Part Value in the netlist, using a combined property string. Most Part Values are specified using the following combined property string: `{Value}`

Timescale	Specify the basic time unit (nano- or pico-second) used for simulation of the netlist. To specify the time unit, use this syntax: `` `timescale X time_unit/Y precision_unit `` where X, Y = 1, 10, or 100 time_unit, precision_unit = s, ms, us, ns, ps, or fs So, for example, a setting of `timescale 1ns/10 ps indicates that delays for the netlist are 1 ns duration with 2 decimal points of precision (since 1 ps = .01 ns). By default, Capture uses a timescale value of 1ns/1ps. If you specifically do not set a timescale for the netlist (that is, if you intentionally leave the field blank), the default timescale for your simulator is used and the timescale directive does not appear in the netlist.
Net Type	Set the default net type of all the wires in the design. By default, this value is set to "wire" (for standard logic), but you can choose "tri," "tri1," "wand," "triand," "tri0," "wor," or "trior."

Text case for Pin/Module names	Specify one of three options: ■ Lower Case - all pin names are converted to lower case in the netlist. ■ Upper Case - all pin names are converted to upper case in the netlist. **Note:** Net names are always converted to upper case in the netlist. ■ User Property for Case - pin name cases are determined via the use of a property, Vlog_Uppercase, which must be assigned to a component. This is the default setting. If Vlog_Uppercase has a value of "TRUE" all pin names are converted to upper case for that component. If the value is "FALSE" all pin names are converted to lower case for that component. All pin names in your design must have consistent case designations. That is, they must all be either upper case or lower case. If you have mixed cases for pin names (for example, if you have specified Vlog_Uppercase as "TRUE" for some components and "FALSE" for others), Capture will notify you with an error message when you attempt to create a Verilog netlist.
Netlist File	Specify the drive and directory for the netlist file, as well as the netlist file name.
View Output	Display the generated netlist in Capture's Verilog editor.
Include Power Pins	Include all power pins connected to the same named signal in the netlist. By default, only visible power pins appear in the netlist.

VHDL tab

Use this control...	To do this...
Part Value	Specify the value for the Part Value in the netlist, using a combined property string. Most Part Values are specified using the following combined property string: `{Value}`
VHDL Standard	Choose a standard. ■ The 1076-87 limits legal characters for node names to: `0..9 A..Z a..z _(underscore)` with the following limitations: ■ The first character is limited to: A..Z a..z ■ The last character is restricted from: _ (underscore) ■ The 1076-93 VHDL standard permits special characters, VHDL reserved words, and names that begin with digits. To do so, delimit the name with backslashes (\) and precede any special characters—including "internal" backslashes (not the delimiters)—with a backslash.
Options	
Entity Architecture Header	Specify default procedures which appear at the beginning of the netlist output file.
Signal Type	Specify a signal type anywhere a signal needs to be defined with a type.
Output net properties	Output net properties in addition to the normal netlist.
Output part properties	Output part properties in addition to the normal netlist.

Output buses as scalars	Write all buses as individual scalar ports when creating the netlist. This option is useful if you have a mismatch of bus and scalar pins in the hierarchy of your design.
Netlist File	Specify the drive and directory for the netlist file.
View Output	Display the generated netlist in an editor. Before you can use this option effectively, you must associate the netlist file type with an editor using the Windows Explorer. For example, if you wanted to view a VHDL netlist in Notepad using this option, you would need to associate *.VHD files with Notepad in the File Manager.

Create Pin Pairs dialog box

The Create Pin Pairs dialog box appears when you click the *Add Pin Pair* button or press the ALT+A shortcut keys in the Propagation Delay/Relative Propagation Delay dialog boxes. Use this dialog box to create a pin-pair for electrical constraints such as `PROPAGATION_DELAY` and `RELATIVE_ROPAGATION_DELAY`.

Use this control...	To do this...
First pin	Select the first pin for the pin-pair.
Second pin	Select the second pin for the pin-pair. **Note:** You cannot select the same pin in both columns.
Apply	Create a pin pair without closing the dialog box.
OK	Accept the changes and close the dialog box.

Tip

You can use the following methods to select multiple consecutive pins in the Create Pin Pairs dialog box:

- Using SHIFT+Down Arrow keys
- Using SHIFT+Left mouse button click
- Dragging the mouse pointer diagonally across the pins appearing in the combo box to select them

Similarly, you can use the CTRL+Left mouse button click to select multiple nonconsecutive pins in the Create Pin Pairs dialog box.

Create PSpice Project dialog box

The Create PSpice Project dialog box appears when you choose the OK button on the New Project dialog box after selecting the Analog or Mixed A/D option.

You must select one of two options on this dialog box:

Use this control...	To do this...
Create based upon an existing project	When you select this option, you indicate that you want to use an existing Capture project file (.OPJ) as an initial starting point for an analog or mixed signal project. If you select this option, you need to also select a project file, using either the relevant drop-down menu or the Browse button to the right. After selecting this option and choosing the OK button, a new project appears. This new project is identical to the existing project you previously selected in the following respects: ■ It has the same name. ■ It contains the same configured libraries and designs. ■ It contains renamed copies of simulation profiles, local simulation files, model libraries, include files, and marker files (.MRK).
Create a blank project	By selecting this option and choosing the OK button, you create a new project that is capable of being simulated in PSpice A/D.

Cross Reference Parts dialog box

The Cross Reference Parts dialog box appears when you choose the Cross Reference command from the Tools menu.

Use this control...	To do this...
Scope	Specify whether to cross-reference the entire design or just the selected schematic page or pages.
Mode	Include either instances or occurrences. Capture automatically sets this option based on the project type. FPGA and PSpice projects default to instances, while PCB and Schematic projects default to occurrences.
Sorting	Specify whether to sort output by part value or reference designator first.
Report	
Report the X and Y coordinates of all parts	Include the X and Y coordinates of all parts in the cross-reference report file.
Report unused parts in multiple part packages	Include unused parts in multiple-part packages in the cross-reference report file.
Report file	Specify the path and file name for the report. For an example of a cross-reference report file, see Creating a cross reference report.
Save as XRF / Save as CSV	Specify the output file type XRF or CSV.
View Output	Open the cross-reference report file in a text editor.
Browse	Display a standard Windows dialog box for selecting files.

Delete Part Property dialog box

The Delete Part Property dialog box appears when you choose Delete Part Property command from the project manager's Edit menu.

Note: The Delete Part Property command is available only when you have selected the design (.DSN) or the schematic page(s) in the Project Manager window.

Use this control...	To do this...
Property Name	Type the name of the property you want to remove.

Design Properties dialog box

The Design Properties dialog box appears when you choose the Design Properties command from the Options menu while a design file is selected.

Use this tab...	To do this...
Fonts	Change the fonts for objects with text. A standard Windows Font dialog box appears when you click on the font display of an item.
Hierarchy	Specify default settings of primitive or nonprimitive for hierarchical blocks and parts. These options affect parts and hierarchical blocks that have the Primitive property set to Default. When parts are marked as primitive, you cannot descend into them, even if they have attached schematic folders.
SDT Compatibility	Define the mapping to use when saving designs in SDT format. Capture uses the properties specified in this tab to define the part field lines when it creates an SDT.CFG during translation. To make SDT part fields carry over into Capture properties, you need to specify them in the SDT.CFG file. For more information on part fields, see Saving in SDT format and Translating part fields. Also specify which properties will be reported in the .INF file when creating a netlist using the VST tab in the Create Netlist dialog box.
Miscellaneous	Specify visibility of power pins in the design. Also displays the design name and other related information. The Date Format drop-down list provides a selection of date formatting options for title blocks. Click the down arrow to expand the list, then select a format and click OK.

Design Rules Check dialog box

The Design Rules Check dialog box displays when you choose the Design Rules Check command from the Tools menu.

Use this tab...	To do this...
Design Rules Options tab	Set the scope, mode and type of design rule (electrical and / or physical) test options for the design rules check.
Electrical Rules tab	Set the electrical design rule checks and reports to be generated from the check.
Physical Rules tab	Set the physical design rule checks and reports to be generated from the check.
ERC Matrix tab	Set the matrix rules used during the design rules check.

Design Rules Options tab

Use this control...	To do this...
Scope	Select the scope of the design rules check. The scope can cover the entire design, or selected schematic folders and pages.
Mode	Specify to check either instances or occurrences. Capture automatically sets this option based on the project type. All designs default to use instances. If a PCB or Schematic design is complex or has occurrence properties, the default shifts to occurrences. Capture recommends the preferred mode, which you can override.

Action	Specifies either a design rules check, deletion of existing DRC markers or creating DRC markers for warning. **Note:** The DRC markers are automatically deleted when you run a subsequent design rules check. Use the Ignore DRC Warnings option to specify any DRC Warnings that you do not want to be checked during the DRC check and netlisting. For example, to ignore the ALG0051 or ALG0016 warnings during netlist, specify these in the Ignore Warnings dialog.
Design Rules	Select the type of rules to run, electrical and / or physical.
Report file	Specify the path and file name for the report.
View Output	Open the design rules check report file in a text editor.
Browse	Displays a standard Windows dialog box for selecting files.

Electrical Rules tab

Electrical Rules

Use this control...	To do this...
Check single node nets	Check if the design contains any nets with only one connection.
Check no driving source and Pin type conflicts	
Check duplicate net names	Check if the design contains any duplicate net names.
Check off-page connector connections	Verify that off-page connector nets on a schematic page match those on other schematic pages.

Check hierarchical port connections	Verify that hierarchical pins in a hierarchical block match hierarchical ports in the child schematic folder or folders. Errors are generated if the number of hierarchical ports and hierarchical pins differ between the parent and child schematic folders. Also generates errors if the types of hierarchical ports are not identical between the parent and child schematic folders.
Check unconnected bus nets	Check for and reports all unconnected bus nets. This check will run for all unconnected bus nets across schematics in a design.
Check unconnected pins	Check for any pins on the design that are unconnected or do not have no-connect attached.
Check SDT compatibility	Check for SDT compatibility. For more information about SDT compatibility, see Saving in SDT format.

Reports

Use this control...	To do this...
Report all net names	List the names of all nets in the report file.
Report off-grid objects	List all objects that are on Fine grid in the report file.
Report hierarchical ports and off-page connectors	List all hierarchical ports and off-page connectors in the report file.
Report misleading tap connections	Checks for and reports those signals that are wrongly connected through a Bus Tap to a bus. Also checks for missing bus taps.

Physical Rules tab

Physical Rules

Use this control...	To do this...
Check power pin visibility	Check if the visibility property of a power pin on one section of multi-section part is different from the corresponding power pin on another section of the part.
Check missing/illegal PCB Footprint property	Check if the PCB footprint property on a part is missing or the property defined is illegal.
Check Normal Convert view sync	Check if the pin numbers on the normal view of a part are different from the pin numbers on the convert view.
Check incorrect Pin_Group assignment	Check if all pins in same pin group in a part are of the same type.
Check high speed props syntax	Check the syntax of the high speed properties of the nets in the design.
Check missing pin numbers	Check if any part on the design has missing pin numbers.
Check device with zero pins	Check if any part on the design has no pin on the part.
Check power ground short	Check if the type of power pin name inside a part is connected to a net on the schematic with a different name.
Check Name Prop consistency	Check if the occurrences of a hierarchical block have the same "Name" property.

Reports

Use this control...	To do this...
Report Visible unconnected power pins	List the names of all visible unconnected power pins.
Report unused part packages	List the names of any unused part packages.
Report invalid packaging	List any invalid packaging.
Report identical part references	List any identical part references.

ERC Matrix tab

Use this control...	To do this...
Matrix	Set the rules used by the Design Rules Check when testing connections between pins, hierarchical blocks, and hierarchical ports. The pins, hierarchical ports, and off-page connectors are listed in columns and rows in the table. A test is represented by the intersection of a row and column. Either the intersection of a row and column is empty, or it contains a "W" or an "E." An empty intersection represents a valid connection, a "W" is a warning, and an "E" represents an error. You can cycle through these three settings by pointing to an intersection and clicking the mouse button until the desired setting displays. You can also type W for warning, E for error, and N for an empty intersection. In addition to these keys, you can use the arrow keys to select other intersections.
Restore defaults	Restore the ERC matrix to its default values.

Design Template / Design Properties dialog box

The Design Template dialog box appears when you choose the Design Template command from the Options menu.

The Design Properties dialog box appears when you choose the Design Properties command from the Options menu while a design file is selected.

Use this tab...	To do this...
Fonts (available in both Design Template and Design Properties dialog box)	Change the fonts for objects with text. A standard Windows Font dialog box appears when you click on the font display of an object. These options are set once per design. Once a design is created, use the Design Properties command to change these options for a particular design.
Title Block (available only in Design Template dialog box)	Enter the title, organization name and address, document number, revision, and CAGE code into the title block. Also enter the path and filename of the library containing the title block, and the title block name. These options affect each new page. The OrCAD-supplied title block resides in the CAPSYM.OLB library. For more information about title blocks, see Setting up the default title block.
Page Size (available only in Design Template dialog box)	Specify the units of measure used in the schematic page editor. Also, change the width and height of a schematic page, as well as spacing between pins in a design. For more information, see Page Size tab.

Grid Reference (available only in Design Template dialog box)	Choose between alphabetic and numeric, and between ascending and descending for both horizontal and vertical grid references. Also set the grid count for both horizontal and vertical grid references, set the width of the grid references, and set title block visibility. For more information, see Grid Reference tab.
Hierarchy (available in both Design Template and Design Properties dialog box)	Specify default settings of primitive or nonprimitive for hierarchical blocks and parts for future designs. These options are set once per design, and affect parts and hierarchical blocks that have the Primitive property set to Default. When parts are marked as primitive, you cannot descend into them, even if they have attached schematic folders.
Miscellaneous (available only in Design Properties dialog box)	Specify visibility of power pins in the design. Also displays the design name and other related information. The Date Format drop-down list provides a selection of date formatting options for title blocks. Click the down arrow to expand the list, then select a format and click OK.
SDT Compatibility (available in both Design Template and Design Properties dialog box)	Define the mapping to use when saving designs in SDT format. It can be changed for individual designs in the SDT Compatibility tab of the Design Properties dialog box. The Part Field to Property mapping fields are used only when you save a Capture design in an SDT format. To make SDT part fields carry over into Capture properties, you need to specify them in the SDT.CFG file. For more information on part fields, see Saving in SDT format and Translating part fields.

Fonts tab

Change the fonts for objects with text. A standard Windows Font dialog box appears when you click on the font display of an object.

These options are set once per design. Once a design is created,

use the Design Properties command to change these options for a particular design.

Title Block tab

Enter the title, organization name and address, document number, revision, and CAGE code into the title block.

Also enter the path and filename of the library containing the title block, and the title block name.

These options affect each new page. The OrCAD-supplied title block resides in the CAPSYM.OLB library. For more information about title blocks, see Setting up the default title block.

Grid Reference tab

The Design Template dialog box appears when you choose the Design Template command from the Options menu.

Set these options for future schematic pages. Changing these options won't affect schematic pages you've already created.

Use this control...	To do this...
Horizontal and Vertical	
Count	Specify the number of divisions in the horizontal or vertical grid references.
Alphabetic and Numeric	Specify whether the grid references are alphabetic or numeric.
Ascending and Descending	Specify whether the grid references ascend or descend.
Width	Specify the width of the grid reference division. The width here is not the distance between grid reference division, but the amount of space taken up in the schematic page editor.
Border Visible	

Displayed	Specify whether the border is visible on the screen.
Printed	Specify whether the border is visible on paper.
Grid Reference Visible	
Displayed	Specify whether the grid references are visible on the screen.
Printed	Specify whether the grid references are visible on paper.
Title Block Visible	
Displayed	Specify whether the title block is visible on the screen.
Printed	Specify whether the title block is visible on paper.
ANSI grid references	Specify if schematic pages use the ANSI Standard grid references.

Page Size tab

The Design Template dialog box appears when you choose the Design Template command from the Options menu.

Set these options for future schematic pages. Changing these options won't affect schematic pages you've already created.

Use this control...	**To do this...**
Units	Specify the unit of measurement for future designs. Select either inches or millimeters. This only affects the schematic page editor. It doesn't affect the part editor, which is always measured in grid units.
New Page Size	Specify the size of schematic pages for future designs. The first five choices are A to E if the unit measurement is inches, or A4 to A0 if the unit measurement is millimeters.

Width	Specify the width of future schematic pages in the indicated unit measurement. The values specified here for page sizes A to E and A4 to A0 are set values in the Schematic Page Properties dialog box.
Height	Specify the height of future schematic pages in the indicated unit measurement. The values specified here for page sizes A to E and A4 to A0 are set values in the Schematic Page Properties dialog box.
Pin-to-Pin Spacing	Specify the spacing between pins in the indicated unit measurement. Also specify grid spacing. For example, a pin-to-pin spacing of 0.1 inches means that the dots or lines on your grid will be 0.1 inches apart.

Hierarchy tab

Specify default settings of primitive or nonprimitive for hierarchical blocks and parts for future designs. These options are set once per design, and affect parts and hierarchical blocks that have the Primitive property set to Default. When parts are marked as primitive, you cannot descend into them, even if they have attached schematic folders.

SDT Compatibility tab

Define the mapping to use when saving designs in SDT format. It can be changed for individual designs in the SDT Compatibility tab of the Design Properties dialog box. The Part Field to Property mapping fields are used only when you save a Capture design in an SDT format. To make SDT part fields carry over into Capture properties, you need to specify them in the SDT.CFG file. For more information on part fields, see Saving in SDT format and Translating part fields.

Differential Pair Automatic Setup dialog box

The Differential Pair Automatic Setup dialog box appears when you click the Auto Setup button in the Create Differential Pair dialog box.

Use this control...	To do this...
All Nets/Diff Pair grid	View all the flat nets or differential pairs defined in a design.
Filter	Specify the nets you want to view in the All Nets grid. **Note:** To view nets of a particular type, specify the initial letters of the net in the Filter text box. All the nets of that particular type will appear in the All Nets grid. For example, if you want to view all nets starting with the letter “A”, then enter “A” in the Filter text box. All the nets starting with letter “A” will appear in the All Nets grid
Prefix	Specify a string (numeric or alphabet) that you want to precede the differential pair name. For example, if you specify “A” in the Prefix text box, then all the differential pair names that will be created will be preceded with “A”.
+ Filter	Specify the last digit of the first net’s name. For example, all net names ending with 1.
- Filter	Specify the last digit of the second net’s name in the - Filter text box. For example, all net names ending with 4.
Diff Pair/+Net/-Net grid	View all the unique differential pairs that are generated for all the nets that qualify the criteria set in the + Filter and - Filter text boxes. The +Net and -Net grid displays the two nets associated with a differential pair.

Create	Create all the differential pairs for the nets displayed in the grid.
Remove	Remove the selected differential pair from the design. **Note:** If you do not want a specific differential pair to be created, select the row containing the differential pair and click the Remove button or double-click the row containing the differential pair. The selected row disappears.
Close	Close the Differential Pair Automatic Setup dialog box and go back to the Create Differential Pair dialog box.

Note: An Auto Differential pair can also be created for a bus. To do so, you need to put _n_ & _p_ as prefix and the Auto command creates differential pairs for all bits in the bus.

Display Properties dialog box

The Display Properties dialog box appears when you click on the Display button in the User Properties dialog box, or when you choose the Properties command from the Edit menu and click the Display button in the property editor.

Use this control...	To do this...
Name	Specifies the property's name.
Value	Specify the property's value.
Display Format	Specify the visibility for the property name and value.
Font	Displays the font name and point size.
Change	Display a standard Windows Font dialog box so you can change the font, font style, and font size of the property.
Use Default	Use the default value for the property. The default value is set in the Design Template / Design Properties dialog box (see Design Template command).
Color	Specify the property's color.
Rotation	Specify the rotation of the property.

Note: You can use the Display Properties dialog box to set the display option of an instance property and its value, but you cannot use it to display properties of an occurrence property.

Distributions dialog box

The Distributions dialog box appears when you select the Monte Carlo/Worst Case option, from the Analysis tab of the Simulate Settings dialog box, and click the Distributions button.

Use this control...	To do this...

Existing distributions	Display a list of existing distributions for tolerances, defined by you. These are only used with Monte Carlo and sensitivity/worst-case analyses.
Distribution name	Specify the name of a new distribution.
Distribution curve values	Specify up to 100 curve values for the distribution. Each curve value is defined by two values in the form (x,y), where x is the deviation and y is the probability. The deviation must be between -1 and 1. The probability must be zero, or positive.
Delete	Delete the selected distribution from the existing distributions list.
Save	Save the distribution defined by the distribution name and curve values options.

Edit Bookmark dialog box

The Edit Bookmark dialog box appears when you select a bookmark in the schematic and choose the Properties command from the Edit menu.

Use this control...	To do this...
Name	Change the name of the bookmark.

Edit Filled Graphic dialog box

The Edit Filled Graphic dialog box appears when you double-click on a closed polyline, an ellipse, a rectangle, or when you select a closed object and choose the Properties command from the Edit menu.

Use this control...	To do this...
Fill Style	Choose the fill style.
Line Style & Width	Choose the line style and width.
Color	Choose the color of the line. This option is not available in the part editor.

Edit Graphic dialog box

The Edit Graphic dialog box appears when you double-click on a line, or when you select a line and choose Properties from the Edit menu.

Use this control...	To do this...
Line Style & Width	Choose the line style and width.
Color	Choose the color of the line. This control is not available in the part editor.

Edit Hierarchical Port dialog box

The Edit Hierarchical Port dialog box appears when you select a hierarchical port, and choose Properties from the Edit menu.

Use this control...	To do this...
Name	Change the name of the hierarchical port.
Type	Select the hierarchical port type from the list of pin types.

Edit Net Alias dialog box

The Edit Net Alias dialog box appears when you choose Properties from the Edit menu with a net alias selected in the schematic page editor.

Use this control...	To do this...
Alias	Change the net alias name.
Color	Choose the color of the net alias.
Rotation	Specify the rotation of the net alias or text.
Font	
Change	Display a Font dialog box so you can select a font.
Use Default	Change the font to the default font specified in the Design Template / Design Properties dialog box.

Edit Off-Page Connector dialog box

The Edit Off-Page Connector dialog box appears when you select an off-page connector, and choose Properties from the Edit menu.

Use this control...	To do this...
Name	Change the name of the off-page connector.

Edit Part Properties dialog box

The Edit Part dialog box appears when you right-click and choose Edit Properties from the pop-up menu while placing a part.

Use this control...	To do this...
Part Value	Change the part value name.
Part Reference	Specify the part reference.
Primitive	
Default	Use the default primitive setting. The default setting is set in the Hierarchy tab of the Design Template dialog box (see Design Template command).
Yes	Indicate the part is a primitive.
No	Indicate the part is nonprimitive and descends in hierarchy.
Graphic	Specify whether Capture displays the normal view or the convert view of the part. The convert view option is only available for parts with convert views.
Packaging	
Parts per Pkg	Indicates the number of parts in the package.
Part	Select a part from the package list.
PCB Footprint	Specify the PCB footprint name, if assigned.
Power Pins Visible	Specify the visibility of the part's power pins.
User Properties	Display the User Properties dialog box so you can modify the part's properties.
Attach Implementation	Display the Attach Implementation dialog box so you can attach a schematic folder to create hierarchy. You must specify the schematic folder's name, but you only need to specify the schematic folder's library or path name if the schematic folder is not in the current project.

Note: Be careful not to create recursion in your design. Capture cannot prevent recursion, and the Design Rules Check command does not report it.

Recursion causes Capture to process infinitely as it tries to expand the design, resulting in the loss of any changes you've made to your design since it was last saved.

Note: Except for occurrence properties, the schematics of externally-referenced libraries and designs should not be edited. You should view them as read-only designs. Trying to edit, then save, these designs from within your schematic can introduce errors such as duplicate reference designators and other problems.

When saving schematics with externally-referenced libraries or designs, occurrence properties are saved but altered instance values are not. If you want to change externally-referenced libraries or designs you should first close the referencing design. Then, open the referenced library or design, make the necessary changes, and save and close the referenced library or design. At this point, you can reopen the original design and reference the modified design.

Note: When you attach a schematic folder to a part or hierarchical block, you can specify a full path and filename in the Library text box. So, although you can specify a library that hasn't been saved, you should not try to descend into the attached schematic folder until the library that contains the schematic folder has been saved.

If you don't specify a full path and filename in the Library text box, Capture expects to find the attached schematic folder in the same design as the part of hierarchical block to which it is attached. If the specified schematic folder doesn't exist in either the design or library, Capture creates the schematic folder when you descend hierarchy on the part or the hierarchical block.

For compatibility with future versions of Windows, Capture preserves the case of the path and filename as you specify them in the Library text box.

Edit Text dialog box

The Edit Text dialog box appears when you choose Properties from the Edit menu when a text object is selected.

Use this control...	To do this...
Text	Change the text to display.
Color	Choose the color of the text. Text that is placed in the part editor uses the part body color.
Rotation	Specify the rotation of the text.
Font	
Change	Display a Font dialog box so you can select a font.
Use Default	Change the font to the default font specified in the Design Template / Design Properties dialog box.

Enter EDIF Netlist Location dialog box

This dialog box opens when you choose the P&R command from the PICFlow menu.

Use this control...	To do this...
Batch Mode	Select this check box to run your vendor place-and-route tool in batch mode.
EDIF Netlist	Specify the path to, and name of the EDIF netlist that resulted from the synthesis operation (using the Synthesize command). This is the netlist that your vendor place-and-route tool targets to a particular vendor device.
Batch File	Specify the path to, and name of the file that contains the commands for running your vendor place-and-route tool in batch mode. Create the batch file using a text editor and ensure that the file has a .BAT extension.

Export Design dialog box

The Export Design dialog box appears when you choose the Export Design command from the File menu.

Use this tab...	To do this...
EDIF	Specify a name for the EDIF file, and the scope of the export.
DXF	Specify a name for the DXF file, and the scope of the export.

EDIF tab

Use this control...	To do this...
Save As	Specify the name of the .EDF file to save the design as. The design is saved as a graphical EDIF file, and not an EDIF netlist. If you want to generate an EDIF netlist, use the EDIF tab in the Create Netlist dialog box, accessible through the Create Netlist command on the Tools menu. Exporting EDIF designs saves the entire design, regardless of which window (project manager or schematic page editor) is currently active.
Configuration File	Specify the name of the configuration file (.CFG) for the translation. Configuration files are not required for translation. For information on configuration files, see Using Capture with OrCAD SDT on page 676 and Electronic Tools Company's *CAP2EDIF (OrCAD Capture to EDIF 2 0 0 Schematic Translator) User's and Reference Manual*.

DXF tab

Use this control...	To do this...
Save As	Specify the name of the .DXF file to save the schematic page as. Capture saves .DXF files in AutoCAD's V12 file format.
Scope	
Entire Design	Export the entire design. Capture appends the schematic name and page name to the name you specified in Save As: `<Save_As><Schematic><Page>.DXF`
Current Page	Export the current page of the design.
Include Border	Check to include the border.
Include Title Block	Check to include the title block.

Note: In order to export a design or schematic to DXF, you must have a schematic page from that design open and selected as the active window. Otherwise, Capture will not allow a DXF export.

Export Properties dialog box

The Export Properties dialog box appears when you choose Export Properties from the Tools menu.

Use this control...	To do this...
Scope	Process the entire design or just the selected documents.
Contents	Export part properties or part and pin properties, or flat net properties.
Mode	Export either instance properties or occurrence properties. Specifies to export either instance properties or occurrence properties. Capture recommends a preferred mode, which you can override.
Export File	Specifies the name of the export output file. For more information about property files, see Editing properties.
Browse	Displays a standard Windows dialog box for selecting files.

Export Selection dialog box

The Export Selection dialog box appears when you choose the Export Selection command from the File menu, when you have objects selected on a schematic page.

Use this control...	To do this...
Export Selection Name	Specify the export name of the selected object or objects.
Library	Specify a path, and a design or library name for the export selection.
Browse	Display a standard Windows dialog box for selecting files.

Export Variant list dialog box

The Export Variant List dialog box appears when you select *Export Variant List* from the Tools menu in the Part Manager.

Use this control...	To do this...
Output File (Variants.lst) Path	Specify the default location for the Variants.lst file. The default location is the Allegro folder in the design directory. You can change this path also.
Config File (Variant.cfg) Path	Specify the default path for the Variant.cfg file. The default path is the same as that of the Capture.exe file. You can change this path also.
Export	Export Variants.lst file containing information about all the variants of the design. The properties listed are the ones specified in the Variant.cfg file.

Find dialog box

The Find dialog box appears when you choose the Find command from the Edit menu.

Note: The available Find dialog box options depend on the active window.

Use this control...	To do this...
Find what	Specify the search string. Use an asterisk (*) to match any string of characters, and a question mark (?) to match any single character.
Find Next	Find the next occurrence of the same search string.
Match case	Specify if the search must match the case of the string. If this option is not selected, lowercase and uppercase letters will be treated the same in the search.
Direction	Specifies the direction of the search—up or down—from the cursor location. This option is only available in the text editor or the property editor.

Scope

Specify the properties to search for. You may specify any of the following scopes in the project manager or schematic page editor:

- Parts
- Nets
- Title Blocks
- Off-page Connectors
- Flat Nets
- Power/GND
- Bookmarks
- Hierarchical Ports
- Text
- DRC Markers
- Parts Pin

You may specify the following scope in the design variant schematic page:

- Variant Parts

For information on how to use the Variant Parts option, see the *OrCAD Capture CIS User Guide*.

This option is not available in the session log or the text editor.

Find and Replace dialog box

The Find and Replace dialog box appears when you choose the Global Replace command from the Edit menu with a schematic page active.

Use this control...	To do this...
Find what	Specify the search string.
Replace with	Specify the string to replace the Find what search string.
Match case	Specify if the search must match the case of the string. If this option is not selected, lowercase and uppercase letters will be treated the same in the search.
Scope	Search the Entire Design or Current Page Only.
Object Type	Specify any combination of net aliases, hierarchical ports, or hierarchical pins by selecting the check boxes.

Font dialog box

The Font dialog box appears when you click the Change button in the Edit Net Alias dialog box, the Place Net Alias dialog box, the Edit Text dialog box, the Place Text dialog box, or the Display Properties dialog box. The font dialog box also appears when you click in a font box on the Fonts tab of the Design Properties dialog box, the Fonts tab of the Design Template / Design Properties dialog box, or the Miscellaneous tab of the Preferences dialog box.

Use this control...	To do this...

Font	Specifies the font for the text. **Note:** Be sure to use a monospaced font (for example, Courier) as the default font for the text editor or the source editor. If you use a true-type font, the editor may distort the appearance of the text, making it difficult to read.
Font Style	Specifies the font style for the text.
Size	Specifies the text size.
Sample	Shows a sample of how the text will appear, based upon the font, style and size.
Script	Specifies the script used for the font.

FPGA Export Dialog Box

The FPGA dialog box appears when you choose Tools Export FPGA with the Project Manager open for a Programmable Logic project.

Use this control...	To do this...
FPGA Family Vendor	Select a FPGA family from the list.
FPGA Component	Select the component you want to export. You can select All to export all the components.
Generate Wrapper File	Generate a wrapper file for the component in Verilog or VHDL
Exclude Power/GND/NC pins	Check to exclude the power, ground, and NC pins from being exported.
Output Reserve Pins	Check this option to display any reserve pin assignments made in the Reserve Pins dialog box in the output file. Any assignment marked as none will not appear in the output file.
Reserve Pins	Open the Reserve Pins dialog. See description of this dialog below.
Generate TCL File	Select to generate the output in the form of a TCL file for Altera and UCF for XILINX.
Net Name V/s Pin Number	Select to generate the TCL file with net names and pin numbers. Enabled for Generate TCL File option.
Pin Names V/S Pin Number	Select to generate the TCL file with pin name and pin number. Enabled for Generate TCL File option.
Generate CSV File	Select to generate the output in the form of a CSV file.
Output Directory	Specify the output file and its location.
View Output	Check to open the generated file

Reserve Pins Dialog Box

The Reserve Pins dialog box appears when you click the Reserve Pins button in the FPGA Export dialog box.

The Global Settings for the Input, Bidirectional and Output type pins ensures that select

Use this control...	To do this...
Input	Select the Input pin type from the drop-down list.
Bidirectional	Select the Bidirectional pin type from the drop-down list.
Output	Select the Output pin type from the drop-down list.
Auto Assign Reserve Pin Assignment	Check this option to make pin assignments as per the Global Settings for the Input, Bidirectional and Output pin types. These assignments will be made in the Pin grid. This can be overwritten for individual pins in the Pins grid.
Reserve Pin Assignment	Select a pin type from the grid cell drop-down for each pin on the FPGA component.

FPGA Options Dialog Box

The FPGA dialog box appears when you click the *FPGA Setup* button in the Generate Part dialog box.

General tab

Use this control...	To do this...

Create single section part	Select to create a part with only one section. This will result in the parts per package property to be set to 1.
Create multi-section part	Select to create a part with more than one section, where pins have separate symbols based on I/O banks specified in pin or pad file. This is suitable for parts with large pin counts. **Note:** When you select this option Split Part Section Input Spreadsheet opens on closing the Generate part dialog box. You can modify the generated part using Split Part Section Input Spreadsheet.
Separate symbols for power/NC pins	Check to specify separate symbols for power or NC pins. This will create Separate symbols for Power/NC pins.
Power/NC Pin limit	Specify the number of Power/NC pins to be in one section. If number of Power/NC pins cross the specified limit, an additional power/NC symbols will be created.
Add Pin-Group to pins	Check to specify auto pin-group information based either on same I/O bank or pins with compatible I/O standard.
Based on same I/O Bank	Check to add pin-group values to pins within the same I/O Bank
Based on same I/O standard	Check to add pin-group values to pins within same I/O Bank with compatible I/O standard. Pins with missing I/O standards are grouped based on same I/O Bank and same pin type.
Add Power/Gnd pins as invisible	Check to ensure if power pins be made visible on the symbol or made invisible.
Rename Duplicate Pins	Check to ensure that pins with duplicate names are renamed during Generate part. The new name is of the format `<original name>_<pin number>`. For example, for a pin named `A` and numbered `2`, the new name will be `A_2`.

Pin Defaults tab

Use this control...	To do this...
Modify pin directions	Check to modify default pin direction and shape. The default pin-direction and shape settings are currently honored by Generate part during import. You can set the direction to Left, Right, Top, or Bottom and the shape to Line, Clock, Dot, Dot-Clock, Line, Short, Short Clock, Short Dot, Short Dot-Clock, Zero length.

Generate Part dialog box

The Generate Part dialog box opens when you choose the Generate Part command from the Tools menu.

Note: To create a pin on a symbol using the Generate Part utility, the pin must have a pin to port mapping in the pin file.

Use this control...	To do this...
Netlist/Source file	Specifies the netlist or schematic file that Capture uses to generate the new symbol. Typically, this is the netlist that is associated with the timing information derived from the vendor fitter tool. You can enter the path and name of the file directly, or use the Browse button to select it.

Netlist/source file type

Specifies the format of the netlist or other source file that Capture uses to generate the symbol. If you select a netlist file name using the Browse button, Capture assigns a default vendor file type based on the netlist file extension. Otherwise, you must select a file type from the drop-down list. You can choose from the following netlist or file types:

- **Actel Pin File.** This file is typically created by the Actel Designer tool.
- **Altera Pin File.** This file is created by the Altera MAX+PLUS II.
- **APD BGA/Die-Text File.** This file is created by the Advanced Package Design tool.
- **Capture Schematic/Design.** A source design or library file from an external file or from the current design. This is automatically set when a schematic folder, which is in a design (.DSN) file or library (.OLB) file, is selected in the project manager at the time the Generate Part dialog box is opened**.**
- **EDIF Netlist.** Altera's MAX+PLUS II tool generates an EDIF netlist. You can also use EDIF files from any other source to generate a symbol.
- **Lattice JEDEC File.** This file is created by Lattice ISP products
- **Lattice Pin File.** This file is created by the Lattice ispExpert tool.

	■ **Lucent ORCA Pad File.** This file is created by the Lucent ORCA tool. ■ **PSpice Model Library.** Used by the PSpice simulator. You can create your own PSpice model libraries using the PSpice Model Editor or use the model libraries that ship with PSpice and install in the Library directory. ■ **Verilog Netlist.** Used for board simulation and for FPGA projects. You can use these netlists to generate a symbol. ■ **VHDL Netlist.** Some vendor tools generate VHDL netlists (with embedded timing information) during place and route. You can use these netlists to generate a symbol.
Netlist/source file type (contd.)	■ **Xilinx M1 Pad File.** This file is created by the Xilinx M1 tool. ■ **Xilinx Pin File.** This file is created by Xilinx place and route tool set. ■ **XNF Netlist**. XNF netlists are the results of the XACTstep place and route tool.
Primitive	Assigns No, Yes, or Default value to the Primitive property. This option is only available for the Capture Schematic/Design source file type. If the value is set to No, you can descend the hierarchy of the placed part instance to see the source schematic.
Copy schematic to library	When this check box is selected, Capture places a copy of the source schematic in the new library created in the Outputs directory of the project manager when a part symbol is generated using a schematic source file. This option is only available for the Capture Schematic/Design source file type. If the part name does not match the source schematic name, the resulting part and schematic will have the same name.

Part name	Specify the name that Capture assigns to the newly generated symbol. If you selected a netlist file name using the Browse button, Capture assigns a default symbol name to this text box that corresponds to the netlist name. Otherwise, you must enter the symbol name directly.
Destination part library	Specifies the name that Capture assigns to the symbol library that will contain the new symbol. If you selected a netlist file name using the Browse button or a schematic file in the project manager, Capture assigns a default symbol library name to this text box that corresponds to the netlist or schematic name and adds a .OLB extension. You can accept the default entry, enter the path and name of the file directly, or use the Browse button to select it.
Create new part	Specifies to create a new part using the specified netlist.
Pick symbols manually (This check box is available only when you have a PSpice project open) (This check box is disabled if the PSpice Model Library item is not selected from the Netlist/source file type drop-down list)	Associate a PSpice model to a Capture symbol. When you click the OK button in the Generate Part dialog box, the Model Import wizard appears allowing you to associate a PSpice model to an existing symbol.
Update pins on existing part in library	Specifies to update the pins on an existing part using the specified netlist, rather than create a new part.
Sort pins	
Ascending order	Specify that the pins are sorted in ascending order.
Descending order	Specify that the pins are sorted in descending order.
Additional pins	

Specify the number of additional pins on part	Check to specify the number of pins Capture creates for the part. By default, Capture creates only the number of pins required such that each input and output specification in the netlist has a unique pin. However, if you are using a particular device, you may want to specify a number of pins that differs from the number of input and output specifications in the netlist.
Number of pins	Specify the number of pins that Capture generates for the part. This option is only available if you have activated the Specify the number of pins on part check box. Any unused pins on the symbol (pins for which there is no input or output specification in the netlist) are considered I/O pins.
Retain alpha-numeric pin-numbers. Device is pin grid array type package.	Check to retain the alphanumeric pin names for the part (for example, "P20"). This is useful for parts that model Xilinx pin grid array type packages. If the Vendor file type in this dialog box is anything other than Xilinx Pin File or Xilinx Pad File, this option is ignored.

Implementation

Implementation type	Specify the type of implementation. The implementation types available to choose from are the same as those available in the Attach Implementation dialog box. The most common Implementation type used with the parts created from PLD vendor pin reports is either <none> or Project (which creates a hierarchy of projects for system simulation). Implementation types signify the following: ■ **<none>** Primitive library part. ■ **EDIF** Non-primitive library part. Contents defined by an EDIF netlist generated by a third party EDA tool. ■ **Project** Primitive library part. Associated with the Simulation Resources of an OrCAD Express project for system-level simulation. ■ **Schematic View** Non-primitive library part. Contents defined by a schematic folder/page. ■ **VHDL** Non-primitive library part. Contents defined by a VHDL model.

Implementation name	Specify the name of the attached object.
Implementation file	Specify the path and name of the library or file of the attached object.
FPGA Setup	Open the FPGA Options dialog box. Using this dialog box, you can specify settings for FPGA symbols, FPGA pins, FPGA pin swapping, and pin shape or pin direction.

Go To dialog box

The Go To dialog box appears when you choose Go To command from the View menu.

Note: The grid reference and bookmark options are unavailable in the part editor.

Location tab

Use this control...	To do this...
X and Y	Specify the X and Y coordinates for the jump.
Absolute and Relative	Specify if the jump is absolute (to the indicated coordinates), or relative (using the coordinates as an offset to the pointer's current position).

Grid Reference tab

Use this control...	To do this...
Horizontal	Specify a horizontal grid reference.
Vertical	Specify a vertical grid reference.

Bookmark tab

Use this control...	To do this...
Name	Specify a jump to a bookmark. Bookmarks are made using the Bookmark command on the Place menu. **Note:** The Go To command is used to go to bookmarks on the currently active schematic page.

Goto Label State dialog box

This dialog box appears when the schematic page editor is active and you choose Label State, Goto from the Edit menu.

Use this control...	To do this...
Enter Label	Specifies the label of the state to which you want to return the schematic.

Go To Line dialog box

This dialog box appears when the text editor is active and you choose Go To from the Edit menu.

Use this control...	To do this...
Line Number	Specifies the line number to view in the text editor window.

Hierarchical PSpice Netlist Settings dialog box

Use this control...	To do this...
Make .PARAM Commands Global	If this option is selected, any PARAM parts in the design become global in scope. If the option is cleared, the PARAM parts are local to the subcircuit in which they occur.
Sub-circuit Patterns	
Products	Specifies which group of settings is active for the netlister. Your choices are PSpice or LVS (Layout versus Schematics) netlist formats. Selecting a different group of settings changes the defaults in the Sub-circuit Patterns frame to reflect the settings of the specified tool.
Global Net Prefix	Defines the syntax of the global net of a subcircuit. The prefix defined here is added to all global net names. For example, if the selected product is PSpice, the prefix “$G_” would be prepended to the “GND” net name, making it “$G_GND”. If you are netlisting a PSpice design, leave the prefix as is. Otherwise the design won’t simulate.
Reference	
Subcircuit Call	Specifies the syntax of the subcircuit call using a modified TEMPLATE syntax.
ParamList Element Definition	Specifies the syntax of how parameters are passed from a reference to a part definition.
Definition	
Subcircuit Header	Specifies the syntax of the subcircuit header using a modified TEMPLATE syntax. If modified, you must make sure the definition header is consistent with the call.
ParamList Element Definition	Specifies the syntax of how parameters are passed from a reference to a part definition.

Param Usage Reference	Specifies the syntax used to enclose the parameters in references.
Subcircuit Ends	Specifies the syntax used for the termination of a subcircuit.
Save as Project Default Settings	Saves the current settings in the CAPTURE.INI file, making the current settings the default settings for any new Capture projects.

For more detailed information about the syntax for these commands, and examples of how to use them, see the *PSpice A/D Reference Guide*.

Import Design dialog box

The Import Design dialog box appears when you choose the Import Design command from the File menu.

PSpice tab

Use this control...	To do this...
Open	Specify the name of the .SCH design file to be translated.
Save As	Specify the name of the .OPJ file for the design to be saved as.
PSPICE.INI File	Specify the path and filename of the PSPICE.INI file.
Translate Hierarchy	Keep the hierarchy of the Schematics design intact, when translating to Capture.
Consolidate all Schematic files into one Design file	If the Translate Hierarchy option is selected, translate the Schematics files into one Capture design file.
Create Simulation Profile for Root Schematic Only	If the Translate Hierarchy option is selected, only create simulation profiles for the root schematic.

EDIF tab

Use this control...	To do this...
Open	Specify the name of the EDIF (*.ED*) file to be translated. The file must be a graphical EDIF design file, and not an EDIF netlist.
Save As	Specify the name of the .DSN file for the design to be saved as.

Configuration File	Specify the name of the configuration file (.CFG) for the translation. Configuration files are not required for translation. For information on configuration files, see Using Capture with OrCAD SDT on page 676 and Electronic Tools Company's *EDIF2CAP (EDIF 2 0 0 to OrCAD Capture Schematic Translator) User's and Reference Manual*.

PDIF tab

Use this control...	To do this...
Open	Specify the name of the design file to be translated.
Save As	Specify the name of the .DSN file for the design to be saved as.

Import Selection dialog box

The Import Selection dialog box appears when you choose the Import Selection command from the File menu.

Use this control...	To do this...
Block	Specify a block to select and view. Use an asterisk (*) to match any string of characters, and a question mark (?) to match any single character.
Block List	Display a list of blocks in the libraries selected in the Libraries list box that match what's entered in the Block text box. When you select a block in this list, its name appears in the Block text box, and its graphic appears in the preview box.
Libraries	Select one or more libraries from the list of available libraries. The Block list displays the blocks from the selected libraries. You also select libraries from the Libraries list box to remove them from the list.
Preview box	Display the graphic of the selected block.
Add Library	Display a standard Windows Open dialog box for adding a library to the Libraries list box. You can add a library in SDT format. If you do, you can save the library in the Capture format (.OLB).
Remove Library	Remove the selected library or libraries from the libraries list box.

Intersheet References dialog box

The Intersheet References dialog box appears when you select:

- Add Intersheet References in the Annotate dialog box, and click OK.

OR

- the Intersheet References option in the Tools menu

Note: Intersheet references are derived from the page number in the title block.

Use this control...	To do this...
Place On Off Page Connectors	Specify if intersheet references are placed on off-page connectors. If this option is not selected, intersheet references won't be placed on off-page connectors.
Position	
Offset Relative to Port	Specify that the positions of intersheet references are relative to their respective ports.
Offset Relative to Port Name	Specify that the positions of intersheet references are relative to their respective port names.
Reset Positions	Specify that existing intersheet references will be reset if their port or port name has moved. If this option is not specified, then existing intersheet references are not moved.
X Offset	Specify the distance between the intersheet reference and either its relative port or port name
Format	
Standard (1, 2, 3)	Specify that all intersheet references listed for a given port. For example, if a signal exists on pages 1,2,3 and 5, then on page 1 the intersheet reference is defined as 2,3,5.

Abbreviated (1..3)	Specify an abbreviated list of intersheet references listed for a given port. For example, if a signal exists on pages 1,2,3,4 and 5, then on page 1 the intersheet reference is defined as 2...5. This indicates all pages from 2 through 5.
Grid(1A5[Zone][Num])	Specify a list of intersheet references by schematic page zone for a given port. For example, if a signal exists on pages 1, 2 and 3. On page 2 the connecting signal exists in the schematic page zone 3D. On page 3 the connecting signal exists in the zone 4C. In this case, the intersheet reference on page 1 is defined as 3D2, 4C3.
Prefix	Specify a prefix that is appended to the front of all intersheet references.
Suffix	Specify a suffix that is appended to the back of all intersheet references.
Port Type Match Matrix	Specify which pin-to-pin pairings that Capture will generate intersheet references for. For example if you select the Input/Output option, then intersheet references will be placed in all cases when an input port on one schematic page connects to an output port on another schematic page.
SelectAll	Selects all the check boxes options in the matrix
DeselectAll	Deselects all the check boxes options in the matrix
Restore Defaults Option	Restores the application default selections in the Port Type Match matrix.
Report File	Specify (or browse for) the name and location of a new CSV file that Capture will use to generate a report of all the intersheet references on the design.
View Output	Specify to view the Report file as soon as the intersheet reference generation is complete.

Layout to PCB Editor dialog box

The Layout to PCB Editor dialog box opens when you choose *Accessories– Layout to PCB Editor translator – Layout to PCB Editor* from OrCAD Capture.

Use this control...	To do this...
Input Layout file (.max)	Specify the layout design (.MAX) file.
Output directory	Specify where you want to store the output files, such as the translated `brd` file and the `log` files.
Overwrite brd and associated files files	Select to overwrite existing files. If you do not select this option, a message will be displayed if files exist.
Update dsn with brd	Select this option to synchronize the design file with the board file that is created after the translation process.
View Log	Select to view the log files. If you select the Update dsn with brd option, the synchronization log will display. If this option is not selected, the translation log will display. You can also view the synchronization log in the Session window.
Translate	Click to start the translation process.

Macro Name dialog box

The Macro Name dialog box appears when you choose the Save As button in the Configure Macro dialog box.

Use this control...	To do this...
Macro Name	Specify the name of the selected macro.
Keyboard Assignment	Specify the keyboard assignment for the selected macro. Keyboard assignments are shown to the right of commands in the Macro menu. If you assign a shortcut to a macro command that is already in use by another command, the shortcut is temporarily assigned to the macro. When you remove the macro from the list of configured macros, the shortcut assignment reverts back to its original menu command. Macros do not require keyboard assignments.
Menu Assignment	Specify the menu name for the selected macro. All macros with menu assignments appear on the Macro menu. Macros do not require menu assignments.
Description	Provide a brief description about the selected macro.

Markers dialog box

The Markers dialog box is available from the Project Manager and the schematic editor. From the Project Manager, choose Marker List from the PSpice menu. From a PSpice schematic page, point to Markers on the PSpice menu and choose List.

Use this control...	To do this...

Markers List	Display or hide markers on your design. Select the check box next to the listed marker to display markers on the schematic. If the check box next to a marker is not selected, it is hidden and will not display in Capture. However, the marker still exists in the profile. This feature is useful for printing a design for documentation.
Go To	If only one marker is selected, click this button to open the schematic page that contains the marker. **Note:** Removing any or all markers from the list removes them from the schematic. You cannot undo the Remove or Remove All operation.
Remove All	Remove all markers from the list and from the design.
Remove	Remove the selected markers from the list and from the design.

Monte Carlo Worst-Case Output File Options dialog box

The Monte Carlo/Worst-Case Output File Options dialog box appears when you select the Monte Carlo/Worst Case option, from the Analysis tab of the Simulation Settings dialog box, and click the More Settings button.

Use this control...	**To do this...**

Find	Find the indicated function on the values of the output variable and reduce these to a single value. The value is the basis for the comparisons between the nominal and subsequent runs. The following functions are available: ■ **YMAX.** Find the absolute value of the greatest difference in each waveform from the nominal run. ■ **MAX.** Find the maximum value of each waveform. ■ **MIN.** Find the minimum value of each waveform. ■ **RISE_EDGE.** Find the first occurrence of the waveform crossing above the threshold value. The waveform must have one or more points at or below the threshold value, followed by one above. The output value listed is the first point that the waveform increases above the threshold value. ■ **FALL_EDGE.** Find the first occurrence of the waveform crossing below the threshold value. The waveform must have one or more points above the threshold value, followed by one below. The output value listed is the first point that the waveform decreases below the threshold value.
Threshold value	Specify the value used in the RISE_EDGE and FALL_EDGE functions.
Evaluate only when the sweep variable is in the range	Specify a beginning and ending range to evaluate the sweep variable in.
List model parameter values in the output file for each turn	List the model parameter values in the output file for each run of the Monte Carlo/Worst Case analysis.

Multi-level Backup Settings dialog box

The Multi-level backup Settings dialog box appears when you choose Autobackup option from the Options menu.

Enter the values for the following fields to determine the duration, number of backups and its storage.

Use this control...	To do this...
Backup time (in minutes)	Enables you to determine the time after which Capture will perform automatic backup.
No of backups to keep	Enables you to determine the total number of backups that will be stored.
Directory for backup	Enables you to determine the storage location for the backup.

Model Import wizard

Associating PSpice model to a Capture part

The Model Import wizard appears when you select the library (.OLB) containing the symbol for which you want PSpice model and choose the Associate PSpice Model command from the Tools menu or right-click the library (.OLB) and select Associate PSpice Model from the pop-up menu.

Select Matching page

Use this control...	To do this...
Select library to pick matching models	Specify the path to the library that contains the PSpice model to be associated with the selected Capture part.
Matching Models	Display a list of PSpice models in the selected model library that can be associated with the Capture symbol.
View Model Text	Display the model definition for the PSpice model currently selected from the Matching Models list.
Symbol pane	Display the name and the graphic for the Capture symbol to which PSpice model is to be attached.
Next	Move to the next step.
Cancel	Select this to cancel the process of associating an existing symbol to a simulation model

Define Pin Mapping page

Use this page for pin to port mapping between the selected symbol shape and the model definition. While you complete the pin-port mapping, you can view the symbol shape in the Symbol pane on the right of the wizard, and the use the View Model Text button to view the model definition.

All the symbol pins must be mapped to a model terminal. After you have mapped each symbol pin to a unique model terminal, if there are any optional model terminals left, you may leave them unmapped.

Use this control...	To do this...
Model Terminal	List the port names from the model definition
Symbol Pin	List the symbol pin names. From the drop-down list, select the pin name that is to be associated with the listed model terminal.
Optional Model Terminals	List the optional ports in the model definition. Depending on the availability of symbol pins, you may or may not map these.
Symbol pane	Display the shape of the symbol selected in the Matching Symbols list.
Back	Move to the previous step, where you selected a matching symbol.
Cancel	Cancel the process of associating an existing symbol to a simulation model.
Save Symbol	Complete the process of associating a symbol to the selected model and to jump back to the Associate/Replace symbol page. **Note:** If you are using Model Import Wizard to associate a PSpice model to a Capture symbol, Finish button is visible instead of the Save Symbol button. Select the Finish button to complete the process of associating the selected PSpice Model to a the Capture symbol and close the wizard
View Model Text	Display the model text for the selected model in a new window.

Associating parts to a PSpice model

Associate/Replace Symbol page

Use this control...	To do this...
Models with symbol	List the PSpice models, for which the Model Import Wizard can find matching symbols, along with the corresponding symbol names.
Models without symbol	List the PSpice models for which matching symbols could not be found.
Associate/Replace Symbols	Select this toggle button when you want to attach an existing symbol to the selected simulation model. Associate Symbol button is available when you select a model from the Models without symbols list. Use the Associate symbol button to associate an existing symbol to a model without symbol. Replace Symbol button is available when the selected model already has a symbol associated to it. Use the Replace symbol button to replace a symbol associated to a model, by an existing symbol of your choice.
Finish	Stop the process of creating symbols. In case you have models that do not have any symbols associated to them, a message box appears, asking you whether rectangular symbols should be attached to these models or not.
View Model Text	Display the model text for the selected model in a new window.

Select Matching page

Use this control...	To do this...
Select a library containing matching symbols	Specify the library that contains the symbol you want to associate the selected model. You can either use the browse button to navigate to the desired OLB file, or select the file from the drop-down list box. The drop-down menu lists a maximum of 10 most recently used libraries.
Matching Symbols	List all the symbols that can be associated with the model selected in Associate/Replace Symbol page. The matching symbols list is generated based on model definition of the selected model by the user.
Symbol pane	Display the graphical shape of the symbol currently selected in the Matching Symbols list.
Next	Move to the next step.
Cancel	Cancel the process of associating an existing symbol to a simulation model.
View Model Text	Display the model text for the selected model in a new window.

Define Pin Mapping page

Use this page for pin to port mapping between the selected symbol shape and the model definition. While you complete the pin-port mapping, you can view the symbol shape in the Symbol pane on the right of the wizard, and the use the View Model Text button to view the model definition.

All the symbol pins must be mapped to a model terminal. After you have mapped each symbol pin to a unique model terminal, if there are any optional model terminals left, you may leave them unmapped.

Use this control...	To do this...
Model Terminal	List the port names from the model definition
Symbol Pin	List the symbol pin names. From the drop-down list, select the pin name that is to be associated with the listed model terminal.
Optional Model Terminals	List the optional ports in the model definition. Depending on the availability of symbol pins, you may or may not map these.
Symbol pane	Display the shape of the symbol selected in the Matching Symbols list.
Back	Move to the previous step, where you selected a matching symbol.
Cancel	Cancel the process of associating an existing symbol to a simulation model.
Save Symbol	Complete the process of associating a symbol to the selected model and to jump back to the Associate/Replace symbol page. **Note:** If you are using Model Import Wizard to associate a PSpice model to a Capture symbol, Finish button is visible instead of the Save Symbol button. Select the Finish button to complete the process of associating the selected PSpice Model to a the Capture symbol and close the wizard
View Model Text	Display the model text for the selected model in a new window.

Push Occ. properties to instance dialog box

This dialog box appears when you choose Transfer Occ. Prop. to Instance, then choose Push Occ. Prop into Instance command from the Accessories menu.

Suppose that you copied a circuit or part of a circuit from design A and pasted it in design B. You might see occurrence and instance level properties with different values on the pasted parts/nets in design B. For example, the reference designators of the occurrences and instances may be different. To avoid confusion in the future you have to ensure that each part has only one reference designator by replacing the instance value of the Part Reference property with the occurrence value of the Part Reference property for each part. You can do this automatically using this dialog box.

To transfer occurrence property values of the Part Reference and PCB footprint properties as instance level property values, select the first radio button and click OK.

To remove all occurrence properties from the design and change the preferred mode of design to instance check the occurrence level properties check box.

To transfer occurrence property values of the flat nets to schematic nets, select the Transfer flat net properties to schematic net properties radio button and click OK.

NC Verilog Simulation dialog box

This dialog box appears when you choose the Board simulation command from the Tools menu, and if you have specified Verilog as the simulation language on the Board Simulation tab of the Preferences dialog box.

Use this option...	To do this...
Use Interactive	Specify that Capture invoke NC Verilog in interactive mode.
Specify Batch File	Specify that Capture invoke NC Verilog in batch mode, using the batch file specified in the associated text box.
Setup	Specify the parameters for the NC Verilog session through the NC Verilog Simulation Setup dialog box
Run	Start the simulation.

NC Verilog Simulation Setup dialog box

This dialog box appears when you click on the Setup button in the NC Verilog Simulation dialog box. This dialog box is organized into a series of tabs that provide a method for setting up various aspects of the simulation session.

Use this tab...	To do this...
Simulation tab (NC Verilog)	Set options for the simulation run.
Testbench tab (NC Verilog)	Specify or create a testbench that provides stimulus for the design.
Model compilation tab (NC Verilog)	Specify simulation files to compile, and options for the compilation.

Simulation tab (NC Verilog)

The Simulation tab of the NC Verilog dialog box provides a method for specifying the simulation options you will use for your simulation session.

Use this control...	To do this...
HDL.VAR file	Specify the path to the HDL.VAR file used by NC Verilog during the simulation. This file is a text file that specifies simulation configuration variables, variables that specify options for compiling, elaborating, and simulating your design, and variables that specify the locations for various support files and invocation scripts.
Log Directory	Specify the directory to which NC Verilog stores the simulation log file.
Compile	Specify that NC Verilog compile the Verilog netlist (and any associated testbench) before simulation. During compilation, NC Verilog checks the netlist for syntax and semantics, and notifies you of any errors. You can specify NC Verilog command line options for the compile in the Cmd Options text box. Enter options exactly as you would from the command line. For example, to use the *Append_log* command line option, in the Cmd Options text box, type: `-Append_log` **Note:** You must compile your design at some point before simulation can occur. This option allows you to skip the compile step in cases where you have compiled your design earlier and do not wish to recompile. If you have not compiled your design, however, and do not select this option, NC Verilog will be unable to simulate your design.

Elaborate	Specify that NC Verilog elaborate the Verilog netlist (and any associated testbench) before simulation. During elaboration, NC Verilog constructs a design hierarchy based on the instantiation and configuration information in the design, establishes signal connectivity, and computes initial values for all objects in the design. You can specify NC Verilog command line options for the elaboration in the Cmd Options text box. Enter options exactly as you would from the command line. For example, to use the *Append_log* command line option, in the Cmd Options text box, type: `-Append_log` **Note:** You must elaborate your design at some point before simulation can occur. This option allows you to skip the elaboration step in cases where you have elaborated your design earlier. If you have not elaborated your design, however, and do not select this option, NC Verilog will be unable to simulate your design. **Note:** Note, also, that you must compile your design (using the Compile option) before you can elaborate it.
Simulate	Start the simulation session. You can specify NC Verilog command line options for the simulation in the Cmd Options text box. Enter options exactly as you would from the command line. For example, to use the *message* command line option, in the Cmd Options text box, type: `-message` **Note:** You can choose not to start the simulation session by deselecting this option. This is useful when you want to compile or elaborate your design without performing the actual simulation.

Start SimVision	Start the NC Verilog SimVision application (which includes waveform displays). **Note:** If you do not select this option, you can still compile, elaborate, or simulate your design (by selecting the corresponding options on the dialog box, but the SimVision application will not be displayed. In this case, when simulation occurs without the waveform display, and the results are reported to a file that you specify as one of the NC Verilog command options.
Enter Interactive Mode	Sets the simulation time for the SimVision session to zero and pauses the simulation to await your input. This option is only available if you choose the Start SimVision option. If, after selecting the SimVision option, you do not select the Enter Interactive Mode option, NC Verilog runs the simulation according to the testbench associated with the design (as specified in the Testbench tab (NC VHDL).)

Note: For specific information on the various NC Verilog commands, as well as the HDL.VAR file, please refer to your NC Verilog documentation.

Testbench tab (NC Verilog)

The Testbench tab of the NC Verilog Simulation dialog box provides a method to specify (or create) a Verilog testbench for your design.

Use this control...	To do this...

Generate Testbench	Create a Verilog testbench template from the top level of your design. The inputs and outputs of the template correspond to the ports and the top level of the design. **Note:** When you generate a testbench in this manner, you must still edit the testbench in order to apply stimuli to the design inputs. In order to edit the testbench, choose the Edit button, which causes Capture to open the testbench in a text editor. You can also open the testbench from the project manager, in which case, the testbench is opened using Capture's Verilog editor.
Include Testbench	Add an existing testbench to your design in order to supply stimuli for the simulation. When you select this option, you must specify the path to the testbench in the Testbench Path field.
None	Specify that there is no existing testbench for the design. Use this option if you want to compile and elaborate your design without simulating.

Note: For specific information on the various NC Verilog commands, please refer to your NC Verilog documentation.

Model compilation tab (NC Verilog)

The NC Verilog Model Compilation tab provides a method for you to specify and compile the simulation models you will use for your board level simulation. This tab is only available for board level simulation. You will not see this tab as an option for FPGA simulation (functional or timing).

Use this control...	**To do this...**

Library extensions	Specify the file extensions of the simulation models to be compiled. Typically, Verilog models have .v or .verilog extensions. You can specify more than one extension by using the "+" symbol. For example:
	`+.v`
	`+.verilog`

Path	Specify the directory in which the simulation models reside.
Verilog Files/Directories	Navigate to the directory containing the simulation models by using the controls in the upper right corner.
Compile location	Specify the directory into which the compiled models will be stored.
Compile at Source	Specify that the compiled models be stored in the same directory as the source files.
Compile	Start the compilation.

NC Verilog Simulation Setup dialog box

This dialog box appears when you click on the Setup button in the NC Verilog Simulation dialog box. This dialog box is organized into a series of tabs that provide a method for setting up various aspects of the simulation session.

Use this tab...	To do this...
Simulation tab (NC Verilog)	Set options for the simulation run.
Testbench tab (NC Verilog)	Specify or create a testbench that provides stimulus for the design.
Model compilation tab (NC Verilog)	Specify simulation files to compile, and options for the compilation.

Simulation tab (NC Verilog)

The Simulation tab of the NC Verilog dialog box provides a method for specifying the simulation options you will use for your simulation session.

Use this control...	To do this...
HDL.VAR file	Specify the path to the HDL.VAR file used by NC Verilog during the simulation. This file is a text file that specifies simulation configuration variables, variables that specify options for compiling, elaborating, and simulating your design, and variables that specify the locations for various support files and invocation scripts.
Log Directory	Specify the directory to which NC Verilog stores the simulation log file.

Compile

Specify that NC Verilog compile the Verilog netlist (and any associated testbench) before simulation. During compilation, NC Verilog checks the netlist for syntax and semantics, and notifies you of any errors.

You can specify NC Verilog command line options for the compile in the Cmd Options text box. Enter options exactly as you would from the command line. For example, to use the *Append_log* command line option, in the Cmd Options text box, type:

```
-Append_log
```

Note: You must compile your design at some point before simulation can occur. This option allows you to skip the compile step in cases where you have compiled your design earlier and do not wish to recompile. If you have not compiled your design, however, and do not select this option, NC Verilog will be unable to simulate your design.

Elaborate	Specify that NC Verilog elaborate the Verilog netlist (and any associated testbench) before simulation. During elaboration, NC Verilog constructs a design hierarchy based on the instantiation and configuration information in the design, establishes signal connectivity, and computes initial values for all objects in the design. You can specify NC Verilog command line options for the elaboration in the Cmd Options text box. Enter options exactly as you would from the command line. For example, to use the *Append_log* command line option, in the Cmd Options text box, type: `-Append_log` **Note:** You must elaborate your design at some point before simulation can occur. This option allows you to skip the elaboration step in cases where you have elaborated your design earlier. If you have not elaborated your design, however, and do not select this option, NC Verilog will be unable to simulate your design. **Note:** Note, also, that you must compile your design (using the Compile option) before you can elaborate it.
Simulate	Start the simulation session. You can specify NC Verilog command line options for the simulation in the Cmd Options text box. Enter options exactly as you would from the command line. For example, to use the *message* command line option, in the Cmd Options text box, type: `-message` **Note:** You can choose not to start the simulation session by deselecting this option. This is useful when you want to compile or elaborate your design without performing the actual simulation.

Start SimVision	Start the NC Verilog SimVision application (which includes waveform displays). **Note:** If you do not select this option, you can still compile, elaborate, or simulate your design (by selecting the corresponding options on the dialog box, but the SimVision application will not be displayed. In this case, when simulation occurs without the waveform display, and the results are reported to a file that you specify as one of the NC Verilog command options.
Enter Interactive Mode	Sets the simulation time for the SimVision session to zero and pauses the simulation to await your input. This option is only available if you choose the Start SimVision option. If, after selecting the SimVision option, you do not select the Enter Interactive Mode option, NC Verilog runs the simulation according to the testbench associated with the design (as specified in the Testbench tab (NC VHDL).)

Note: For specific information on the various NC Verilog commands, as well as the HDL.VAR file, please refer to your NC Verilog documentation.

Testbench tab (NC Verilog)

The Testbench tab of the NC Verilog Simulation dialog box provides a method to specify (or create) a Verilog testbench for your design.

Use this control...	To do this...

Generate Testbench	Create a Verilog testbench template from the top level of your design. The inputs and outputs of the template correspond to the ports and the top level of the design. **Note:** When you generate a testbench in this manner, you must still edit the testbench in order to apply stimuli to the design inputs. In order to edit the testbench, choose the Edit button, which causes Capture to open the testbench in a text editor. You can also open the testbench from the project manager, in which case, the testbench is opened using Capture's Verilog editor.
Include Testbench	Add an existing testbench to your design in order to supply stimuli for the simulation. When you select this option, you must specify the path to the testbench in the Testbench Path field.
None	Specify that there is no existing testbench for the design. Use this option if you want to compile and elaborate your design without simulating.

Note: For specific information on the various NC Verilog commands, please refer to your NC Verilog documentation.

Model compilation tab (NC Verilog)

The NC Verilog Model Compilation tab provides a method for you to specify and compile the simulation models you will use for your board level simulation. This tab is only available for board level simulation. You will not see this tab as an option for FPGA simulation (functional or timing).

Use this control...	**To do this...**

Library extensions	Specify the file extensions of the simulation models to be compiled. Typically, Verilog models have .v or .verilog extensions. You can specify more than one extension by using the "+" symbol. For example:
	`+.v`
	`+.verilog`

Path	Specify the directory in which the simulation models reside.
Verilog Files/Directories	Navigate to the directory containing the simulation models by using the controls in the upper right corner.
Compile location	Specify the directory into which the compiled models will be stored.
Compile at Source	Specify that the compiled models be stored in the same directory as the source files.
Compile	Start the compilation.

NC VHDL Postroute Simulation dialog box

This dialog box appears after you select postroute as the simulation configuration with the Select Simulation Configuration dialog box.

Use this control...	To do this...
Use Interactive	Specify that Capture invoke NC VHDL in interactive mode.
Specify Batch File	Specify that Capture invoke NC VHDL in batch mode, using the batch file specified in the associated text box.
Setup	Display the NC VHDL Postroute Simulation Setup dialog box, from which you can specify the parameters of your simulation.
Run	Start the simulation.

NC VHDL Postroute Simulation Setup dialog box

This dialog box appears when you click on the Setup button in the NCVHDL Preroute Simulation dialog box. This dialog box is organized into a series of tabs that provide a method for setting up various aspects of the simulation session.

Use this tab...	To do this...
Simulation tab (NC VHDL)	Set options for the simulation run.
Testbench tab (NC VHDL)	Specify or create a testbench that provides stimulus for the design.

Simulation tab (NC VHDL)

The Simulation tab of the NC VHDL Preroute or Postroute Simulation Setup dialog box provides a method for specifying the simulation options you will use for your simulation session.

Use this control...	To do this...
HDL.VAR file	Specify the path to the HDL.VAR file used by NC VHDL during the simulation. This file is a text file that specifies simulation configuration variables, variables that specify options for compiling, elaborating, and simulating your design, and variables that specify the locations for various support files and invocation scripts.
Log Directory	Specify the directory to which NC VHDL stores the simulation log file.

Compile

Specify that NC VHDL compile the VHDL netlist (and any associated testbench) before simulation. During compilation, NC VHDL checks the netlist for syntax and semantics, and notifies you of any errors.

You can specify NC VHDL command line options for the compile in the Cmd Options text box. Enter options exactly as you would from the command line. For example, to use the *Append_log* command line option, in the Cmd Options text box, type:

```
-Append_log
```

Note: You must compile your design at some point before simulation can occur. This option allows you to skip the compile step in cases where you have compiled your design earlier and do not wish to recompile. If you have not compiled your design, however, and do not select this option, NC VHDL will be unable to simulate your design.

Elaborate

Specify that NC VHDL elaborate the VHDL netlist (and any associated testbench) before simulation. During elaboration, NC VHDL constructs a design hierarchy based on the instantiation and configuration information in the design, establishes signal connectivity, and computes initial values for all objects in the design.

You can specify NC VHDL command line options for the elaboration in the Cmd Options text box. Enter options exactly as you would from the command line. For example, to use the *Append_log* command line option, in the Cmd Options text box, type:

```
-Append_log
```

Note: You must elaborate your design at some point before simulation can occur. This option allows you to skip the elaboration step in cases where you have elaborated your design earlier. If you have not elaborated your design, however, and do not select this option, NC VHDL will be unable to simulate your design.

Note: Note, also, that you must compile your design (using the Compile option) before you can elaborate it.

Simulate

Specify that NC VHDL start the simulation after the design has been compiled and elaborated.

You can specify NC VHDL command line options for the simulation in the Cmd Options text box. Enter options exactly as you would from the command line. For example, to use the *message* command line option, in the Cmd Options text box, type:

```
-message
```

Note: You can choose not to start the simulation session by deselecting this option. This is useful when you want to compile or elaborate your design without performing the actual simulation.

Start SimVision	Start the NC VHDL SimVision application (which includes waveform displays). **Note:** If you do not select this option, you can still compile, elaborate, or simulate your design (by selecting the corresponding options on the dialog box, but the SimVision application will not be displayed. In this case, when simulation occurs without the waveform display, and the results are reported to a file that you specify as one of the NC VHDL command options.
Enter Interactive Mode	Sets the simulation time for the SimVision session to zero and pauses the simulation to await your input. This option is only available if you choose the Start SimVision option. If, after selecting the SimVision option, you do not select the Enter Interactive Mode option, NC VHDL runs the simulation according to the testbench associated with the design (as specified in the Testbench tab (NC VHDL).)

Note: For specific information on the various NC VHDL commands, as well as the HDL.VAR file, please refer to your NC VHDL documentation.

Testbench tab (NC VHDL)

The Testbench tab of either the NCVHDL Preroute or Postroute Simulation dialog box provides a method to specify (or create) a VHDL testbench for your design.

Use this control...	To do this...

Generate Testbench	Create a VHDL testbench template from the top level of your design. The inputs and outputs of the template correspond to the ports and the top level of the design. **Note:** When you generate a testbench in this manner, you must still edit the testbench in order to apply stimuli to the design inputs. In order to edit the testbench, choose the Edit button, which causes Capture to open the testbench in the text editor. You can also open the testbench from the project manager, in which case, the testbench is opened using Capture's Verilog editor.
Include Testbench	Add an existing testbench to your design in order to supply stimuli for the simulation. When you select this option, you must specify the path to the testbench in the Testbench Path field.
None	Specify that there is no existing testbench for the design. Use this option if you want to compile and elaborate your design without simulating.

Note: For specific information on the various NC VHDL commands, please refer to your NC VHDL documentation.

Model compilation tab (NC VHDL)

The NC VHDL Model Compilation tab provides a method for you to specify and compile the simulation models you will use for your board level simulation. This tab is only available for board level simulation. You will not see this tab as an option for FPGA simulation (functional or timing).

Use this control...	**To do this...**

Library extensions--	Specify the file extensions of the simulation models to be compiled. Typically, VHDL models have .vhd or .vhdl extensions. You can specify more than one extension by using the "+" symbol. For example:
	`+.vhd`
	`+.vhdl`

Path	Specify the directory in which the simulation models reside.
VHDL Files/Directories	Navigate to the directory containing the simulation models by using the controls in the upper right corner.
Compile location	Specify the directory into which the compiled models will be stored.
Compile at Source	Specify that the compiled models be stored in the same directory as the source files.
Compile	Start the compilation.

NC VHDL Preroute Simulation dialog box

This dialog box appears when you choose Preroute on the Select Simulation Configuration dialog box.

Use this option...	To do this...
Use Interactive	Specify that Capture invoke NC VHDL in interactive mode.
Specify Batch File	Specify that Capture invoke NC VHDL in batch mode, using the batch file specified in the associated text box.
Setup	Specify the parameters for the NC VHDL session through the NC VHDL Simulation Setup dialog box.
Run	Start the simulation.

NC VHDL Preroute Simulation Setup dialog box

This dialog box appears when you click on the Setup button in the NC VHDL Simulation dialog box. This dialog box is organized into a series of tabs that provide a method for setting up various aspects of the simulation session.

Use this tab...	To do this...
Simulation tab (NC VHDL)	Set options for the simulation run.
Testbench tab (NC VHDL)	Specify or create a testbench that provides stimulus for the design.
Model compilation tab (NC VHDL)	Specify simulation files to compile, and options for the compilation.

NC VHDL Simulation dialog box

This dialog box appears when you choose the Board simulation command from the Tools menu, and if you have specified VHDL as the simulation language on the Board Simulation tab of the Preferences dialog box.

Use this option...	To do this...
Use Interactive	Specify that Capture invoke NC VHDL in interactive mode.
Specify Batch File	Specify that Capture invoke NC VHDL in batch mode, using the batch file specified in the associated text box.
Setup	Specify the parameters for the NC VHDL session through the NC VHDL Simulation Setup dialog box.
Run	Start the simulation.

NC VHDL Simulation Setup dialog box

This dialog box appears when you click on the Setup button in the NC VHDL Simulation dialog box. This dialog box is organized into a series of tabs that provide a method for setting up various aspects of the simulation session.

Use this tab...	To do this...
Simulation tab (NC VHDL)	Set options for the simulation run.
Testbench tab (NC VHDL)	Specify or create a testbench that provides stimulus for the design.
Model compilation tab (NC VHDL)	Specify simulation files to compile, and options for the compilation.

NC VHDL Library Compilation dialog box

The NC VHDL Library Compilation dialog box appears when you choose the Compile Vendor Libraries command from the Tools menu. This dialog box provides a method for compiling the simulation libraries for the target vendor of your FPGA design.

Use this control...	To do this...
Simulation library	Select the VHDL simulation libraries that correspond to the target technology for your FPGA design.
Run display in session log	Specify that Capture display the commands and results of the compilation in the session log.
CMD path	Specify the path to, and name of, the command file that contains the compilation command settings for the target library.

New Alias dialog box

The New Alias dialog box appears when you click on the New button in the Part Aliases dialog box.

Use this control...	To do this...
Name	Specify the name of the new alias.

New Page in Schematic dialog box

The New Page In Schematic dialog box appears when you choose New Schematic Page from the Design menu, when you have a schematic folder selected in the project manager.

Use this control...	To do this...
Name	Specify the schematic folder or schematic page name.

New Part Creation Spreadsheet

You can use the New Part Creation Spreadsheet to create new parts (multi-section/single section). The New Part Creation Spreadsheet has a spreadsheet-like interface that allows you to paste contents copied from a part data sheet to the spreadsheet.

Each row in the New Part Creation Spreadsheet corresponds to a pin while each column corresponds to properties associated with the pins. The property names are listed as the column header.

Important

The multi-section parts created using the New Part Creation Spreadsheet cannot be split. You can only split either a single-section part or parts already split using the New Part Creation Spreadsheet.

Tip

To sort on any property, double-click its name in the column header.

Tip

You can hide or show a property column in the New Part Creation Spreadsheet. To do this, right-click the property column header you want to hide and select Hide from the pop-up menu. The selected property column will not appear now. To show a property column, right-click the property column header next, on the right-hand side of the hidden property column and select Unhide from the pop-up menu. The hidden property column appears in the New Part Creation Spreadsheet. Alternatively, you can show a property column by:

- Double-clicking the column handle ( ) of the property column header.
- Dragging the column handle of the property column header.

(only the last two methods can be used to show a property column, which is the last column in the New Part Creation Spreadsheet).

Note: You can change the order in which the property columns appear in the New Part Creation Spreadsheet. To do this, select the property column header you want to move and drag and drop it to the location where you want it in the New Part Creation Spreadsheet.

Note: The spreadsheet window is resizable. You can resize the window using the resize cursor you see when you move the mouse pointer to any of the edges of the dialog. You can also use the standard Maximize button on the top right corner of the window.

Use this control...	To do this...
Part Name	Specify a name for the new part.
Part Ref Prefix	Specify a part reference for the new part.
Part Numbering	Specify a numbering format (alphabetic or numeric) that should be added as suffix to the current part reference for the new part. If you select Alphabetic, an alphabet (between A to Z) will be added as a suffix to the current part reference for each of the new part. If you select Numeric, a number (between 1 and 1024) will be added as a suffix to the current part reference for each of the new part. **Note:** The Section property column changes based on your selection in the Part Numbering group. For example, if Alphabetic is selected, the Section property column displays “A”.
No. of Sections	If you want to create a multi-section part, specify the number of sections you want to have in your new part in the No. of Sections text box. The New Part Creation Spreadsheet creates single-section parts, by default. **Note:** If you select alphabetic numbering, then you can create up to a maximum of 26 sections only. If you select numeric numbering, then you can create up to a maximum of 1024 sections.
Number	Specify the pin number.
Name	Specify the name of the pin.

Type	Specify the type of pin. To change a pin type, select the Type cell, and select *Input, Output, Passive, Open Emitter, Open collector, 3 State, Bidirectional,* or *Power*. *Tip* You can select the Type cells for multiple pins simultaneously using the SHIFT+Down Arrow keys and then enter the pin type. The selected Type cells get populated with the pin type of your choice. Alternatively, you can: ❍ Select the Type cells for multiple pins simultaneously using the SHIFT+Left mouse button click, then press the CTRL key, and then select a pin type of your choice from the list box. The selected Type cells get populated with the pin type of your choice. ❍ Click the first cell of the range, and then drag to the last cell, and then enter the pin type of your choice. The selected Type cells get populated with the pin type of your choice. (You can use these methods to make selection in the Shape, Position, and Section property column list boxes also).
Shape	Specify a shape for the pin. To change a pin shape, select the Shape cell, and select *Clock, Dot, Dot-Clock, Line, Short, Short Clock, Short Dot, Short Dot-Clock, Zero length*
PinGroup	Specify a value for each swappable (input) pin of the part.
Position	Specify the pin position as left, right, top or bottom. To change position for a pin, select the Position cell, and select *Left*, *Right*, *Top*, or *Bottom*.
Section	Specify a section number. To change a section for a pin, select the Section cell, and select the required section number from the list.

Tip

You can select Section cells for multiple pins simultaneously using the SHIFT+Down arrow keys and enter the section number. Alternatively, you can:

- Select the Section cells for multiple pins simultaneously using the SHIFT+Left mouse button click, then press the CTRL key, and then select a section number of your choice from the list box. The selected Section cells get populated with the section number of your choice.
- Click the first cell of the range, and then drag to the last cell, and then enter the section number of your choice. The selected Section cells get populated with the section number of your choice.

Tip

You can select alternate Section cells for multiple pins simultaneously using the CTRL+Left mouse button click and enter the section number.

Add Pins	Add new pins at the end of the current row set in the New Part Creation Spreadsheet.
Delete Pins	Delete selected row containing the pin information from the New Part Creation Spreadsheet.

Caution

Once you delete a pin from the New Part Creation Spreadsheet, you cannot retrieve it later.

Save	Save the new part. If any warnings are generated during the save operation, a message box appears asking you whether you want to view the warnings. If you want to view the warnings, click the View Warnings button. The New Part Creation Spreadsheet expands and displays a grid showing warnings messages. If you select the Continue button, the part is saved as is.
Hide Warnings	Hide the warnings messages.
Show Warnings	Show the warnings messages again.

New Part Properties dialog box

The New Part Properties dialog box appears when you choose the New Part command from the Design menu, when you have a library selected in the project manager.

Use this control...	To do this...
Name	Specify the part's name. This is used as the default part value when the part is placed on a schematic page. Part names can be up to 31 characters long.
Part Reference Prefix	Specify the part reference prefix, such as "C" for capacitor or "R" for resistor. For example: C?1(capacitor) R?1 (resistor)
PCB Footprint	Specify the PCB name to be included for this part in the netlist. Contains a value for a device consisting of zero or more pads, other objects, and a name.
Create Convert View	Specify whether the part has a convert. You might use the convert to define a DeMorgan equivalent. A part with this option specified will have two views (a normal and a convert) you can switch between once the part is placed.
Multiple-Part Package	
Parts per Pkg	If there are multiple parts in the package, specify the number of parts in the package.

Package Type	If the part is a package, specify whether all the parts in the package have the same graphical representation (homogeneous) or different graphical representations (heterogeneous). **Note:** The package type can only be set at creation time. These options are not available when you edit the part later. You should not cut and paste parts between homogeneous and heterogeneous packages.
Part Numbering	If the part is a multiple-part package, specify whether parts in the package are identified by letter or number. For example: ■ U?A (alphabetic) ■ U?1 (numeric)
Part Aliases	Display the Part Aliases dialog box to add or remove aliases. Part aliases show up in a library represented by the part symbol with a horizontal line through the center.
Attach Implementation	Display the Attach Implementation dialog box so you can attach a schematic folder to create hierarchy. You must specify the schematic folder's name, but you only need to specify the schematic folder's library or path name if the schematic folder is not in the current project.
Pin Number Visible	Specify whether the pin number (s) for the part should be displayed when you open the part in the Part editor window or view the part in the package view.

Note: Be careful not to create recursion in your design. Capture cannot prevent recursion, and the Design Rules Check command does not report it.

Recursion causes Capture to process infinitely as it tries to expand the design, resulting in the loss of any changes you've made to your design since it was last saved.

Note: If you attach external schematic folders or other files to hierarchical blocks in a design or parts in a library, be sure to include the attachments when you pass the design or library to a board fabrication house or to another engineer. Attached schematic folder and other files are not carried along automatically when you copy or move a part, schematic folder, or schematic page to another library, design, or schematic folder. Only the "pointers" to the attached schematic folder and files—that is, their names and the names of the designs or libraries that contain them—are carried along.

Attached files work much like their counterparts in email—they do not provide an alternative definition of the part (as do attached schematic folders).

Note: When you attach a schematic folder to a part or hierarchical block, you can specify a full path and filename in the Library text box. So, although you can specify a library that hasn't been saved, you should not try to descend into the attached schematic folder until the library that contains the schematic folder has been saved.

If you don't specify a full path and filename in the Library text box, Capture expects to find the attached schematic folder in the same design as the part of hierarchical block to which it is attached. If the specified schematic folder doesn't exist in either the design or library, Capture creates the schematic folder when you descend hierarchy on the part or the hierarchical block.

For compatibility with future versions of Windows, Capture preserves the case of the path and filename as you specify them in the Library text box.

Note: You can access this dialog box after you place a new part. To change the part parameters, change to package view and choose the Package Properties command from the Options menu.

Note: Once you have attached a file and associated a text editor with it, you can use the Descend Hierarchy command to open that file. If you have an attached schematic folder as well as an attached file, Descend Hierarchy opens the schematic folder and not the file.

New Project dialog box

The New Project dialog box appears when you choose New and click Project command from the File menu.

Use this control...	To do this...
Name	Specify the name of the new project.
Create a New Project Using	
Analog or Mixed-Signal Circuit Wizard	Target your project as an analog or mixed-signal design. The Project Wizard will help you configure libraries based for your project.
PC Board Wizard	Target your project as a PCB design. The PCB Wizard will help you configure libraries for your project.
Programmable Logic Wizard	Target your project as a CPLD or FPGA design. The Project Wizard will help you configure libraries based on the vendor you choose to target.
Schematic	Create a project not specifically targeted for PCBs, CPLDs, or FPGAs.
Location	Specify the location of the new project.

Select Project Type dialog box

The Select Project Type dialog box appears when you choose the Change Project Type option on the design pop-up menu in the Project manager.

Use this control...	To do this...
Name	Specify the name of the new project.
Associate Project To	
Analog or Mixed-Signal Circuit Wizard	Target your project as an analog or mixed-signal design.
PC Board Wizard	Target your project as a PCB design.
Programmable Logic Wizard	Target your project as a CPLD or FPGA design.
Schematic	Choose to define the project not specifically targeted for PCBs, CPLDs, or FPGAs.

New Property dialog box

The New Property dialog box appears when you click on the New button in the User Properties dialog box or the New button in the Edit Part Properties dialog box.

Note: Property names and values can have up to 256 characters each.

Use this control...	To do this...
Name	Specify the new property's name.
Value	Specify the new property's value.

New Schematic dialog box

The New Schematic dialog box appears when you choose the New Schematic command from the Design menu, when you have the .DSN file selected in the project manager.

Use this control...	To do this...
Name	Specify the schematic folder or schematic page name.

New Simulation dialog box

The New Simulation dialog box appears when you choose the New Simulation Profile command from the PSpice menu.

Use this control...	To do this...
Name	Specify the name for the new profile. This is not a file name.
Inherit From	Specify a simulation model to inherit properties from. The list box displays all of the simulation models in designs open in Capture.
Root Schematic	Shows selected schematic to act as the root for the simulation profile.

New Symbol Properties dialog box

The New Symbol Properties dialog box appears when you choose the New Symbol command from the Design menu, when you have a library selected in the project manager.

Use this control...	To do this...
Name	Specify the name for the new symbol. **Note:** A Symbol name cannot be more than 31 characters long.
Symbol Type	Select the symbol type. Symbols may be one of the following: ■ Power ■ Off-Page Connector ■ Hierarchical Port ■ Title Block ■ Pin Shape

Open dialog box

The Open dialog box appears when you choose Open from the File menu. Use this command to open projects or files. This is a standard Windows Open dialog box in which you can locate and select the project or file of your choice.

Use this control...	To do this...
Look in	Browse the hierarchical drive and directory structure for your system.
File name	Select or type the name of the project or file.
Files of type	Filter files by extension.

Package Properties dialog box

The Package Properties dialog box appears when you choose the Properties command from the Edit menu while a part is open in package view in the part editor.

Note: You can edit homogeneous sets of the following objects in the spreadsheet editor:

- Bookmarks
- DRC markers
- Hierarchical ports
- Nets
- Off-page connectors
- Parts
- Pins

To select an item in the spreadsheet editor, click on the corresponding row number.

To select a common property of the items in the spreadsheet, click on the column heading that contains the desired property.

To select a single property of one item, click on the cell containing the property.

To edit a single property of one item, double-click on the cell.

Use this control...	To do this...

Update	Update the properties of all the pins in the package. This button is useful if you change a property on one pin, and need to change this property on the same pin in the other parts of the package. For example, say you have a four-part package. Each part in the package has a pin named IN. If you change this pin from a passive pin to an input pin in the A package part, you could use this button to update the type property for the IN pin in the B, C, and D package parts. The Update button updates all pins at once, without requiring that you click OK.
Validate	Check for duplicate pins. For example, suppose you have a pin 1, and then change another pin to pin 1. Using this button would detect the duplicate. This button checks for duplicate pin numbers, without requiring that you click OK.
Copy	Copy the selected cell. The selected cell is copied to the Clipboard, but in a format that cannot be displayed.
Paste	Paste the cell currently in the Clipboard over the selected cell or column to unify or set all properties in a column to the same value.

Part Aliases dialog box

The Part Aliases dialog box appears when you click on the Part Aliases button in the New Part Properties dialog box.

Use this control...	To do this...
Alias Names	Select an alias name from the displayed list.
New	Display the New Alias dialog box to add new aliases.
Delete	Delete the selected alias from the list.

Part Search dialog box

The Part Search dialog box appears when you choose Part Search in the Place Part dialog box.

Use this control...	To do this...
Part Name	Specify the part name to search for. Use an asterisk (*) to match any string of characters, and a question mark (?) to match any single character.
Libraries	Displays the location of all libraries for the part specified in Part Name. After Capture has searched for the part and located it, select the part from one of the libraries and click OK. If the library is configured in the Place Part dialog box, then Capture closes this dialog box, and selects the part in the Place Part dialog box.
Library Path	Specify the path containing libraries for Capture to search through. Set this to your library directory.
Begin Search	Begin searching for the part specified by Part Name, and in the directory specified by Library Path.
Browse	Display a standard Windows dialog box for selecting files.

PCB Project Wizard dialog box

PCB Project Wizard creates your project as a PCB design. The PCB Wizard helps you configure libraries for your project.

To create a PC Board project:

1. Select the Enable project simulation check box if you intend to have simulation capabilities in your PCB design. If you selected Enable project simulation, go to step 2. Otherwise, go to step 3.
2. Select the type of simulation resources you want to include:
   - ❑ Analog or mixed signal
   - ❑ VHDL-based
   - ❑ Verilog-based
3. Click Next.
4. Continue with the steps below that are appropriate for the simulation resource you chose.

Analog or mixed signal simulation:

1. Select a PSpice symbol library you want to include in your project and click the Add button (or double-click the library name). Continue this step until you have chosen all the libraries you want.
2. Click the Finish button.

VHDL-based simulation:

1. Select the PCB part symbol libraries you want to include in your project, and click the Add button.
2. Click the Finish button.

Note: Typically, referenced projects are FPGA projects that you want to include in your PCB project. This is useful for board simulation that includes the appropriate timing and functionality information for an FPGA that is included in your printed circuit board.

Note: Some symbol libraries do not have corresponding simulation models.

Pin Properties dialog box

The Pin Properties dialog box appears when you select a pin in the part editor, and then choose the Properties command from the Edit menu.

Use this control...	To do this...
Name	Specify the pin name. If the name ends with a digit (0--9), each pin is incremented by one every time you place a pin. You can create a pin name with an overbar by adding a backslash (\) after every letter in the pin name.
Number	Specify the pin number. The pin number doesn't need to be a number; it can be alphabetic. If it ends in a number, it is incremented by one after each pin is placed.
Width	Specify whether the pin connects to a bus or a wire. If bus is specified, the pin must connect to a bus; otherwise, it must connect to a wire.
Shape	Select the pin shape from the list of pin shapes.
Type	Select the pin type from the list of pin types.
Pin Visible	Specify the pin visibility on the schematic page. Only power pins can be set to not visible.
User Properties	Display the User Properties dialog box so you can add and edit the pin properties.

Note: Bus pins cannot be used directly as netlisting pins. Their main purpose is to make it possible to use nonprimitive parts more easily by connecting large numbers of signals to a child schematic folder.

Note: You can place one pin on a part that represents all pins for a bus. Such a pin is called a bus pin. Bus pins use the same naming convention as buses.

- You can use bus pins in most cases where you can use scalar pins. For example:
  - Off-page connectors

- Hierarchical ports
- Hierarchical pins of nonprimitive parts and hierarchical blocks

■ Do not use pins in the following situations:

- Hierarchical pins of primitive parts and hierarchical blocks
- Any design that you intend to use with your board layout tool

Place and Route Settings dialog box

The Place and Route Settings dialog box appears when you select Postroute as the simulation configuration for programmable logic projects.

Use this control...	To do this...
Build Netlist Path	Specify the path to the netlist that resulted from the place-and-route of your project using your vendor place-and-route tool.
SDF File Path	Specify the path to the standard delay file that resulted from the place-and-route of your project using your vendor place-and-route tool.

Place Bookmark dialog box

The Place Bookmark dialog box appears when you choose the Bookmark command from the Place menu.

Use this control...	To do this...
Name	Specifies the bookmark's name.

Place Ground dialog box

The Place Ground dialog box appears when you choose the Ground command from the Place menu, or when you choose the Ground tool palette button.

Use this control...	To do this...
Symbol	Specify a symbol to select and view. Use an asterisk (*) to match any string of characters, and a question mark (?) to match any single character.
Symbol List	Displays a list of power symbols and ground symbols in the libraries selected in the Libraries list box that match what's entered in the Symbol text box. When you select an object in this list, its name appears in the Symbol text box, and its graphic appears in the preview box. Select an object from the list of symbols available in the selected libraries.
Libraries	Select one or more libraries from the list of available libraries. The symbol list displays the objects from the selected libraries. You also select libraries from the Libraries list box to remove them from the list. **Note:** The CAPSYM.OLB, which is the default library in Capture now includes the PSpice ground (0) symbol. Use the '0' symbol to place a PSpice ground 0 symbol in your design. If your design does not have a PSpice ground (0) symbol, then the PSpice analog simulation may not run. To place a PSpice ground '0' symbol in your design, see "Placing PSpice ground 0 symbols for PSpice simulations" on page 670.
Preview box	Displays the graphic of the selected object.
Name	Specify the object's name.

Add Library	Display a standard Windows Open dialog box for adding a library to the Libraries list box. You can add a library in SDT format. If you do, you can save the library in the Capture format (.OLB).
Remove Library	Remove the selected library or libraries from the libraries list box.

Place Hierarchical Block dialog box

The Place Hierarchical Block dialog box appears when you choose the Hierarchical Block command from the Place menu, or when you choose the Hierarchical Block tool palette button.

Use this control...	To do this...
Reference	Specify the hierarchical block's name.
Primitive	
Default	Use the default primitive setting, which for hierarchical blocks is nonprimitive. The default setting for hierarchical blocks is set in the Hierarchy tab of the Design Template dialog box (see Design Template command).
Yes	Indicate the hierarchical block is a primitive.
No	Indicate the hierarchical block is nonprimitive and descends in hierarchy.
User Properties	Display the User Properties dialog box so you can modify the hierarchical block's user defined properties.
Implementation	

Implementation Type

Schematic View Indicate that the attached implementation is a schematic folder. Capture automatically generates the appropriate hierarchical pins for the block based on the hierarchical ports.

VHDL Indicate that the attached implementation is a VHDL entity. Capture automatically generates the appropriate hierarchical pins for the hierarchical block based on the port declarations in the VHDL entity.

EDIF Indicate that the attached implementation is an EDIF netlist. If your design includes EDIF implementations for hierarchical blocks, you must specify the hierarchical pins for the block; Capture will not generate them from the EDIF netlist. Also, if your design includes EDIF implementations, you can simulate them, but you cannot compile or build them.

Project Indicate that the attached implementation is a Capture programmable logic project. You must specify the hierarchical pins for the hierarchical block; Capture will not generate them.

PSpice Model Indicate that the attached implementation is a PSpice model file. You must specify the hierarchical pins for the block; Capture will not generate them.

PSpice Stimulus Indicate that the attached implementation is PSpice stimulus file. You must place the hierarchical pins on the block. Capture will not generate them.

Verilog Indicate that the attached implementation is a Verilog model. Capture automatically generates the appropriate hierarchical pins for the hierarchical block based the Verilog model.

Attaching an implementation does not automatically add that file, project, or schematic folder to the project. You must specifically add the implementation to the project with the Project command (Edit menu).

Implementation name	Specify the name of the attached schematic folder, VHDL entity, netlist, or project for the hierarchical block.
Path and filename	Specify the path and filename for the library of the attached object. Use the Browse button to locate the file, or supply both the path and filename. If the attached object is in the same design as the hierarchical block you are placing, leave this option unspecified.

Note: If you attach external schematic folders or other files to hierarchical blocks in a design or parts in a library, be sure to include the attachments when you pass the design or library to a board fabrication house or to another engineer. Attached schematic folder and other files are not carried along automatically when you copy or move a part, schematic folder, or schematic page to another library, design, or schematic folder. Only the "pointers" to the attached schematic folder and files—that is, their names and the names of the designs or libraries that contain them—are carried along.

Attached files work much like their counterparts in email—they do not provide an alternative definition of the part (as do attached schematic folders).

Note: Be careful not to create recursion in your design. Capture cannot prevent recursion, and the Design Rules Check command does not report it.

Recursion causes Capture to process infinitely as it tries to expand the design, resulting in the loss of any changes you've made to your design since it was last saved.

Note: When you attach a schematic folder to a part or hierarchical block, you can specify a full path and filename in the Library text box. So, although you can specify a library that hasn't been saved, you should not try to descend into the attached schematic folder until the library that contains the schematic folder has been saved.

If you don't specify a full path and filename in the Library text box, Capture expects to find the attached schematic folder in the same design as the part of hierarchical block to which it is attached. If the specified schematic folder doesn't exist in either the design or library, Capture creates the schematic folder when you descend hierarchy

on the part or the hierarchical block.

For compatibility with future versions of Windows, Capture preserves the case of the path and filename as you specify them in the Library text box.

Note: Once you have attached a file and associated a text editor with it, you can use the Descend Hierarchy command to open that file. If you have an attached schematic folder as well as an attached file, Descend Hierarchy opens the schematic folder and not the file.

Place Hierarchical Pin dialog box

The Place Hierarchical Pin dialog box appears when you select a hierarchical block, and then either choose the Hierarchical Pin command from the Place menu or choose the Hierarchical Pin tool palette button.

Use this control...	To do this...
Name	Specify the hierarchical pin's name.
Type	Select the pin type from the list of pin types.
Width	Specify if the pin connects to a bus or a wire. If bus is specified, the hierarchical pin must connect to a bus; otherwise, it must connect to a wire.
User Properties	Display the User Properties dialog box so you can edit the pin's properties.

Note: Bus pins cannot be used directly as netlisting pins. Their main purpose is to make it possible to use nonprimitive parts more easily by connecting large numbers of signals to a child schematic folder.

Note: You can place one pin on a part that represents all pins for a bus. Such a pin is called a bus pin. Bus pins use the same naming convention as buses.

Note: You can use bus pins in most cases where you can use scalar pins. For example:

- Off-page connectors
- Hierarchical ports
- Hierarchical pins of nonprimitive parts and hierarchical blocks
- Do not use pins in the following situations:
- Hierarchical pins of primitive parts and hierarchical blocks
- Any design that you intend to use with your board layout tool

Place Hierarchical Port dialog box

The Place Hierarchical Port dialog box appears when you choose the Hierarchical Port command from the Place menu, or when you choose the Hierarchical Port Tool palette button.

Use this control...	To do this...
Symbol	Specify a symbol to select and view. Use an asterisk (*) to match any string of characters, and a question mark (?) to match any single character.
Symbol List	Displays a list of hierarchical ports in the libraries selected in the Libraries list box that match what's entered in the Symbol text box. When you select an object in this list, its name appears in the Symbol text box, and its graphic appears in the preview box. Select an object from the list of symbols available in the selected libraries.
Libraries	Select one or more libraries from the list of available libraries. The symbol list displays the objects from the selected libraries. You also select libraries from the Libraries list box to remove them from the list.
Preview box	Displays the graphic of the selected object.
Name	Specify the object's name.
Add Library	Display a standard Windows Open dialog box for adding a library to the Libraries list box. You can add a library in SDT format. If you do, you can save the library in the Capture format (.OLB).
Remove Library	Remove the selected library or libraries from the libraries list box.
NetGroup Port	Place the hierarchical port as a named NetGroup port. **Note:** Select the NetGroup, to be used, from the drop-down list of NetGroups.

Show UnNamed NetGroup	Place the hierarchical port as an unnamed NetGroup port.

Place IEEE Symbol dialog box

The Place IEEE Symbol dialog box appears when you choose the IEEE Symbol com\mand from the Place menu, or when you choose the IEEE Symbol tool palette button.

Use this control...	To do this...
Symbols	Select a symbol from the list of available symbols.
Preview box	Displays the graphic of the selected symbol.

Place Net Alias dialog box

The Place Net Alias dialog box appears when you choose the Net Alias command from the Place menu or choose the Place net alias button on the tool palette.

Use this control...	To do this...
Alias	Enter the net alias name in the text box.
Color	Specify the color of the net alias.
Rotation	Specify the rotation of the net alias or text.
Font	
Change	Display the Font dialog box so you can select a font.
Use Default	Change the font to the default font specified in the Design Template dialog box.

Place Off-Page Connector dialog box

The Place Off-Page Connector dialog box appears when you choose the Off-Page Connector command from the Place menu, or when you choose the Off-Page Connector tool palette button.

Use this control...	To do this...
Symbol	Specify a symbol to select and view. Use an asterisk (*) to match any string of characters, and a question mark (?) to match any single character.
Symbol List	Displays a list of off-page connectors in the libraries selected in the Libraries list box that match what's entered in the Symbol text box. When you select an object in this list, its name appears in the Symbol text box, and its graphic appears in the preview box. Select an object from the list of symbols available in the selected libraries.
Libraries	Select one or more libraries from the list of available libraries. The symbol list displays the objects from the selected libraries. You also select libraries from the Libraries list box to remove them from the list.
Preview box	Displays the graphic of the selected object.
Name	Specify the object's name.
Add Library	Display a standard Windows Open dialog box for adding a library to the Libraries list box. You can add a library in SDT format. If you do, you can save the library in the Capture format (.OLB).
Remove Library	Remove the selected library or libraries from the libraries list box.
NetGroup Port	Place the off-page connector as a named NetGroup off-page connector. **Note:** Select the NetGroup, to be used, from the drop-down list of NetGroups.

Show UnNamed NetGroup	Place the off-page connector as an unnamed NetGroup off-page connector.

Place Part dialog box

The Place Part dialog box appears when you choose the Part command from the Place menu, or choose the Place Part button on the Draw toolbar.

Place Part

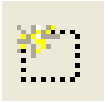
Use this control...	To do this...
Part	Specify the name of the part. Use an asterisk (*) to match any string of characters, and a question mark (?) to match any single character.
Part List	Displays a list of parts in the libraries selected in the Libraries list box that match what's entered in the Part text box. When you select a part in this list, its name appears in the Part text box, and its graphic appears in the preview box. Select a part from the list of parts available in the selected libraries. **Note:** You can filter the part list, using the Filter button described below.
Filter	Display the Specify Part Filter dialog box that allows you to restrict part searches in part libraries based on specific criteria. For example, if you are a PSpice user, you can restrict your part library search such that only parts with associated PSpice simulation models will be listed in the Part List.
Libraries	Select one or more libraries from the list of available libraries. The part list displays the parts from the selected libraries. You also select libraries from the Libraries list box to remove them from the list.

Graphic

Select either Normal or Convert view. All parts have a normal view. Some parts have a convert view that can be used for things such as a DeMorgan equivalent part.

Add Library

Display a standard Windows Open dialog box for adding a library to the Libraries list box. You can add a library in SDT format. If you do, you can save the library in the Capture format (.OLB).



Remove Library

Remove the selected library or libraries from the libraries list box.

Packaging

Parts per Pkg

Displays the number of parts in the package.

Part

Select the part in the package to place on the schematic page.

Type

A package may be either homogeneous or heterogeneous.

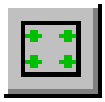
Preview box

Displays the graphic of the selected part.

Application indicator

This feature uses icons to indicate whether the selected part has certain properties. The icon displayed for each property is described below. Note that, in the case of the Implementation Type property, only Implementation Type properties with values of “Schematic View” or “VHDL” are indicated with an icon.

Property: PCB Footprint. **Value**: Various values related to PCB layout.



Property: Implementation Type. **Value**: “Schematic View”

Property: Implementation Type. **Value**: “VHDL”

Property: Implementation Type. **Value**: “Verilog”

Property: PSpice Template. **Value**: PSpice syntax for part netlist entry

This icon is not associated with any property. It indicates that the part is associated with a template-based parameterized PSpice model.

Search Part

The Search for Part section of the Place Part dialog box is viewed if you click the Expand button.

Search For	Enter the part name (you can include wildcard characters) to search through the libraries for a specific part or parts.
Path	Enter the path of the library to search for the part. You can use the Browse button to select the library.
Libraries	Displays a list of libraries in which you searched for parts.
Add	Add libraries from the search library list to the Place Part library list

Place Pin Array dialog box

The Place Pin Array dialog box appears when you choose the Pin Array command from the Place menu, or the Pin Array tool palette button.

Use this control...	To do this...
Starting Name	Specify the name for the pin array. If the name ends with a digit (0--9), each pin in the array is incremented by the value specified in the Increment text box. You can create a pin name with an overbar by adding a backslash (\) after every letter in the pin name.
Starting Number	Specify the starting number for the pin array. Pin numbers don't need to be numbers. If a pin number ends in a number, it is incremented by the value specified in the Increment text box.
Number of Pins	Specify the number of pins in the pin array.
Increment	Specify the increment between pin numbers for the pin array.
Pin Spacing	Specify the spacing between pins for the pin array.
Shape	Select the pin shape from the list of pin shapes.
Type	Select the pin type from the list of pin types.
Pins Visible	Specify the pin visibility on the schematic page. Only power pins can be set to not visible.

Place Pin dialog box

The Place Pin dialog box appears when you choose Pin from the Place menu, or the Place Pin tool palette button.

Use this control...	To do this...
Name	Specify the pin name. If the name ends with a digit (0--9), each pin is incremented by one every time you place a pin. You can create a pin name with an overbar by adding a backslash (\) after every letter in the pin name.
Number	Specify the pin number. The pin number doesn't need to be a number; it can be alphabetic. If it ends in a number, it is incremented by one after each pin is placed.
Width	Specify whether the pin connects to a bus or a wire. If bus is specified, the pin must connect to a bus; otherwise, it must connect to a wire.
Shape	Select the pin shape from the list of pin shapes.
Type	Select the pin type from the list of pin types.
Pin Visible	Specify the pin visibility on the schematic page. Only power pins can be set to not visible.
User Properties	Display the User Properties dialog box so you can add and edit the pin's properties.

Note: Bus pins cannot be used directly as netlisting pins. Their main purpose is to make it possible to use nonprimitive parts more easily by connecting large numbers of signals to a child schematic folder.

Note: You can place one pin on a part that represents all pins for a bus. Such a pin is called a bus pin. Bus pins use the same naming convention as buses.

You can use bus pins in most cases where you can use scalar pins. For example:

- Off-page connectors
- Hierarchical ports

- Hierarchical pins of nonprimitive parts and hierarchical blocks

Do not use pins in the following situations:

- Hierarchical pins of primitive parts and hierarchical blocks
- Any design that you intend to use with your board layout tool

Place Power dialog box

The Place Power dialog box appears when you choose the Power command from the Place menu, or when you choose the Power tool palette button.

Use this control...	To do this...
Symbol	Specify a symbol to select and view. Use an asterisk (*) to match any string of characters, and a question mark (?) to match any single character.
Symbol List	Displays a list of power symbols and ground symbols in the libraries selected in the Libraries list box that match what's entered in the Symbol text box. When you select an object in this list, its name appears in the Symbol text box, and its graphic appears in the preview box. Select an object from the list of symbols available in the selected libraries.
Libraries	Select one or more libraries from the list of available libraries. The symbol list displays the objects from the selected libraries. You also select libraries from the Libraries list box to remove them from the list.
Preview box	Displays the graphic of the selected object.
Name	Specify the object's name.
Add Library	Display a standard Windows Open dialog box for adding a library to the Libraries list box. You can add a library in SDT format. If you do, you can save the library in the Capture format (.OLB).
Remove Library	Remove the selected library or libraries from the libraries list box.

Place Text dialog box

The Place Text dialog box appears when you choose the Text command from the Place menu, or when you choose the Text tool palette button.

Use this control...	To do this...
Text	Enter the text in the text box.
Color	Specify the color of the text. Text that is placed in the part editor uses the part body color.
Rotation	Specify the rotation of the text.
Font	
Change	Display a Font dialog box so you can select a font.
Use Default	Change the font to the default font specified in the Design Template dialog box.

Place Title Block dialog box

The Place Title Block dialog box appears when you choose the Title Block command from the Place menu.

Use this control...	To do this...
Symbol	Specify a symbol to select and view. Use an asterisk (*) to match any string of characters, and a question mark (?) to match any single character.
Symbol List	Displays a list of title blocks in the libraries selected in the Libraries list box that match what's entered in the Symbol text box. When you select an object in this list, its name appears in the Symbol text box, and its graphic appears in the preview box. Select an object from the list of symbols available in the selected libraries.
Libraries	Select one or more libraries from the list of available libraries. The symbol list displays the objects from the selected libraries. You also select libraries from the Libraries list box to remove them from the list.
Preview box	Displays the graphic of the selected object.
Name	Specify the object's name.
Add Library	Display a standard Windows Open dialog box for adding a library to the Libraries list box. You can add a library in SDT format. If you do, you can save the library in the Capture format (.OLB).
Remove Library	Remove the selected library or libraries from the libraries list box.

Preferences dialog box

The Preferences dialog box appears when you choose the Preferences command from the Options menu in Capture.

Use this tab...	To do this...
Colors/Print	Define the default color of objects such as aliases, wires, design variants, part not present, and pins. A standard Windows default Color dialog box appears when you click on the color of an item. The check boxes next to the objects control whether the objects will be printed or plotted. If an object's box is selected, the object can be printed or plotted. Objects always appear on your screen, regardless of the setting of their check boxes. The Use Defaults button resets colors to the default colors shipped with Capture. **Note:** The border and grid references of schematic pages use the color specified for title blocks.
Grid Display	Control the behavior and appearance of the grid display for both the schematic page editor and the part editor. See Grid Display tab for more information.
Pan And Zoom	Set auto scrolling options and zoom factor for both the schematic page editor and the part editor. See Pan and Zoom tab for more information.
Select	Specify selection options, change the maximum number of objects you can drag, and set tool palette visibility for both the schematic page editor and the part editor. For more information, see Select tab

Miscellaneous	Specify the fill style, line style, and line width for both the schematic page editor and the part editor. Also specify the line color for the schematic page editor. You can also define the session log font, set text rendering, set auto recovery intervals, and enable intertool communication. For more information, see Miscellaneous tab.
Text Editor	Specify font and color information for the text editor. Also specify tab setting in terms of character spacing, and highlighting options. For more information, see Text Editor tab.
Board Simulation	Specify the hardware development language to be used during board level simulation. For more information, see Board Simulation tab.

Color tab

The Color dialog box appears when you click on a color in the Colors tab in the Preferences dialog box

Use this control...	To do this...
Basic colors	Shows the color of the object selected in the Colors tab. To change the color, click the left mouse button on a different color and then click OK.
Custom colors	This feature is disabled in Capture.
Define Custom Colors	This feature is disabled in Capture.

Grid Display tab

The Preferences dialog box appears when you choose the Preferences command from the Options menu in Capture.

Use these options to specify the appearance of the grid for your working area. You use this dialog box to set grid properties for both the schematic page grid and the part and symbol grid.

Use this control...	To do this...
Visible	Specify whether the schematic page or part's grid is visible or hidden on the screen.
Grid Style	Specify whether the grid appears as grid dots or lines in the editor.
Grid spacing	Specify the grid spacing on the schematic page as a fraction of pin-to-pin spacing. For example, a setting of 1/2 specifies that the grid spacing on the schematic page is set to exactly half the specified pin-to-pin spacing.
Pointer snap to grid	Specify whether the pointer snaps to the grid in the editor. This check box is selected by default.
Fine *(only for schematic page editor)*	Specify whether connectivity (part, bus) and drawing objects, like Line, Polyline, Text, Rectangle, Ellipse, Arc, and Picture can be placed and moved on the fine grid. For description of various scenarios for this option, see Customizing placement and movement of objects on the schematic. **Note:** This setting is saved in the CAPTURE.INI file and it is used whenever you start the next Capture session.
Coarse *(only for schematic page editor)*	Specify whether connectivity and drawing objects can be placed and moved on the coarse grid. For description of various scenarios for this option, see Customizing placement and movement of objects on the schematic. **Note:** This setting is saved in the CAPTURE.INI file and it is used whenever you start the next Capture session.

Master *(only for schematic page editor)*	Specify whether connectivity and drawing objects can be placed and moved on the coarse grid, if *Pointer snap to grid* checkbox is selected. This setting is equivalent to the Snap To grid toolbar state . Specify whether connectivity and drawing objects can be placed and moved on the fine grid, if *Pointer snap to grid* checkbox is not selected. This setting is equivalent to the Snap To grid toolbar state . For description of various scenarios for this option, see Customizing placement and movement of objects on the schematic. **Note:** This setting is saved in the CAPTURE.INI file and it is used whenever you start the next Capture session.

Note: Ensure that the *Pointer snap to grid* check box is selected and the Connectivity Elements is set to Coarse while placing connectivity objects. Otherwise, your part pins may be placed on the fine grid, making it difficult to connect them properly.

Note: When you place a part on fine grid, it remains on fine grid through any cut-and-paste and drag-and-drop operations.

Miscellaneous tab

The Preferences dialog box appears when you choose the Preferences command from the Options menu in Capture.

Use these options to specify miscellaneous options in Capture.

Use this control...	To do this...
Fill Style	Specify a fill pattern for rectangles, ellipses, and polygons.
Line Style	Specify line style for lines, polylines, rectangles, ellipses, and arcs.

Line Width	Specify line width for lines, polylines, rectangles, ellipses, and arcs.
Color	Specify the color of lines, rectangles, and ellipses. Polylines and arcs use the default color of objects set in the Colors tab. This option only applies to lines, rectangles, and ellipses in the schematic page editor. This color is not the default color, but can be set to use the default color. Objects placed while this option is not set to the default color, won't use the default color. Changing this option won't change the color of objects already placed in the schematic page editor.

Note: You can change the fill style, line and width style, and color on individual objects using the Properties command on the Edit menu.

Junction Dot Size	Specify the dot size as Small, Medium, Large, and Very Large. This will increase or decrease the size of the dots created when a wire is connected to another wire.
Project Manager and Session Log	Specify the font for the session log. If you click on this box, a standard Windows Font dialog box for font selection appears. This option is neither a schematic page nor a part editor option.

Text Rendering

Render TrueType fonts with strokes	Specify that text appears as a series of lines, connected to resemble the outlines of the corresponding TrueType letters or numbers they represent.
Fill text	Specify that text outlines be filled in.

Auto Recovery

Enable Autorecover	Enable or disable auto recovery. If the option is checked, then auto recovery is enabled.
Update every N minutes	Specify the time interval in minutes (where N is the number of minutes) after which Capture performs an auto-save.

Note: Auto recovery is not an automatic saving feature. If you intentionally exit Capture without first saving your changes, they will be lost. Autorecovered files are automatically deleted when you exit Capture normally.

Auto Reference

Automatically reference placed parts	Enable automatic part referencing. When a part is placed on the schematic page, the next available reference designator will automatically be assigned. Disabled, parts placed on the schematic will be assigned the reference designator found in the library. For example: U?A or JP?. This is the default selection.

Note: The Auto Reference feature should be used to provide unique part references for simulation, and is not intended to replace the packaging process for a PCB design. For packaging you should Annotate your design.

Preserve reference on copy	Enable part references to be preserved while pasting a part to a schematic page. When you copy a part and paste it on a schematic page, the part will retain the same reference designator as that of the copied part. But, if you place a new part on a schematic page, Capture will assign the reference designator found in the library. For example: U?A or J?P. **Note:** This option is not supported for complex hierarchical designs.

Note: You can select only one option at a time.

Depending on the check box selection state, the following scenarios are possible:

- If both the check boxes are disabled:
  - the new part that you place on a schematic page will not be annotated.
  - the part references of the copied part will not be preserved while pasting that part on a schematic page.

- If the Automatically reference placed parts check box is enabled:
  - the new parts that you place on a schematic page will be annotated.
  - the part references of the copied part will not be preserved while pasting that part on a schematic page, rather they will be incremented.
- If the Preserve reference on copy check box is enabled:
  - the new part that you place on a schematic page will not be annotated.
  - the part references of the copied part will preserved while pasting that part on a schematic page.

Intertool Communication

Enable intertool communication	Enable intertool communication with other OrCAD products such as Simulate or Layout. For more information about intertool communication, see Intertool communication. This option is not specific to either the schematic page editor or the part editor.

Wire Drag

Allow component move with connectivity changes	If this check box is selected or the toolbar button is in the state, then Capture allows you to drag and place the selected part or wire on the schematic, even if it results in connectivity changes. Also, Capture flags a warning with a changed cursor and will show the temporary markers. If the check box is not selected or the toolbar button is in the state, then the selected part or wire attaches to the cursor and does not get placed on the schematic, if it results in connectivity changes. Also, Capture flags only a warning with a changed cursor and does not show the temporary markers.

Docking

Docking Place Part	If this option is checked, the dockable Place Part dialog is invoked when you select the Place Part command. Unchecking this option will ensure that the modal Place Part dialog displays. **Note:** You need to restart Capture to make changes to this option effective.
Find	
Search Toolbar	Checking this option ensures that the Search toolbar is displayed when you use the Tools - Find command. Unchecking the option ensure the modal Find dialog is invoked when you use the Tools - Find command.
IREF Display Property	
Global Visibility	Checking this option ensures that the intersheet references are visible. Unchecking this option will hide the intersheet references. **Note:** If you un-check this option (to hide the intersheet references in a design), and then run the Intersheet References command, the intersheet references will be displayed on the relavant pages of the design. If you then open the Miscellaneous tab, notice the the Global Visibility option is checked.

Pan and Zoom tab

The Preferences dialog box appears when you choose the Preferences command from the Options menu in Capture.

Use these options to specify panning and zooming factors. Set them separately for the schematic page editor, and the part and symbol editor.

Use this control...	To do this...
Zoom Factor	Specifies the zoom factor for the editor.

Auto Scroll Percent	Specifies how much of the schematic page or part scrolls across the screen when the pointer drags a selected object into the border area of the editor.

Select tab

The Preferences dialog box appears when you choose the Preferences command from the Options menu in Capture.

Use these options to specify selection factors.

Use this control...	To do this...
Area Select	Specify whether objects are selected when the selection area border intersects them, or only when they are completely enclosed in the selection area. **Note:** If the Fully Enclosed option is selected and you select an object on a schematic page, make sure that you select the object along with its name and number. Otherwise, the object does not get selected.
Maximum number of objects to display at high resolution while dragging	Specify the maximum number of objects that are visible at high resolution while performing a drag-and-drop operation. When you drag a number of objects greater than this value, a rectangular placeholder appears in lieu of the selected objects.
Show Palette	Specifies whether the tool palette is visible or hidden.

Text Editor tab

The Preferences dialog box appears when you choose the Preferences command from the Options menu in Capture.

Use this control...	To do this...
Syntax Highlighting	Displays the current colors for VHDL and Verilog keywords, comments, and quoted strings. Select one of the color buttons to display the standard Windows Color dialog box. In the Color dialog box, you can change the color of the selected language element.
Current Font Setting	Displays the current settings of the font item selected in the Set Font For option. The settings displayed are the font, font size, style, effects, and color.
Set	Display the standard Windows Font dialog box for setting font options. The settings apply to the selected font item only.

Note: Be sure to use a monospaced font (for example, Courier) as the default font for the text editor or the source editor. If you use a true-type font, the editor may distort the appearance of the text, making it difficult to read.

Tab Setting	Specify the spacing between tabs in terms of character spaces for the text editor. The range is limited to 1-100. This tab setting is stored in the CAPTURE.INI file. Capture will ignore existing CAPTURE.INI files that specify the tab setting in inches and will reset spacing to a default of four character spaces.
Highlight Keywords, Comments, and Quoted Strings	Specify that Capture highlight all VHDL or Verilog keywords, comments, and quoted strings in the active file.
Show line numbers	Specify that the text editor display line numbers in text files

Save text files on deactivate	Specify that any open text files are saved in their current state whenever the text editor window loses focus
Auto reload text files	Specify that the text editor reload text files automatically when there is a more recent version of the file as a result of a Capture operation (such as netlist generation).
Save text files before running tools	Specify that the text editor save any open text files before running any Capture tools (such as design rules check or netlist generation).
Reset	Reset all the tab options to Capture's default values.

Board Simulation tab

The Preferences dialog box appears when you choose the Preferences command from the Options menu in Capture.

Use these options to specify the hardware development language used for board simulation.

Use this control...	To do this...
VHDL	Specify that Capture use VHDL for the board simulation netlist and testbench.
Verilog	Specify that Capture use Verilog for the board simulation netlist and testbench.

Print dialog box

The Print dialog box appears when you choose the Print command from the File menu. Click the Setup button to go to the Print Setup dialog box and check settings before you print. All settings you choose (except the number of copies) are saved to CAPTURE.INI and will become the default when you restart Capture.

Use this control...	To do this...
Printer	Displays the active printer and printer connection.
Scale	Specify the scaling factor to print by, or let Capture automatically scale to the specification. ■ Scaling to paper size - Forces Capture to scale the printing job to the page size specified in the Page Size tab in the Schematic Page Properties dialog box. Use the Page Size tab in the Design Template dialog box on the Options menu to reset the Custom page size. ■ Scale to page size - Forces Capture to scale the printing job to the page size specified by the Page size option in the Print dialog box. ■ Scale - Specifies the scaling factor to print by, or lets Capture automatically scale to the specified scale.
Page size	If Scale to page size is selected, select the page size to which the image will be scaled. Choose one of the standard page sizes, or Custom. These sizes are defined in the Schematic Page Properties dialog box, in the Page Size tab.

Print offsets

Specifies horizontal and vertical printing offsets in inches or millimeters (mm) depending on the setting you've chose in the Design Template dialog box. Capture centers the page horizontally and vertically when both check boxes are selected.

Your entire schematic page will be output to the printing or plotting device, regardless of the use of offsets. The following rules define the number of output pages that will be printed or plotted:

- The device and its driver determine the dimensions of the printed page area.
- The number of pages is calculated from the physical dimensions of the schematic page and the driver-provided area dimensions.
- A positive offset shifts the entire schematic page to the right in the X direction, and down in the Y direction. Additional pages are output as necessary so the entire schematic is printed. There is no truncation.
- A negative offset shifts the schematic page left, and up. The effect of a negative offset is to start the drawing on a "previous" page. Previous pages are "prepended" so drawing can start at the starting portion of the schematic. There is no truncation.
- Only the number of pages required to print or plot the schematic page will be printed. Extra, blank pages are omitted.

Print option

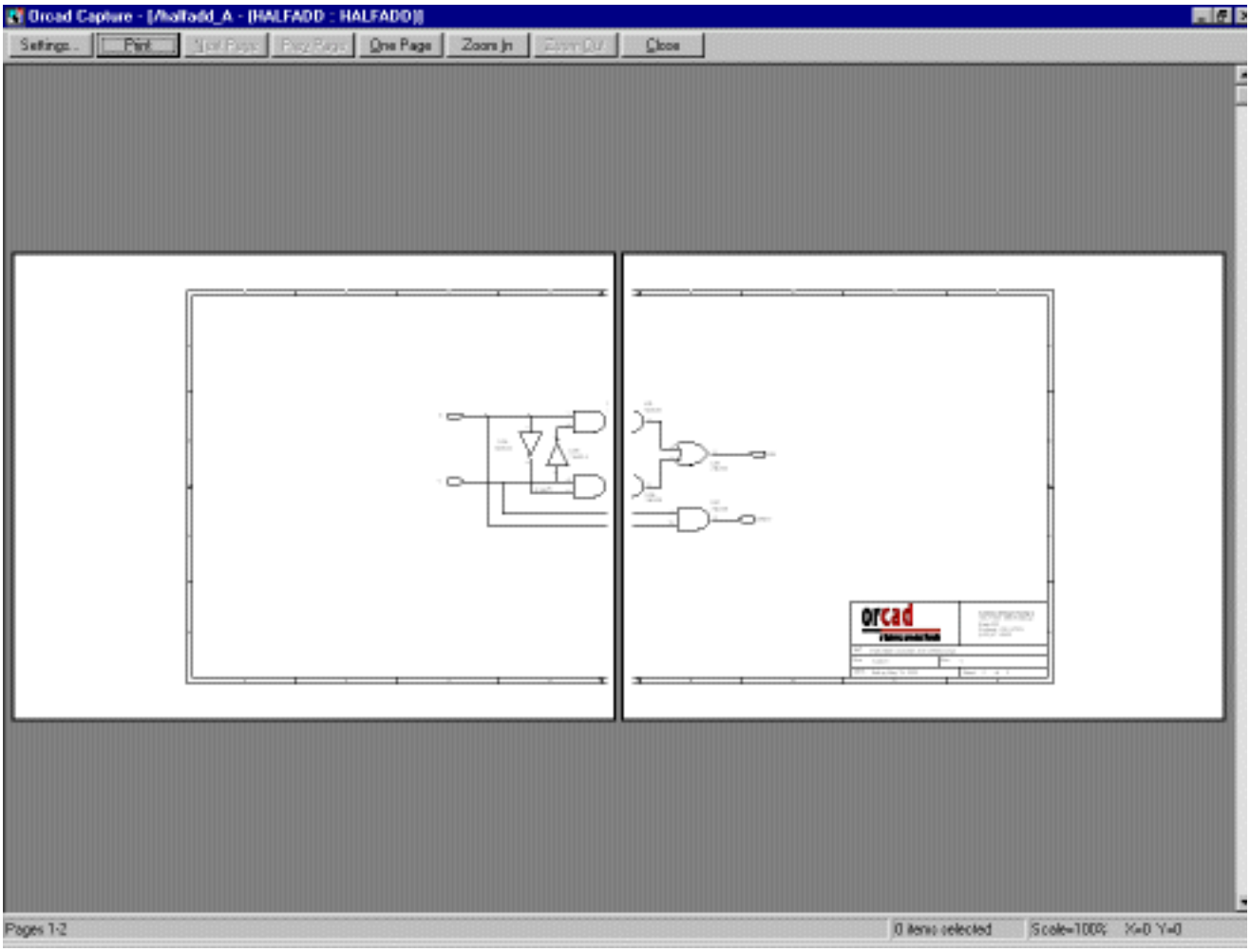
Specify whether you want to print instances or occurrences of a page.

- Inst. Mode (Instance mode) - Enables you to print only the instances of a page in a schematic. This option is selected by default.
- Occ. Mode (Occurrence mode) - Enables you to print multiple occurrences of a page in a schematic.

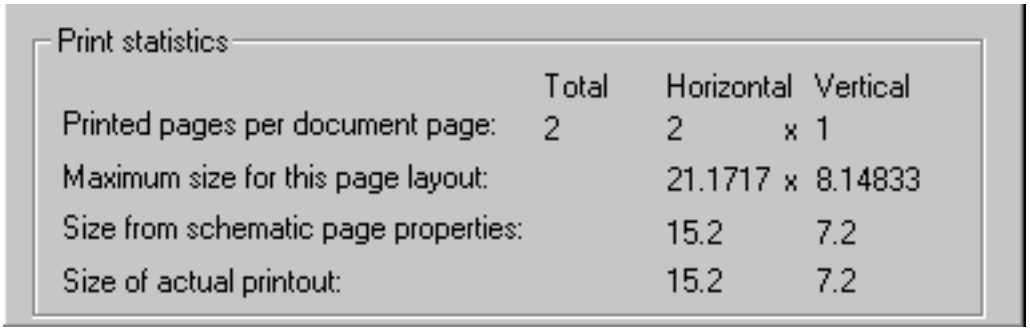
Print quality	Specify the resolution of the print. Choose a setting from the drop-down list.
Copies	Specify the number of copies to print.
Print to file	Print the object to a file. If you select this option, the Print to File dialog box appears after you click OK.
Print all colors in black	Causes difficult-to-read colors to print in black.
Collate copies	Print copies organized in order of page numbers
Print area	When a specific print area is set for the schematic page and this option is selected, the print output is the print area of the schematic page. Clear this check box to print the entire schematic page. When Print area is selected, all print options except Print quality, Copies, Print to file, and Print all colors in black are unavailable. Output of selected print area is zoomed in and centered.
Include pages outside hierarchy	Specifies to also print pages in the design that are not included in the root hierarchy. If you do not select this option, only those files included in the root hierarchy will print.
Include referenced pages in other libraries or designs	Specifies to also print pages outside of the design that the root hierarchy references. If you do not select this option, only the files in the design's root hierarchy will print.

Print statistics	■ Printed pages per document page - Specifies the number of horizontal and vertical pages needed to print a document. If a schematic page (document page) takes more than one page to print out, Capture reports the total number of pages under the Total column heading. Horizontal and Vertical refers to the pages that will make up the printed schematic page. For example, a schematic page may take four pages to print, so the Total is 4. Depending on physical shape of the design, the Horizontal may be 2 and the Vertical may be 2 (2 x 2), or the Horizontal may be 4 and the Vertical may be 1 (4 x 1). ■ Maximum page size for selected printer - These dimensions identify the printable page area of the printer and are dependent on the printer and paper size. ■ Size from schematic page properties - Specifies the dimensions of the page size selected on the Page Size tab of the Schematic Page Properties dialog box. ■ Size of actual printout - Specifies the scaled document size as it changes with different settings in the Scale options or when you change the page orientation in the Print Setup dialog box. The Maximum size for the page layout, Size from schematic page properties, and Size of actual printout dimensions are shown in inches or millimeters, depending on the setting you've chose in the Design Template dialog box.
Setup	Display a standard Windows dialog box to set printer or plotter configuration.

The Print statistics section of the Print and Print Preview dialog boxes reports the number of horizontal and vertical pages it takes to print out the selected document. If the schematic page you want to print takes a two-page layout as shown here:



You would see this in the Printed pages per document page statistics:



Note: When printing a multi-page schematic, make sure that the pages do not have multiple Title Blocks with different page numbers. Otherwise, the pages will not be printed in the correct order. If you change the page numbers in the Title Blocks manually, then make sure that the Do not change the page number check box is checked in the Annotate dialog box.

Print Preview and Print Setup dialog boxes

The Print Preview dialog box displays when you choose the Print Preview command from the File menu. Click the Setup button to go to the Print Setup dialog box before you print.

All settings you choose (except the number of copies) are saved to CAPTURE.INI and will become the default when you restart Capture.

Use this control...	To do this...
Printer	Displays the active printer and printer connection.
Scale	Specify the scaling factor to print by, or let Capture automatically scale to the specification. ■ Scaling to paper size - Forces Capture to scale the printing job to the page size specified in the Page Size tab in the Schematic Page Properties dialog box. Use the Page Size tab in the Design Template dialog box on the Options menu to reset the Custom page size. ■ Scale to page size - Forces Capture to scale the printing job to the page size specified by the Page size option in the Print dialog box. ■ Scale - Specifies the scaling factor to print by, or lets Capture automatically scale to the specified scale.
Page size	If Scale to page size is selected, select the page size to which the image will be scaled. Choose one of the standard page sizes, or Custom. These sizes are defined in the Schematic Page Properties dialog box, in the Page Size tab.

Print offsets	Specifies horizontal and vertical printing offsets in inches or millimeters (mm) depending on the setting you've chose in the Design Template dialog box. Capture centers the page horizontally and vertically when both check boxes are selected. Your entire schematic page will be output to the printing or plotting device, regardless of the use of offsets. The following rules define the number of output pages that will be printed or plotted: ■ The device and its driver determine the dimensions of the printed page area. ■ The number of pages is calculated from the physical dimensions of the schematic page and the driver-provided area dimensions. ■ A positive offset shifts the entire schematic page to the right in the X direction, and down in the Y direction. Additional pages are output as necessary so the entire schematic is printed. There is no truncation. ■ A negative offset shifts the schematic page left, and up. The effect of a negative offset is to start the drawing on a "previous" page. Previous pages are "prepended" so drawing can start at the starting portion of the schematic. There is no truncation. ■ Only the number of pages required to print or plot the schematic page will be printed. Extra, blank pages are omitted.
Print option	Specify whether you want to print instances or occurrences of a page. ■ Inst. Mode (Instance mode) - Enables you to print only the instances of a page in a schematic. This is the default option. ■ Occ. Mode (Occurrence mode) - Enables you to print multiple occurrences of a page in a schematic.
Print quality	Specify the resolution of the print. Choose a setting from the drop-down list.
Copies	Specify the number of copies to print.

Print to file	This option is not available in Print Preview. If you want to print to file, use the Print dialog box.
Print all colors in black	Causes difficult-to-read colors to print in black.
Collate copies	Print copies organized in order of page numbers
Print area	When a specific print area is set for the schematic page and this option is selected, the print output is the print area of the schematic page. Clear this check box to print the entire schematic page. When Print area is selected, all print options except Print quality, Copies, Print to file, and Print all colors in black are unavailable. Output o selected print area is zoomed in and centered.
Include pages outside hierarchy	Specifies to also print pages in the design that are not included in the root hierarchy. If you do not select this option, only those files included in the root hierarchy will print.
Include referenced pages in other libraries or designs	Specifies to also print pages outside of the design that the root hierarchy references. If you do not select this option, only the files in the design's root hierarchy will print.

Print statistics

- Printed pages per document page - Specifies the number of horizontal and vertical pages needed to print a document. If a schematic page (document page) takes more than one page to print out, Capture reports the total number of pages under the Total column heading. Horizontal and Vertical refers to the pages that will make up the printed schematic page.

  For example, a schematic page may take four pages to print, so the Total is 4. Depending on physical shape of the design, the Horizontal may be 2 and the Vertical may be 2 (2 x 2), or the Horizontal may be 4 and the Vertical may be 1 (4 x 1).

- Maximum page size for selected printer - These dimensions identify the printable page area of the printer and are dependent on the printer and paper size.

- Size from schematic page properties - Specifies the dimensions of the page size selected on the Page Size tab of the Schematic Page Properties dialog box.

- Size of actual printout - Specifies the scaled document size as it changes with different settings in the Scale options or when you change the page orientation in the Print Setup dialog box.

  The Maximum size for the page layout, Size from schematic page properties, and Size of actual printout dimensions are shown in inches or millimeters, depending on the setting you've chose in the Design Template dialog box.

Setup

Display a standard Windows dialog box to set printer or plotter configuration.

Print Setup dialog box

This dialog box appears when you choose the Print Setup command from the File menu or when you click the Setup button on the Print dialog box or Print Preview and Print Setup dialog boxes.

The Print Setup dialog box is a standard windows dialog box for configuring your printer or plotter. Use it to choose a printer, paper

source, and orientation before printing. For more information on setting up printers and plotters, refer to the documentation for your configured printer driver.
Many times, the options for your printer are not available in the standard setup dialog box. If you do not find the options you need, try the printer setup in the Windows Control Panel.

Print to File dialog box

The Print to File dialog box appears when you select the Print to File option and then click OK in the Print dialog box.

Use this control...	To do this...
Output file name	Specify the name of the output file.

Programmable Logic Project Wizard dialog box

Programmable logic project for designs may include Verilog or VHDL models as part of the structure. Projects of this nature will often use simulation and synthesis tools as part of the design flow. When you create a programmable logic project, certain folders are added to the project. These are discussed in Working with the project manager.

To create a programmable logic project:

1. Select the logic vendor and target family for the project (for example, Actel, Altera, and Xilinx family).
2. Click the Finish button.

Propagation Delay dialog box

The Propagation Delay dialog box appears when you choose the Invoke UI command from the Edit menu or press CTRL+U shortcut keys while editing the PROPAGATION_DELAY property in the Property Editor. Alternatively, you can right-click the grid corresponding to the PROPAGATION_DELAY property and select Invoke UI from the popup menu.

The PROPAGATION_DELAY property has the following syntax:

<Pin_pair>:<min_value>:<max_value>

You can use this dialog box to specify a pin-pair and select valid minimum and maximum value for the PROPAGATION_DELAY property.

Use this control...	To do this...
Pin Pair	Applies Min and/or Max delay constraint to various pin-pairs. This value may be set to one of the following: ■ *Longest/Shortest pin-pair*—Minimum delay is applied to the shortest pin-pair and maximum delay is applied to the longest pin-pair. ■ *Longest/Shortest Driver/Receiver*—Minimum is applied to the shortest Driver/Receiver pin-pair and maximum is applied to the longest Driver/Receiver pin-pair. ■ *All Drivers/All Receivers*—Min/Max constraints apply to all Driver/Receiver pin-pairs.
Min	Specifies the minimum allowable propagation delay/length for the pin-pairs.
Min Rule	Specifies whether the minimum allowable propagation delay is measured as DELAY in ns, %MANHATAN, or LENGTH in mills (mils), micron (um), millimeter (mm), centimeter (cm), and inches (in).

Max	Specifies the maximum allowable propagation delay/length for the pin-pairs.
Max Rule	Specifies whether the maximum allowable propagation delay is measured as DELAY in ns, %MANHATAN, or LENGTH in mills (mils), micron (um), millimeter (mm), centimeter (cm), and inches (in).
Add Pin Pair	Displays the Create Pin Pairs dialog box dialog box. Use this dialog box to define a pin-pair. *Keyboard shortcut: ALT, A*
Delete Pin Pair	Deletes the pin-pair corresponding to the selected row. *Keyboard shortcut: ALT, D*
OK	Performs syntax checking and if the syntax is correct assigns the PROPAGATION_DELAY property on the selected net.

Note: You can use the User Properties dialog box to assign the PROPAGATION_DELAY property to all the bits of a bus at the same time. Make sure that you use the correct syntax for specifying a value for the PROPAGATION_DELAY property. The syntax is:

```
<Pin_pair>:<min_value>:<max_value>
```

The pin-pairs can only be:

- L:S
- D:R
- AD:AR

Properties dialog box

The Properties dialog box appears when you choose the Properties command from the Edit menu, or from the pop-up menu. You can use the dialog box to access information about the current project, or the file currently selected in the project manager window. You can also change the description of a file.

Use this tab...	To do this...
General tab	Provide information about the file name, size, and the date it was last modified. For more information, see General tab
Type tab	Specify the type of the file, such as schematic or simulation model. For more information, see Type tab.
Project tab	Specify project options. These options include project type, vendor, and family. For more information, see Project tab.

General tab

Use this control...	To do this...
File name	Displays the name of the file currently selected in the project manager window.
Last modified date	Displays the date that the file was last modified.
Size	Displays the size (in bytes) of the file currently selected in the project manager window.

Project tab

Use this control...	To do this...

Project Type	Displays the type of project, PSpice, FPGA, PCB, or Schematic, as specified in the project wizard.
Vendor	Displays the name of the device vendor you specified for the project if you are working on an FPGA project. Otherwise, this field is blank.
Family	Displays the device family of the vendor named in the Vendor field (above). Otherwise, this field is blank.

Type tab

Use this control...	To do this...
File type drop-down list	The drop-down list provides a list of file descriptions. The file description of the file that is currently selected in the project manager window appears in the window. Select another file description from the drop list to change the file type of the file currently selected in the project manager window.

Relative Propagation Delay dialog box

The Relative Propagation Delay dialog box appears when you choose the Invoke UI command from the Edit menu or press CTRL+U shortcut keys while editing the RELATIVE_PROPAGATION_DELAY property in the Property Editor. Alternatively, you can right-click the grid corresponding to the RELATIVE_PROPAGATION_DELAY property and select Invoke UI from the popup menu.

The Relative Propagation Delay dialog box allows you to define an error-free RELATIVE_PROPAGATION_DELAY property.

The RELATIVE_PROPAGATION_DELAY property can have one of the following two syntax:

1. For the target pin-pair

   <match_group>:<scope>:<pin-pair>::

   where <pin-pair> has the following syntax:

   <pin1>:<pin2>

2. For non-target pin-pairs

   <match_group>:<scope>:<pin-pair>:<delta>:<tolerance>

You can use the Relative Propagation Delay dialog box to specify a pin-pair and select valid match_group, scope, pin-pair, delta and tolerance for the RELATIVE_PROPAGATION_DELAY property.

Use this control...	To do this...
Matched Group	Displays the current match group. To change the match group: ■ Select a group from the list box. ■ Type a new match group name. Do not press Enter after typing match group name as it will close the dialog box. Based on the match group selected, all nets contained in it will display in the *Nets Attached* box.

Pin Pair	Applies Min and/or Max delay constraint to various pin-pairs. This value may be set to one of the following: ■ *Longest/Shortest pin-pair*—Minimum delay is applied to the shortest pin-pair and maximum delay is applied to the longest pin-pair. A constraint when set on the longest pin-pair of a net is most stringent. If the constraint is met by the longest pin-pair, it is ensured that the constraint will be met by all other pin-pairs of the net also. ■ *Longest/Shortest Driver/Receiver*—Minimum is applied to the shortest Driver/Receiver pin-pair and maximum is applied to the longest Driver/Receiver pin-pair. ■ *All Drivers/All Receivers*—Min/Max constraints apply to all Driver/Receiver pin-pairs.
Scope	Specifies whether the scope of the pin-pair is `Global` or `Local`. By setting the scope as global, you can define the `RELATIVE_PROPAGATION_DELAY` property on different nets of same match group. When scope is set as `Local`, you can define the `RELATIVE_PROPAGATION_DELAY` property on different pin-pairs of same net.
Delta	Specifies the relative value from the target net that all nets in the group should match. **Note:** If a delta value is not defined, all members of the group will be matched within the specified tolerance. **Note:** The delta value may be negative, in which case the delta is subtracted from the routed length of the Target. If it is positive (or unsigned), the value is added to the routed length of the Target.

Units	Specifies whether the measurement unit for delta is DELAY (ns) or LENGTH mills (mils), micron (um), millimeter (mm), centimeter (cm), and inches (in).
Tolerance	Specifies the maximum allowable propagation delay/length for the pin-pairs.
Tol. Units	Specifies the unit for Tolerance. You can select one of the following options in *Tol. Units* field: ■ % ■ DELAY (ns) ■ LENGTH (mils, um, mm, cm, and in)
Add Pin Pair	Displays the Create Pin Pairs dialog box dialog box. Use this dialog box to define a pin-pair. *Keyboard shortcut: ALT, A*
Delete Pin Pair	Deletes the pin-pair corresponding to the selected row. *Keyboard shortcut: ALT, D*
Set Target	Specifies the selected pin-pair as the target pin-pair. The minimum and maximum propagation delay values for other nets will be set relative to the target net. **Note:** When you select a target net pair, the *Target Net Name, Target Pin Pair,* and *Scope* fields above the grid get populated. *Keyboard shortcut: ALT, S*
Delete Target	Removes the target status from the specified net. You can now select a new pin-pair and assign it as target. *Keyboard shortcut: ALT, T*
Nets Attached	This view-only section displays all the nets that are attached to the Match group.

OK

Performs syntax checking and if the syntax is correct assigns the RELATIVE_PROPAGATION_DELAY property on the selected net.

Note: You can use the User Properties dialog box to assign the RELATIVE_PROPAGATION_DELAY property to all the bits of a bus at the same time. Make sure that you use the correct syntax for specifying a value for the RELATIVE_PROPAGATION_DELAY property. The syntax is:

For the target pin-pair:

```
<match_group>:<scope>:<pin-pair>::
```

where <pin-pair> has the following syntax:

```
<pin1>:<pin2>
```

For non-target pin-pairs:

```
<match_group>:<scope>:<pin-pair>:<delta>:<tolerance>
```

The pin-pairs can only be:

- AD:AR
- L:S
- D:R

Remove Occurrence Properties box

The Remove occurrence properties box appears when you choose the Remove Occurrence Properties command from the Design menu with the design name selected in the project manager.

Click Yes, if you want to remove all backannotation and occurrence properties from the design. Otherwise, click No.

If you chose to remove all backannotation and occurrence properties from your design, these properties are permanently removed from the design. You cannot undo this action.

Rename Hierarchical Port dialog box

The Rename Hierarchical Port dialog box appears when you choose the Rename command from the Design menu with a hierarchical port selected in a library in the project manager.

Use this control...	To do this...
Name	Specify the name of the hierarchical port.

Rename Off-Page Connector dialog box

The Rename Off-Page Connector dialog box appears when you choose the Rename command from the Design menu with an off-page connector selected in a library in the project manager.

Use this control...	To do this...
Name	Specify the name of the off-page connector.

Rename Page dialog box

The Rename Page dialog box appears when you choose the Rename command from the Design menu with a schematic page selected in the project manager.

Use this control...	To do this...
Name	Specify the name of the schematic page.

Rename Part dialog box

The Rename Part dialog box appears when you choose the Rename command from the Design menu with a schematic part selected in a library in the project manager.

Use this control...	To do this...
Name	Specify the name of the part.

Rename Part Property dialog box

The Rename Part Property dialog box appears when you choose the Rename Part Property command from the project manager's Edit menu.

Note: The Rename Part Property command is available only when you have selected the design (.DSN) or the schematic page (s) in the Project Manager window.

Use this control...	To do this...
Find User Property	Type the name of the part property you want to change.
Replace with User Property	Type the name of the part property you want.

Rename Power Symbol dialog box

The Rename Power Symbol dialog box appears when you choose the Rename command from the Design menu with a power or ground symbol selected in a library in the project manager. It also appears when you choose the Properties command from the Edit menu with a power or ground symbol selected in the schematic page editor.

If you rename a power or ground symbol using this dialog box, the name is limited to 31 characters.

Use this control...	To do this...
Name	Specify the name of the power or ground symbol.

Rename Schematic dialog box

The Rename Schematic dialog box appears when you choose the Rename command from the Design menu with a schematic folder selected in the project manager.

Use this control...	To do this...
Name	Specifies the name of the schematic folder.

Rename Title Block dialog box

The Rename Title Block dialog box appears when you choose the Rename command from the Design menu with a title block selected in a library in the project manager.

Use this control...	To do this...
Name	Specify the name of the title block.

Replace Cache dialog box

The Replace Cache dialog box appears when you have a part in the design cache folder selected and you choose Replace Cache command from the Design menu.

Use this control...	To do this...
New Part Name	Specify the part's name. The current name appears in the text box. **Note:** If the list of parts is not available in the *Part name* list box, select a library in the *Part Library* field.
Part Library	Specify the path and library containing the replacement part. The current path and library appear in the text box. **Note:** When you select a library, the *Part Name* field displays a sorted list of all parts that you can select.
Browse	Display a standard Windows dialog box for selecting files.
Actions	
Preserve schematic part properties	Retain all instance and occurrence properties of the schematic part in the design, bringing in the graphics, pins, and package properties from the library.
Replace schematic part properties	Bring in graphics, pins, and package properties from the library, totally replacing the schematic part in the design.
Preserve Refdes	Preserve the reference designator of parts and/or symbols that you want to change. **Note:** This option is not available for symbols that do not require preserving of the reference designator. For example, if you have selected a title block, off-page connector, h-port, or power ground symbols, the *Preserve Refdes* check box will be unavailable for selection.

Replace dialog box

The Replace dialog box appears when you choose Replace from the Edit menu while a text editor window is active.

Use this control...	To do this...
Find what	Specify the string to be found and replaced.
Replace with	Specify the string to replace the one specified in the Find What option.
Match whole word only	Specify that the search cannot match the Find What string within another word.
Match case	Specify the search must match the case of the string specified in the Find What option.
Find Next	Find the next occurrence of the specified text, without replacing the currently selected string.
Replace	Replace the currently selected string with the one specified in the Replace With option.
Replace All	Replace all occurrences of the string specified in Find what with the string specified in Replace with. The search and replace takes place in the specified section of the file.

Save Files in Project dialog box

The Save Files in Project dialog box appears when you save a file in a project without first saving the project. Capture may also display this dialog box if you perform an action that requires the project be saved first, and it has not been saved.

Use this control...	To do this...
Yes	Save the design file (*.DSN) and the project file (*.OPJ).
Yes All	Save the design file (*.DSN) and the project file (*.OPJ). Also save any other open files that are part of the project.
No	Don't save the design file (*.DSN).
No All	Don't save any file in the project (*.OPJ).
Cancel	Cancel the action.

Save Part As dialog box

The Save Part As dialog box appears when you choose Save As from the File menu, while in the part editor.

Use this control...	To do this...
Name	Specify the name of the part to be saved.
Library	Specify the path and filename of the library that the part is saved in.

Save Part Instance dialog box

The Save Part Instance dialog box appears when you finish editing a part instance in the part editor window and close its part editor window.

Use this control...	To do this...
Update Current	Apply the changes only to the selected part instance.
Update All	Apply the changes to all instances of the selected part. If you have an identical part from another library, the instances of the part from the second library won't be affected.
Discard	Return to the schematic page editor without applying any changes to the selected part instance.
Cancel	Return to the part editor and continue editing the part.

Schematic Page Properties dialog box

The Schematic Page Properties dialog box appears when you choose the Schematic Page Properties command from the Options menu, when you are in the schematic page editor.

Use this tab...	To do this...
Page Size	Specify the measuring scale used, the page width and height, and the spacing between pins on a schematic page. For more information, see Page Size tab.
Grid Reference	Choose between alphabetic and numeric, and between ascending and descending for both horizontal and vertical grid references. Also use it to set the grid count for both horizontal and vertical grid references, and set the width of grid references. For more information, see Grid Reference tab.
Miscellaneous	Displays the schematic folder's creation time, last modification time, and the number of the schematic page being viewed in the schematic page editor.

Page Size tab

The Schematic Page Properties dialog box appears when you choose the Schematic Page Properties command from the Options menu, when you are in the schematic page editor.

The Design Template dialog box appears when you choose the Design Template command from the Options menu.

Set these options for future schematic pages. Changing these options won't affect schematic pages you've already created.

Use this control...	To do this...

Units	Specify the unit of measurement future designs are measured in. Select either inches or millimeters. This only affects the schematic page editor. It doesn't affect the part editor, which is always measured in grid units.
New Page Size	Specify the size of new schematic pages in the current design. The first five choices are A to E if the unit measurement is inches, or A4 to A0 if the unit measurement is millimeters.
Width	Displays the width of new schematic pages in the indicated unit measurement. You may specify the width of the custom schematic page. All other schematic page widths are permanently set for the current design.
Height	Displays the height of new schematic pages in the indicated unit measurement. You may specify the height of the custom schematic page. All other schematic page heights are permanently set for the current design.
Pin-to-Pin Spacing	Displays the pin-to-pin spacing in the indicated unit measurement.

Grid Reference tab

The Schematic Page Properties dialog box appears when you choose Schematic Page Properties from the Options menu, when you are in the schematic page editor.

The Design Template dialog box appears when you choose the Design Template command from the Options menu.

Set these options for existing schematic pages. Changing these options won't affect future schematic pages.

Use this control...	**To do this...**
Horizontal and Vertical	

Count	Specify the number of divisions in the horizontal or vertical grid references.
Alphabetic and Numeric	Specify whether the grid references are alphabetic or numeric.
Ascending and Descending	Specify whether the grid references ascend or descend.
Width	Specify the width of the grid reference division.
Border Visible	
Displayed	Specify whether the border is visible on the screen.
Printed	Specify if the border is visible on paper.
Grid Reference Visible	
Displayed	Specify whether the grid references are visible on the screen.
Printed	Specify whether the grid references are visible on paper.
Title Block Visible	
Displayed	Specify whether the title block is visible on the screen.
Printed	Specify whether the title block is visible on paper.
ANSI grid references	Specify if schematic pages use the ANSI Standard grid references.

Select Directory dialog box

The Select Directory dialog box appears when you choose the... button in the Archive Project dialog box.

Use this control...	To do this...
Directories	Displays the current selected drive and directory.
Drives	Specify the drive to create the new project on.
Create Dir	Display the Create Directory dialog box to create a new directory on the current drive. The new directory is created below the current selected directory.
Network	Display a standard Windows Map Network Drive dialog box to select a different drive.

Select File Type dialog box

The Select File Type dialog box appears after you add a file to a project.

Use this control...	To do this...
File Types list	Select a file type for the file you are adding to the project. Choose the appropriate type from the provided list: ■ EDIF Netlist ■ List ■ OrCAD Project ■ Report ■ Schematic Design ■ Schematic Library ■ Simulate Stimulus ■ Standard Delay File ■ Unknown ■ VHDL Netlist ■ VHDL SimModel ■ VHDL Source ■ VHDL Synthesis Macro Library ■ VHDL Synthesis Target Library ■ VHDL Testbench ■ Waveform ■ XNF Netlist

Selection Filter dialog box

The Selection Filter dialog box allows you to control the selection of objects in a schematic page during a block-select operation. It provides check box options that allow you to include or exclude objects from a list. For example, if you select the Parts, Nets, and Power/GND check boxes, only these objects will be selected when you perform the block-select operation.

You can open the Selection Filter dialog box in the following ways from the schematic page:

- Right-click the schematic page and select the Selection Filter option from the popup menu.
- Select the Selection Filter command from the View menu
- Use the keyboard shortcut, Ctrl + I

Use this control...	To do this...
Check box under the Schematic Page Drag Selection Filter group	Specify the objects that should be selected when the mouse pointer is dragged diagonally across the schematic page.
Select All	Select all the check boxes in the Schematic Page Drag Selection Filter group.
Clear All	Clear all the selected check boxes in the Schematic Page Drag Selection Filter group.

Select New Project Path dialog box

The Select New Project Path dialog box allows you to specify a different location for the project in the new format.

New Project Path

Specify the location where you want the project in the new format to be created. The project in the old format will be retained in its original location.

Select Occurrence dialog box

This dialog box appears when you try to open a schematic page that has multiple occurrences.

Use this control...	To do this...
Occurrence list	Specify which occurrence of the schematic page you want to open. This option lists all occurrences available for the selected schematic page.

Select Simulation Configuration dialog box

The Select Simulation Configuration dialog box appears when you choose Simulate from the Picflow menu.

Use this control...	To do this...
Simulation configuration	Generate a VHDL netlist of your design and store it in the project manager's In Design folder (if you choose Preroute) or Timed folder (if you choose Postroute) for simulation. **Note:** Before generating the netlist, Capture checks the .DSN file to see if it is current (that is, if you have saved it). If the .DSN file is not current, Capture prompts you to save it.

Note: Legacy programmable logic projects (that is, projects created with a version of Capture previous to version 14.2) that include schematic components from the Xilinx 4000E library, must use the OrCAD XC4KE VHDL libraries for simulation. However, Xilinx 4000E schematics created with Capture version 14.2 (or any later versions), or schematics that have been modified to include the new Xilinx 4000E part symbols, must use the UNISIM VHDL libraries for simulation.

Set Label State dialog box

This dialog box appears when the schematic page editor is active and you choose Label State, Set from the Edit menu.

Use this control...	To do this...
Enter Label	Specify a label for the current state of the schematic page.

Setup dialog box

The Setup dialog box is used to set up, edit and view information about the configuration file used for netlisting and back annotating property information between Capture and PCB Editor. For more information about configuration file, see "Updating the PCB Editor configuration file" on page 578.

You can reach this dialog box by clicking the Setup button in the PCB Editor tab of the Create Netlist or Back Annotate dialog boxes.

Use this control...	To do this...
Configuration File	Mapping file used to pass properties back and forth between Capture and PCB Editor. If you have run a previous netlisting or back annotation the configuration file you used is listed. If not, the first found *.CFG file in your design directory is used. If no *.CFG file is found in your design directory, then the CFG file on the path defined by the CDS_SITE environment variable will be used. Finally, if the CDS_SITE environment variable is not set, the default will be to use the sample ALLEGRO.CFG file that was installed with Capture. The precedence used is: Last Used > Design Directory > CDS_SITE path > Capture Install Directory
Edit	Click this button to edit the configuration file listed in the Configuration File field. The file opens in your default text editor. You can edit the configuration in any text editor. Only changes that are saved to the file get used when you run the netlist. Just having the file open with changes won't be enough.

Backup Versions	Species the number of backup versions of the PST*.DAT files you want to maintain in your design directory. The highest value is the latest (newest). For example, PSTXNET.DAT,2 is the third version of the PSTXNET.DAT netlist file saved, and PSTXNET.DAT is the most recent version saved.
Device/Net/Pin name char limit	Specifies the maximum permissible length of the component, net or pin name. The default is 31. The maximum value permitted by Capture is 255.
Ignore Electrical constraints	Specifies that the following electrical constraints will be ignored during netlist: ■ PROPAGATION_DELAY ■ RATSNEST_SCHEDULE ■ RELATIVE_PROPAGATION_DELAY ■ DIFFERENTIAL_PAIR ■ NET_SPACING_TYPE ■ NET_PHYSICAL_TYPE ■ ELECTRICAL_CONSTRAINT_SET ■ RATSNEST_SCHEDULE ■ VOLTAGE ■ MIN_LINE_WIDTH ■ MIN_NECK_WIDTH ■ MATCHED_DELAY **Note:** These electrical warnings are ignored when the design is forward annotated to layout. However, if any of the above constraints is defined on the board, these constraints will again be ignored in the back-annotation process.
Output Warnings	Specifies if netlist warnings (ALG*) are to be logged during netlisting.

Suppress Warnings	Specifies the netlist warnings (ALG*) to be ignored during netlist.

Simulation Settings dialog box

The Simulation Settings dialog box appears when you choose the Edit Simulation Profile command from the PSpice menu. This dialog box is similar to the Simulation Settings dialog box in PSpice. Both dialog boxes set simulation profile properties.

Use this tab...	To do this...
General	Specify file information and simulation notes. For more information, see General tab
Analysis	Specify analysis options. This includes time domain, DC sweep, AC sweep and noise, and bias point options. For more information, see Analysis tab
Include Files	Add include files for the current design only, or globally for all designs. PSpice searches model libraries, stimulus files, and include files for any information it needs to complete the definition of a part or to run a simulation. Include files are user-defined files that contain: ■ PSpice commands or ■ Supplemental text comments that you want to appear in the PSpice output file Create include files using any text editor, such as Notepad. Include file names typically have an .INC extension. For more information, see the Include Files tab help topic.

Libraries	■ Add new model libraries that were created outside of Capture or the model editor ■ Remove libraries from the configuration list. Removing a library using this dialog box means that you are removing it from the configured list. The library still exists on your computer and you can add it back in if needed. ■ Establish whether a model library is for the current design only, or global for all designs ■ Change the order in which PSpice searches the model libraries ■ Change or add directory search paths PSpice searches model libraries, stimulus files, and include files for any information it needs to complete the definition of a part or to run a simulation. For more information, see the Libraries tab help topic.
Stimulus	Add a stimulus file which contains time-based definitions for analog and digital input waveforms. Pspice searches model libraries, stimulus files, and include files for any information it needs to complete the definition of a part or to run a simulation. You can create a stimulus file by: ■ Manually using the Model Text View of the model editor (or a standard text editor) to create the definition. Stimulus files typically have an .STM extension. ■ Using the stimulus editor, which automatically generates a file with an .STL extension For more information, see the Stimulus tab help topic.

Options	Specify values, limits, and conditions for analog and gate-level simulation, and the information to include in the output file. For more information, see the Options tab help topic.
Data Collection	Specify which data is collected, and what file format is used to write the information. For more information, see the Data Collection Settings tab help topic.
Probe Window	Determine if the Probe window appears when the profile is opened, and either during simulation or after simulation has completed. You can also choose to show all markers on open schematics or show the last plot. For more information, see the Probe Window tab help topic.

Analysis tab

The Analysis tab specifies analysis options for the simulation.

Use this control...	To do this...
Analysis Type	Specify the analysis type. The type determines the options that are available in the Options box. Analysis types include: ■ Time Domain (Transient) ■ DC Sweep ■ AC Sweep/Noise ■ Bias Point

Options	Depending on the analysis type selected, a sub-set of the following options are available. ■ General settings options ■ Primary and secondary sweep options ■ Monte Carlo/Worst Case options ■ Parametric Sweep options ■ Temperature Sweep options ■ Save Bias Point options ■ Load Bias Point options

General settings options

Use this control...	To do this...
Run to time	Specifies a finishing time, or stopping time, for the simulation. You can specify periods shorter than seconds, by including the time increment (such as "ns") immediately after the time period.
Start saving data after	Specifies the time to wait before saving data. This is useful for saving only specific portions of the analysis data and reducing the size of the data file. You can specify periods shorter than seconds, by including the time increment (such as "ns") immediately after the time period.
Transient options	
Maximum step size	Specifies a smaller internal time step value than the default value.
Skip the initial transient bias point calculation	Specifies to skip the calculation of the bias point.
Output File Options	This button displays the Transient Output File Options dialog box

Primary and secondary sweep options

Use this control...	To do this...
Sweep variable	
Voltage source	Specifies the source's voltage is used to set the sweep.
Current source	Specifies the source's current is used to set the sweep.
Global parameter	Specifies that during the sweep, the global parameter's value is set to the sweep value and all expressions are reevaluated.
Model parameter	Specifies that the parameter in the model is set to the sweep value.
Temperature	Specifies to set the temperature to the sweep value. For each value in the sweep, all the circuit components have their model parameters updated to that temperature.
Name	Specifies the name of the source.
Model type	Specifies the model type.
Model name	Specifies the model name.
Parameter name	Specifies the name of the global or model parameter.
Sweep Variable	
Linear	Specifies that the sweep variable is swept linearly from the starting to the ending value.
Logarithmic	Specifies that the sweep variable is swept logarithmically by octaves or decades.
Value list	Specifies that the sweep uses a list of values.
Start value	Specifies the starting value for the sweep.
End value	Specifies the ending value for the sweep.
Increment	Specifies the step size for the sweep.

Monte Carlo/Worst Case options

The Monte Carlo/Worst Case options in the Simulation Settings dialog box's Analysis tab specifies analysis options for the simulation.

Monte Carlo/Worst Case analyses vary the lot or device tolerances of devices, among multiple runs of an analysis (DC sweep, AC sweep, or transient).

You can run either a Monte Carlo or a worst-case analysis, but not both at the same time. Before running either analysis, you must set up the device and lot tolerances of the model parameters to be investigated.

Use this control...	To do this...
Monte Carlo	Perform a Monte Carlo (statistical) analysis of the circuit.
Worst-case/Sensitivity	Perform a sensitivity and worst-case analysis of the circuit.
Monte Carlo options	
Number of runs	Specifies the total number of runs to be performed.
Use distribution	Specifies whether to use the Uniform or Gaussian distribution curve. Uniform is the default distribution. You can also create your own distribution curves by clicking the Distributions button.
Random number seed	Specify the seed for the random number generator within the Monte Carlo analysis. This value must be an odd integer ranging between 1 and 32,767. If this is not specified, the default value of 17,533 is used.

Save data from	Produce output from subsequent runs, after the nominal (first) run. ■ <none> Only the nominal run produces output. ■ All Forces all output to be generated. ■ First Generates output only during the specified number of runs. ■ Every Generates output every specified number of runs. ■ Runs (list) Does analysis for the listed runs.
Distributions	Display the Distributions dialog box.
Worst-case/Sensitivity options	
Vary devices that have	Specify which devices are included in the analysis by the model parameter indicating use of DEV or LOT tolerance.
Limit devices to type(s)	Specify the types of devices to include in the analysis. The list is a string containing the initial letters of PSpice primitives.
Save data from each sensitivity run	Save the worst case data for every run of the DC, AC, or Time Domain analysis.
More Settings	Display the Monte Carlo Worst-Case Output File Options dialog box.

Parametric Sweep options

Use this control...	To do this...
Sweep options	
Voltage source	Specifies the source's voltage is used to set the sweep.
Current source	Specifies the source's current is used to set the sweep.

Global parameter	Specifies that during the sweep, the global parameter's value is set to the sweep value and all expressions are reevaluated.
Model parameter	Specifies that the parameter in the model is set to the sweep value.
Temperature	Specifies to set the temperature to the sweep value. For each value in the sweep, all the circuit components have their model parameters updated to that temperature.
Name	Specifies the name of the source.
Model type	Specifies the model type.
Model name	Specifies the model name.
Parameter name	Specifies the name of the global or model parameter.
Sweep Type	
Linear	Specifies that the sweep variable is swept linearly from the starting to the ending value.
Logarithmic	Specifies that the sweep variable is swept logarithmically by octaves or decades.
Value list	Specifies that the sweep uses a list of values.
Start value	Specifies the starting value for the sweep.
End value	Specifies the ending value for the sweep.
Increment	Specifies the step size for the sweep.

Temperature Sweep options

Use this control...	To do this...
Run the simulation at temperature	Specifies a temperature at which the analysis is done. The value is specified in degrees Centigrade.

Repeat the simulation for each of the temperatures	Specifies that the analysis must be performed for each of the temperatures listed. The values are specified in degrees Centigrade, and must be separated by spaces.

Save Bias Point options

Use this control...	To do this...
Save bias information in filename	Specifies the path and filename to save the bias point node voltages and inductor currents in.
Options	
Save bias information	Specifies to save the bias either at a specific time, or at each time interval. All times are specified in seconds. If a time interval is specified, then only the latest bias is saved.
When Primary Sweep value is	Specifies the first DC sweep value at which the bias point is to be saved. If there are two sweep variables, Primary Sweep value specifies the first value.
When Secondary Sweep value is	Specifies the second value, if there are two DC sweep variables. If there is only one variable, type the value in the Primary Sweep value text box.
When Parametric Sweep value is	Specifies the transient analysis time at which the bias point is to be saved.
When Monte Carlo run number is	Specifies the number of Monte Carlo or worst-case analysis run for which the bias point is to be saved.
When Temperature and Sweep temperature is	Specifies the temperature at which the bias point is to be saved.
Do not save subcircuit voltages and currents	When selected, specifies that node voltages and inductor currents for subcircuits are not saved.

Load Bias Point options

Use this control...	To do this...
Load bias information from filename	Specifies the name of the file to load bias points. It is used in setting initial bias conditions for subsequent simulations. However, loading a bias point file does not guarantee convergence.

Data Collection Settings tab

The Data Collection Settings tab specifies data collection options.

Use this control...	To do this...
Schematic/Circuit Data	
All voltages, currents, and digital states	Collect data for voltages, currents, and digital states.
All but internal subcircuit data	Exclude subcircuit data.
At Markers only	Collect data for the marked node only.
None	Do not collect data.
Save data in the CSDF format (.CSD)	Specify that PSpice will write simulation results to the data file in ASCII format following the CSDF convention.

General tab

The General tab specifies file properties, and simulation profile notes.

Use this control...	To do this...
Simulation Profile	Specifies the name of the current simulation profile.
Input	

Project Name (.OPJ)	Specifies the path and file name of the project file containing the schematic for simulation.
Schematic filename (.DSN)	If Schematic is selected, this specifies the path and file name of the design file containing the schematic for simulation.
Schematic name	Specifies the name of the root schematic for the simulation profile.
Output	
Output filename	Specifies the file name for simulation output.
Probe data filename	Specifies the name for Probe data output.
Notes	Provides a text area for you to record notes on the active simulation profile.

Include Files tab

Include files contain PSpice circuit file commands. PSpice reads these before reading the netlist or simulation profile. Include files are useful for defining mathematical functions used in expressions.

Use this control...	To do this...
Filename	Display an include file name to be added to the current design only, or globally for all designs.
Include Files	Lists the include files to be loaded for the simulation.
Add as Global	Add the include file named in the Filename box to the Include Files list box, as global to all designs.
Add to Design	Add the include file named in the Filename box to the Include Files list box, for the current design only.
Edit File	Open a file you select from the Include Files list for editing.

Libraries tab

Use this tab to configure global and design only model libraries.

Use this control...	To do this...
Filename	Display a selected model library file name to be added to the current design only, or globally for all designs.
Include Files	Lists the model library files to be loaded for the simulation.
Add as Global	Add the include file named in the Filename box to the Include Files list box, as global to all designs.
Add to Design	Add the model library file named in the Filename box to the Library Files list box, for the current design only.
Edit File	Open a model library you select from the Library Files list for editing.

Options tab

Use this control...	To do this...
Category	Specify the category of options available on this tab. The sets of options are: ■ Analog Simulation ■ Gate-level Simulation ■ Output file
Analog Simulation	Use the Analog Simulation settings to fine-tune analog simulation accuracy, set iteration limits, set operating temperature, and specify MOSFET parameters.
MOSFET options	Enter values for the default drain area, default source area, default length, and default width.

Advanced options	Enter values for the total transient iteration limit, relative magnitude for matrix pivot, and absolute magnitude for matrix pivot.
Gate-level Simulation	Use the Gate-Level Simulation settings to set timing, I/O levels for A/D interfaces, drive strength, and error message limits.
Advance options	Enter values for the minimum output drive resistance, maximum output drive resistance, overdrive ratio, default delay calculation, and error message limits.
Output file	Use the Output File settings to select the types of information PSpice A/D saves to the simulation output file.

Note: The option names shown to the right of each text box correspond to the option names used in the PSpice OPTIONS command. For more information about this command, refer to the online PSpice Reference Manual.

Probe Window tab

Use this control...	To do this...
Display Probe window when profile is opened	Display the Probe windows that were displayed the last time the profile was opened.
Display Probe window	
during simulation.	Display the Probe windows when the simulation is running, and update the waveforms as the simulation progresses.
after simulation has completed.	Display the Probe windows when the simulation is finished.
Show	
All markers on open schematics	Show the traces for all the markers that are placed on currently open designs in Capture.
Last plot	Show the traces that were used the last time the profile was opened.

Nothing	Show the traces that were used the last time the profile was opened.

Stimulus tab

Use this tab to configure global and design stimulus files.

Use this control...	To do this...
Filename	Display a selected stimulus file name to be added to the current design only, or globally for all designs.
Include Files	Lists the stimulus files to be loaded for the simulation.
Add as Global	Add the stimulus file named in the Filename box to the Stimulus Files list box, as global to all designs.
Add to Design	Add the stimulus file named in the Filename box to the Stimulus Files list box, for the current design only.
Edit File	Open a stimulus file you select from the Stimulus Files list for editing.

Specify Part Filter dialog box

The Specify Part Filter dialog box appears when you choose Part Search in the Place Part dialog box.

Use this control...	To do this...
Contains Simulation Model	Specify that you want to restrict the part search to only parts that have associated PSpice or HDL simulation models.
PSpice Model	Specify that you want to restrict the part search to only parts that have associated PSpice models. You can also restrict the search to only parts that have associated parameterized or non-parameterized PSpice models.
Smoke information	Specify that you want to restrict the part search to only parts that have associated PSpice models that contain smoke information.
HDL Model	Specify that you want to restrict the part search to only parts that have associated HDL models. You can also restrict the search to only parts that have associated VHDL or Verilog models.
Contains Packaging Information	Specify that you want to restrict the part search to only parts that have packaging information.

Split Part Section Input Spreadsheet

The Split Part Section Input Spreadsheet allows you to divide a part into multiple sections.

Each row in the Split Part Section Input Spreadsheet corresponds to a pin while each column corresponds to properties associated with the pins. The property names are listed as the column header. You can sort a property by double-clicking its column header.

- **Part Name**—Displays the name of the part. This is a non-editable field.
- **Part Ref Prefix**—Displays the part reference. This is a non-editable field.

Important

You need to select a single-sectioned part from a library. You can split a multi-sectioned part only when it has already been split using the Split Part Section Input Spreadsheet.

Tip

To sort on any property, double-click its name in the column header.

Tip

You can hide or show a property column in the Split Part Section Input Spreadsheet. To do this, right-click the property column header you want to hide and select Hide from the pop-up menu. The selected property column will not appear now. To show a property column, right-click the property column header next, on the right-hand side of the hidden property column and select Unhide from the pop-up menu. The hidden property column appears in the Split Part Section Input Spreadsheet. Alternatively, you can show a property column by:

- Double-clicking the column handle ( ) of the property column header.
- Dragging the column handle of the property column header.

(only the last two methods can be used to show a property column, which is the last column in the Split Part Section Input Spreadsheet).

Note: You can change the order in which the property columns appear in the Split Part Section Input Spreadsheet. To do this, select the property column header you want to move and drag and drop it to the location where you want it in the Split Part Section Input Spreadsheet.

Note: You can use standard copy and paste feature to copy all data from the Split Part Section Input Spreadsheet to MS Excel. You can later use the MS Excel file for archiving or documentation. It is recommended that you avoid using MS Excel to paste information into the Split Part Section Input Spreadsheet.

Note: The spreadsheet window is resizable. You can resize the window using the resize cursor you see when you move the mouse pointer to any of the edges of the dialog. You can also use the standard Maximize button on the top right corner of the window.

Use this control...	To do this...
Part Numbering	Specify a numbering format (alphabetic or numeric) that should be added as suffix to the current part reference for the split part. If you select Alphabetic, an alphabet (between A to Z) will be added as a suffix to the current part reference for each of the split parts. If you select Numeric, a number (between 1 and 1024) will be added as a suffix to the current part reference for each of the split parts. **Note:** The Section property column changes based on your selection in the Part Numbering group. For example, if Alphabetic is selected, the Section property column displays “A”.

No. of Sections	Specify the number of sections you want to have in the split part. **Note:** If you select alphabetic numbering, then you can create up to a maximum of 26 sections only. If you select numeric numbering, then you can create up to a maximum of 1024 sections.
Number	Specify the pin number.
Name	Specify the name of the pin.
Type	Specify the type of pin. To change a pin type, select the Type cell, and select *Input, Output, Passive, Open Emitter, Open collector, 3 State, Bidirectional,* or *Power*. *Tip* You can select the Type cells for multiple pins simultaneously using the SHIFT+Down Arrow keys and then enter the pin type. The selected Type cells get populated with the pin type of your choice. Alternatively, you can: ❑ Select the Type cells for multiple pins simultaneously using the SHIFT+Left mouse button click, then press the CTRL key, and then select a pin type of your choice from the list box. The selected Type cells get populated with the pin type of your choice. ❑ Click the first cell of the range, and then drag to the last cell, and then enter the pin type of your choice. The selected Type cells get populated with the pin type of your choice. (You can use these methods to make selection in the Shape, Position, and Section property column list boxes also).
Shape	Specify a shape for the pin. To change a pin shape, select the Shape cell, and select *Clock, Dot, Dot-Clock, Line, Short, Short Clock, Short Dot, Short Dot-Clock, Zero length.*
PinGroup	Specify a value for each swappable (input) pin of the part.

Position	Specify the pin position as left, right, top or bottom. To change position for a pin, select the Position cell, and select *Left*, *Right*, *Top*, or *Bottom*.
Section	Specify a section number. By default, all pins are assigned the sections 1 or A depending on the selection made in the Part Numbering group. To change a section for a pin, select the Section cell, and select the required section number from the list. *Tip* You can select Section cells for multiple pins simultaneously using the SHIFT+Down arrow keys and enter the section number. Alternatively, you can: ❑ Select the Section cells for multiple pins simultaneously using the SHIFT+Left mouse button click, then press the CTRL key, and then select a section number of your choice from the list box. The selected Section cells get populated with the section number of your choice. ❑ Click the first cell of the range, and then drag to the last cell, and then enter the section number of your choice. The selected Section cells get populated with the section number of your choice. *Tip* You can select alternate Section cells for multiple pins simultaneously using the CTRL+Left mouse button click and enter the section number.
Add Pins	Add new pins at the end of the current pin set in the Split Part Section Input Spreadsheet.

Delete Pins	Delete selected row containing the pin information from the Split Part Section Input Spreadsheet. *Caution* ***Once you delete a pin from the Split Part Section Input Spreadsheet, you cannot retrieve it later.***
Save	Splits the part into multiple sections as specified in the *Section* property column and saves the current part. If any warnings are generated during the save operation, a message box appears asking you whether you want to view the warnings. If you want to view the warnings, click the View Warnings button. The Split Part Section Input Spreadsheet expands and displays a grid showing warnings messages. If you select the Continue button, the split part is saved as is.
Hide Warnings	Hide the warning messages.
Show Warnings	Show the warning messages again.
Save As	Retain the original part and save the changed part as a new part in the same library.

Synthesis Option dialog box

This dialog box provides a method to set certain options for Synplify (Synplicity's synthesis tool).

Use this control...	To do this...
Interactive Mode	Specify that Synplify is started in interactive mode, allowing you to set any particular synthesis or optimization options, "on the fly."
Batch Mode	Specify a batch file that runs Synplify "in the background," according to the parameters specified in the file.
Create Synplify Project	Specify that Capture create a new Synplify project for the current synthesis run. If you have already created a Synplify project, perhaps from a previous synthesis run, you can specify a path to that project in the appropriate text box.

Note: For specific information on the various Synplify commands, please refer to your Synplify documentation.

Transient Output File Options dialog box

The Transient Output File Options dialog box appears when you select the General Settings option from the Analysis tab of the Simulate Settings dialog box, and click the Output File Options button.

Use this control...	To do this...
Print values in the output file every:	Specify the interval for printing transient values to the output file.
Perform Fourier Analysis	Perform a Fourier analysis, which decomposes the results of transient analysis to Fourier components.

Center Frequency	Specify the fundamental frequency. Not all of the transient results are used; only the interval from the end, back to 1/frequency before the end is used. This means that the transient analysis must be at least 1/frequency seconds long.
Number of Harmonies	Specify the number of harmonics of the selected voltages and currents to be calculated in the transient analysis.
Output Variables	Specify a list of output variables. The output is split up depending upon the width of the data columns and the output width.
Include detailed bias point information for nonlinear controlled sources and semiconductors (/OP)	Include detailed information about the bias point. The bias point is calculated regardless of whether this option is selected or not. However, if this option is not selected, then the only information about the bias point is a list of the node voltages, voltage source currents, and total power dissipation. Selecting this option can cause the small-signal (linearized) parameters of all the nonlinear controlled sources and all the semiconductor devices to be placed in the output file. This option controls the output for the regular bias point only.

Update Properties dialog box

The Update Properties dialog box appears when you choose the Update Properties command from the Tools menu.

Use this control...	To do this...
Scope	Specify whether to process all the properties in the design or just in the selected schematic page or pages.
Mode	Update either instances or occurrences. Capture automatically sets this option based on the project type. FPGA and PSpice projects default to use instances, while PCB and Schematic projects default to occurrences.
Action	
Update parts and Update nets	Specify whether to update the properties of parts or nets.
Use case insensitive compares	Match the combined property string with update properties without regards to case sensitivity.
Convert the update property to uppercase	Convert the case of characters in the update property to uppercase. The update file itself remains unchanged.
Unconditionally update the property (normally only updated if empty)	Unconditionally change the specified property. By default, a property is only updated if it is empty. That is, properties with values already in them are not updated.
Do not change updated properties visibility	Specify that the visibility of the updated properties is not changed
Make the updated property visible	Specify that the updated property is to be made visible.
Make the updated property invisible	Specify that the updated property is to be made invisible.
Create a report file	Specify whether Capture creates a report file.
Report file	Specify a report filename and path.

Property update file	Specify an update file. The update file must be in ASCII format.
Browse	Displays a standard Windows dialog box for selecting files.

Update Old Project wizard

The Update Old Project wizard allows you to convert your project to the Capture 10.0 format. Converting your analog project to the Capture 10.0 format has the following benefits:

- Capture 10.0 introduces a new directory structure for analog projects that makes it easier to manage the files for the project.
- You can use the new simulation profile features in PSpice if your project is in the Capture 10.0 format. For more information on the new simulation profile features in PSpice, see the PSpice online help.

Important

Once you convert your project to the new format, you cannot open the project in the new format in Capture version 9.2.3 or older versions. You can create the project in the new format in a different location so that you have a backup of the project created in Capture 9.2.3 or older versions.

Important

Before you convert a project to the new format, ensure that the schematic names do not have the / (forward slash) or the \ (backward slash) character. If you do not do this, the conversion will fail. To rename a schematic that has the / or \ character in its name, select the schematic name in the Capture Project Manager and choose Rename from the Design menu.

Convert the Project

Select this option if you want to convert the project to the new format.

Retain Old Project

Select this check box if you want to retain the project in its original location and create the project in the new format in a different location.

If you do not select this check box, the project in the new format will overwrite the project in the old format.

Note: Cadence recommends that you select this check box so that you have a backup of the project in the old format.

None

Select this option if you do not convert the project to the new format.

Do not ask me this question again

Select this check box if you want Capture to remember the settings in the Update Old Project wizard.

- If the Convert the Project option is selected, any analog project created using version Capture 9.2.3 or older versions that you open in Capture 10.0 will be automatically converted to the new format.

  Later on, if you want to disable automatic conversion of old analog projects to the new project format, delete the entry given below that exists in the `[PSPICE]` section of the PSPICE.INI file.

  - CONVERTDESIGN=CONVERT

    Or

  - CONVERTDESIGN=CONVERT_AND_RETAIN

- If the None option is selected, Capture will not prompt you to convert any analog project created using Capture version 9.2.3 or older versions to the new format.

  Later on, if you want to enable conversion of old analog projects to the new project format, delete the following entry that exists in the `[PSPICE]` section of the PSPICE.INI file located in the `/tools/pspice` directory under your installation directory:

  ```
  CONVERTDESIGN=NOCONVERT
  ```

User Properties dialog box

The User Properties dialog box appears when you click on the User Properties button, or choose Part Properties from the part editor's Options menu.

Use this control...	To do this...
Name	List the item’s properties.
Value	Display the value of each property.
Attributes	Display the attributes of each property. An "R" indicates the property is read-only, and a "V" indicates the property is visible to the user. You cannot remove or change the values of read-only properties, but you can set their visibility in the Display Properties dialog box.
New	Display the New Property dialog box so you can create a property for the item.
Remove	Remove the selected property from the item's property list.
Display	Display the Display Properties dialog box so you can change the appearance of the selected property.

Note: You can use the User Properties dialog box to assign PROPAGATION_DELAY and RELATIVE_PROPAGATION_DELAY properties to all the bits of a bus at the same time. Make sure that the syntax is correct. For more information, see “Assigning signal flow properties” on page 607.

VHDL Samples dialog box

The VHDL Samples dialog box opens when you choose Samples from the Edit menu. When you select a sample in the upper box, the associated sample lines appear in the lower box. Double-click on the sample type in the upper box or select it and click OK to copy the sample into the text editor.

The VHDL Samples dialog box contains an alphabetical reference of VHDL language keywords and samples.

In addition to the samples, there are overviews of four important VHDL packages compatible with Capture:

- Numeric_Std (IEEE 1076.3)
- Standard (IEEE 1076)
- Std_Logic (IEEE 1076-1164)
- Textio (IEEE 1076)

Upper box

Displays a list of VHDL sample types. When you select a sample type, the associated sample lines appear in the lower box.

Some of the sample constructs available:

Use this control...	To do this...
Component Instance	This sample provides a template for component instantiation in a VHDL model.
ENTITY/ARCHITECTURE	This sample provides a template for the ENTITY and ARCHITECTURE statements required in all VHDL models.
PROCESS STATEMENT	This sample provides a template for sequential PROCESS statements in your VHDL model.
Testbench clock	This sample provides a template for a VHDL clock definition.

Testbench Self-Check (ASSERT)	This sample provides a template for defining report statements that appear when a particular condition is met during simulation.
Testbench Table of Vectors	This sample provides a template for defining a table of test bench vectors.
Testbench Wire to Bus	This sample merges scalar ports into a vector signal.

Note: You can add your own samples to the list by editing the STANDARD.VHX file in the /Capture directory.

Lower box

Displays a list of VHDL sample file lines. The sample lines displayed are associated with the selected sample type in the upper box.

OK

Copies the contents of the lower box to the active VHDL file and to the Clipboard.

View DRC Marker dialog box

The View DRC Marker dialog box appears when you select a DRC marker and choose Properties from the Edit menu.

Use this control...	To do this...
DRC Marker text box	Displays the DRC marker number and message. This is the same message that appears in the session log and the DRC report.

Zoom Scale dialog box

The Zoom Scale dialog box appears when you choose Zoom and then Scale from the schematic page editor's View menu.

Use this control...	To do this...
X%	Choose a pre-defined zoom scale ranging from 25% to 400%.
Custom X%	Specify a custom zoom scale.

NetGroup dialog box

The NetGroup dialog displays when you choose NetGroup from the Place menu.

Use this control...	To do this...
Add NetGroup	Click this button to open the New NetGroup dialog to create a NetGroup.
Modify NetGroup	Click this button to open the Modify NetGroup dialog to modify a NetGroup. **Note:** You need to click the check mark next to a NetGroup name to open the associated NetGroup definition in this dialog.
Import NetGroups	Click this button to import NetGroups definition Xml files.
Instance Name	Enter the instance name of a named NetGroup to place on the schematic page.
Place NetGroup Block	Check this box to place the NetGroup as a block on the schematic page.
Place Unnamed NetGroup	Check this box to place the NetGroup as an unnamed NetGroup block on the schematic page.

New NetGroup / Modify NetGroup dialog box

The New NetGroup or Modify NetGroup dialog boxes displays when you click the Add NetGroup or Modify NetGroup buttons on the NetGroup dialog box.

Use this control...	To do this...

NetGroup Name	Enter the name of the NetGroup. **Note:** This textbox is disabled in the Modify NetGroup dialog.
Apply	Use this button to save the name of the NetGroup. **Note:** You cannot add members to a NetGroup, until you have applied the NetGroup name.
Add	Add a member (NetGroup, bus, or scalar) to the NetGroup.
Delete	Delete a NetGroup member.
Rename	Rename a NetGroup member.
UP	Move the NetGroup member position up.
Down	Move the NetGroup member position down.

Rename NetGroup Member dialog box

The Rename NetGroup Member dialog displays when you click the Rename NetGroup button on the New NetGroup or Modify NetGroup dialog boxes.

Use this control...	**To do this...**
Name	Enter the name of the NetGroup member to rename. **Note:** When you rename a NetGroup member that is a NetGroup, you need to choose the name of a NetGroup that already exists in this design. Also, the NetGroup to which you rename this member to, must not already exist in the current NetGroup.

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Window descriptions

The following is an exhaustive set of descriptions for the window types you may encounter using Capture. Each description is listed alphabetically, using the window title.

Browse window

The browse window displays the results of a browse of parts, nets, hierarchical ports, off-page connectors, DRC markers, and bookmarks.

When you browse a design or library, you can sort the results using the buttons at the top of the browse window. Each type of object offers a different set of buttons. When you click on one of these buttons, Capture alphabetically sorts the selection by the value of the corresponding property. To view a specific object, double-click on the item in the browse window. To add, delete, or change properties, select objects in the browse window, and then choose the Properties command from the Edit menu.

Parts

Reference	Order by the part reference.
Value	Order by the part value. If the part has no alias, this column is identical to Source Part.
Source Part	Order by the source part. If the part is an alias, this column shows the original part.

Source Library	Order by the source library. This column shows the path and library where the part exists.
Page	Order by the schematic page the part is on.
Schematic	Order by the schematic folder the part is in.

Nets

Name	Order by the net alias name.
Net Name	Order by the net name.
Page	Order by the schematic page the net is on.
Schematic	Order by the schematic folder the net is in.

Hierarchical ports

Port Name	Order by the hierarchical port name.
Port Type	Order by the hierarchical port type.
Page	Order by the schematic page the hierarchical port is on.
Schematic	Order by the schematic folder the hierarchical port is in.

Off-page connectors

Off-Page Name	Order by the off-page connector name.
Page	Order by the schematic page the off-page connector is on.

Schematic	Order by the schematic folder the off-page connector is in.

Bookmarks

Bookmark Name	Order by the bookmark name.
Page	Order by the schematic page the bookmark is on.
Schematic	Order by the schematic folder the bookmark is in.

DRC markers

DRC Error	Order by the DRC error message text. This is the text that appears in the session log, the DRC report, and the View DRC Marker dialog box.
DRC Detail	Order by the object generating the error.
DRC Location	Order by the absolute location of the error.
Page	Order by the schematic page the DRC marker is on.

Session frame window

The session frame contains the following components:

- session log
- project manager
- browse window
- schematic page editor
- part editor

As with other true Windows applications, each of these components can be reduced to an icon (minimized), opened (maximized), and resized. For more information on using Windows applications, see your Windows documentation.

Session log window

The session log contains a record of events that occur during the current session of Capture. This window has a ruler with adjustable tabs, so you can format the way the information in the session log appears. This formatting only applies to the session log. It doesn't affect the way reports are formatted in other applications. You can set the session log ruler measurements to appear in U.S. or metric units by using the appropriate setting in the Regional Settings of your Control Panel.

The session log also includes results and messages from Capture utilities found on the Tools menu. If Capture reports an error or warning in the session log, you can get specific help on it by double-clicking on the message. In this case, Capture opens the file that contains the error and places the cursor at the location of the error. These files include netlists, CDS.LIB, HDL.VAR, and VHDL/Verilog models.

Note: The following Capture utilities are found on the Tools menu:

Annotate
Back Annotate
Update Properties
Design Rules Check
Create Netlist
Cross Reference
Bill of Materials
Export Properties
Import Properties

The session log is replaced every time you start Capture, so it is initially empty. You can clear the session log at any time by choosing Clear Session Log (ALT, E, S) from the Edit menu, or pressing CTRL+DEL.

You can minimize the session log by pressing CTRL+F4, or by choosing the Close button in the upper-right corner of the session log

window. To open the session log, choose Session Log (ALT, W, 1) from the Window menu. The session log records utility results and error messages even while it is minimized.

You can save the session log as an ASCII text file, and you can copy text from the session log onto the Clipboard. You cannot load a saved session log into Capture, and you cannot cut or paste text in the session log.

Part editor window

You edit parts and symbols in the part editor window. This window has two view splitters. The splitter at the upper right divides the view horizontally. The splitter at the lower left divides the view vertically. Each view has its own scroll bars, so you can view separate areas on the same part.

You can create parts up to 32 by 32 inches.

Part View

You edit parts in this view.

Package View

You see the entire package in this view. You cannot edit parts in this view, but you can select parts to edit. This view has no view splitters.

The part editor tool palette is unavailable in this view.

Property editor window

The property editor window appears when you select some combination of parts, nets, pins, title blocks, aliases and globals in the schematic page editor, and then choose Properties from the Edit menu or choose Edit Properties from the pop-up menu. You can use the property editor window to edit part, net, pin, title block, global, port, and alias properties. The property editor displays all library definitions, instance properties, and occurrence properties for an object.

Do not manually change the reference designators of heterogeneous parts for a complex hierarchical design. In case you want to change the reference designator for a part placed in the schematic page, delete the part and add it again. This way all the occurrences will get updated correctly.

New Column or New Row

Displays the Add new column or row dialog box, depending on the property editor orientation, to add a new property column or row. To add the property to an object, you must enter a property value for a given object.

Apply

Applies the changes in the property editor to the schematic page. The Apply button does not dismiss the property editor. You can also apply the changes to the schematic page by closing the property editor.

Display

Displays the Display Properties dialog box to set the display option of the selected property and its value. You cannot display properties of an occurrence property using the Display Properties dialog box.

Delete Property

Deletes the editable property from the selected object or objects. (Properties that are not editable appear in italics.) If you select all of a property's cells and click the Delete Property button, the property will be removed from the selected objects but will remain in the filter. This is indicated by the hash marks that appear in the cell.

Filter by

Specifies a filter by which to view the objects. Use the property editor filter to constrain the available properties. For example, the Capture filter displays common schematic capture properties available to most parts, while the Cadence-Allegro filter displays properties needed to send a design to PCB Editor. You can view all the properties available on the objects in the property editor by selecting the <Current properties> filter from the drop-down list.

Parts

Displays the parts of the selected objects. The Parts tab includes hierarchical blocks.

Schematic Nets

Displays the schematic nets of the selected objects. This tab includes constituent nets within buses.

Pins

Displays the pins of the selected objects. This tab includes hierarchical pins in hierarchical blocks.

Title Blocks

Displays the title blocks of the selected objects.

With the Title Blocks tab selected, you can add a property to the Title Block instance on a schematic page that will display the full hierarchical path to the schematic.

Globals

Displays selected globals for simultaneous editing of multiple names.

Ports

Displays source symbol, source library, and type of port. Provides for simultaneous editing of multiple ports.

Aliases

Displays color, font, name, and rotation of net aliases. Use the Aliases tab to edit multiple aliases at one time.

Rows and columns

Each row displays an instance or an occurrence of an object. Instance rows appear with a white background. Occurrences appear in yellow below their associated instance row. Occurrence rows automatically appear when one or more of the occurrence property values are different from the instance property values.

Each column is a placeholder that you can use to add properties. The cells in the property editor show the property values for each instance or occurrence. A cell with hash marks in indicates that the property does not exist on the object that the cell represents. You can add a value by clicking inside the cell, typing the value, and pressing ENTER or clicking the Apply button. A property value in italics is a read only property cannot be edited.

Tip

Roll the mouse wheel up and down to scroll through vertically in the Property Editor.

Tip

Hold down the CTRL key and roll the mouse wheel to zoom in and zoom out.

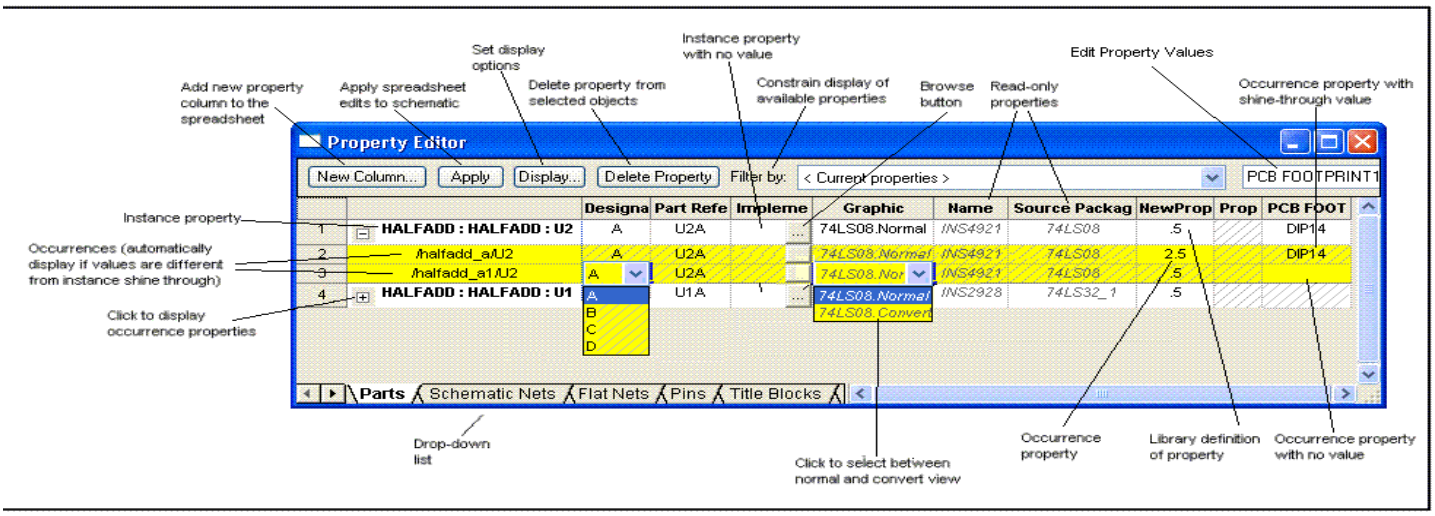
Tip

Hold down the SHIFT key and roll the mouse wheel up and down to scroll through horizontally in the Property Editor.

Tip

Click the mouse wheel button and drag the mouse wheel:

- To the right or left in the Property Editor window to scroll horizontally.
- Up or down in the Property Editor window to scroll vertically.



Short-cut keys

The following short-cut keys apply to the Property Editor:

Operation/command	Short-cut key
Undo	CTRL+Z
Copy	CTRL+C
Paste	CTRL+V
Cut	CTRL+X
Find	CTRL+F
Move to first cell in column	PageUp/CTRL+<Up-Arrow>
Move to last cell in column	PageDown/CTRL+<Down-Arrow>
Move to first cell in row	CTRL+<Left-Arrow>

Operation/command	Short-cut key
Move to last cell in row	CTRL+<Right-Arrow>
Undo Edit (within a cell)	Esc
Select	SHIFT+<Arrow key>
Move to top left cell in spreadsheet	CTRL+Home
Move to bottom right cell in spreadsheet	CTRL+End
Select cell contents	CTRL+F2
Close spreadsheet	CTRL+F4

Project manager window

The project manager appears in the Capture session frame whenever you open or create a project. Use the project manager to collect and organize all the resources you need for your project throughout the design flow. These resources include schematic design files, part libraries, netlists, VHDL models, simulation models, timing files, stimulus files, and any other related information.

The project manager provides two views of a project. If you choose the File tab, you see a complete list of all project resources and files, organized in folders. If you choose the Hierarchy tab, you see the hierarchy view, which displays the hierarchical relationship among the various design modules. A design module is a structural block, typically represented as a distinct hierarchical entity, that defines the functionality of a particular portion of your design. A design module in Capture can be either a VHDL model or a schematic folder.

Each project may contain one design. This design may consist of any number of schematic folders, schematic pages, or VHDL models, but must have a single root module. The root module is the module that is defined as the top-level entity for the design. That is, all other modules in the design are referenced within the root module.

Within the project manager, you can expand or collapse the structure you are viewing by clicking on the plus sign or minus sign to the left of a folder. A plus sign indicates that the folder has contents that are not currently visible; a minus sign indicates that the folder is open and

its contents are visible, listed below the folder. When you double-click on a schematic folder, Capture displays the schematic pages within that folder. If the folder is a VHDL model, Capture displays each defined entity in that model. When you double-click on a schematic page or a VHDL entity, you open that object in an appropriate editor. For example, double-clicking on a VHDL entity opens the VHDL model file at the location of that entity definition in Capture's VHDL editor.

Each project you open has its own project manager window. You can move or copy folders or files between projects by dragging them from one project manager window to another (as well as from the Windows Explorer). If you close a project manager window, you close the project.

File tab

The file tab shows all the files included in the project. These files may include VHDL models, netlists, schematic pages, simulation models, stimulus files, or any other files that contain information related to the project. The file view is organized in folders, each of which contains certain types of project files.

Hierarchy tab

The Hierarchy tab shows the hierarchical relationship among the various modules of the design.

Each instantiation of a particular module appears in the hierarchy view as part of a hierarchical "tree". The hierarchical view of the design is derived from the files that exist in the Design Resources folder.

Schematic page editor window

You edit schematic pages in the schematic page editor window. This window has two view splitters. The splitter at the upper right divides the view horizontally. The splitter at the lower left divides the view vertically. Each view has its own scroll bars, so you can view separate areas on the same page.

Tip

Roll the mouse wheel up and down to scroll through vertically.

Tip

Hold down the CTRL key and roll the mouse wheel to zoom in and zoom out.

Tip

Hold down the SHIFT key and roll the mouse wheel up and down to scroll through horizontally.

Tip

Click the mouse wheel button and drag the mouse wheel:

- To the right or left in the schematic page editor to scroll horizontally.
- Up or down in the schematic page editor to scroll vertically.

Text editor window

Use the text editor to create or edit text files such as VHDL or Verilog files and simulation models. You can set syntax for VHDL and Verilog to appear in different colors in the Text Editor tab in the Preferences dialog box.

You can open the text editor by choosing Open from the File menu, by selecting a text file in the project manager and choosing Edit from the pop-up menu, or by dragging the file from the Explorer into the session frame. You can only open ASCII text files using the text editor.

The text editor has the following features:

Help

Help Topics	F1

Saving and Printing

Save	CTRL+S
Print	CTRL+P

Editing text

Join Line	ALT+J
Split Line	ALT+S
Copy	CTRL+C
Paste	CTRL+V
Cut	CTRL+X
Cut line to clipboard	CTRL+Y
Undo	CTRL+Z
Redo	CTRL+A
Delete	DELETE
Toggle insert/overwrite mode	INSERT

Searches

Search Forward	CTRL+F
Search Backward	CTRL+SHIFT+F

Blocks and marks

Select up one line	SHIFT+UP ARROW
Select down one line	SHIFT+DOWN ARROW
Select left one character	SHIFT+LEFT ARROW
Select right one character	SHIFT+RIGHT ARROW
Select left one word	CTRL+SHIFT+LEFT ARROW
Select right one word	CTRL+SHIFT+RIGHT ARROW
Select to end of line	SHIFT+END
Select to end of file	CTRL+SHIFT+END
Select to beginning of line	SHIFT+HOME
Select to beginning of file	CTRL+SHIFT+HOME
Select one page down	SHIFT+PAGE DOWN
Select to end of file	CTRL+SHIFT+PAGE DOWN
Select one page up	SHIFT+PAGE UP
Select to beginning of file	CTRL+SHIFT+PAGE UP

Cursor control

Move cursor up one line	UP ARROW
Move cursor down one line	DOWN ARROW
Move cursor left one character	LEFT ARROW
Move cursor right one character	RIGHT ARROW
Move cursor left one word	CTRL+LEFT ARROW
Move cursor right one word	CTRL+RIGHT ARROW
Move cursor to end of line	END

Move cursor to beginning of line	HOME
Page up	PAGE UP
Page down	PAGE DOWN
Move cursor to beginning of file	CTRL+HOME
Move cursor to beginning of file	CTRL+PAGE UP
Move cursor to end of file	CTRL+END
Move cursor to end of file	CTRL+PAGE DOWN

Pop-up menu

A pop-up menu is available in the text editor window. Click the right mouse button to bring up the pop-up menu. The following commands are available in this menu:

- Cut command
- Copy command
- Paste command
- Delete command
- Select All command
- Undo command
- Find command

Browse Spreadsheet editor window

You use the Browse spreadsheet editor to perform the following tasks:

- Create a new property
- Copy a value from one property to another property
- Remove a user-defined property
- Replace property values

You can display the Browse spreadsheet editor from the project manager, schematic page editor, or the part editor.

From the project manager - Select the schematic design and select the Browse command from the Edit menu. You can select a component from the resulting popup menu. To display the Browse spreadsheet editor, select the component and click Properties from the Edit menu. You can change the properties of the following components from the Browse spreadsheet editor.

- Parts (including hierarchical blocks)
- Nets (including constituent nets within a bus) occurrences
- Flat Netlist
- Hierarchical ports
- Off-page connectors
- Title blocks
- Bookmarks
- DRC markers

From schematic page editor - Select the schematic page in the project manager and select the Browse command from the Edit menu. You can select a component from the resulting popup menu. To display the Browse spreadsheet editor, select the component and click Properties from the Edit menu. You can change the properties of the following components from the Browse spreadsheet editor.

- Parts (including hierarchical blocks)
- Nets (including constituent nets within a bus) occurrences
- Hierarchical ports
- Off-page connectors
- Title blocks
- Bookmarks
- DRC markers

From the part editor (while in Part View) - You can edit the following properties from the Browse spreadsheet editor:

- Pin properties

The Browse spreadsheet editor browses the entire design for the objects you select, then displays their properties. Each property appears as a column heading in the spreadsheet. Each row is an object located by the editor.

It is important to note that, in the Browse spreadsheet editor you can edit only occurrences. The only exception being in the part editor, where you can only edit instances. To edit instance properties, you must use the property editor.

Note: You can use the CTRL + C keys to copy a value from a cell and the CTRL + V keys to paste onto another cell in the Browse spreadsheet editor. Also, you can use the CTRL+ INSERT keys to copy a value from a cell in the Browse spreadsheet editor and paste it onto a cell in Microsoft Excel worksheet or use the SHIFT+ INSERT keys to paste values copied from Microsoft Excel onto a cell in the Browse spreadsheet editor.

Command Window

OrCAD Capture includes a scripting functionality that allows you to execute a Capture command through a command prompt in the Capture command window.

Every user action performed in Capture is logged in the form of a command. This command that logged is registered with a TCL interpreter. When the command is played back, Capture uses the TCL interpreter to retrieve the command and execute it in the resident application. However, this process is completely abstracted from the Capture. This makes logging and replaying of a set of commands an intuitive and simple task.

To execute a command, you type the command at the command prompt and press Enter.

Also, if you perform an operation in the Capture interface, the associated command is registered with the TCL interpreter and the command is logged in the Command window.

Finally, every command that is registered with the interpreter is logged in a captcl file. You can then use this file to re-run a complete

set of commands. You can do this from the Capture command window or from the Operating System command prompt by passing the script name (including location) as an argument to capture.

PCB Editor 3D Footprint Viewer

The PCB Editor 3D Footprint viewer provides a three dimensional view of the footprint symbol of a selected part on the schematic or the part editor. Along with the footprint symbol, the viewer also displays pin numbers and pin names.

When you select to view the footprint of a part, the footprint viewer displays the three dimensional view of PCB associated footprint. In the footprint viewer, selecting the footprint or a pin on the footprint queries for and displays the part or pint information at the top of the viewer.

The footprint in the viewer can be viewed from the following perspectives:

- Top
- Bottom
- Front
- Back
- Left
- Right
- Isometric (the angles between the projection of the x, y, and z axes are all the same, or 120°)

Besides the footprint views, the feature also includes a measure tool that allows you to measure an distance across the window.

You can also use the zoom in, zoom out and zoom fit features when viewing the footprint in the window.

Project Manager folders

The project manager is a tool that allows you to collect and organize all the resources you need for your project throughout the design flow. These resources include schematic pages, part libraries, and netlists, and may also include VHDL models, simulation models, timing files, stimulus files, and other related information.

When the project is first created, the project manager creates a design file with the same name as the project. It also creates a schematic folder within the design file, and a schematic page within the folder. You can create a new design to replace the design created by the project manager

Folder	Description
Design cache	A local library contained in each project that contains all the parts and symbols used in the design.
Library	Lists the library files and related files included in the current project. These files include library (*.OLB) files, simulation and synthesis (*.VHD) files, *.STL files, and *.SML files.
Outputs	Stores output files generated by Capture tools, such as Create Netlist, Design Rules Check, Cross reference reports, Bill of Materials, Export Properties, and Generate Part etc.
Referenced projects	Stores any projects referenced from within the current project. Typically, referenced projects are FPGA projects that you want to include in your PCB project. This is useful for board simulation that includes the appropriate timing and functionality information for an FPGA that is included in your printed circuit board.

Simulation resources	Contains simulation resources of your PCB designs which may include FPGA designs, as components. This folder can contain Verilog or VHDL simulation of your PCB designs. This folder is created when you choose the Board Simulation command from the Tools menu.

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Toolbar descriptions

The following is a set of descriptions for the toolbars and status bar.

You can move a toolbar anywhere on the screen by pressing the left mouse button over the toolbar not covered by a button, then moving the mouse to the toolbar's new location. If you move the toolbar to an edge of the session frame, it snaps into place along the side of the window. Otherwise, it floats on the screen wherever it is released. When you move the pointer over a button on the toolbar, Capture displays the name of the button in the form of a tool tip.

You can hide or display the toolbar by choosing the required toolbar from within the Toolbar submenu on the View menu. Alternatively, you can right-click on the menu bar and choose the required toolbar.

Viewing the toolbar

The toolbars provide easy access to common actions. Each toolbar contain buttons that related to the specific functional group, like Find toolbar or PSpice toolbar. If you need more clear space on the screen to view your work, you can hide the toolbar, then display it again when you wish to use one of the tools. All the tools on the toolbar are available as menu commands.

To display the toolbar

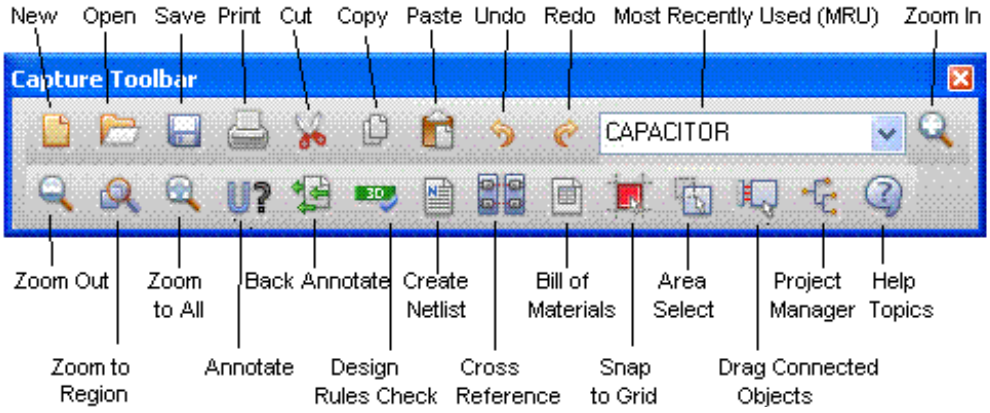
➤ From the View menu, choose Toolbar then choose the required toolbar from the submenu.

OR

➤ Right-click on the menu bar at the top of the Capture screen then choose the required toolbar.

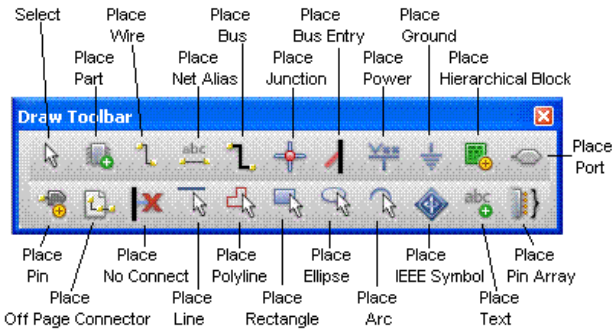
The Capture toolbar

The Capture toolbar provides shortcuts for many of the most frequently used generic Capture commands.



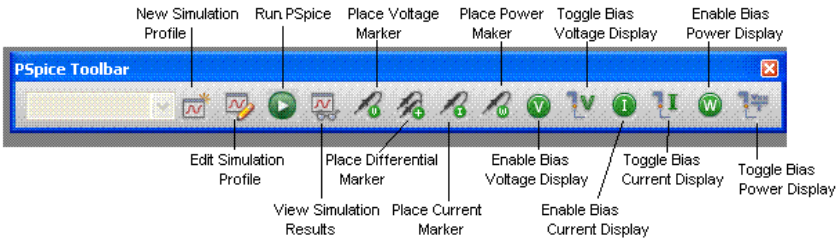
The Draw toolbar

The Draw Tool Palette provides shortcuts for commands to place components, pins, wires, bus, and drawing objects, such as arcs, polyline, ellipse, and text.



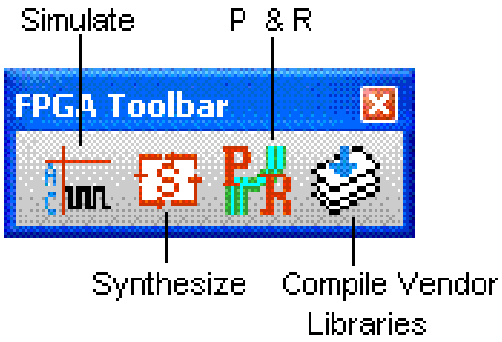
The Pspice toolbar

The PSpice toolbar provides shortcuts for many of the most frequently used PSpice commands.



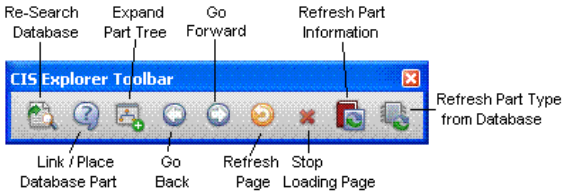
The FPGA toolbar

The FPGA toolbar offers a quick and easy way to simulate, synthesize, and compile vendor library projects. This toolbar is active only when you open a project of type Programmable Logic Design.



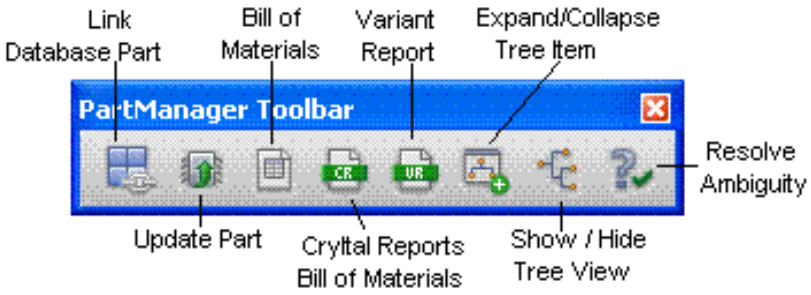
The CIS Explorer toolbar

The CIS Explorer toolbar offers a quick and easy way to perform common tasks. This toolbar is active only when you open OrCAD Capture CIS.



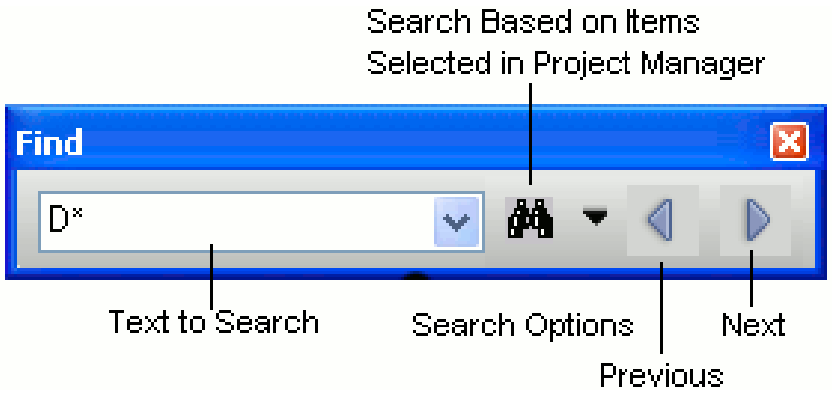
The Part Manager Explorer toolbar

The Part Manager toolbar offers a quick and easy way to perform common tasks. This toolbar is active only when you open OrCAD Capture CIS.



The Find toolbar

The Find toolbar provides shortcuts for the find functions available in Capture.



Viewing the status bar

The status bar appears at the bottom of the Capture window and reports on current actions, pointer location, and zoom scale. If you need more clear space on the screen to view your work, you can hide the status bar temporarily.

To display the status bar

➤ From the View menu, choose Status Bar.

A

VHDL and Verilog reserved words

VHDL reserved words

The 1076-93 VHDL standard lists the following reserved words. For complete information, see the specification and associated documents.

abs	access	after	alias	all
and	architecture	array	assert	attribute
begin	block	body	buffer	bus
case	component	configuration	constant	disconnect
downto	else	elsif	end	entity
exit	file	for	function	generate
guarded	if	in	inout	is
label	library	linkage	loop	map
mod	nand	new	next	nor
not	null	of	on	open
or	others	out	package	port
procedure	process	range	record	register
rem	report	return	select	severity

signal	subtype	then	to	transport
type	units	until	use	variable
wait	when	while	with	xor

Verilog reserved words

always	and	assign	begin	buf
bufif0	bufif1	case	casex	casez
cmos	deassign	default	defparam	disable
edge	else	end	endattribute	endcase
endmodule	endfunction	endprimitive	endspecify	endtable
endtask	event	for	force	forever
fork	function	highz0	highz1	if
initial	inout	input	integer	join
large	macromodule	medium	module	nand
negedge	negedge	nmos	nor	not
notif0	notif1	or	output	parameter
pmos	posedge	primitive	pull0	pull1
pullup	pulldown	rcmos	real	realtime
reg	release	repeat	rnmos	rpmos
rtran	rtranif0	rtranif1	scalared	signed
small	specify	specparam	strength	strong0
strong1	supply0	supply1	table	task
time	tran	tranif0	tranif1	tri
tri0	tri1	triand	trior	trireg
unsigned	vectored	wait	wand	weak0
weak1	while	wor	xnor	

B

NC VHDL and NC Verilog batch files

NC VHDL batch files

When you create a batch file for your NC VHDL simulation, it is best (and easiest) if you have already performed an interactive simulation run on your design, and you are confident that the simulation provides adequate coverage for your design. NC VHDL automatically creates log files for each step in the simulation process; specifically compilation, elaboration, and simulation.

The compilation log file, NCVHDL.LOG, contains information about the compilation of your design. An example compilation log file follows:

Example NCVHDL.LOG file

```
ncvhdl: v3.20.(p1): (c) Copyright 1995 - 2000 Cadence Design
Systems, Inc.
ncvhdl: *W,DLNOHV: Unable to find an 'hdl.var' file to load
in.
ncvhdl: v3.20.(p1): Started on Aug 10, 2001 at 11:16:27
```

ncvhdl
-work worklib
-cdslib E:/cad/junk4/cds.lib
-logfile ncvhdl.log
-errormax 15
-update
-v93
-messages
-status
E:/cad/junk4/PREP4.VHD
E:/cad/junk4/PREP4TB.VHD

...

In this example, the text in **bold** represents the compiler invocation and the associated options.

To create a batch file that replicates the compile run, copy the compiler invocation and the associated options into a text file. You can name the file anything you want, as long as it has a .BAT extension. So, for example, you might name the file SIMULATE.BAT.

It is best to include all the options on a single line, thusly:

```
ncvhdl -work worklib -cdslib ./cds.lib -logfile
ncvhdl.log -errormax 15 -update -v93 -messages -status
./design_file.VHD ./testbench_file.VHD
```

Note: Note that you should also change any "hard" paths in the file to dynamic paths, to facilitate using the batch file on different systems. For example, using the illustration above, the paths for the two .VHD files are changed from "hard" to dynamic when they are included in the batch file.

Similarly, you can include appropriate text from the elaboration and simulation log files in your batch file. Continuing with the example, an elaboration log file, NCELAB.LOG, might contain the following data:

Example NCELAB.LOG file

```
ncelab: v3.20.(p1): (c) Copyright 1995 - 2000 Cadence
Design Systems, Inc.
ncelab: *W,DLNOHV: Unable to find an 'hdl.var' file to
load in.
ncelab: v3.20.(p1): Started on Aug 10, 2001 at 11:16:37
```

ncelab
-work worklib
-cdslib E:/cad/junk4/cds.lib
-logfile ncelab.log
-errormax 15
-messages
-status
worklib.prep4tb:test_bench

...

A simulation log file, NCSIM.LOG, might contain the following data:

Example NCSIM.LOG file

```
ncsim: v3.20.(p1): (c) Copyright 1995 - 2000 Cadence
Design Systems, Inc.
ncsim: *W,DLNOHV: Unable to find an 'hdl.var' file to
load in.
ncsim: v3.20.(p1): Started on Aug 10, 2001 at 11:16:47
```

ncsim.dll
+cuzco_gui
-gui
-cdslib E:/cad/junk4/cds.lib
-logfile ncsim.log
-errormax 15
-messages
-status
worklib.prep4tb:test_bench

...

With simulation log files, before including the relevant text into your batch file, you should remove the .DLL extension from the invocation, as well as the +CUSCO_GUI option, thusly:

```
ncsim -gui -cdslib ./cds.lib -logfile ncsim.log -errormax 15
-messages -status
./worklib.testbench_file:test_bench
```

To complete the example, the illustration below shows a batch file, SIMULATE.BAT, that includes invocations (with associated options) for the compilation, elaboration, and simulation of a design:

Example batch file for NC VHDL

```
ncvhdl -work worklib -cdslib ./cds.lib -logfile ncvhdl.log
-errormax 15 -update -v93 -messages -status ./design_file.VHD
./testbench_file.VHD

ncelab -work worklib -cdslib ./cds.lib -logfile ncelab.log
-errormax 15 -messages -status
./worklib.testbench_file:test_bench

ncsim -gui -cdslib ./cds.lib -logfile ncsim.log -errormax 15
-messages -status
```

For the specifics of working with NC VHDL, please refer to your NC VHDL documentation.

C

PCB Editor netlist files

PSTCHIP.DAT

The PSTCHIP.DAT file contains a description for each physical part used in a Capture design. The Capture netlister extracts this physical description from properties on all occurrences rather than just instances.

File format

Here is the file format for the PSTCHIP.DAT file:

```
FILE_TYPE=LIBRARY_PARTS;
primitive 'Part Name';
pin
'Name':
PIN_NUMBER='(Number,Number...)';
INPUT_LOAD='(*)';
OUTPUT_LOAD='(*)';
OUTPUT_TYPE='(Type)';
PIN_GROUP='PinGroup';
.
.
.
end_pin;
body
POWER_PINS='(Power:Number;Ground:Number)';
PART_NAME='Source Package';
JEDEC_TYPE='PCB Footprint';
VALUE='Value';
NC_PINS='(Number,Number)';
Package (Component Definition) Property='occurrence_value;
.
.
.
end_body;
end_primitive;
END.
```

Explanation of file elements

PSTCHIP.DAT section	Description
Header	This line begins the PSTCHIP.DAT file by declaring the file type. A PSTCHIP.DAT file always starts with the FILE_TYPE=LIBRARY_PARTS statement.
primitive	A primitive is the description of the physical part.
Part Name	Concatenation of Source Package, PCB Footprint and other properties found in the [ComponentDefinitionProps] section of the configuration file used for netlisting.
pin	Starts the pin section.
Name	Pin name. There is a section for every pin name.
Number, Number...	The pin number for that pin name. If you have a multi-section part, then the pin numbers containing that pin name are separated by commas.
INPUT_LOAD	The netlister assigns this property to an input pin. The input local current is measured in milliamperes. If there is an output load on an output pin you get an OUTPUT_LOAD property.
OUTPUT_TYPE	Netlister assigns this property to define an output pin as open collector, open-emitter, or tri-state (3 state). This data is used to make sure all outputs on a net have the same output type. The OUTPUT_TYPE property also specifies the logic function created by tying the outputs together.
Type	Value of the output pin type when open collector, open emitter, 3 state.
PinGroup	This is taken from the PinGroup column in the part editor package property spreadsheet. To see the spreadsheet, from the Package menu choose View, then from the Properties menu choose Edit. This property only shows up in PSTCHIP.DAT if you have a positive value for PinGroup meaning that pin is swappable with the other input pins for that section in the multi-section part.

Power:Numbers; Ground:Numbers	This POWER_PINS line defines the default power and ground requirements for the physical part. Power or ground pins that need to be connected together on the board will share the same name. This syntax for this line is: name of your power pins (VCC for example):the numbers of the power pins; the name of the ground pins:the numbers of the ground pins
NC_PINS	Describes the pins not connected to the logic, but which are present in the physical package. Currently the netlister gets this value from an NC property added to the part and this property has a value of the pins you want to be no connects; these values are separated by commas. You can also cause this line to be generated if you put a no-connect symbol on a pin in the schematic. This property doesn't show up if you don't have any NC pins in your design.
Package (Component Definition) Property	Any property found in the property editor on a part that is specified as a property to use in the [ComponentDefinitionProps] section of the configuration file. Properties are separated by commas. The last property is followed by a semicolon. There can by any number of properties. PART_NAME, JEDEC_TYPE, and VALUE are always given in this section regardless of what is in the configuration file.
occurrence_value	The occurrence value of the property is given between the single quotation marks.

A sample PSTCHIP.DAT file

The PSTCHIP.DAT file contains one or more primitives, organized into a pin section and a body section. Here is an example:

```
FILE_TYPE=LIBRARY_PARTS;
{ Using PSTWRITER 14.0-p002 Oct-09-2000 at 10:32:05}
primitive 'OR14';
pin
'I0':
PIN_NUMBER='(1,4,9,12)';
INPUT_LOAD='(*)';
PIN_GROUP='1';
```

```
'I1':
PIN_NUMBER='(2,5,10,13)';
INPUT_LOAD='(*)';
PIN_GROUP='1';
'O':
PIN_NUMBER='(3,6,8,11)';
OUTPUT_LOAD='(*)';
end_pin;
body
POWER_PINS='(VCC:14)';
POWER_PINS='(GND:7)';
PART_NAME='74LS32_0';
CLASS='IC';
JEDEC_TYPE='dip14_3';
VALUE='74LS32';
end_body;
end_primitive;
primitive 'AND14';
pin
'I0':
PIN_NUMBER='(1,4,9,12)';
INPUT_LOAD='(*)';
PIN_GROUP='1';
'I1':
PIN_NUMBER='(2,5,10,13)';
INPUT_LOAD='(*)';
PIN_GROUP='1';
'O':
PIN_NUMBER='(3,6,8,11)';
OUTPUT_LOAD='(*)';
end_pin;
body
POWER_PINS='(VCC:14)';
POWER_PINS='(GND:7)';
PART_NAME='74LS08_0';
CLASS='IC';
JEDEC_TYPE='dip14_3';
VALUE='74LS08';
end_body;
end_primitive;
primitive '74LS04_IC_DIP14_3_74LS04';
pin
'I':
PIN_NUMBER='(1,3,5,9,11,13)';
INPUT_LOAD='(*)';
'O':
PIN_NUMBER='(2,4,6,8,10,12)';
OUTPUT_LOAD='(*)';
end_pin;
body
POWER_PINS='(VCC:14)';
POWER_PINS='(GND:7)';
PART_NAME='74LS04';
CLASS='IC';
JEDEC_TYPE='dip14_3';
VALUE='74LS04';
end_body;
end_primitive;
END.
```

PSTXNET.DAT

The PSTXNET.DAT file is the connectivity file. This file lists each net, its properties, its attached nodes, and node properties. The list is ordered by physical net name and contains all net properties and the logic-to-physical binding of nets and nodes.

File format

```
FILE_TYPE=EXPANDEDNETLIST;
NET_NAME
'Name'
'Canonical Path';
NODE_NAME Reference Number
'Canonical Path':
'Type':;
Net Property='occurrence_value',
.
.
. ;
END.
```

Explanation of file elements

PSTXNET.DAT section	Description
NET_NAME	Marks the beginning of a net entry. The net name entry always ends with a semicolon after the net property list.
'Name'	Name of the net or the value of the Name property. If you have a net alias, it is used as the name. This is the flat net name, so if a child schematic has a different name or alias than the same net on the root, the name or alias on the root is the one that gets used.
Canonical Path	The first canonical path uniquely identifies each net in your schematics. It contains your design name, schematic folders, name, and other identifiers.
NODE_NAME	Marks the beginning of a node entry. The node name entry always ends with a semicolon after the node property list.

Reference	The reference of the physical part.
Number	The pin number on the part attached to the net.
Canonical Path	The second canonical path uniquely identifies each part the net is attached to in your schematic pages. It contains your design name, schematic folders, ID, and other identifiers.
Type	Pin type of the pin attached to the net: input (I), output (O), bidirectional (IO), and so on.
Net Property	Any property found in the property editor that is specified as a property to use in the configuration file, [netprops] section. Properties are separated by commas. The last property in the list is followed by a semicolon. There can by any number of properties. An example would be ECL='TRUE';
occurrence_value	The occurrence value of the property is given between the single quotation marks.

Sample PSTXNET.DAT (expanded net list) file

```
FILE_TYPE = EXPANDEDNETLIST;
{ Using PSTWRITER 14.0-p002 Oct-09-2000 at 10:32:05 }
NET_NAME
'N00011'
'@FULLADD.FULLADD(SCH_1):N00011':
C_SIGNAL='@fulladd.fulladd(sch_1):n00011',
ECL='TRUE';
NODE_NAME U3 3
'@FULLADD.FULLADD(SCH_1):HALFADD_A@FULLADD.HALFADD(SCH_1):I5
05679612@TTL.74LS04.NORMAL(CHIPS)':
'I':;
NODE_NAME U2 4
'@FULLADD.FULLADD(SCH_1):HALFADD_A@FULLADD.HALFADD(SCH_1):I5
05679613@FULLADD.74LS08_0.NORMAL(CHIPS)':
'I0':;
NODE_NAME U2 9
'@FULLADD.FULLADD(SCH_1):HALFADD_A@FULLADD.HALFADD(SCH_1):I5
05679614@FULLADD.74LS08_0.NORMAL(CHIPS)':
'I0':;
NODE_NAME U1 8
'@FULLADD.FULLADD(SCH_1):HALFADD_B@FULLADD.HALFADD(SCH_1):I5
05679615@FULLADD.74LS32_0.NORMAL(CHIPS)':
'O':;
NET_NAME
'SUM'
'@FULLADD.FULLADD(SCH_1):SUM':
C_SIGNAL='@fulladd.fulladd(sch_1):sum';
NODE_NAME U1 6
```

```
'@FULLADD.FULLADD(SCH_1):HALFADD_A@FULLADD.HALFADD(SCH_1):I5
05679615@FULLADD.74LS32_0.NORMAL(CHIPS)':
 'O':;
NET_NAME
'X'
'@FULLADD.FULLADD(SCH_1):X':
C_SIGNAL='@fulladd.fulladd(sch_1):x';
NODE_NAME U3 5
'@FULLADD.FULLADD(SCH_1):HALFADD_B@FULLADD.HALFADD(SCH_1):I5
05679610@TTL.74LS04.NORMAL(CHIPS)':
'I':;
NODE_NAME U2 12
 '@FULLADD.FULLADD(SCH_1):HALFADD_B@FULLADD.HALFADD(SCH_1):I
505679611@FULLADD.74LS08_0.NORMAL(CHIPS)':
'I0':;
NODE_NAME U4 5
 '@FULLADD.FULLADD(SCH_1):HALFADD_B@FULLADD.HALFADD(SCH_1):I
505679614@FULLADD.74LS08_0.NORMAL(CHIPS)':
'I1':;
NET_NAME
'Y'
'@FULLADD.FULLADD(SCH_1):Y':
C_SIGNAL='@fulladd.fulladd(sch_1):y';
NODE_NAME U3 9
'@FULLADD.FULLADD(SCH_1):HALFADD_B@FULLADD.HALFADD(SCH_1):I5
05679612@TTL.74LS04.NORMAL(CHIPS)':
'I':;
NODE_NAME U4 1
'@FULLADD.FULLADD(SCH_1):HALFADD_B@FULLADD.HALFADD(SCH_1):I5
05679613@FULLADD.74LS08_0.NORMAL(CHIPS)':
'I0':;
NODE_NAME U4 4
'@FULLADD.FULLADD(SCH_1):HALFADD_B@FULLADD.HALFADD(SCH_1):I5
05679614@FULLADD.74LS08_0.NORMAL(CHIPS)':
'I0':;
NET_NAME
'CARRY_IN'
'@FULLADD.FULLADD(SCH_1):CARRY_IN':
C_SIGNAL='@fulladd.fulladd(sch_1):carry_in';
NODE_NAME U3 1
'@FULLADD.FULLADD(SCH_1):HALFADD_A@FULLADD.HALFADD(SCH_1):I5
05679610@TTL.74LS04.NORMAL(CHIPS)':
'I':;
NODE_NAME U2 1
'@FULLADD.FULLADD(SCH_1):HALFADD_A@FULLADD.HALFADD(SCH_1):I5
05679611@FULLADD.74LS08_0.NORMAL(CHIPS)':
'I0':;
NODE_NAME U2 10
'@FULLADD.FULLADD(SCH_1):HALFADD_A@FULLADD.HALFADD(SCH_1):I5
05679614@FULLADD.74LS08_0.NORMAL(CHIPS)':
'I1':;
NET_NAME
'N00013'
'@FULLADD.FULLADD(SCH_1):N00013':
C_SIGNAL='@fulladd.fulladd(sch_1):n00013';
NODE_NAME U1 1
'@FULLADD.FULLADD(SCH_1):I505679590@FULLADD.74LS32_0.NORMAL(
CHIPS)':
'I0':;
NODE_NAME U2 8
'@FULLADD.FULLADD(SCH_1):HALFADD_A@FULLADD.HALFADD(SCH_1):I5
```

```
05679614@FULLADD.74LS08_0.NORMAL(CHIPS)':
'O':;
NET_NAME
'N00023'
'@FULLADD.FULLADD(SCH_1):N00023':
C_SIGNAL='@fulladd.fulladd(sch_1):n00023';
NODE_NAME&#9;U1 2
'@FULLADD.FULLADD(SCH_1):I505679590@FULLADD.74LS32_0.NORMAL(
CHIPS)':
'I1':;
NODE_NAME U4 6
'@FULLADD.FULLADD(SCH_1):HALFADD_B@FULLADD.HALFADD(SCH_1):I5
05679614@FULLADD.74LS08_0.NORMAL(CHIPS)':
'O':;
NET_NAME
'CARRY_OUT'
'@FULLADD.FULLADD(SCH_1):CARRY_OUT':
C_SIGNAL='@fulladd.fulladd(sch_1):carry_out';
NODE_NAME&#9;U1 3
'@FULLADD.FULLADD(SCH_1):I505679590@FULLADD.74LS32_0.NORMAL(
CHIPS)':
'O':;
NET_NAME
'X_BAR'
'@FULLADD.FULLADD(SCH_1):X_BAR':
C_SIGNAL='@fulladd.fulladd(sch_1):x_bar';
NODE_NAME U3 2
'@FULLADD.FULLADD(SCH_1):HALFADD_A@FULLADD.HALFADD(SCH_1):I5
05679610@TTL.74LS04.NORMAL(CHIPS)':
'O':;
NODE_NAME U2 5
'@FULLADD.FULLADD(SCH_1):HALFADD_A@FULLADD.HALFADD(SCH_1):I5
05679613@FULLADD.74LS08_0.NORMAL(CHIPS)':
'I1':;
NET_NAME
'N5056796111'
'@FULLADD.FULLADD(SCH_1):N5056796111':
C_SIGNAL='@fulladd.fulladd(sch_1):n5056796111';
NODE_NAME U2 2
'@FULLADD.FULLADD(SCH_1):HALFADD_A@FULLADD.HALFADD(SCH_1):I5
05679611@FULLADD.74LS08_0.NORMAL(CHIPS)':
'I1':;
NODE_NAME U3 4
'@FULLADD.FULLADD(SCH_1):HALFADD_A@FULLADD.HALFADD(SCH_1):I5
05679612@TTL.74LS04.NORMAL(CHIPS)':
'O':;
NET_NAME
'N00032'
'@FULLADD.FULLADD(SCH_1):N00032':
C_SIGNAL='@fulladd.fulladd(sch_1):n00032';
NODE_NAME U2 3
'@FULLADD.FULLADD(SCH_1):HALFADD_A@FULLADD.HALFADD(SCH_1):I5
05679611@FULLADD.74LS08_0.NORMAL(CHIPS)':
'O':;
NODE_NAME U1 4
'@FULLADD.FULLADD(SCH_1):HALFADD_A@FULLADD.HALFADD(SCH_1):I5
05679615@FULLADD.74LS32_0.NORMAL(CHIPS)':
'I0':;
NET_NAME
'N00034'
'@FULLADD.FULLADD(SCH_1):N00034':
```

```
C_SIGNAL='@fulladd.fulladd(sch_1):n00034';
NODE_NAME U1 5
'@FULLADD.FULLADD(SCH_1):HALFADD_A@FULLADD.HALFADD(SCH_1):I5
05679615@FULLADD.74LS32_0.NORMAL(CHIPS)':
'I1':;
NODE_NAME U2 6
'@FULLADD.FULLADD(SCH_1):HALFADD_A@FULLADD.HALFADD(SCH_1):I5
05679613@FULLADD.74LS08_0.NORMAL(CHIPS)':
'O':;
NET_NAME
'X_BAR_74'
'@FULLADD.FULLADD(SCH_1):X_BAR_74':
C_SIGNAL='@fulladd.fulladd(sch_1):x_bar_74';
NODE_NAME U3 6
'@FULLADD.FULLADD(SCH_1):HALFADD_B@FULLADD.HALFADD(SCH_1):I5
05679610@TTL.74LS04.NORMAL(CHIPS)':
'O':;
NODE_NAME U4 2
'@FULLADD.FULLADD(SCH_1):HALFADD_B@FULLADD.HALFADD(SCH_1):I5
05679613@FULLADD.74LS08_0.NORMAL(CHIPS)':
 'I1':;
NET_NAME
'N5056796111_76'
'@FULLADD.FULLADD(SCH_1):N5056796111_76':
C_SIGNAL='@fulladd.fulladd(sch_1):n5056796111_76';
NODE_NAME U2 13
'@FULLADD.FULLADD(SCH_1):HALFADD_B@FULLADD.HALFADD(SCH_1):I5
05679611@FULLADD.74LS08_0.NORMAL(CHIPS)':
'I1':;
NODE_NAME U3 8
'@FULLADD.FULLADD(SCH_1):HALFADD_B@FULLADD.HALFADD(SCH_1):I5
05679612@TTL.74LS04.NORMAL(CHIPS)':
'O':;
NET_NAME
'N00032_77'
'@FULLADD.FULLADD(SCH_1):N00032_77':
C_SIGNAL='@fulladd.fulladd(sch_1):n00032_77';
NODE_NAME U2 11
'@FULLADD.FULLADD(SCH_1):HALFADD_B@FULLADD.HALFADD(SCH_1):I5
05679611@FULLADD.74LS08_0.NORMAL(CHIPS)':
'O':;
NODE_NAME U1 9
'@FULLADD.FULLADD(SCH_1):HALFADD_B@FULLADD.HALFADD(SCH_1):I5
05679615@FULLADD.74LS32_0.NORMAL(CHIPS)':
'I0':;
NET_NAME
'N00034_79'
'@FULLADD.FULLADD(SCH_1):N00034_79':
C_SIGNAL='@fulladd.fulladd(sch_1):n00034_79';
NODE_NAME U1 10
'@FULLADD.FULLADD(SCH_1):HALFADD_B@FULLADD.HALFADD(SCH_1):I5
05679615@FULLADD.74LS32_0.NORMAL(CHIPS)':
'I1':;
NODE_NAME U4 3
'@FULLADD.FULLADD(SCH_1):HALFADD_B@FULLADD.HALFADD(SCH_1):I5
05679613@FULLADD.74LS08_0.NORMAL(CHIPS)':
'O':;
END.
```

PSTXPRT.DAT

The PSTXPRT.DAT file (the expanded part list) lists each reference designator and the sections assigned to it. The PSTXPRT.DAT file is ordered by reference designator and section number.

File format

```
FILE_TYPE = EXPANDEDPARTLIST;
DIRECTIVES
PST_VERSION='PST_HDL_CENTRIC_VERSION_0';
ROOT_DRAWING = 'Root schematic folder of design' ;
POST_TIME = 'Date and Time of Netlist' ;
SOURCE_TOOL='Capture_Writer';
END_DIRECTIVES ;
PART_NAME
Part Reference ’PART NAME’;
ComponentInstanceProperty='occurence_value';
.
.
SECTION_NUMBER #
'Canonical path',
'Physical path',
Part(function) property='occurrence_value',
.
.
.
PRIM_FILE='.\pstchip.dat',
SECTION='designator';
END.
```

Explanation of file elements

PSTXPRT.DAT section	Description
DIRECTIVES	Marks the beginning of the directives section. Directives always end with a semicolon.
PST_VERSION	Version of PCB Editor interface.
ROOT_DRAWING	Root schematic folder of design in Capture.
POST_TIME	Date and time of netlist.
SOURCE_TOOL	Tool used is Capture Writer or Design Entry HDL Writer.

END_DIRECTIVES	Marks the end of the Directives section.
Part Reference	The reference designator name of the physical part.
ComponentInstanceProperty	Properties and values of any component instance (package) properties found on the part and listed in the configuration file under the [ComponentInstanceProperty] section.
PART NAME	Concatenation of Source Package, PCB Footprint, and other properties found in the [ComponentDefinitionProps] section of the configuration file used for netlisting.
SECTION_NUMBER #	Marks the beginning of a physical section number. Each section of the package used gets its own section number. Single section parts have only one section number.
Canonical path	The canonical path uniquely identifies each part in your schematic pages. It contains your design name, schematic folders, part ID, source part, implementation type, and other identifiers.
Physical path	The physical path uniquely identifies each part in a design. The physical path contains the design name, schematic folder, page number, part ID, source part, implementation type, and other identifiers specific to the selected part in the design.
Part (function) property	Any property found in the property editor that is specified as a property to use in the configuration file, [functionprops] section. Properties are separated by commas. The last property in the list is followed by a semicolon. There can by any number of properties.

occurrence_value	The occurrence value of the property is given between the single quotation marks.
PRIM_FILE	Location of the where package properties are listed. This is the PSTCHIP.DAT file which is closely linked to the PSTXPRT.DAT file.
designator	The designator is now stored so that we know if designators are numeric or alphabetic.

Sample PSTXPRT.DAT file

```
FILE_TYPE = EXPANDEDPARTLIST;
{ Using PSTWRITER 16.5.0 p001Apr-05-2011 at 10:09:06 }
DIRECTIVES
 PST_VERSION='PST_HDL_CENTRIC_VERSION_0';
 ROOT_DRAWING='FULLADD';
 POST_TIME='Mar 29 2011 00:05:38';
 SOURCE_TOOL='CAPTURE_WRITER';
END_DIRECTIVES;

PART_NAME
 U1 'ORGATE':;

SECTION_NUMBER 1

'@FULLADD.FULLADD(SCH_1):I505679590@FULLADD.74LS32.NORMAL(CH
IPS)':

C_PATH='@fulladd.fulladd(sch_1):i505679590@fulladd.\74ls32.n
ormal\(chips)',

P_PATH='@fulladd.fulladd(sch_1):page1_i505679590@fulladd.\74
ls32.normal\(chips)',
 PRIM_FILE='.\pstchip.dat',
 SECTION='A';

SECTION_NUMBER 2

'@FULLADD.FULLADD(SCH_1):HALFADD_A@FULLADD.HALFADD(SCH_1):I5
05679615@FULLADD.74LS32.NORMAL(CHIPS)':

C_PATH='@fulladd.fulladd(sch_1):halfadd_a@fulladd.halfadd(sc
h_1):i505679615@fulladd.\74ls32.normal\(chips)',

P_PATH='@fulladd.fulladd(sch_1):page1_halfadd_a@fulladd.half
add(sch_1):page2_i505679615@fulladd.\74ls32.normal\(chips)',
 PRIM_FILE='.\pstchip.dat',
 SECTION='B';

SECTION_NUMBER 3
```

```
'@FULLADD.FULLADD(SCH_1):HALFADD_B@FULLADD.HALFADD(SCH_1):I5
05679615@FULLADD.74LS32.NORMAL(CHIPS)':

C_PATH='@fulladd.fulladd(sch_1):halfadd_b@fulladd.halfadd(sc
h_1):i505679615@fulladd.\74ls32.normal\(chips)',

P_PATH='@fulladd.fulladd(sch_1):page1_halfadd_b@fulladd.half
add(sch_1):page2_i505679615@fulladd.\74ls32.normal\(chips)',
 PRIM_FILE='.\pstchip.dat',
 SECTION='C';

PART_NAME
 U2 'ANDGATE':;

SECTION_NUMBER 1

'@FULLADD.FULLADD(SCH_1):HALFADD_A@FULLADD.HALFADD(SCH_1):I5
05679611@FULLADD.74LS08.NORMAL(CHIPS)':

C_PATH='@fulladd.fulladd(sch_1):halfadd_a@fulladd.halfadd(sc
h_1):i505679611@fulladd.\74ls08.normal\(chips)',

P_PATH='@fulladd.fulladd(sch_1):page1_halfadd_a@fulladd.half
add(sch_1):page2_i505679611@fulladd.\74ls08.normal\(chips)',
 PRIM_FILE='.\pstchip.dat',
 SECTION='A';


SECTION_NUMBER 2

'@FULLADD.FULLADD(SCH_1):HALFADD_A@FULLADD.HALFADD(SCH_1):I5
05679613@FULLADD.74LS08.NORMAL(CHIPS)':

C_PATH='@fulladd.fulladd(sch_1):halfadd_a@fulladd.halfadd(sc
h_1):i505679613@fulladd.\74ls08.normal\(chips)',

P_PATH='@fulladd.fulladd(sch_1):page1_halfadd_a@fulladd.half
add(sch_1):page2_i505679613@fulladd.\74ls08.normal\(chips)',
 PRIM_FILE='.\pstchip.dat',
 SECTION='B';

SECTION_NUMBER 3

'@FULLADD.FULLADD(SCH_1):HALFADD_A@FULLADD.HALFADD(SCH_1):I5
05679614@FULLADD.74LS08.NORMAL(CHIPS)':

C_PATH='@fulladd.fulladd(sch_1):halfadd_a@fulladd.halfadd(sc
h_1):i505679614@fulladd.\74ls08.normal\(chips)',

P_PATH='@fulladd.fulladd(sch_1):page1_halfadd_a@fulladd.half
add(sch_1):page2_i505679614@fulladd.\74ls08.normal\(chips)',
 PRIM_FILE='.\pstchip.dat',
 SECTION='C';

SECTION_NUMBER 4

'@FULLADD.FULLADD(SCH_1):HALFADD_B@FULLADD.HALFADD(SCH_1):I5
05679611@FULLADD.74LS08.NORMAL(CHIPS)':
```

```
C_PATH='@fulladd.fulladd(sch_1):halfadd_b@fulladd.halfadd(sc
h_1):i505679611@fulladd.\74ls08.normal\(chips)',

P_PATH='@fulladd.fulladd(sch_1):page1_halfadd_b@fulladd.half
add(sch_1):page2_i505679611@fulladd.\74ls08.normal\(chips)',
 PRIM_FILE='.\pstchip.dat',
 SECTION='D';

PART_NAME
 U3 'NOTGATE':;

SECTION_NUMBER 1

'@FULLADD.FULLADD(SCH_1):HALFADD_A@FULLADD.HALFADD(SCH_1):I5
05679610@FULLADD.74LS04.NORMAL(CHIPS)':

C_PATH='@fulladd.fulladd(sch_1):halfadd_a@fulladd.halfadd(sc
h_1):i505679610@fulladd.\74ls04.normal\(chips)',

P_PATH='@fulladd.fulladd(sch_1):page1_halfadd_a@fulladd.half
add(sch_1):page2_i505679610@fulladd.\74ls04.normal\(chips)',
 PRIM_FILE='.\pstchip.dat',
 SECTION='A';

SECTION_NUMBER 2

'@FULLADD.FULLADD(SCH_1):HALFADD_A@FULLADD.HALFADD(SCH_1):I5
05679612@FULLADD.74LS04.NORMAL(CHIPS)':

C_PATH='@fulladd.fulladd(sch_1):halfadd_a@fulladd.halfadd(sc
h_1):i505679612@fulladd.\74ls04.normal\(chips)',

P_PATH='@fulladd.fulladd(sch_1):page1_halfadd_a@fulladd.half
add(sch_1):page2_i505679612@fulladd.\74ls04.normal\(chips)',
 PRIM_FILE='.\pstchip.dat',
 SECTION='B';

SECTION_NUMBER 3

'@FULLADD.FULLADD(SCH_1):HALFADD_B@FULLADD.HALFADD(SCH_1):I5
05679610@FULLADD.74LS04.NORMAL(CHIPS)':

C_PATH='@fulladd.fulladd(sch_1):halfadd_b@fulladd.halfadd(sc
h_1):i505679610@fulladd.\74ls04.normal\(chips)',

P_PATH='@fulladd.fulladd(sch_1):page1_halfadd_b@fulladd.half
add(sch_1):page2_i505679610@fulladd.\74ls04.normal\(chips)',
 PRIM_FILE='.\pstchip.dat',
 SECTION='C';

SECTION_NUMBER 4

'@FULLADD.FULLADD(SCH_1):HALFADD_B@FULLADD.HALFADD(SCH_1):I5
05679612@FULLADD.74LS04.NORMAL(CHIPS)':

C_PATH='@fulladd.fulladd(sch_1):halfadd_b@fulladd.halfadd(sc
h_1):i505679612@fulladd.\74ls04.normal\(chips)',
```

```
P_PATH='@fulladd.fulladd(sch_1):page1_halfadd_b@fulladd.half
add(sch_1):page2_i505679612@fulladd.\74ls04.normal\(chips)',
 PRIM_FILE='.\pstchip.dat',
 SECTION='D';

PART_NAME
 U4 'ANDGATE':;

SECTION_NUMBER 1

'@FULLADD.FULLADD(SCH_1):HALFADD_B@FULLADD.HALFADD(SCH_1):I5
05679613@FULLADD.74LS08.NORMAL(CHIPS)':

C_PATH='@fulladd.fulladd(sch_1):halfadd_b@fulladd.halfadd(sc
h_1):i505679613@fulladd.\74ls08.normal\(chips)',

P_PATH='@fulladd.fulladd(sch_1):page1_halfadd_b@fulladd.half
add(sch_1):page2_i505679613@fulladd.\74ls08.normal\(chips)',
 PRIM_FILE='.\pstchip.dat',
 SECTION='A';

SECTION_NUMBER 2

'@FULLADD.FULLADD(SCH_1):HALFADD_B@FULLADD.HALFADD(SCH_1):I5
05679614@FULLADD.74LS08.NORMAL(CHIPS)':

C_PATH='@fulladd.fulladd(sch_1):halfadd_b@fulladd.halfadd(sc
h_1):i505679614@fulladd.\74ls08.normal\(chips)',

P_PATH='@fulladd.fulladd(sch_1):page1_halfadd_b@fulladd.half
add(sch_1):page2_i505679614@fulladd.\74ls08.normal\(chips)',
 PRIM_FILE='.\pstchip.dat',
 SECTION='B';

END.
```

D

SDT configuration files

Capture requires either an SDT.CFG file or an SDT.BCF file when translating SDT designs into Capture. If you don't have one of these files, you can create an SDT.CFG in a text editor using the sample file provided here.

You may need to edit the following items in your SDT.CFG file to insure correct importation of your schematic folders:

- Path and libraries
- Page dimensions and units
- Part fields

After you finish editing the SDT.CFG file, save it in the directory where you keep your SDT schematic folders. Capture will use the SDT.CFG file to locate the libraries and parts needed to translate your schematic folders.

Path and libraries

The PLIB= line in the SDT.CFG file specifies the exact path to the SDT libraries (.LIB files). Each library must be specified by a LIB= line. Make only one 'PLIB=' line in your SDT.CFG file. Make one 'LIB=' line for each library your SDT schematic folders use. If you keep your SDT libraries in the same directory as your SDT schematic folder, use the following lines in the SDT.CFG (where pathname specifies the directory path where the .LIB files are located, and filename specifies the name of one .LIB file):

```
PLIB = 'pathname\*.LIB'
LIB = '.\filename.LIB'
```

Page dimensions and units

If design is in metric units, replace the corresponding lines above with those found below:

```
HOR = 264000 374300 548300 795300 1143300
VRT = 177000 264000 374300 548300 795300
P2P = 2540 2540 2540 2540 2540
UNTS = 'METRIC'
```

Part fields

Use part field lines in the SDT.CFG file to map properties and values of parts from SDT to Capture. The eighth part field is typically reserved for the PCB footprint.

Sample SDT.CFG file

The following is a sample SDT.CFG file:

```
PLIB = 'C:\ORCADESP\SDT\LIBRARY\*.LIB'
LIB = 'TTL.LIB' Design library filename
FN1 = '1ST PART FIELD'
FN2 = '2ND PART FIELD'
FN3 = '3RD PART FIELD'
FN4 = '4TH PART FIELD'
FF5 = '5TH PART FIELD'
FN6 = '6TH PART FIELD'
FN7 = '7TH PART FIELD'
FN8 = 'PCB Footprint'
HOR = 9700 17000 20200 32200 42200
VRT = 7200 11000 15200 20200 32200
P2P = 100 100 100 100 100
SIZ = 'B'
UNTS = 'ENGLISH'
ATB = 0
```

E

Netlist examples

This chapter provides a brief overview of some of the netlist formats available from Capture.

Accel netlist format

The Accel PCB format netlists from ACCEL Technologies have these characteristics:

- All ASCII characters are legal.

For more information, see the ACCEL Technologies website or the Protel website.

Example

```
(compinst "Y1"
(patternName "10MHz")
(compvalue "10MHz "))
(compinst "Y2"
(patternName "DIP.100/14/W.300/L.800")
(compvalue "24.576MHz"))
(compinst "Y3"
(patternName "4.9152MHz")
(compvalue "4.9152MHz"))
(compinst "Y4"
(patternName "3.6864MHz")
(compvalue "3.6864MHz"))
(net "N03627"
(node "JP5" "26")
(node "R43" "2"))
(net "N08082"
(node "L1" "2")
(node "C8" "1")
(node "L2" "1"))
(net "N03663"
(node "U72" "1")
(node "R53" "2"))
(net "N08139"
(node "L6" "2")
(node "C19" "1")
```

```
(node "R20" "1")
(node "C15" "2"))
```

Algorex netlist format

The Algorex format has these characteristics:

- Part names, module names, reference strings, node names, and pin numbers are not checked for length.
- Node numbers are limited to six digits following the "N" prefix.
- Pin names are not used.

All ASCII characters are legal.

Example

```
GND
U1 (14DIP300)-7,
U2 (14DIP300)-7
VCC
U1 (14DIP300)-14,
U2 (14DIP300)-14
CLOCK
U1 (14DIP300)-10
Q
U1 (14DIP300)-6,
U2 (14DIP300)-2,
U1 (14DIP300)-9
OUT
U2 (14DIP300)-3
B
U1 (14DIP300)-4
N00019
U1 (14DIP300)-3,
U2 (14DIP300)-1
N00013
U1 (14DIP300)-5,
U1 (14DIP300)-8
A
U1 (14DIP300)-1,
U1 (14DIP300)-2
```

Altera ADF netlist format

The AlteraADF format has these characteristics:

- Part names, module names, reference strings, node names, and pin numbers are not checked for length.
- All ASCII characters are legal.

Altera netlist constraints

When you create an AlteraADF netlist, you must include the OrCAD-supplied ALTERA_P.OLB and ALTERA_M.OLB libraries in your project. You can use only the parts in these two libraries to create the schematic design.

Inputs and outputs are handled differently in Capture and the Altera software. Capture defines inputs and outputs with hierarchical ports and library objects. Altera defines inputs and outputs with a library object, which is then tagged with the appropriate pin number. In the example schematic page, the CLOCK signal is an input and the STROBE signal is an output.

Additionally, library objects with unused pins default to predefined levels in the Altera software. Because Capture does not default unconnected pins to any particular level, you must tie all unused pins to the appropriate level.

Altera pipe commands

You can place equations in your schematic folder to be included in the netlist. To place these equations on the schematic page, choose the Text command from the Place menu.

Each equation must start with the pipe character (|). The first line must be:

```
|EQUATIONS
```

This tells Capture that some AlteraADF equations need to be included in the netlist. The equations can contain any information you want to include in the netlist.

Altera title block information

Title block information is placed in the first 10 lines of the netlist. The following table shows an example netlist header and the title block

information from which the header was extracted. Header information in bold is text entered in the schematic page's title block.
i

Line	Example header	Title block field
1	ADF Example	Title of schematic page
1	May 15, 2002	Date
2	OrCAD-02	Document number
2	A	Revision code
3	OrCAD	Organization name
4	9300 SW Nimbus Avenue	1st Address Line
6	Turbo = ON	3rd Address Line
7	5C031	4th Address Line

Example

```
ADF Example Revised: Friday, November 13, 1998
OrCAD-02 Revision: A
OrCAD
9300 S.W. Nimbus Ave.

TURBO = ON
5C031

OPTIONS:TURBO = ON
PART:5C031

INPUTS:
CLOCK
ENABLE
COINDROP
CUPFULL
RESET

OUTPUTS:
STROBE
POURDRNK
DROPCUP

NETWORK:
```

```
J=INP(ENABLE) % SYM 1 %
N=INP(CUPFULL) % SYM 2 %
O=OR(P,Q) % SYM 3 %
POURDRNK,E=RORF(O,D,H,I,J) % SYM 4 %
Q=AND(F,R) % SYM 5 %
R=NOT(E) % SYM 6 %
B=XOR(E,F) % SYM 7 %
A=AND(B,C) % SYM 8 %
STROBE=CONF(A,VCC) % SYM 9 %
C=NOT(D) % SYM 10 %
D=INP(CLOCK) % SYM 11 %
H=AND(F,E) % SYM 12 %
I=INP(RESET) % SYM 13 %
G=AND(K,L,M) % SYM 14 %
DROPCUP,F=RORF(G,D,H,I,J) % SYM 15 %
M=INP(COINDROP) % SYM 16 %
K=NOT(F) % SYM 17 %
P=AND(K,E,L) % SYM 18 %
L=NOT(N) % SYM 19 %

EQUATIONS:
G = (K & L & M);
H = (F & E);
O = (P # Q);
END$
```

AppliconBRAVO netlist format

AppliconBRAVO netlists have the following characteristics:

- Part names, module names, reference strings, node names, and pin numbers are not checked for length.
- Node numbers are limited to five digits following the "N" prefix.
- Pin names are not used.
- All ASCII characters are legal.

Example

```
*** Desig 14DIP300
U1
*** Desig 14DIP300
U2
** NET GND
U1 7
U2 7
*** NET VCC
U1 14
U2 14
*** NET CLOCK
U1 10
*** NET Q
```

```
U1 6
U2 2
U1 9
*** NET OUT
U2 3
** NET B
U1 4
*** NET N00019
U1 3
U2 1
*** NET N00013
U1 5
U1 8
*** NET A
U1 1
U1 2
```

AppliconLEAP netlist format

AppliconLEAP netlists have the following characteristics:

- Part names, module names, reference strings, node names, and pin numbers are not checked for length.
- Node numbers are limited to five digits following the "N" prefix.
- Pin names are not used.
- All ASCII characters are legal.

See the AppliconLEAP netlist format example for more information.

Example

```
*** NET GND
U1 7 14DIP300
U2 7 14DIP300
*** NET VCC
U1 14 14DIP300
U2 14 14DIP300
*** NET CLOCK
U1 10 14DIP300
*** NET Q
U1 6 14DIP300
U2 2 14DIP300
U1 9 14DIP300
*** NET OUT
U2 3 14DIP300
*** NET B
U1 4 14DIP300
*** NET N00019
U1 3 14DIP300
U2 1 14DIP300
** NET N00013
```

```
1 5 14DIP300
1 8 14DIP300
*** NET A
U1 1 14DIP300
U1 2 14DIP300
```

Cadnetix netlist format

Cadnetix netlists have the following characteristics:

- Part names can contain up to 17 characters.
- Module names can contain up to 15 characters.
- Reference strings plus pin numbers can contain up to 12 characters.
- Node names can contain up to 16 characters.
- Pin numbers can contain up to three digits.
- Pin names are not used.
- Node numbers are not checked for length.
- All ASCII characters are legal.

Example

```
PARTS LIST
74LS00 14DIP300 U1
74LS32 14DIP300 U2
EOS
NET LIST
NODENAME GND $
U1 7 U2 7
NODENAME VCC $
U1 14 U2 14
NODENAME CLOCK $
U1 10
NODENAME Q $
U1 6 U2 2 U1 9
NODENAME OUT $
U2 3
NODENAME B $
U1 4
NODENAME N00019 $
U1 3 U2 1
NODENAME N00013 $
U1 5 U1 8
NODENAME A $
U1 1 U1 2
EOS
```

Calay netlist format

This is the older of two Calay netlists formats. The newer Calay format is Calay 90.

Calay netlists have the following characteristics:

- Part names, module names, and reference strings can each contain up to 19 characters.
- Node names can contain up to eight characters. Legal characters for node names are:

  + - 0..9 A..Z a..z
- Node numbers are limited to five digits following the "N" prefix.
- Pin names are not used.
- Pin numbers are not checked for length.
- All ASCII characters are legal except as noted for node names.

Example

Calay netlists normally have a .NET file extension.

```
/GND U1(7) U2(7);
/VCC U1(14) U2(14);
/CLOCK U1(10);
/Q U1(6) U2(2) U1(9);
/OUT U2(3);
/B U1(4);
/N00019 U1(3) U2(1);
/N00013 U1(5) U1(8);
/A U1(1) U1(2);
```

Calay90 netlist format

The Calay 90 format creates two files: the netlist file and a component file. You must enter the component filename in the appropriate text box in the Create Netlist dialog box. Calay 90 netlists have the following characteristics:

- Part names, module names, and reference strings can each contain up to 19 characters.

- Node names can contain up to eight characters. Legal characters for node names are:

  + - 0..9 A..Z a..z

- Node numbers are limited to five digits following the "N" prefix.
- Pin names are not used.
- Pin numbers are not checked for length.
- All ASCII characters are legal except as noted for node names.

Example

```
GND U1('7) U2('7);
VCC U1('14) U2('14);
CLOCK U1('10);
Q U1('6) U2('2) U1('9);
OUT U2('3);
B U1('4);
N00019 U1('3) U2('1);
N00013 U1('5) U1('8);
A U1('1) U1('2);
```

Case netlist format

Sophia Systems & Technologies CASE netlists have the following characteristics:

- Part names, module names, reference strings, node names, and pin numbers are not checked for length.
- Node numbers are limited to five digits following the "N" prefix.
- Pin names are not used.
- All ASCII characters are legal except as noted for node names.

Example

```
ASSERTIONS=OFF;VERSION=400;LOCATION=LOC;
[SIZE=1;TIMES=1;LOC=(U1);PLOC=U1;SHAPE=14DIP300]
1=A;
2=A;
3=N00019;
4=B;
5=N00013;
6=Q;
7=GND;
```

```
8=N00013;
9=Q;
10=CLOCK;
11=NC;
12=NC;
13=NC;
14=VCC;
;
[SIZE=1;TIMES=1;LOC=(U2);PLOC=U2;SHAPE=14DIP300]
1=N00019;
2=Q;
3=OUT;
4=NC;
5=NC;
6=NC;
7=GND;
8=NC;
9=NC;
10=NC;
11=NC;
12=NC;
13=NC;
14=VCC;
;
;
```

CBDS netlist format

BNR CBDS netlists have the following characteristics:

- Part names, module names, reference strings, and pin numbers are not checked for length.
- Node names can contain up to 20 characters. These characters are legal:

  / - 0..9 a..z A..Z
- Node numbers are limited to five digits following the "N" prefix.
- Pin names are not used.
- All ASCII characters are legal except as noted for node names.

Example

```
.SEARCH P,C
.DD U1 14DIP300
.DD U2 14DIP300
.S,GND,U1,7,U2,7
.S,VCC,U1,14,U2,14
.S,CLOCK,U1,10
.S,Q,U1,6,U2,2,U1,9
```

```
.S,OUT,U2,3
.S,B,U1,4
.S,N00019,U1,3,U2,1
.S,N00013,U1,5,U1,8
.S,A,U1,1,U1,2
```

Computervision netlist format

ComputerVision CADDS3 and CADDS4X netlists have the following characteristics:

- Part names, module names, reference strings, and pin numbers are not checked for length.
- Node names can contain up to 19 characters.
- Node numbers are limited to five digits following the "N" prefix.
- Pin names are not used.
- All ASCII characters are legal except as noted for node names.

Example

```
0001 GND U1-7 U2-7
0002 VCC U1-14 U2-14
0003 CLOCK U1-10
0004 Q U1-6 U2-2 U1-9
0005 OUT U2-3
0006 B U1-4
0007 N00019 U1-3 U2-1
0008 N00013 U1-5 U1-8
0009 A U1-1 U1-2
```

DUMP netlist format

This format produces a flat netlist containing all the information on the schematic pages. No information is omitted or changed. You can use this netlist format when troubleshooting a design.

EDIF 2 0 0 netlist format

EEDesigner netlists have the following characteristics:

- Part names, module names, reference strings, node names, and pin numbers are not checked for length.

- Node numbers are limited to five digits following the "N" prefix.
- Legal characters are:

  0..9 a..z A..Z _(underscore)

  Case is not significant. When Capture encounters an illegal character, it issues a warning and makes the following changes:

  - Changes "-" to "MINUS"
  - Changes "+" to "PLUS"
  - Changes "\" and "/" to "BAR"
  - Changes all other illegal characters to "_"

EDIF 2 0 0 formats

Capture provides two EDIF netlist formats. The first format produces either hierarchical or flat netlist output, depending on your design structure and the active mode. It is accessible from the EDIF 2 0 0 tab in the Create Netlist dialog box. The second format produces only flat netlists, and is accessible through the Other tab in the Create Netlist dialog box.

Use the EDIF 2 0 0 tab if:

- You want to include net, pin, or part properties in the netlist.
- You want a hierarchical netlist.

Use the Other tab if:

- You want a flat netlist for a simple hierarchical design.

Hierarchical designs in EDIF

Capture manages the hierarchy by defining pages in the schematic folder as CELLs in the main LIBRARY. These cells can then be referred to by INSTANCE where needed. Because EDIF requires a define-before-use philosophy, the hierarchy appears to be inverted in the netlist (the root schematic page is the last CELL in the main LIBRARY).

Note: Some of the options specific to the EDIF netlist format are included to support PC Board Layout Tools 386+. If you are creating a netlist for use with PCB 386+, be sure to select the Allow non-EDIF characters option.

Example flat netlist

```
(edif (rename &FIG_BMINUS01 "FIG_B-01")
(edifVersion 2 0 0)
(edifLevel 0)
(keywordMap (keywordLevel 0))
(status
(written
(timeStamp 0 0 0 0 0 0)
(program "EDIF.DLL")
(comment "Original data from OrCAD CAPTURE schematic"))
(comment "Generic Netlist Example")
(comment "Thursday, November 12, 1998")
(comment "OrCAD-01")
(comment "A")
(comment "OrCAD")
(comment "9300 S.W. Nimbus Ave.")
(comment "Beaverton, OR 97008")
(comment "(503) 671-9500 Corporate Offices")
(comment "(503) 671-9400 Technical Support"))
(external OrCAD_LIB
(edifLevel 0)
(technology
(numberDefinition
(scale 1 1 (unit distance))))
(cell &74LS00
(cellType generic)
(comment "From OrCAD library D:\ORCAD
DEMO\CAPTURE\SDT\FIG_B-01.OLB")
(view NetlistView
(viewType netlist)
(interface
(port &1 (direction INPUT))
(port &2 (direction INPUT))
(port &3 (direction OUTPUT))
(port &4 (direction INPUT))
(port &5 (direction INPUT))
(port &6 (direction OUTPUT))
(port &7 (direction INPUT))
(port &8 (direction OUTPUT))
(port &9 (direction INPUT))
(port &10 (direction INPUT))
(port &11 (direction OUTPUT))
(port &12 (direction INPUT))
(port &13 (direction INPUT))
(port &14 (direction INPUT)))))
(cell &74LS32
(cellType generic)
(comment "From OrCAD library D:\ORCAD
DEMO\CAPTURE\SDT\FIG_B-01.OLB")
(view NetlistView
(viewType netlist)
(interface
```

```
(port &1 (direction INPUT))
(port &2 (direction INPUT))
(port &3 (direction OUTPUT))
(port &4 (direction INPUT))
(port &5 (direction INPUT))
(port &6 (direction OUTPUT))
(port &7 (direction INPUT))
(port &8 (direction OUTPUT))
(port &9 (direction INPUT))
(port &10 (direction INPUT))
(port &11 (direction OUTPUT))
(port &12 (direction INPUT))
(port &13 (direction INPUT))
(port &14 (direction INPUT))))))
(library MAIN_LIB
(edifLevel 0)
(technology
(numberDefinition
(scale 1 1 (unit distance))))
(cell (rename &FIG_BMINUS01 "FIG_B-01")
(cellType generic)
(view NetlistView
(viewType netlist)
(interface
(port &CLOCK (direction INPUT))
(port &OUT (direction OUTPUT))
(port &B (direction INPUT))
(port &A (direction INPUT)))
(contents
(instance &U1
(viewRef NetlistView
(cellRef &74LS00
(libraryRef OrCAD_LIB)))
(property PartValue (string "74LS00"))
(property ModuleValue (string "14DIP300"))
(property TimeStampValue (string "6CB84CBA")))
(instance &U2
(viewRef NetlistView
(cellRef &74LS32
(libraryRef OrCAD_LIB)))
(property PartValue (string "74LS32"))
(property ModuleValue (string "14DIP300"))
(property TimeStampValue (string "6E46169D")))
(net &GND
(joined
(portRef &7 (instanceRef &U1))
(portRef &7 (instanceRef &U2))))
(net &VCC
(joined
(portRef &14 (instanceRef &U1))
(portRef &14 (instanceRef &U2))))
(net &CLOCK
(joined
(portRef &CLOCK)
(portRef &10 (instanceRef &U1))))
(net &Q
(joined
(portRef &6 (instanceRef &U1))
(portRef &2 (instanceRef &U2))
(portRef &9 (instanceRef &U1))))
(net &OUT
```

```
(joined
(portRef &OUT)
(portRef &3 (instanceRef &U2))))
(net &B
(joined
(portRef &B)
(portRef &4 (instanceRef &U1))))
(net &N00019
(joined
(portRef &3 (instanceRef &U1))
(portRef &1 (instanceRef &U2))))
(net &N00013
(joined
(portRef &5 (instanceRef &U1))
(portRef &8 (instanceRef &U1))))
(net &A
(joined
(portRef &A)
(portRef &1 (instanceRef &U1))
(portRef &2 (instanceRef &U1)))))))))
(design (rename &FIG_BMINUS01 "FIG_B-01")
(cellRef &FIG_BMINUS01
(libraryRef MAIN_LIB))))
```

Example hierarchical netlist

```
(edif FULLADD
(edifVersion 2 0 0)
(edifLevel 0)
(keywordMap (keywordLevel 0))
(status
(written
(timeStamp 1998 11 13 23 03 20)
(program "CAPTURE.EXE" (Version "9.00.1120"))
(comment "Original data from OrCAD/CAPTURE schematic"))
(comment "Hierarchy (Complex) Example")
(comment "Thursday, November 12, 1998")
(comment "OrCAD-06")
(comment "A")
(comment "OrCAD")
(comment "9300 S.W. Nimbus Ave.")
(comment "Beaverton, OR 97008")
(comment "(503)671-9500 Corporate Offices")
(comment "(503) 671-9400 Technical Support"))
(external OrCAD_LIB
(edifLevel 0)
(technology
(numberDefinition
(scale 1 1 (unit distance))))
(cell &74LS32
(cellType generic)
(comment "From OrCAD library FULLADD.OLB")
(view NetlistView
(viewType netlist)
(interface
(port &1 (direction INPUT))
(port &2 (direction INPUT))
(port &3 (direction OUTPUT))
(port &14 (direction INPUT))
```

```
(port &7 (direction INPUT))
(port &4 (direction INPUT))
(port &5 (direction INPUT))
(port &6 (direction OUTPUT))
(port &9 (direction INPUT))
(port &10 (direction INPUT))
(port &8 (direction OUTPUT))
(port &12 (direction INPUT))
(port &13 (direction INPUT))
(port &11 (direction OUTPUT)))))
(cell &74LS08
(cellType generic)
(comment "From OrCAD library FULLADD.OLB")
(view NetlistView
(viewType netlist)
(interface
(port &1 (direction INPUT))
(port &2 (direction INPUT))
(port &3 (direction OUTPUT))
(port &14 (direction INPUT))
(port &7 (direction INPUT))
(port &4 (direction INPUT))
(port &5 (direction INPUT))
(port &6 (direction OUTPUT))
(port &9 (direction INPUT))
(port &10 (direction INPUT))
(port &8 (direction OUTPUT))
(port &12 (direction INPUT))
(port &13 (direction INPUT))
(port &11 (direction OUTPUT)))))
(cell &74LS04
(cellType generic)
(comment "From OrCAD library FULLADD.OLB")
(view NetlistView
(viewType netlist)
(interface
(port &1 (direction INPUT))
(port &2 (direction OUTPUT))
(port &14 (direction INPUT))
(port &7 (direction INPUT))
(port &3 (direction INPUT))
(port &4 (direction OUTPUT))
(port &5 (direction INPUT))
(port &6 (direction OUTPUT))
(port &9 (direction INPUT))
(port &8 (direction OUTPUT))
(port &11 (direction INPUT))
(port &10 (direction OUTPUT))
(port &13 (direction INPUT))
(port &12 (direction OUTPUT))))))
(library MAIN_LIB
(edifLevel 0)
(technology
(numberDefinition
(scale 1 1 (unit distance))))
(cell EX6B
(cellType generic)
(view NetlistView
(viewType netlist)
(interface
(port X (direction INPUT))
```

```
(port Y (direction INPUT))
(port CARRY (direction OUTPUT))
(port SUM (direction OUTPUT)))
(contents
(instance U1
(viewRef NetlistView
(cellRef &74LS32
(libraryRef OrCAD_LIB))))
(instance U2
(viewRef NetlistView
(cellRef &74LS08
(libraryRef OrCAD_LIB))))
(instance U3
(viewRef NetlistView
(cellRef &74LS04
(libraryRef OrCAD_LIB))))
(net Y
(joined
(portRef &9 (instanceRef U2))
(portRef &3 (instanceRef U3))
(portRef &4 (instanceRef U2))
(portRef Y)))
(net CARRY
(joined
(portRef &8 (instanceRef U2))
(portRef CARRY)))
(net SUM
(joined
(portRef &6 (instanceRef U1))
(portRef SUM)))
(net X_BAR
(joined
(portRef &5 (instanceRef U2))
(portRef &2 (instanceRef U3))))
(net X
(joined
(portRef &10 (instanceRef U2))
(portRef &1 (instanceRef U3))
(portRef &1 (instanceRef U2))
(portRef X)))
(net N00037
(joined
(portRef &5 (instanceRef U1))
(portRef &6 (instanceRef U2))))
(net N00035
(joined
(portRef &3 (instanceRef U2))
(portRef &4 (instanceRef U1))))
(net GND
(joined
(portRef &7 (instanceRef U3))
(portRef &7 (instanceRef U2))
(portRef &7 (instanceRef U1))))
(net VCC
(joined
(portRef &14 (instanceRef U3))
(portRef &14 (instanceRef U2))
(portRef &14 (instanceRef U1))))
(net N5056796111
(joined
(portRef &4 (instanceRef U3))
```

```
(portRef &2 (instanceRef U2)))))))
(cell FULLADD
(cellType generic)
(view NetlistView
(viewType netlist)
(interface
(port SUM (direction OUTPUT))
(port X (direction INPUT))
(port Y (direction INPUT))
(port CARRY_OUT (direction OUTPUT))
(port CARRY_IN (direction INPUT)))
(contents
(instance U1
(viewRef NetlistView
(cellRef &74LS32
(libraryRef OrCAD_LIB))))
(instance halfadd_A
(viewRef NetlistView
(cellRef EX6B)))
(instance halfadd_B
(viewRef NetlistView
(cellRef EX6B)))
(net CARRY_IN
(joined
(portRef X (instanceRef halfadd_A))
(portRef CARRY_IN)))
(net SUM
(joined
(portRef SUM (instanceRef halfadd_A))
(portRef SUM)))
(net N00015
(joined
(portRef CARRY (instanceRef halfadd_A))
(portRef &1 (instanceRef U1))))
(net X
(joined
(portRef X (instanceRef halfadd_B))
(portRef X)))
(net N00013
(joined
(portRef Y (instanceRef halfadd_A))
(portRef SUM (instanceRef halfadd_B))))
(net Y
(joined
(portRef Y (instanceRef halfadd_B))
(portRef Y)))
(net N00025
(joined
(portRef CARRY (instanceRef halfadd_B))
(portRef &2 (instanceRef U1))))
(net CARRY_OUT
(joined
(portRef &3 (instanceRef U1))
(portRef CARRY_OUT)))
(net VCC
(joined
(portRef &14 (instanceRef U1))))
(net GND
(joined
(portRef &7 (instanceRef U1)))))))))
(design FULLADD
```

```
(cellRef FULLADD
(libraryRef MAIN_LIB))))
```

EEDesigner netlist format

EEDesigner netlists have the following characteristics:

- Part names, module names, and pin numbers are not checked for length.
- Reference strings are limited to eight characters.
- Node names are not supported.
- Node numbers are limited to three digits following the "UN" prefix.
- Pin names are not used.
- All ASCII characters are legal.

Example

```
(PATH,OrCAD()
(COMPONENTS
U1 ,14DIP300
U2 ,14DIP300
)
(NODES
(UN001
U1 , 7
U2 , 7
)
(UN002
U1 , 14
U2 , 14
)
(UN003
U1 , 10
)
(UN004
U1 , 6
U2 , 2
U1 , 9
)
(UN005
U2 , 3
)
(UN006
U1 , 4
)
(UN007
U1 , 3
```

```
U2 , 1
)
(UN008
U1 , 5
U1 , 8
)
(UN009
U1 , 1
U1 , 2
)
)
),OrCAD
```

Futurenet netlist format

FutureNet netlists have the following characteristics:

- Part names are limited to 16 characters.
- Module names, node names, and pin numbers are not checked for length.
- Reference strings are limited to six characters.
- Node numbers are limited to eight digits.

You can use Capture to generate FutureNet pinlists or netlists.

Pinlist example

```
PINLIST,2
(DRAWING,ORCAD.PIN,1-1
(SYM,1
DATA,2,U1
DATA,3,74LS00
DATA,4,14DIP300
PIN,,A,1-1,5,23,I0_A
PIN,,A,1-1,5,23,I1_A
PIN,,N00019,1-1,5,21,O_A
PIN,,B,1-1,5,23,I0_B
PIN,,N00013,1-1,5,23,I1_B
PIN,,Q,1-1,5,21,O_B
PIN,,GND,1-1,5,23,GND
PIN,,N00013,1-1,5,21,O_C
PIN,,Q,1-1,5,23,I0_C
PIN,,CLOCK,1-1,5,23,I1_C
PIN,,UN000001,1-1,5,21,O_D
PIN,,UN000002,1-1,5,23,I0_D
PIN,,UN000003,1-1,5,23,I1_D
PIN,,VCC,1-1,5,23,VCC
)
(SYM,2
DATA,2,U2
DATA,3,74LS32
```

```
DATA,4,14DIP300
PIN,,N00019,1-1,5,23,I0_A
PIN,,Q,1-1,5,23,I1_A
PIN,,OUT,1-1,5,21,O_A
PIN,,UN000004,1-1,5,23,I0_B
PIN,,UN000005,1-1,5,23,I1_B
PIN,,UN000006,1-1,5,21,O_B
PIN,,GND,1-1,5,23,GND
PIN,,UN000007,1-1,5,21,O_C
PIN,,UN000008,1-1,5,23,I0_C
PIN,,UN000009,1-1,5,23,I1_C
PIN,,UN000010,1-1,5,21,O_D
PIN,,UN000011,1-1,5,23,I0_D
PIN,,UN000012,1-1,5,23,I1_D
PIN,,VCC,1-1,5,23,VCC
)
SIG,GND,1-1,5,GND
SIG,VCC,1-1,5,VCC
SIG,CLOCK,1-1,5,CLOCK
SIG,Q,1-1,5,Q
SIG,OUT,1-1,5,OUT
SIG,B,1-1,5,B
SIG,N00019,1-1,5,N00019
SIG,N00013,1-1,5,N00013
SIG,A,1-1,5,A
)
```

Netlist example

```
NETLIST,2
(DRAWING,ORCAD.NET,1-1
DATA,50,Generic Netlist Example
DATA,51,OrCAD-01
DATA,52,A
DATA,54,Thursday, November 12, 1998
)
(SYM,1-1,1
DATA,2,U1
DATA,3,74LS00
DATA,4,14DIP300
DATA,23,I0_A
DATA,23,I1_A
DATA,21,O_A
DATA,23,I0_B
DATA,23,I1_B
DATA,21,O_B
DATA,23,GND
DATA,21,O_C
DATA,23,I0_C
DATA,23,I1_C
DATA,21,O_D
DATA,23,I0_D
DATA,23,I1_D
DATA,23,VCC
)
(SYM,1-1,2
DATA,2,U2
DATA,3,74LS32
DATA,4,14DIP300
```

```
DATA,23,I0_A
DATA,23,I1_A
DATA,21,O_A
DATA,23,I0_B
DATA,23,I1_B
DATA,21,O_B
DATA,23,GND
DATA,21,O_C
DATA,23,I0_C
DATA,23,I1_C
DATA,21,O_D
DATA,23,I0_D
DATA,23,I1_D
DATA,23,VCC
)
(SIG,,GND,1-1,5,GND
PIN,1-1,1,U1,23,GND
PIN,1-1,2,U2,23,GND
)
(SIG,,VCC,1-1,5,VCC
PIN,1-1,1,U1,23,VCC
PIN,1-1,2,U2,23,VCC
)
(SIG,,CLOCK,1-1,5,CLOCK
PIN,1-1,1,U1,23,I1_C
)
(SIG,,Q,1-1,5,Q
PIN,1-1,1,U1,21,O_B
PIN,1-1,2,U2,23,I1_A
PIN,1-1,1,U1,23,I0_C
)
(SIG,,OUT,1-1,5,OUT
PIN,1-1,2,U2,21,O_A
)
(SIG,,B,1-1,5,B
PIN,1-1,1,U1,23,I0_B
)
(SIG,,N00019,1-1,5,N00019
PIN,1-1,1,U1,21,O_A
PIN,1-1,2,U2,23,I0_A
)
(SIG,,N00013,1-1,5,N00013
PIN,1-1,1,U1,23,I1_B
PIN,1-1,1,U1,21,O_C
)
(SIG,,A,1-1,5,A
PIN,1-1,1,U1,23,I0_A
PIN,1-1,1,U1,23,I1_A
)
```

HiLo netlist format

HiLo netlists have the following characteristics:

- Part names, module names, reference strings, and pin numbers are not checked for length.

- Node names are limited to 14 characters.
- Node numbers are limited to five digits following the "N" prefix.
- Pin names are not used.
- All ASCII characters are legal.

Example

```
** Generic Netlist Example Revised: Thursday, November 12,
1998
** OrCAD-01 Revision: A
** OrCAD
** 9300 S.W. Nimbus Ave.
** Beaverton, OR 97008
** (503) 671-9500 Corporate Offices
** (503) 671-9400 Technical Support
CCT ORCAD (
** Please put your circuit interface definition here
);
14DIP300
U1 (
A,
A,
N00019,
B,
N00013,
Q,
GND,
N00013,
Q,
CLOCK,
,
,
,
VCC
);
14DIP300
U2 (
N00019,
Q,
OUT,
,
,
,
GND,
,
,
,
,
,
,
VCC
);
```

Intel ADF netlist format

Intel ADF netlists have the following characteristics:

- Part names, module names, reference strings, and pin numbers are not checked for length.
- Node numbers are not used.
- All ASCII characters are legal.

Intel ADF netlist constraints

When you create an Intel ADF netlist, you must include the OrCAD-supplied ALTERA_P.OLB and ALTERA_M.OLB libraries in your project. You can use only the parts in these two libraries to create the schematic folder.

Inputs and outputs are handled differently in Capture than in the Altera software. Capture defines inputs and outputs with hierarchical ports and library objects. Altera defines inputs and outputs with a library object, which is then tagged with the appropriate pin number. In the example schematic page, the CLOCK signal is an input and the STROBE signal is an output.

Also, library objects with unused pins default to predefined levels in the Altera software. Because Capture does not default unconnected pins to any particular level, you must tie all unused pins to the appropriate level.

Intel ADF pipe commands

You can place equations in your schematic folder to be included in the netlist. To place these equations on the schematic page, choose the Text command from the Place menu.

Each equation must start with the pipe character (|). The first line must be:

```
|EQUATIONS
```

This tells Capture that some Intel ADF equations need to be included in the netlist. The equations can contain any information you want to include in the netlist.

Intel ADF title block information

Title block information is placed in the first 10 lines of the netlist. The following table shows an example netlist header and the title block information from which the header was extracted. Header information in bold is text entered in the schematic page's title block
.

Line	Example header	Title block field
1	ADF Example	Title of schematic page
1	May 15, 2002	Date
2	OrCAD-03	Document number
2	D	Revision Code
3	Dade's House of Boards	Organization Name
4	933 SW 52nd St.	1st Address Line
6	Turbo=ON	3rd Address Line
7	5C031	4th Address Line

Example

```
ADF Example Revised: Friday, November 13, 1998
OrCAD-02 Revision: A
OrCAD
9300 S.W. Nimbus Ave.

TURBO = ON
5C031

OPTIONS:TURBO = ON
PART:5C031

INPUTS:
CLOCK
ENABLE
COINDROP
CUPFULL
RESET

OUTPUTS:
STROBE
POURDRNK
DROPCUP
```

```
NETWORK:
J=INP(ENABLE) % SYM 1 %
N=INP(CUPFULL) % SYM 2 %
O=OR(P,Q) % SYM 3 %
POURDRNK,E=RORF(O,D,H,I,J) % SYM 4 %
Q=AND(F,R) % SYM 5 %
R=NOT(E) % SYM 6 %
B=XOR(E,F) % SYM 7 %
A=AND(B,C) % SYM 8 %
STROBE=CONF(A,VCC) % SYM 9 %
C=NOT(D) % SYM 10 %
D=INP(CLOCK) % SYM 11 %
H=AND(F,E) % SYM 12 %
I=INP(RESET) % SYM 13 %
G=AND(K,L,M) % SYM 14 %
DROPCUP,F=RORF(G,D,H,I,J) % SYM 15 %
M=INP(COINDROP) % SYM 16 %
K=NOT(F) % SYM 17 %
P=AND(K,E,L) % SYM 18 %
L=NOT(N) % SYM 19 %

EQUATIONS:
G = (K & L & M);
H = (F & E);
O = (P # Q);
END$
```

Intergraph netlist format

Intel ADF netlists have the following characteristics:

- Part names, module names, reference strings, and pin numbers are not checked for length.
- Node numbers can have up to five digits following the "N" prefix.
- Pin names are not used.
- All ASCII characters are legal.

Example

```
%PART
14DIP300 U1
14DIP300 U2
%NET
GND U1-7 U2-7
VCC U1-14 U2-14
CLOCK U1-10
Q U1-6 U2-2 U1
OUT U2-3
B U1-4
N00019 U1-3 U2-1
N00013 U1-5 U1-8
```

```
A U1-1 U1-2
$
```

Mentor netlist format

Mentor Graphics BoardStation Version 7 netlists have the following characteristics:

- Part names, module names, and reference strings are limited to nineteen characters.
- Node names and pin numbers are not checked for length.
- Node numbers are limited to five digits following the "N" prefix.
- Pin names are not used.
- All ASCII characters are legal.

Note: Capture includes a netlister (available from the Accessories menu) developed specifically for Mentor netlist generation. There is also a document that discusses the use of the netlister. It is available in the Vendor directory of your Capture installation.

Example component file

```
# OrCAD Formatted Netlist for MENTOR Board Station V6
# Reference Value Field Module Field
U1 PART 74LS00 14DIP300
U2 PART 74LS32 14DIP300
```

Example netlist

```
NET 'GND' U1-7 U2-7
NET 'VCC' U1-14 U2-14
NET 'CLOCK' U1-10
NET 'Q' U1-6 U2-2 U1-9
NET 'OUT' U2-3
NET 'B' U1-4
NET 'N00019' U1-3 U2-1
NET 'N00013' U1-5 U1-8
NET 'A' U1-1 U1-2
```

Multiwire netlist format

MultiWire netlists have the following characteristics:

- Part names and module names are not checked for length.
- Reference strings and pin numbers together are limited to thirty-two characters.
- Node names are limited to sixteen characters.
- Node numbers are limited to five digits following the "N" prefix.
- Pin names are not used.
- All ASCII characters are legal.

Example

```
GND U1 7
GND U2 7
VCC U1 14
VCC U2 14
CLOCK U1 10
Q U1 6
Q U2 2
Q U1 9
OUT U2 3
B U1 4
N00019 U1 3
N00019 U2 1
N00013 U1 5
N00013 U1 8
A U1 1
A U1 2
-1
```

OHDL netlist format

OrCAD PLD 386+ netlists have the following characteristics:

- Part names, module names, reference strings, node names, and pin numbers are not checked for length.
- Node numbers are limited to five digits following the "N" prefix.
- Pin names are not used.
- All ASCII characters are legal.

For more information, see the OrCAD web site.

OHDL netlist constraints

The OHDL netlist format uses the OrCAD-supplied PLDGATES.OLB and TTL.OLB libraries. Be sure you include one of these libraries in your project.

Example

OHDL netlists normally have a .PLD file extension.

```
|| CNTMUX (Example for MACH 110) Revised: Friday, November 13,
1998
|| D:\ORCAD DEMO\CAPTURE\NETLIST UPDATES\DESIGN6\Revision: ?
|| OrCAD
||
||
||
||
||
| Type: "IFX780_132"
|
|
| Netlist:
| {
| PAD (I0,"IN") | PAD1
| PAD (I6,"IN") | PAD10
| PAD (O3,"OUT") | PAD11
| PAD (I7,"IN") | PAD12
| PAD (O4,"OUT") | PAD13
| PAD (I8,"IN") | PAD14
| PAD (O5,"OUT") | PAD15
| PAD (I9,"IN") | PAD16
| PAD (O6,"OUT") | PAD17
| PAD (I10,"IN") | PAD18
| PAD (O7,"OUT") | PAD19
| PAD (I1,"IN") | PAD2
| PAD (I11,"IN") | PAD20
| PAD (O8,"OUT") | PAD21
| PAD (I12,"IN") | PAD22
| PAD (O9,"OUT") | PAD23
| PAD (O10,"OUT") | PAD24
| PAD (I14,"IN") | PAD25
| PAD (O11,"OUT") | PAD26
| PAD (I15,"IN") | PAD27
| PAD (O12,"OUT") | PAD28
| PAD (O13,"OUT") | PAD29
| PAD (I2,"IN") | PAD3
| PAD (LOAD,"IN") | PAD30
| PAD (O14,"OUT") | PAD31
| PAD (O15,"OUT") | PAD32
| PAD (CLK,"IN") | PAD33
| PAD (UP,"IN") | PAD34
| PAD (COUNT,"IN") | PAD35
| PAD (SELECT,"IN") | PAD36
| PAD (I3,"IN") | PAD4
| PAD (O0,"OUT") | PAD5
| PAD (I4,"IN") | PAD6
```

```
| PAD (O1,"OUT") | PAD7
| PAD (I5,"IN") | PAD8
| PAD (O2,"OUT") | PAD9
| G169
(UP,CLK,I0,I1,I2,I3,GND,-,N00185,N00193,Q3,Q2,Q1,Q0,N00177)
| U1
| G257
(SELECT,Q12,I12,O12,Q13,I13,O13,-,O14,I14,Q14,O15,I15,Q15,GN
D) | U10
| G257 (SELECT,Q0,I0,O0,Q1,I1,O1,-,O2,I2,Q2,O3,I3,Q3,GND) |
U2
| G169
(UP,CLK,I4,I5,I6,I7,GND,-,N00185,N00177,Q7,Q6,Q5,Q4,-) | U3
| G04 (LOAD,N00185) | U4
| G257 (SELECT,Q4,I4,O4,Q5,I5,O5,-,O6,I6,Q6,O7,I7,Q7,GND) |
U5
| G169
(UP,CLK,I8,I9,I10,I11,GND,-,N00185,N00193,Q11,Q10,Q9,Q8,N003
55) | U6
| G04 (COUNT,N00193) | U7
| G257
(SELECT,Q8,I8,O8,Q9,I9,O9,-,O10,I10,Q10,O11,I11,Q11,GND) |
U8
| G169
(UP,CLK,I12,I13,I14,I15,GND,-,N00185,N00355,Q15,Q14,Q13,Q12,
-) | U9
| }
|
|Vectors:
|{ Display COUNT, LOAD, SELECT, CLK, \
| (I[15..8])d, (O[15..8])d, \
| (I[7..0])d, (O[7..0])d
|
| Test LOAD=1; CLK
| Test LOAD=0; COUNT=1; UP=1; CLK=25(0,1)
| Set I[15..8] = 10
| Set I[7..0] = 11
| Test SELECT=1,0
| Test LOAD=0; COUNT=1; UP=0; CLK=25(0,1)
| Test SELECT=1,0
| End }
```

PADS 2000 netlist format

PADS 2000 netlists have the following characteristics:

- Part names, module names, and pin numbers are not checked for length.
- Reference strings are limited to sixteen characters.
- Header information is included at the top of the netlist file:

  ```
  !PADS-POWERPCB-V2
  ```

- Net and signal names are limited to forty-seven characters.

- Legal characters for reference strings and node names are limited to:
  - ~ ! # $ % _ - =
  - + | / . : ; < >
  - A..Z a..z 0..9
- Node numbers are limited to five digits following the "N" prefix.
- Pin names are not used.
- All ASCII characters are legal except as noted for reference strings and node names.

Note: You can add a property called "tracewidth" to nets in Capture. The value of tracewidth will carry through into the PADS 2000 netlist. Capitalization of this property is important, and the property won't appear in the netlist if any uppercase letters are used in the property name.

For more information see the PADS website.

Example

This netlist was created with no options selected. PADS 2000 netlists normally have a .ASC file extension.

The header information in this example was created without the Create Pads BGA netlist option selected. If you choose this option when you create the PADS netlist, the header information will appear differently. In effect, choosing the Create Pads BGA netlist option causes Capture to generate a Powerpcb v3.0 netlist.

```
*PADS 2000*
*PART*
U1 14DIP300
U2 14DIP300
*NET*
*SIGNAL* GND
U1.7 U2.7
*SIGNAL* VCC
U1.14 U2.14
*SIGNAL* CLOCK
U1.10
*SIGNAL* Q
U1.6 U2.2 U1.9
*SIGNAL* OUT
U2.3
*SIGNAL* B
```

```
U1.4
*SIGNAL* N00019
U1.3 U2.1
*SIGNAL* N00013
U1.5 U1.8
*SIGNAL* A
U1.1 U1.2
*END*
```

PADS PCB netlist format

PADS-Software PADS PowerPCB netlists have the following characteristics:

- Part names, module names, and pin numbers are not checked for length.
- Reference strings are limited to sixteen characters.
- Header information is included at the top of the netlist file:

  ```
  !PADS-POWERPCB-V2
  ```

- Net and signal names are limited to twelve characters.
- Legal characters for reference strings and node names are limited to:
  - ~ ! # $ % _ - =
  - + | / . : ; < >
  - A..Z a..z 0..9
- Node numbers are limited to five digits following the "N" prefix.
- Pin names are not used.
- All ASCII characters are legal except as noted for reference strings and node names.

Example

This netlist was created with no options selected. PADS-PCB netlists normally have a .ASC file extension.

The header information in this example was created without the Create Pads BGA netlist option selected. If you choose this option when you create the PADS netlist, the header information will appear

differently. In effect, choosing the Create Pads BGA netlist option causes Capture to generate a Powerpcb v3.0 netlist.

```
*PADS-PCB*
*PART*
U1 14DIP300
U2 14DIP300
*NET*
*SIGNAL* GND
U1.7 U2.7
*SIGNAL* VCC
U1.14 U2.14
*SIGNAL* CLOCK
U1.10
*SIGNAL* Q
U1.6 U2.2 U1.9
*SIGNAL* OUT
U2.3
*SIGNAL* B
U1.4
*SIGNAL* N00019
U1.3 U2.1
*SIGNAL* N00013
U1.5 U1.8
*SIGNAL* A
U1.1 U1.2
*END*
```

PCAD netlist format

PCAD PCB netlists from ACCEL Technologies have the following characteristics:

- Part names, module names, reference strings, and pin numbers are not checked for length.
- Node names are limited to eight characters.
- Node numbers are limited to five digits following the "NET" prefix.
- Pin names are not used.
- Characters are not checked for legality.

For more information, see the ACCEL Technologies web site, the Protel web site, and the netlist example.

Example

This netlist was created with no options selected. PCAD netlists normally have a .NET file extension.

```
{COMPONENT ORCAD.PCB
 {ENVIRONMENT LAYS.PCB}
  {PDIFvrev 1.30}
  {DETAIL
  {SUBCOMP
{I 14DIP300.PRT U1
{CN
  1 A
  2 A
  3 N00019
  4 B
  5 N00013
  6 Q
  7 GND
  8 N00013
  9 Q
  10 CLOCK
  11 ?
  12 ?
  13 ?
  14 VCC
}
}
{I 14DIP300.PRT U2
{CN
  1 N00019
  2 Q
  3 OUT
  4 ?
  5 ?
  6 ?
  7 GND
  8 ?
  9 ?
  10 ?
  11 ?
  12 ?
  13 ?
  14 VCC
}
}
}
}
}
```

PCADnlt netlist format

PCADnlt netlists from ACCEL Technologies have the following characteristics:

- Part names, module names, reference strings, node names, and pin numbers are not checked for length.
- Legal characters for node names are limited to:

  ```
  $ - + _ (underscore)
  A..Z a..z 0..9
  ```

- Node numbers are limited to five digits following the "N" prefix.
- Pin names are not used.
- All ASCII characters are legal except as noted for node names.

For more information, see the ACCEL Technologies web site, the Protel web site.

Example

PCADnlt netlists normally have a .NET file extension.

```
% Generic Netlist Example Revised: Thursday, November 12, 1998
% OrCAD-01 Revision: A
% OrCAD
% 9300 S.W. Nimbus Ave.
% Beaverton, OR 97008
% (503) 671-9500 Corporate Offices
% (503) 671-9400 Technical Support
BOARD = ORCAD.PCB;

PARTS
14DIP300 = U1, % 74LS00
  U2; % 74LS32

NETS

GND = U1/7 U2/7 ;
VCC = U1/14 U2/14 ;
CLOCK = U1/10 ;
Q = U1/6 U2/2 U1/9 ;
OUT = U2/3 ;
B = U1/4 ;
N00019 = U1/3 U2/1 ;
N00013 = U1/5 U1/8 ;
A = U1/1 U1/2 ;
```

PCBII and PCBIIL netlist formats

PCB netlists are used with OrCAD's PCB II Layout Tools. See the *PCB II User's Guide* for details.

The PCBII and PCBIIL netlist formats are identical with the following exception: the PCBIIL.DLL netlist format has no restrictions on netname length.

PCB netlists have the following characteristics:

- Part names, module names, reference strings, node names, and pin numbers are not checked for length.
- Node numbers are limited to five digits following the "N" prefix.
- All ASCII characters are legal.
- Footprint names are limited to eight characters.
- PCBII (but not PCBIIL) net names are limited to eight characters.

For more information, see the OrCAD web site.

PDUMP netlist format

This format produces a parts list containing all the information on the schematic pages. No information is omitted or changed. You can use this netlist format when troubleshooting a project.

PLD netlist format

This file produces netlists that define logic for use with Programmable Logic Design Tools 386+. See the *Programmable Logic Design Tools User's Guide* and the *Programmable Logic Design Tools Reference Guide* for details.

PLD netlists have the following characteristics:

- Part names, module names, reference strings, node names, and pin numbers are not checked for length.
- Pin names are not used.
- All ASCII characters are legal.

For more information, see the OrCAD web site.

PLD netlist constraints

When you create a PLD netlist, be sure to include the OrCAD-supplied PLDGATES.OLB library in your project. You can use only the parts in PLDGATES.OLB, DEVICE.OLB (VCC, POWER, GND), and TTL.OLB (most 74LSxx) in a schematic folder to be netlisted for PLD.

Example

This netlist was created with no options selected. PLD netlists normally have a .NET file extension.

```
|| PLD Netlist Example Revised: Friday, November 13, 1998
|| OrCAD-05 Revision: A
|| OrCAD
|| 9300 S.W. Nimbus Ave.
|| Beaverton, OR 97008
|| (503) 671-9500 Corporate Offices
|| (503) 671-9400 Technical Support
||
| Netlist: A0,A1,B1,B0
| ->
| Y0,Y3,Y1,Y2
| {
| G08 (B0,A0,Y0) | U1
| G32 (N00103,N00107,N00095) | U10
| G04 (B1,N00113) | U11
| G11 (N00113,B0,-,-,-,-,-,-,-,-,-,N00107,A1) | U12
| G11 (B1,A1,-,-,-,-,-,-,-,-,-,N00133,N00137) | U13
| G04 (A0,N00137) | U14
| G32 (N00133,N00145,Y2) | U15
| G04 (B0,N00151) | U16
| G11 (B1,N00151,-,-,-,-,-,-,-,-,-,N00145,A1) | U17
| G21 (A0,A1,-,B0,B1,Y3) | U18
| G04 (A0,N00063) | U2
| G11 (N00063,B0,-,-,-,-,-,-,-,-,-,N00069,A1) | U3
| G32 (N00069,N00083,N00087) | U4
| G04 (A1,N00081) | U5
| G11 (B1,N00081,-,-,-,-,-,-,-,-,-,N00083,A0) | U6
| G32 (N00087,N00095,Y1) | U7
| G04 (B0,N00101) | U8
| G11 (B1,N00101,-,-,-,-,-,-,-,-,-,N00103,A0) | U9
| }
```

Protel2 netlist format

Protel2 netlists have the following characteristics:

- Part names, module names, reference strings, and node names can be up to 16 characters in length.

- Node numbers are limited to 5 digits (plus the leading 'N'.
- Pin numbers are not checked for length.
- The Reference and ModuleName must be in uppercase only.
- All ASCII characters are legal except { '()[],-'}.

For more information, see the Protel web site.

Example

Accel netlists normally have a .NET file extension.

This example was created with the combined property strings for Create Netlist set to their default values, as shown below:

```
]
[
DESIGNATOR
C10
FOOTPRINT
SM/C_0805
PARTTYPE
390PF
DESCRIPTION
]
[
DESIGNATOR
C100
FOOTPRINT
0.1UF
PARTTYPE
0.1UF
DESCRIPTION
]
[
DESIGNATOR
C101
FOOTPRINT
0.1UF
PARTTYPE
0.1UF
DESCRIPTION
```

RecalRedac netlist format

The newer version of the RacalRedac netlist format is RINF.

Zuken-Redac CADStar PCB netlists have the following characteristics:

- Part names, module names, reference strings, node names, and pin numbers are not checked for length.
- Node numbers are limited to five digits following the "N" prefix.
- Pin names are not used.
- All ASCII characters are legal.

For more information, see the Zuken-Redac web site at http://www.zuken.com/.

Example

RacalRedac netlists normally have a .NET file extension.

```
.PCB
.REM Generic Netlist Example Revised: Thursday, November 12,
1998
.REM OrCAD-01 Revision: A
.REM OrCAD
.REM 9300 S.W. Nimbus Ave.
.REM Beaverton, OR 97008
.REM (503) 671-9500 Corporate Offices
.REM (503) 671-9400 Technical Support
.CON
.COD 2

.REM GND
U1 7 U2 7
.REM VCC
U1 14 U2 14
.REM CLOCK
U1 10
.REM Q
U1 6 U2 2 U1 9
.REM OUT
U2 3
.REM B
U1 4
.REM N00019
U1 3 U2 1
.REM N00013
U1 5 U1 8
.REM A
U1 1 U1 2
.EOD
```

RINF netlist format

Zuken-Redac Visual PCB netlists have the following characteristics:

- Part names, module names, reference strings, node names, and pin numbers are not checked for length.
- Node numbers are limited to five digits following the "N" prefix.
- Pin names are not used.
- All ASCII characters are legal.

Example

RINF netlists normally have a .NET file extension.

```
 .HEA
.APP "Cadstar RINF Output - Version 2.3"
.UNI INCH 1000.0 in
.TYP FULL
.JOB "FIG_B-01"

.ADD_COM U1 "14DIP300"
.ADD_COM U2 "14DIP300"

.ADD_TER U1 7 "GND"
.TER U2 7

.ADD_TER U1 14 "VCC"
.TER U2 14

.ADD_TER U1 10 "CLOCK"

.ADD_TER U1 6 "Q"
.TER U2 2
  U1 9

.ADD_TER U2 3 "OUT"

.ADD_TER U1 4 "B"

.ADD_TER U1 3 "N00019"
.TER U2 1

.ADD_TER U1 5 "N00013"
.TER U1 8

.ADD_TER U1 1 "A"
.TER U1 2

.END
```

Scicards netlist format

Harris EDA SciCards netlists have the following characteristics:

- Part names are limited to seventeen characters.

- Module names are limited to fifteen characters.
- Reference strings and pin numbers combined are limited to twelve characters.
- Pin numbers are limited to three characters.
- Node names are limited to eight characters.
- Node numbers are not checked for length.
- Pin names are not used.
- All ASCII characters are legal.

For more information, see the netlist example.

Example

Scicards netlists normally have a .NET file extension.

```
PARTS LIST
74LS00 14DIP300 U1
74LS32 14DIP300 U2
EOS
NET LIST

NODENAME GND $
  U1 7 U2 7
NODENAME VCC $
  U1 14 U2 14
NODENAME CLOCK $
  U1 10
NODENAME Q $
  U1 6 U2 2 U1 9
NODENAME OUT $
  U2 3
NODENAME B $
  U1 4
NODENAME N00019 $
  U1 3 U2 1
NODENAME N00013 $
  U1 5 U1 8
NODENAME A $
  U1 1 U1 2
EOS
```

SPICE netlist format

Generic, flat SPICE format netlists have the following characteristics:

- Part names, module names, reference strings, node names, and pin numbers are not checked for length.
- Node numbers are limited to five characters.
- If the Use net names option is selected, legal characters for node names are limited to:

  `0..9 A..Z a..z $ _ (underscore)`

  If you select this option, Capture uses the node names you placed on the schematic page (via aliases and hierarchical ports) where available. Not all versions of SPICE support alphanumeric node names. Check your SPICE manual for details. If your version of SPICE does not allow alphanumeric node names, you can still give them numeric names such as "17." These numeric names do not interfere with the ones generated by Capture, since the node numbers it generates begin at 10000 (except GND, which is always 0).
- All ASCII characters are legal except as noted for node names.

For more information on flat SPICE netlists, see the flat SPICE netlist example.

The Spice formats

Capture provides two SPICE netlist formats. The first format produces either hierarchical or flat netlist output, depending on your project structure and the active view. It is accessible from the SPICE tab on the Create Netlist dialog box. The second format produces only flat netlists, and is accessible through the Other tab on the Create Netlist dialog box.

Use the SPICE tab if:

- You want to include net, part, and pin properties.
- You want a hierarchical netlist.

Use the Other tab if:

- You want a flat netlist of a simple hierarchical design.

Hierarchical designs in SPICE

For hierarchical designs, the SPICE format produces netlists with subcircuit (.SUBCKT) definitions for schematic pages in the hierarchy. These subcircuits are called by the X command (subcircuit call). Since SPICE does not require the subcircuits to be defined before use, the hierarchy appears in normal form in the netlist with the root page at the top of the file.

Note: According to the PSPICE manual, the X subcircuit general form is:

```
X name [nodes] subcircuit-name
```

where:
name Specifies a unique name for the device.
nodes Specifies the list of nets that attach to the device in the same order as the .SUBCKT definition used by the device.
subcircuit-name Specifies the name of a .SUBSCKT definition that the X device uses.

The following is an example of an X subcircuit call:

```
XBUF 13 15 UNITAMP
```

For more information on hierarchical SPICE netlists, see the hierarchical SPICE netlist example.

SPICE netlist constraints

Capture can create netlists larger than most PC-based SPICE programs accept. Consult your SPICE manual for the limits. If your PC meets SPICE's memory requirements, you can generate the largest netlist allowed.

The part value is used to pass modeling information to the netlist. For instance, resistor RS1 in the example flat schematic folder has a value of 1K Ohms; in the example hierarchical schematic folder R1 has a value of 6.8K Ohms.

Use the special PSPICE.OLB or SPICE.OLB libraries supplied by OrCAD when generating a SPICE netlist. These libraries already have pin numbers on the parts and are compatible with most versions of SPICE. The PSPICE.OLB contains many specific part types, such

as a 2N2222 NPN transistor, that are not provided in the generic SPICE.OLB.

All library part pin names should be changed to reflect the model node index. To find out the proper node ordering, see your SPICE manual.

As an example of what to change, the OrCAD-supplied NPN transistor has the pin names defined as base, emitter, and collector in the DEVICE.OLB library. For SPICE to understand the nodal information, the pin names must be changed from base, emitter, and collector to 2, 3, and 1 (as defined in the SPICE manual). Therefore, the library source file for an NPN transistor that is compatible with the SPICE pin numbering convention is as follows:

```
'NPN'
REFERENCE 'Q'
{X Size =} 2 {Y Size =} 2 {Parts per Package =} 0
L1 SHORT IN '2'
B2 SHORT IN '3'
T2 SHORT IN '1'
{ 0}..##.#
{ 1} ## #
  .
  .
  .
```

SPICE map files

In addition to the netlist file, Capture also creates a map file when you select the SPICE format. The node numbers created by Capture are placed in the .MAP file so you can cross-reference the SPICE node numbers with the node names that you specified on your schematic page. You must enter the map filename in the Map File text box in the Create Netlist dialog box.

Note: If you select the Use net names option, the map file may contain erroneous results.

For more information on SPICE map files, see the flat and hierarchical map file examples.

SPICE pipe commands

You can place lines of text on your schematic page to be included in the SPICE netlist. Select the Text command on the Place menu to place the text on your schematic page.

Each line of text must start with the pipe character (|). The first line must be:

```
|SPICE
```

This tells Capture to extract the information in the following lines of text when generating a SPICE netlist. The remaining lines can contain any information you want to include in the netlist. The lines following |SPICE are placed at the top of the netlist.

Tango netlist format

ACCEL Technologies Tango PCB and Tango PRO netlists have the following characteristics:

- Part names, module names, reference strings, and node names are limited to sixteen characters.
- Node numbers are limited to five digits following the "N" prefix.
- Pin numbers are not checked for length.
- Pin names are not used.
- Reference strings and module names must be uppercase characters.
- All ASCII characters are legal except:

  ```
  ( ) [ ] - (dash) , (comma)
  ```

  and as noted for reference strings and module names.

For more information, see the ACCEL Technologies web site at http://www.techaccel.com and the Protel web site at http://www.protel.com, as well as the Tango netlist example.

Telesis netlist format

Cadence Telesis netlists have the following characteristics:

- Part names, module names, reference strings, node names, and pin numbers are not checked for length.
- Node numbers are limited to five digits following the "N" prefix.
- Pin names are not used.
- All ASCII characters are legal.

For more information, see the OrCAD web site as well as the Telesis netlist example.

Example

Telesis netlists normally have a .NET file extension.

```
$PACKAGES
14DIP300! 74LS00; U1
14DIP300! 74LS32; U2
$NETS
GND; U1.7 U2.7
VCC; U1.14 U2.14
CLOCK; U1.10
Q; U1.6 U2.2 U1.9
OUT; U2.3
B; U1.4
N00019; U1.3 U2.1
N00013; U1.5 U1.8
A; U1.1 U1.2
$END
```

Vectron netlist format

Vectron netlists have the following characteristics:

- Part names, module names, and pin numbers are not checked for length.
- Reference strings are limited to eight characters.
- Node names are limited to twelve characters.
- Node numbers are limited to five digits following the "N" prefix.
- Pin names are not used.
- All ASCII characters are legal.

In addition to the netlist file, Capture also creates a part list file when you select the Vectron netlist format. You must enter a second

filename in the Destination 2 text box on the Netlist Format dialog box.

Example netlist

Vectron netlists normally have a .NET file extension.

```
*GND U1 7 U2 7
*VCC U1 14 U2 14
*CLOCK U1 10
*Q U1 6 U2 2 U1 9
*OUT U2 3
*B U1 4
*N00019 U1 3 U2 1
*N00013 U1 5 U1 8
*A U1 1 U1 2
```

Example part list

```
U1 14DIP300
U2 14DIP300
```

Verilog netlist format

Verilog netlists have the following characteristics:

- Part identifiers, module identifiers, reference strings, node identifiers, and pin numbers are not checked for length.
- Part identifiers, module identifiers, reference strings, node identifiers, and pin numbers must begin with a letter.
- Part identifiers, module identifiers, reference strings, node identifiers, and pin numbers must all be unique. That is, none of these can share a name.
- Legal characters for part identifiers, module identifiers, reference strings, node identifiers, and pin numbers are limited to:

  ```
  A..Z a..z 0..9
  ```

  If there are illegal characters in a part identifier, module identifier, reference string, node identifier, or pin number, the netlister converts them to legal Verilog names. This conversion uses the backslash character (\) to escape otherwise illegal characters. For spaces, the conversion uses the ASCII equivalent (#20).

Consider these examples:

This string....	converts to this...
____	
RAS	\R\A\S\
A B	\A#20B
AggB	\A#20#20B
A#B	\A#B
A#20B	\A#2320B
A#23B	\A#2323B

For more information, see the Verilog netlist example.

Note: In cases where a net name is different from a port name, Capture uses aliases to associate the two. That is, if a wire with one net name is connected to a port with a different name, Capture creates an alias to associate the two components to the same net.

The alias takes either of the following forms:

```
alias_bit alias_inst1(NetName, PortName)
alias_vector alias_inst1(NetName, PortName)
```

Where:

NetName is the name assigned to the net.
PortName is the name assigned to the port.

If these aliases are used, they will appear at the beginning of the netlist.

Assigning a Verilog parameter to a component instance

Identifiers for parts, modules, part references, nodes, pins, and nets must not conflict with any Verilog reserved word. See Verilog reserved words for a list of reserved words.

You can specify Verilog parameters on component instances as properties, using this method:

1. Assign the property Vlog_param to the component, using the following syntax:

   ```
   Vlog_Param = Parameter_name:Parameter_type
   ```

   Where:

   Parameter_name is the name of the parameter to be specified in the netlist.
   Parameter_type is the type of the parameter (for example, "integer," or "string").

Note: You can specify multiple Verilog parameters on a component instance, as well, by using the following format:

```
Vlog_ParamXX = Parameter_name:Parameter_type
```

Where:

XX is an integer that is unique to the parameter being defined.

2. Assign a value to the declared parameter:

Note: *Parameter_name* = *Parameter_value*

Where:

Parameter_name is the name of the parameter to be specified in the netlist.
Parameter_value is the value of the parameter.

The parameter will appear in the netlist as:

```
\7400 U7(
  .A_A( IN1 ) ,
  .B_A( IN2 ) ,
  .Y_A( OUT ) ,
  .VCC( VCC ) ,
  .GND( GND )
```

```
) ;
defparam U7.Parameter_name = Parameter_value;
```

If the parameter value is a string, the netlister encloses it in quotes ("") in the netlist. If a parameter does not have a value, the netlister will report an error.

Support of global signals and creation of global module

The Verilog netlister connects to global signals using the global module "glbl". This distinguishes global signals from local signals. For example:

```
//Verilog global signals module
module glbl() ;
wire global;
...
endmodule

module schematic1() ;
...
wire global; //local alias for the global signal "global"
assign global = glbl.global;
...
ls04 i1(
.a(global),
...);

...
endmodule
```

By default, only power signals are considered global. Capture inserts the global module at the top of the Verilog netlist.

If your design is a PSpice A/DV design, Capture places the connections to the global signals under `ifdef VAN. This is so that the normal Verilog simulation will not get affected. For example:

```
`ifdef VAN
module glbl;
wire global;
...
endmodule
`endif

module schematic1;

...
`ifdef VAN
wire global; //local alias for the global signal "global"
assign global = glbl.global;
`endif
...
ls04 i1(
`ifdef VAN
```

```
.a(glbl.global),
`else
.a(global),
`endif
...);
...
Endmodule
```

Verilog netlists normally have a .V file extension.

Example Verilog netlist with power pins included

```
`timescale 1ns/1ps

module alias_vector (a, a);
parameter size = 1;
inout [size-1:0] a;
endmodule

module alias_bit (a, a);
inout a;
endmodule

module glbl;
  wire VCC;
  wire GND;
endmodule

module HALFADD ( X, Y, CARRY, SUM);
input X;
input Y;
output CARRY;
output SUM;

// SIGNALS
wire VCC;
assign VCC = glbl.VCC;
wire GND;
assign GND = glbl.GND;
wire N00032;
wire X_BAR;
wire N00034;
wire N5056796111;

// GATE INSTANCES
\74LS32 U1(
  .I0_B( N00032 ) ,
  .I1_B( N00034 ) ,
  .O_B( SUM )
 ) ;

\74LS08 U2(
  .I0_A( X ) ,
  .I1_A( N5056796111 ) ,
  .O_A( N00032 ) ,
  .VCC( VCC ) ,
  .GND( GND ) ,
  .I0_B( Y ) ,
  .I1_B( X_BAR ) ,
  .O_B( N00034 ) ,
  .I0_C( Y ) ,
  .I1_C( X ) ,
```

```
  .O_C( CARRY )
) ;

\74LS04 U3(
  .I_A( X ) ,
  .O_A( X_BAR ) ,
  .VCC( VCC ) ,
  .GND( GND ) ,
  .I_B( Y ) ,
  .O_B( N5056796111 ) ) ;
endmodule

module FULLADD ( SUM, X, Y, CARRY_OUT, CARRY_IN);
output SUM;
input X;
input Y;
output CARRY_OUT;
input CARRY_IN;

// SIGNALS
wire VCC;
assign VCC = glbl.VCC;
wire GND;
assign GND = glbl.GND;
wire N00011;
wire N00013;
wire N00023;

// GATE INSTANCES
\74LS32 U1(
  .I0_A( N00013 ) ,
  .I1_A( N00023 ) ,
  .O_A( CARRY_OUT ) ,
  .VCC( VCC ) ,
  .GND( GND )
 ) ;

HALFADD HALFADD_A (
  .X( CARRY_IN ) ,
  .Y( N00011 ) ,
  .CARRY( N00013 ) ,
  .SUM( SUM )
 ) ;

HALFADD HALFADD_B (
  .X( X ) ,
  .Y( Y ) ,
  .CARRY( N00023 ) ,
  .SUM( N00011 )
 ) ;
endmodule
```

Example Verilog netlist without power pins included

```
`timescale 1ns/1ps

module alias_vector (a, a);
parameter size = 1;
inout [size-1:0] a;
endmodule
```

```
module alias_bit (a, a);
inout a;
endmodule

module glbl;
endmodule

module HALFADD ( X, Y, CARRY, SUM);
input X;
input Y;
output CARRY;
output SUM;

// SIGNALS
wire N00032;
wire X_BAR;
wire N00034;
wire N5056796111;

// GATE INSTANCES
\74LS32 U1(
  .I0_B( N00032 ) ,
  .I1_B( N00034 ) ,
  .O_B( SUM )
) ;

\74LS08 U2(
  .I0_A( X ) ,
  .I1_A( N5056796111 ) ,
  .O_A( N00032 ) ,
  .I0_B( Y ) ,
  .I1_B( X_BAR ) ,
  .O_B( N00034 ) ,
  .I0_C( Y ) ,
  .I1_C( X ) ,
  .O_C( CARRY )
 ) ;

\74LS04 U3(
  .I_A( X ) ,
  .O_A( X_BAR ) ,
  .I_B( Y ) ,
  .O_B( N5056796111 )
 ) ;
endmodule

module FULLADD ( SUM, X, Y, CARRY_OUT, CARRY_IN);
output SUM;
input X;
input Y;
output CARRY_OUT;
input CARRY_IN;

// SIGNALS
wire N00011;
wire N00013;
wire N00023;

// GATE INSTANCES
\74LS32 U1(
  .I0_A( N00013 ) ,
  .I1_A( N00023 ) ,
  .O_A( CARRY_OUT )
 ) ;
```

```
HALFADD HALFADD_A (
  .X( CARRY_IN ) ,
  .Y( N00011 ) ,
  .CARRY( N00013 ) ,
  .SUM( SUM )
 ) ;
HALFADD HALFADD_B (
  .X( X ) ,
  .Y( Y ) ,
  .CARRY( N00023 ) ,
  .SUM( N00011 )
 ) ;
endmodule
```

VHDL netlist format

VHDL netlists have the following characteristics:

- If the 1076-87 VHDL standard is selected, legal characters for node names are limited to:

  `0..9 A..Z a..z _` (underscore)

  with the following limitations:

  - The first character is limited to: `A..Z a..z`
  - The last character restricted from: _ (underscore)
  - If the 1076-93 VHDL standard is selected, you can use special characters, VHDL reserved words, and names that begin with digits. To do so, delimit the name with backslashes (\) and precede any special characters—including "internal" backslashes (not the delimiters)—with a backslash. The following table contains some examples.

Object	Name	Problem	Solution
Node	signal	Reserved Word	\signal\
Node	SIGNAL	Case sensitivity	\SIGNAL\
Pin	Q\	Overbar	\Q\\\
Pin	R\E\S\E\T\	Overbar	\R\\E\\S\\E\\T\\\
Pin	12-GND	Leading digit, hyphen	\12\-GND\

For more information, see the 1076-93 VHDL standard, as well as the list of VHDL reserved words, and the VHDL netlist example.

Note: Do not name the data buses in your design in this format: *datain1 [11..0]*, *datain2 [11..0]*, and so on. Instead use this format for naming the data buses: *dataina [11..0]*, *datainb [11..0]*. Because the VHDL netlister expands the data bits in the port map section and writes it as *datain (111)*.

Schematic attributes in VHDL netlists

You can enter part or net attributes on your schematic for inclusion in the VHDL netlist in one of three ways:

- You can enter attributes (properties) with your own user-defined types.

  To do this, when you assign a property to a part or net in the schematic, you define it thusly:

  ```
  attribute name: name
  attribute value: vhdl_type is value
  ```

  So, for example, to enter a property for the user-defined type part_version, you assign the name and value as follows:

  ```
  attribute name: my_part
  attribute value: part_version is XC1.2
  ```

  The resulting VHDL netlist would include the attribute as follows:

  ATTRIBUTE my_part:part_version
  ATTRIBUTE my_part of PA3 : signal is XC1.2

Note: If you do not define the property's VHDL type in the value field, or if the VHDL type is not defined in the ATTRIBUTE.VHX file, Capture assigns the type "string" to that property.

- You can enter attributes (properties) without a user-defined type.

  To do this, when you assign a property to a part or net in the schematic, you define it thusly:

  ```
  attribute name: name
  attribute value: value
  ```

  So, for example, to enter a property without a user-defined type, you assign the name and value as follows:

  ```
  attribute name: blackbox
  attribute value: no_touch
  ```

The resulting VHDL netlist would include the attribute as follows:

```
ATTRIBUTE blackbox:string
ATTRIBUTE no_touch of PA3 : signal is true
```

- You can enter attributes (properties) that are assigned types in the ATTRIBUTE.VHX file by matching the attribute name with an attribute type that is defined in that file.

  To do this, when you assign a property to a part or net in the schematic, you do not explicitly assign it a type and you use a name that is defined as a particular type in the ATTRIBUTES.VHX file. Thus:

  ```
  attribute name: defined_name
  attribute value: value
  ```

  In this case, Capture checks the contents of the ATTRIBUTE.VHX file, locates the attribute name and associates the type with the attribute name.

  So, for example, to enter a property and assign it a type as defined in the ATTRIBUTE.VHX file, you assign the name and value as follows:

  ```
  attribute name: attribute_syn_preserve
  attribute value: false
  ```

  The property attribute_syn_preserve is defined as type “boolean” in the ATTRIBUTE.VHX file. Therefore, the resulting VHDL netlist would include the attribute as follows:

  ```
  ATTRIBUTE attribute_syn_preserve:boolean
  ATTRIBUTE attribute_syn_preserve of PA3 : signal is false
  ```

Note: The ATTRIBUTE.VHX file is a text file that you can edit to define your own attributes and associated types.

Example

This netlist was created with no options selected. VHDL netlists normally have a .VHD file extension.

```
LIBRARY IEEE;
USE IEEE.std_logic_1164.all;

ENTITY EX6B IS PORT (
X : IN std_logic;
Y : IN std_logic;
CARRY : OUT std_logic;
SUM : OUT std_logic
); END EX6B;

ARCHITECTURE STRUCTURE OF EX6B IS
```

```
-- COMPONENTS

COMPONENT \74LS32\
PORT (
I0_A : IN std_logic;
I1_A : IN std_logic;
O_A : OUT std_logic;
VCC : IN std_logic;
GND : IN std_logic;
I0_B : IN std_logic;
I1_B : IN std_logic;
O_B : OUT std_logic;
I0_C : IN std_logic;
I1_C : IN std_logic;
O_C : OUT std_logic;
I0_D : IN std_logic;
I1_D : IN std_logic;
O_D : OUT std_logic
); END COMPONENT;

COMPONENT \74LS08\
PORT (
I0_A : IN std_logic;
I1_A : IN std_logic;
O_A : OUT std_logic;
VCC : IN std_logic;
GND : IN std_logic;
I0_B : IN std_logic;
I1_B : IN std_logic;
O_B : OUT std_logic;
I0_C : IN std_logic;
I1_C : IN std_logic;
O_C : OUT std_logic;
I0_D : IN std_logic;
I1_D : IN std_logic;
O_D : OUT std_logic
); END COMPONENT;

COMPONENT \74LS04\
PORT (
I_A : IN std_logic;
O_A : OUT std_logic;
VCC : IN std_logic;
GND : IN std_logic;
I_B : IN std_logic;
O_B : OUT std_logic;
I_C : IN std_logic;
O_C : OUT std_logic;
I_D : IN std_logic;
O_D : OUT std_logic;
I_E : IN std_logic;
O_E : OUT std_logic;
I_F : IN std_logic;
O_F : OUT std_logic
); END COMPONENT;

-- SIGNALS

SIGNAL X_BAR : std_logic;
SIGNAL N00037 : std_logic;
SIGNAL N00035 : std_logic;
SIGNAL GND : std_logic;
```

```
SIGNAL VCC : std_logic;
SIGNAL N5056796111 : std_logic;

-- GATE INSTANCES

BEGIN
U1 : \74LS32\ PORT MAP
I0_A => 'Z',
I1_A => 'Z',
O_A => OPEN,
VCC => OPEN,
GND => OPEN,
I0_B => N00035,
I1_B => N00037,
O_B => SUM,
I0_C => 'Z',
I1_C => 'Z',
O_C => OPEN,
I0_D => 'Z',
I1_D => 'Z',
O_D => OPEN
);

U2 : \74LS08\ PORT MAP(
I0_A => X,
I1_A => N5056796111,
O_A => N00035,
VCC => VCC,
GND => GND,
I0_B => Y,
I1_B => X_BAR,
O_B => N00037,
I0_C => Y,
I1_C => X,
O_C => CARRY,
I0_D => 'Z',
I1_D => 'Z',
O_D => OPEN
);

U3 : \74LS04\ PORT MAP(
I_A => X,
O_A => X_BAR,
VCC => VCC,
GND => GND,
I_B => Y,
O_B => N5056796111,
I_C => 'Z',
O_C => OPEN,
I_D => 'Z',
O_D => OPEN,
I_E => 'Z',
O_E => OPEN,
I_F => 'Z',
O_F => OPEN
);

END STRUCTURE;

LIBRARY IEEE;
USE IEEE.std_logic_1164.all;

ENTITY FULLADD IS PORT (
SUM : OUT std_logic;
```

```
X : IN std_logic;
Y : IN std_logic;
CARRY_OUT : OUT std_logic;
CARRY_IN : IN std_logic
); END FULLADD;

ARCHITECTURE STRUCTURE OF FULLADD IS

-- COMPONENTS

COMPONENT \74LS32\
PORT (
I0_A : IN std_logic;
I1_A : IN std_logic;
O_A : OUT std_logic;
VCC : IN std_logic;
GND : IN std_logic;
I0_B : IN std_logic;
I1_B : IN std_logic;
O_B : OUT std_logic;
I0_C : IN std_logic;
I1_C : IN std_logic;
O_C : OUT std_logic;
I0_D : IN std_logic;
I1_D : IN std_logic;
O_D : OUT std_logic
); END COMPONENT;

COMPONENT EX6B PORT (
X : IN std_logic;
Y : IN std_logic;
CARRY : OUT std_logic;
SUM : OUT std_logic
); END COMPONENT;

-- SIGNALS

SIGNAL N00015 : std_logic;
SIGNAL N00013 : std_logic;
SIGNAL N00025 : std_logic;
SIGNAL VCC : std_logic;
SIGNAL GND : std_logic;

-- GATE INSTANCES

BEGIN
U1 : \74LS32\&#9;PORT MAP
I0_A => N00015,
I1_A => N00025,
O_A => CARRY_OUT,
VCC => VCC,
GND => GND,
I0_B => 'Z',
I1_B => 'Z',
O_B => OPEN,
I0_C => 'Z',
I1_C => 'Z',
O_C => OPEN,
I0_D => 'Z',
I1_D => 'Z',
O_D => OPEN
);

halfadd_A : EX6B PORT MAP(
X => CARRY_IN,
```

```
Y => N00013,
CARRY => N00015,
SUM => SUM
);
halfadd_B : EX6B PORT MAP(
X => X,
Y => Y,
CARRY => N00025,
SUM => N00013
);
END STRUCTURE;
```

VST Model netlist format

This format file produces netlists for modeling with OrCAD's Digital Simulation Tools 386+. See the *Digital Simulation Tools User's Guide* for details.

VST Model netlists have the following characteristics:

- Part names, module names, reference strings, node names, and pin numbers are not checked for length.
- Node numbers and pin names are not used.
- All ASCII characters are legal.

For more information, see the VST netlist example.

VST netlist constraints

When you create a VST Model netlist, be sure you include the OrCAD-supplied VSTGATES.OLB, VSTRAM.OLB, VSTROM.OLB, and VSTOTHER.OLB part libraries in your project. You can use only the parts provided in these libraries to create the schematic folder.

VST pipe commands

Lines of text may be placed on your schematic page to be included in the VST Model netlist. Select the Text command from the Place menu to place the text on a schematic page.

Each line of text must start with the pipe character (|). The first line must be:

```
|VST_MODEL
```

This tells Capture to extract the information in the following lines of text when generating a VST Model netlist. The remaining lines can contain a header, comments, and directives compatible with OrCAD's Digital Simulation Tools 386+ Add Device Model device modeling language. For details on the Add Device Model Language, see the *Digital Simulation Tools User's Guide*.

WinBoard netlist format

Ivex WinBoard netlists have the following characteristics:

- Part names are not checked for length.
- Module names are not checked for length.
- Reference strings are not checked for length.
- Node names are limited to eight characters.
- Node numbers are limited to five digits following the "N" prefix.
- Pin numbers are not checked for length.

For more information see the WinBoard netlist example.

Example

WinBoard netlists normally have an .NET file extension.

```
WINBOARD 1.01
`I "ORCAD CAPTURE 7.20";
`F "D:\ORCAD DEMO\CAPTURE\NETLIST
UPDATES\DESIGN1\FIG_B-01.SCH";
`T "Generic Netlist Example";
`S "Thursday, November 12, 1998";
`C "OrCAD-01";
`R "A";
`C "OrCAD";
`C "9300 S.W. Nimbus Ave.";
`C "Beaverton, OR 97008";
`C "(503) 671-9500 Corporate Offices";
`C "(503) 671-9400 Technical Support";
`M 14DIP300,,74LS00,6CB84CBA,U1,C,GR1
(1 A IN A1)
(2 A IN A1)
(3 N00019 OU A1)
(4 B IN A1)
(5 N00013 IN A1)
(6 Q OU A1)
(7 GND PO A1)
```

```
(8 N00013 OU A1)
(9 Q IN A1)
(10 CLOCK IN A1)
(11 ?1 OU A1)
(12 ?2 IN A1)
(13 ?3 IN A1)
(14 VCC PO A1)
;
`M 14DIP300,,74LS32,6E46169D,U2,C,GR1
(1 N00019 IN A1)
(2 Q IN A1)
(3 OUT OU A1)
(4 ?4 IN A1)
(5 ?5 IN A1)
(6 ?6 OU A1)
(7 GND PO A1)
(8 ?7 OU A1)
(9 ?8 IN A1)
(10 ?9 IN A1)
(11 ?10 OU A1)
(12 ?11 IN A1)
(13 ?12 IN A1)
(14 VCC PO A1)
;
```

WireList netlist format

WireList netlists have the following characteristics:

- Part and node names are not checked for length.
- Module names are limited to twenty-nine characters.
- Reference strings are limited to nine characters.
- Node numbers are limited to five digits following the "N" prefix.
- Pin numbers are limited to seven characters.
- Pin names are limited to fifteen characters.
- Legal characters for node numbers are `0..9`.
- Legal characters for pin numbers are `0..9`, unless the option Do not output pin numbers for Grid Array parts is selected. If you select this option, Capture skips nonnumeric pin numbers, such as those on grid array parts, and any ASCII character is legal.
- All ASCII characters are legal except as noted for node numbers and pin numbers.

Note: WireList netlists generated by Capture use all uppercase letters for pin names, pin numbers, and net names.

For more information, see the WireList netlist example.

Example

WireList netlists normally have an .NET file extension.

```
Wire List

Generic Netlist Example Revised: Thursday, November 12, 1998
OrCAD-01 Revision: A
OrCAD
9300 S.W. Nimbus Ave.
Beaverton, OR 97008
(503) 671-9500 Corporate Offices
(503) 671-9400 Technical Support

<<< Component List >>>
74LS00 U1 14DIP300
74LS32 U2 14DIP300

<<< Wire List >>>

  NODE REFERENCE PIN # PIN NAME PIN TYPE PART VALUE

[00001] GND
  U1 7 GND Power 74LS00
  U2 7 GND Power 74LS32

[00002] VCC
  U1 14 VCC Power 74LS00
  U2 14 VCC Power 74LS32

[00003] CLOCK
  U1 10 I1_C Input 74LS00

[00004] Q
  U1 6 O_B Output 74LS00
  U2 2 I1_A Input 74LS32
  U1 9 I0_C Input 74LS00

[00005] OUT
  U2 3 O_A Output 74LS32

[00006] B
  U1 4 I0_B Input 74LS00

[00007] N00019
  U1 3 O_A Output 74LS00
  U2 1 I0_A Input 74LS32

[00008] N00013
  U1 5 I1_B Input 74LS00
  U1 8 O_C Output 74LS00

[00009] A
  U1 1 I0_A Input 74LS00
  U1 2 I1_A Input 74LS00
```

F

Additional Capture Utilities

Myriad Capture Viewer

Myriad Capture Viewer enables PCB designers, design managers, and end-users to share native schematic files. With Capture Viewer, you can view/review OrCAD Capture schematics without changing the original design. This utility has been developed by Informative Graphics®, MYRIAD® and is available free of cost. To download the viewer and for more information, go to the downloads area of www.cadence.com/orcad.

OrCAD ViewReader

You use the OrCAD ViewReader to convert Viewlogic ViewDraw designs in OrCAD Capture or Capture CIS v7.2 or later. To download the viewer and for more information, go to the downloads area of www.cadence.com/orcad.

Library Correction Utility

Using the Library Correction Utility, you can:

- Verify and correct missing pin numbers and duplicate pin names in the Capture symbol library.
- Change all lowercase pin numbers and pin names to uppercase in the Capture symbol library.
- Make all Power pins visible in the Capture symbol library.

This utility scans through all the parts in the library, and finds out and corrects the components that have missing pin numbers and duplicate logical pin names, converts components with lowercase pin numbers and pin names to uppercase, and makes the Power pins visible for components.

See Appendix G, “Library Correction Utility,” for more information.

Push Occurrence Properties into Instance Utility

Suppose that you copied a circuit or part of a circuit from design A and pasted it in design B. You might see occurrence and instance level properties with different values on the pasted parts in design B. In previous releases of Capture, you had to invoke the property editor on each part, copy and paste the occurrence property values of the Part Reference, PCB Footprint property and any other property as instance property values, and remove occurrence properties.

The Push Occurrence Properties into Instance Utility allows you to automatically do this. It automatically:

- transfers occurrence property values of the part reference and PCB footprint properties as instance level property values
  - removes all occurrence properties from the design and sets the preferred mode of the design to instance (if you select the Remove occurrence level properties check box).
- transfer occurrence property values of flat nets to schematic nets.

To run this utility, from the Accessories menu in Capture, choose Push Occ. Prop into Instance, then choose Transfer Occ. Prop. to Instance.

See Push Occ. properties to instance dialog box for more information.

G

Library Correction Utility

Overview

The Library correction utility is a new feature in Capture 10.0. This utility automatically verifies/corrects missing pin numbers and duplicate pin names in the Capture symbol library by scanning through all the parts in the library, finding out, and correcting the components that have missing pin numbers and duplicate logical pin names.

This utility also converts components with lowercase pin names to uppercase and makes the Power pins visible for all the components in the library

To run the Library correction utility, from the Accessories menu in Capture, choose LibCorrectionUtil, then Library Verification/Correction.

Verification Vs Correction

If you select Verify, the utility verifies the library for the Missing Pin Numbers and/or Duplicate pin names depending on your selection, and generates a log file.

If you select Correct, the utility will correct the library for Missing Pin numbers and/or Duplicate Pin names depending on the selection, and generates a log file.

Note that when you opt for correction, the library will get corrected, so if you want to have the copy of old library you need back-up the library. In fact it would be always safe to make a back-up of the old library before correcting the library.

Missing Pin numbers option

When you check this option, this library correction utility will scan through all the parts in the library and find out the components that have missing pin numbers.

All the missing pin numbers get updated by their corresponding pin names. At the end of updating process this utility will pop up message: "Corrected <number of parts corrected> of Parts in <lib_path>/<lib_name>.olb for missing pin numbers" or "No Part in this library has missing pin numbers".

The log file is generated at the location where the selected library is residing. The naming convention used for log files is <Library_name>Miss.log. The log file lists all the parts and also the pin numbers for each of the corrected part in the library. If user chooses the Verify option, only the log file is generated but the library is not updated.

Missing pins Log File Example:

```
List of verified / corrected packages
CONNECTOR DB25
        No missing Pin numbers
CAPACITOR NON-POL
        CAPACITOR NON-POL.Normal1
        CAPACITOR NON-POL.Normal2


1 parts in library C:\TEMP\MISSINGPIN_NUMBERS.OLB have
missing pin numbers.
```

The last line of the log file shown above indicates that one part in the MISSINGPIN_NUMBERS.OLB library has missing pin numbers. The pin names for the missing pin numbers are 1, 2.

Duplicate Pin names option

When you check this option, the utility will scan through all the parts in the library and find out the components that have duplicate logical pin names. If a component has duplicate power pin names, those pins are not considered as duplicate pin names.

To remove duplicate pin names, the library correction utility changes the duplicate pin names by appending "#" followed by the pin number to the duplicate pin names. The combination of the pin name and the pin number makes the pin name unique. Note that the first pin that this utility encounters does not get appended with # followed by its pin number. At the end of updating process this utility will pop up message: "Corrected <number of parts corrected> of Parts in <lib_path>/<lib_name>.olb for duplicate pin names" or "No Part in this library has duplicate pin names".

The log file is generated at the location where the selected library is residing. The naming convention used for log files is <Library_name>Dup.log. The log file lists all the parts and also the corrected pin names for each of the corrected part in the library. If user chooses the Verify option, only the log file is generated but the library is not updated.

Duplicate Logical pins Log File Example:

```
List of verified / corrected packages

ASSYMETRICAL

               ASSYMETRICALAA.Normal2A#2

               ASSYMETRICALCC.Normal8A\#8

74LS00

               No duplicate Pin names


1 parts in library C:\TEMP\DUPLICATE_PIN_NAMES.OLB have
     duplicate pin names
```

The last line of the log file shown above indicates that one part in the DUPLICATE_PIN_NAMES.OLB library has duplicate pin names. The corrected pin names are A#2 and A\#8.

Change the Pin name and number to uppercase option

When you check this option, the utility will scan through all the parts in the library and convert all the components that have pin names appearing in lowercase to uppercase.

At the end of updating process this utility will pop up message: "Changed all the Pin name to upper case. Please close the library and reopen to see the change."

Make All Power Pins Visible option

When you check this option, the utility will scan through all the parts in the library and change the Power pins settings for all the non-zero length pins in the library to *Visible*. Additionally, you can also make all zero length Power pins in the library visible. To do this, check the Change Zero Length Pins to check box and choose an appropriate pin shape option (Line/Short) from the list box.

Note: The Change Zero Length Pins to check box is available only, if the Make All Power Pins Visible check box is checked.

At the end of updating process this utility will pop up message: " Made all the Power Pins visible. Please close the library and reopen to see the change.“

What is the Use of This Utility in Flow?

In Capture-PCB Editor flow, new Capture-PCB Editor interface gives "Error ALG0031" if any of the components on your design have missing pin numbers. Old third party interface used to netlist the null pin number as pin name and take the component through flow, but that was not the proper way because the component was not updated at all.

In Capture-PCB Editor Flow, new Capture-PCB Editor interface gives "Error ALG0050" if any of the components on your design have duplicate pin names.

What is the Use Model for Capture-PCB Editor Flow?

For New Designs:

Run this utility on library files, for correcting missing pin numbers and duplicate pin names, then use these libraries in creating new designs. After correcting the libraries you will not encounter the ALG0031 and ALG0050 Errors.

Correcting Existing Designs:

Run this utility on library files for correcting missing pin numbers and duplicate pin names, then use the update cache command from the Capture Design Menu.

What if you do not have libraries for Existing Design?

Though this is not the preferred way, you can copy all design cache components to a new library and then run this utility on that library. Now use Replace Cache command from Design menu. In this process please note that, design cache will point to single library after using replace cache, and this will effect the Canonical Path in pst* files, as source library name is embedded in the Canonical path.

1. Copy all design cache components to a new library.
2. Run the library correction utility on the new library, created in step 1.
3. Use Replace Cache command from Design menu.

Assumption:

This utility will put pin name in place of empty pin number. Matching foot print is users responsibility, as in some cases footprint may not match with pin numbers if we copy pin name like in the following example

Pin number	Pin name
1	A
	B
3	C
4	D

Now this utility will copy B to missing pin number. Now in this case footprint should contain pin numbers as 1,B,3,4 NOT 1,2,3,4

Known Limitation:

Suppose if all pin types other than Power, have duplicate pin names and missing pin numbers, then the missing pin numbers functionality will copy the pin names in place of missing pin numbers. Next, the Duplicate pin names functionality will append the pin names to pin numbers followed by #, still pin names will not be unique. This will generate Error ALG0050. For these parts, user would need to edit each part and create unique pin names for each pin type other than the Power pin type.

H

Database Migration

Overview

Capture CIS, v16.3, ships with a new design and library database schema version. This new data format improves application performance and ensures data integrity in your Capture designs and libraries. If you currently have designs and libraries developed in a previous version of Capture, you can automatically upgrade these using v16.3. This section provides a brief overview of the scenarios and application prompts you may encounter when upgrading your designs and libraries to v16.3.

Note: In this section, the Capture version v16.2 refers to Capture versions prior to and including v16.2.

Note: The data format used in Capture versions prior to and including v16.2 is v9.0.

Upgrade Matrix

The following version matrix provides a quick glance and the possible Design versus Application versus Library version scenarios while upgrading your environment from v16.2 to v16.3.

Application Version	Design Version	External Referred Design Version	Library Version	Is Supported? (YES / NO)
v16.3	v16.3		v16.2	**YES** Recommendation to upgrade Library ***See Capture v16.2 Library in Capture v16.3***
v16.3	v16.2		v16.3	**YES** Recommendation to upgrade Design ***See Capture v16.2 Design in Capture v16.3***
v16.3	v16.3		v16.3	**YES** Recommended
v16.3	Any	v16.3	Any	**YES** Recommended
v16.3	Any	v16.2	Any	**YES** Recommendation to upgrade Referred Design ***See Capture v16.3 Design with Externally Referenced v16.2 Design***
v16.2	v16.3		v16.3	**YES** ***See Downgrade v16.3 Design or Library***
v16.2	v16.3		v16.2	**YES** ***See Downgrade v16.3 Design or Library***

Application Version	Design Version	External Referred Design Version	Library Version	Is Supported? (YES / NO)
v16.2	v16.2		16.3	**YES** ***See Downgrade v16.3 Design or Library***

Table H-1

Upgrade Batch Script

You can use a TCL batch script provided by Cadence to upgrade your v16.2 designs and libraries to v16.3. Please contact Cadence Customer Support for details.

Capture v16.2 Design in Capture v16.3

This scenario arises when you install Capture v16.3 and you currently have Capture designs in v16.2.

Opening v16.2 design in Capture v16.3

As soon as you open a v16.2 design in Capture v16.3, the application prompts you to upgrade the design.

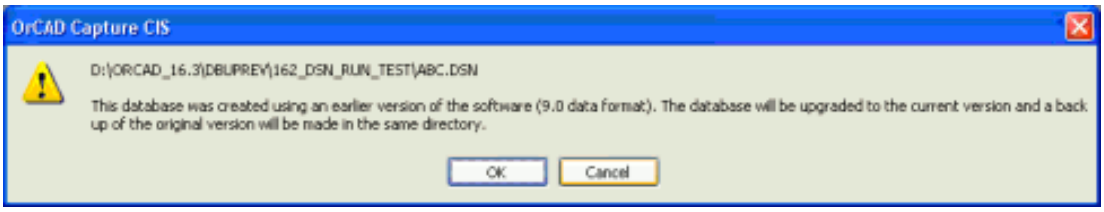


Figure H-1

Choose OK to upgrade the design.

Note: If you choose Cancel, the design will not open in v16.3.

Capture v16.2 Library in Capture v16.3

This scenario arises when you install Capture Release 16.3 and you currently have Capture libraries in v16.2.

Saving v16.2 library in Capture v16.3

When you save a v16.2 library opened in v16.3, the application prompts you to upgrade the library.

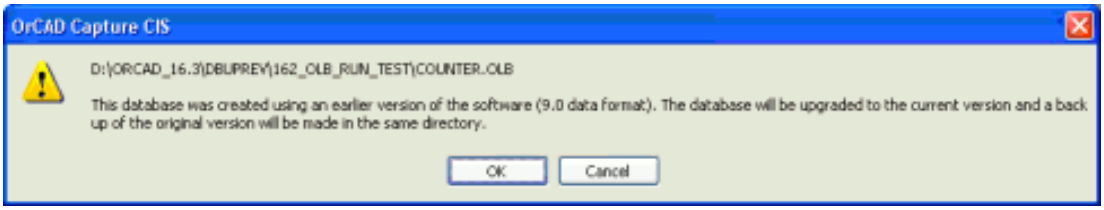


Figure H-2

Choose OK to upgrade the library.

Note: If you choose Cancel, the library will not be saved.

Closing (or exiting Capture) v16.2 library in Capture v16.3

When you close a v16.2 library opened in Capture v16.3 or when you exit Capture after opening a v16.2 library, the application prompts you to upgrade the library,

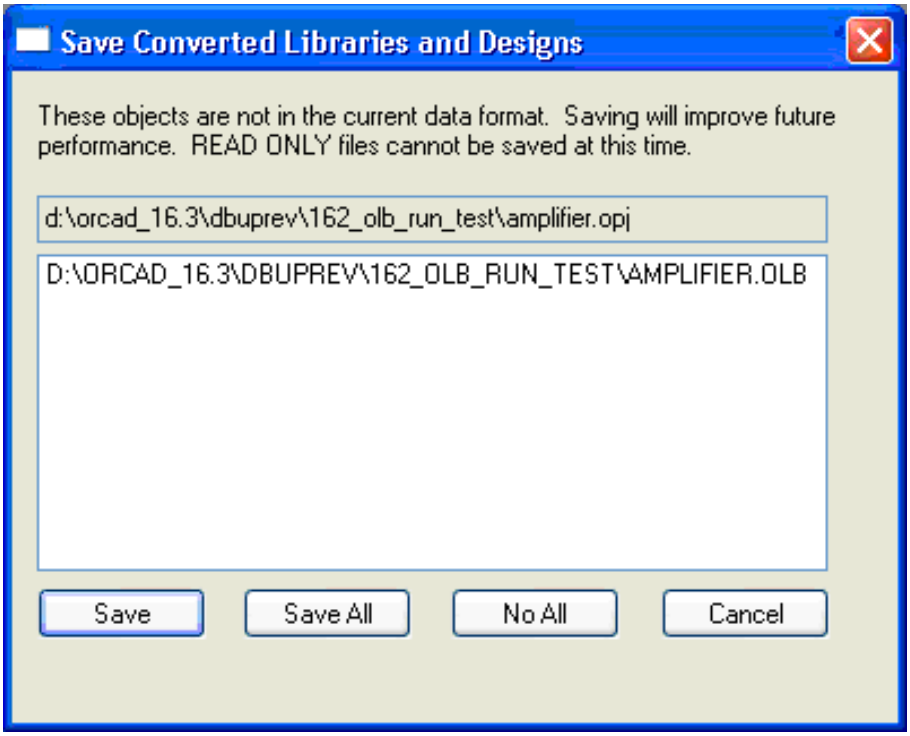


Figure H-3

The Save Converted Libraries and Designs dialog displays the list of the v16.2 libraries.

The Save Converted Libraries and Designs dialog displays the list of the v16.2 libraries.

Choose **Save All** to upgrade all the listed libraries.

Choose **No All** to not upgrade any of the listed libraries.

Note: The Cancel option is only available if you close the library and not when you exit the application.

Note: When you open a v16.2 design in v16.3, Capture prompts you to upgrade the design. However, this does not happen when you open a v16.2 library in v16.3. In this case, you will only be prompted to upgrade the library if you choose the Save command, close the project or close Capture.

Note: If the v16.2 library is in Read Only mode, you will not be able to save and hence upgrade the library.

Capture v16.3 with v16.2 Referenced Libraries

This scenario arises when v16.2 libraries are referenced through the Place Part dialog in Capture. This occurs either if v16.2 libraries are configured in the Capture INI OR when you select v16.2 libraries through the Add Library command in the Place Part dialog.

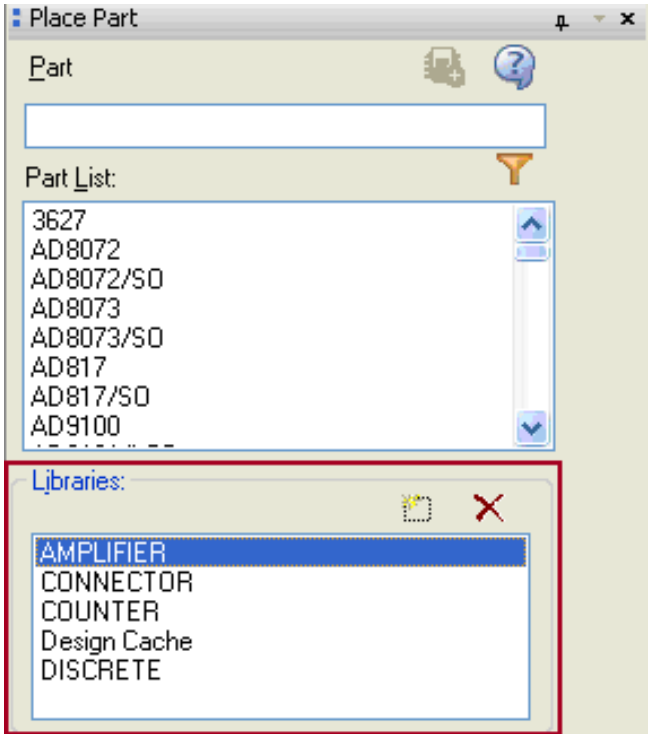


Figure H-4

Exiting Capture v16.3 with v16.2 referenced libraries

When you refer v16.2 libraries in Capture v16.3, on exit the application prompts you to upgrade these libraries.

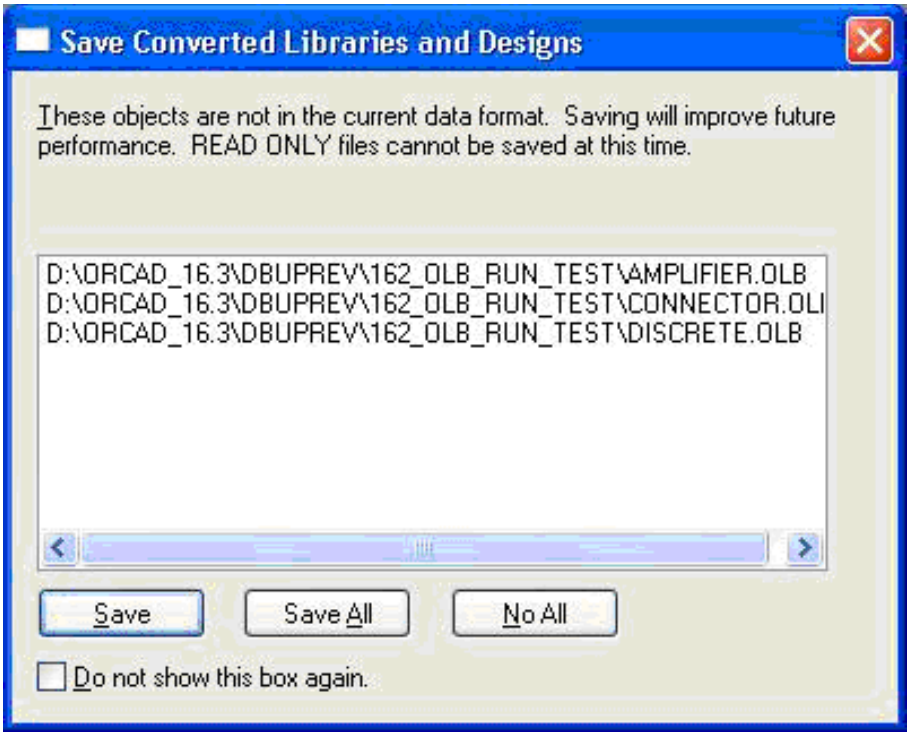


Figure H-5

The Save Converted Libraries and Designs dialog displays the list of all the v16.2 libraries.

Select specific libraries from the list and choose Save to upgrade the selected libraries.

Choose **Save All** to upgrade all the listed libraries.

Choose **No All** to not upgrade any of the listed libraries.

Check the **Do not show this box again** option to retain your current selection.

> For example, if you select this option and then choose Save All, then whenever this scenario arises, this dialog box will not be displayed and the libraries will be upgraded automatically on exit.

Note: If a v16.2 referenced library is in Read Only mode, you will not be able to save and hence upgrade the library.

Note: If you perform library-specific commands like Update Cache or Replace Cache in Capture v16.3, the libraries will not be upgraded.

Capture v16.3 Project with v16.2 Libraries included

This scenario arises when you have a v16.3 project with one or more v16.2 libraries added to the project.

Note: You add a library in a Capture project by choosing Add File from the pop-up menu on the Library folder in Project Manager.

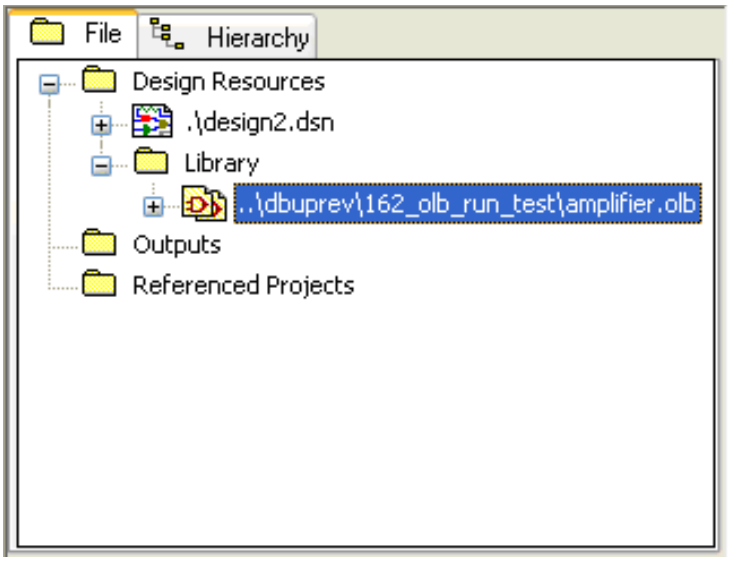


Figure H-6

Saving v16.2 Library included in v16.3 Project

When you save a v16.2 library that is included in a v16.3 project, the application prompts you to upgrade the library.

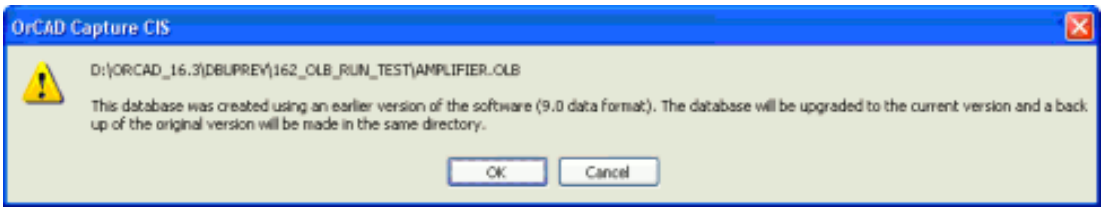


Figure H-7

Choose **OK** to upgrade the library.

Note: If you choose Cancel, the library will not be saved.

Closing (or exiting Capture) v16.3 project with added v16.2 library

When you close a v16.3 project to which you have added one or more v16.2 libraries, the application prompts you to upgrade the added libraries.

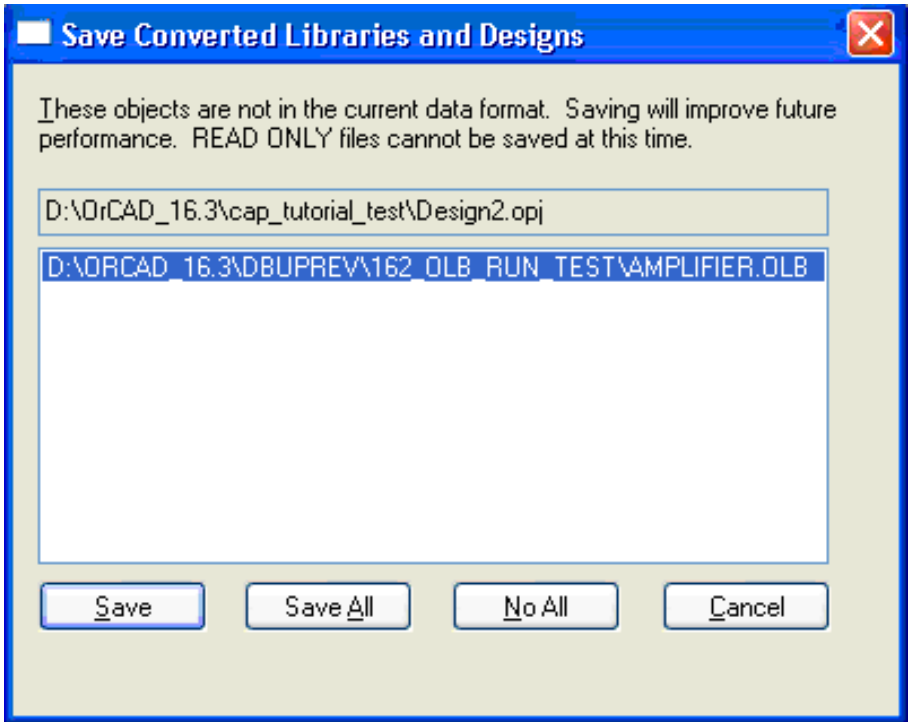


Figure H-8

The Save Converted Libraries and Designs dialog displays the list of all the v16.2 libraries.

Select specific libraries from the list and choose Save to upgrade the selected libraries.

Choose **Save All** to upgrade all the listed libraries.

Choose **No All** to not upgrade any of the listed libraries.

Note: The **Cancel** option is only available if you close the project and not when you exit the application.

Note: If a v16.2 configured library is in **Read Only** mode, you will not be able to save and hence upgrade the library.

Capture v16.3 Design with Externally Referenced v16.2 Design

This scenario arises when you have a v16.3 design that contains an external reference to a v16.2 design. For example, a v16.3 design with a hierarchical block that references a external v16.2 design or a v16.3 design with a hierarchical part that reference a v16.2 schematic.

Exiting Capture v16.3 design with Externally Referenced v16.2 Design

If you have a v16.3 design that contains an external reference to a v16.2 design and you close Capture, the application prompts you to upgrade the externally referenced design.

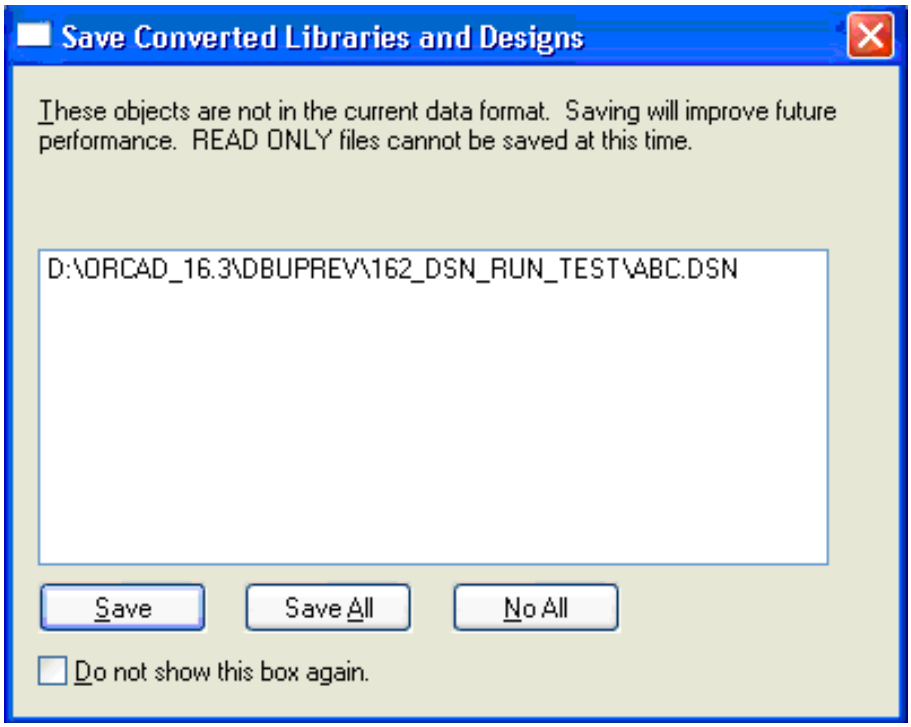


Figure H-9

The Save Converted Libraries and Designs dialog displays the list of the externally referenced designs.

Select specific design from the list and choose Save to upgrade the selected designs.

Choose **Save All** to upgrade all the listed designs.

Choose **No All** to not upgrade any of the listed designs.

Check the **Do not show this box again** option to retain your current selection.

For example, if you select this option and then choose Save All, then whenever this scenario arises, this dialog box will not be displayed and the Save All option will be executed.

Important

If you open a v16.3 design with a v16.2 externally referenced design and you descend to the v16.2 design (by choosing the Descend Hierarchy command), the v16.2 design is upgraded to v16.3 and a backup of the v16.2 design is made in the same location as the original v16.2 design.

Opening a v16.3 Design or Library in Capture v16.2

This down-grade scenario arises when you need to open a v16.3 library or design in v16.2.

Downgrade v16.3 Design or Library

To make a v16.3 design or library available for use in v16.2, you need to downgrade your design or library.

To downgrade a v16.3 design or library, choose the File - Save As menu option.

In the **Save As** dialog, choose the 16.2 Design / Library file type option.

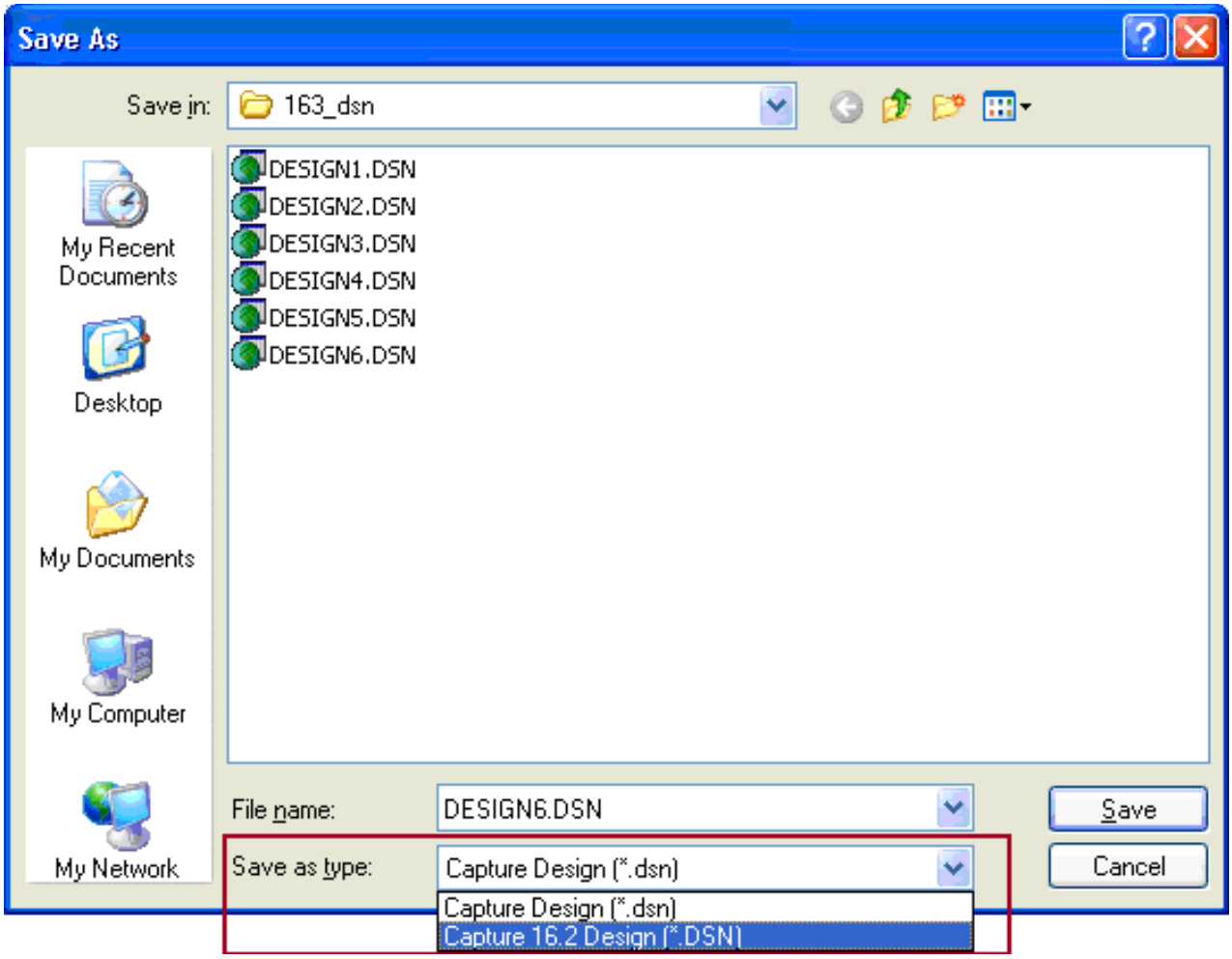


Figure H-10

You can now open the design or library in v16.2.

Important

Capture v16.3 enhancements like user-defined pin shapes, color wire and color part, Bezier curves, OLE object support, will not be available in a design that is down-graded from v16.3 to v16.2. So, you are recommended to down-grade designs with caution as you may lose data in the down-grade.

Upgraded Design & Library backup

Design Backup

When a v16.2 design is upgraded, a backup of the design file (.DSN) is made in the same location using the nomenclature - <Design Name (excluding file extension)> _9_0_0.DBK. You can then rename this backup file with a .DSN extension to make it available for use in Capture v16.2.

Library Backup

When a v16.2 library is upgraded, a backup of the library file (.OLB) is made in the same location using the nomenclature - <Library Name (excluding file extension)> _9_0_0.OBK. You can then rename this backup file with a .OLB extension to make it available for use in Capture v16.2.

NetGroup / Bus Member Net Generation

Overview

In a design that contains multiple NetGroups and buses, if you short two of these objects together, the signal output of the short depends on the definition of the objects.

Important

If you short together buses and NetGroups, the resultant signal will be generated by the object with higher significance (as described in this section). In this section, the term **Winning Bus** is used to specifiy the object (bus or NetGroup) that defines the resultant signals in the connectivity of a design. This term is used in the case of a bus as well as a NetGroup.

Net Generation Scenarios

When you short a bus/NetGroup to a bus/NetGroup, the short will result in:

- a resultant object (bus or NetGroup)
- a winning bus
- the flat nets generated from the short
- the associated NetGroup definition (in case a NetGroup is involved in the short)

This table describes scenarios that you encounter when you short together NetGroups and buses in a Capture design. The table is followed by one example for each of the described scenarios.

Short	Generated Object (*Bus or NetGroup*)	Winning Bus	Generated Flat Nets	Defintion
Bus & Bus (different width)	Bus	Higher width bus	Follow lexicographic order	NA
EXAMPLE Bus A[0:3] - Members: A0, A1, , A2, A3 Bus B[0:5] - Members: B0, B1, B2, B3, B4, B5				
	B[0..5]	B[0..5]	A0 A1 A2 A3 B4 B5	NA
NetGroup & NetGroup - physical short (different width)	NetGroup	Higher width NetGroup	Winning Bus defines flat nets	associated NetGroup definition should match winning bus
EXAMPLE NetGroup S[0..5] - Members: S.JTAG0, S.JTAG1 ,S.JTAG2 ,S.JTAG3, S.JTAG4, S.JTAG5 NetGroup B[0:2] - Members: B.B0, B.B1, B.B2				
	S[0..5]	S[0..5]	S.JTAG0, S.JTAG1, S.JTAG2, S.JTAG3, S.JTAG4, S.JTAG5	S[0..5]
NetGroup & NetGroup - logical short (different width)	NetGroup	Higher width NetGroup	Winning Bus defines flat nets	associated NetGroup definition should match winning bus
EXAMPLE NetGroup S[0..5] - Members: S.JTAG0, S.JTAG1 ,S.JTAG2 ,S.JTAG3, S.JTAG4, S.JTAG5 NetGroup B[0:2] - Members: B.B0, B.B1, B.B2				

Short	Generated Object (*Bus or NetGroup*)	Winning Bus	Generated Flat Nets	Defintion
	S[0..5]	S[0..5]	S.JTAG0, S.JTAG1, S.JTAG2, S.JTAG3, S.JTAG4, S.JTAG5	S[0..5]

Important

In the case of a logical (named) connection:

- if the NetGroups aliases are different, the NetGroups are shorted together.
- if the associated NetGroup definitions are the same, the NetGroups are shorted together.

NetGroup & NetGroup (same width)	NetGroup	Lexicographically smaller NetGroup	Winning Bus defines flat nets	associated NetGroup definition should match winning bus

EXAMPLE

NetGroup S[0..2] - Members: S.JTAG0, S.JTAG1 ,S.JTAG2

NetGroup B[0..2] - Members: B.B0,B.B1 and B.B2

NetGroup & NetGroup - logical short (same width)	NetGroup	Lexicographically smaller NetGroup	Winning Bus defines flat nets	associated NetGroup definition should match winning bus

EXAMPLE

NetGroup S[0..2] - Members: S.JTAG0, S.JTAG1 ,S.JTAG2

NetGroup B[0..2] - Members: B.B0,B.B1 and B.B2

Important

In the case of a logical (named) connection, if the aliases names of both the NetGroups is the same, only then will the two NetGroups be shorted together.

	B[0..2]	B[0..2]	B.B0,B.B1 and B.B2	B[0..2]

Short	Generated Object (*Bus or NetGroup*)	Winning Bus	Generated Flat Nets	Defintion
Bus & NetGroup (NetGroup width higher)	NetGroup	NetGroup	Winning Bus defines flat nets	associated NetGroup definition should match winning bus
EXAMPLE NetGroup S[0..5] - Members: S.JTAG0, S.JTAG1, S.JTAG2, S.JTAG3, S.JTAG4, S.JTAG5 Bus B[0:2] - Members: B.B0, B.B1, B.B2				
	S[0..5]	S[0..5]	S.JTAG0, S.JTAG1, S.JTAG2, S.JTAG3, S.JTAG4, S.JTAG5	S[0..5]
Bus & NetGroup (Bus width higher)	Hybrid Bus (Bus+NetGroup)	Higher width NetGroup	Winning Bus defines flat nets	associated NetGroup definition should match winning bus
EXAMPLE NetGroup S[0..2] - Members: S.JTAG0, S.JTAG1, S.JTAG2 Bus B[0:5] - Members: B.B0, B.B1, B.B2, B.B3, B.B4, B.B5				
	B[0..5]	B[0..5]	B.JTAG0, B.JTAG1, B.JTAG2, B3, B4 and B5	S[0..2]
Bus & NetGroup (same width)	NetGroup	NetGroup	Winning Bus defines flat nets	associated NetGroup definition should match winning bus
EXAMPLE NetGroup S[0..2] - Members: S.JTAG0, S.JTAG1 ,S.JTAG2 Bus B[0:2] - Members: B.B0, B.B1, B.B2				

Short	Generated Object (*Bus or NetGroup*)	Winning Bus	Generated Flat Nets	Defintion
	S[0..5]	S[0..5]	S.JTAG0, S.JTAG1, S.JTAG2	S[0..5]
NetGroup wire & NetGroup OPC/GLOBAL/PORT (different widths)	NetGroup	NetGroup OPC/GLOBAL /PORT	Winning Bus defines flat nets	associated NetGroup definition should match winning bus
EXAMPLE NetGroup S[0..5] - Members: S.JTAG0, S.JTAG1 ,S.JTAG2, S.JTAG3, S.JTAG4, S.JTAG5 NetGroup OPC B[0..2] - Members: B.B0, B.B1, B.B2				
	B[0..2]	B[0..2]	B.B0, B.B1, S.JTAG2, S.JTAG3, S.JTAG4, S.JTAG5	B[0..2]
Bus & NetGroup OPC/GLOBAL/PORT (NetGroup width higher)	NetGroup	NetGroup OPC/GLOBAL /PORT	Winning Bus defines flat nets	associated NetGroup definition should match winning bus
EXAMPLE NetGroup OPC S[0..5] - Members: S.JTAG0, S.JTAG1, S.JTAG2, S.JTAG3, S.JTAG4, S.JTAG5 Bus B[0:2] - Members: B.B0, B.B1, B.B2				
	S[0..5]	S[0..5]	S.JTAG0, S.JTAG1, S.JTAG2, S.JTAG3, S.JTAG4, S.JTAG5	S[0..5]
Bus & NetGroup OPC/GLOBAL/PORT (bus width higher)	NetGroup	NetGroup OPC/GLOBAL /PORT	Winning Bus defines flat nets	associated NetGroup definition should match winning bus

Short	Generated Object (*Bus or NetGroup*)	Winning Bus	Generated Flat Nets	Defintion
EXAMPLE				
NetGroup S[0..5] - Members: S.JTAG0, S.JTAG1, S.JTAG2, S.JTAG3, S.JTAG4, S.JTAG5				
Bus OPC B[0:2] - Members: B.B0, B.B1, B.B2				
	S[0..2]	S[0..2]	S.JTAG0, S.JTAG1, S.JTAG2, B3,B4,B5	S[0..2]
NetGroup wire and Bus OPC/GLOBAL/PORT (NetGroup width higher)	Bus	Bus OPC/GLOBAL /PORT	Winning Bus defines flat nets	associated NetGroup definition should match winning bus
EXAMPLE				
NetGroup S[0..2] - Members: S.JTAG0, S.JTAG1, S.JTAG2				
Bus OPC B[0:5] - Members: B.B0, B.B1, B.B2, B.B3, B.B4, B.B5				
	S[0..2]	S[0..2]	B0,B1, B2, S.JTAG3, S.JTAG4, S.JTAG5	S[0..5]
NetGroup wire and Bus OPC/GLOBAL/PORT (bus width higher)	Bus	Bus OPC/GLOBAL /PORT	Winning Bus defines flat nets	associated NetGroup definition should match winning bus
EXAMPLE				
NetGroup S[0..2] - Members: S.JTAG0, S.JTAG1, S.JTAG2				
Bus OPC B[0:5] - Members: B.B0, B.B1, B.B2, B.B3, B.B4, B.B5				
	B[0..5]	B[0..5]	B0,B1, B2, B3,B4,B5	S[0..2]
NetGroup wire and NetGroup connector	NetGroup	NetGroup connector	Winning Bus defines flat nets	associated NetGroup definition should match winning bus

Short	**Generated Object (***Bus or NetGroup***)**	**Winning Bus**	**Generated Flat Nets**	**Defintion**
NetGroup connector and NetGroup connector	NetGroup	Lexicographically smaller NetGroup connector	Winning Bus defines flat nets	associated NetGroup definition should match winning bus

Color Reference

Introduction

The following list contains a mapping of the Capture Color IDs to their corresponding RGB values.

Color ID	RGB Value / Color Sample
1	255, 255, 128
2	128, 255, 128
3	0, 255, 128
4	128, 255, 255
5	0, 128, 255
6	255, 128, 192
7	255, 128, 255
8	255, 0, 0
9	255,255, 0
10	128,255,0
11	0, 255, 64
12	0, 255, 255
13	0, 128, 192

Color ID	RGB Value / Color Sample
14	128, 128, 192
15	255, 0, 255
16	128, 64, 64
17	255, 128, 64
18	0, 255, 0
19	0, 128, 128
20	0, 64, 128
21	128, 128, 255
22	128, 0, 64
23	255, 0, 128
24	128, 0, 0
25	255, 128, 0
26	0, 128, 0
27	0, 128, 64
28	0, 0, 255
29	0, 0, 160
30	128, 0, 128
31	128, 0, 255
32	64, 0, 0
33	128, 64, 0
34	0, 64, 0
35	0, 64, 64
36	0, 0, 128
37	0, 0, 64
38	64, 0, 64
39	64, 0, 128
40	0, 0, 0

Color ID	RGB Value / Color Sample
41	128, 128, 0
42	128, 128, 64
43	128, 128, 128
44	64, 128, 128
45	192, 192, 192
46	64, 0, 64
47	255, 255, 255
48	Windows Default Color

How to use this guide

This guide is designed to make the most of the advantages of onscreen books. The table of contents, index, and cross references provide instant links to the information you need. Just click on the text and jump.

If you find printed paper helpful, print only the section you need at the time. When you want an in-depth tutorial, print the example. When you want a quick reminder of a procedure, print the procedure.

Symbols and conventions

Our documentation uses a few special symbols and conventions.

Notation	Examples	Description
Bold text	**Import Measurements**, **Modified LSQ,** **PDF Graph**	Indicates that text is a menu or button command, dialog box option, column or graph label, or drop-down list option
Icon graphic		Shows the toolbar icon that should be clicked with your mouse button to accomplish a task
Lowercase file extensions	.aap, .sim, .drt	Indicates a file name extension

Using Capture

OrCAD Capture can be used by designers to create schematics and produce connectivity and simulation information for printed circuit boards and programmable logic designs. You can use OrCAD Capture to create designs for other EDA applications by choosing to set up a PSpice project, PCB project, or programmable logic project when you start a new project. You can set your user preferences for the appearance of all designs on your system, and set up design options for each particular project or design you create.

Capture provides standard libraries that can be used to design schematics. You can also create your own library.

In Capture, you can drag and drop schematic folders and pages in the project manager in the session window. You can place parts and pins in Capture's schematic editor, then connect the parts with buses, wires, off-page connectors, and more. Use a multitude of Capture tools to edit the design, including the part editor, the Edit menu and the pop-up menu. Create your own parts and part packages, or use the standard libraries provided with Capture.

The property editor of Capture shows you properties of all or selected parts in your schematic design one page at a time. You can use the property editor to add, change, or delete user properties and property values in your own custom filter for any design.

Capture also includes verification and reporting, printing, and netlisting features for your schematic page, folder, or entire design.

For more information about	See
OrCAD Capture	Capture User's Guide
OrCAD Capture messages	Capture Messages Reference Guide
Libraries	OrCAD Supplied Libraries Reference Guide
Toolbar commands and shortcut keys	OrCAD Capture Quick Reference
PSpice simulations	PSpice User's Guide
PCB design	Allegro PCB Editor User Guide
PCB design cycle	OrCAD Flow Tutorial

Related documentation

In addition to this guide, you can find technical product information on the Cadence website www.cadence.com/orcad. The table below

describes the types of technical documentation provided with Capture.

This documentation component . . .	Provides this . . .
This guide— OrCAD Capture User Guide	A comprehensive guide for understanding and using the features available in OrCAD Capture.
Help system (automatic and manual)	Provides comprehensive information for understanding the features in Capture and using them to perform schematic capture. Capture provides help in two ways: context-sensitive help and manual help. Context-sensitive help displays help topics that are associated with your current activity when you press the F1 key or click the Help button on the active dialog box or window within the Capture workspace and interface. It provides immediate access to information that is relative to your current task. The manual method gives you full navigational access to all topics and resources outside of the help system. Using either method, help topics include: ■ Explanations and instructions for common tasks ■ Descriptions of menu commands, dialog boxes, tools on the toolbar and tool palettes, and the status bar ■ Glossary terms ■ Reference information
Online interactive tutorial	A series of self-paced interactive lessons. You can practice what you've learned by going through the tutorial's specially designed exercises that interact directly with Capture. You can start the tutorial by choosing Learning Capture from the Help menu.

This documentation component . . .	Provides this . . .
OrCAD Capture Quick Reference Card	Concise descriptions of the commands, shortcuts, and tools available in Capture

Glossary

A|B|C|D|E|F|G|H|I|J|L|M|N|O|P|R|S|T|U|V|W|X|Y|Z

A

absolute simulation time

A time measured from the beginning of the simulation.

absolute stimulus

See force.

actual

The value of a parameter passed to a VHDL subprogram.

alias

See net alias, part alias.

ANSI

The acronym for *American National Standards Institute*.

ARCHITECTURE

A VHDL construct that describes the behavior of a design unit (ENTITY/ARCHITECTURE pair). The ARCHITECTURE can also serve to connect other VHDL design units.

arrow keys

On your computer keyboard, the keys you use to navigate around your screen. Each key is marked with an arrow and is named for the direction in which the arrow points. There is an up arrow, down arrow, left arrow, and right arrow key. Also known as *direction keys*.

ascend

In a hierarchical design, to move from a child schematic folder to its parent schematic folder. This is done in the schematic page editor using the Ascend Hierarchy command on the View menu. *See also* descend.

ASCII

The acronym for *American Standard Code for Information Interchange*. The ASCII character-coding set enables different applications to exchange information.

ASSERT

A VHDL keyword typically used in conjunction with the REPORT and SEVERITY keywords to detect a particular circuit state and announce the condition with an associated severity level.

AutoECO

The acronym for *automatic engineering change order*. Layout's AutoECO command translates schematic netlist information from Capture to Layout. *See also* forward annotate.

B

back annotate

To apply modifications to part properties in a schematic folder, such as updating part references and pin numbers, swapping gates, or swapping pins. Properties are back annotated in the project manager, using the Back Annotate command or the Update Properties command on the Tools menu.

bitmap

Bitmaps are graphic images that are made up of pixels, which are the tiny dots on your computer screen. Each pixel in a bitmap is represented by a number between 0 and 255, inclusive, with 0 being the darkest (no luminance) and 255 being the lightest (full luminance). Bitmaps have a .BMP extension, and can be placed on a schematic page using the Picture command from the schematic page editor's Place menu.

BLIF

Berkeley Logic Interchange Format. This format, developed at the University of California, Berkeley, is used to convey Boolean logic between programs. BLIF files are termed PLAs.

bookmark

Just as you can place bookmarks in a book to mark a specific place, you can place bookmarks on a schematic page to indicate a location you would like to return to frequently. To place a

bookmark, use the Bookmark command on the Place menu in the schematic page editor. To go to a bookmark when in the schematic page editor, use the Go To command on the View menu. To go to a bookmark when in the project manager, use the Browse command on the Edit menu to display bookmarks in the browse window, and then choose the bookmark.

BRD

An PCB Editor board file. The .BRD contains information about the board, component symbols, pins, nets, keep-ins and keep-outs, plus how the parts are placed and routed. The .BRD file also includes the properties and constraints that apply to parts and areas of the board.

breakpoint

A pause in the simulation triggered by a particular condition. You can set a breakpoint to occur when a certain state exists on a signal, or just before a particular line in a VHDL model is executed during a simulation.

browse window

This window displays the results of queries done using the Browse command from the Edit menu. You can double-click on an object in the browse window to go to that item on its schematic page.

bus

A group of scalar signals (wires) that are never connected to a net. A bus name defines the signals carried by the bus and connects those signals to the corresponding nets. For example, the bus name A[0:3] defines a four-signal bus and connects the four signals A[0], A[1], A[2], and A[3] with nets A0, A1, A2, and A3. *See also* bus pin, bus entry.

bus entry

A bus entry is used to tie a signal to a bus. The advantage of using bus entries instead of wires is that two bus entries can be connected at the same point on a bus without connecting the signals. If two wires are run directly to a bus at the same location, the signals are connected. *See also* bus, bus pin.

bus pin

A pin width that can carry multiple signals, as opposed to a scalar that carries only one signal. A bus pin represents all the pins for a bus, and it uses the same naming convention as buses. *See also* bus, bus entry.

C

CAGE code

Abbreviation for *Commercial and Government Entity Code*. A number—provided by the federal government to its suppliers—that can be present in the title block of a schematic page.

CELL

An EDIF keyword that defines the interface to a hierarchical block or part. An OrCAD Capture hierarchical block or part will generate a cell in the EDIF netlist. Simulate displays EDIF cells as contexts within the Simulate netlist.

child

In a hierarchical design, a schematic folder whose circuitry is represented by a hierarchical block in the parent schematic folder. To move from parent to child is to descend the hierarchy. This is done in the schematic page editor by selecting the hierarchical block representing the child, and then choosing the Descend Hierarchy command on the View menu. A child schematic folder contains circuitry referenced by its parent schematic folder. The child schematic folder may contain hierarchical ports that connect its signals to signals in the parent schematic folder or to signals on other pages of the child schematic folder. *See also* ascend.

Clipboard

A temporary storage location used to transfer data between files and between applications. You transfer data to the Clipboard by using the Copy or Cut command on the Edit menu, and you insert data from the Clipboard by using the commands on the Edit menu.

clock

A signal that has a simple repeating waveform pattern. Typically, clocks drive the synchronous devices in your design. Clock stimuli in Simulate can be overwritten by forces.

clock to output delay

The propagation time for a clocked device. That is, this delay is the length of time required for a data signal to propagate to the device output after being clocked.

command line window

Use the command line window to execute a subset of frequently-used Simulate commands.

complex hierarchy

A design in which two or more hierarchical blocks (or parts with attached schematic folders) reference the same schematic folder. *See also* hierarchical design, simple hierarchy.

context

The level of hierarchy at which logic macros, pins, and signals are found. A context in Simulate corresponds to an EDIF cell or a VHDL ENTITY/ARCHITECTURE pair. A hierarchical block on an OrCAD Capture schematic page appears as a context in Simulate.

convert

An alternate form—such as a DeMorgan equivalent—that can be stored with each part.

cross probing

When intertool communication is enabled in Capture, selecting objects in Capture causes the corresponding objects to be highlighted in PCB Editor. Also, selecting objects in PCB E ditor causes the corresponding objects to be highlighted in Capture. Both applications must be open. *See also* intertool Communication.

CurrentLocation

A value stored by Capture that determines the starting point for the next macro command. This value is set by the previous macro. You can also set this value by moving the pointer to the desired location, and clicking the left mouse button.

D

DeMorgan equivalent

An electrically-equivalent part based on the DeMorgan rules of equivalence. These rules represent the duality of AND and OR in Boolean expressions: if all AND operations are changed to OR operations, all OR operations are changed to AND operations, and all variables and constants are negated, then the value of the expression remains unchanged. A DeMorgan equivalent can be stored in the convert of a part.

descend

In a hierarchical design, to open and view the child schematic folder represented by a hierarchical block in the parent schematic folder. To descend a hierarchical design, you select a hierarchical block in the schematic page editor, then choose the Descend Hierarchy command from the View menu. *See also* ascend.

design

The set of schematics and models that collectively define the behavior of your project.

design cache

A local library contained in each project that contains all the parts and symbols used in the design.

design entry

The process of expressing an electronic design. Typically, design entry involves describing a structure using schematic logic macros, behavioral description with a hardware description language (HDL), or some combination of both methods. The design expression is processed to produce a gate-level netlist that can be used for simulation or design implementation.

design implementation

The process of mapping, fitting, or routing your design to or within a specific device. Design implementation can yield timing values that allow you to perform timing analysis and ensure that your design meets your performance requirements.

device-fitter

A software tool to implement a logic design (usually recorded as an Open-PLA or gate-level netlist) into the physical resources of a CPLD.

DIFFERENTIAL_PAIR

Represents a pair of flat nets that will be routed in a way that the signals passing through them are opposite in sign with respect to the same reference. This ensures that any electromagnetic noise in the circuit is cancelled out.

document

A project, schematic page, library, part, or symbol. Each of these is part of a project or a library file. In addition, stimulus files, simulation result files, and simulation models are documents.

DRC

The abbreviation for *Design Rules Check*, a tool found on the Tools menu in the project manager. This tool checks a project (or a subset of the design) for conformance to a set of configurable design criteria, electrical rules and physical rules for creating netlists.

E

EDA

The acronym for *Electronic Design Automation*. Software and hardware tools used to ascertain the viability of an electronic design. These tools perform simulation, synthesis, verification, analysis, and testing of a design.

EDIF

The acronym for *Electronic Design Interchange Format*. A standard published by the EIA (Electronic Industries Association) that defines the semantics and syntax for an interchange format that communicates electronic designs. Simulate uses EDIF 2 0 0 standard netlists as a simulation resource.

ENTITY

A VHDL construct that defines the interface to a VHDL design unit (an ENTITY/ARCHITECTURE pair).

equivalent

See convert, DeMorgan equivalent.

ERC

The abbreviation for *Electrical Rules Check*, a subset of the Design Rules Check tool found on the Tools menu in the project manager. The ERC matrix is the decision matrix that tells the Design Rules Check tool the conditions to check for when evaluating connections between pins, hierarchical ports, and off-page connectors.

event

Any signal transition that occurs during simulation. An event appears as a transition in the wave window, and generates a new row in the list window. Simulate records the history of all events for any signal that are traced in either window.

external design

Any referenced design that is not included as part of the main design's schematic pages. An external design may be a library (.OLB) part which you can place with the Part command from the Place menu. Alternately, an external design may be a complete schematic (.DSN) design which you can include by using the Hierarchical Block command from the Place menu. Whenever you use external designs you set up a hierarchical structure. If you copy an external designs without taking into consideration the occurrence properties inherent in a hierarchical structure, you might get instance property but not occurrence values.

Note: Except for occurrence properties, the schematics of externally-referenced libraries and designs should not be edited. You should view them as read-only designs. Trying to edit, then save, these designs from within your schematic can introduce errors such as duplicate reference designators and other problems.

When saving schematics with externally-referenced libraries or designs, occurrence properties are saved but altered instance values are not. If you want to change externally-referenced libraries or designs you should first close the referencing design. Then, open the referenced library or design, make the necessary changes, and save and close the referenced library or design. At this point, you can reopen the original design and reference the modified design.

F

flat design

A schematic folder structure without hierarchy (no hierarchical blocks or ports; no parts with attached schematic folders). A flat design can include schematic pages in which output lines of one schematic page connect laterally to input lines of another schematic page through objects called off-page connectors. You place off-page connectors using the Off-Page Connector command on the Place menu in the schematic page editor. Flat designs are practical for small designs with few schematic pages. *See also* hierarchical design, complex hierarchy, simple hierarchy.

flat net

A type of net represented by a flattened (non hierarchical) netlist for a PCB, such as a layout netlist.

force

A scheduled state change that occurs at a *specific* simulation time. A force will override any other signals driving the node. That is, a force is equivalent to placing a probe on the node. When you place a force, it remains in effect until you replace it with another force, or until you remove the force from the stimulus file.

forward annotate

The process of sending netlist data in the form of a .BRD file from Capture to PCB Editor.

functional simulation

Simulation that verifies design logic and functionality without regard to timing (for example propagation or critical path).

fuse plot

An ASCII representation of a fuse map. You can use this file to visually review the fuse map that Express creates for your simple PLD. Fuse plots appear as shown in the following example:

FUSE MAP FOR P12H6

	0	2	4	6	8	10	12	14	16	18	20	22
0	--	x-	--	--	--	--	x-	--	--	--	--	--
24	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx
48	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx
72	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx
96	x-	--	--	--	--	--	--	--	--	--	--	--
120	--	--	--	--	--	--	--	x-	--	--	--	--
144	--	--	--	-x	--	--	--	--	x-	--	--	--
168	--	--	--	x-	--	--	--	--	-x	--	--	--
192	--	--	-x	--	--	--	--	--	--	--	--	--
216	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx
240	--	--	--	--	-x	--	--	--	--	--	--	--
264	--	--	--	--	--	--	--	--	--	--	-x	--
288	--	--	--	--	--	-x	--	--	--	-x	--	--
312	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx
336	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx
360	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx

Legend: x fuse intact

- fuse open

203 fuses open of 384 total.

G

globals

Power symbols and ground symbols. Could also be other objects that function the same as power or ground.

graphic object

An object drawn or placed on a schematic page or part -- such as an arc, line, rectangle, ellipse, polygon, image, or text -- that has no electrical connectivity.

grid references

The border around a schematic page that provides a visual reference to the grid. Grid references can be used as a destination for the Go To command on the View menu. Grid references can be set to visible or hidden in both the Design Template and Schematic Page Properties commands on the Options menu.

H

heterogeneneous part

A package with multiple parts that are graphically different or contain different numbers of pins (for example, a relay). See also homogeneous part.

hierarchical block

A symbol that refers to a child schematic folder in a project. The connection points on a hierarchical block are called hierarchical pins and hierarchical ports. You place a hierarchical block using the Hierarchical Block command on the Place menu.

hierarchical design

A project structure in which schematic folders are interconnected vertically with hierarchical blocks. At least one schematic folder, the root schematic folder, contains symbols representing other schematic folders. See also complex hierarchy, simple hierarchy, flat design.

hierarchical pin

A symbol, placed within a hierarchical blocks, that represents a signal connected to a like-named hierarchical port on another

schematic page. You place a hierarchical pin using the Hierarchical Pin command on the Place menu.

hierarchical port

A symbol that specifies that a signal on one schematic page connects to a hierarchical pin on another schematic page. A hierarchical port includes a name and a type (either scalar or bus). You place a hierarchical port using the Hierarchical Port command on the Place menu. See also hierarchical block.

homogeneous part

A package with multiple parts that are graphically identical. See also heterogeneneous part.

HPGL

Acronym for *Hewlett-Packard Graphics Language*, which is a plotter protocol.

I

IEEE

Acronym for *Institute of Electrical and Electronics Engineers*.

IEEE Std VDHL 1076

VHDL standard determined by the *Institute of Electrical and Electronics Engineers*.

implementation path

The path for an attached object, such as a referenced design folder or a library part.

inherent property

One of the set of properties required for a given object. Unlike user defined property, inherent properties cannot be removed.

instance

A part or a symbol that you have placed on a schematic page.

instance property

A user property applied to the placed instance of a part or symbol in the design. This includes PCB Footprint, Value, and Name properties of each placed part or symbol in a design. This

is the same as the user properties displayed and editable from the Capture v7.2 Physical view.

An instance property will "shine through" to all occurrences of that instance unless it is overridden by occurrence properties that you have edited. A change using any of the tools, like Annotate, also may update the instance property.

intertool Communication

Abbreviated ITC. A capability that allows OrCAD EDA tools to share information for display and transfer.

ITC

Intertool Communication. A capability available with OrCAD for Windows tools that allows these tools to share information for display and transfer.

J

Junction

A junction, shown as a small dot, is placed at the connection point where two perpendicular wires or buses cross, to give visual confirmation that the items are electrically connected. If you draw a wire across another at a 90-degree angle, the wires are not electrically connected unless you create a junction by clicking the left mouse button on the existing wire as you draw the new wire across it.

L

library

A collection of often-used parts, graphics, schematic pages, and symbols.

library definition

A package property or user property associated with the part in the library.

A library definition will "shine through" to the instance and occurrences of that part property. Shine through is indicated by hash marks in the cell. You can assign a value to it creating an instance property. The instance property then will override the shine-through definition.

location

An X, Y coordinate on the schematic page or part. You can move to a location using the Go To command on the View menu.

M

macrofunction

A high-level building block made of two or more primitives. Muxes, counters, and adders are examples of macrofunctions.

MDD

PCB Editor Module Definition File (.MDD). This is the file type created in PCB Editor once you've designated the extents of a reuse module and specified a module origin. Each physical module is assigned a REUSE_MODULE property and contains placed and routed components.

mirror

To flip along the X (horizontal) or Y (vertical) axis, or both.

N

net

1. All of the wires, buses, parts, and symbols that are logically connected via net names, net aliases, off-page connectors, and hierarchical ports.
2. A general electronic term for a circuit node that ties a collection of component pins together. The EDIF 2 0 0 netlist format contains a netlist region that declares the net name and all component instances that are tied to it. You can trace EDIF nets in Simulate.

net alias

A name used to specify signal connections between unconnected wires or buses. For example, if you have wires in two remote locations in a schematic page, you can assign each wire an alias such as "ABC" to connect the signals without physically drawing a wire between them.

netlist

A file, usually ASCII, that lists the interconnections of a schematic folder by the names of the connected signals, parts, and pins.

nonprimitive

A part with an underlying hierarchy, such as an attached schematic folder.

O

occurrence

A user property applied to multiple occurrences of placed instances of parts or symbols in a design. This is the same as the user properties displayed and editable from the Capture v7.2 Physical view.

The spreadsheet will expand to display occurrence properties if values are different from the instance shine through value; otherwise, the rows are hidden from view. To quickly hide or display all the occurrence properties, press and hold the CTRL key while clicking on one of the plus (+) symbols in the property editor.

A change using any of the tools, like Annotate, also may update the instance property.

off-page connector

An object that conducts signals between schematic pages within a schematic folder. See also flat design, hierarchical port.

P

package

A physical part that contains more than one logical part. For example, a 2N3905 transistor, a fuse, and a 74LS00 are packages. Each part in a package has a unique part reference comprised of a prefix common to all the parts in the package, and a letter unique to each part. For example, a 74LS00 whose part reference prefix is U15 would have four parts whose part references are U15A, U15B, U15C, and U15D. See also homogeneous part, heterogeneneous part.

pan

To change the portion of the schematic page or part being viewed by dragging objects from one location to another. As you drag the object, the schematic page or part *pans* across the active window.

parent

A schematic folder that contains a hierarchical block that refers to another schematic folder (called a child schematic folder).

part

A part is a basic building block of a design. A part may represent one or more physical components, or it may represent a function, a simulation model, or a text description for use by an external application. A part's behavior is described by a SPICE model, an attached schematic folder, HDL statements, or other means. Parts usually correspond to physical objects—gates, connectors, and so on—that come in packages of one or more parts. Packages with more than one part are sometimes referred to as "multiple-part packages". See also package.

part alias

A duplicate copy of a part using a different name in a library. A part alias uses the same graphics, attached schematic folders, and properties as the original, with the exception of the part value.

part editor

The editor used to create and edit parts and symbols.

part instance

An instance property of a part.

part primitive

See primitive.

part property

A part property is a characteristic of a part that can be edited. A property consists

of a name and a value. Examples of property names are part value and color. Their

respective property values can be something such as capacitor and red.

part reference

When you place parts on a schematic page, all parts of the same type are assigned the same part reference. For example, C? is assigned to all capacitors. Regardless of the ultimate purpose of your design, each part needs a unique part reference. You can assign part references by editing individual parts in the part editor, or, for PCB designs, by creating a swap file to use with the Back Annotate tool.

If you want to incrementally update a design in which some of the schematic pages have already been updated, you can use the Annotate command to remove part references from those schematic pages.

pattern

A set of events that occur on a signal, *relative* to a specific simulation time. This pattern may or may not be repeating. Patterns may be overwritten by forces. Conflicts between patterns, or between a pattern and signal propagation are resolved using signal contention resolution.

PCB

Abbreviation for printed circuit board.

pending event

A simulation event that will occur in the future. As signals change state during simulation, a VHDL simulator must evaluate the input stimuli and all design units of the circuit, then anticipate or schedule all events that must be reported before the simulation time can advance. Simulate allows you to view pending events with the Pending Events command.

pin

A pin acts as a point of connectivity for the part it is attached to. In addition to input and output pins, there are also 3-state, bidirectional, open collector, open emitter, passive, and power pins. If a pin connects to a wire, it is a scalar pin; if it connects to a bus, it is a bus pin. See also hierarchical pin.

pin delay

The propagation delay for a pin to pin transition. That is, pin delay is the length of time required for the effects of a signal at an input pin to be reflected at the corresponding output pin(s).

pin swap

The exchange of identical pins in order to decrease route lengths.

pin to pin spacing

The physical spacing between pins on a device.

PLA

A file that uses the BLIF to express Boolean logic. Typically, PLA files are used as entry mechanisms for simulation models into Simulate.

place and route

1. A software tool to implement a logic design (usually recorded as a gate-level netlist) into the physical resources of an FPGA.
2. The process of determining a design layout in order to estimate routing delays and predict design performance.

PLD

Abbreviation for programmable logic device.

Preferred mode warning

Capture automatically sets the preferred mode based on the project type. FPGA and PSpice projects default to use instances, while PCB and Schematic projects default

to occurrences.

polygon

A graphic object made up of polylines (multiple contiguous segments) whose beginning and end are attached to form a closed shape that can be filled.

polyline

A line with multiple contiguous segments. You place a polyline using the Polyline command on the Place menu.

port

A VHDL term for an interface element of an ENTITY. A port serves as a communication channel between VHDL design units. A part pin on an OrCAD Capture schematic page generates a VHDL port. See hierarchical port.

primitive

A part or hierarchical block with no underlying hierarchy.

programmable logic device

A type of integrated circuit whose behavior can be determined by programming it. Abbreviated *PLD*.

project

An OrCAD project file (.OPJ) includes references to all of the resources you use throughout the design process. These resources including elements that define design structure (VHDL source files, schematic folders, etc.), as well as part libraries, test benches, stimulus files, simulation models, vendor files, and standard delay files. You can view these resources in the project manager.

project manager

The project manager is a tool that allows you to collect and organize all the resources you need for your project throughout the design flow. These resources include schematic pages, part libraries, and netlists, and may also include VHDL models, simulation models, timing files, stimulus files, and other related information.

PROPAGATION_DELAY

Defines the minimum and maximum propagation delay constraint between any pair of pins in a net. By assigning this property to nets, you can make the router restrict the length of interconnect to meet timing margin. This property often is best applied to a common clock sourced designed bus.

property

A characteristic of an object that can be edited. A property consists of a name and a value. Examples of property names are part value and color. Their respective property values can be something such as capacitor and red.

R

radix

The number base in which a signal value is displayed: binary, octal, signed or unsigned decimal, or hexadecimal.

RAM

Abbreviation for Random Access Memory. This is the memory that can be used by applications to perform necessary tasks while the computer is on. When you turn the computer off, all information in RAM is lost.

random access memory

The memory that can be used by applications to perform necessary tasks while the computer is on. When you turn the computer off, all information in random access memory is lost. Abbreviated *RAM*.

RATSNEST_SCHEDULE

Specifies the type of ratsnest calculation that Constraint Manager performs on the net. By using the `RATSNEST_SCHEDULE` property, you can meet a balance between time margin and noise margin. This property is useful for defining the placement of receiver or driver in multi-drop buses and asynchronous signals.

recursive design

A hierarchical design in which a schematic folder in the hierarchy is attached to a part instance or hierarchical block placed "higher" in the hierarchy. The simplest case of recursion is some schematic folder X containing a part instance or hierarchical block to which schematic folder X is attached.

reference designator

The designator, or identification code, for a component. A reference designator uniquely identifies a part in a design. For uniquely identifying parts, you can use the Annotate command on the Tools menu. For PCB designs, the Annotate tool assigns individual parts to a package and assigns unique pin numbers to each part in a multiple-part package. References are assigned in order from top to bottom and left to right; parts located at the top of the page have the lowest numerical designation. If two

parts share a vertical coordinate, the part further to the left has the lower numerical designation.

The format for reference designators should never be changed as <Alphabet(s)><Numeric><Alphabet(s)> or <Alphabet(s)>-<Alphabet(s).

RELATIVE_PROPAGATION_DELAY

An electrical constraint attached to pin-pairs on a net. It specifies a group of pin-pairs that are required to have interconnect propagation delays matching a specified delta (offset) and tolerance with respect to the target pin pair. You can apply the RELATIVE_PROPAGATION_DELAY property to a source synchronous bus design, such as DDR interfaces.

root schematic folder

The schematic folder at the top of a flat design or hierarchical design. The root schematic folder contains a backslash (\ ) in its icon in the project manager. A project has only one root schematic folder.

S

scalar

A pin width that carries only one signal, as opposed to a bus pin that can carry multiple signals.

schematic folder

A collection of the schematic pages at the same level of hierarchy in a design is contained within a schematic folder, which is shown in the project manager. *See also* flat design, hierarchical design, schematic page, root schematic folder.

schematic page

A page within a schematic folder on which a design is drawn. Schematic pages display in a window called the schematic page editor, in which you can place parts and draw wires.

schematic page editor

The editor used to create and edit schematic page.

SDF

Standard Delay File. This is a file containing delay values that relate design performance after place-and-route. You can add this file to your simulation project in order to perform timing analysis.

session frame

1. The Capture application window in which the various components of Capture—such as the session log, project manager, schematic page editor, and part editor—run.
2. The Simulate application window in which the various components of Simulate—such as the session log, wave windows, list windows, watch window, and project window—run.

session log

A window that displays text messages generated by Capture, such as errors and informational messages. The session log starts empty with each new Capture session, but you can save its contents to a text file.

setup time

The length of time for which data must be stable at a pin before being clocked into the device.

signal

1. An electrical impulse of a predetermined voltage, current, polarity, and pulse width.
2. The logical state that exists on a circuit node.
3. A VHDL term for a local circuit node that is not visible outside a VHDL design unit. A bus or wire on an OrCAD Capture schematic page that is not connected to a hierarchical port produces a signal.

signal contention

A condition that occurs when a circuit node is driven by multiple conflicting sources at the same time. In most circuit nodes, output-type ports fan out to drive multiple input-type ports. However, some networks are constructed such that it is possible for multiple drivers to drive a single node. Simulate uses MVL-9 signal contention resolution to resolve these conflicts.

signal context

The level of hierarchy at which a signal or port exists.

simple hierarchy

A project in which there is a one-to-one correspondence between hierarchical block (or parts with attached schematic folders) and the schematic pages they reference. Each hierarchical block (or part with attached schematic folder) represents a unique schematic page. See also hierarchical design, complex hierarchy.

simulation model

VHDL descriptions of the behavior of primitive components in your design. Typically, the simulation models for your design will exist in a single VHDL file, but they may also exist within the netlist file or in several different model files. Simulation models are necessary elements in an Simulate project.

simulation project

A simulation project is a collection of the resources you need to simulate your design. Generally, a simulation project requires the following elements: a netlist, a set of simulation models, and a set of stimuli. In addition, your simulation project may include timing annotation files after it has been through the design implementation process.

simulation resolution

The amount of time that represents one "step" in a simulation run. Simulate has two resolution settings: nanoseconds (the default) and picoseconds.

source library

The path and filename of the part definition. A filename with an .OLB extension means that the part was placed as is from a library. A filename with a .DSN extension means that the part no longer match the original library definition and its current definition only resides in the design file where it was edited.

spreadsheet editor

A window used to edit the properties of multiple objects at once.

split part

A part that consists of a package in which pins are split across multiple sections.

static timing analysis

A process that inspects the layout of a PLD or FPGA design to estimate the timing characteristics of the manufactured device. Typically, static timing analysis generates a delay annotation file for a digital simulator.

stimuli

Signal states that are applied to nodes in an electronic design in order to view the effects of those states on circuit behavior. There are three types of stimuli in Simulate: forces, patterns, and clocks.

subprogram

A term used to refer, collectively, to VHDL functions and procedures.

symbol

The graphical object that represents a part on a schematic page.

T

tabbed dialog box

A dialog box that has different views you can display by clicking on tabs at the top of the dialog box.

test bench

A VHDL module that defines the interface to one or more designs under test, applies input vectors, and (optionally) generates reports about the output behavior of the design(s) under test. A test bench ENTITY does not provide communication ports; therefore, test benches are usually used exclusively by VHDL simulators.

timing analysis

Simulation that identifies timing problems in the design. Timing analysis is performed after design implementation.

timing annotation file

A file containing delay values associated with the implementation of a design. In general, timing annotation files are produced from place and route tools.

timing violation

A simulation condition indicating that the timing constraints for a device have been violated. Simulate detects timing violations via the error trapping of VITAL VHDL models.

tri state enable delay

The length of time required for a tri-state device to transition from a Z state to a 0 or 1 once an enable has been received.

True Type

A font (typeface) that appears in a printout exactly the way it appears on the screen. TrueType fonts are scalable to any font size, and several of these type of fonts are installed automatically when you install Windows.

twos complement

An alternate method for representing a binary value. Two's complement allows positive and negative values to be represented in the same format and thus enhances arithmetic operations. The most significant bit of a two's complement value is the sign bit: a "0" indicates a positive value; a "1" indicates a negative value. The two's complement of a value is derived by inverting each bit in that value, then adding 1 to it. Thus, the binary value 0111 (representing +7) becomes 1000+1, or 1001 (representing -7).

U

user defined property

A property you add to an object. Unlike inherent properties, user-defined properties can be removed.

V

vertex

The point at which the sides of an angle meet. You create this by drawing a wire or line in one direction, then changing direction to create an L-shaped or V-shaped wire or line.

VITAL

VHDL Initiative Toward ASIC Libraries. An informal consortium formed to accelerate the development of ASIC macrocell simulation libraries modeled with VHDL.

W

waveform pattern

A set of events that occur on a signal, relative to a specific simulation time. A waveform pattern may or may not be repeating.

wildcard

A symbol, usually used in searches, that represents a missing or unknown character or sequence of characters. Valid wildcard characters are an asterisk (*) to match multiple characters and a question mark (?) to match individual characters.

X

X axis

The horizontal or left-to-right direction in a two-dimensional system of coordinates. The X axis is perpendicular to the Y axis.

XNF

Xilinx Netlist Format. This is a netlist format generated by Xilinx design implementation tools. You must convert XNF files to VHDL format before you can use them with Simulate.

Y

Y axis

The vertical or bottom-to-top direction in a two-dimensional system of coordinates. The Y axis is perpendicular to the X axis.

Z

zoom

To change the view of a window, making objects appear larger or smaller. When you zoom out, objects are smaller, and you see more of the schematic page, part, or waveform pattern. When you zoom in, objects are larger, but you only see a small portion of the schematic page, part, or waveform.

zoom factor

The amount by which the zoom scale is multiplied or divided when you choose Zoom In or Zoom Out on the View menu. The Zoom factor is normally 2, but you can change it using the Preferences command on the Options menu. For example, a zoom scale of two makes the image on the screen twice as large when you zoom in and half as large when you zoom out. You can also zoom in or out of a print preview.

zoom scale

The relative size of the image on the screen, as a percentage of the normal size. For example, a zoom scale of 250% means the image on the screen is two and one-half times as large as normal.

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