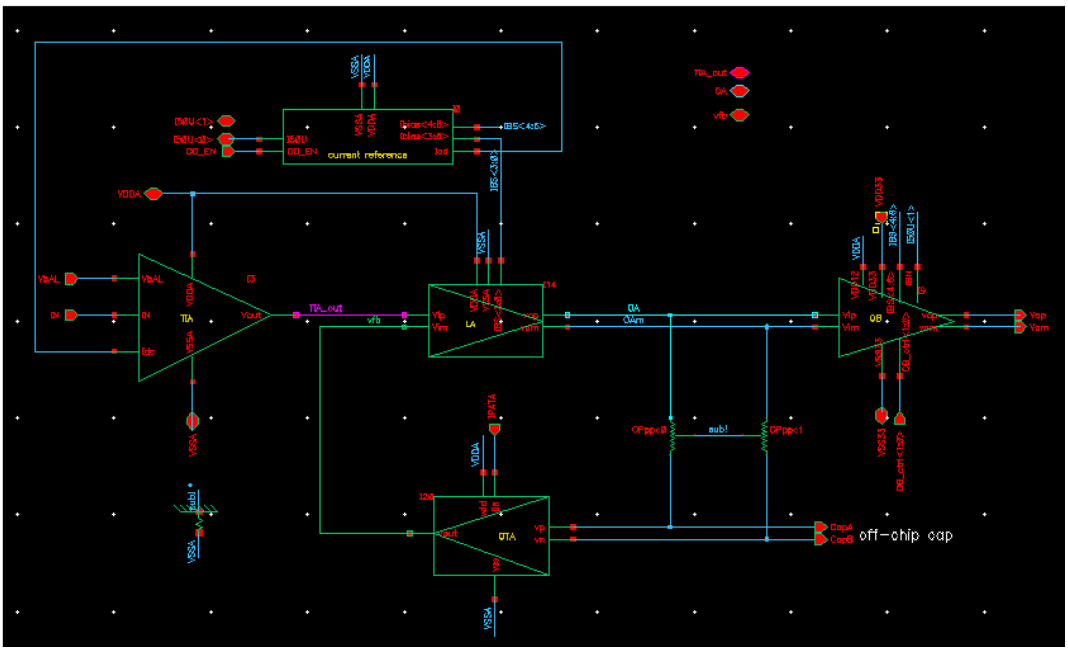

Figure 1 limiting-receiver top-level schematics.

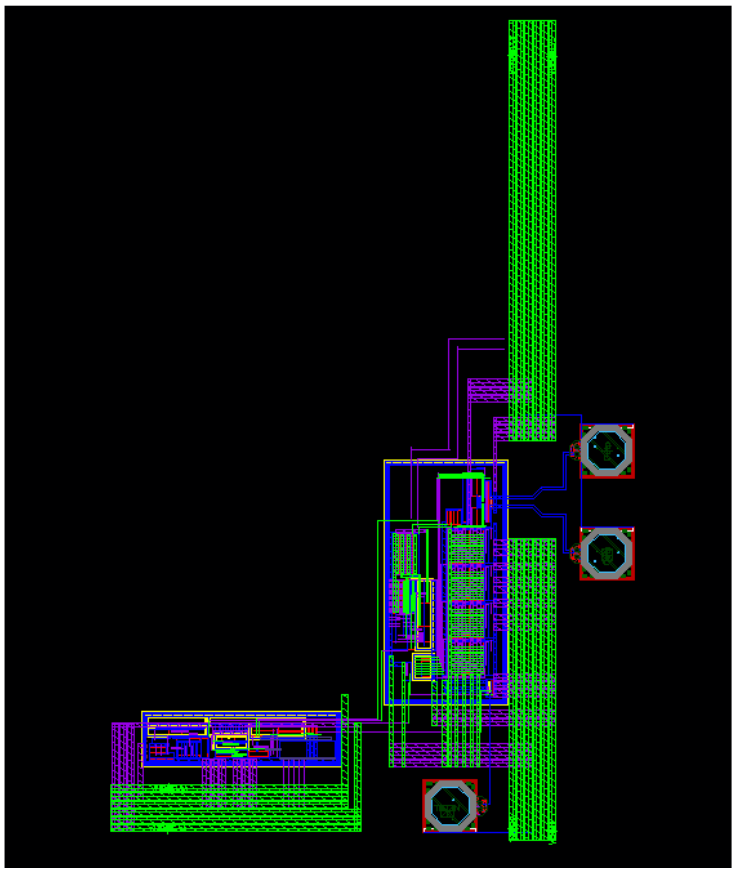

Figure 2 layout of limiting receiver (Figure 1) and bandgap references.

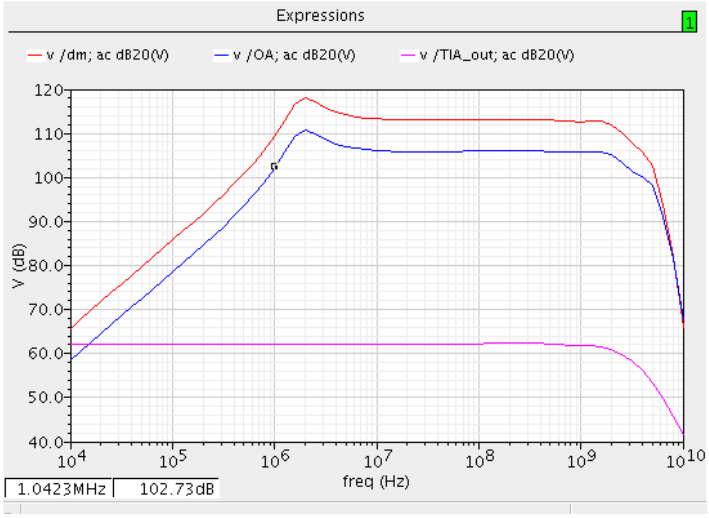

Figure 3 individually extracted sub-blocks simulation results.

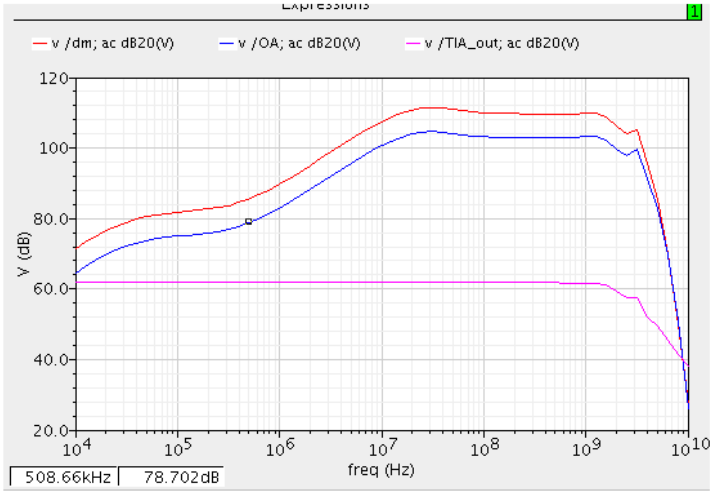

Figure 4 Overall extracted simulation.