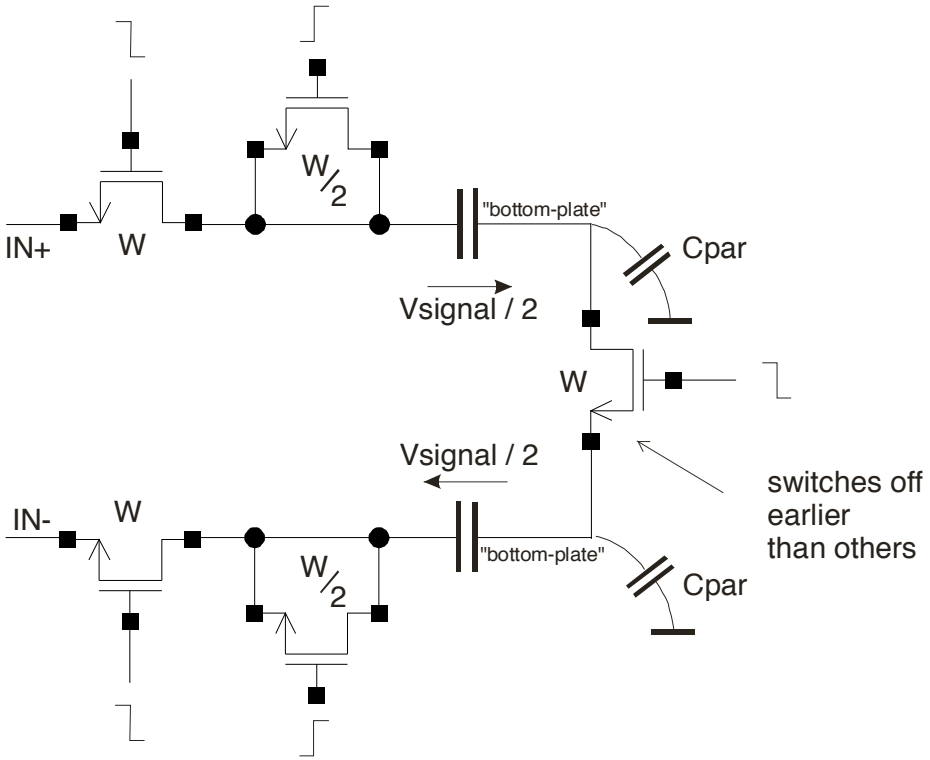
- Analog switches:

MOS-Transistors inject charge in drain and source nodes when turning off. Charge is split by the ratio of the admittance at D and S (approx.).
UMC-process offers 3,3V-Transistors, which are most suitable for the switches. 3,3V-power-supply is availlable on this chip, too. This allows to use NMOS-only switches for the 1,8V signal range.



„Bottom-Plate-Sampling": appropriate sequence of turning off the switches minimizes perturbations. Rightmost switch turns off first, injecting only common-mode-charge. Other switches turn off later, injecting differential charge, but influence on signal voltages on capacitors is small due to capacitive voltage division with C_{par}. Influence is minimized further by compensation switches switching in opposit direction.

The two "bottom-plate" marked nodes are the switches' "outputs".