Sonnet
Bond Wire Simulation

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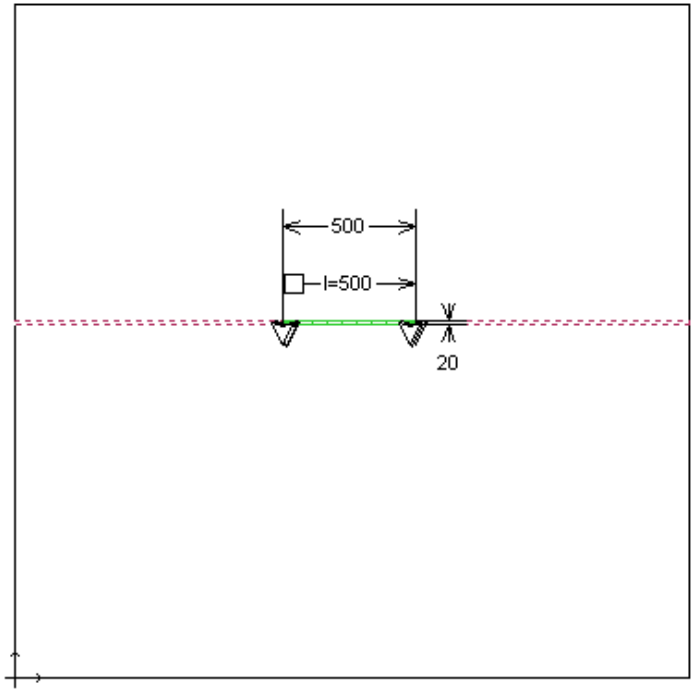
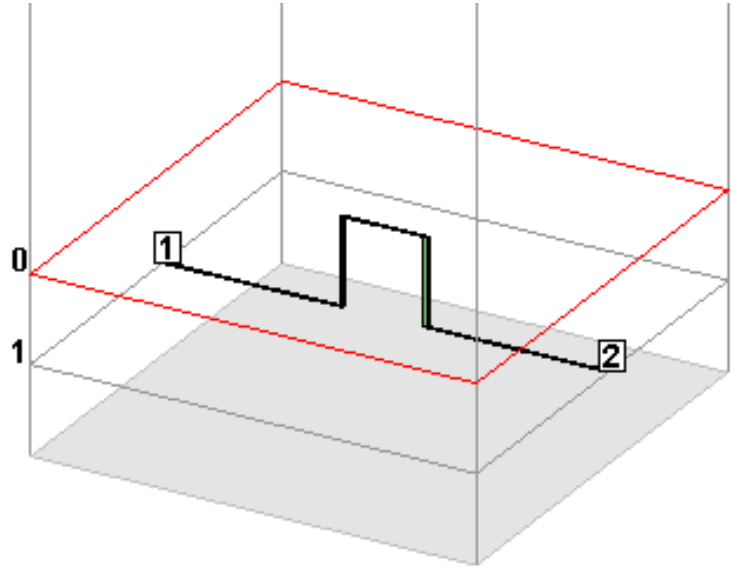
Single Bond Wire





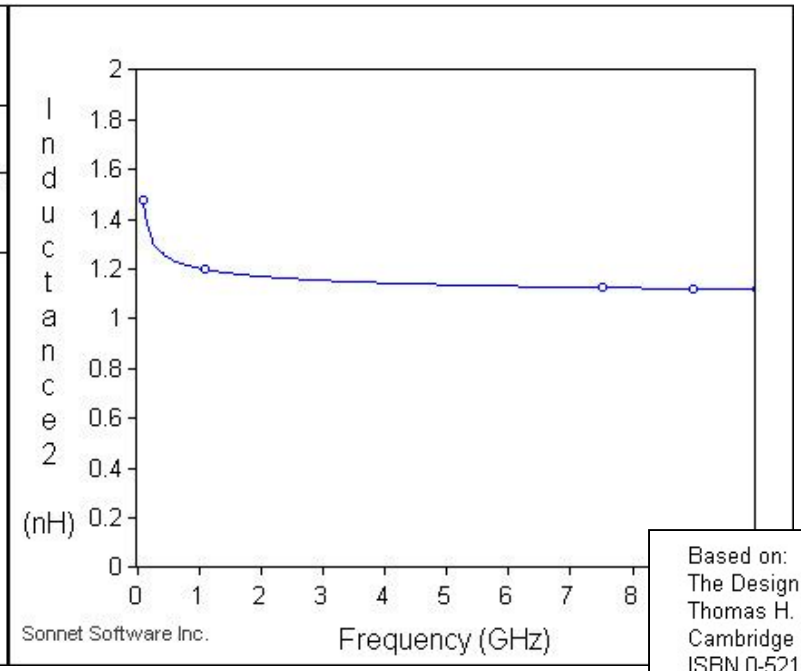
	Thickness (microns)	Mat. Name	Erel	Dielectric Loss Tan	Diel Cond (S/m)
0	5000.0	Air	1.0	0.0	0.0
1	500.0	Air	1.0	0.0	0.0
	510.0	Rogers RO4003C	3.55	0.0027	0.0

Compare Result

Cartesian Plot
Z0 = 50.0

Left Axis
RFIC_Series_Inductance (nH
bondwire_single_pcb

Right Axis
[empty]



Based on:
The Design of CMOS Radio-Frequency Integrated Circuits
Thomas H. Lee
Cambridge University Press 1998
ISBN 0-521-63922-0

Inductance

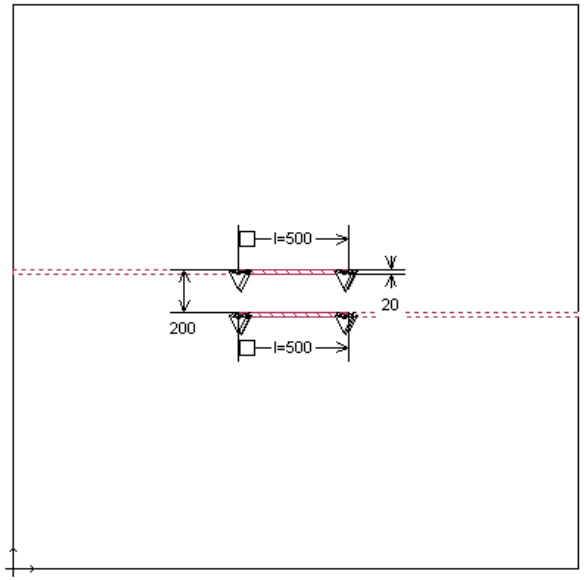
Length of bond wire [m] $length := 1.5 \times 10^{-3}$

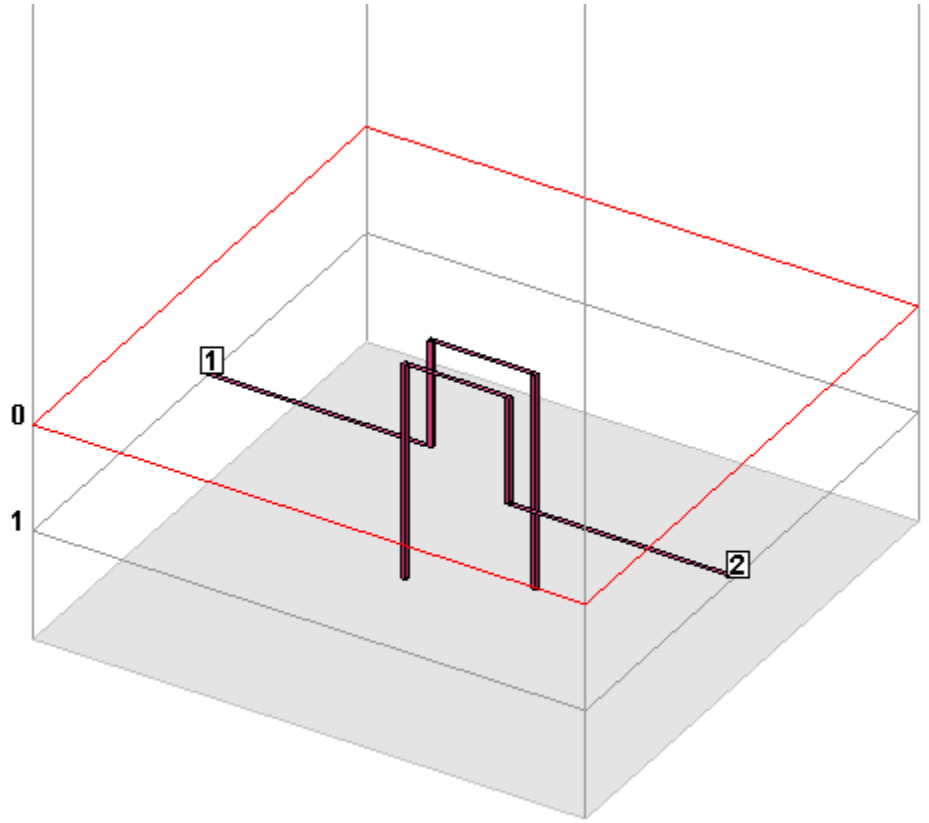
Wire diameter [m] $radius := 0.02 \times 10^{-3}$

$$L := 2 \cdot 10^{-7} \cdot length \cdot \left(\ln\left(2 \cdot \frac{length}{radius} \right) - 0.75 \right)$$

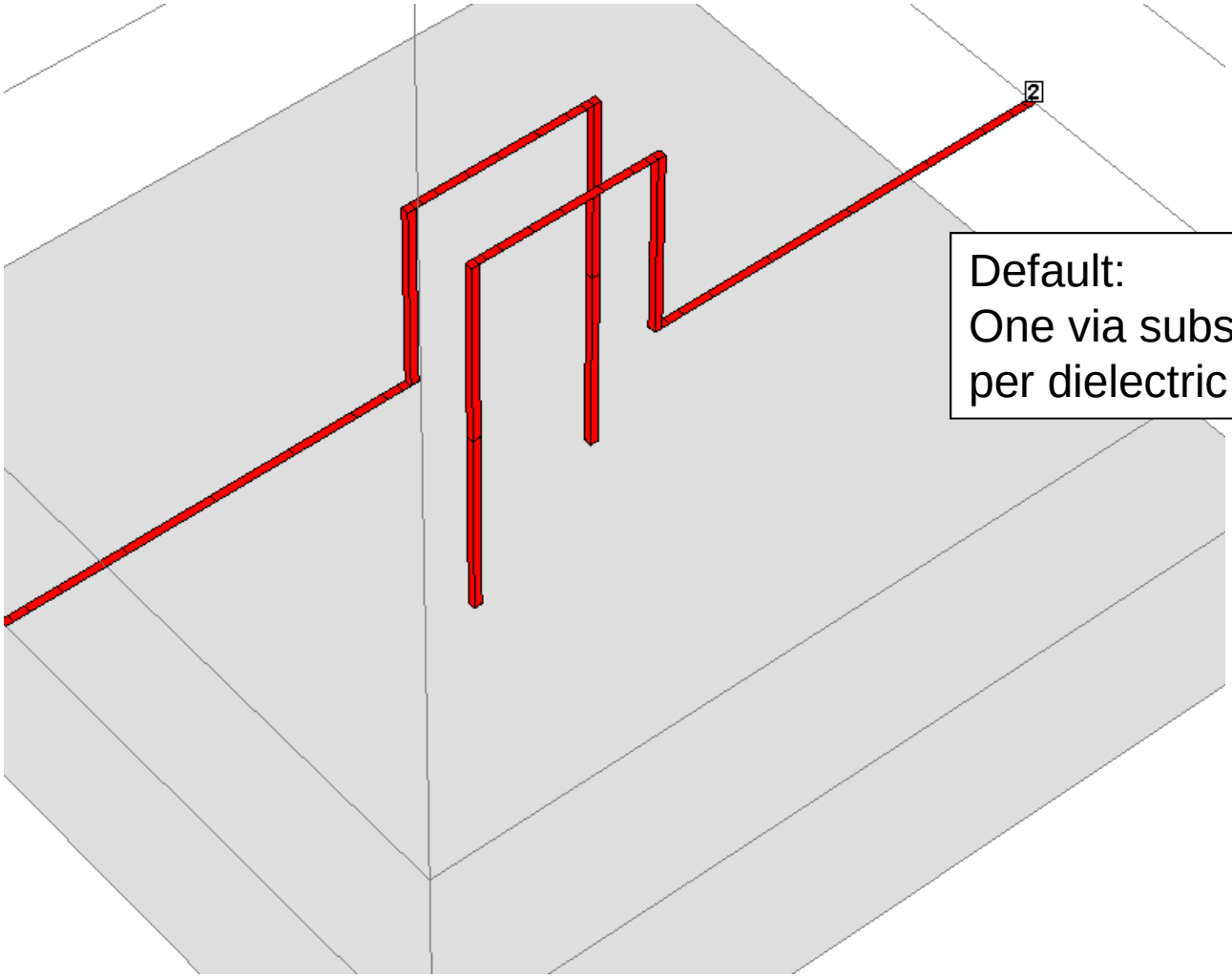
Estimated inductance $L = 1.278 \times 10^{-9}$

Double Bond Wire



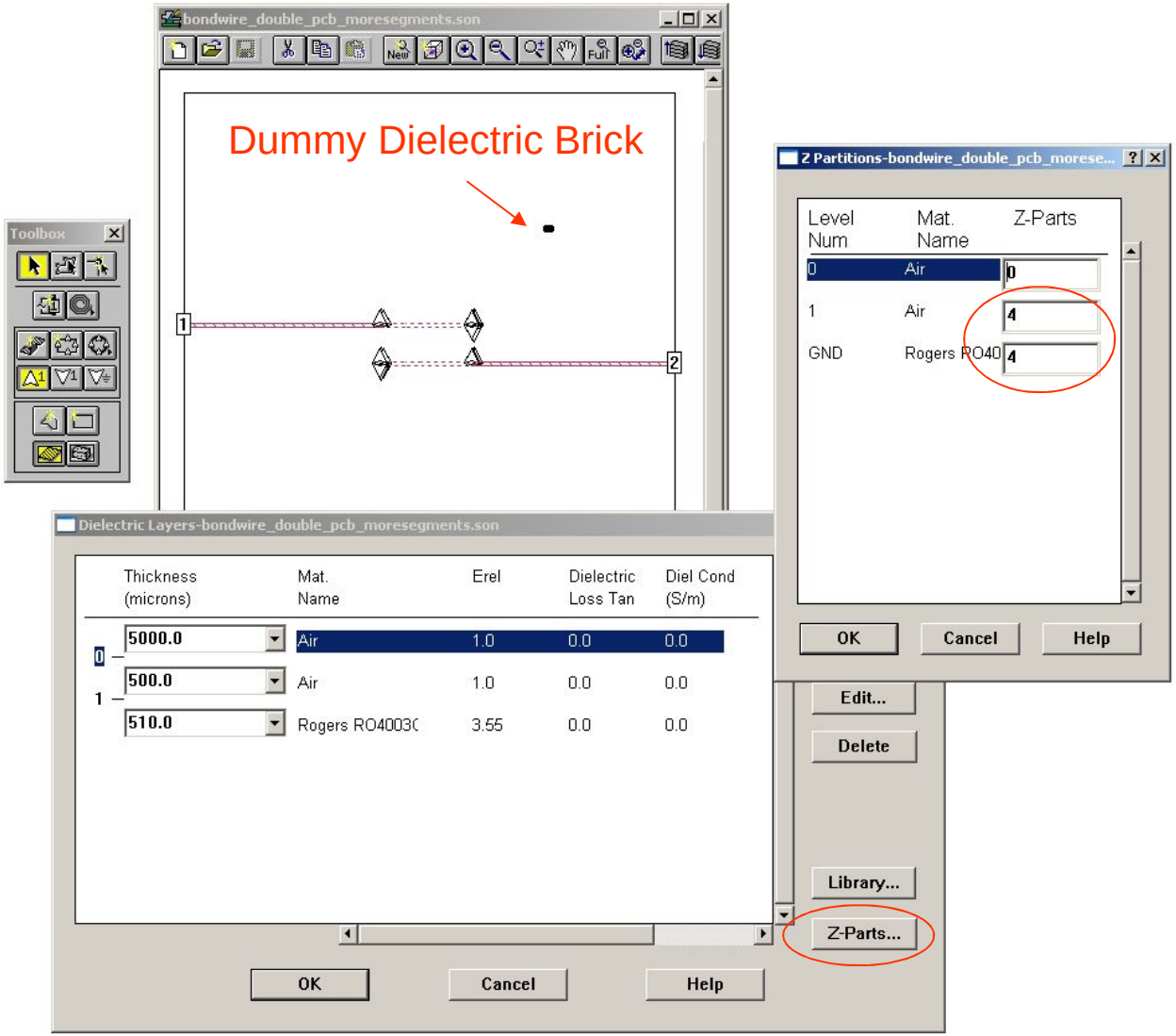


Subsections

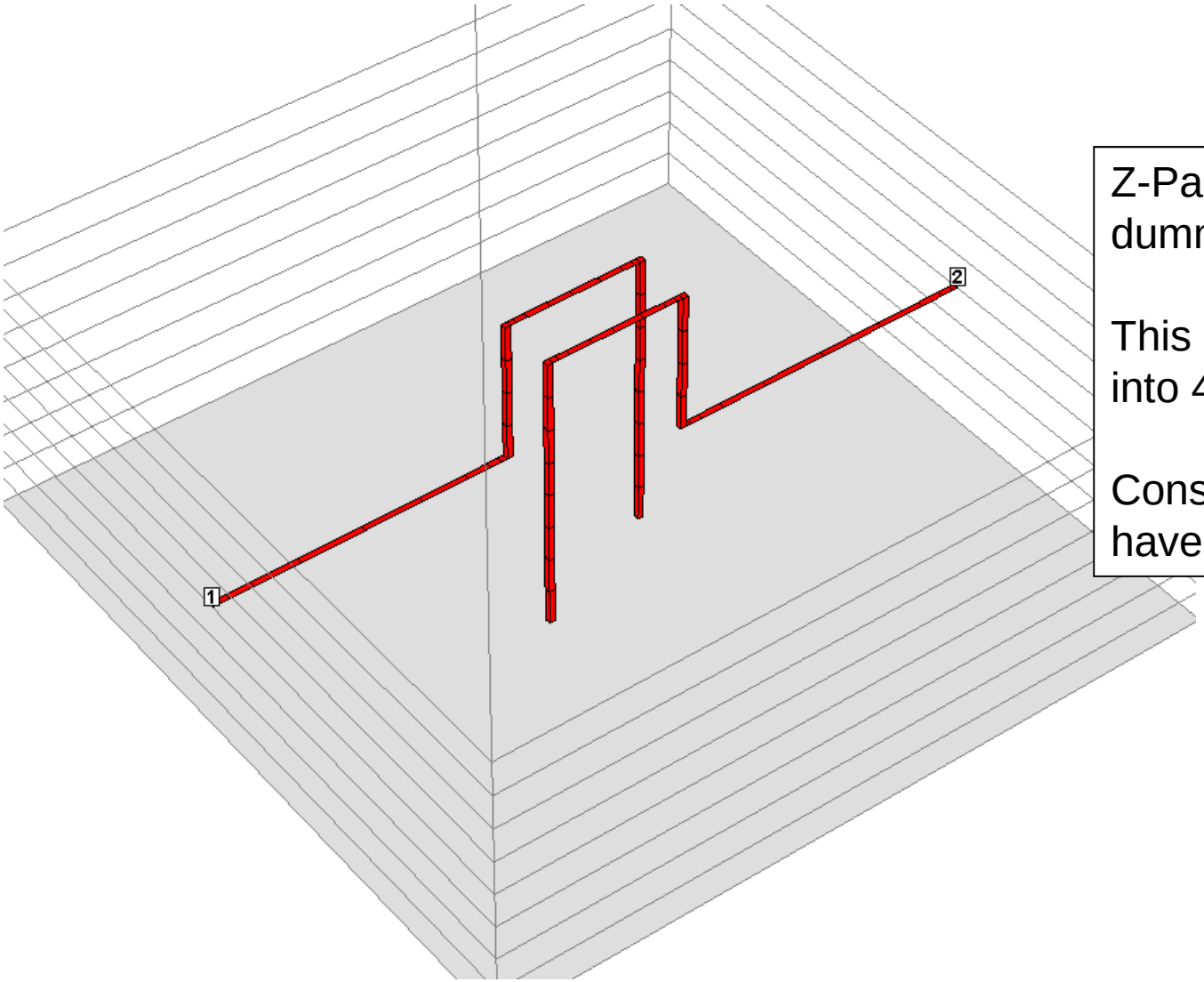


Default:
One via subsection per dielectric layer

Add more vertical subsections



More Subsections

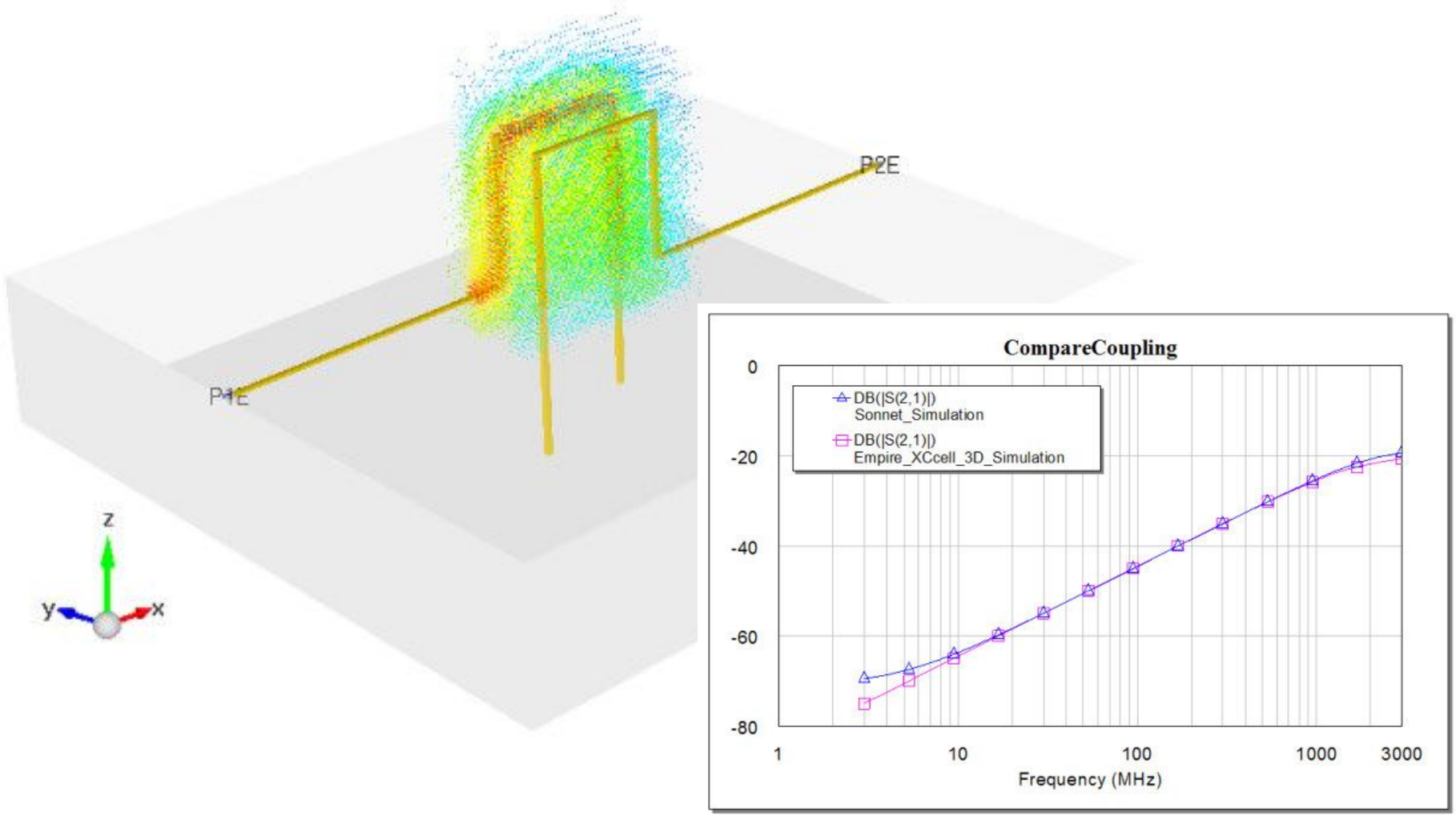


Z-Parts = 4 for layers with dummy brick:

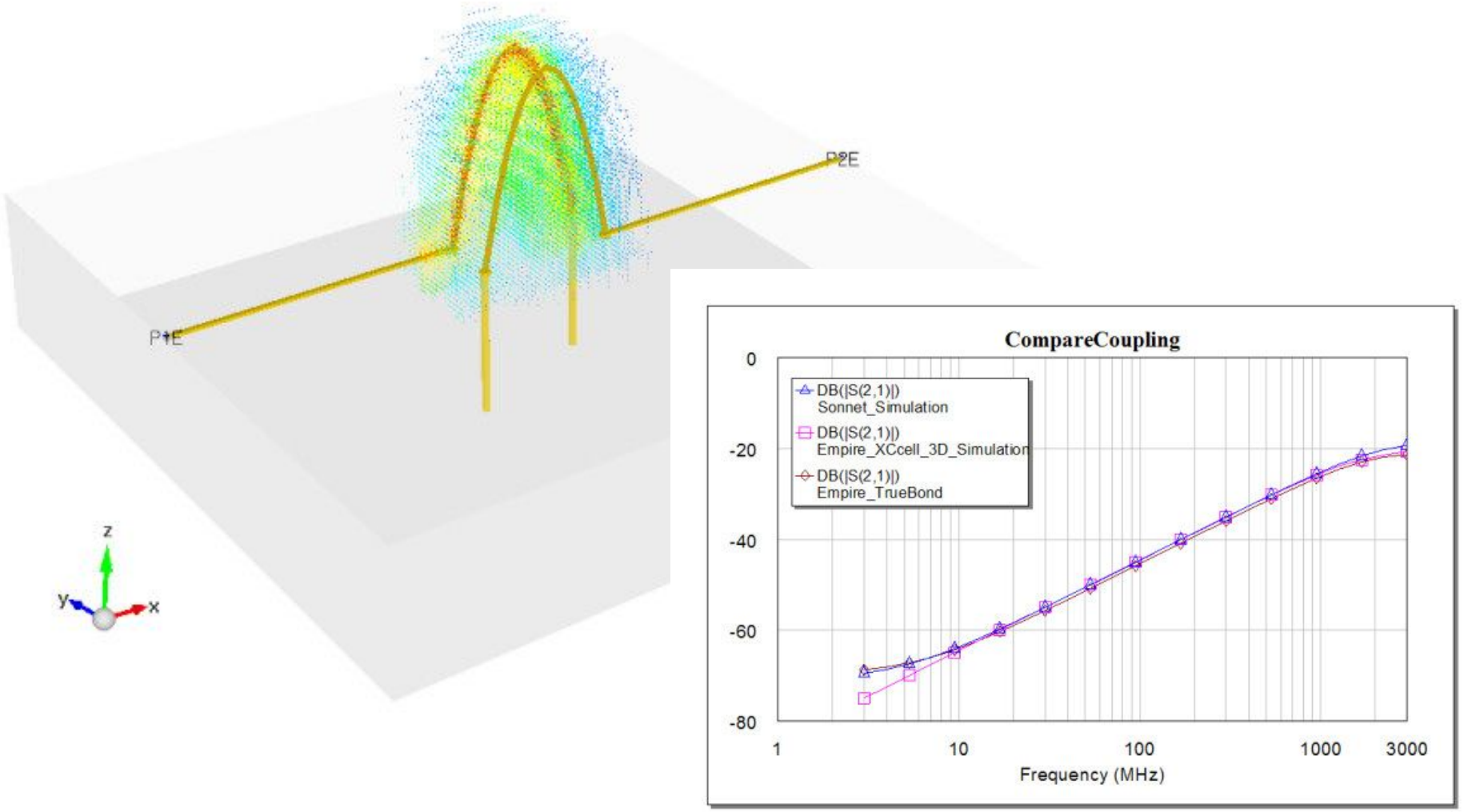
This divides dielectric layer into 4 pieces for the solver.

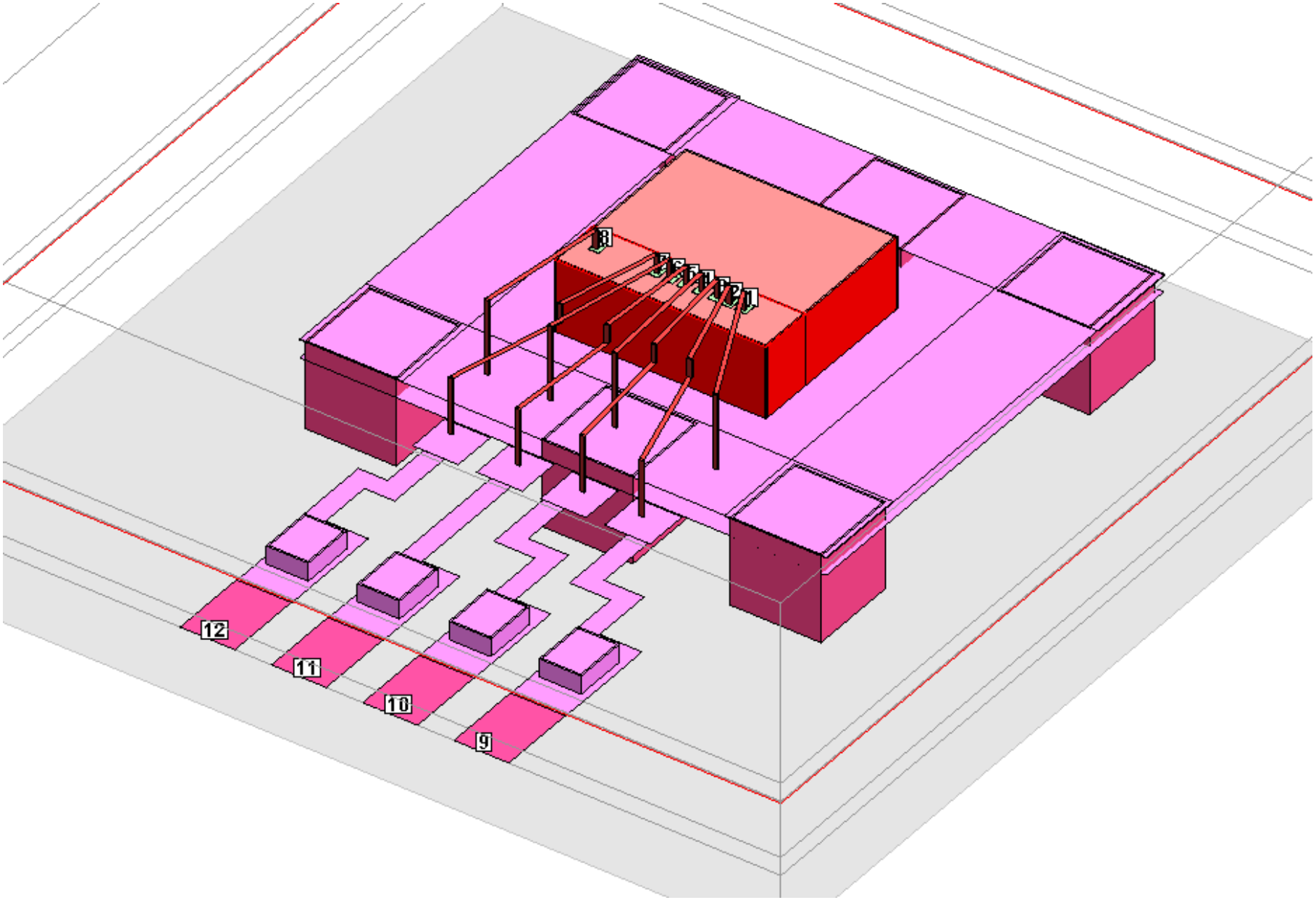
Consequently, vias also have more segements.

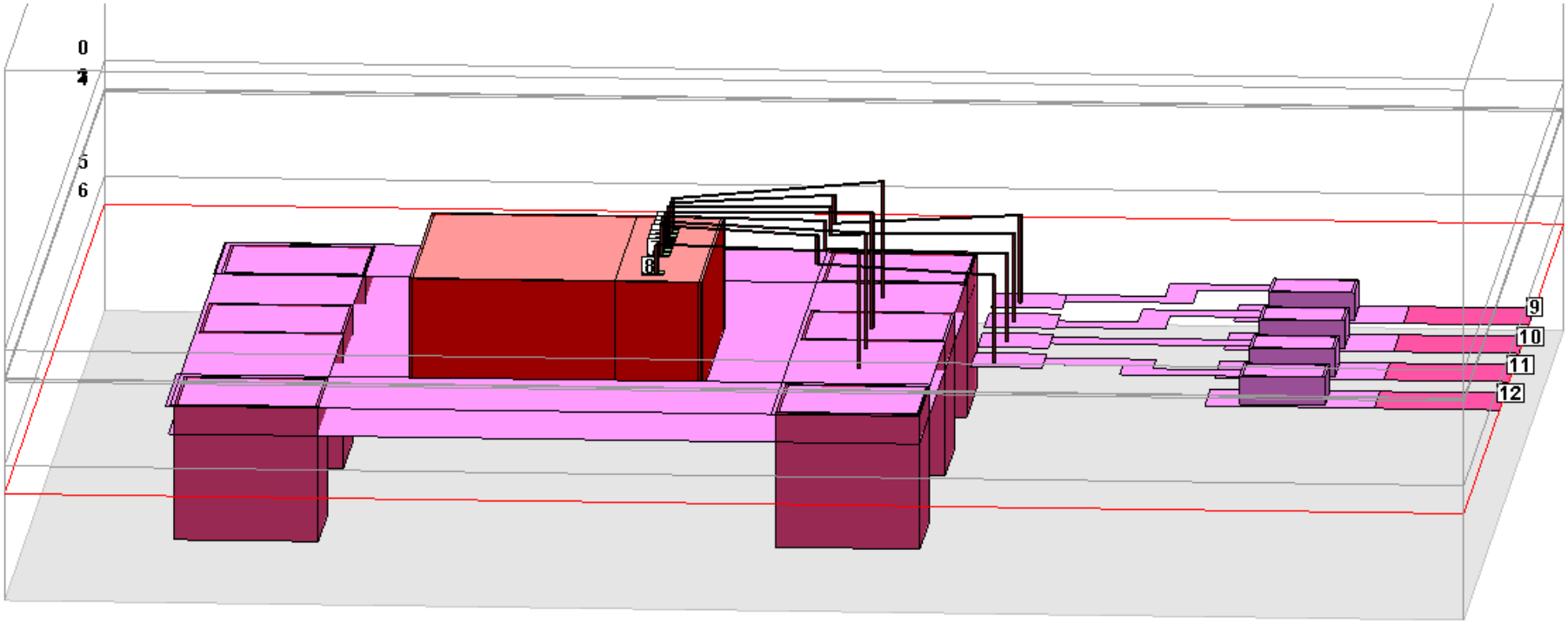
Compare to Empire 3D FDTD



Curved with same Length




12
11
10
9


0
4
5
6
8
9
10
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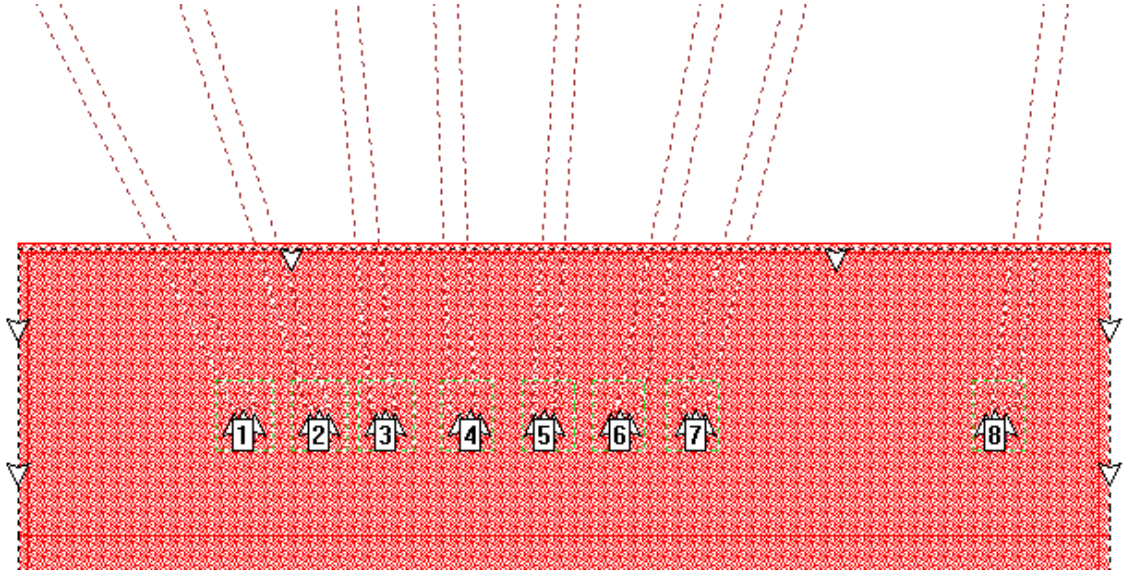
12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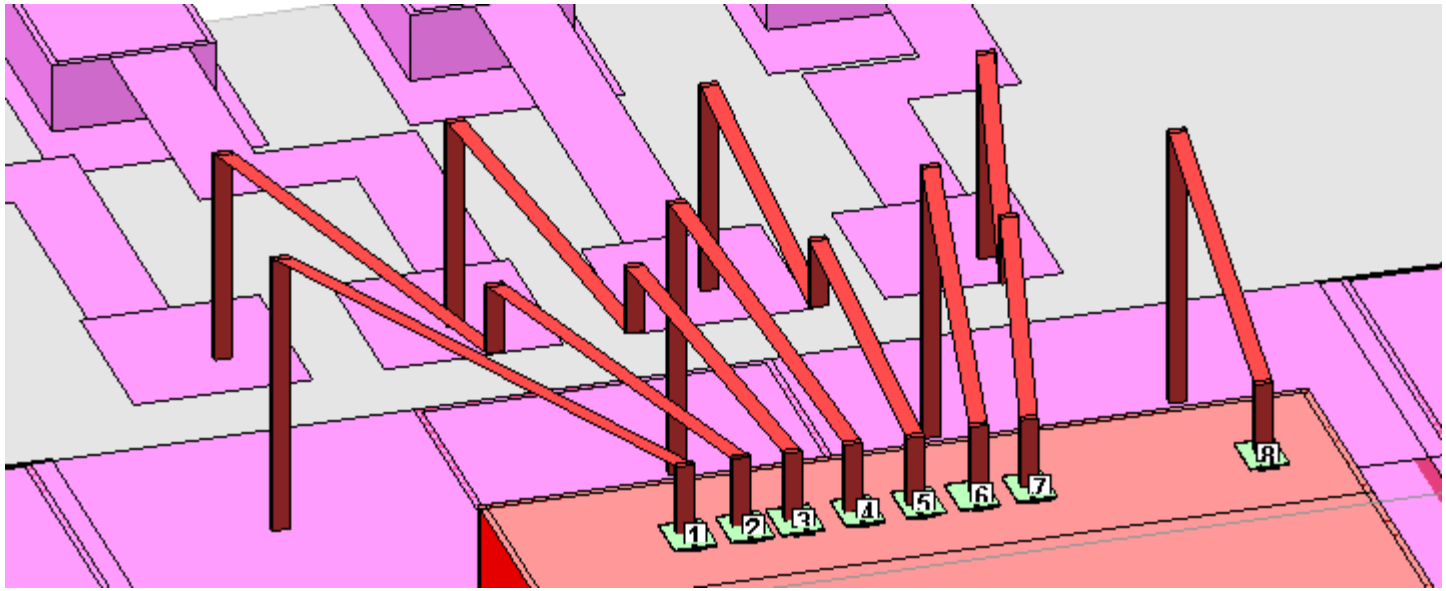
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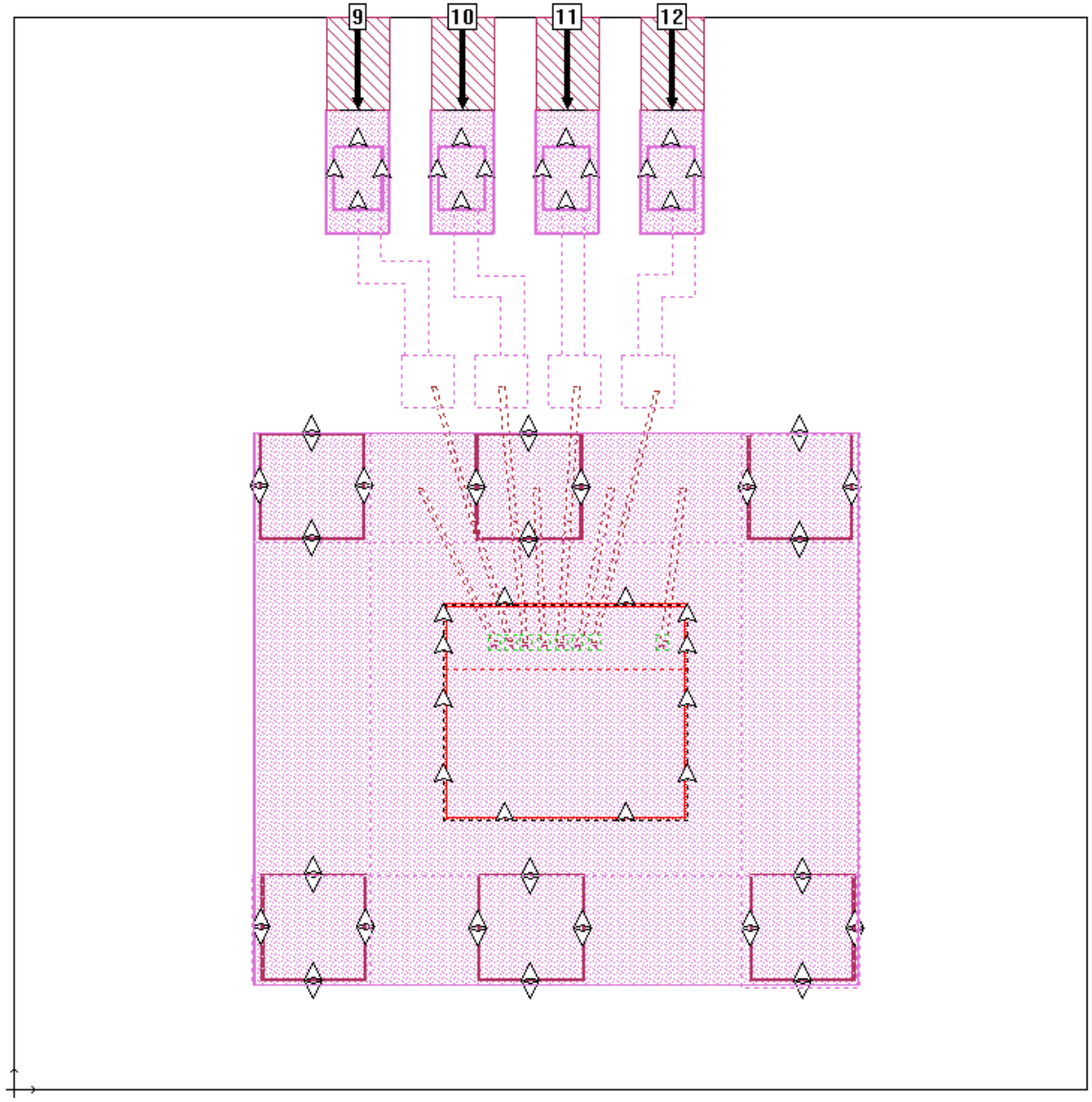
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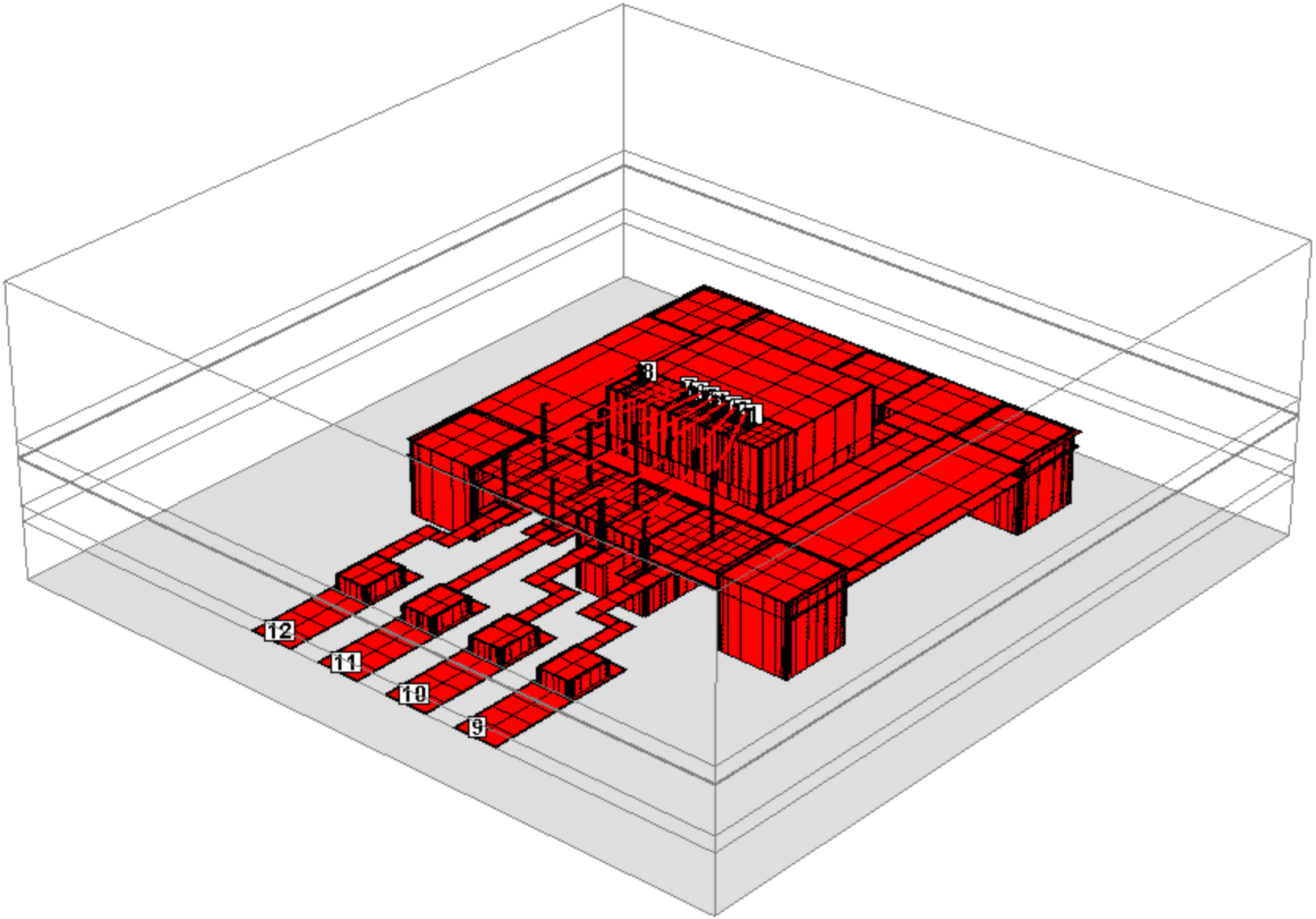
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