Ghibli_CFS Schematic

CFL-H

2018/08/22

REV :SC

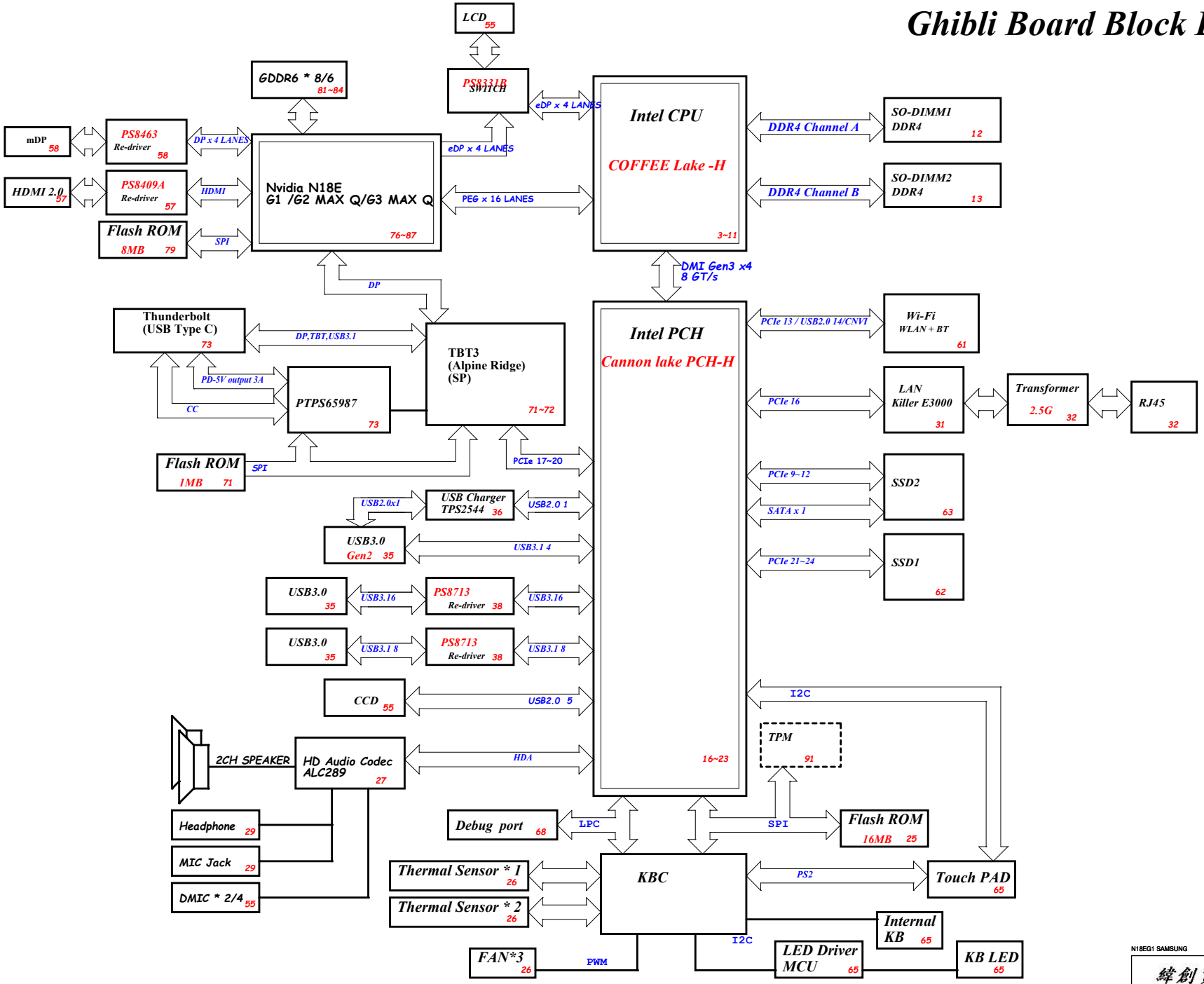
DY : None Installed
OPS: DISCRTE OPTIMUS installed

N18EG1 SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Block Diagram	
Size A4	Document Number Ghibli_CFL	Rev SC
Date: Monday, December 03, 2018	Sheet 1 of 106	

Ghibli Board Block Diagram



CHARGER BQ24781	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC RT6575D	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5

CPU Core Power NCP81215	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

DDR4 power RT8231	
INPUTS	OUTPUTS
DCBATOUT	1D2V_S3 0D6V_S0

2D5V_S3 APL5934	
INPUTS	OUTPUTS
3D3V_S5	2D5V_S3

1D05V_S5 AOZ2262	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S5

Switches 40	
INPUTS	OUTPUTS
5V_S5 3D3V_S5 1D0V_S5	5V_S0 3D3V_S0 0D95V_VCCIO 1V_VCCST

1D35V_VGA_S0 RT8816B	
INPUTS	OUTPUTS
DCBATOUT	1D35V_VGA_S0

NVVDD_S0 MP2886A	
INPUTS	OUTPUTS
DCBATOUT	NVVDDS0

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

Size: C | Document Number: Ghibli_CFL | Rev: SC

Date: Tuesday, December 04, 2018 | Sheet 2 of 106

PEG

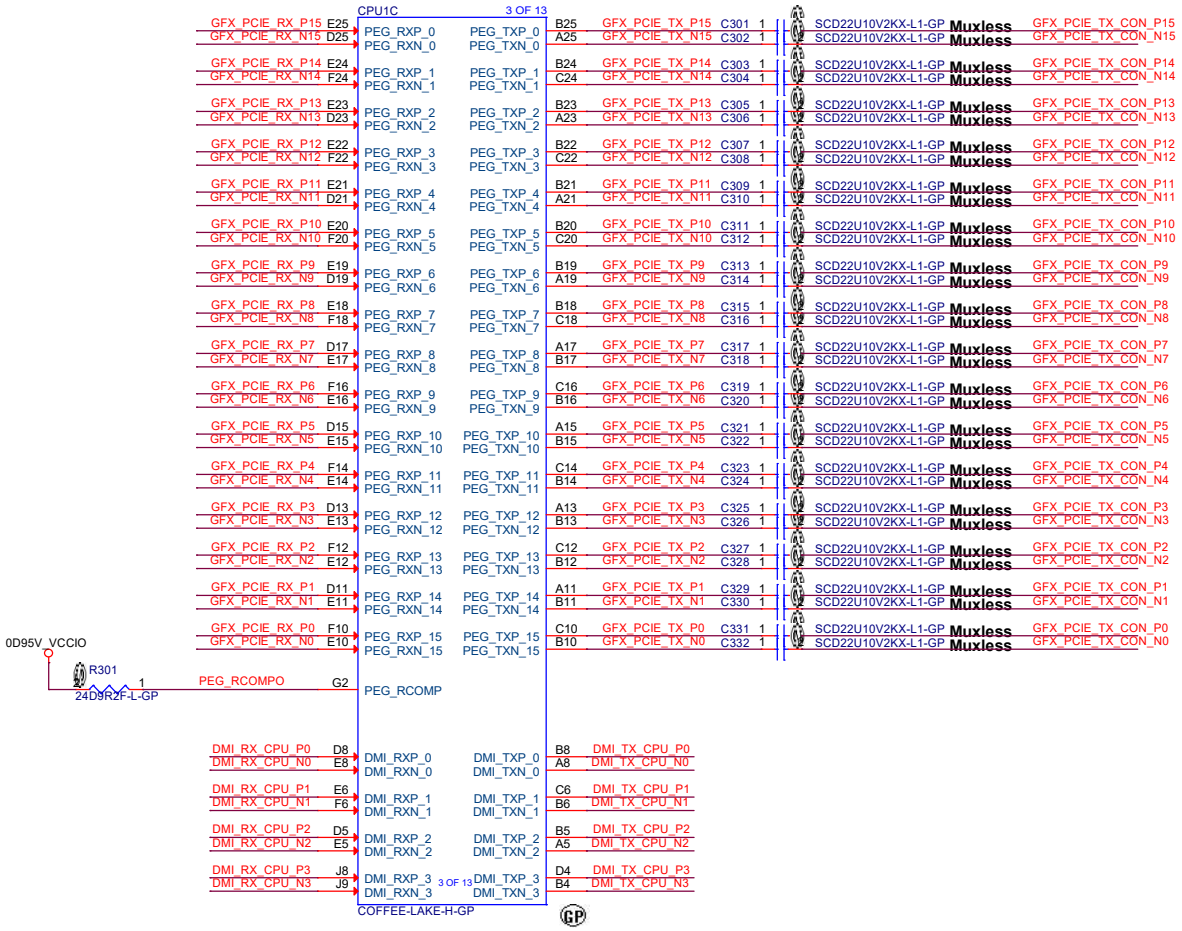
[76] GFX_PCIE_RX_N0
[76] GFX_PCIE_RX_P0
[76] GFX_PCIE_RX_N1
[76] GFX_PCIE_RX_P1
[76] GFX_PCIE_RX_N2
[76] GFX_PCIE_RX_P2
[76] GFX_PCIE_RX_N3
[76] GFX_PCIE_RX_P3
[76] GFX_PCIE_RX_N4
[76] GFX_PCIE_RX_P4
[76] GFX_PCIE_RX_N5
[76] GFX_PCIE_RX_P5
[76] GFX_PCIE_RX_N6
[76] GFX_PCIE_RX_P6
[76] GFX_PCIE_RX_N7
[76] GFX_PCIE_RX_P7
[76] GFX_PCIE_RX_N8
[76] GFX_PCIE_RX_P8
[76] GFX_PCIE_RX_N9
[76] GFX_PCIE_RX_P9
[76] GFX_PCIE_RX_N10
[76] GFX_PCIE_RX_P10
[76] GFX_PCIE_RX_N11
[76] GFX_PCIE_RX_P11
[76] GFX_PCIE_RX_N12
[76] GFX_PCIE_RX_P12
[76] GFX_PCIE_RX_N13
[76] GFX_PCIE_RX_P13
[76] GFX_PCIE_RX_N14
[76] GFX_PCIE_RX_P14
[76] GFX_PCIE_RX_N15
[76] GFX_PCIE_RX_P15

[76] GFX_PCIE_TX_CON_N0
[76] GFX_PCIE_TX_CON_P0
[76] GFX_PCIE_TX_CON_N1
[76] GFX_PCIE_TX_CON_P1
[76] GFX_PCIE_TX_CON_N2
[76] GFX_PCIE_TX_CON_P2
[76] GFX_PCIE_TX_CON_N3
[76] GFX_PCIE_TX_CON_P3
[76] GFX_PCIE_TX_CON_N4
[76] GFX_PCIE_TX_CON_P4
[76] GFX_PCIE_TX_CON_N5
[76] GFX_PCIE_TX_CON_P5
[76] GFX_PCIE_TX_CON_N6
[76] GFX_PCIE_TX_CON_P6
[76] GFX_PCIE_TX_CON_N7
[76] GFX_PCIE_TX_CON_P7
[76] GFX_PCIE_TX_CON_N8
[76] GFX_PCIE_TX_CON_P8
[76] GFX_PCIE_TX_CON_N9
[76] GFX_PCIE_TX_CON_P9
[76] GFX_PCIE_TX_CON_N10
[76] GFX_PCIE_TX_CON_P10
[76] GFX_PCIE_TX_CON_N11
[76] GFX_PCIE_TX_CON_P11
[76] GFX_PCIE_TX_CON_N12
[76] GFX_PCIE_TX_CON_P12
[76] GFX_PCIE_TX_CON_N13
[76] GFX_PCIE_TX_CON_P13
[76] GFX_PCIE_TX_CON_N14
[76] GFX_PCIE_TX_CON_P14
[76] GFX_PCIE_TX_CON_N15
[76] GFX_PCIE_TX_CON_P15

DMI

[16] DMI_RX_CPU_P0
[16] DMI_RX_CPU_N0
[16] DMI_RX_CPU_P1
[16] DMI_RX_CPU_N1
[16] DMI_RX_CPU_P2
[16] DMI_RX_CPU_N2
[16] DMI_RX_CPU_P3
[16] DMI_RX_CPU_N3

[16] DMI_TX_CPU_P0
[16] DMI_TX_CPU_N0
[16] DMI_TX_CPU_P1
[16] DMI_TX_CPU_N1
[16] DMI_TX_CPU_P2
[16] DMI_TX_CPU_N2
[16] DMI_TX_CPU_P3
[16] DMI_TX_CPU_N3



Parameter	Segment	Units	Min Trace Width	Trace Spacing to Other Signals	Max Routing Length	Resistance
PEG_RCOMP [1]	L1	mils	5	15	600	NA
Resistor	R1	Ω	NA	NA	NA	24.9 ± 1%
Note: Must maintain low DC resistance routing (<0.1 Ω)						

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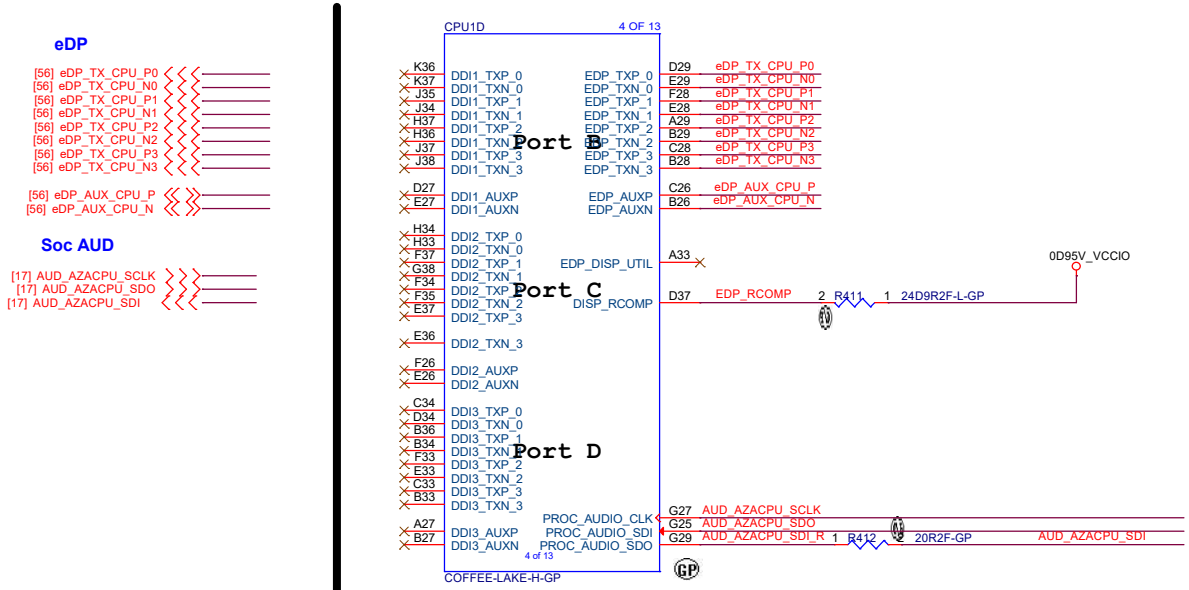
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PEG/DMI)

Size: A3 | Document Number: Ghibli_CFL | Rev: SC

Date: Monday, December 03, 2018 | Sheet 3 of 106



Signal	Min Trace Width	Isolation Spacing	Resistor Value	Max Length
DISP_RCOMP	5 mils	20 mils	24.9 Ω ±1%	600 mils
Note: Must maintain low DC resistance routing (<0.1Ω)				

Resistor Value	Rs	NA	Ω	20

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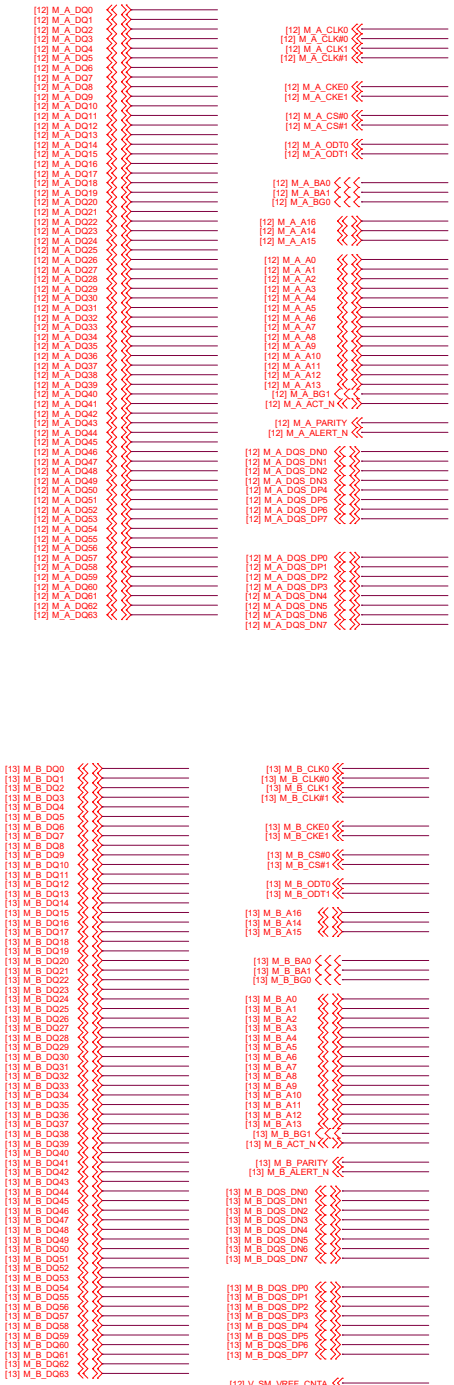
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

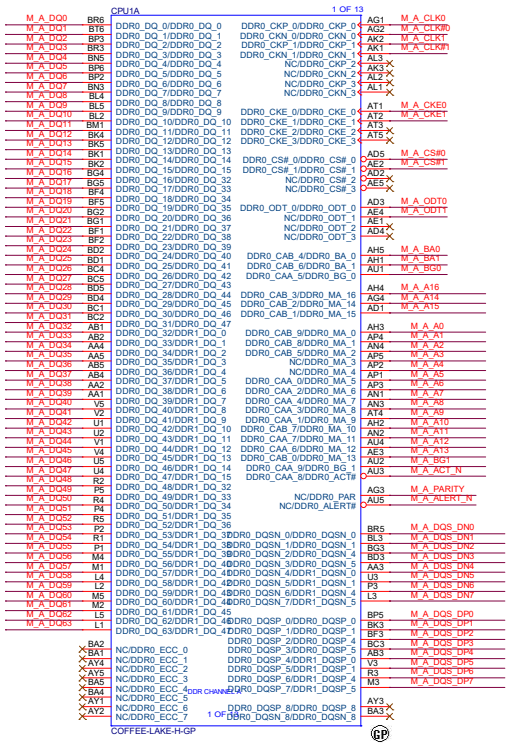
Title: CPU (DDI/EDP)

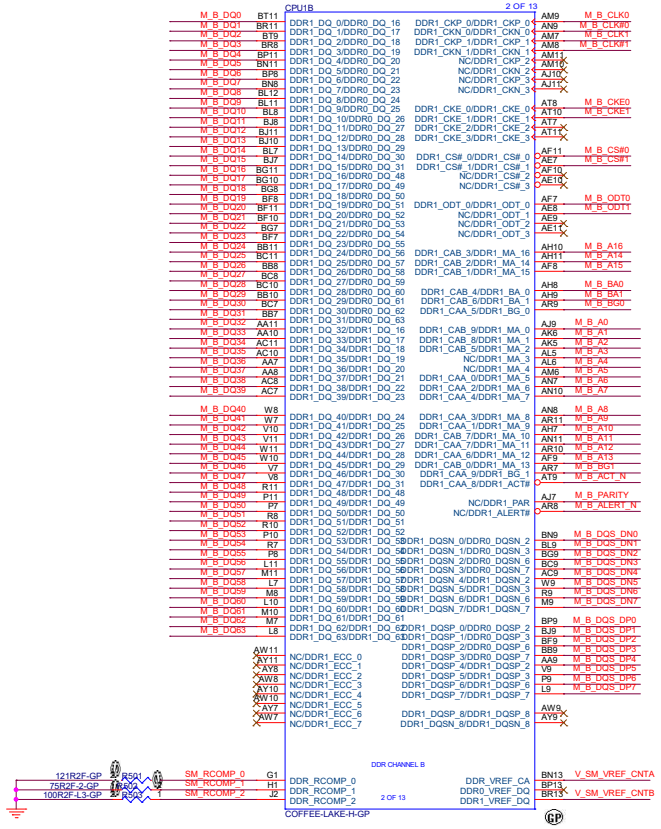
Size: A3 | Document Number: Ghibli_CFL | Rev: SC

Date: Monday, December 03, 2018 | Sheet 4 of 106

SSID = CPU







RCOMP [0]	M	MS	VSS	2	12-15					20	25/25				500	121
RCOMP [1]	M	MS	VSS	2	12-15					20	25/25				500	75
RCOMP [2]	M	MS	VSS	2	12-15					20	25/25				500	100

N18EG1 SAMSUNG

緯創資通 Wistron Corporation
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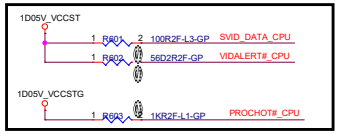
Title: CPU (DDR)

Size: A2 | Document Number: Ghibli_CFL | Rev: SC

Date: Monday, December 03, 2018 | Sheet 5 of 106

AROUND_CPU



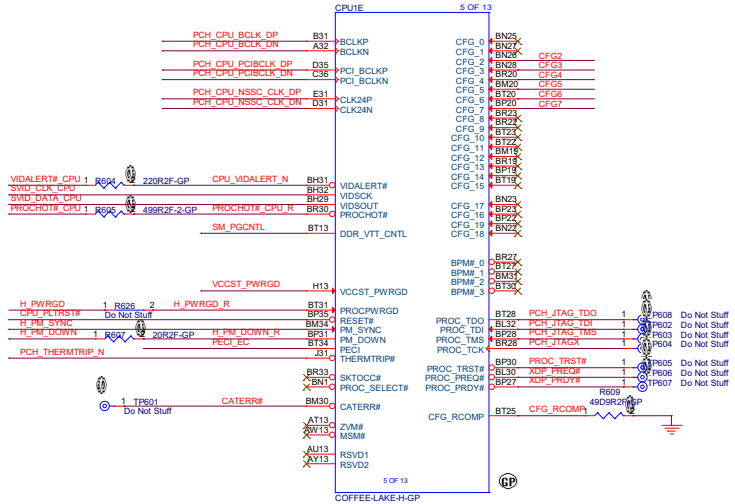


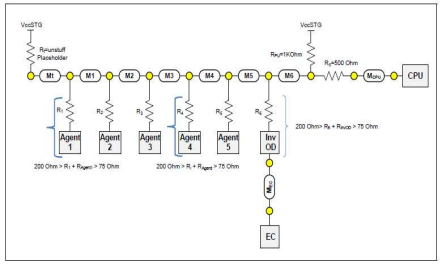
Table 6-8. Reset and Miscellaneous Signals

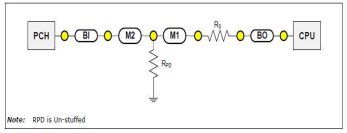
Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: – 1 = (Default) Normal Operation; No stall. – 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal. – 1 = Normal operation – 0 = Lane numbers reversed. • **CFG[3]**: Reserved configuration lane. • **CFG[4]**: eDP enable: – 1 = Disabled. – 0 = Enabled. • **CFG[6:5]**: PCI Express* Bifurcation – 00 = 1 x8, 2 x4 PCI Express* – 01 = reserved – 10 = 2 x8 PCI Express* – 11 = 1 x16 PCI Express* • **CFG[7]**: PEG Training: – 1 = (default) PEG Train immediately following RESET# de assertion. – 0 = PEG Wait for BIOS for training. • **CFG[19:8]**: Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

Table 13-14. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

Note: For additional information regarding SVID and power management refer to *"Power Architecture Guide"*.

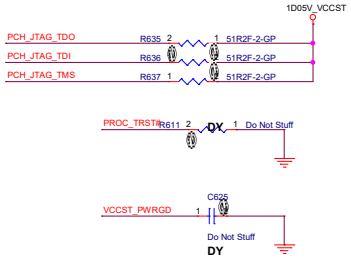


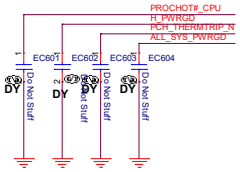


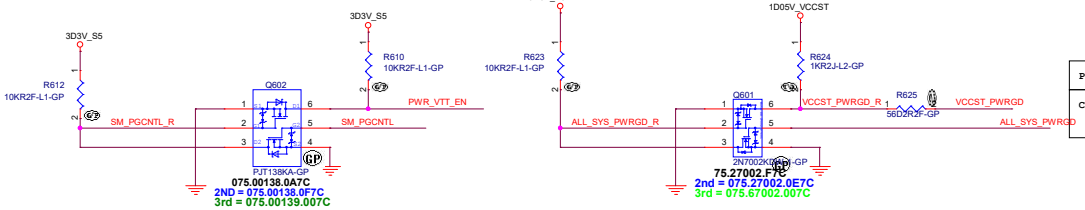
Note: RPD is Un-stuffed

.2. PM_DOWN Routing Guidelines

Parameter	Segment	Stackup (MS/SL/DSL)	Units	Routing Recommendation
Breakout Length: Short route: M1 + M2 > 3" Long route: M1 + M2 < 3"	BO	MS/SL/DSL	inches	<0.2 <0.6
M1+M2: Short route Long route	Mi	MS/SL/DSL	inches	1-3 3-11
Breakin Length Max.	BI	MS/SL/DSL	inches	<0.5
Resistor Value (±5%)	Rs	NA	Ω	20
Resistor Value (±5%)	R_{PD}	NA	Ω	Unstuffed
Note: All segments are 50 Ω and vias are optional.				







PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition. 0:Lane Reversed

eDP Enable	
CFG4	1:Disable 0:Enable

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Physical_Debug_Enabled (DFX privacy)	
CFG4	1:Disable 0:Enable (Set DXF enables bit in debug)

PEG Training	
CFG7	1:(default) PEG Train immediately following RESET# de assertion. 0 = PEG Wait for BIOS for training.

N18EG1 SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (SVID/CFG/JTAG/CLK)

Size: A2 | Document Number: Ghibli_CFL | Rev: SC

Date: Tuesday, December 04, 2018 | Sheet 6 of 106

SSID = CPU

[46] VCCCORE_SENSE
[46] VSSCORE_SENSE
[46] VSSGT_SENSE
[46] VCCGT_SENSE

1V_CPU_CORE

CPU1I — 9 OF 13 — COFFEE-LAKE-H-GP

AA13			AH13
AA31	VCC1	VCC64	AH14
AA32	VCC2	VCC65	AH29
AA33	VCC3	VCC66	AH30
AA34	VCC4	VCC67	AH31
AA35	VCC5	VCC68	AH32
AA36	VCC6	VCC69	AJ14
AA37	VCC7	VCC70	AJ29
AA38	VCC8	VCC71	AJ30
AB29	VCC9	VCC72	AJ31
AB30	VCC10	VCC73	AJ32
AB31	VCC11	VCC74	AJ33
AB32	VCC12	VCC75	AJ34
AB35	VCC13	VCC76	AJ35
AB36	VCC14	VCC77	AJ36
AB37	VCC15	VCC78	AK31
AB38	VCC16	VCC79	AK32
AC13	VCC17	VCC80	AK33
AC14	VCC18	VCC81	AK34
AC29	VCC19	VCC82	AK35
AC30	VCC20	VCC83	AK36
AC31	VCC21	VCC84	AK37
AC32	VCC22	VCC85	AK38
AC33	VCC23	VCC86	AL13
AC34	VCC24	VCC87	AL29
AC35	VCC25	VCC88	AL30
AC36	VCC26	VCC89	AL31
AD13	VCC27	VCC90	AL32
AD14	VCC28	VCC91	AL35
AD31	VCC29	VCC92	AL36
AD32	VCC30	VCC93	AL37
AD33	VCC31	VCC94	AL38
AD34	VCC32	VCC95	AM13
AD35	VCC33	VCC96	AM14
AD36	VCC34	VCC97	AM29
AD37	VCC35	VCC98	AM30
AD38	VCC36	VCC99	AM31
AE13	VCC37	VCC100	AM32
AE14	VCC38	VCC101	AM33
AE30	VCC39	VCC102	AM34
AE31	VCC40	VCC103	AM35
AE32	VCC41	VCC104	AM36
AE35	VCC42	VCC105	AN13
AE36	VCC43	VCC106	AN14
AE37	VCC44	VCC107	AN31
AE38	VCC45	VCC108	AN32
AF29	VCC46	VCC109	AN33
AF30	VCC47	VCC110	AN34
AF31	VCC48	VCC111	AN35
AF32	VCC49	VCC112	AN36
AF33	VCC50	VCC113	AN37
AF34	VCC51	VCC114	AN38
AF35	VCC52	VCC115	AP13
AF36	VCC53	VCC116	AP30
AF37	VCC54	VCC117	AP31
AF38	VCC55	VCC118	AP32
AG14	VCC56	VCC119	AP35
AG31	VCC57	VCC120	AP36
AG32	VCC58	VCC121	AP37
AG33	VCC59	VCC122	AP38
AG34	VCC60	VCC123	K13
AG35	VCC61	VCC124	
AG36	VCC62		
	VCC63		

9 OF 13
VCC_SENSE — AG37 — VCCCORE_SENSE
VSS_SENSE — AG38 — VSSCORE_SENSE

1V_CPU_CORE
R701 100R2F-L3-GP
R702 100R2F-L3-GP
NEAR CPU

1V_VCCGT

CPU1K — 11 OF 13 — COFFEE-LAKE-H-GP

AT14			BD35
AT31	VCCGT1	VCCGT80	BD36
AT32	VCCGT2	VCCGT81	BE31
AT33	VCCGT3	VCCGT82	BE32
AT34	VCCGT4	VCCGT83	BE33
AT35	VCCGT5	VCCGT84	BE34
AT36	VCCGT6	VCCGT85	BE35
AT37	VCCGT7	VCCGT86	BE36
AT38	VCCGT8	VCCGT87	BE37
AU14	VCCGT9	VCCGT88	BE38
AU29	VCCGT10	VCCGT89	BF13
AU30	VCCGT11	VCCGT90	BF14
AU31	VCCGT12	VCCGT91	BF29
AU32	VCCGT13	VCCGT92	BF30
AU35	VCCGT14	VCCGT93	BF31
AU36	VCCGT15	VCCGT94	BF32
AU37	VCCGT16	VCCGT95	BF35
AU38	VCCGT17	VCCGT96	BF36
AV29	VCCGT18	VCCGT97	BF37
AV30	VCCGT19	VCCGT98	BF38
AV31	VCCGT20	VCCGT99	BG29
AV32	VCCGT21	VCCGT100	BG30
AV33	VCCGT22	VCCGT101	BG31
AV34	VCCGT23	VCCGT102	BG32
AV35	VCCGT24	VCCGT103	BG33
AV36	VCCGT25	VCCGT104	BG34
AW14	VCCGT26	VCCGT105	BG35
AW31	VCCGT27	VCCGT106	BG36
AW32	VCCGT28	VCCGT107	BH33
AW33	VCCGT29	VCCGT108	BH34
AW34	VCCGT30	VCCGT109	BH35
AW35	VCCGT31	VCCGT110	BH36
AW36	VCCGT32	VCCGT111	BH37
AW37	VCCGT33	VCCGT112	BH38
AW38	VCCGT34	VCCGT113	BJ16
AY29	VCCGT35	VCCGT114	BJ17
AY30	VCCGT36	VCCGT115	BJ19
AY31	VCCGT37	VCCGT116	BJ20
AY32	VCCGT38	VCCGT117	BJ21
AY35	VCCGT39	VCCGT118	BJ23
AY36	VCCGT40	VCCGT119	BJ24
AY37	VCCGT41	VCCGT120	BJ26
AY38	VCCGT42	VCCGT121	BJ27
BA13	VCCGT43	VCCGT122	BJ37
BA14	VCCGT44	VCCGT123	BJ38
BA29	VCCGT45	VCCGT124	BK16
BA30	VCCGT46	VCCGT125	BK17
BA31	VCCGT47	VCCGT126	BK19
BA32	VCCGT48	VCCGT127	BK20
BA33	VCCGT49	VCCGT128	BK21
BA34	VCCGT50	VCCGT129	BK23
BA35	VCCGT51	VCCGT130	BK24
BA36	VCCGT52	VCCGT131	BK26
BB13	VCCGT53	VCCGT132	BK27
BB14	VCCGT54	VCCGT133	BL15
BB31	VCCGT55	VCCGT134	BL16
BB32	VCCGT56	VCCGT135	BL17
BB33	VCCGT57	VCCGT136	BL23
BB34	VCCGT58	VCCGT137	BL24
BB35	VCCGT59	VCCGT138	BL25
BB36	VCCGT60	VCCGT139	BL26
BB37	VCCGT61	VCCGT140	BL27
BB38	VCCGT62	VCCGT141	BL28
BC29	VCCGT63	VCCGT142	BL36
BC30	VCCGT64	VCCGT143	BL37
BC31	VCCGT65	VCCGT144	BM15
BC32	VCCGT66	VCCGT145	BM16
BC35	VCCGT67	VCCGT146	BM17
BC36	VCCGT68	VCCGT147	BM36
BC37	VCCGT69	VCCGT148	BM37
BC38	VCCGT70	VCCGT149	BN15
BD13	VCCGT71	VCCGT150	BN16
BD14	VCCGT72	VCCGT151	BN17
BD29	VCCGT73	VCCGT152	BN36
BD30	VCCGT74	VCCGT153	BN37
BD31	VCCGT75	VCCGT154	BN38
BD32	VCCGT76	VCCGT155	BP15
BD33	VCCGT77	VCCGT156	BP16
BD34	VCCGT78	VCCGT157	BP17
BP37	VCCGT79	VCCGT158	BR37
BP38	VCCGT159	VCCGT164	BT15
BR15	VCCGT160	VCCGT165	BT16
BR16	VCCGT161	VCCGT166	BT17
BR17	VCCGT162	VCCGT167	BT37
	VCCGT163	VCCGT168	

11 OF 13
VSSGT_SENSE — AH37 — VSSGT_SENSE
VCCGT_SENSE — AH38 — VCCGT_SENSE

1V_VCCGT
R703 100R2F-L3-GP
R704 100R2F-L3-GP

1V_CPU_CORE

CPU1J — 10 OF 13 — COFFEE-LAKE-H-GP

K14			W35
L13	VCC1	VCC64	W36
L14	VCC2	VCC65	W37
N13	VCC3	VCC66	W38
N14	VCC4	VCC67	Y29
N30	VCC5	VCC68	Y30
N31	VCC6	VCC69	Y31
N32	VCC7	VCC70	Y32
N35	VCC8	VCC71	Y33
N36	VCC9	VCC72	Y34
N37	VCC10	VCC73	Y35
N38	VCC11	VCC74	Y36
P13	VCC12	VCC75	
P14	VCC13		
P29	VCC14		
P30	VCC15		
P31	VCC16		
P32	VCC17		
P33	VCC18		
P34	VCC19		
P35	VCC20		
P36	VCC21		
R13	VCC22		
R31	VCC23		
R32	VCC24		
R33	VCC25		
R34	VCC26		
R35	VCC27		
R36	VCC28		
R37	VCC29		
R38	VCC30		
T29	VCC31		
T30	VCC32		
T31	VCC33		
T32	VCC34		
T35	VCC35		
T36	VCC36		
T37	VCC37		
T38	VCC38		
U29	VCC39		
U30	VCC40		
U31	VCC41		
U32	VCC42		
U33	VCC43		
U34	VCC44		
U35	VCC45		
U36	VCC46		
V13	VCC47		
V14	VCC48		
V31	VCC49		
V32	VCC50		
V33	VCC51		
V34	VCC52		
V35	VCC53		
V36	VCC54		
V37	VCC55		
V38	VCC56		
W13	VCC57		
W14	VCC58		
W29	VCC59		
W30	VCC60		
W31	VCC61		
W32	VCC62		
	VCC63		

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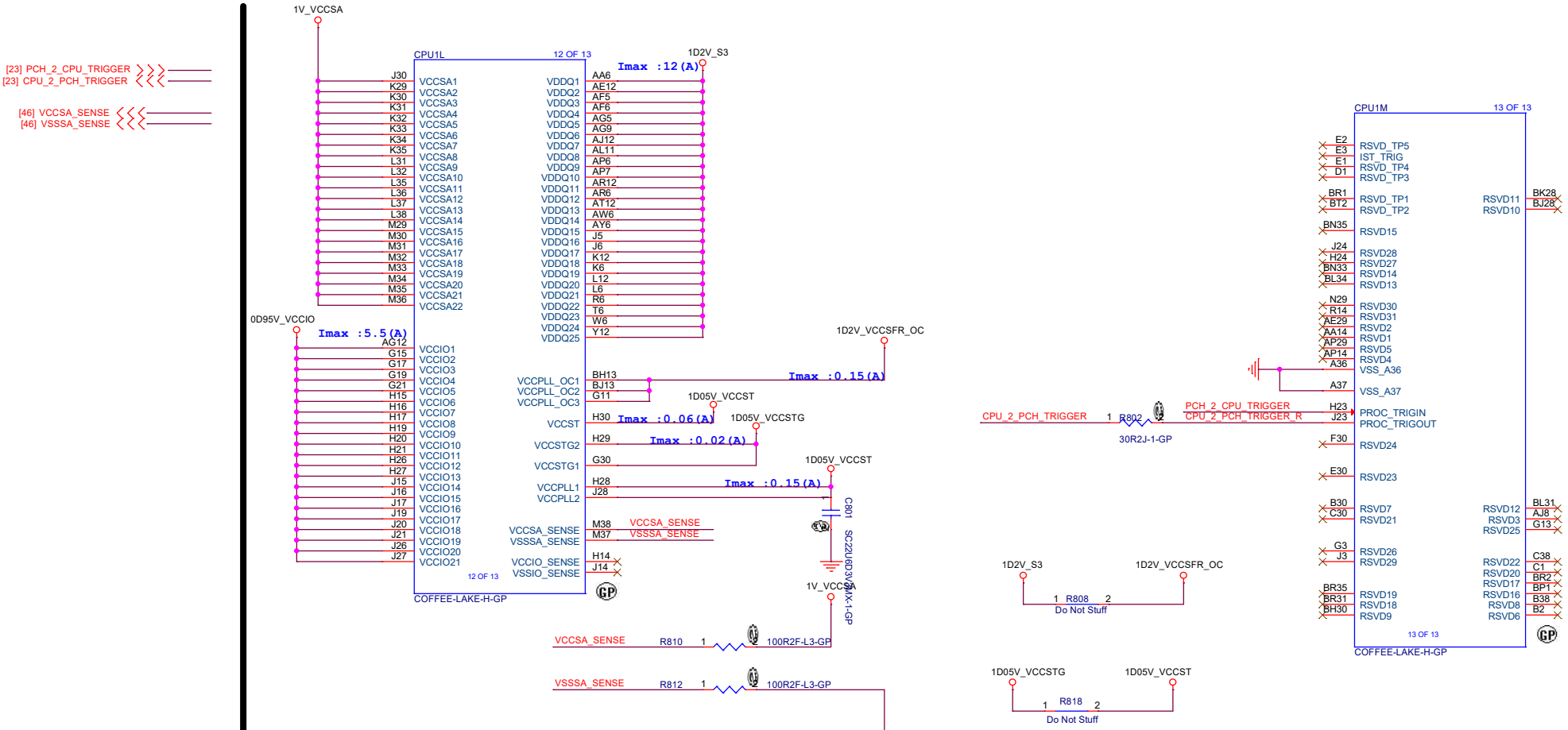
N18EG1 SAMSUNG

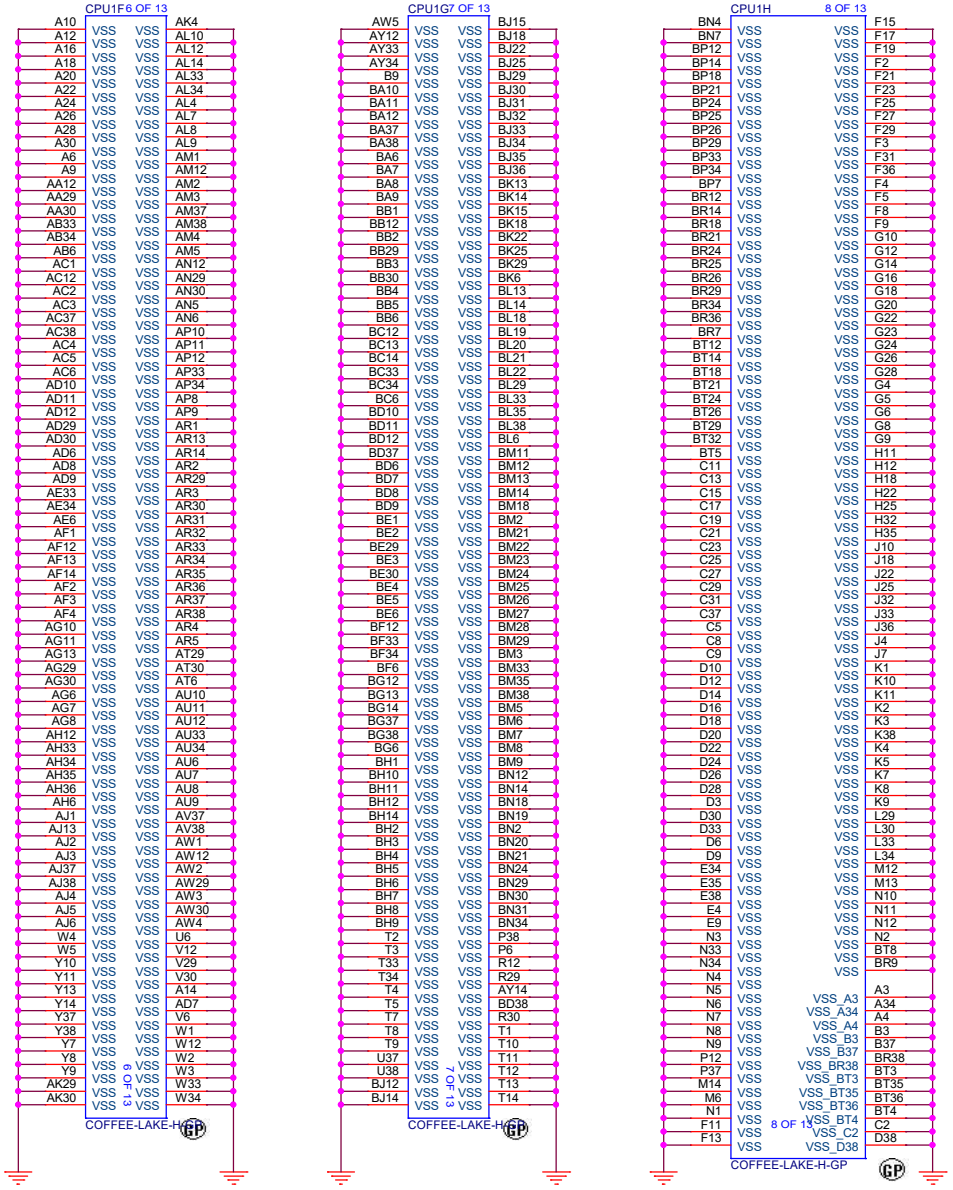
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (VCORE/VCCGT)	
Size A3	Document Number Ghibli_CFL	Rev SC
Date: Monday, December 03, 2018	Sheet 7 of 106	



N18EG1 SAMSUNG

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CPU (CCSA/VCCIO/VDDQ/RSVD)**	
Size: Custom	Document Number: **Ghibli_CFL**	Rev: **SC**
Date: Tuesday, December 04, 2018	Sheet 8 of 106	



N18EG1 SAMSUNG

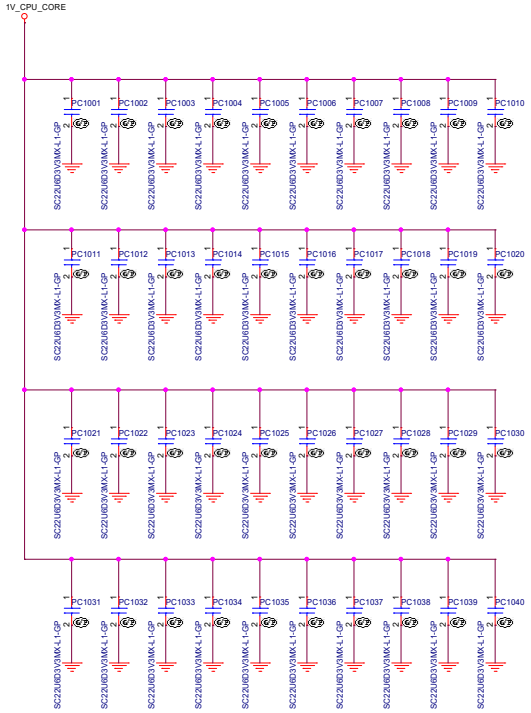
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CPU (VSS)**	
Size A3	Document Number **Ghibli_CFL**	Rev **SC**
Date: Monday, December 03, 2018	Sheet 9 of 106	

Main Func = CPU

VCORE CFL-H_45W

H-line 45W
IccMax current-10ms max = 128A

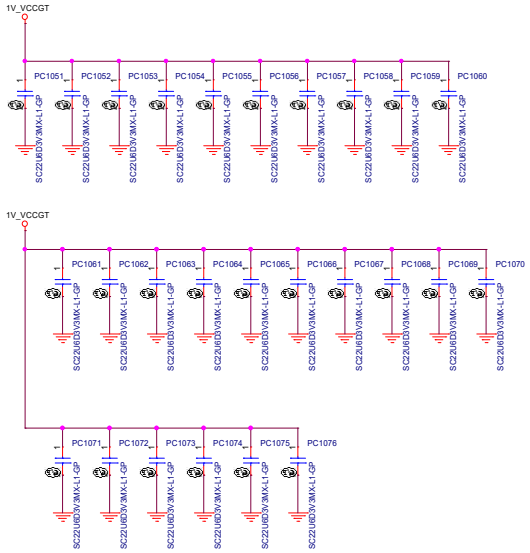
22uF 40 Pcs
DY 0 Pcs



VCCGT CFL-H_45W

IccMax current-10ms max[A] = 32 A

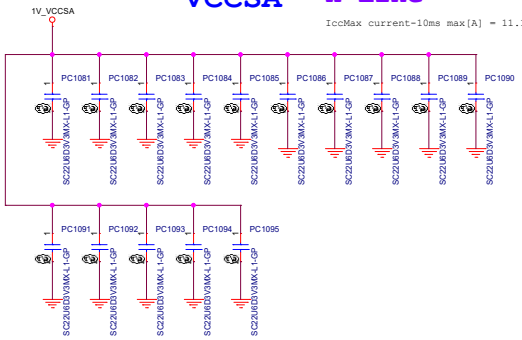
22uF 26 Pcs
DY 0 Pcs



VCCSA H-Line

22uF 15Pcs
DY 0 Pcs

IccMax current-10ms max[A] = 11.1 A



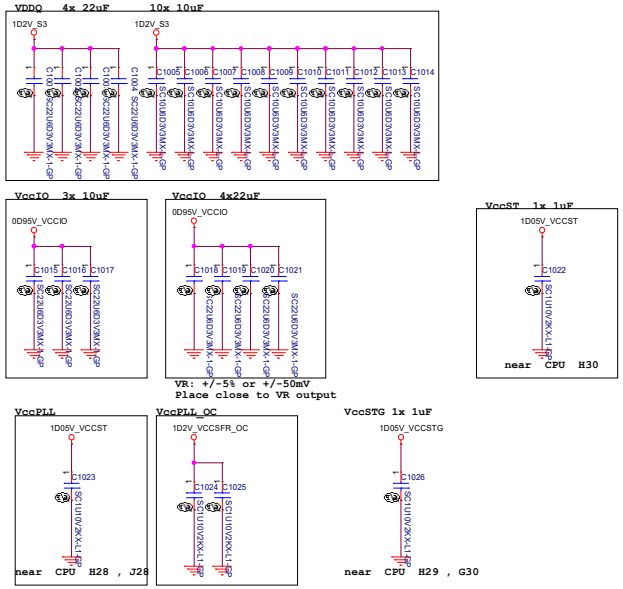


Table 49-3. Decoupling Requirements for KBL H Processor

Domain	Board Edge cap	Backside cap	Notes
V_{CC}	4: 47uF 0805		
		8: 22uF 0603	
		28: 10uF 0402	
		63: 1uF 0201	
$V_{CC_{ST}}$	6: 47uF 0805		
		8: 22uF 0603	
		25: 10uF 0402	
		68: 1uF 0201	
$V_{CC_{GFX}}$	8: 22uF 0603		Only needed when supporting 44e
		4: 10uF 0402	Only needed when supporting 44e
		12: 1uF 0201	Only needed when supporting 44e
$V_{CC_{SA}}$	1: 47uF 0805		
		1: 47uF 0805	
		7: 10uF 0402	
		3: 1uF 0201	
V_{DDQ}		4: 22uF 0603	
		10: 10uF 0402	
V_{DDQC}		1: 10uF 0402	
V_{CCIO}		3: 10uF 0402	
$V_{CC_{ST}}$		1: 1uF 0201	Do not route $V_{CC_{ST}}$ closest adjacent layer over any power net other than ground.
$V_{CC_{STG}}$		1: 1uF 0201	Share supply with 1.0V PCH rail
$V_{CC_{PLL}}$		1: 1uF 0201	Do not route $V_{CC_{PLL}}$, $V_{CC_{STG}}$ closest adjacent layer over any power net other than ground.
$V_{CC_{PLL\_OC}}$		2: 1uF 0201	Share with VDDQ. Do not route $V_{CC_{PLL\_OC}}$ closest adjacent layer over any power net other than ground.
$V_{CC_{OPC}}$		10: 10uF 0402	Only needed when supporting 44e VR: +/-5% or +/-50mV.
$V_{CC_{DFRD}}$		3: 10uF 0402	Only needed when supporting 44e VR: +/-5% or +/-50mV.

N18EG1 SAMSUNG

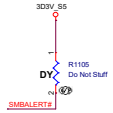
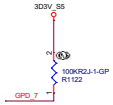
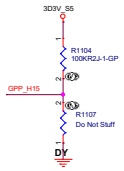
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CORE Power Cap1)

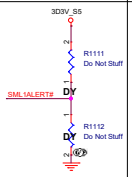
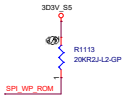
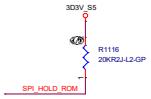
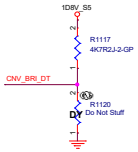
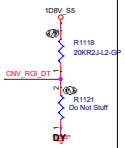
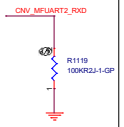
Size: Custom | Document Number: Ghibli_CFL | Rev: SC

Date: Monday, December 03, 2018 | Sheet 10 of 106

[17] SMBALERT#
[18] GPP_H15
[17] SML1ALERT#
[18,25] SPI_WP_ROM
[18,25] SPI_HOLD_ROM
[20,61] CNV_BRI_DT
[20,61] CNV_RGI_DT
[20] CNV_MFUART2_RXD
[16] GPD_7

Description	Top Swap Override	No Reboot	TLS Confidentiality	Boot BIOS	eSPI or LPC	Reserved	Reserved
GPIO	GPP_B14	GPP_B18	GPP_C2	GPP_B22	GPP_C5	GPP_D7	GPP_H15
Schematic	default is internal pull down add TP at PCH side	default is internal pull down add TP at PCH side		default is internal pull down add TP at PCH side			
High	Enable	Enable	Enable	LPC	eSPI		Enable
Low	Disable	Disable	Disable	SPI	LPC		Disable
	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down		

Signal	Usage	When Sampled	Comment
GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal Pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap . ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.
GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal Pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_C2 / SMBALERT#	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal Pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. ***Notes:*** 1. The internal Pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

Description	Intel DCI-OOB	Reserved	Reserved	Reserved	XTAL Frequency Select	CNV Mode select	VCCSPI select
GPIO	GPP_B23	SPI0_IO2	SPI0_IO3	GPP_H12	GPP_J4 CNV_BRI_DT UART0_RTS#	GPP_J6 CNV_RGI_DT UART0_TXD	GPP_J9
Schematic				GPP_H_12 add TP at PCH side			
High	Enable			Enable	24MHz	Enable	Disable
Low	Disable			Disable	38.4Hz	Disable	Enable
	internal pull-down				internal pull-down	internal pull-down	internal pull-down

Signal	Usage	When Sampled	Comment
GPP_B22 / GSPI_MOSI	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 6). **Bit 6** — **Boot BIOS Destination** 0 — SPI (Default) 1 — LPC ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.
GPP_C5 / SML0ALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** is selected (for EC). (Default) 1 = **eSPI** is selected (for EC). ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **If this strap is configured to '0' (eSPI is disabled), the *eSPI Flash Sharing Mode* strap must be configured to '0' as well (SAFS is disabled)**
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_H15 / SML3ALERT#	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_B23 / SML3ALERT# / PCHHOT#	Intel® DCI-OOB	Rising edge of RSMRST#	This signal has an internal pull-down. 0 = Disable Intel® DCI-OOB (Default) 1 = Enable Intel® DCI-OOB ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. This signal is in the primary well.
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

Signal	Usage	When Sampled	Comment
GPP_J4 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_J6 / CNV_RGI_DT / UART0_TXD	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.
GPP_J9	1.8V VCCPSPI	Rising edge of RSMRST#	The signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail 1 = VCCSPI is connected to 1.8V rail ***Note:*** If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os
GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

Signal	Usage	When Sampled	Comment
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H12 / SML3ALERT#	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **This strap must be configured to '0' (SAFS is disabled) if the *eSPI or LPC* strap is configured to '0' (eSPI is disabled)**
GPP_I6 / DDPB_C-TRLDATA	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_I8 / DDPC_C-TRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_I10 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_F23	Display Port F Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port F is not detected. (Default) 1 = Port F is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.

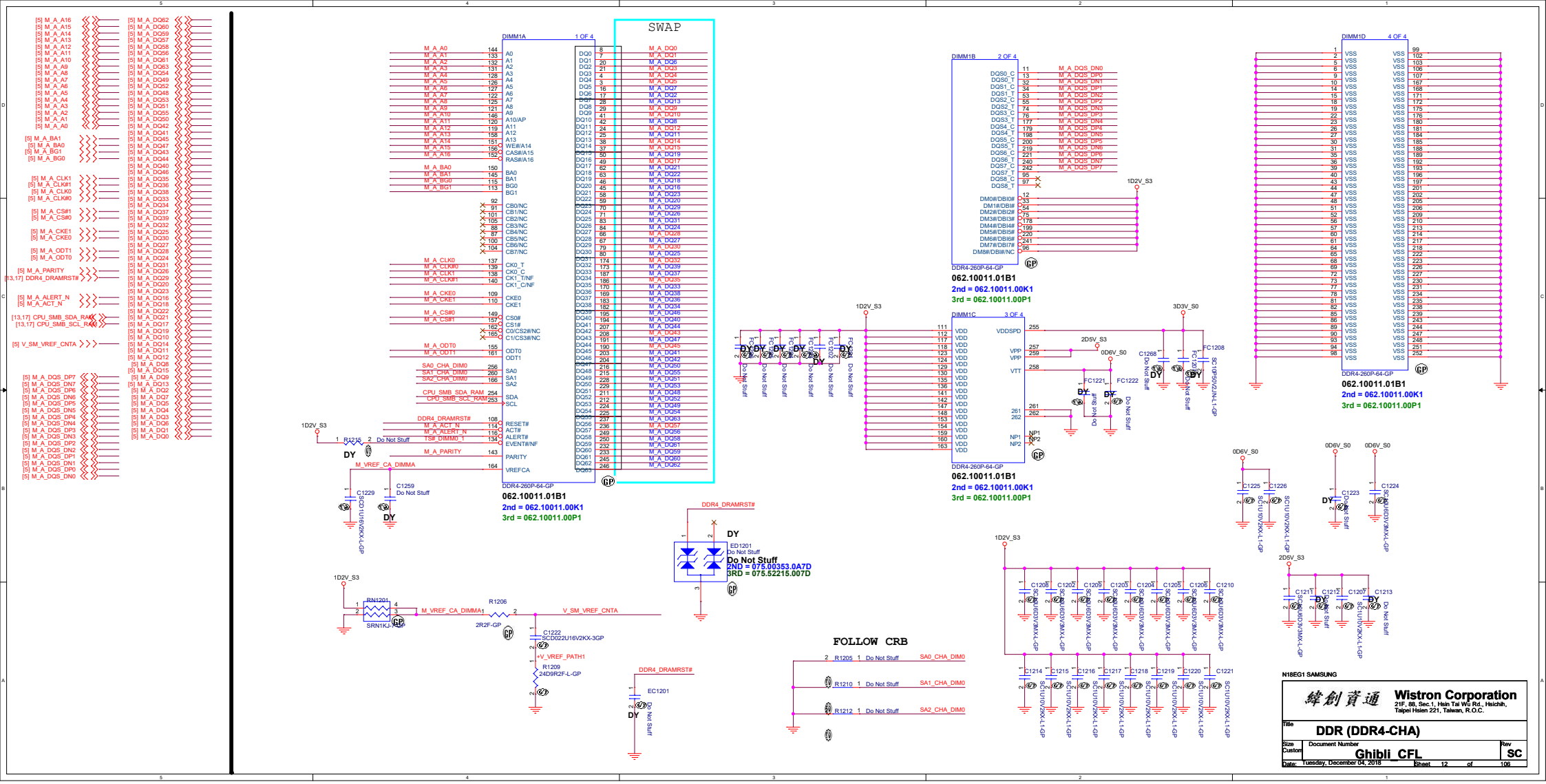
N18EG1 SAMSUNG

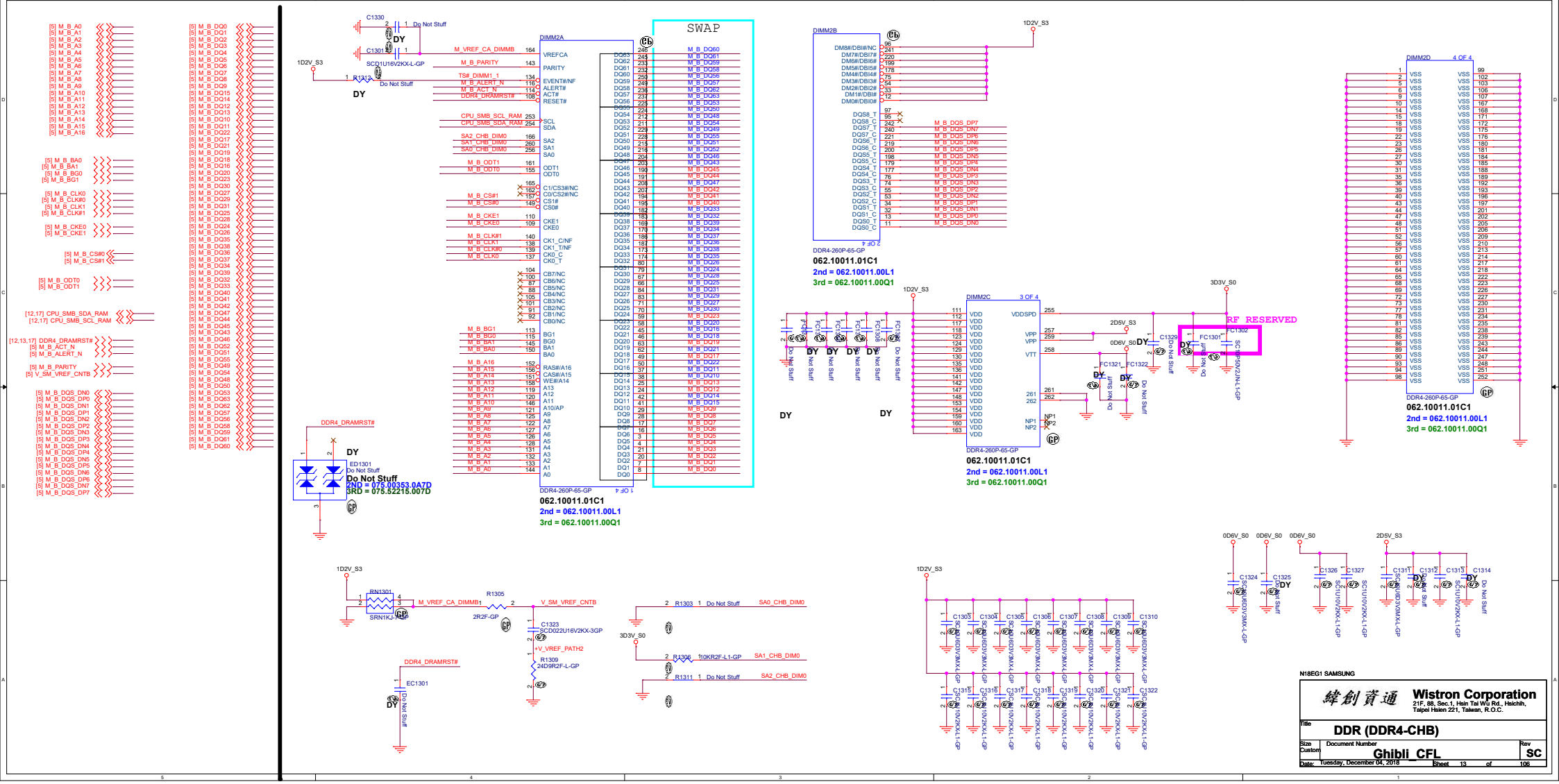
Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (STRAP)

Size	Document Number	Rev
Custom	Ghibli_CFL	SC

Date: Tuesday, December 04, 2018 Sheet 11 of 106


SWAP
DIMM1A
1 OF 4
DDR4-260P-64-GP
062.10011.01B1
2nd = 062.10011.00K1
3rd = 062.10011.00P1
DIMM1B
2 OF 4
DIMM1C
3 OF 4
DIMM1D
4 OF 4
FOLLOW CRB
Do Not Stuff
2ND = 075.00353.0A7D
3RD = 075.52215.007D
N18EG1 SAMSUNG
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR (DDR4-CHA)
Size
Custom
Document Number
Ghibli_CFL
Rev
SC
Date: Tuesday, December 04, 2018
Sheet 12 of 106


DIMM2A
DDR4-260P-65-GP
062.10011.01C1
2nd = 062.10011.00L1
3rd = 062.10011.00Q1
SWAP
DIMM2B
DIMM2C
DIMM2D
RF RESERVED
Do Not Stuff
2nd = 075.00353.0A7D
3RD = 075.52215.007D
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
N18EG1 SAMSUNG
DDR (DDR4-CHB)
Ghibli_CFL
SC
Tuesday, December 04, 2018
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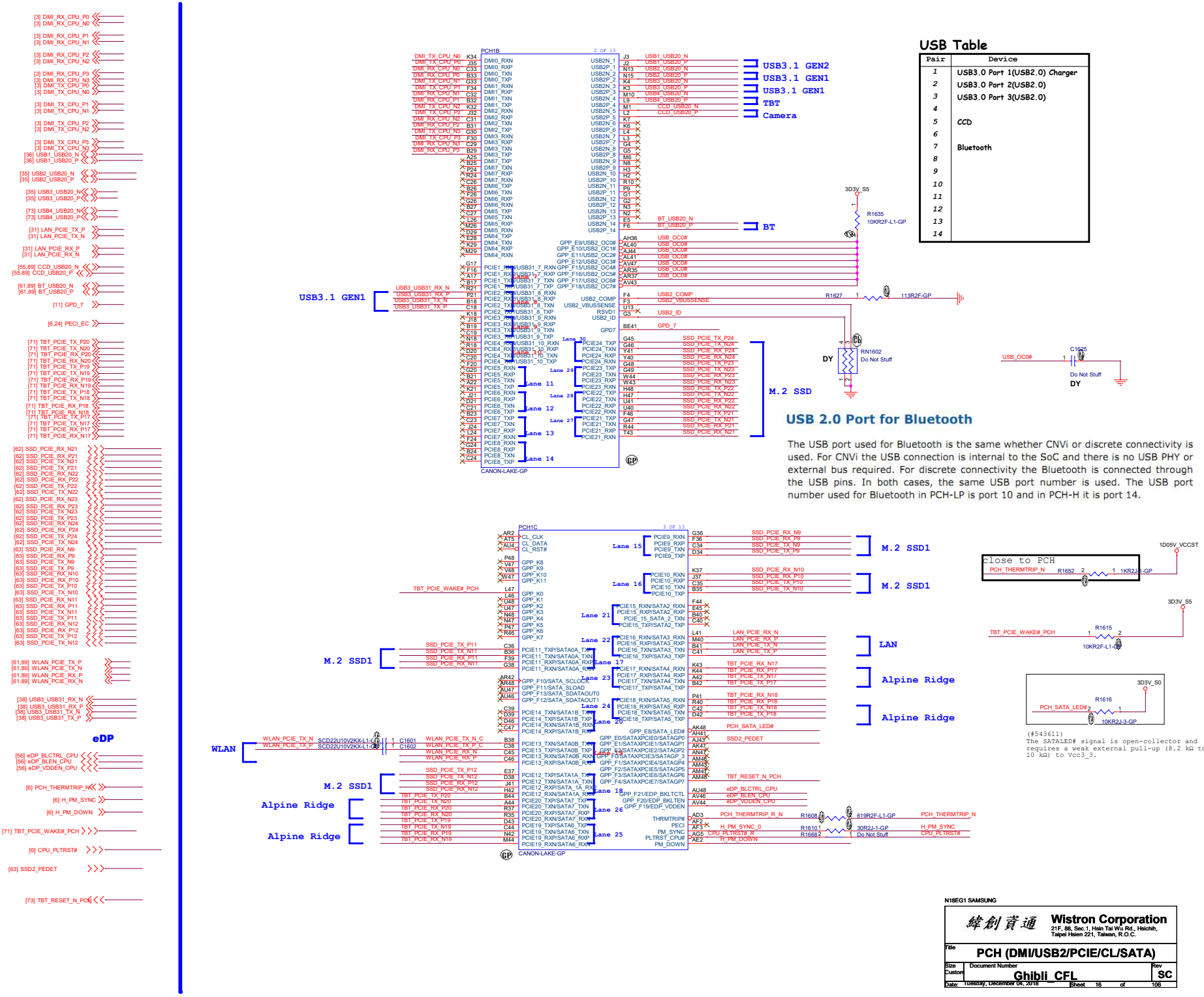
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Block Diagram	
Size A4	Document Number Ghibli_CFL	Rev SC
Date: Monday, December 03, 2018	Sheet 14 of 106	

N18EG1 SAMSUNG

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**DDR (RSVD)**
Size: Custom	Document Number: **Ghibli_CFL**
Rev	**SC**
Date: Monday, December 03, 2018	Sheet 15 of 106



USB Table

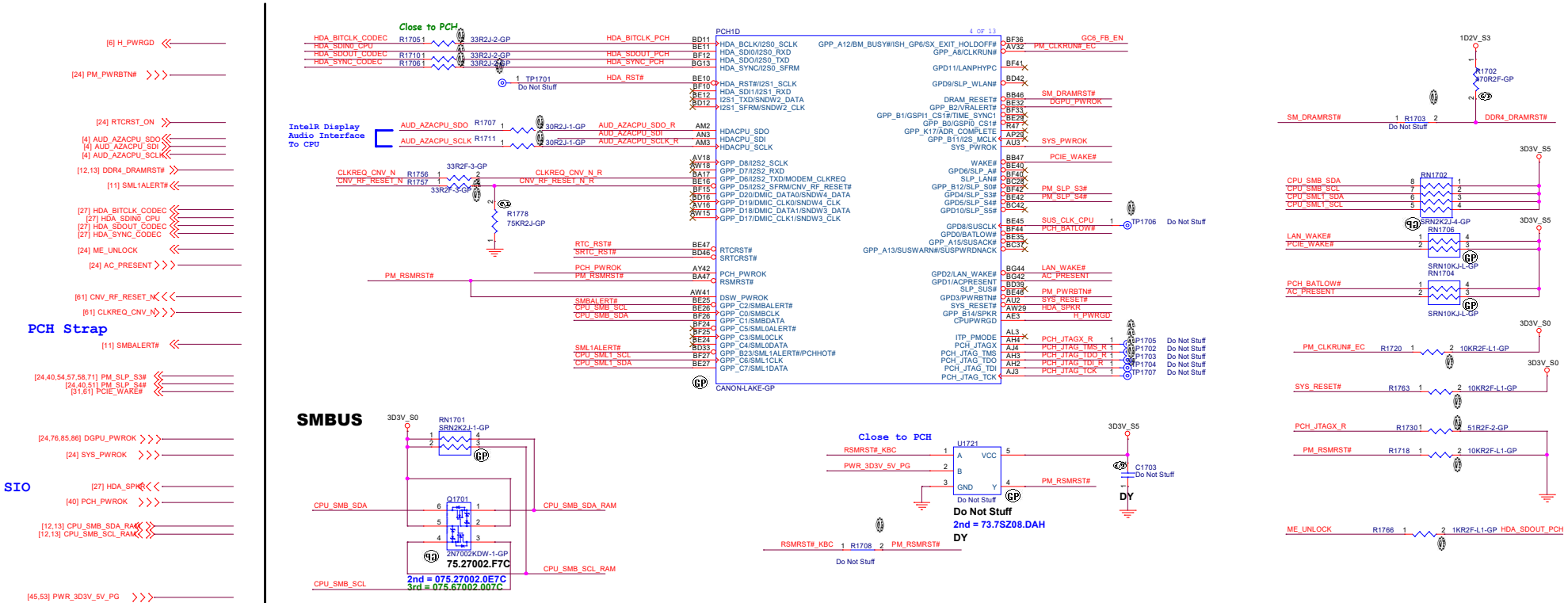
Pair	Device
1	USB3.0 Port 1(USB2.0) Charger
2	USB3.0 Port 2(USB2.0)
3	USB3.0 Port 3(USB2.0)
4	
5	CCD
6	
7	Bluetooth
8	
9	
10	
11	
12	
13	
14	

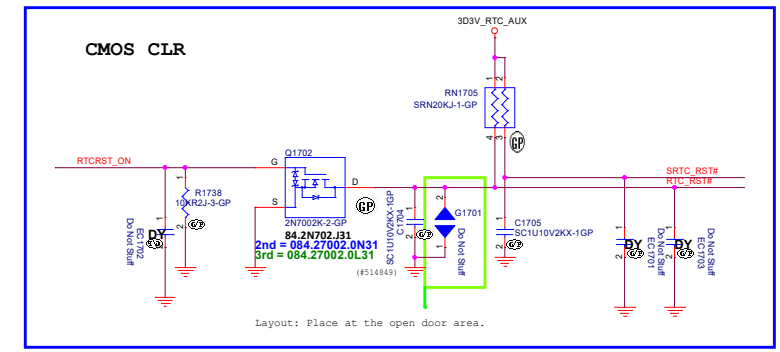
USB 2.0 Port for Bluetooth

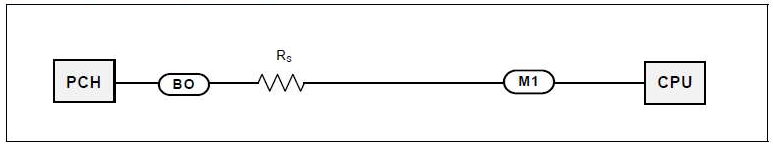
The USB port used for Bluetooth is the same whether CNVi or discrete connectivity is used. For CNVi the USB connection is internal to the SoC and there is no USB PHY or external bus required. For discrete connectivity the Bluetooth is connected through the USB pins. In both cases, the same USB port number is used. The USB port number used for Bluetooth in PCH-LP is port 10 and in PCH-H it is port 14.

N18EG1 SAMSUNG

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	PCH (DMI/USB2/PCIE/CL/SATA)
Size: Custom	Document Number: Ghibli_CFL
Rev	SC
Date: Tuesday, December 04, 2018	Sheet 16 of 106







HDACPU_SDO/HDACPU_SCLK Routing Guidelines

Parameter	Segment	Stackup	Units	Routing Recommendation
Trace Length Maximum	BI, B0	MS/SL/DSL	mils	500
Trace Length Maximum	M1	MS/SL/DSL	mils	7500
Trace Length Maximum	BO+M1	MS/SL/DSL	mils	8000
Trace Length Matching with respect to HDACPU_SCLK	NA	NA	mils	500
Resistor Value	Rs	NA	Ω	30
PCH Buffer Impedance Target	NA	NA	Ω	50

N18EG1 SAMSUNG

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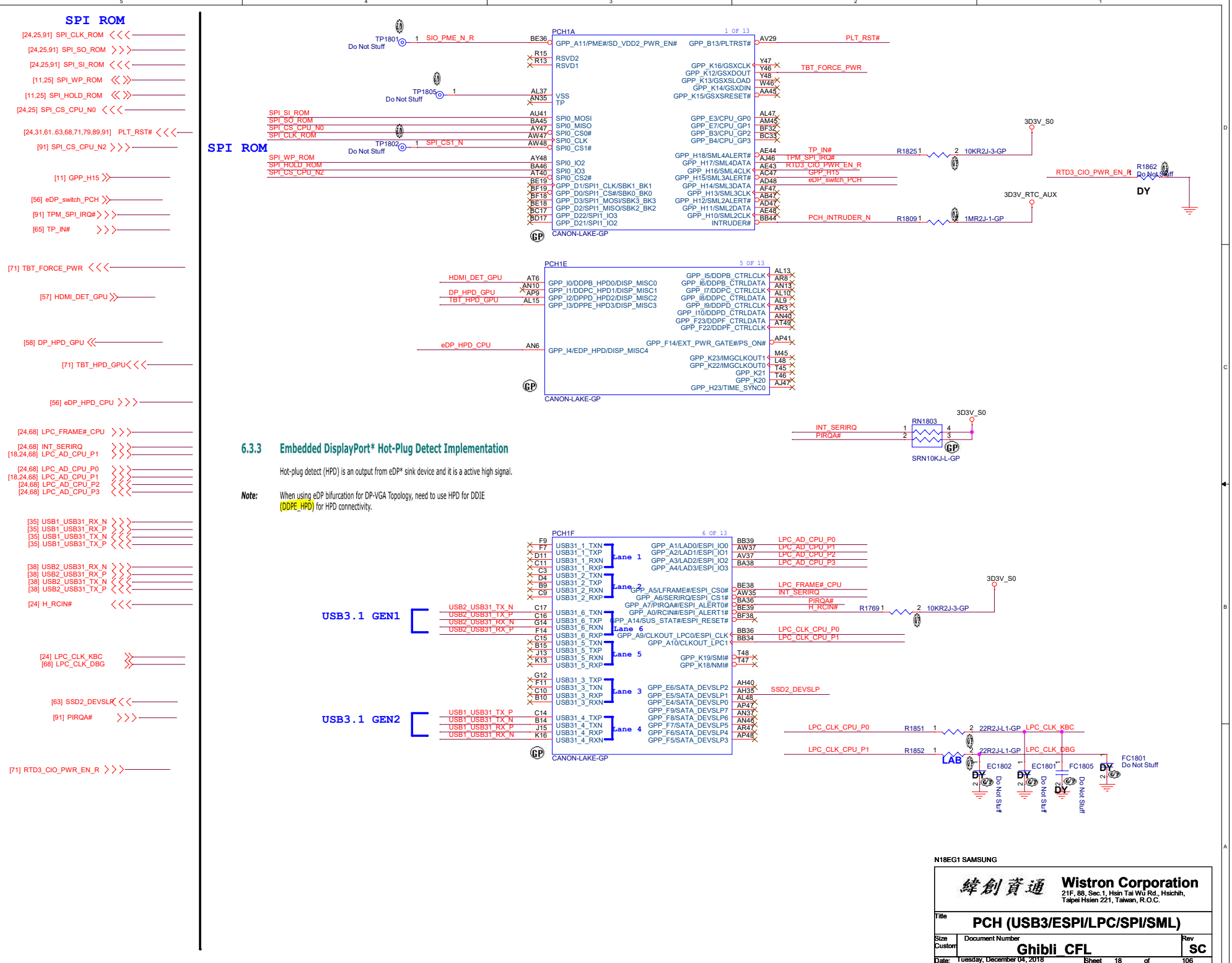
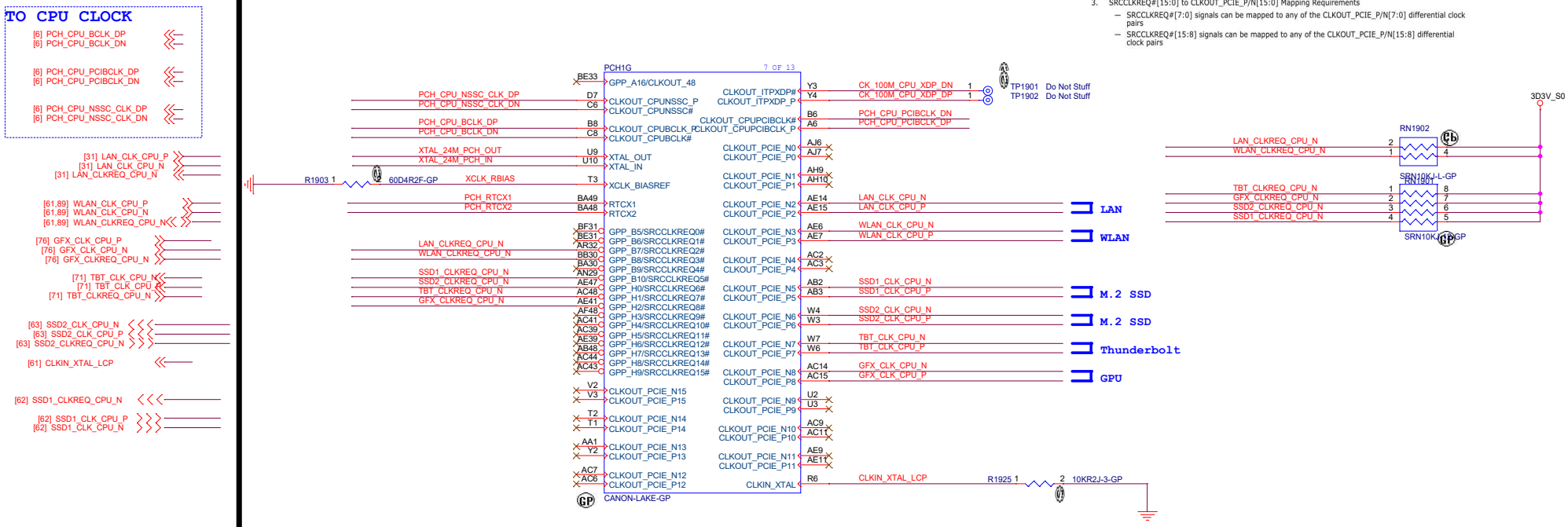
Title: PCH (HDA/SMB/PM)

Size: Custom | Document Number: Ghibli_CFL | Rev: SC

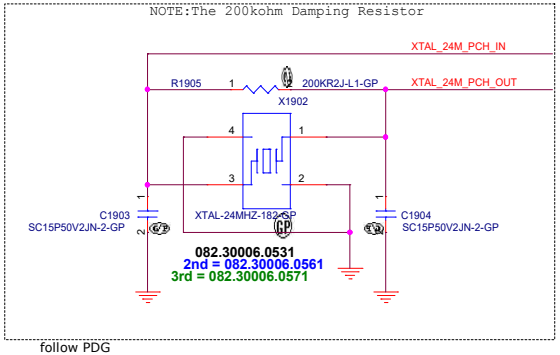
Date: Monday, December 03, 2018 | Sheet 17 of 106


SPI ROM
[24,25,91] SPI_CLK_ROM
[24,25,91] SPI_SO_ROM
[24,25,91] SPI_SI_ROM
[11,25] SPI_WP_ROM
[11,25] SPI_HOLD_ROM
[24,25] SPI_CS_CPU_N0
[24,31,61..63,68,71,79,89,91] PLT_RST#
[91] SPI_CS_CPU_N2
[11] GPP_H15
[56] eDP_switch_PCH
[91] TPM_SPI_IRQ#
[65] TP_IN#
[71] TBT_FORCE_PWR
[57] HDMI_DET_GPU
[58] DP_HPD_GPU
[71] TBT_HPD_GPU
[56] eDP_HPD_CPU
[24,68] LPC_FRAME#_CPU
[24,68] INT_SERIRQ
[18,24,68] LPC_AD_CPU_P1
[24,68] LPC_AD_CPU_P0
[18,24,68] LPC_AD_CPU_P1
[24,68] LPC_AD_CPU_P2
[24,68] LPC_AD_CPU_P3
[35] USB1_USB31_RX_N
[35] USB1_USB31_RX_P
[35] USB1_USB31_TX_N
[35] USB1_USB31_TX_P
[38] USB2_USB31_RX_N
[38] USB2_USB31_RX_P
[38] USB2_USB31_TX_N
[38] USB2_USB31_TX_P
[24] H_RCIN#
[24] LPC_CLK_KBC
[68] LPC_CLK_DBG
[63] SSD2_DEVSLP
[91] PIRQA#
[71] RTD3_CIO_PWR_EN_R
PCH1A
1 OF 13
CANON-LAKE-GP
TP1801
Do Not Stuff
SIO_PME_N_R
BE36
GPP_A11/PME#/SD_VDD2_PWR_EN#
GPP_B13/PLTRST#
AV29
PLT_RST#
R15
R13
RSVD2
RSVD1
GPP_K16/GSXCLK
GPP_K12/GSXDOUT
GPP_K13/GSXSLOAD
GPP_K14/GSXDIN
GPP_K15/GSXSRESET#
Y47
Y46
Y48
W46
AA45
TBT_FORCE_PWR
TP1805
Do Not Stuff
AL37
AN35
VSS
TP
SPI_SI_ROM
SPI_SO_ROM
SPI_CS_CPU_N0
SPI_CLK_ROM
AU41
BA45
AY47
AW47
AW48
SPI0_MOSI
SPI0_MISO
SPI0_CS0#
SPI0_CLK
SPI0_CS1#
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
AL47
AM45
BF32
BC33
TP1802
Do Not Stuff
SPI_CS1_N
SPI_WP_ROM
SPI_HOLD_ROM
SPI_CS_CPU_N2
AY48
BA46
AT40
SPI0_IO2
SPI0_IO3
SPI0_CS2#
GPP_H18/SML4ALERT#
GPP_H17/SML4DATA
GPP_H16/SML4CLK
GPP_H15/SML3ALERT#
GPP_H14/SML3DATA
GPP_H13/SML3CLK
GPP_H12/SML2ALERT#
GPP_H11/SML2DATA
GPP_H10/SML2CLK
INTRUDER#
AE44
AJ46
AE43
AC47
AD48
AF47
AB47
AD47
AE48
BB44
TP_IN#
TPM_SPI_IRQ#
RTD3_CIO_PWR_EN_R
GPP_H15
eDP_switch_PCH
PCH_INTRUDER_N
R18251
R18091
10KR2J-3-GP
1MR2J-1-GP
3D3V_S0
3D3V_RTC_AUX
R1862
Do Not Stuff
DY
BE19
BF19
BF18
BE18
BC17
BD17
GPP_D1/SPI1_CLK/SBK1_BK1
GPP_D0/SPI1_CS#/SBK0_BK0
GPP_D3/SPI1_MOSI/SBK3_BK3
GPP_D2/SPI1_MISO/SBK2_BK2
GPP_D22/SPI1_IO3
GPP_D21/SPI1_IO2
PCH1E
5 OF 13
CANON-LAKE-GP
HDMI_DET_GPU
DP_HPD_GPU
TBT_HPD_GPU
AT6
AN10
AP9
AL15
GPP_I0/DDPB_HPD0/DISP_MISC0
GPP_I1/DDPC_HPD1/DISP_MISC1
GPP_I2/DDPD_HPD2/DISP_MISC2
GPP_I3/DDPE_HPD3/DISP_MISC3
GPP_I5/DDPB_CTRLCLK
GPP_I6/DDPB_CTRLDATA
GPP_I7/DDPC_CTRLCLK
GPP_I8/DDPC_CTRLDATA
GPP_I9/DDPD_CTRLCLK
GPP_I10/DDPD_CTRLDATA
GPP_F23/DDPF_CTRLDATA
GPP_F22/DDPF_CTRLCLK
AL13
AR8
AN13
AL10
AL9
AR3
AN40
AT49
eDP_HPD_CPU
AN6
GPP_I4/EDP_HPD/DISP_MISC4
GPP_F14/EXT_PWR_GATE#/PS_ON#
AP41
GPP_K23/IMGCLKOUT1
GPP_K22/IMGCLKOUT0
GPP_K21
GPP_K20
GPP_H23/TIME_SYNC0
M45
L48
T45
T46
AJ47
INT_SERIRQ
PIRQA#
RN1803
SRN10KJ-L-GP
3D3V_S0
6.3.3 Embedded DisplayPort* Hot-Plug Detect Implementation
Hot-plug detect (HPD) is an output from eDP* sink device and it is a active high signal.
Note: When using eDP bifurcation for DP-VGA Topology, need to use HPD for DDIE (DDPE_HPD) for HPD connectivity.
PCH1F
6 OF 13
CANON-LAKE-GP
USB3.1 GEN1
USB3.1 GEN2
USB2_USB31_TX_N
USB2_USB31_TX_P
USB2_USB31_RX_N
USB2_USB31_RX_P
USB1_USB31_TX_P
USB1_USB31_TX_N
USB1_USB31_RX_P
USB1_USB31_RX_N
C17
C16
G14
F14
C14
B14
J15
K16
USB31_1_TXN
USB31_1_TXP
USB31_1_RXN
USB31_1_RXP
USB31_2_TXN
USB31_2_TXP
USB31_2_RXN
USB31_2_RXP
USB31_6_TXN
USB31_6_TXP
USB31_6_RXN
USB31_6_RXP
USB31_5_TXN
USB31_5_TXP
USB31_5_RXN
USB31_5_RXP
USB31_3_TXP
USB31_3_TXN
USB31_3_RXP
USB31_3_RXN
USB31_4_TXP
USB31_4_TXN
USB31_4_RXP
USB31_4_RXN
Lane 1
Lane 2
Lane 6
Lane 5
Lane 3
Lane 4
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS0#
GPP_A6/SERIRQ/ESPI_CS1#
GPP_A7/PIRQA#/ESPI_ALERT0#
GPP_A0/RCIN#/ESPI_ALERT1#
GPP_A14/SUS_STAT#/ESPI_RESET#
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_K19/SMI#
GPP_K18/NMI#
GPP_E6/SATA_DEVSLP2
GPP_E5/SATA_DEVSLP1
GPP_E4/SATA_DEVSLP0
GPP_F9/SATA_DEVSLP7
GPP_F8/SATA_DEVSLP6
GPP_F7/SATA_DEVSLP5
GPP_F6/SATA_DEVSLP4
GPP_F5/SATA_DEVSLP3
BB39
AW37
AV37
BA38
BE38
AW35
BA36
BE39
BF38
BB36
BB34
T48
T47
AH40
AH35
AL48
AP47
AN37
AN46
AR47
AP48
LPC_AD_CPU_P0
LPC_AD_CPU_P1
LPC_AD_CPU_P2
LPC_AD_CPU_P3
LPC_FRAME#_CPU
INT_SERIRQ
PIRQA#
H_RCIN#
LPC_CLK_CPU_P0
LPC_CLK_CPU_P1
SSD2_DEVSLP
R17691
10KR2J-3-GP
3D3V_S0
LPC_CLK_CPU_P0
LPC_CLK_CPU_P1
R1851
R1852
22R2J-L1-GP
LPC_CLK_KBC
LPC_CLK_DBG
LAB
EC1802
EC1801
FC1805
FC1801
Do Not Stuff
DY
N18EG1 SAMSUNG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (USB3/ESPI/LPC/SPI/SML)
Size Custom
Document Number
Ghibli_CFL
Rev
SC
Date: Tuesday, December 04, 2018
Sheet 18 of 106

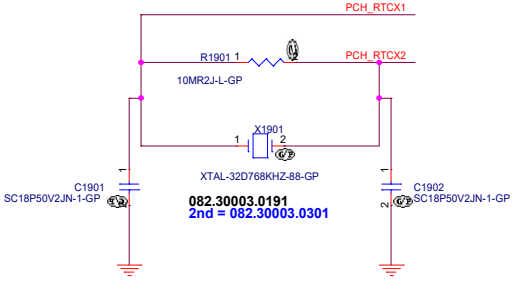
2. The SRCCLKREQ#[15:0] signals can be configured to map to any of the PCH-H PCI Express* Root Ports
3. SRCCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements
   - SRCCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs
   - SRCCLKREQ#[15:8] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:8] differential clock pairs



NOTE:The 200kohm Damping Resistor



follow PDG
Frequecy: 24MHz
Series Resistance :< 30ohm MAX
CL: 12pF



24 MHz Crystal Specifications (Sheet 1 of 2)

Parameter	Values	Units	Max/Min Range
Frequency	24	MHz	
Frequency Tolerance	≤ 100	PPM	
Duty Cycle Variation	+/- 5	%	
Pk to Pk jitter	≤ 150	pS	Includes cycle to cycle and period
Operating Temperature	-40 to 85	°C	

Parameter	Values	Units	Max/Min Range
Series Resistance	≤ 30	Ω	
Aging	±3	PPM	

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Title: PCH (CLK/RTC)

Size: Custom | Document Number: Ghibli_CFL | Rev: SC

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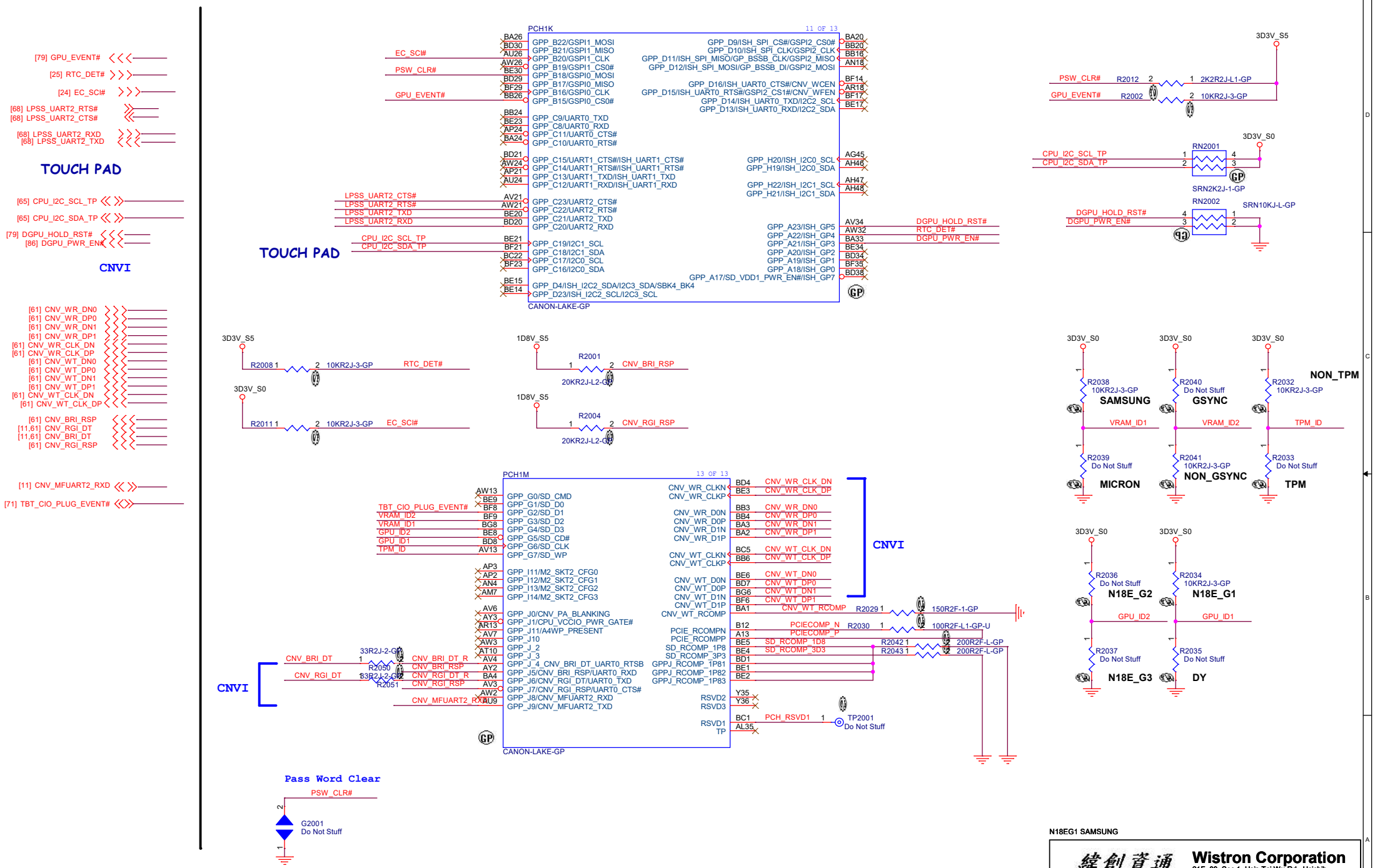

N18EG1 SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SD/CNV/GSPI/UATR/I2C/ISH)

Size: A3 | Document Number: Ghibli_CFL | Rev: SC

Date: Monday, December 03, 2018 | Sheet 20 of 106

N18EG1 SAMSUNG

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Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH (DDP/RSVD)	
Size: Custom	Document Number: Ghibli_CFL	Rev: SC
Date: Monday, December 03, 2018	Sheet 21 of 106	

VCCDPHY_1P24	**1.24V for CNVi logic**. This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC. Refer to the Platform Design Guide for implementation details.

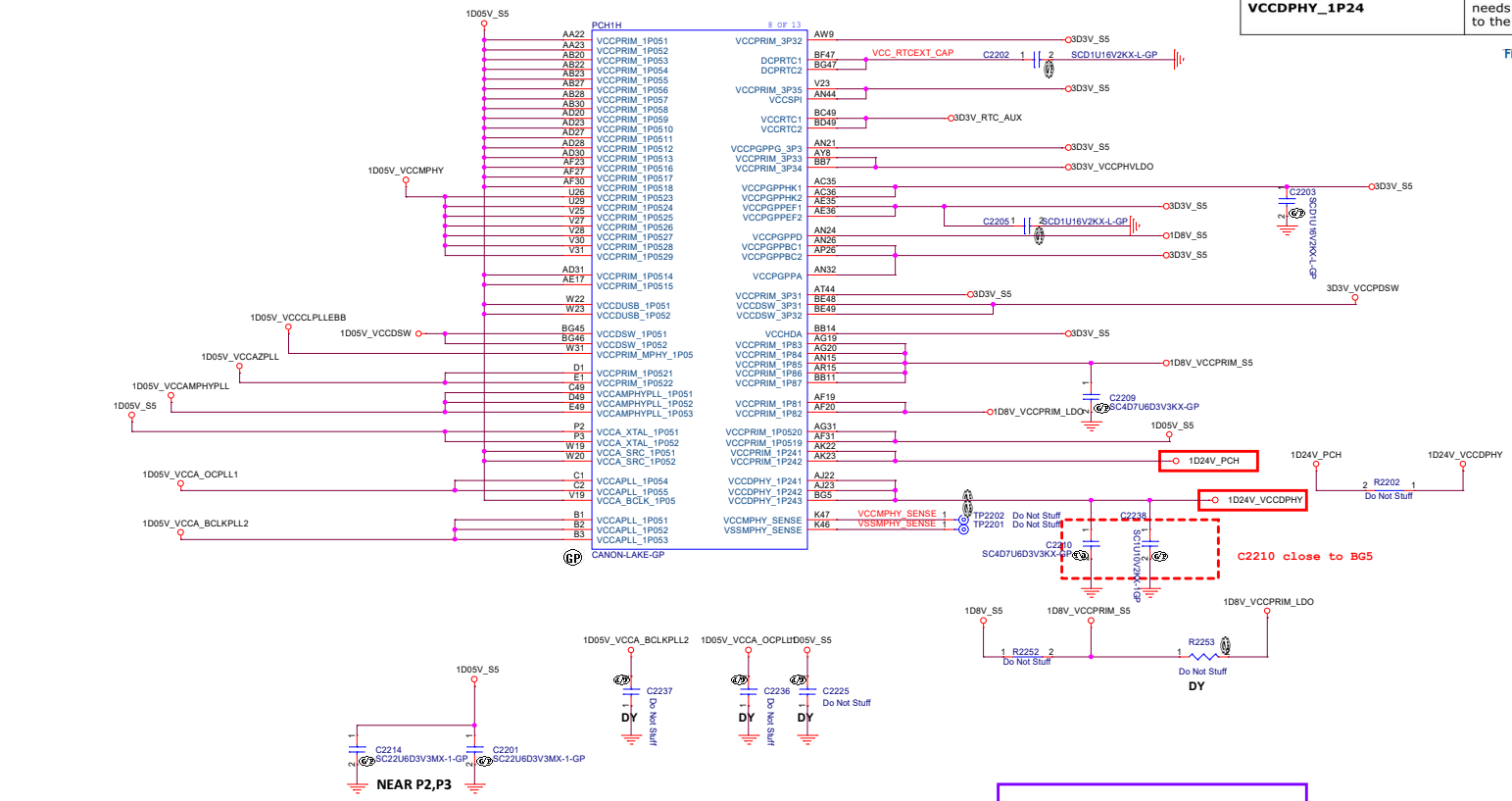
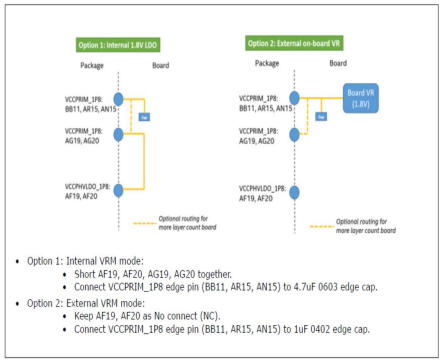
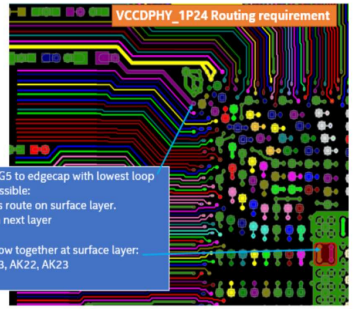


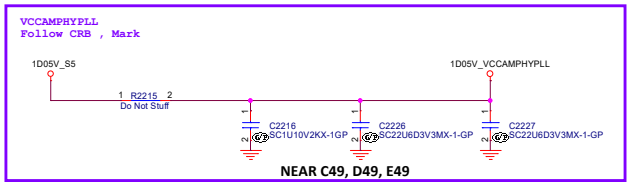
Figure 50-9. CFL PCH-H Power Rail VRM Recommendations

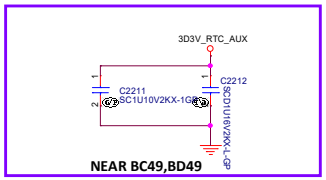


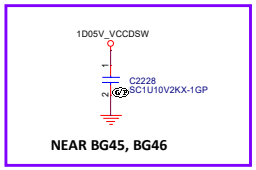
- Option 1: Internal VRM mode:
  - Short AF19, AF20, AG19, AG20 together.
  - Connect VCCPRIM_1P8 edge pin (BB11, AR15, AN15) to 4.7uF 0603 edge cap.
- Option 2: External VRM mode:
  - Keep AF19, AF20 as No connect (NC).
  - Connect VCCPRIM_1P8 edge pin (BB11, AR15, AN15) to 1uF 0402 edge cap.

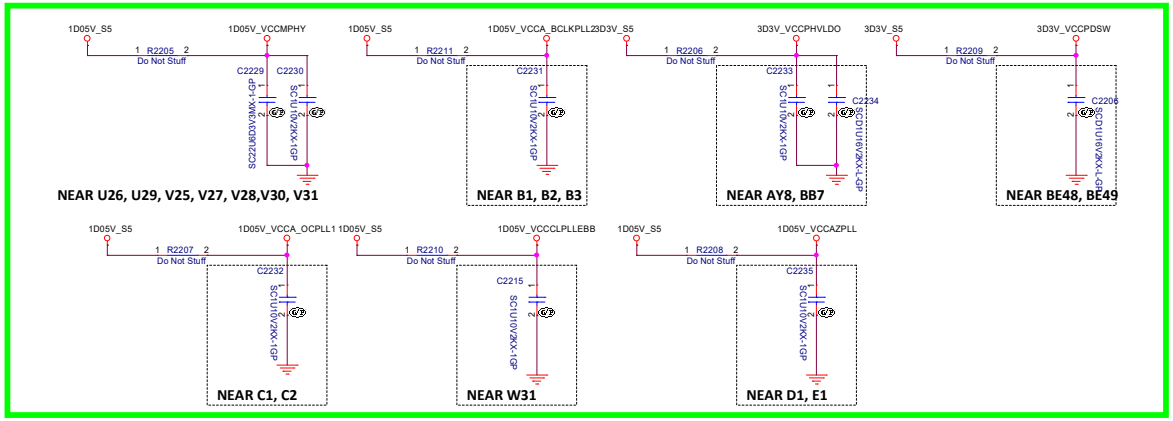
CFL PCH-H VCCDPHY_1P24 Routing











Electrical Specifications for CNVi 1.8V Signals

For using GPP_D bank signals for CNVi, the input voltage to the VCCPGPPD pin must be set to 1.8V.

The below diagrams illustrate the detailed electrical requirements for the 1.8V CNVi signals:

N18EG1 SAMSUNG

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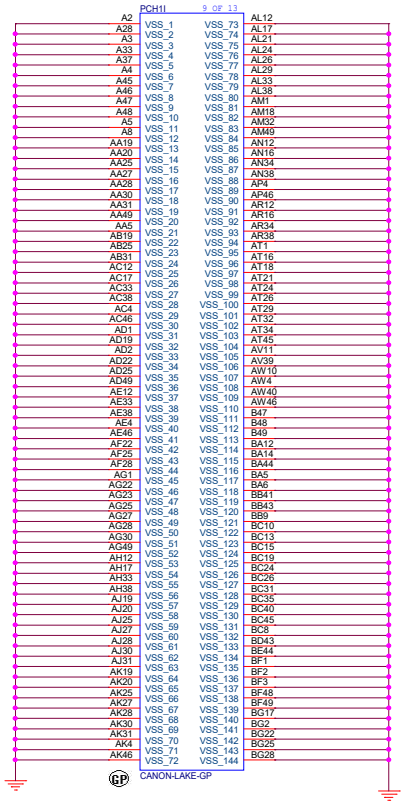
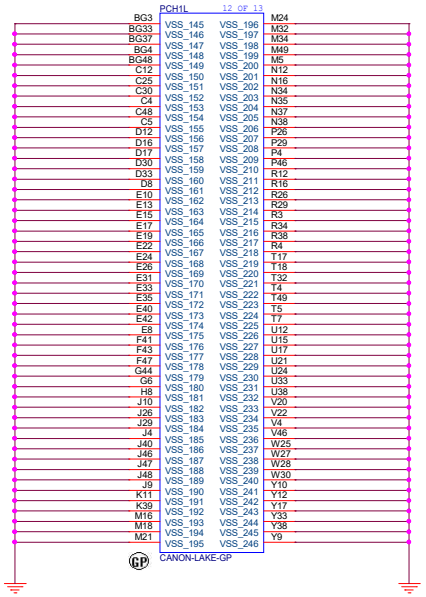
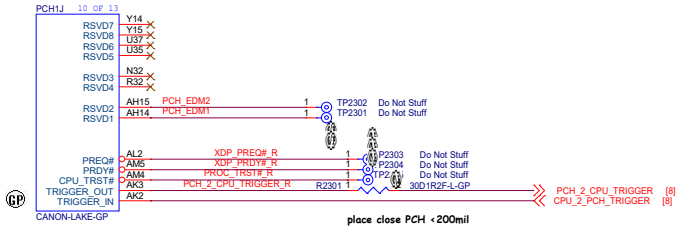
Title: PCH (POWER&Cap)		
Size: Custom	Document Number: Ghibli_CFL	Rev: SC
Date: Tuesday, December 04, 2018	Sheet 22 of 108	







place close PCH <200mil

N18EG1 SAMSUNG

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	PCH (VSS)	
Size Custom	Document Number Ghibli_CFL	Rev SC
Date: Tuesday, December 04, 2018	Sheet 23 of 106	

SSID = KBC

5 4 3 2 1

Power

3D3V_AUX_S5
3D3V_S0
3D3V_RTC_AUX

Signal

H_RCIN# [18]
FUN_OFF# [65,89]
LPC_FRAME#_CPU [18,68]
LPC_AD_CPU_P3 [18,68]
LPC_AD_CPU_P2 [18,68]
LPC_AD_CPU_P1 [18,68]
LPC_AD_CPU_P0 [18,68]
LPC_CLK_KBC [18]
PLT_RST# [18,31,61..63,68,71,79,89,91]

LID_CLOSE# [67]
PTP_PWR_EN [65]
PURE_HW_SHUTDOWN# [26,40]
PM_CLKRUN#_EC [17]
E51_TXD [61,68]

EC_TP_IN# [24,65]
KBC_BEEP [27]
FAN1_PWM [26,89]
FAN_TACH1 [26,89]

KSI0 [65,89]
KSI1 [65,89]
KSI2 [65,89]
KSI3 [65,89]
KSI4 [65,89]
KSI5 [65,89]
KSI6 [65,89]
KSI7 [65,89]
KSO0 [65,89]
KSO1 [65,89]
KSO2 [65,89]
KSO3 [65,89]
KSO4 [65,89]
KSO5 [65,89]
KSO6 [65,89]
KSO7 [65,89]
KSO8 [65,89]
KSO9 [65,89]
KSO10 [65,89]
KSO11 [65,89]
KSO12 [65,89]
KSO13 [65,89]
KSO14 [65,89]
KSO15 [65,89]
KSO16 [65,89]
KSO17 [65,89]

PWR_AC_IN# [44]

KBC_PWRBTN# [64,65,89]
BAT_IN# [43,44]

AD_IA [44]
BT_IA [44]
ALL_SYS_PWRGD [6,40]
STDBY_LED [64]
TBT_RESET_N_EC [71,73]
VD_IN2 [26]

CPU_SML1_SCL [17,65,73,79]
CPU_SML1_SDA [17,65,73,79]
BAT_SDA [43,44]
BAT_SCL [43,44]
SPI_WP_ROM [11,18,25]
FAN3_PWM [26,89]
FAN_TACH3 [26,89]
EC_TPCLK [65]
EC_TPDATA [65]
ME_UNLOCK [17]
EC_TP_IN# [24,65]

RTCRST_ON [17]
BLON_OUT [55]

VD_IN1 [26]
VD_OUT1 [26]
PROCHOT#_CPU [6,44,46]
CHARGE_LED [64]
DC_BATFULL [64]
RSMRST#_KBC [17]
AMP_MUTE# [27]
PWR_5V_EN [45]

3V_S5_ENABLE [40]

AC_PRESENT [17]
eDP_BLEN_MUX [56]
PM_PWRBTN# [17]

INT_SERIRQ [18,68]
EC_SCI# [20,24]

3.3V
PM_SLP_S3# [17,40,54,57,58,71]
PM_SLP_S4# [17,40,51]

LPC BUS=>3.3V
SPI BUS=>3.3V/1.8V (VCC_IO2 PIN:124
OPTION)

TURBO_KEY [64,89]
TURBO_LED [64,89]

TURBO

USB_CHAR_SEL [36]
USB_CHAR_CT1 [36]
USB_CHARGER_EN [36]

Charger

WIFI_RF_EN [61,89]
BLUETOOTH_EN [61,89]
USB_PWR_EN [35]
PWR_CHG_ON# [44]
PECI_EC [6,16]
DGPUHOT [79]
DGPU_PWROK [17,76,85,86]
EC_SCI# [20,24]
eDP_switch_EC [56]

TYPE_C_INT_EC [73]
SYS_PWROK [17]
POWER_LED [64]
SPI_SO_ROM [18,25,91]
SPI_SI_ROM [18,25,91]
SPI_CLK_ROM [18,25,91]
SPI_CS_CPU_N0 [18,25]

[26,89] FAN2_PWM
[26,89] FAN_TACH2
[36] USB_CHAR_CT2
[55] OD
[80,85] PFM_EN_R

Close to the EC

PLT_RST#
R2460 47KR2J-2-GP

RN2412 PWR_5V_EN, 3V_S5_ENABLE, FUN_OFF#
SRN10KJ-7-GP
RN2415 FAN_TACH2, FAN_TACH1
SRN10KJ-7-GP
RN2416 FAN_TACH3, TURBO_KEY
SRN10KJ-7-GP
RN2413 BAT_IN#, PWR_CHG_ON#
SRN100KJ-6-GP
R2468 10KR2J-3-GP LID_CLOSE#

3D3V_S0
3D3V_AUX_KBC
3D3V_AUX_S5

For EC power consumption reserver

3D3V_AUX_KBC — R2406 2 — 3D3V_AUX_S5
Do Not Stuff

VCC_LPC(Pin9)

3D3V_AUX_KBC
R2435 Do Not Stuff
3D3V_VCC_LPC

U2401

LPC_CLK_KBC
LPC_FRAME#_CPU
LPC_AD_CPU_P0
LPC_AD_CPU_P1
LPC_AD_CPU_P2
LPC_AD_CPU_P3
INT_SERIRQ
H_RCIN#
PLT_RST#
ECSCI#_KBC
PM_CLKRUN#_EC
ECRST#

KBC_BEEP
FAN3_PWM
DC_BATFULL

FAN1_PWM
FAN2_PWM
FAN_TACH1
FAN_TACH2

KSO0
KSO1
KSO2
KSO3
KSO4
KSO5
KSO6
KSO7
KSO8
KSO9
KSO10
KSO11
KSO12
KSO13
KSO14
KSO15
KSO16
KSO17
KSI0
KSI1
KSI2
KSI3
KSI4
KSI5
KSI6
KSI7

CPU_SML1_SDA
CPU_SML1_SCL
BAT_SDA
BAT_SCL

DGPU_PWROK

EC_TPCLK
EC_TPDATA

PWR_5V_EN
PWR_CHG_ON#

LID_CLOSE#
TYPE_C_INT_EC

STDBY_LED

E51_TXD
TURBO_KEY
TURBO_LED
CHARGE_LED
WIFI_RF_EN

PCICLK
LFRAME#
LAD0
LAD1
LAD2
LAD3
SERIRQ
GA20
KBRST#
PCIRST#
SCI#
CLKRUN#
ECRST#
PWM0
PWM1
PWM2
FANPWM0
FANPWM1
FANFB0
FANFB1
KSO0
KSO1
KSO2
KSO3
KSO4
KSO5
KSO6
KSO7
KSO8
KSO9
KSO10
KSO11
KSO12
KSO13
KSO14
KSO15
KSO16
KSO17
KSI0
KSI1
KSI2
KSI3
KSI4
KSI5
KSI6
KSI7
SDA0
SCL0
SDA1
SCL1
PSCLK1
PSDAT1
PSCLK2
PSDAT2
PSCLK3
PSDAT3
GPIO0B
GPIO0C
GPIO0A
GPIO0D
GPIO19
GPIO16
GPIO17
GPIO52
GPIO54
GPIO56

3.3V
3.3V
3.3V

VCC
VCC
VCC
VCC0
VCC
VCC_LPC
AVCC
GND
GND
GND
GND
GND
AGND
VCC_IO2
DA0
DA1
DA2
DA3
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
GPXIOA00
GPXIOA01
GPXIOA02
GPXIOA03
GPXIOA04
GPXIOA05
GPXIOA06
GPXIOA07
GPXIOA08
GPXIOA09
GPXIOA10
GPXIOA11
GPXIOD00
AC_IN#
EC_EN#
PWRBTN#
GPXIOD04
GPXIOD05
GPIOD06
PECI
GPIO1A
GPIO53
GPIO55
GPIO5D
GPIO5E
GPIO59
GPIO57
GPIO50
GPIO18
GPIO08
GPIO07
GPIO04
SPICS#
MOSI
MISO
SPICLK

3.3V
3.3V
3.3V
3.3V
3.3V

KB9028Q-C-GP

071.09028.000G

3D3V_AUX_KBC
3D3V_RTC_AUX
3D3V_VCC_LPC
EC_AGND
AMP_MUTE#
DGPUHOT
PM_SLP_S4#
OD
AD_IA
PLS_ID
AUT_TYPE_AD
EC_TP_IN#
BT_IA
MODEL_ID_AD
FAN_TACH3
USB_CHARGER_EN
BLON_OUT
3V_S5_ENABLE
FUN_OFF#
VD_IN2
RSMRST#_KBC
VD_OUT1
USB_PWR_EN
SYS_PWROK
RTCRST_ON
TBT_RESET_N_EC
VD_IN1
PWR_AC_IN#
USB_CHRG_SEL
KBC_PWRBTN#_R
ALL_SYS_PWRGD
USB_CHAR_CT1
ME_UNLOCK
PECI_EC
eDP_switch_EC
BAT_IN#
POWER_LED
eDP_BLEN_MUX
PM_PWRBTN#
USB_CHAR_CT2
AC_PRESENT
PFM_EN_R
PTP_PWR_EN
PROCHOT_EC
BLUETOOTH_EN
PM_SLP_S3#
SPI_CS_KBC_N0 — R2412 1 — 2 Do Not Stuff — SPI_CS_CPU_N0
SPI_SI_KBC — R2407 1 — 2 Do Not Stuff — SPI_SI_ROM
SPI_SO_KBC — R2418 1 — 2 Do Not Stuff — SPI_SO_ROM
SPI_CLK_KBC — R2411 1 — 2 Do Not Stuff — SPI_CLK_ROM

3D3V_AUX_KBC
3D3V_AUX_KBC_AVCC
L2407 BLM15AG121SN-1GP
68.00084.921
2nd = 68.00217.401
C2421 C2424 C2425 C2426 C2420 C2416 SCD1U16V2KX-L-GP
C2422 C2427 SCD1U16V2KX-L-GP
C2429 SCD1U16V2KX-L-GP
L2401 BLM15AG121SN-1GP
68.00084.921
2nd = 68.00217.401
EC_AGND

SYS_PWROK(S0_PWR_GOOD) ==DELAY 99ms

EC_SCI# — R2465 1 — 2 — ECSCI#_KBC
Do Not Stuff

GPU/KB_BL/TBT/PCH/DP --->
BATTER /CHARGER --->
KB_BL --->
Touch Pad --->

3D3V_AUX_S5
R2441 330KR2J-L-GP
KBC_PWRBTN# — R2444 1 — 2 — KBC_PWRBTN#_R
470R2F-GP
G2402 Do Not Stuff

ECRST#
RN2407 SRN10KJ-7-GP
PURE_HW_SHUTDOWN# — ECRST#_Q — 3D3V_AUX_S5
MMBT3906-3-GP Q2403
C2428 SC1U10V2KX-L1-GP
84.03906.R11
2nd = 84.T3906.E11

3D3V_AUX_KBC
ECRST# — DY — R2451 1 — 2 Do Not Stuff

close RN2407

PURE_HW_SHUTDOWN#
ED2401 Do Not Stuff
DY

GPIO0 High Active

PROCHOT_EC — R2408 100KR2F-L3-GP
C2430 SC100D50V2KX-GP
Q2404 2N7002K-2-GP
PROCHOT#_CPU
84.2N702.J31
2nd = 084.27002.0N31
3rd = 084.27002.0L31

3D3V_AUX_KBC
Model_ID — R2434 33KR2F-2-GP
MODEL_ID_AD
Model_ID — R2455 100KR2J-4-GP
EC_AGND

PCB_ID	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Seting	
N18E_G3	100K	10K	3V	3.005V	>-2.875V	
N18E_G2	100K	20K	2.75V	2.759V	>-2.616V	<2.875V
N18E_G1	100K	33K	2.431V	2.493V	>-2.363V	<2.616V
RSVD	100K	47K	2.245V	2.259V	>-2.123V	<2.363V
RSVD	100K	64.9K	2.001V	2.017V	>-1.934V	<2.123V
RSVD	100K	76.8K	1.867V	1.883V	>-1.758V	<1.934V
RSVD	100K	100K	1.650V	1.667V	>-1.504V	<1.758V

3D3V_AUX_KBC
R2428 33KR2F-2-GP
PCB_ID
R2427 100KR2F-L3-GP
EC_AGND

PCB_ID_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Seting	
65W	10.0 K	10.0 K	3.000 V	3.005 V	>= 2.875 V	
56W	10.0 K	20.0 K	2.759 V	2.759 V	>= 2.616 V	<2.875 V
45W	10.0 K	33.0 K	2.493 V	2.493 V	>= 2.363 V	<2.616 V
120W	20.0 K	47.0 K	2.245 V	2.259 V	>= 2.123 V	<2.363 V
135W	20.0 K	64.9 K	2.017 V	2.017 V	>= 1.934 V	<2.123 V
150W	20.0 K	76.8 K	1.883 V	1.883 V	>= 1.758 V	<1.934 V
Reserved	20.0 K	100.0 K	1.667 V	1.667 V	>= 1.504 V	<1.758 V
Reserved	100.0 K	10.0 K	1.250 V	1.274 V	>= 1.201 V	<1.504 V
Reserved	100.0 K	20.0 K	1.000 V	1.025 V	>= 0.926 V	<1.201 V
Reserved	100.0 K	33.0 K	0.750 V	0.775 V	>= 0.676 V	<1.000 V
Reserved	100.0 K	47.0 K	0.500 V	0.525 V	>= 0.426 V	<0.750 V
Reserved	100.0 K	64.9 K	0.250 V	0.275 V	>= 0.176 V	<0.500 V
Reserved	100.0 K	76.8 K	0.000 V	0.025 V	>= 0.000 V	<0.250 V

3D3V_AUX_KBC
R2425 Do Not Stuff
ADT_TYPE_AD
DY
R2430 Do Not Stuff
EC_AGND

N18EG1 SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

ECIO (KBC KB9028)

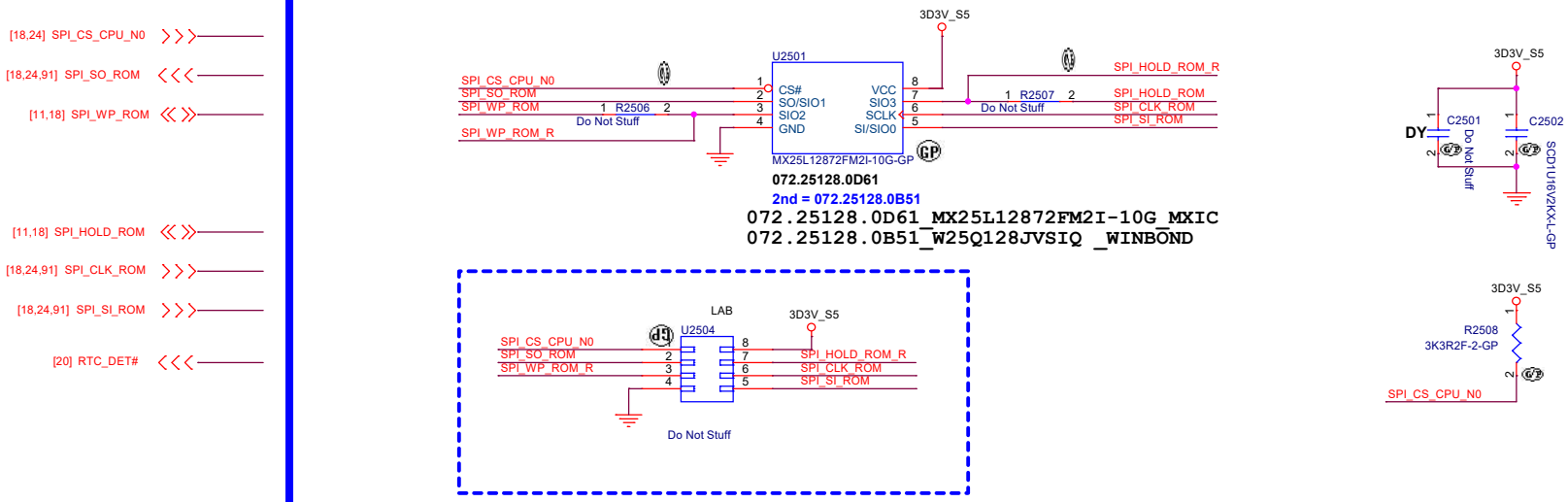
Size: Custom | Document Number: Ghibli_CFL | Rev: SC

Date: Tuesday, December 04, 2018 | Sheet 24 of 106

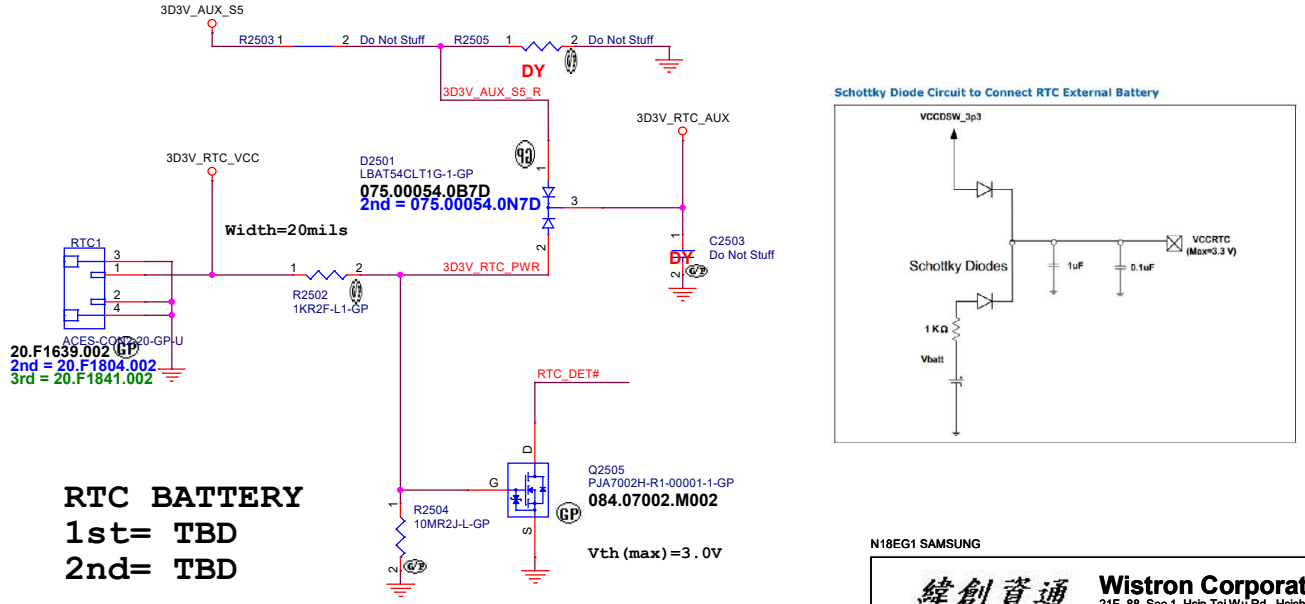
Main Func = SPI Flash

SPI FLASH ROM (16M byte) for PCH

SPI ROM Equal length need to less than 500mil



Main Func = RTC



RTC BATTERY
1st= TBD
2nd= TBD

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緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Flash/RTC	
Size Custom	Document Number Ghibli_CFL	Rev SC
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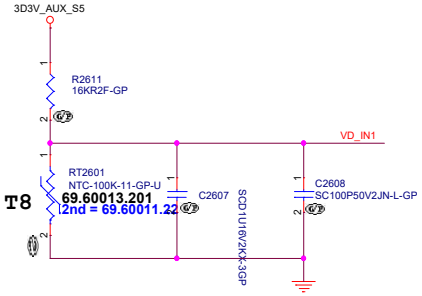
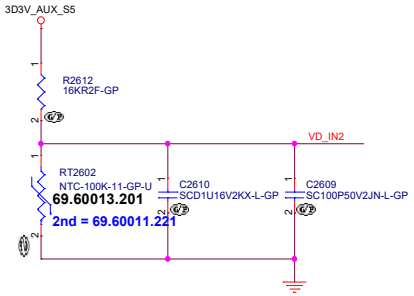
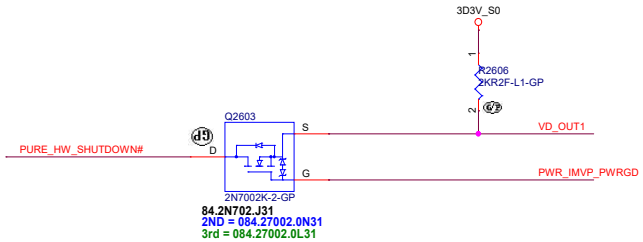
[24] VD_IN2
[24] VD_IN1
[24,26,89] FAN1_PWM
[24,89] FAN_TACH1
[24,89] FAN2_PWM
[24,89] FAN_TACH2
[24,89] FAN3_PWM
[24,89] FAN_TACH3
[24,40] PURE_HW_SHUTDOWN#
[24] VD_OUT1
[40,46] PWR_IMVP_PWRGD
[24,26,89] FAN1_PWM

SSID = Thermal



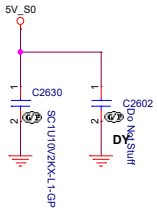


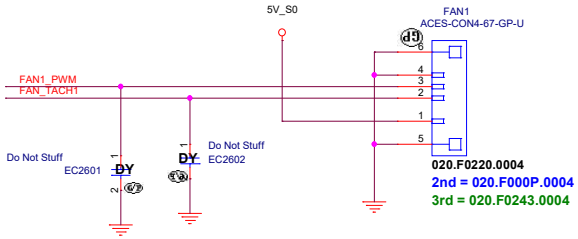


RT2601 close CPU and Vcore chock

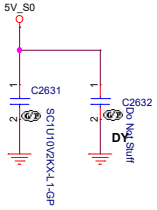
VD_IN1 trace 10 mli

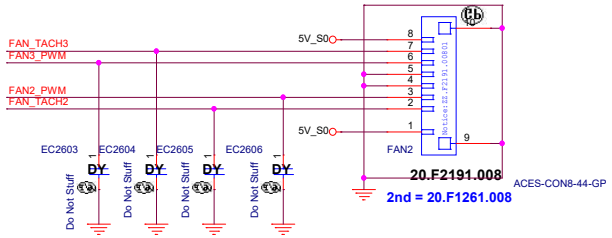
Layout 15 mil





Layout 15 mil





N18EG1 SAMSUNG

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**INT IO (Thermal/Fan)**	
Size: Custom	Document Number: **Ghibli_CFL**	Rev: **SC**
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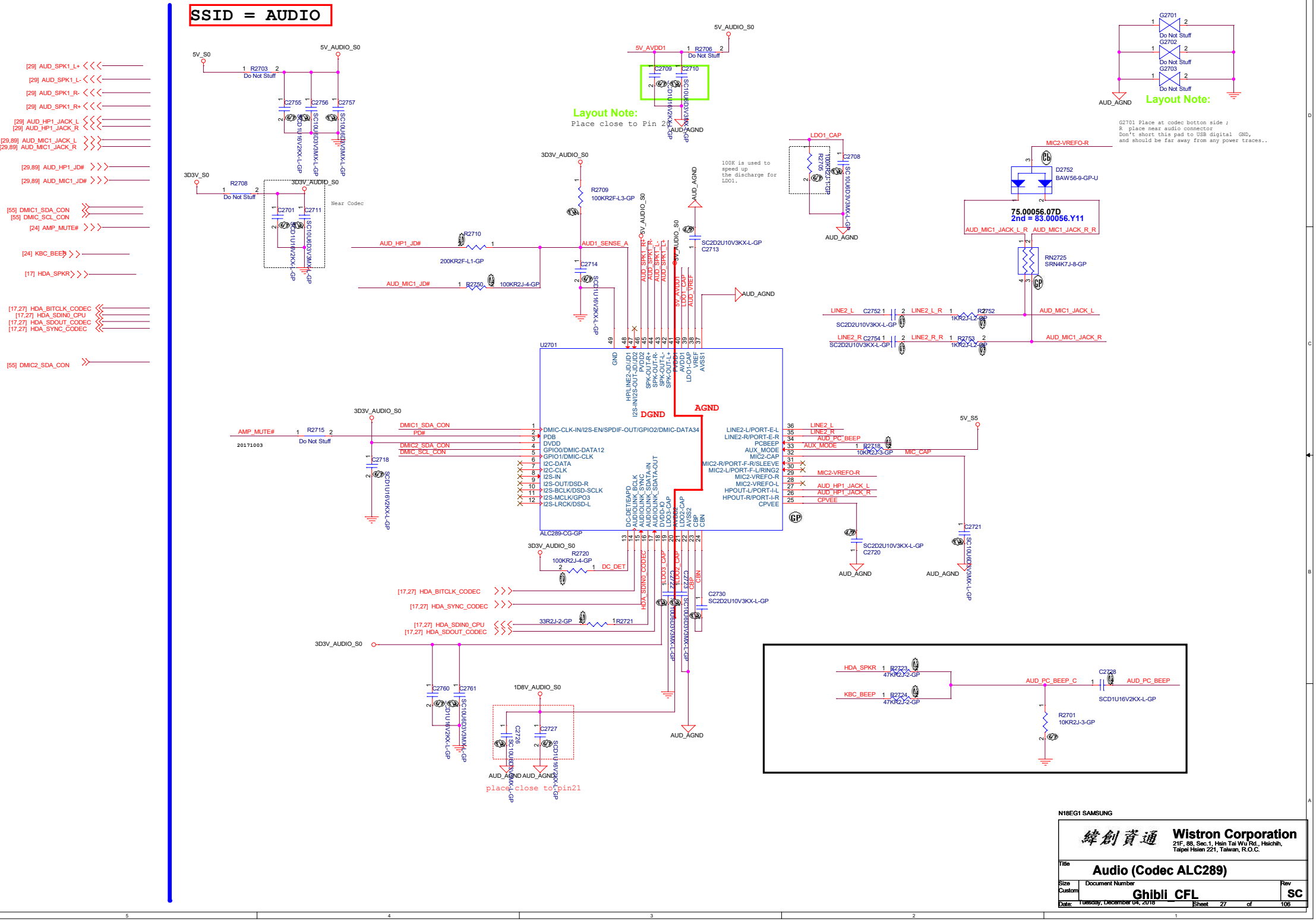
SSID = AUDIO



N18EG1 SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio (Codec ALC289)**

Size	Document Number	Rev
Custom	Ghibli_CFL	SC

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N18EG1 SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Audio (RSVD)	
Size A4	Document Number Ghibli_CFL	Rev SC
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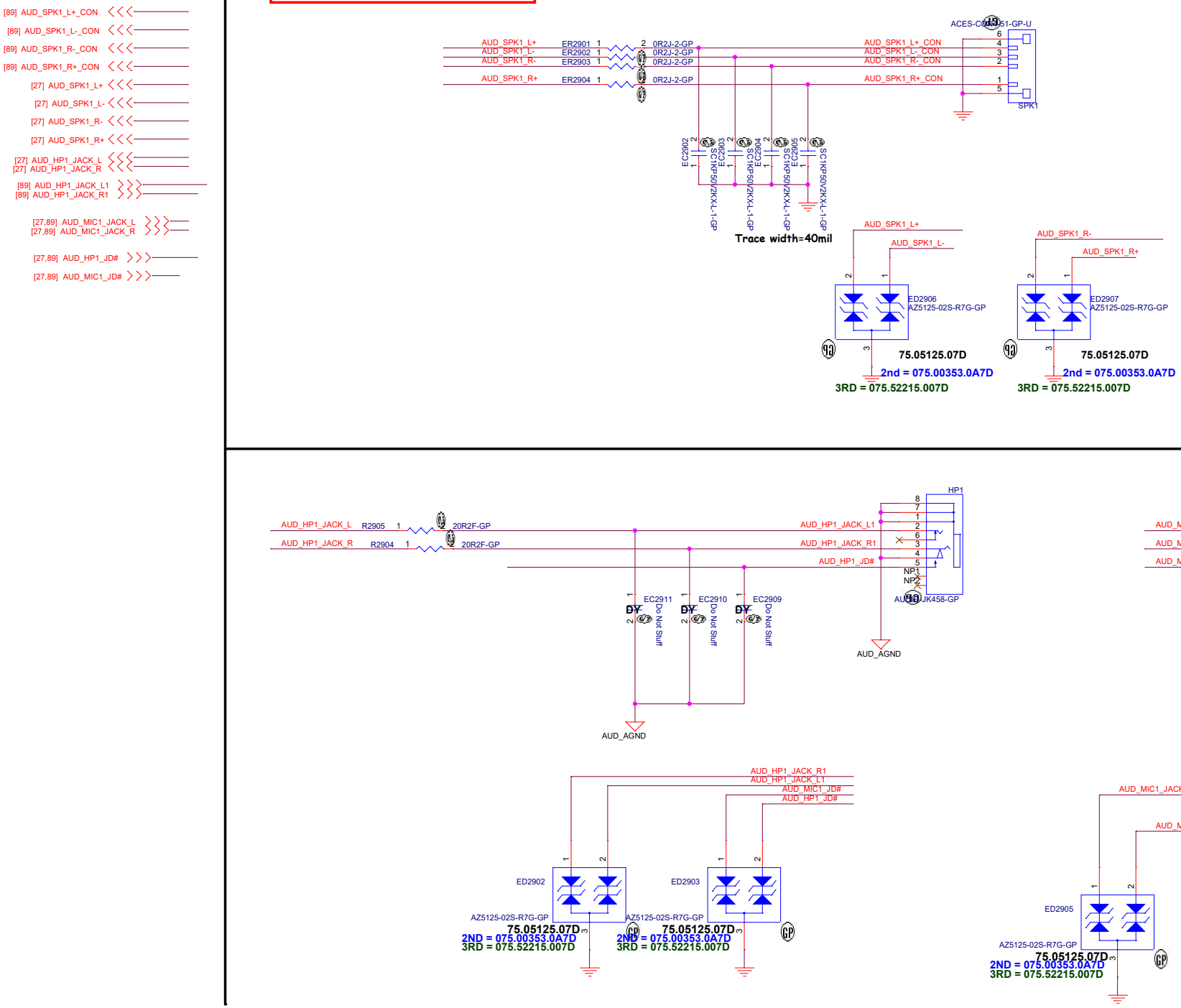
Main Func = Audio



N18EG1 SAMSUNG

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	Audio (HP/SPK/MIC Jack)		
Size Custom	Document Number Ghibli_CFL		Rev SC
Date: Tuesday, December 04, 2018	Sheet 29 of 106		

N18EG1 SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**Audio (RSVD)**	
Size A	Document Number **Ghibli_CFL**	Rev **SC**
Date: Monday, December 03, 2018	Sheet 30 of 106	

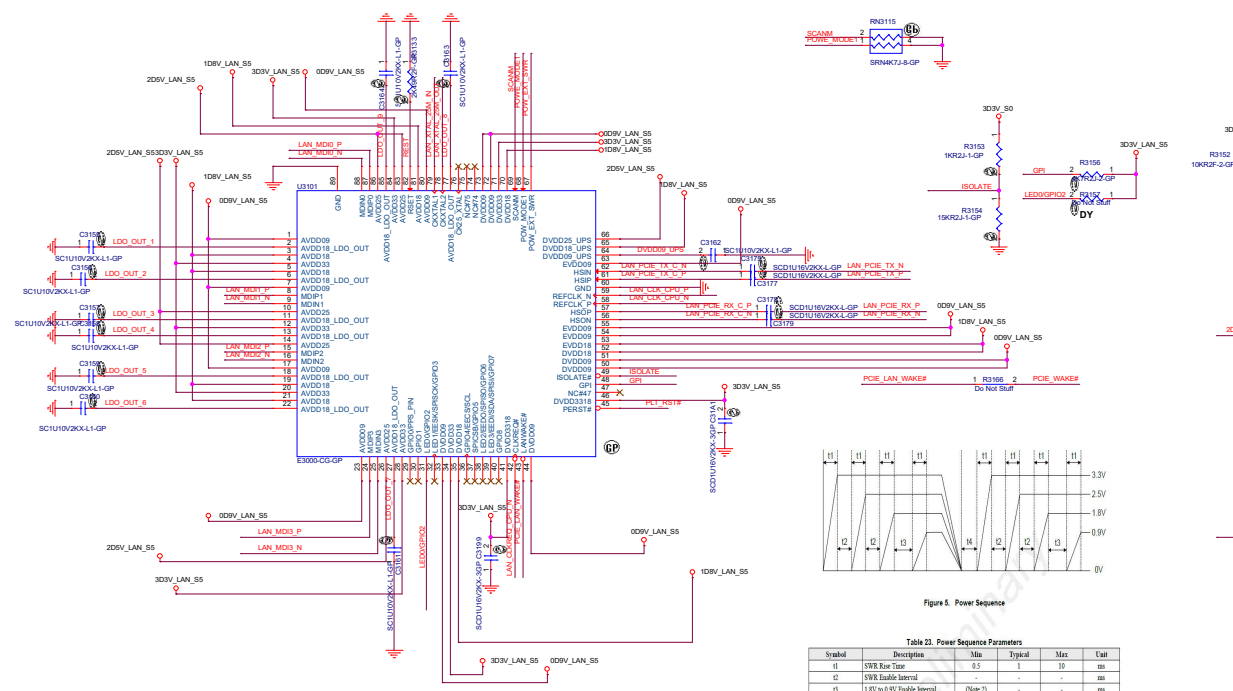
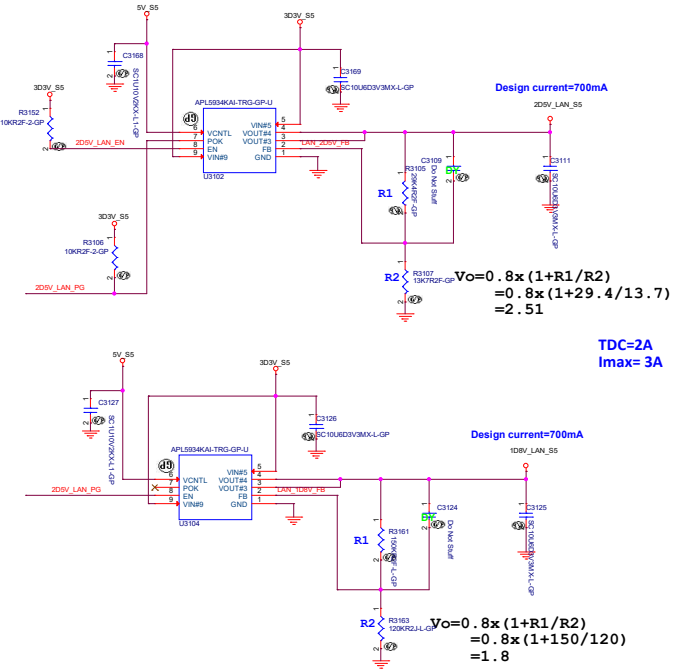


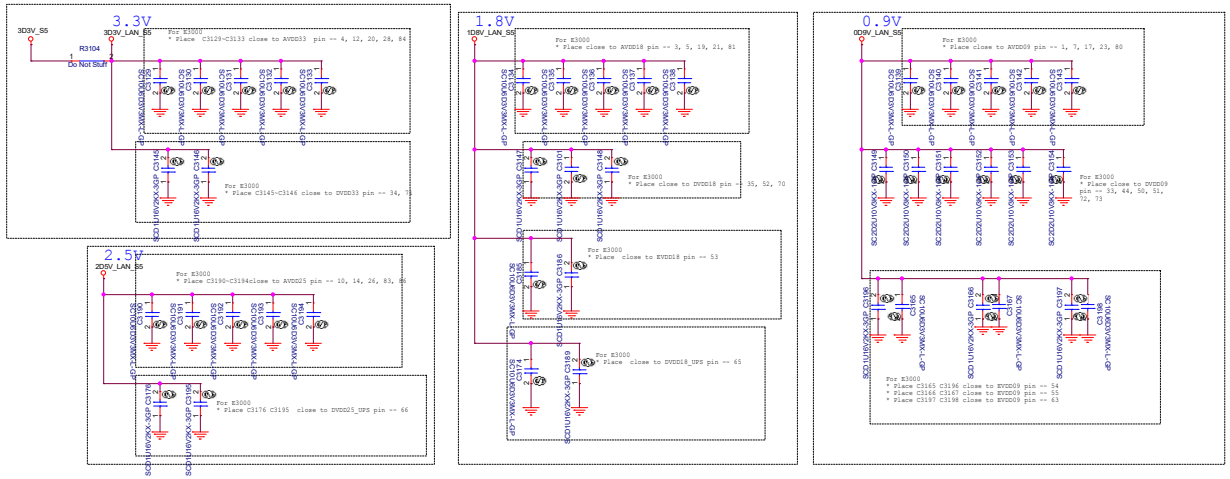
Figure 5. Power Sequence

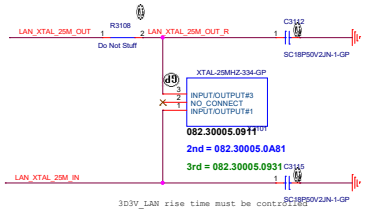
Table 23. Power Sequence Parameters

Symbol	Description	Min	Typical	Max	Unit
t1	SWR Rise Time	0.5	1	10	ms
t2	SWR Enable Interval	-	-	-	ms
t3	1.8V to 0.9V Enable Interval	(Note 2)	-	-	ms
t4	On/Off Interval	50	-	-	ms

Note 1: The power sequence should be strictly followed as described above.
Note 2: t3 should be well controlled by the KILLER E3000.
Note3: The output DC level tolerance is +/- 5% of the target voltage. Therefore the lowest counting of t1 would be the rising time required for the power rail to output from 0V to 90% target voltage.







N18EG1 SAMSUNG

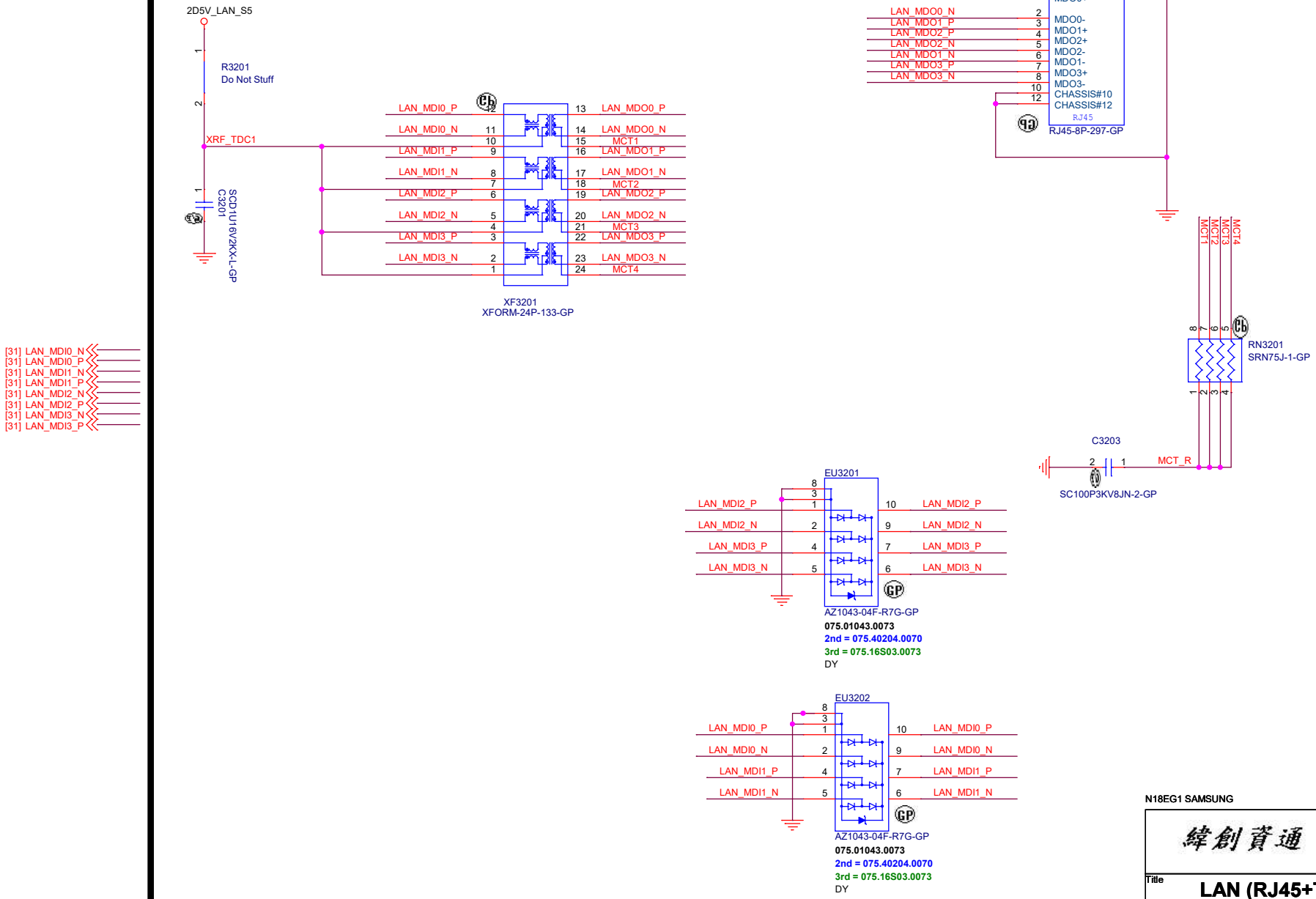
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN(Killer E3000)**

Size	Document Number	Rev
Custom	Ghibli_CFL	SC

Date: Tuesday, December 04, 2018 Sheet 31 of 106

SSID = LAN



N18EG1 SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN (RJ45+Transformer)**

Size	Document Number	Rev
B	Ghibli_CFL	SC

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N18EG1 SAMSUNG

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
CARDREADER (RSVD)

Size	Document Number	Rev
A4	Ghibli_CFL	SC

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N18EG1 SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
USB (RSVD)

Size	Document Number	Rev
A	Ghibli_CFL	SC

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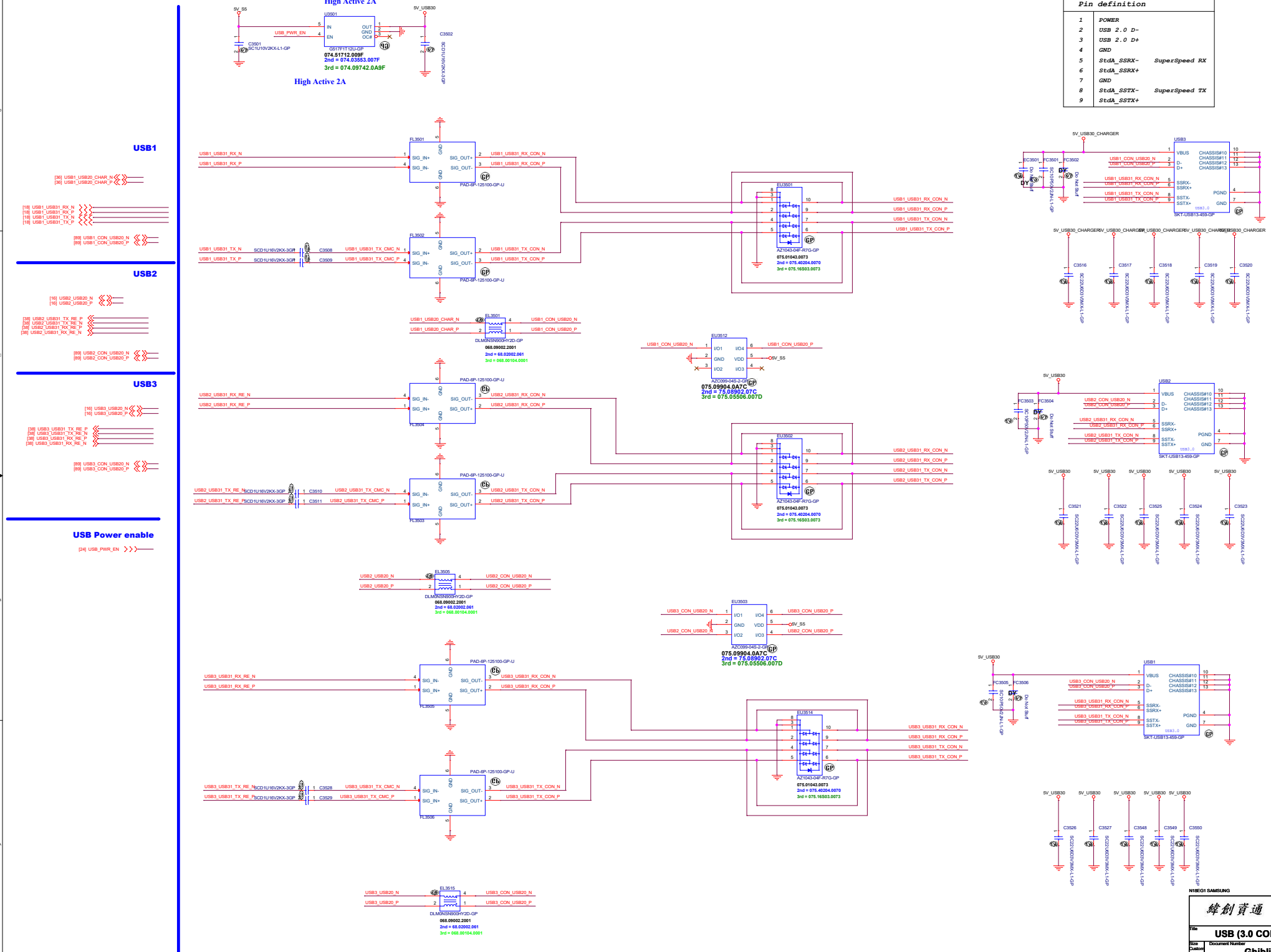
USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (3.0 CONN)

Size: Custom | Document Number: Ghibli_CFL | Rev: SC

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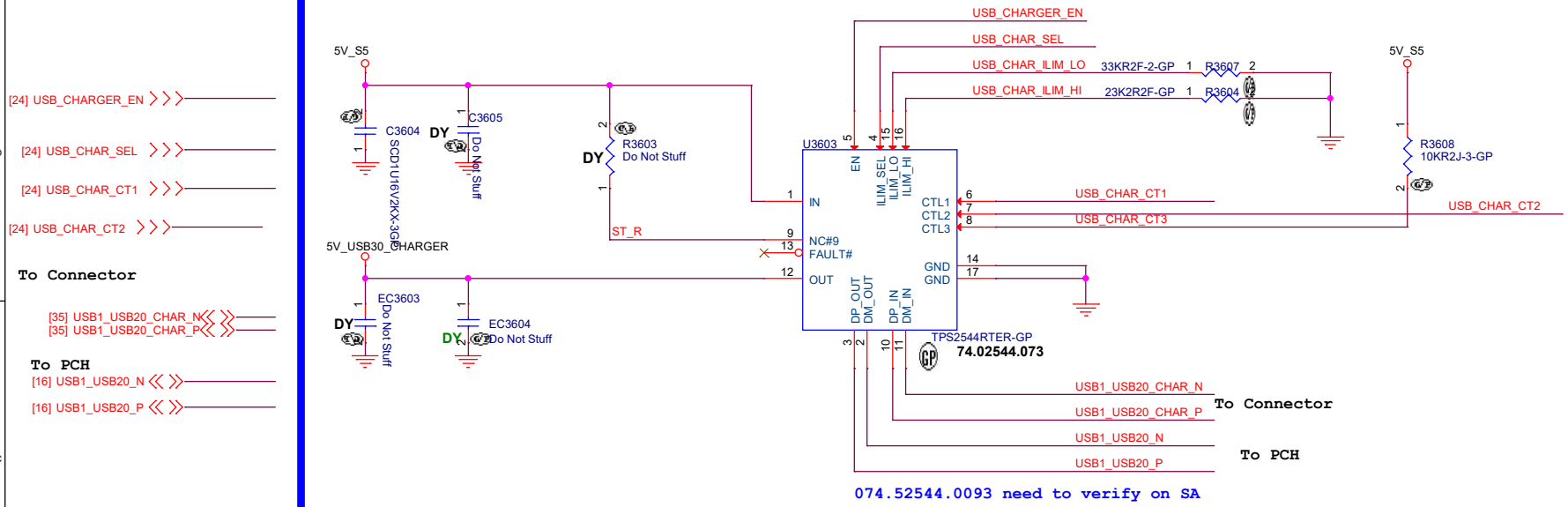


074.52544.0093 need to verify on SA

CTL1	CTL2	CTL3	ILIM_SEL	Mode	Current Limit Setting	Comment
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	
0	0	1	0	DCP_Auto	ILIM_HI	Data Lines Disconnected
0	1	1	X			
0	1	0	0	SDP1	ILIM_LO	Data Lines connected
0	1	0	1		ILIM_HI	
1	0	0	0	DCP Forced Shorted	ILIM_LO	Device Forced to stay in DCP BC 1.2 charging mode
1	0	0	1		ILIM_HI	
1	0	1	0	DCP / Divider1	ILIM_LO	Device Forced to stay in DCP Divider 1 Charging Mode
1	0	1	1		ILIM_HI	
1	1	0	0	SDP1	ILIM_LO	Data Lines Connected
1	1	0	1	SDP1	ILIM_HI	
1	1	1	0	SDP2 (1)	ILIM_LO	
1	1	1	1	CDP (1)	ILIM_HI	Data Lines Connected

N18EG1 SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (USB Charger)

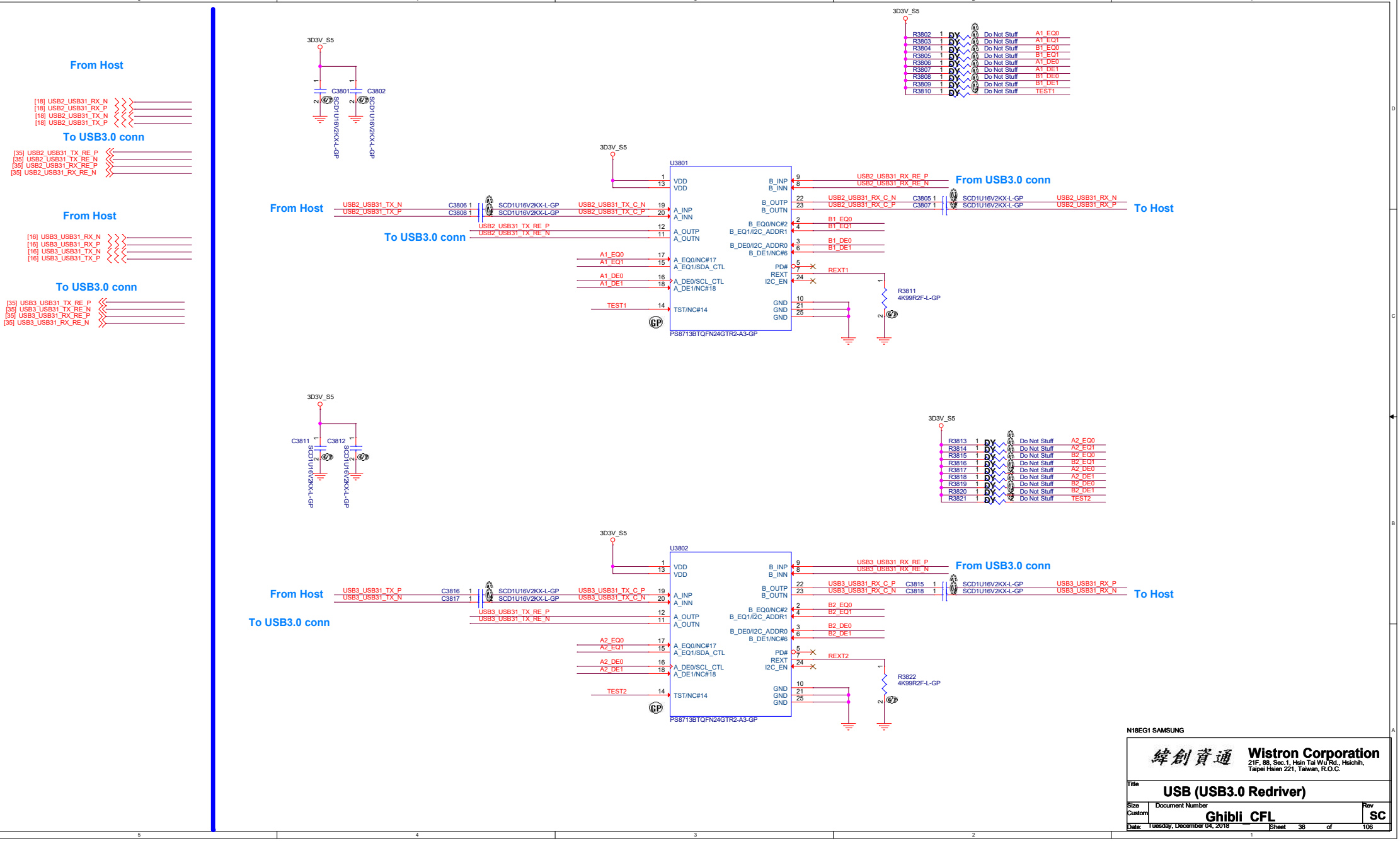
Size: B | Document Number: Ghibli_CFL | Rev: SC

Date: Tuesday, December 04, 2018 | Sheet 36 of 106

N18EG1 SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RSVD	
Size A	Document Number Ghibli_CFL	Rev SC
Date: Monday, December 03, 2018	Sheet 37 of 106	



N18EG1 SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB (USB3.0 Redriver)**

Size	Document Number	Rev
Custom	Ghibli_CFL	SC

Date: Tuesday, December 04, 2018 Sheet 38 of 106

N18EG1 SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Sequence (RSVD)**

Size	Document Number	Rev
A	Ghibli_CFL	SC

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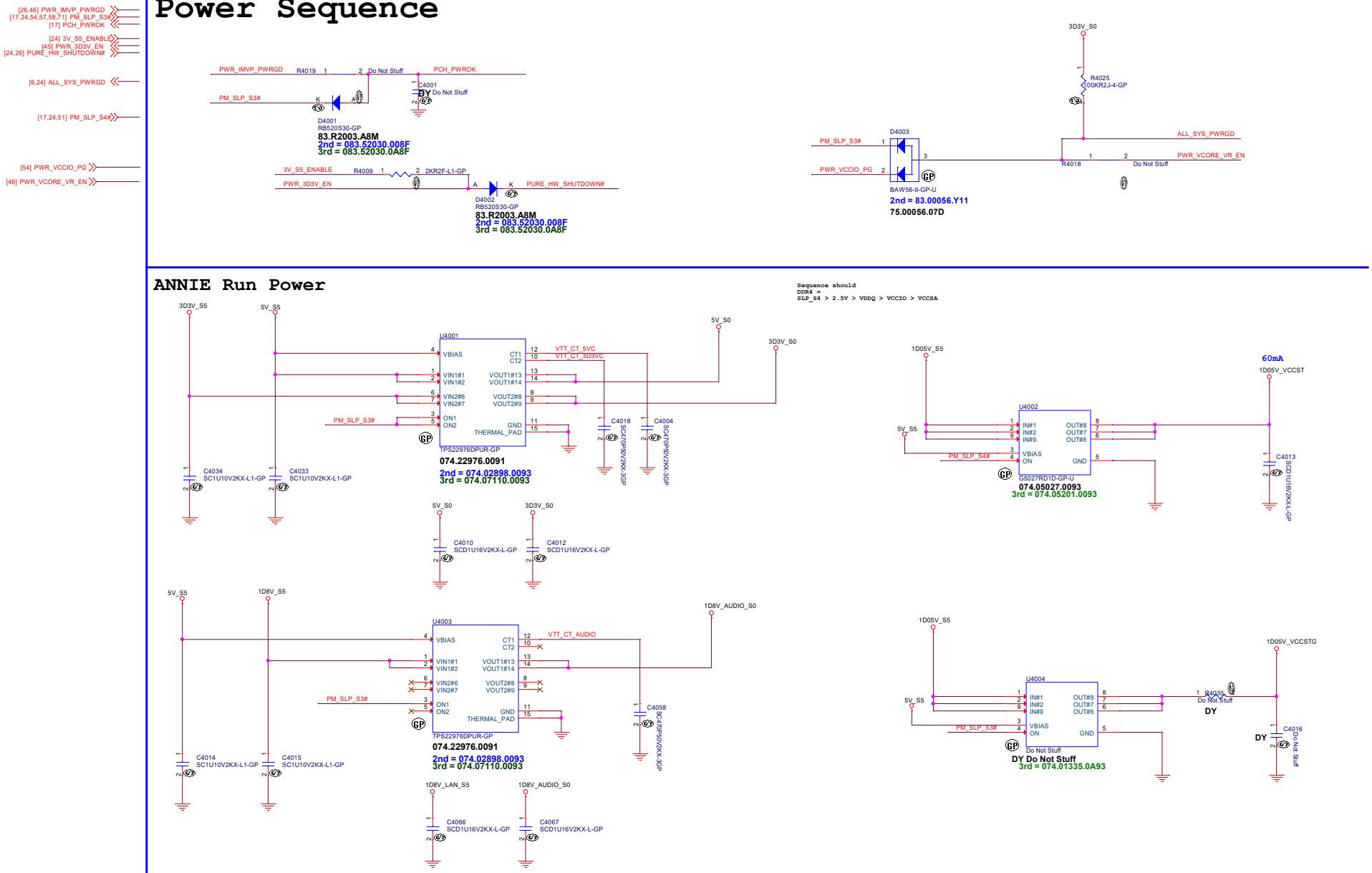
Power Sequence



N18EG1 SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Sequence (Power Plane Enable)	
Size: Custom	Document Number: Ghibli_CFL	Rev: SC
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Main Func = Power & Sequence

N18EG1 SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Sequence (RSVD)

Size	Document Number	Rev
A3	Ghibli_CFL	SC

Date: Monday, December 03, 2018 Sheet 41 of 106

N18EG1 SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**INT IO (RSVD)**	
Size A	Document Number **Ghibli_CFL**	Rev **SC**
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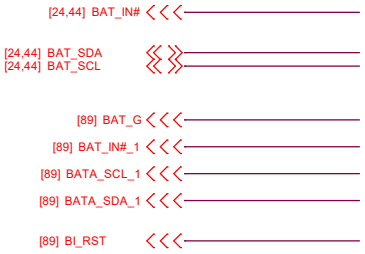
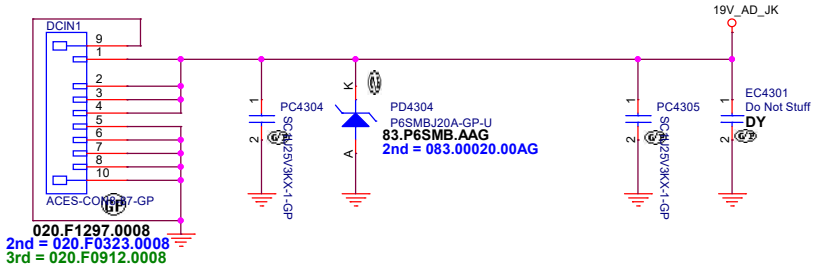
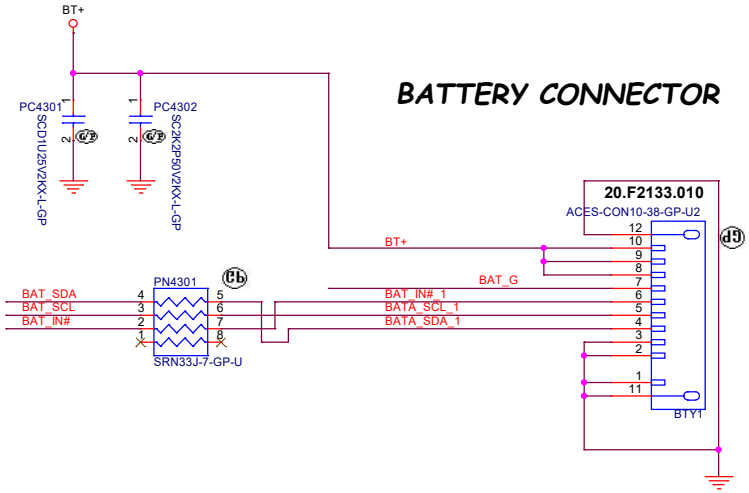
ANNIE solution

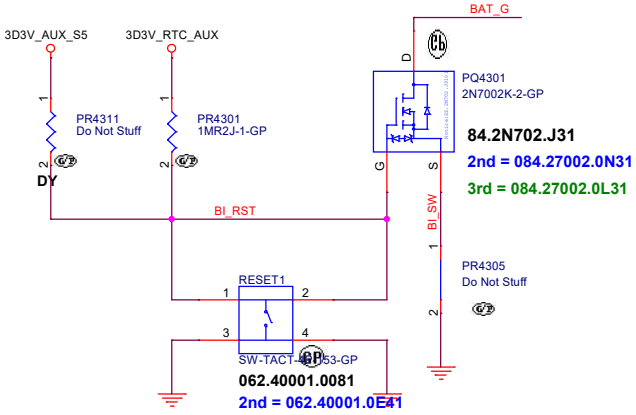


Adaptor in to generate DCBATOUT



BATTERY CONNECTOR





N18EG1 SAMSUNG

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**INT IO (ATX/ DC/ BATT Conn)**	
Size A3	Document Number **Ghibli_CFL**	Rev **SC**
Date: Tuesday, December 04, 2018	Sheet 43 of 106	

OFFPAGE

PH on EE Side

[24,43] BAT_SCL — BAT_SCL
[24,43] BAT_SDA — BAT_SDA

Dicharge Current

[24] BT_IA — BT_IA
[24] AD_IA — AD_IA

PH on EE Side

[19] DGPUHOT# — DGPUHOT#
[8,24,46] PROCHOT#_CPU — PROCHOT#_CPU

PH on EE Side

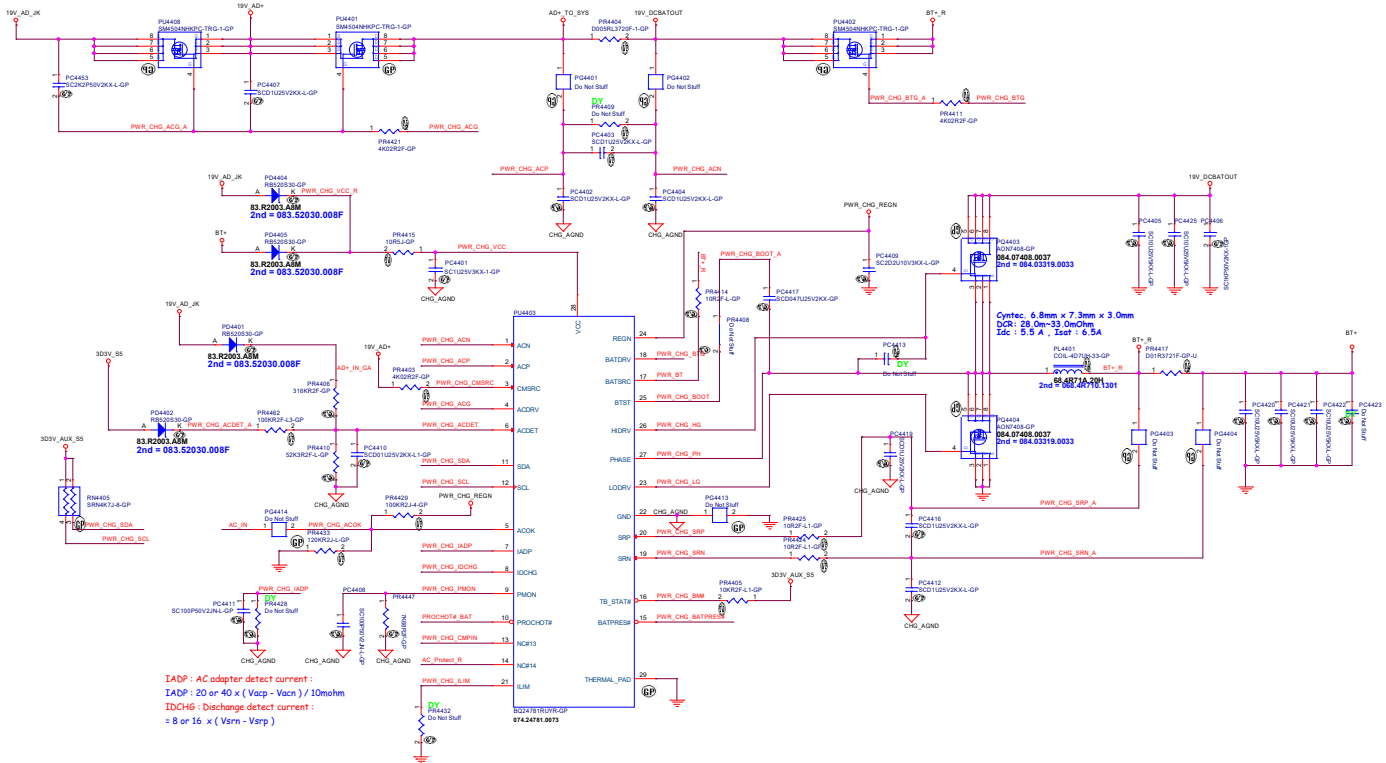
[24,43] BAT_IN# — BAT_IN#
[24] PWR_AC_IN# — PWR_AC_IN#
[24] PWR_CHG_ON# — PWR_CHG_ON#

PMON : Total system power(PSYS)

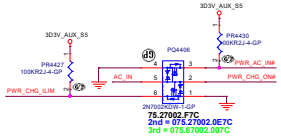
[46] CHGR_PSYS_IMVP — CHGR_PSYS_IMVP

SSID = Charger

BAT_SCL	PR4459 Do Not Stuff	PWR_CHG_SCL
BAT_SDA	PR4460 Do Not Stuff	PWR_CHG_SDA
BT_IA	PR4454 Do Not Stuff	PWR_CHG_IDCHG
CHGR_PSYS_IMVP	PR4455 Do Not Stuff	PWR_CHG_PMON
AD_IA	PR4456 Do Not Stuff	PWR_CHG_IADP
BAT_IN#	PR4457 Do Not Stuff	PWR_CHG_BATPRES#



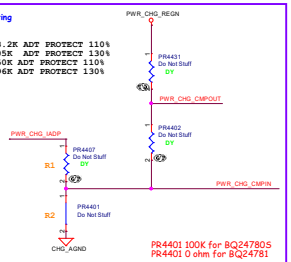
IADP : AC adapter detect current :
IADP : 20 or 40 x (Vacp - Vacn) / 10mohm
IDCHG : Dischange detect current :
= 8 or 16 x (Vsrn - Vsrp)



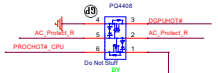
Adaptor			Protect	Sense	Amplifer		R1	R2
Watt	Current	Persent	Current	Resistor	Ratio	IADP	PR4407	PR4401
135.00 W	6.92 A	102%	7.06 A	10 m Ohm	40	2.82 V	137 K	100 K
120.00 W	6.15 A	102%	6.28 A	10 m Ohm	40	2.51 V	110 K	100 K
90.00 W	4.62 A	102%	4.71 A	10 m Ohm	40	1.88 V	56 K	100 K

Total Power Setting

PR4407 45W 73.2K ADT PROTECT 110%
PR4407 45W 105K ADT PROTECT 130%
PR4407 65W 150K ADT PROTECT 110%
PR4407 65W 196K ADT PROTECT 130%

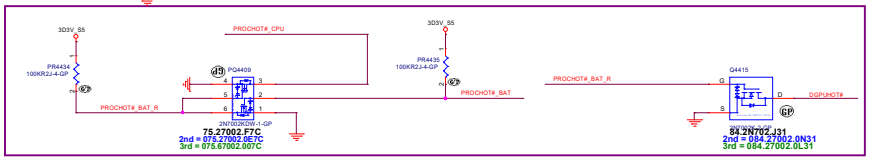


PR4401 100K for BQ24780S
PR4401 0 ohm for BQ24781



Do Not Stuff
2nd = 075.27002.0E7C
3rd = 075.67002.007C

PQ4408 上件 for BQ24780S
PQ4408 DY for BQ24781



NI BEG1 SAMBUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Power (CHARGER BQ247801)

Size	Document Number	Rev
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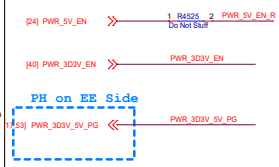
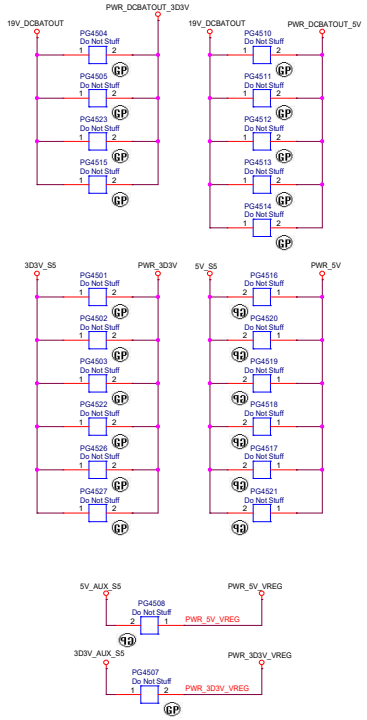
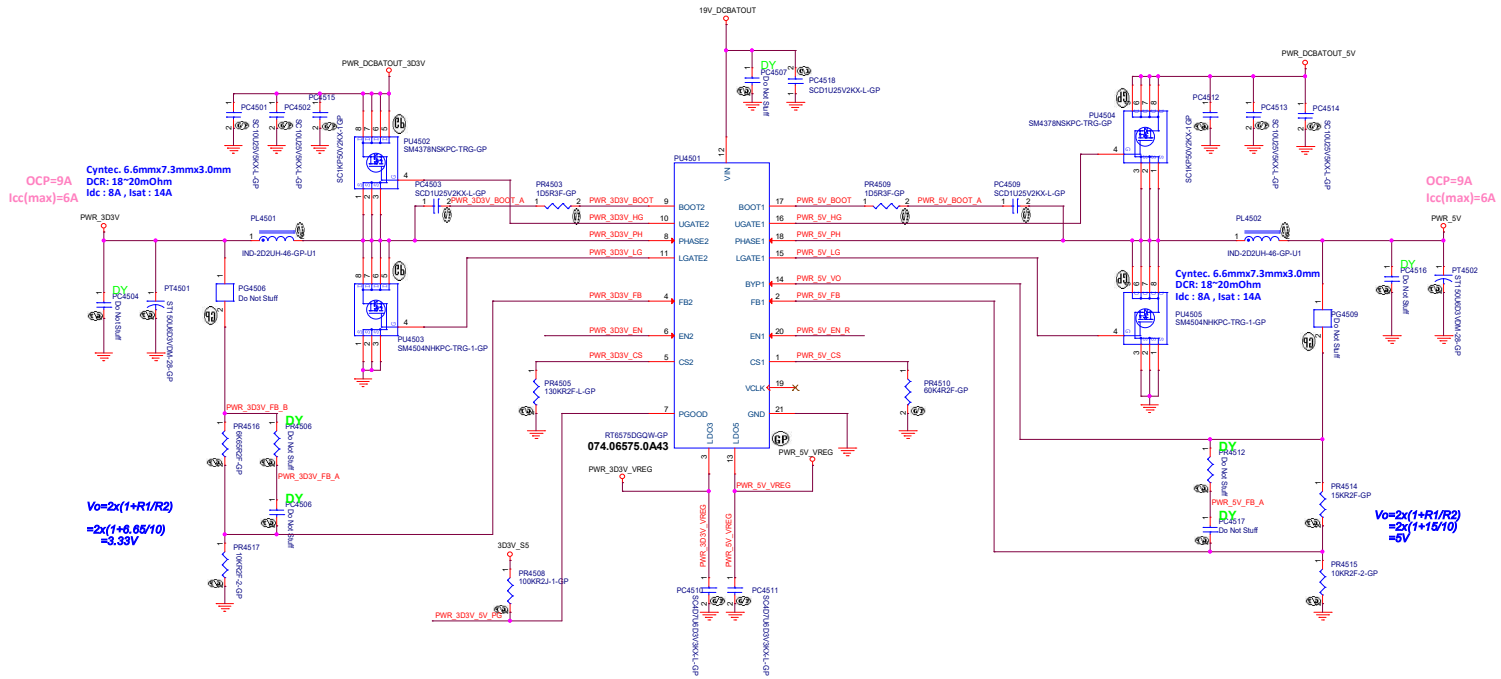
OFFPAGE-Signal



OFFPAGE-GAP



Main Func = 3D3V_5V



N18EG1 SAMSUNG

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Power (RT6575D_5V/3D3V)	
Size / Custom	Document Number: Ghibli_CFL	Rev: SC
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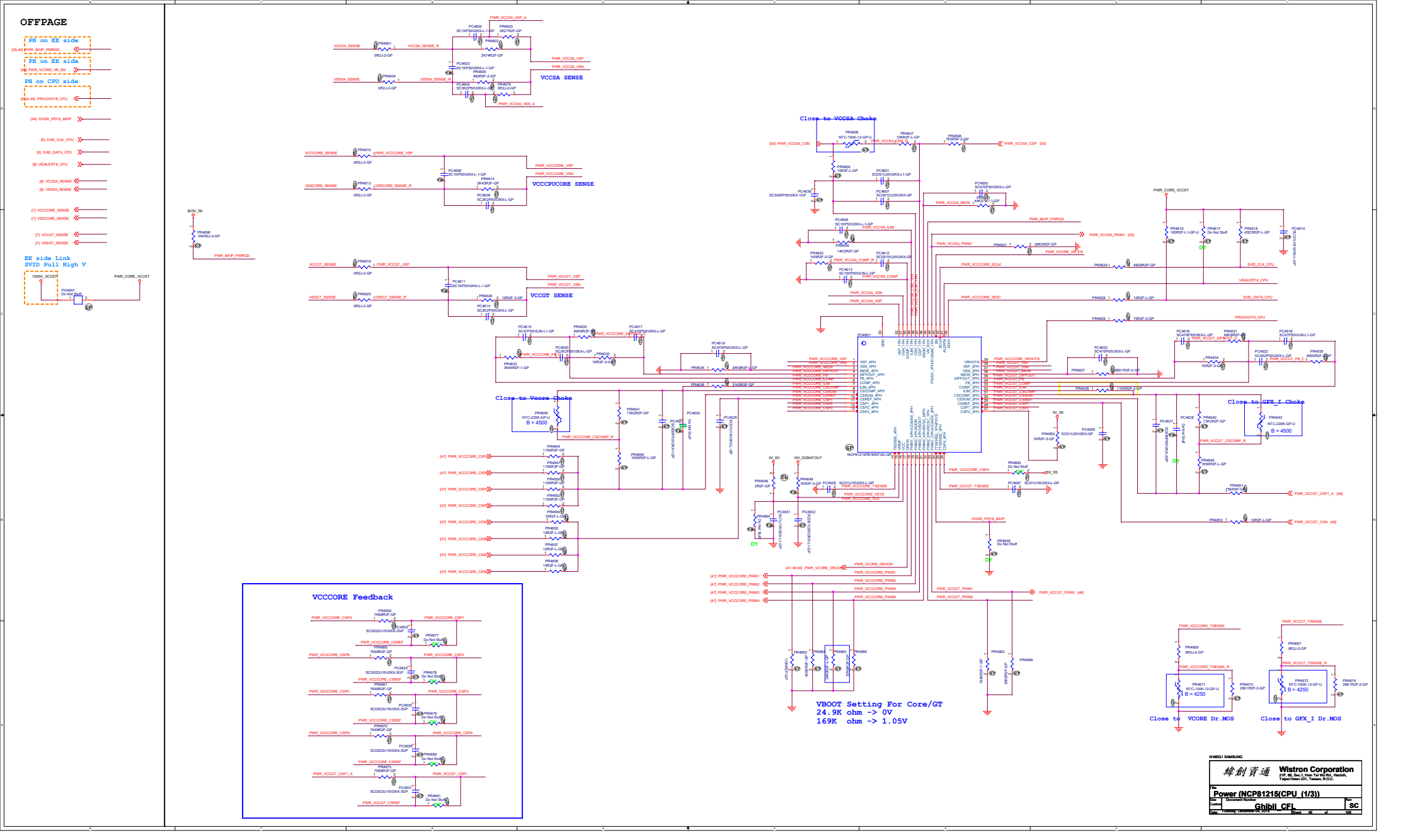
OFFPAGE
PH on EE side
PH on EE side
PH on CPU side
EE side Link
SVID Pull High V
VCCSA SENSE
VCCCPUCORE SENSE
VCCGT SENSE
Close to VCCSA Choke
Close to Vcore Choke
Close to GFX_I Choke
VCCCORE Feedback
VBOOT Setting For Core/GT
24.9K ohm -> 0V
169K ohm -> 1.05V
Close to VCORE Dr.MOS
Close to GFX_I Dr.MOS
Wistron Corporation
Power (NCP81215(CPU (1/3))
Ghibli_CFL
SC

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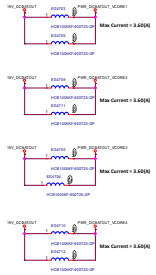
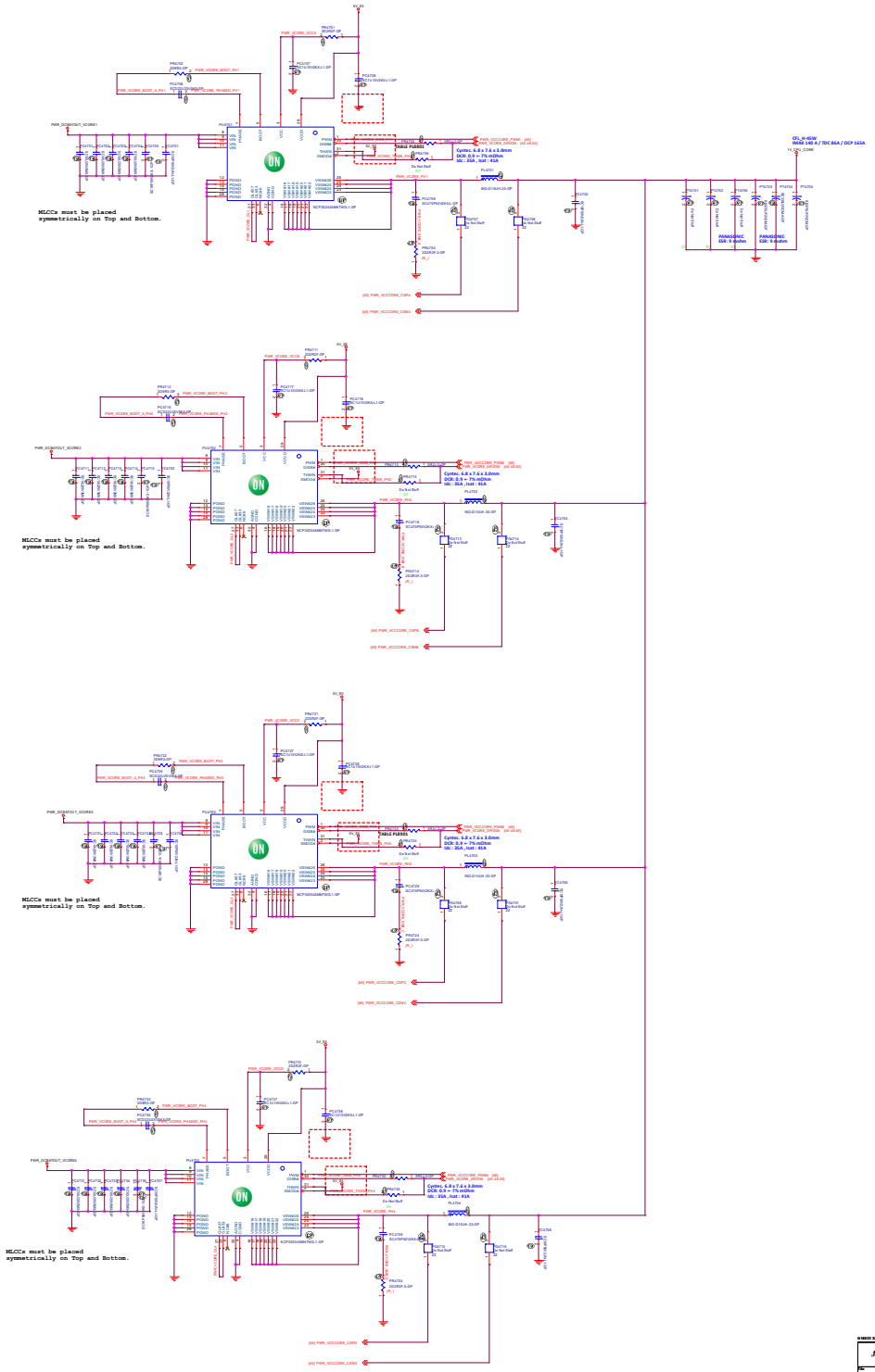
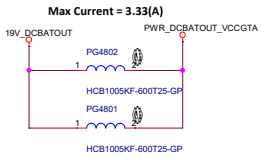
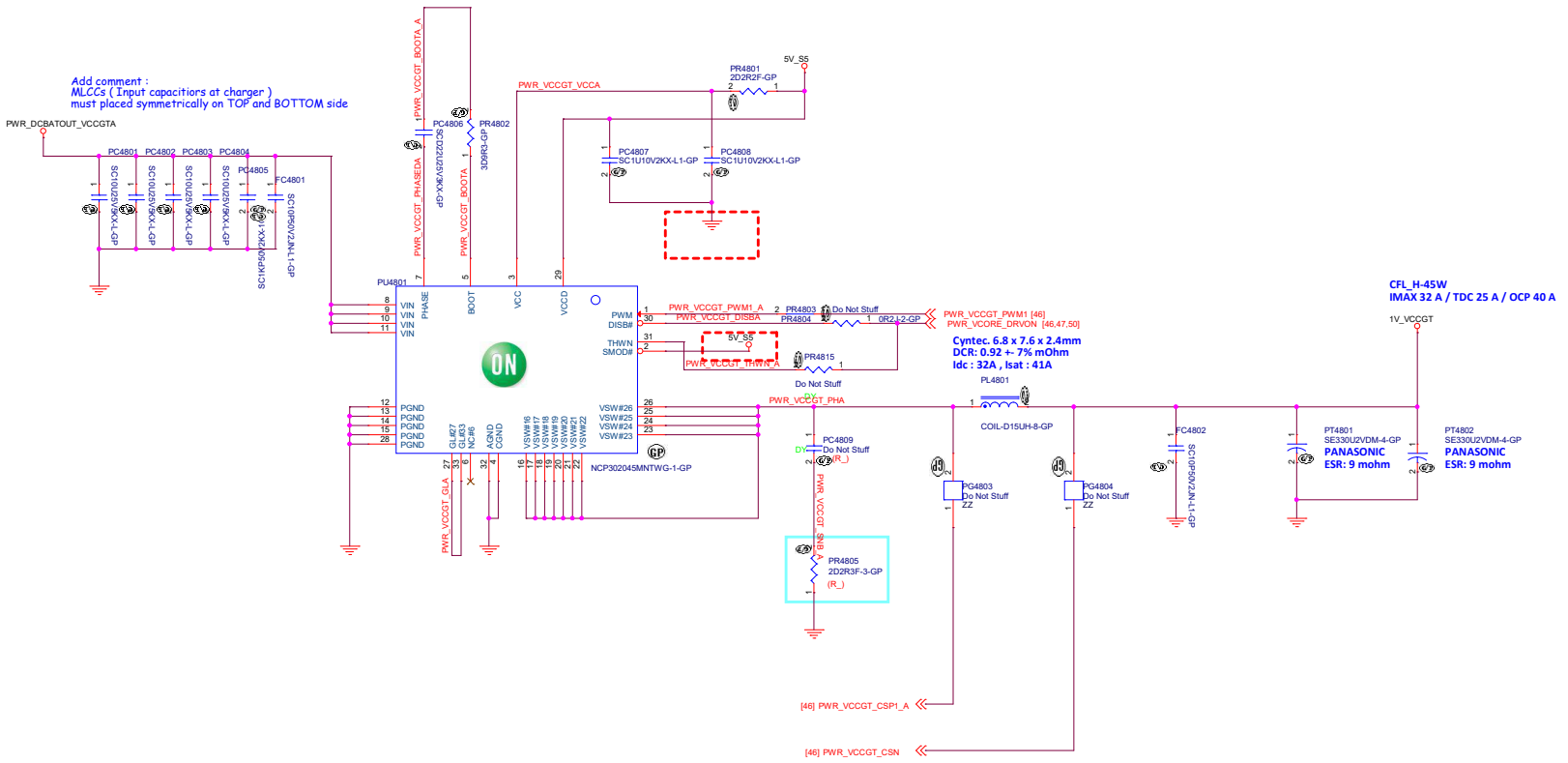




緯創資通	Wistron Corporation Power (NCP8121S(CPU (2/3))
Project	Ghibli CFL
Date	Sheet 2 of 2

OFFPAGE





N18EG1 SAMSUNG

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**Power_NCP81215MN_CPU_VCCGT(3/4)**
Size: Custom	Document Number: **Ghibli_CFL**
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N18EG1 SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Power (Reserved)
Size: Custom	Document Number: Ghibli_CFL
Rev	SC
Date: Monday, December 03, 2018	Sheet 49 of 106

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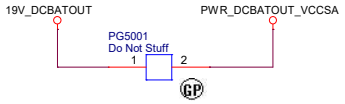
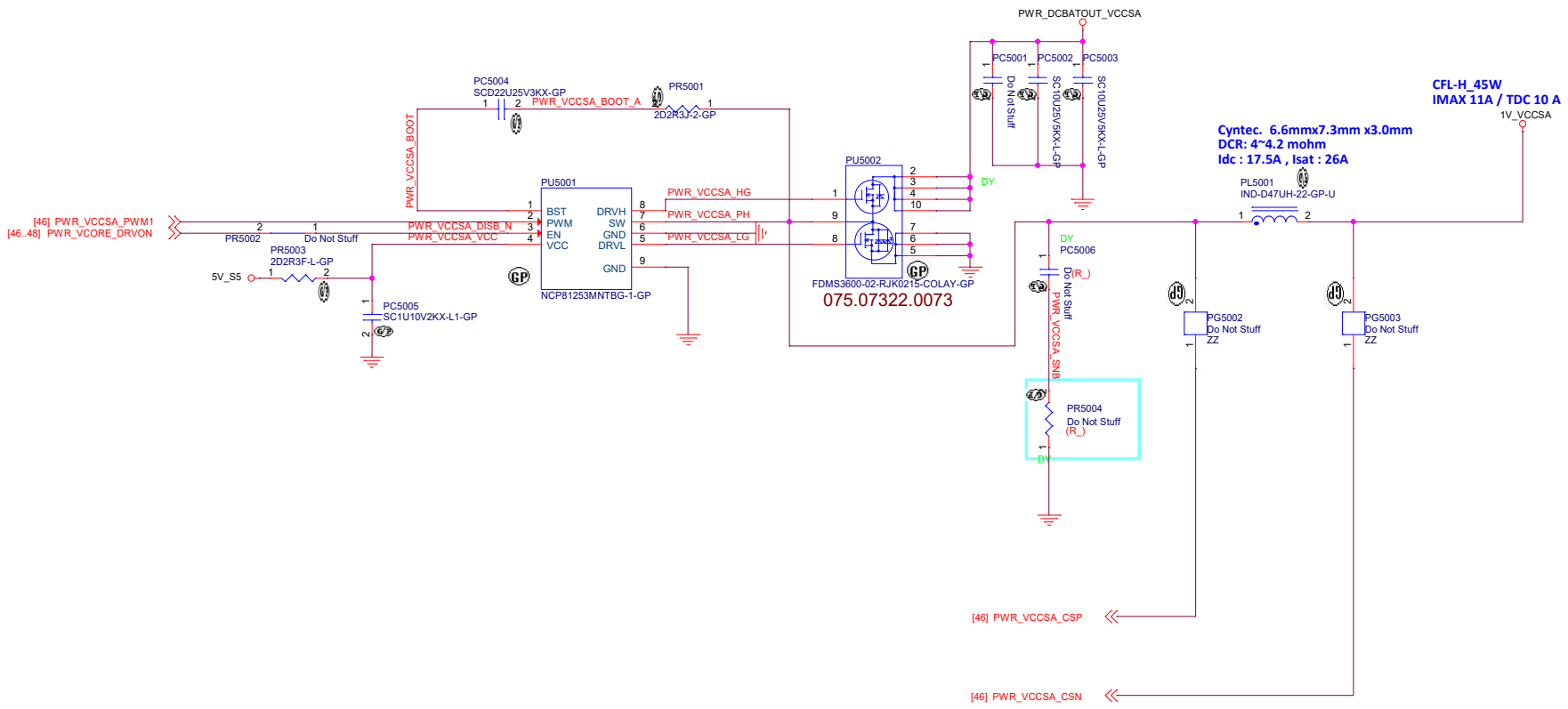


Max Current = 1.15(A)



N18EG1 SAMSUNG

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Power_NCP81215MN_CPU_VCCSA(4/4)**	
Size: Custom	Document Number: **Ghibli_CFL**	Rev: **SC**
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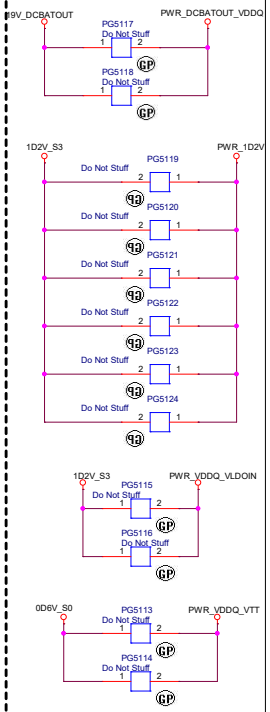
OFFPAGE

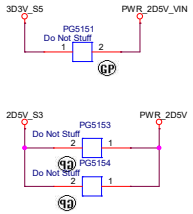
S5
[17,24,40] PM_SLP_S4# — PM_SLP_S4#

S3
[6] PWR_VTT_EN — PWR_VTT_EN

PH on EE Side
[54] PWR_VDDQ_PG — PWR_VDDQ_PG

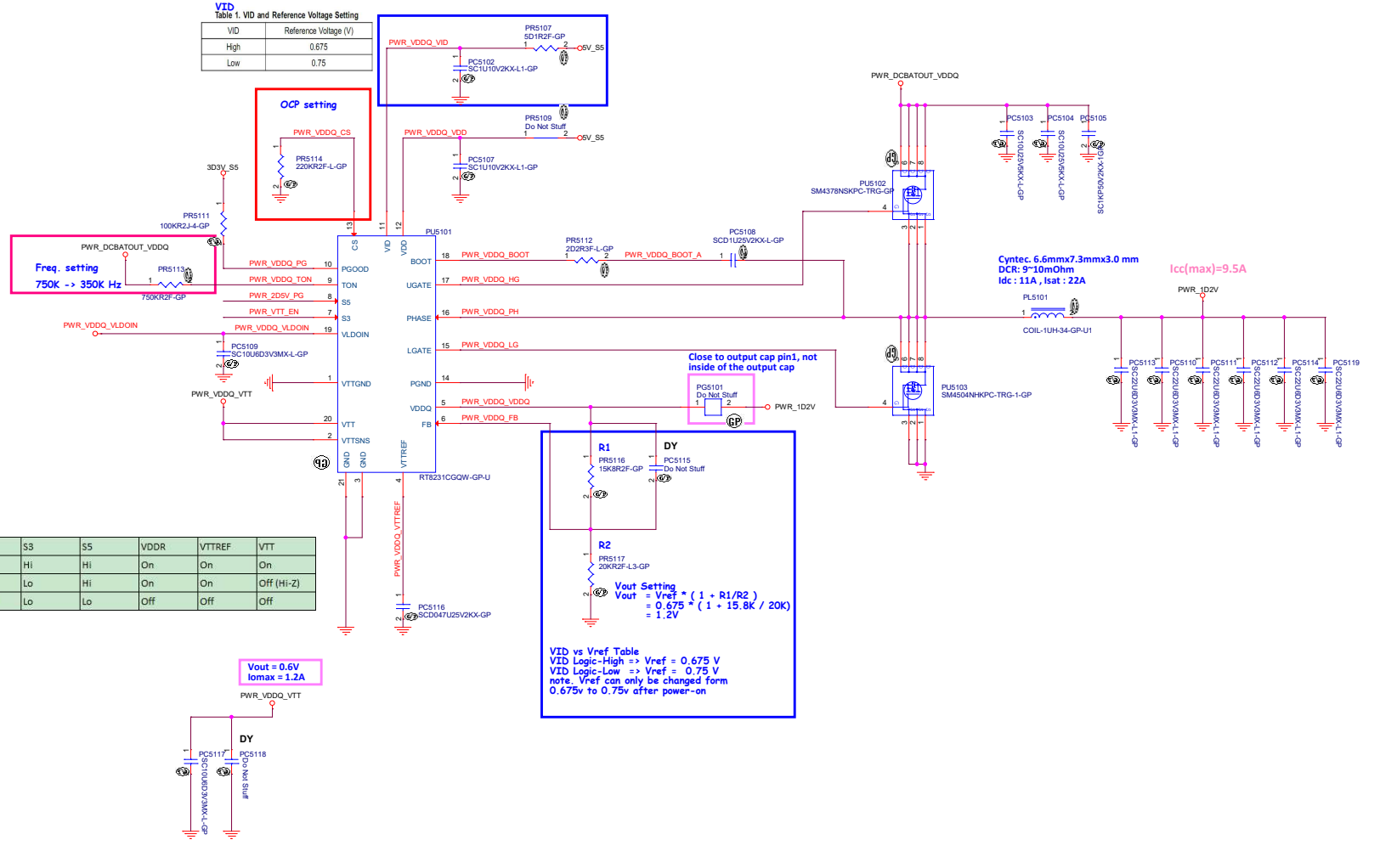
OFFPAGE_GAP





VID
Table 1. VID and Reference Voltage Setting

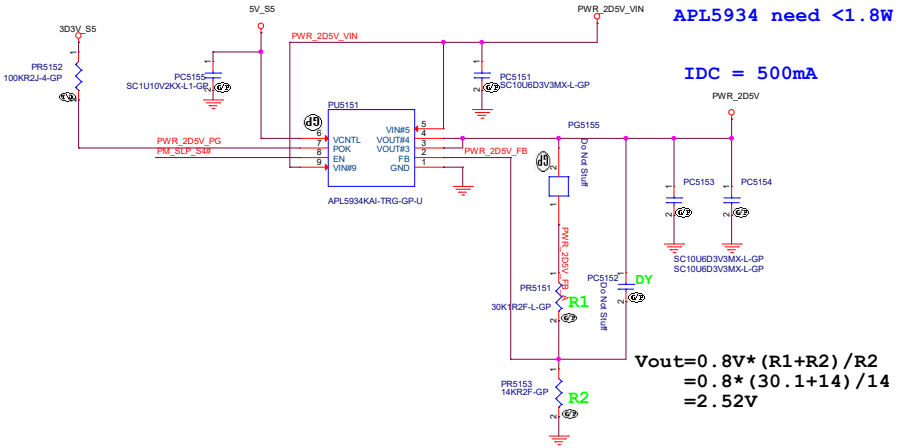
VID	Reference Voltage (V)
High	0.675
Low	0.75



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Main Func = 2D5V

APL5934 for 2D5V



APL5934 need <1.8W

IDC = 500mA

Vout=0.8V*(R1+R2)/R2
=0.8*(30.1+14)/14
=2.52V

N18EG1 SAMSUNG

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Power (RT8231_VDDQ/VTT/VPP)		
Size: A2	Document Number: Ghibli_CFL	Rev: SC
Date: Tuesday, December 04, 2018	Sheet 51 of 106	

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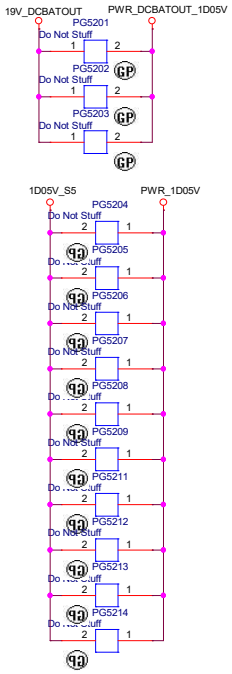
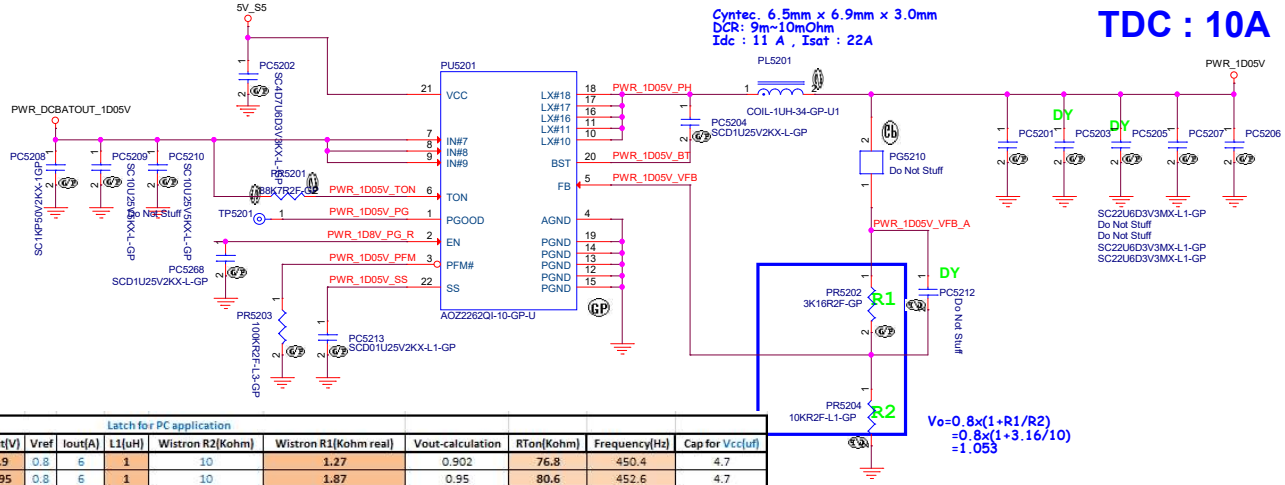


SSID = PWR.Plane.Regulator_1p05v

COM \ IC	AOZ2262(10A) 074.02262.0043	AOZ2261(8A) 074.02261.0A73	AOZ2260(6A) 074.02260.0043
Chock	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A
Output CAP	22uF/6.3V * 5pcs DY*1	22uF/6.3V * 4pcs DY*1	22uF/6.3V * 4pcs DY*1

AOZ2262 for 1D05V



Latch for PC application										
Vin(V)	Vout(V)	Vref	Iout(A)	L1(uH)	Wistron R2(Kohm)	Wistron R1(Kohm real)	Vout-calculation	RTon(Kohm)	Frequency(Hz)	Cap for Vcc(uf)
19.5	0.9	0.8	6	1	10	1.27	0.902	76.8	450.4	4.7
19.5	0.95	0.8	6	1	10	1.87	0.95	80.6	452.6	4.7
19.5	1	0.8	6	1	10	2.55	1.004	84.5	454.4	4.7
19.5	1.05	0.8	6	1	10	3.16	1.053	88.7	454.5	4.7
19.5	1.1	0.8	6	1	10	3.83	1.106	93.1	453.7	4.7
19.5	1.2	0.8	6	1	10	5.11	1.209	102	451.7	4.7
19.5	1.25	0.8	6	1	10	5.62	1.25	107	448.6	4.7
19.5	1.35	0.8	6	1	10	6.98	1.358	115	450.8	4.7
19.5	1.5	0.8	6	1	10	8.87	1.51	127	453.5	4.7
19.5	1.8	0.8	6	1	10	12.7	1.816	154	448.8	4.7
19.5	2.5	0.8	6	1	10	21.5	2.52	215	446.5	4.7

Latch for PC application						6A Vout		8A Vout			10A Vout		
Vin(V)	Vout(V)	Vref	Iout(A)	Frequency(Hz)	Cap for Vcc(uf)	10uf Cap# for Vin	22uf Cap# for Vout	10uf Cap# for Vin	22uf Cap# for Vout	22uf reserve for Vout	10uf Cap# for Vin	22uf Cap# for Vout	22uf reserve for Vout
19.5	0.9	0.8	6	450.4	4.7	2	3	2	4	1	2	5	1
19.5	0.95	0.8	6	452.6	4.7	2	3	2	4	1	2	5	1
19.5	1	0.8	6	454.4	4.7	2	3	2	4	1	2	5	1
19.5	1.05	0.8	6	454.5	4.7	2	3	2	4	1	2	5	1
19.5	1.1	0.8	6	453.7	4.7	2	3	2	4	1	2	5	1
19.5	1.2	0.8	6	451.7	4.7	2	3	2	4	1	2	5	1
19.5	1.25	0.8	6	448.6	4.7	2	3	2	4	1	2	5	1
19.5	1.35	0.8	6	450.8	4.7	2	3	2	4	1	2	5	1
19.5	1.5	0.8	6	453.5	4.7	2	3	2	4	1	2	5	1
19.5	1.8	0.8	6	448.8	4.7	2	3	2	4	1	2	5	1
19.5	2.5	0.8	6	446.5	4.7	2	3	2	4	1	2	5	1

N18EG1 SAMSUNG

緯創資通 Wistron Corporation
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Title: Power (AOZ2262Q_1D05V)

Size: Custom | Document Number: Ghibli_CFL | Rev: SC

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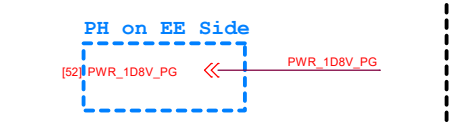
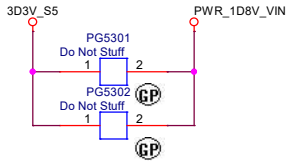
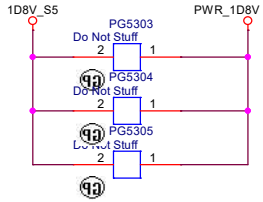
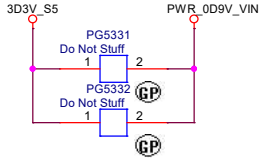
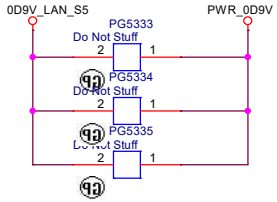


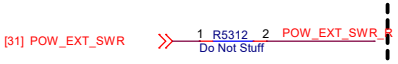
OFFPAGE_GAP

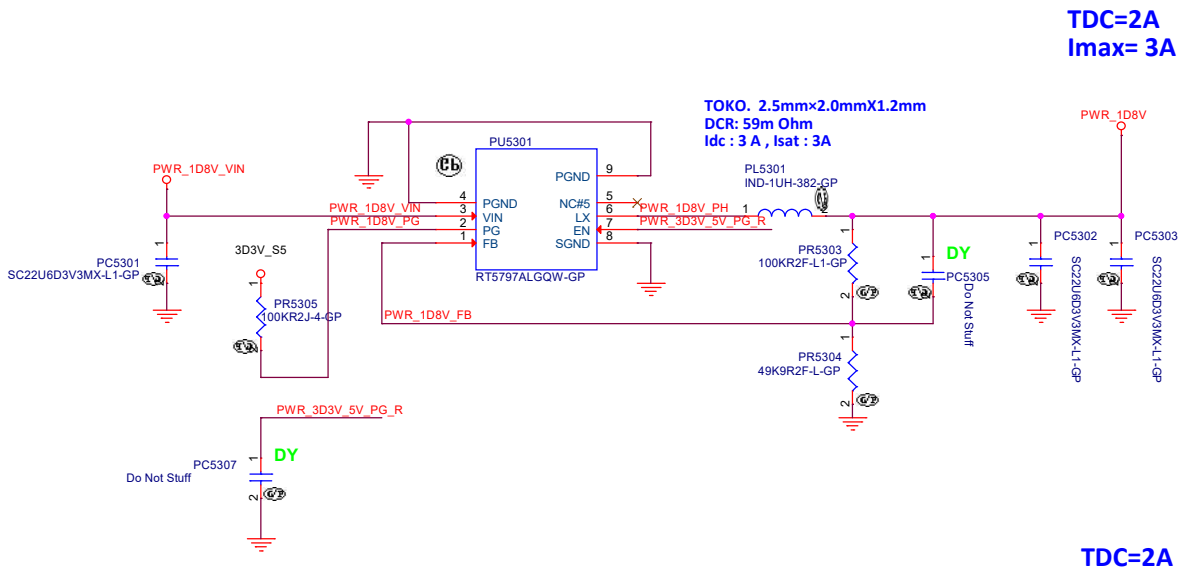


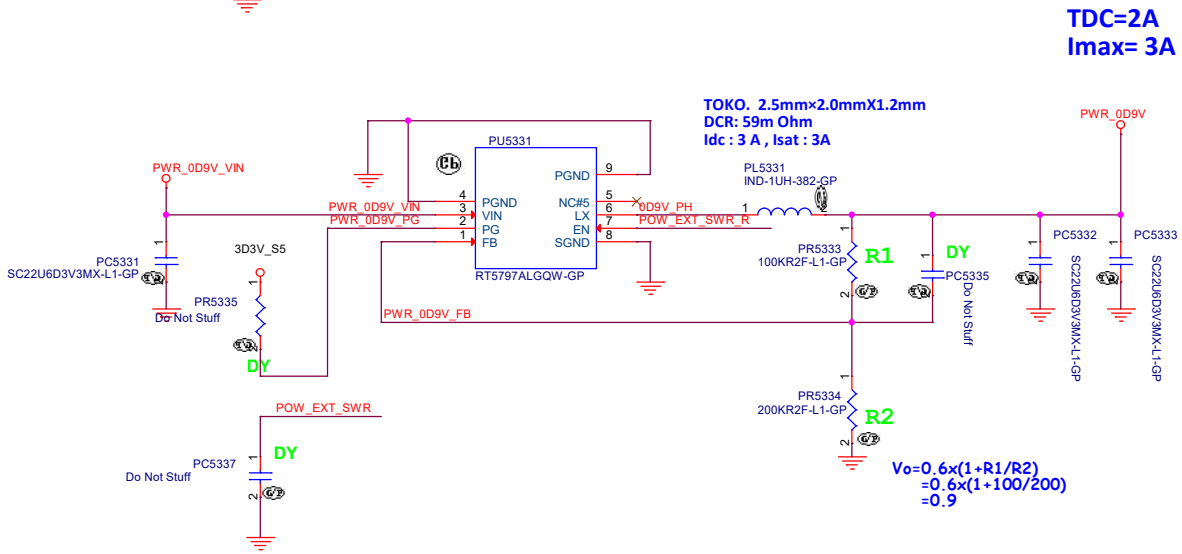












N18EG1 SAMSUNG

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**053_Power (RT5797A_1D8V)**	
Size A3	Document Number **Ghibli_CFL**	Rev **SC**
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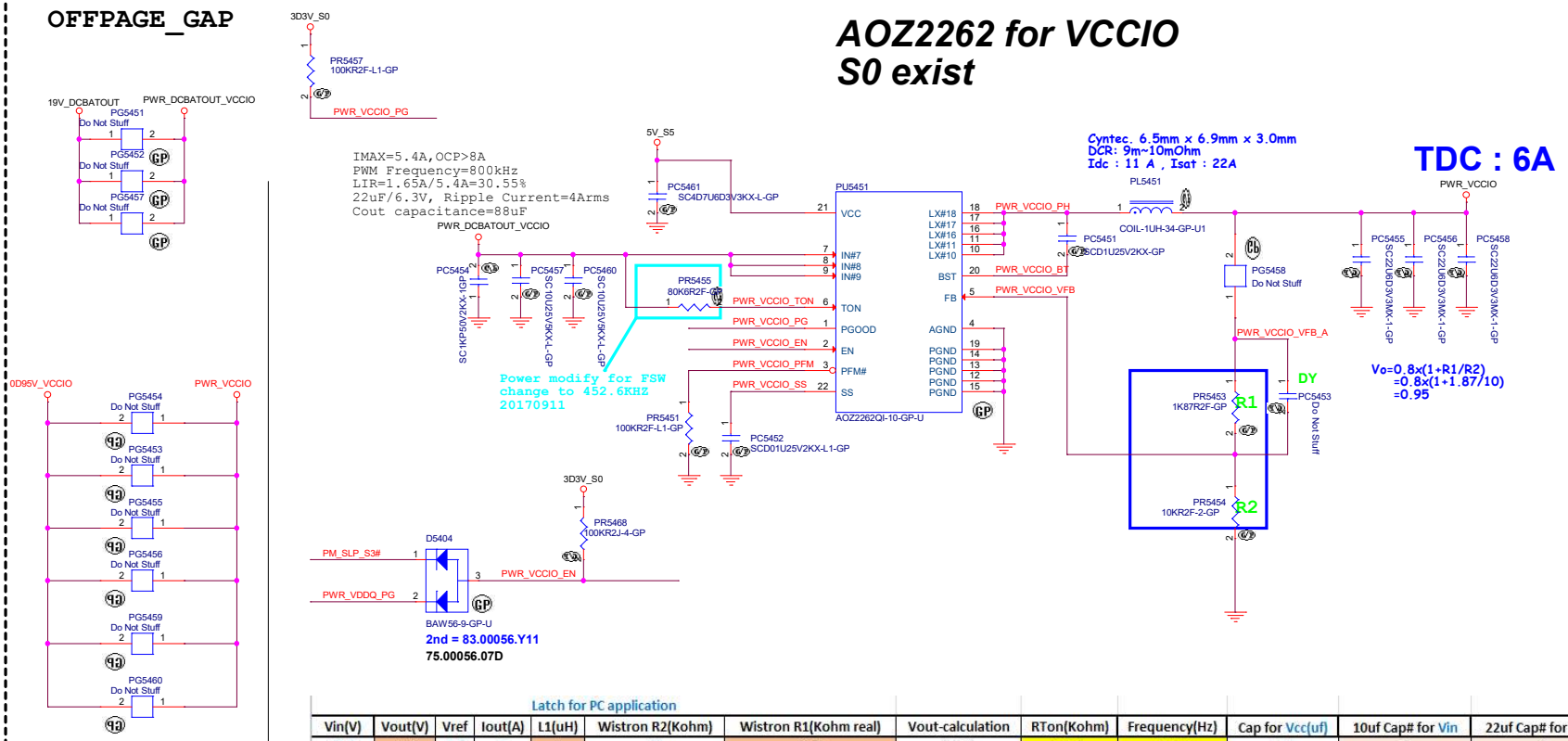
[17,24,40,57,58,71] PM_SLP_S3#

[40] PWR_VCCIO_PG — PWR_VCCIO_PG

[51] PWR_VDDQ_PG

OFFPAGE_GAP



Latch for PC application

Vin(V)	Vout(V)	Vref	Iout(A)	L1(uH)	Wistron R2(Kohm)	Wistron R1(Kohm real)	Vout-calculation	RTon(Kohm)	Frequency(Hz)	Cap for Vcc(uf)	10uf Cap# for Vin	22uf Cap# for Vout
19.5	0.9	0.8	6	1	10	1.27	0.902	76.8	450.4	4.7	2	3
19.5	0.95	0.8	6	1	10	1.87	0.95	80.6	452.6	4.7	2	3
19.5	1	0.8	6	1	10	2.55	1.004	84.5	454.4	4.7	2	3
19.5	1.05	0.8	6	1	10	3.16	1.053	88.7	454.5	4.7	2	3
19.5	1.1	0.8	6	1	10	3.83	1.106	93.1	453.7	4.7	2	3
19.5	1.2	0.8	6	1	10	5.11	1.209	102	451.7	4.7	2	3
19.5	1.25	0.8	6	1	10	5.62	1.25	107	448.6	4.7	2	3
19.5	1.35	0.8	6	1	10	6.98	1.358	115	450.8	4.7	2	3
19.5	1.5	0.8	6	1	10	8.87	1.51	127	453.5	4.7	2	3
19.5	1.8	0.8	6	1	10	12.7	1.816	154	448.8	4.7	2	3
19.5	2.5	0.8	6	1	10	21.5	2.52	215	446.5	4.7	2	3

Auto Recovery for High voltage output application

Vin(V)	Vout(V)	Vref	Iout(A)	L1(uH)	Wistron R2(Kohm)	Wistron R1(Kohm real)	Vout-calculation	RTon(Kohm)	Frequency(Hz)	Cap for Vcc(uf)	10uf Cap# for Vin	22uf Cap# for Vout
19.5	10	0.8	6	2.2	10	115	10	866	443.8	4.7	2	4
19.5	12	0.8	6	3.3	10	140	12	1050	438.8	4.7	2	4

N18EG1 SAMSUNG

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Title: 054_Power (AOZ2262Q_VCCIO)

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Main Func = LCD

LCD

[56] eDP_TX_RE_P0
[56] eDP_TX_RE_N0
[56] eDP_TX_RE_P1
[56] eDP_TX_RE_N1
[56] eDP_TX_RE_P2
[56] eDP_TX_RE_N2
[56] eDP_TX_RE_P3
[56] eDP_TX_RE_N3

[56] eDP_AUX_RE_P
[56] eDP_AUX_RE_N

[56] eDP_HPD_MUX

[24] OD

[56] eDP_VDDEN_MUX

[56] eDP_BLCTRL_MUX

[24] BLON_OUT
[79] GSYNC_ID

CCD

[16,89] CCD_USB20_N
[16,89] CCD_USB20_P

DMIC CODEC

[27] DMIC2_SDA_CON
[27] DMIC1_SDA_CON
[27] DMIC_SCL_CON

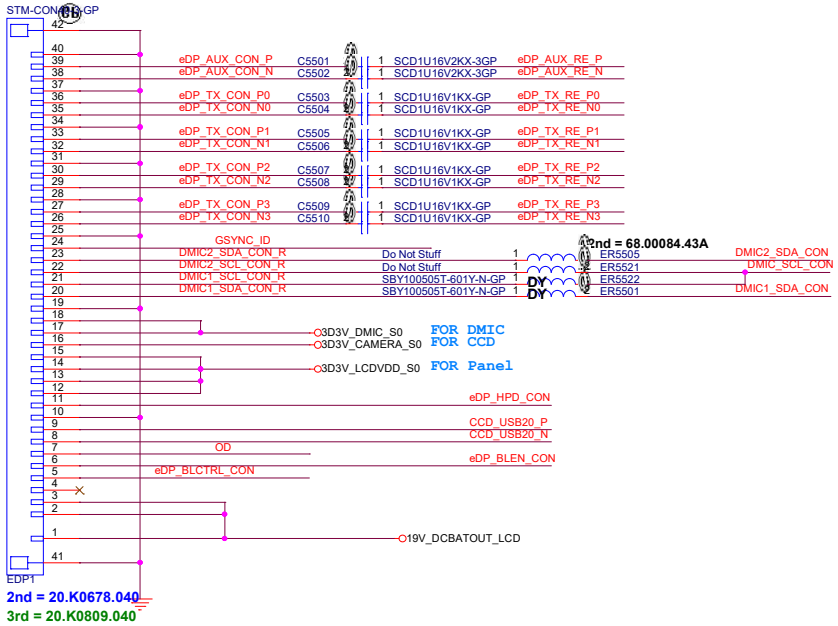
AFTP

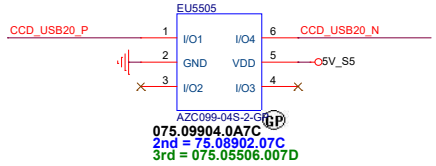
[89] eDP_HPD_CON
[89] eDP_BLEN_CON
[89] eDP_BLCTRL_CON

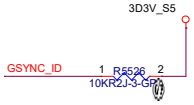
[89] eDP_TX_CON_P0
[89] eDP_TX_CON_N0
[89] eDP_TX_CON_P1
[89] eDP_TX_CON_N1
[89] eDP_AUX_CON_P
[89] eDP_AUX_CON_N
[89] eDP_TX_CON_P2
[89] eDP_TX_CON_N2

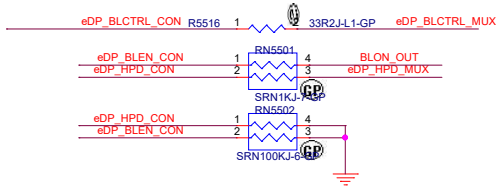
[89] eDP_TX_CON_P3
[89] eDP_TX_CON_N3

[89] DMIC2_SDA_CON_R
[89] DMIC1_SDA_CON_R
[89] DMIC1_SCL_CON_R
[89] DMIC2_SCL_CON_R



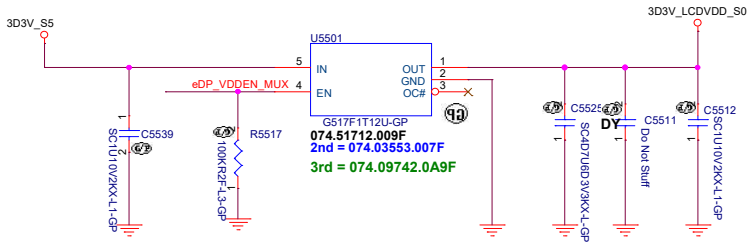


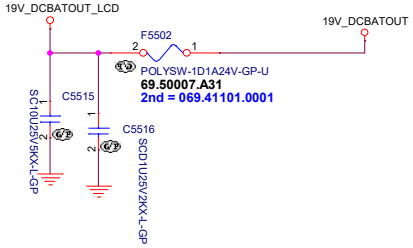




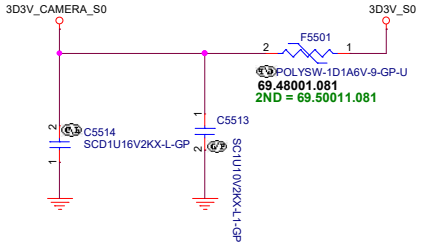
panel Power

For LCD

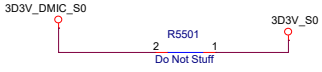




CCD Power



DMIC Power



N18EG1 SAMSUNG

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Title: Display (LCD/Scalar)

Size: Custom | Document Number: Ghibli_CFL | Rev: SC

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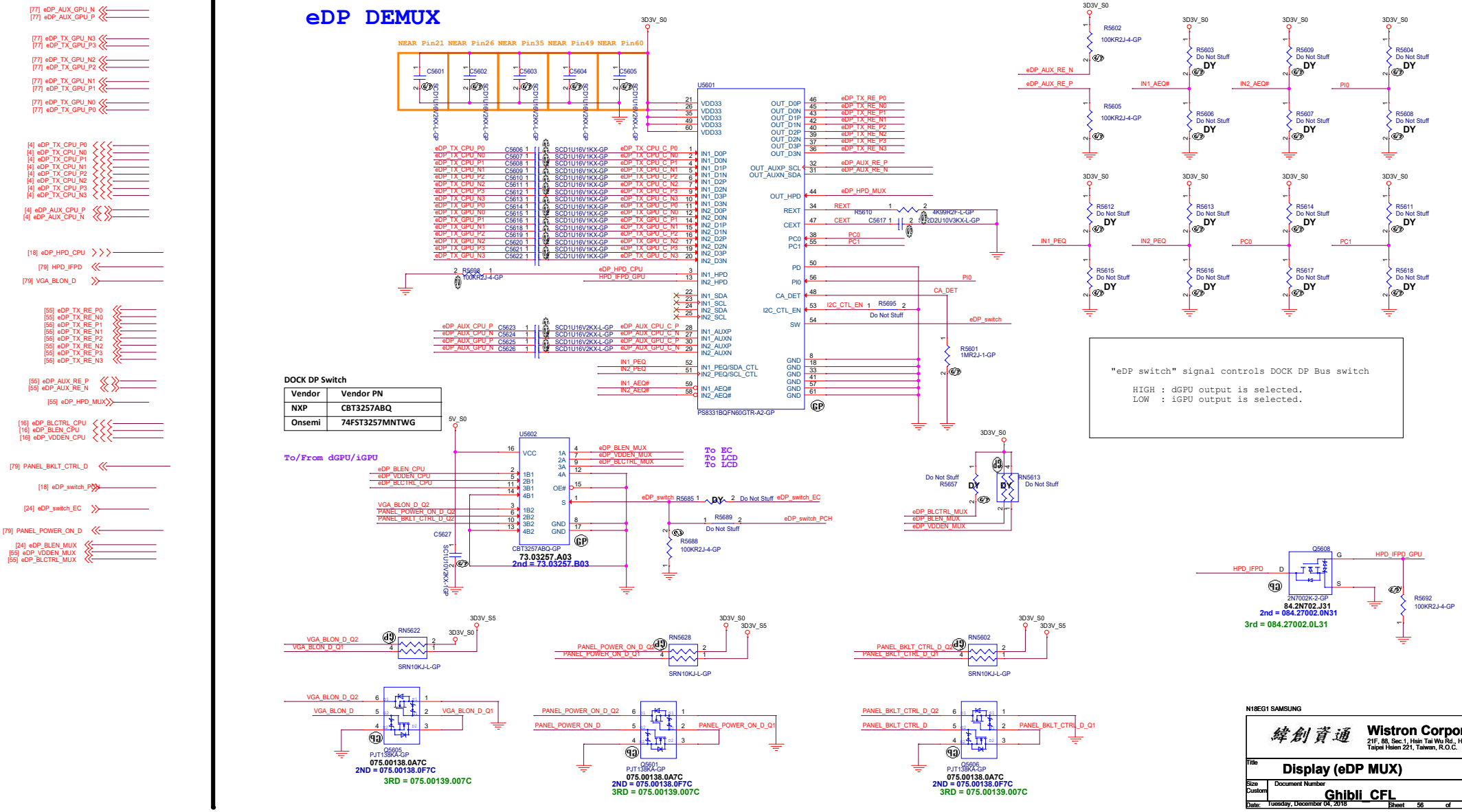
eDP DEMUX



DOCK DP Switch

Vendor	Vendor PN
NXP	CBT3257ABQ
Onsemi	74FST3257MNTWG

N18EG1 SAMSUNG

Wistron Corporation
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Title: **Display (eDP MUX)**

Size: Custom | Document Number: Ghibli_CFL | Rev: SC

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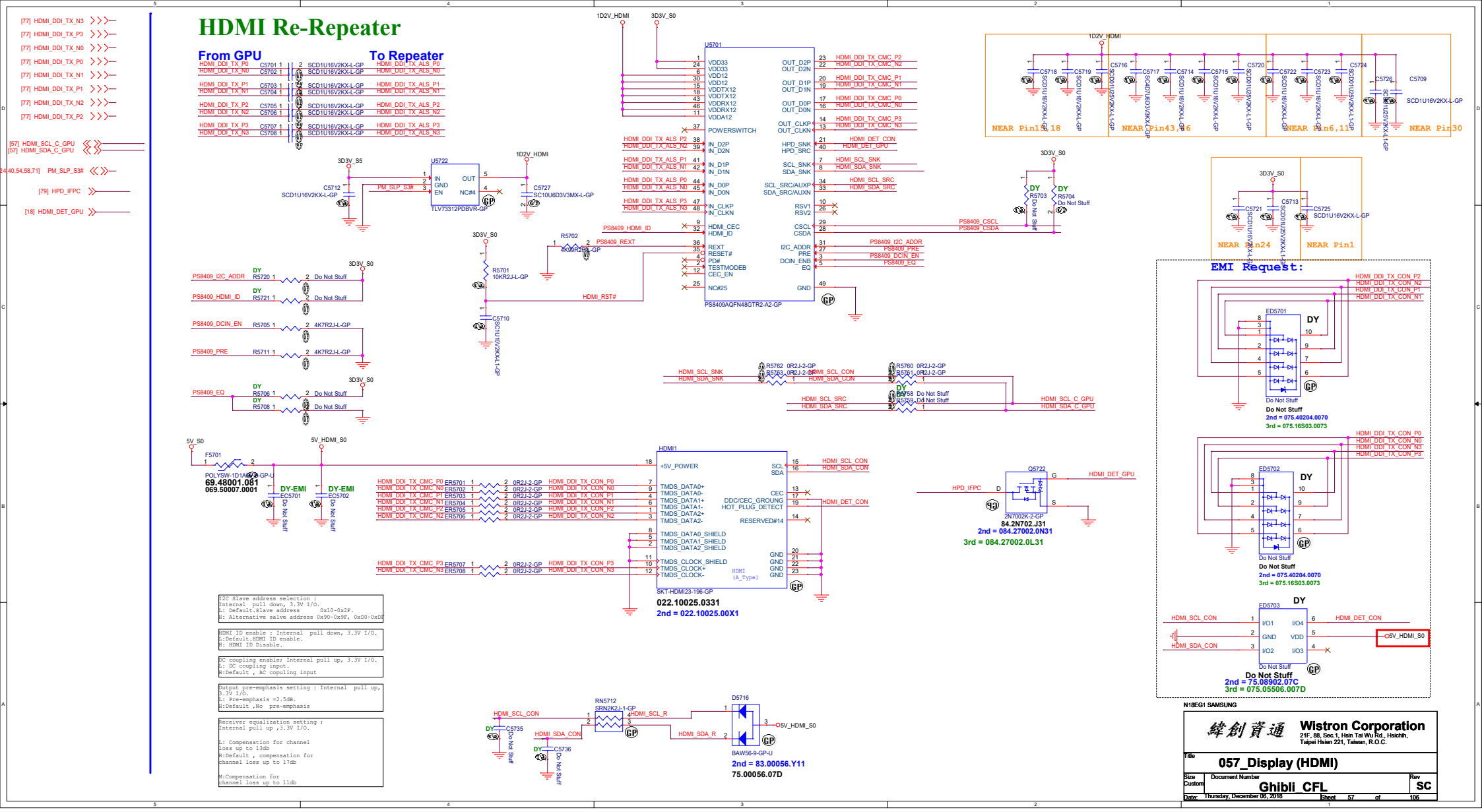
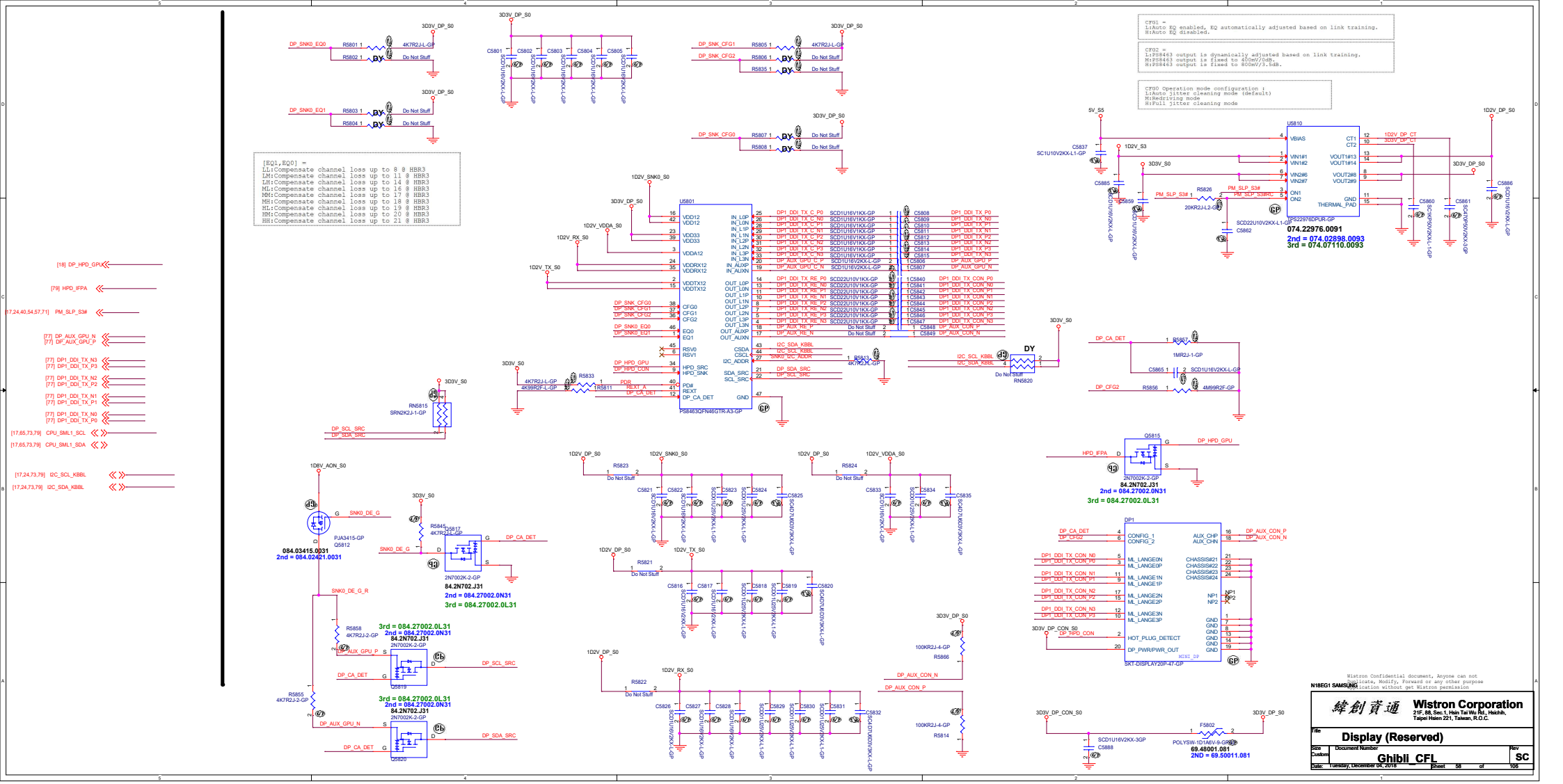
HDMI Re-Repeater




CFG1 =
L:Auto EQ enabled, EQ automatically adjusted based on link training.
H:Auto EQ disabled.
CFG2 =
L:PS8463 output is dynamically adjusted based on link training.
M:PS8463 output is fixed to 400mV/0dB.
H:PS8463 output is fixed to 800mV/3.5dB.
CFG0 Operation mode configuration :
L:Auto jitter cleaning mode (default)
M:Redriving mode
H:Full jitter cleaning mode
[EQ1,EQ0] =
LL:Compensate channel loss up to 8 @ HBR3
LM:Compensate channel loss up to 11 @ HBR3
LH:Compensate channel loss up to 14 @ HBR3
ML:Compensate channel loss up to 16 @ HBR3
MM:Compensate channel loss up to 17 @ HBR3
MH:Compensate channel loss up to 18 @ HBR3
HL:Compensate channel loss up to 19 @ HBR3
HM:Compensate channel loss up to 20 @ HBR3
HH:Compensate channel loss up to 21 @ HBR3
U5801
PS8463QFN46GTR-A3-GP
U5810
TPS22976DPUR-GP
074.22976.0091
2nd = 074.02898.0093
3rd = 074.07110.0093
DP1
SKT-DISPLAY20P-47-GP
Q5815
2N7002K-2-GP
84.2N702.J31
2nd = 084.27002.0N31
3rd = 084.27002.0L31
Q5812
PJA3415-GP
084.03415.0031
2nd = 084.02421.0031
Q5817
Q5819
Q5820
F5802
POLYSW-1D1A6V-9-GP
69.48001.081
2ND = 69.50011.081
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Title
Display (Reserved)
Size Custom
Document Number
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N18EG1 SAMSUNG

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title **Display (Reserved)**

Size	Document Number	Rev
A	Ghibli_CFL	SC

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SSID = Wireless

N18EG1 SAMSUNG

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Title	INT IO (RSVD)	
Size A	Document Number Ghibli_CFL	Rev SC
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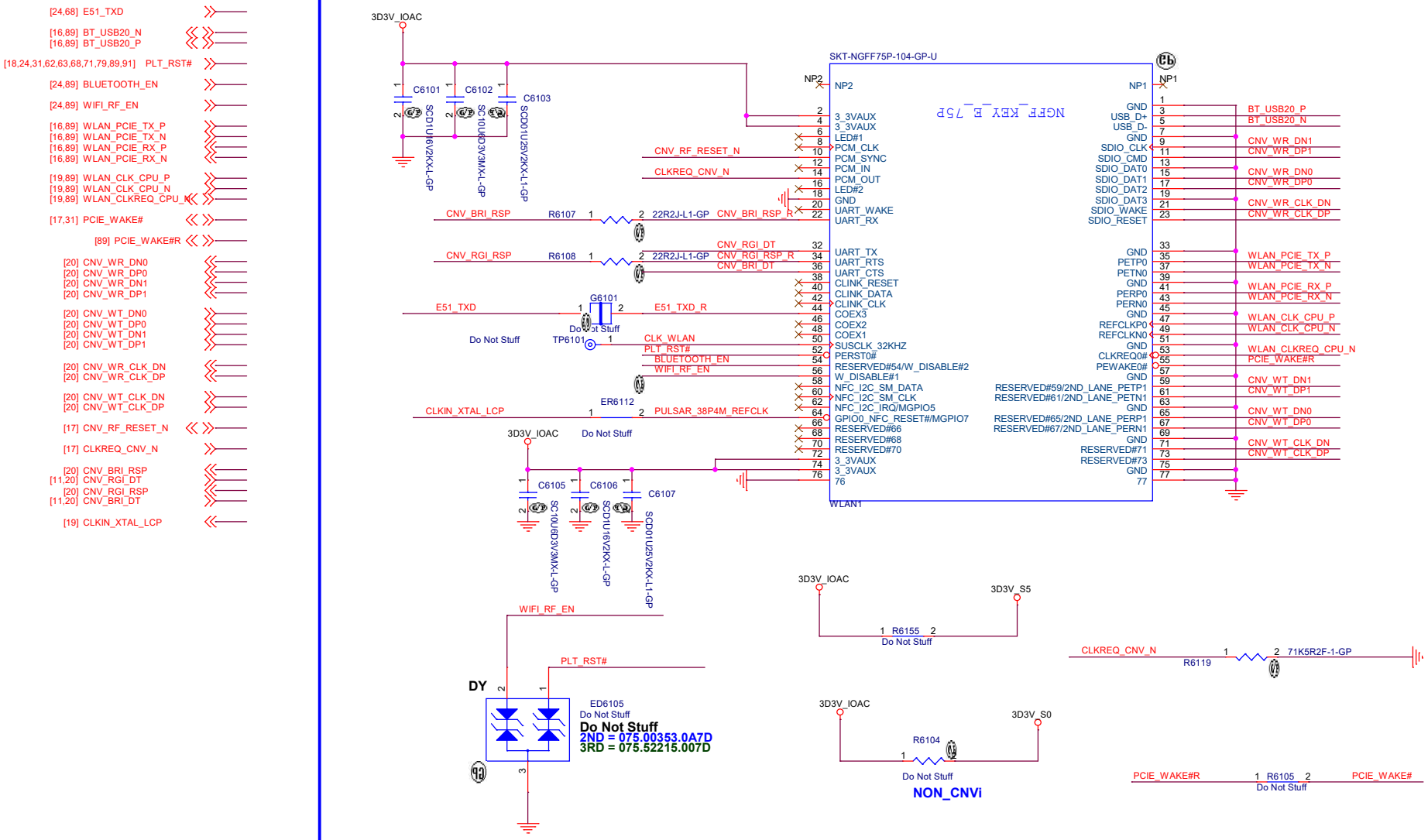
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



N18EG1 SAMSUNG

Wistron Corporation
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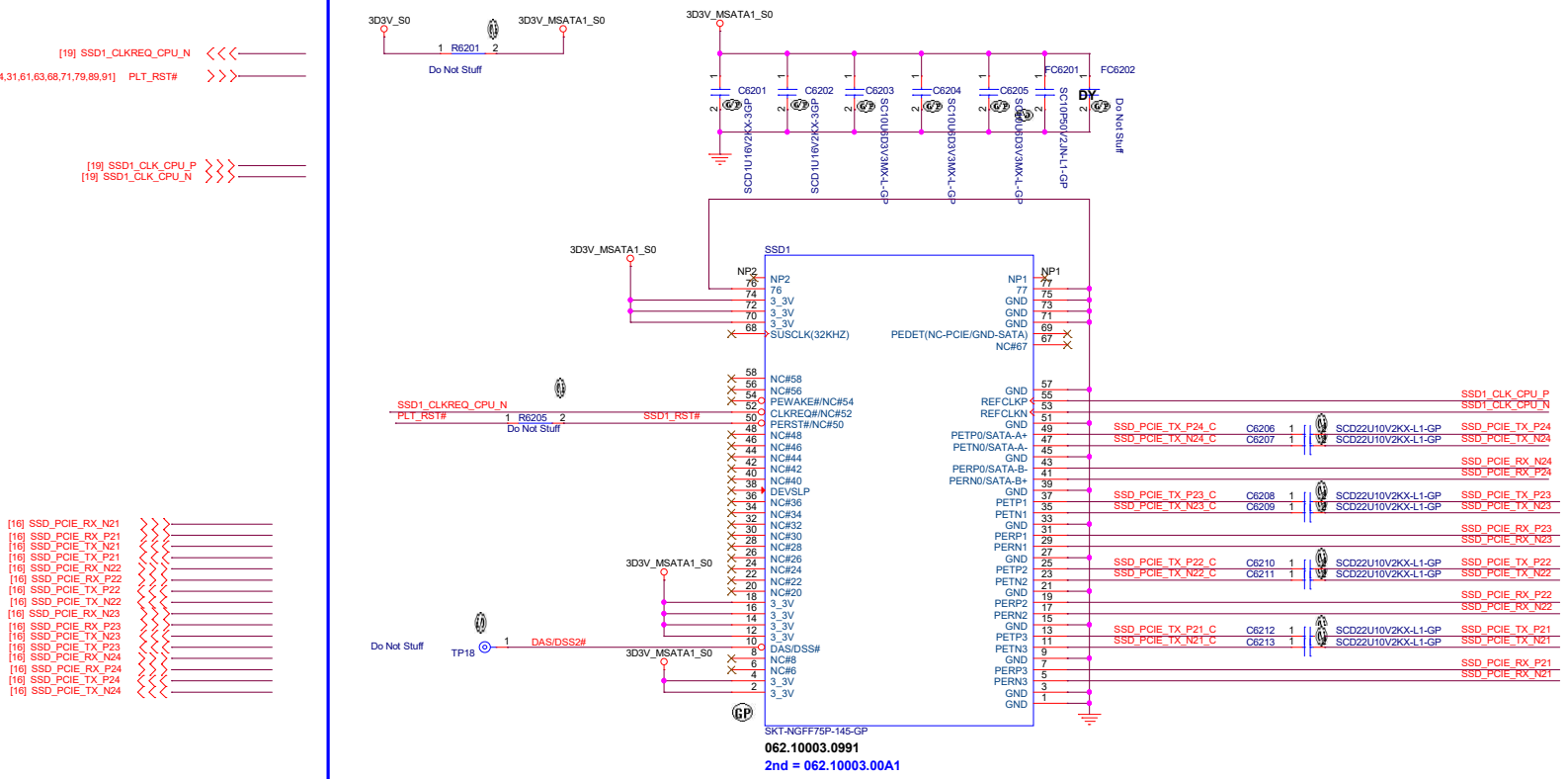
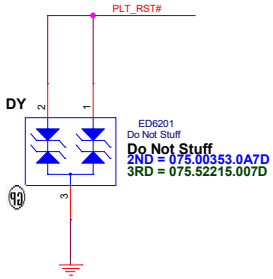
Title: Block Diagram

Size: A3 | Document Number: Ghibli_CFL | Rev: SC

Date: Tuesday, December 04, 2018 | Sheet 61 of 106

SSID = mSATA Mini Card Connector (NGFF m-SATA)





Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer tChapter 3, "General Differential Signals Design Guidelines" " along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration where the motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

N18EG1 SAMSUNG

緯創資通 Wistron Corporation
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Title: INT IO (SSD-NGFF-1)

Size: Custom | Document Number: Ghibli_CFL | Rev: SC

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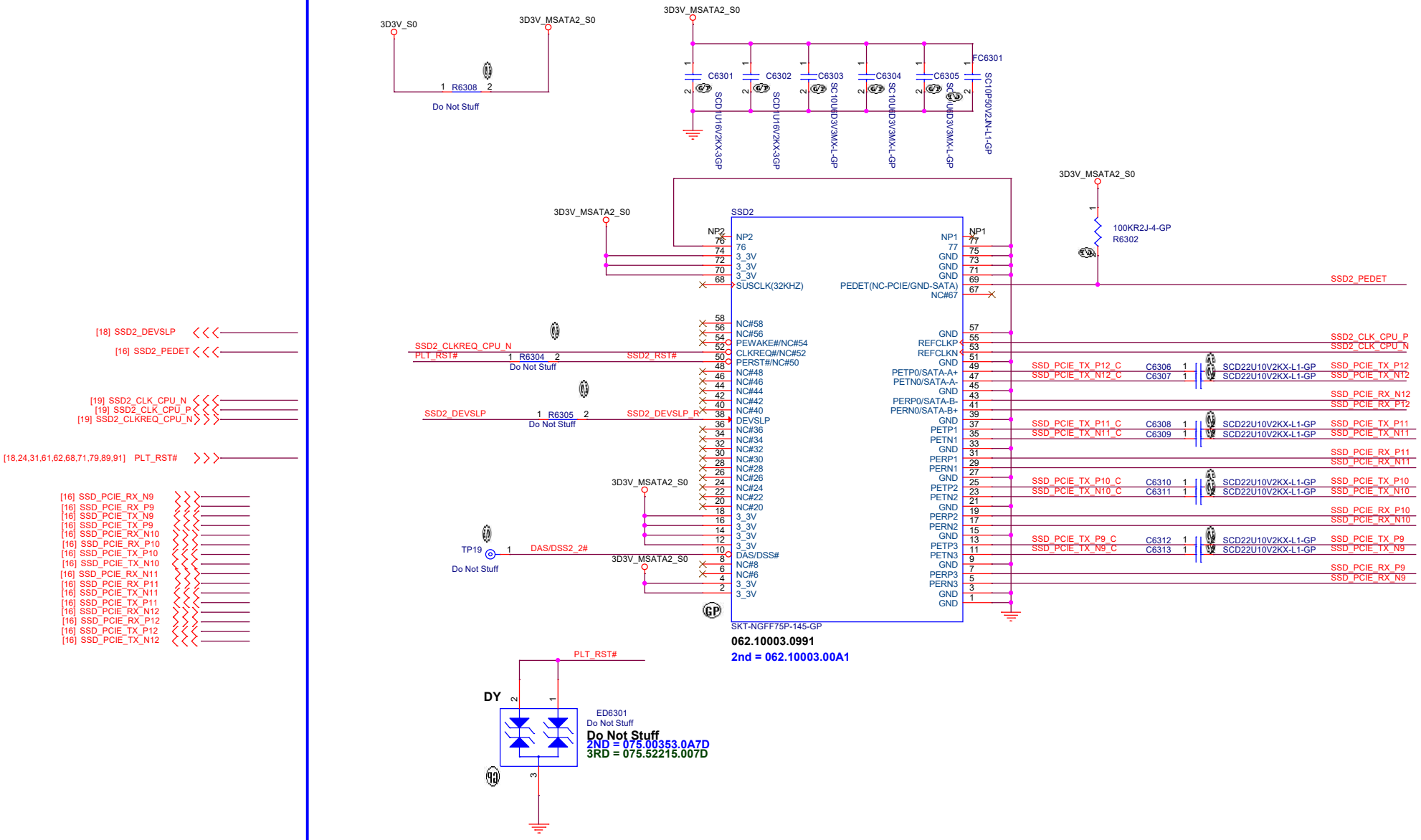
SSID = mSATA



N18EG1 SAMSUNG

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**INT IO (SSD-NGFF-2)**	
Size A3	Document Number **Ghibli_CFL**	Rev **SC**
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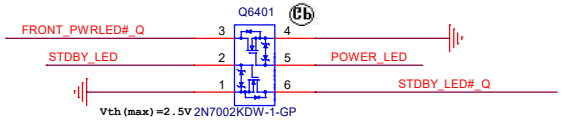
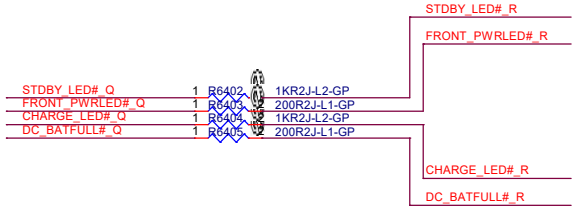
Power button LED

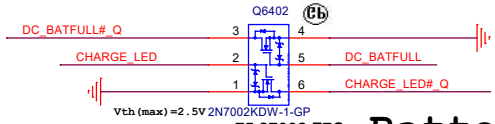


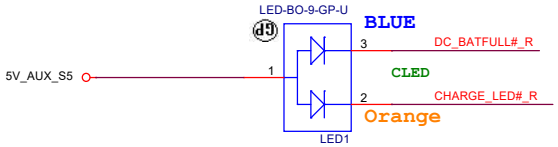


Power STDBY_LED

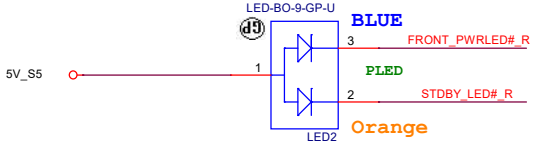
[24] DC_BATFULL
[24] POWER_LED
[24] STDBY_LED
[24] CHARGE_LED
[24,89] TURBO_KEY
[24,89] TURBO_LED
[24,65,89] KBC_PWRBTN#

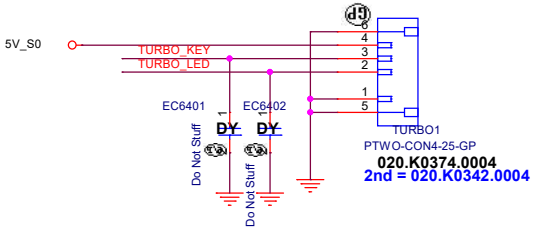
Battery LED2(DC_BATFULL)

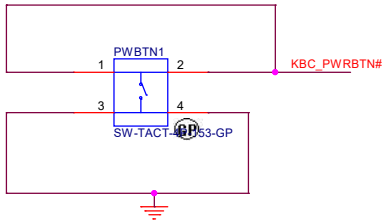




Battery LED1(CHARGE)







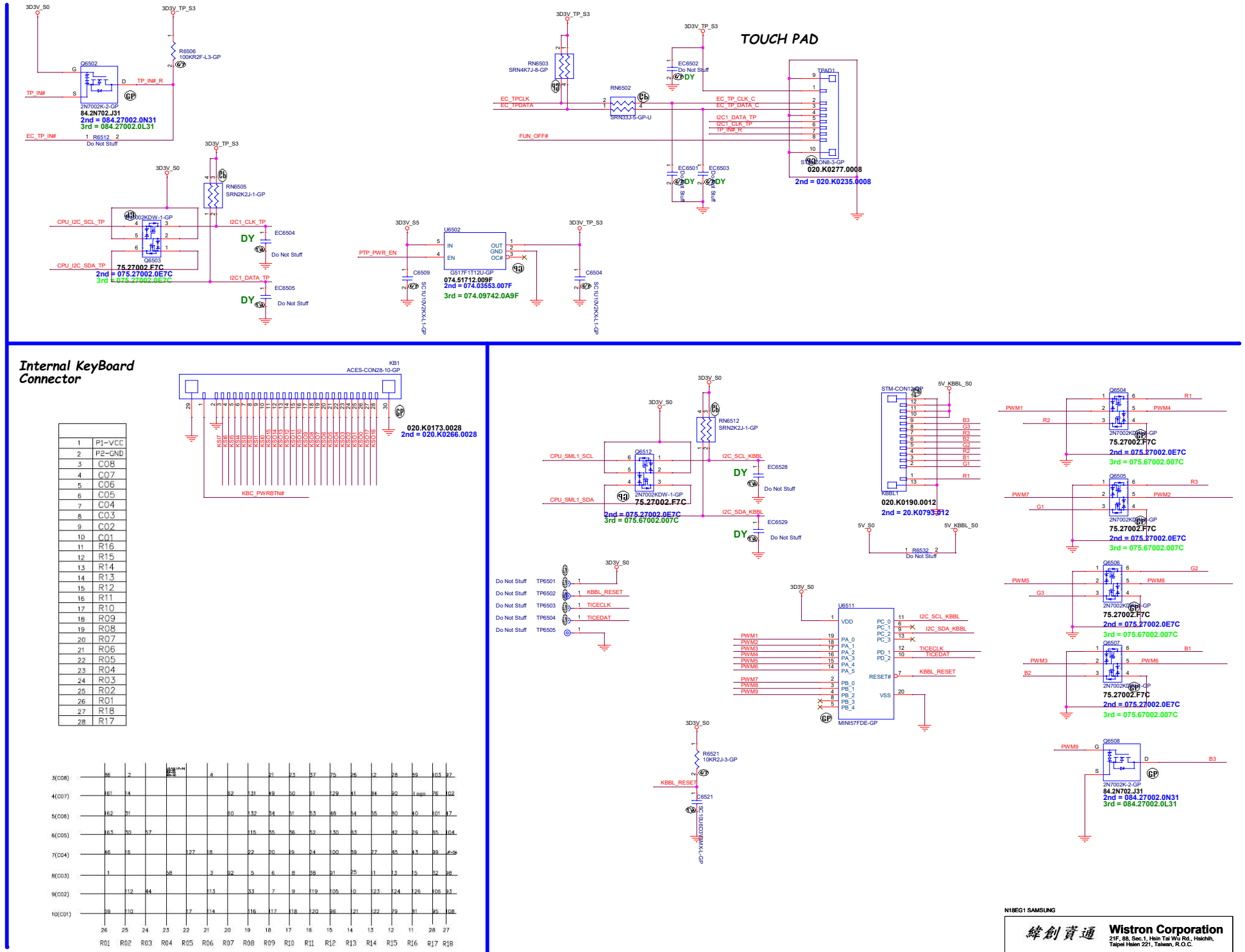
N18EG1 SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED / Button / Power Button

Size: A3 | Document Number: Ghibli_CFL | Rev: SC

Date: Tuesday, December 04, 2018 | Sheet 64 of 106



1	P1-VCC
2	P2-GND
3	CO8
4	CO7
5	CO6
6	CO5
7	CO4
8	CO3
9	CO2
10	CO1
11	R16
12	R15
13	R14
14	R13
15	R12
16	R11
17	R10
18	R09
19	R08
20	R07
21	R06
22	R05
23	R04
24	R03
25	R02
26	R01
27	R18
28	R17

N18EG1 SAMSUNG

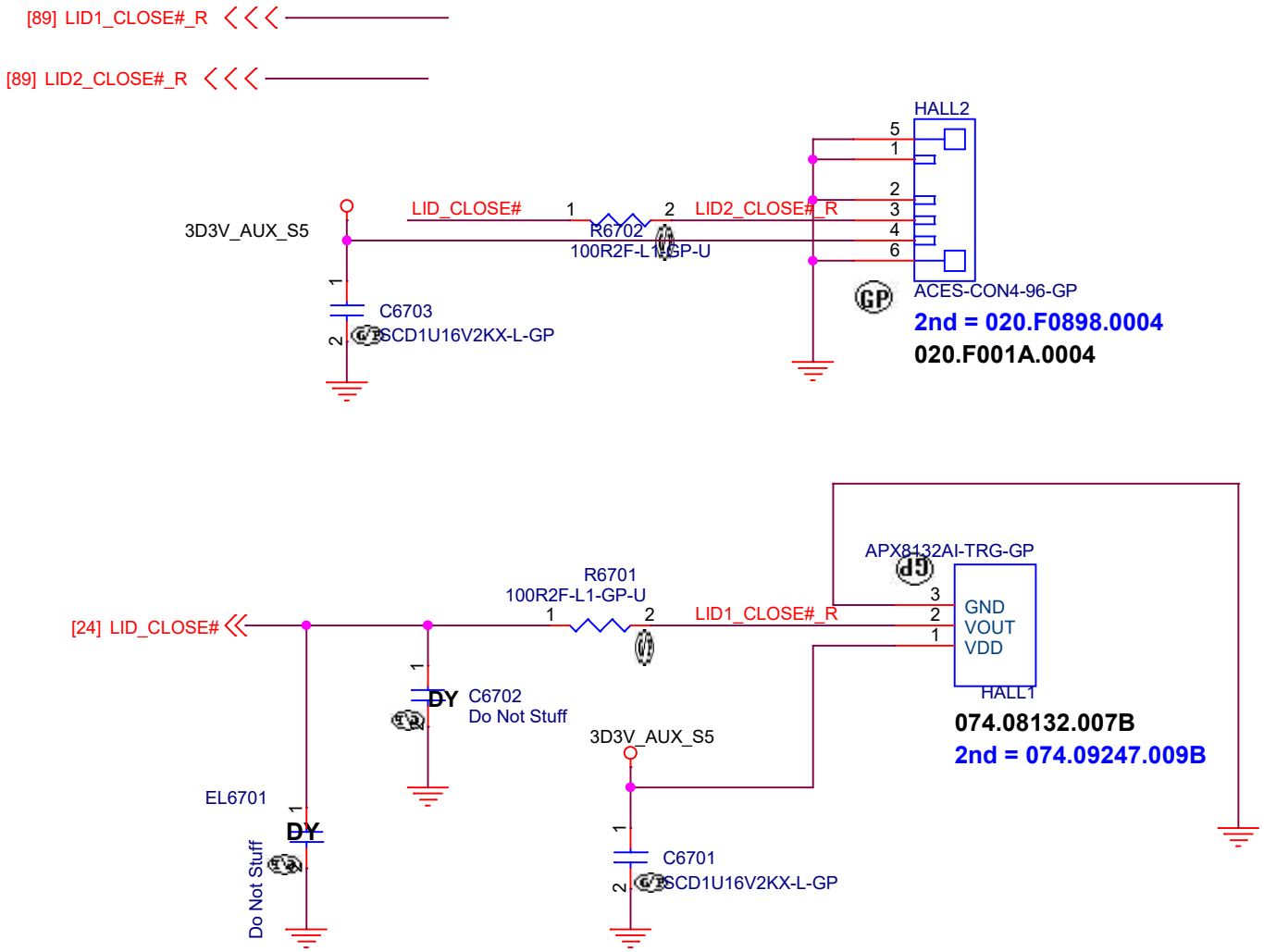
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
IO Board Conn (RSVD)

Size	Document Number	Rev
A	Ghibli_CFL	SC

Date: Monday, December 03, 2018 Sheet 66 of 106

Main Func = Hall Sensor

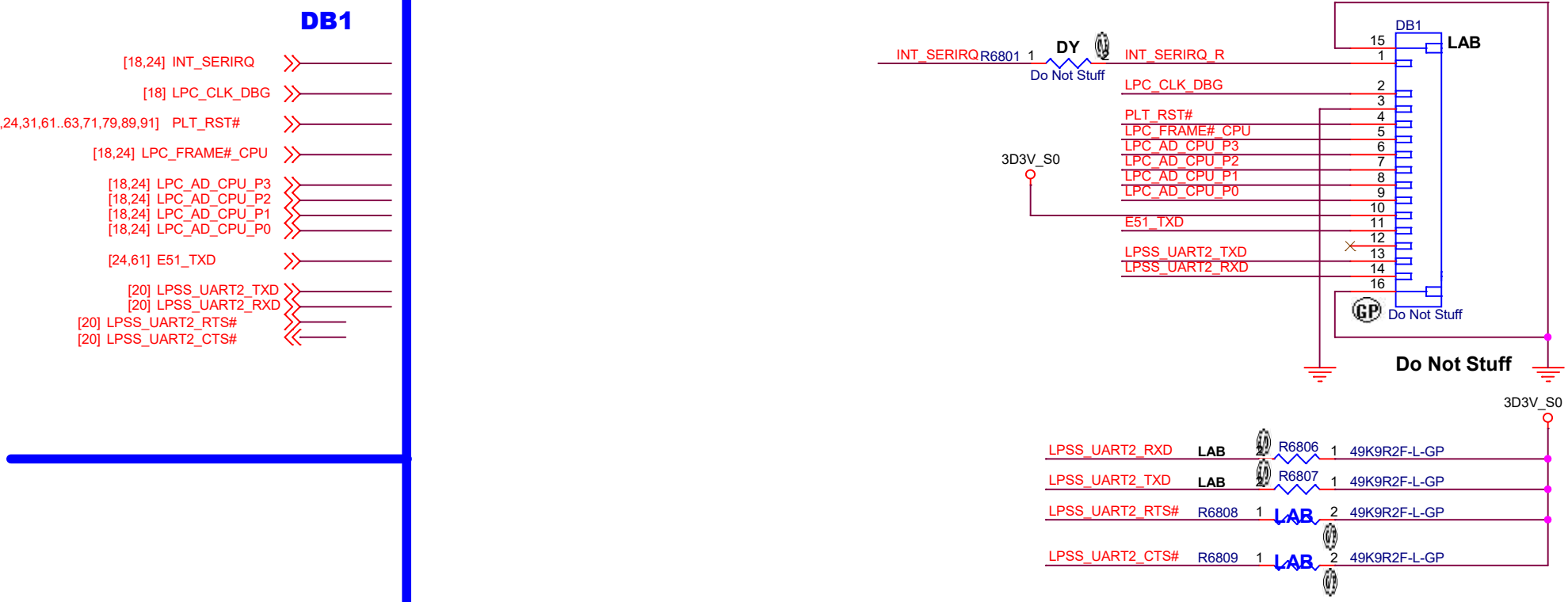


N18EG1 SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**Sensor (Hall-Sensor)**	
Size A	Document Number **Ghibli_CFL**	Rev **SC**
Date: Tuesday, December 04, 2018	Sheet 67 of 106	

Main Func = Debug



N18EG1 SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Debug (LPC debug)**

Size	Document Number	Rev
A4	Ghibli_CFL	SC

Date: Tuesday, December 04, 2018 Sheet 68 of 106

N18EG1 SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

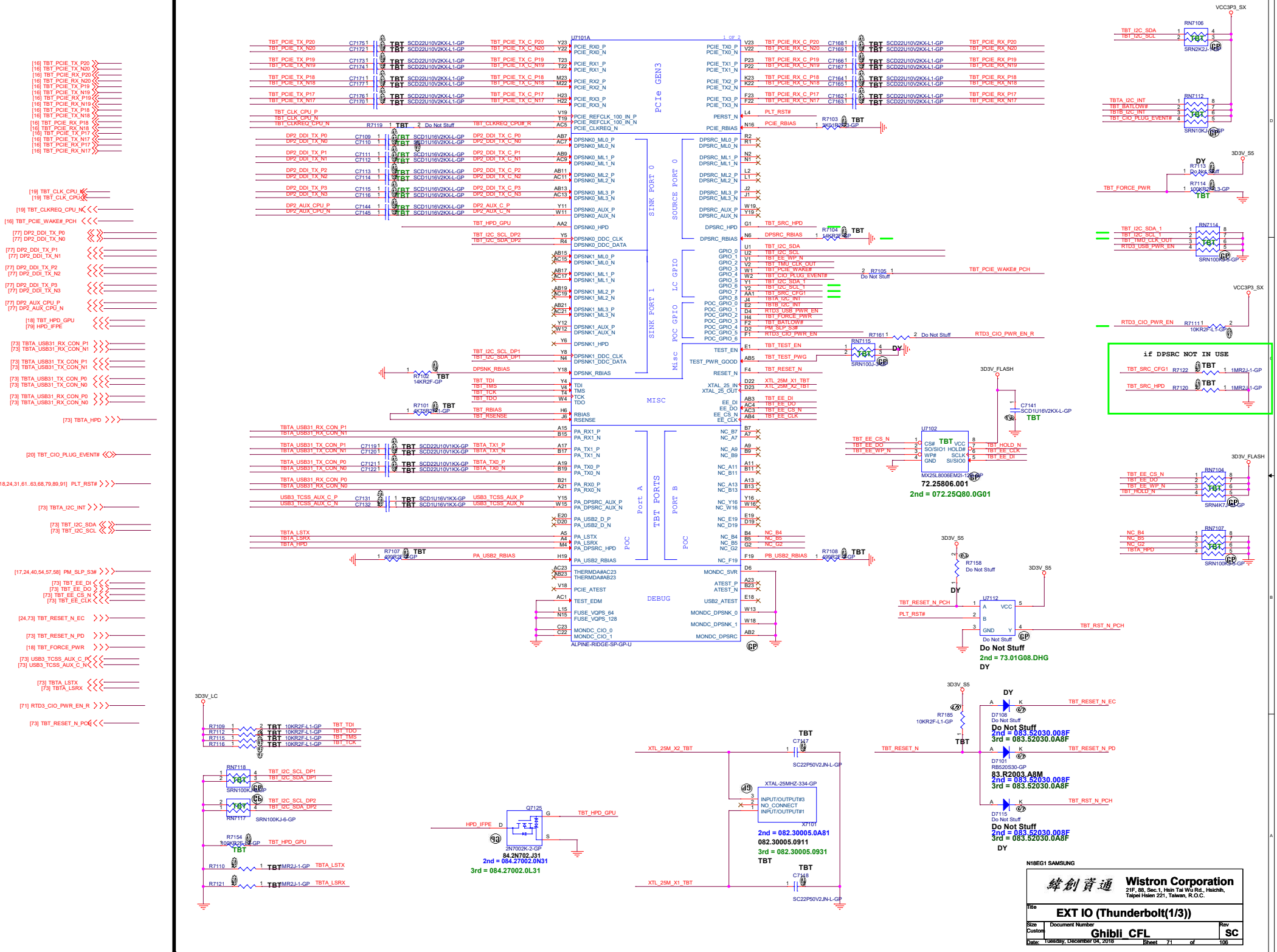
Title	Sensor (RSVD)	
Size A4	Document Number Ghibli_CFL	Rev SC
Date: Monday, December 03, 2018	Sheet 69 of 106	

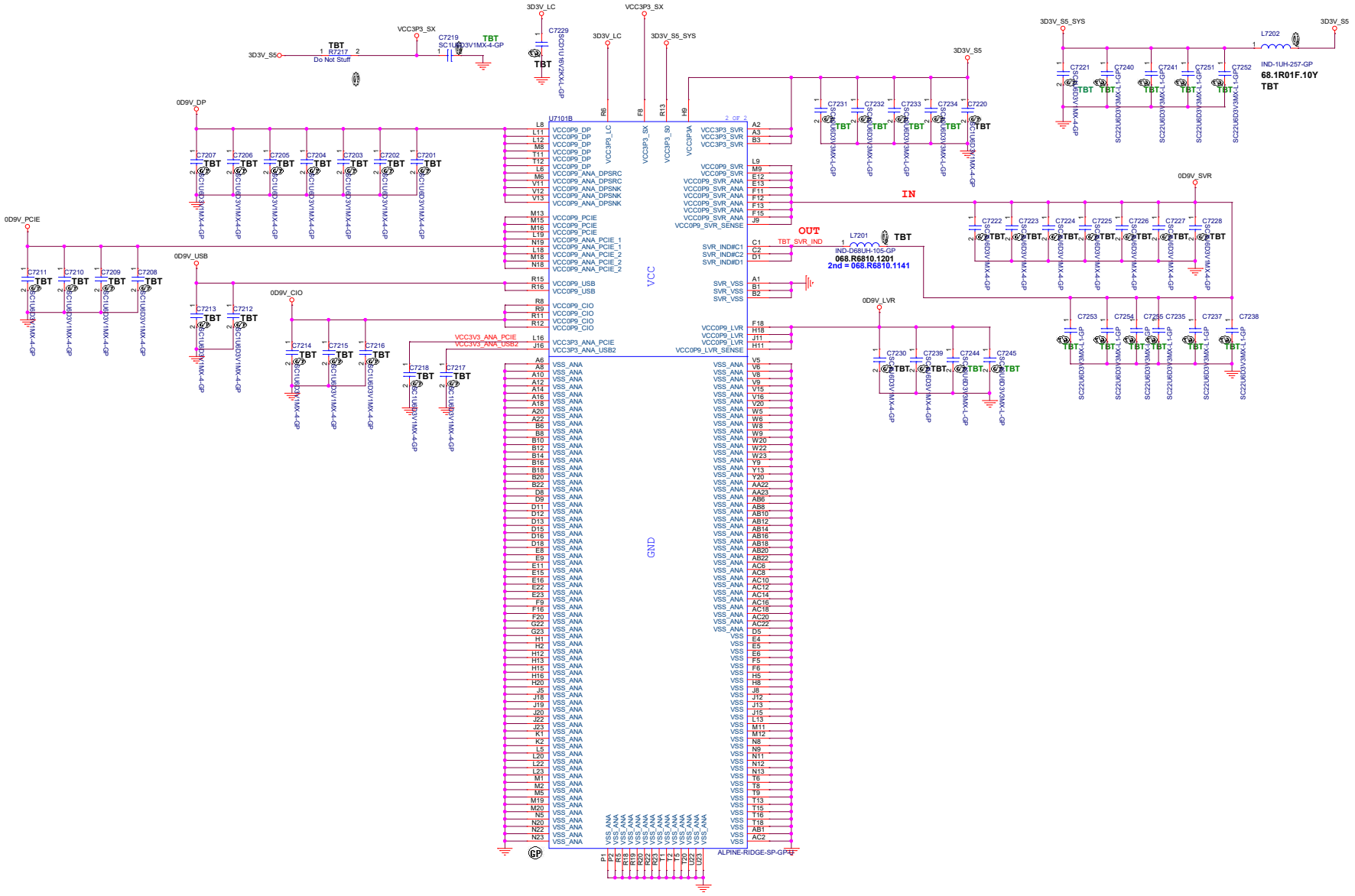
Main Func = Free Fall Sensor

N18EG1 SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Sensor (RSVD)	
Size A4	Document Number Ghibli_CFL	Rev SC
Date: Monday, December 03, 2018	Sheet 70 of 106	


U7101A
ALPINE-RIDGE-SP-GP-U
PCIe GEN3
SINK PORT 0
SOURCE PORT 0
LC GPIO
SINK PORT 1
POC GPIO
Misc
MISC
TBT PORTS
Port A
PORT B
POC
DEBUG
if DPSRC NOT IN USE
U7102
MX25L8006EM2I-12G-GP
72.25806.001
2nd = 072.25Q80.0G01
U7112
Do Not Stuff
2nd = 73.01G08.DHG
DY
Q7125
2N7002K-2-GP
84.2N702.J31
2nd = 084.27002.0N31
3rd = 084.27002.0L31
XTAL-25MHZ-334-GP
X7101
2nd = 082.30005.0A81
082.30005.0911
3rd = 082.30005.0931
D7108
D7101
RB520S30-GP
83.R2003.A8M
2nd = 083.52030.008F
3rd = 083.52030.0A8F
D7115
N18EG1 SAMSUNG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
EXT IO (Thunderbolt(1/3))
Size Custom
Document Number
Ghibli_CFL
Rev
SC
Date: Tuesday, December 04, 2018
Sheet 71 of 106



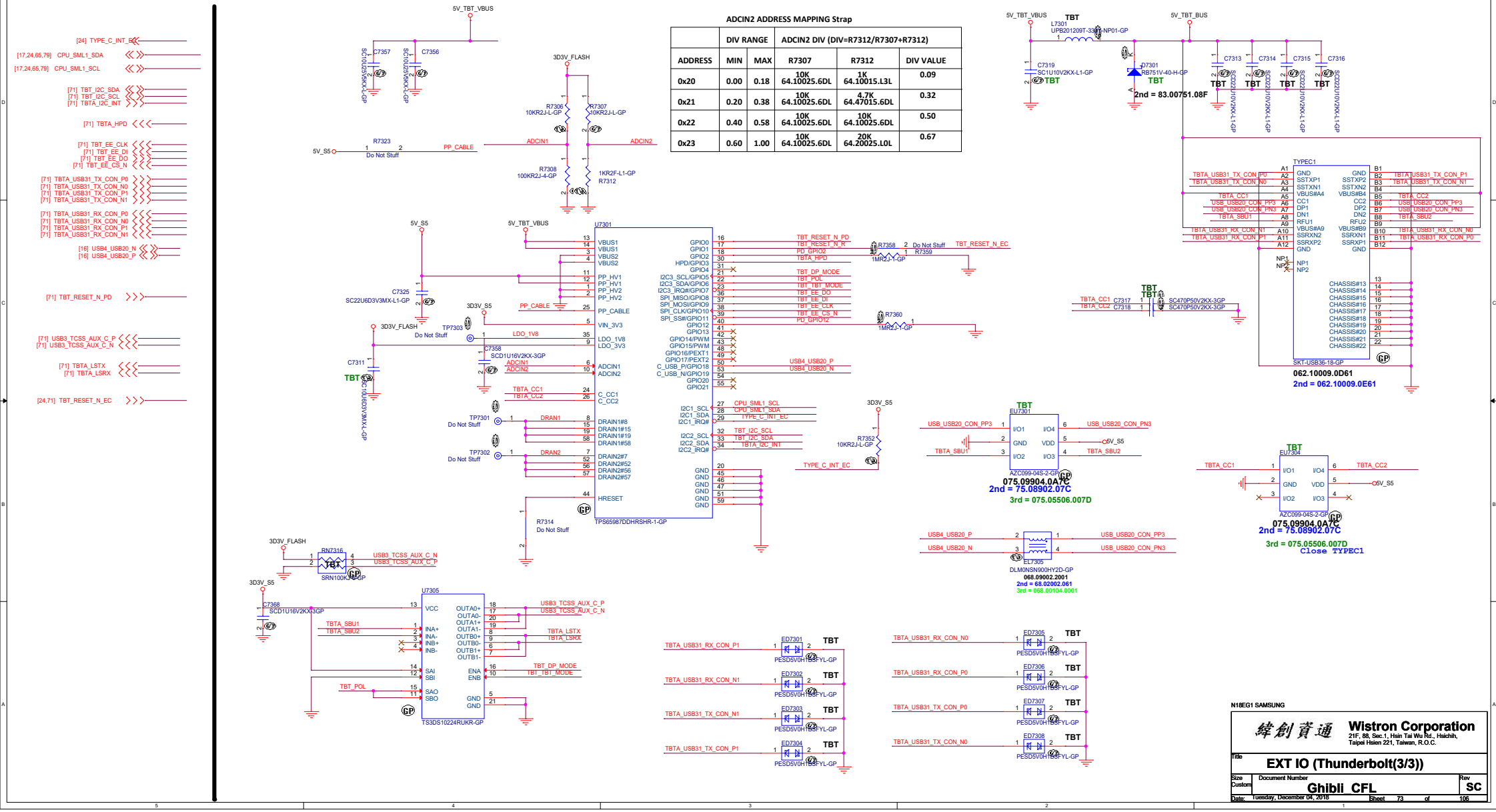
N18EG1 SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **EXT IO (Thunderbolt(2/3))**

Size	Document Number	Rev
A2	Ghibli_CFL	SC

Date: Tuesday, December 04, 2018 Sheet 72 of 106



ADCIN2 ADDRESS MAPPING Strap

	DIV RANGE		ADCIN2 DIV (DIV=R7312/R7307+R7312)		
ADDRESS	MIN	MAX	R7307	R7312	DIV VALUE
0x20	0.00	0.18	10K 64.10025.6DL	1K 64.10015.L3L	0.09
0x21	0.20	0.38	10K 64.10025.6DL	4.7K 64.47015.6DL	0.32
0x22	0.40	0.58	10K 64.10025.6DL	10K 64.10025.6DL	0.50
0x23	0.60	1.00	10K 64.10025.6DL	20K 64.20025.L0L	0.67

N18EG1 SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **EXT IO (Thunderbolt(3/3))**

Size: Custom | Document Number: **Ghibli_CFL** | Rev: **SC**

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N18EG1 SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (VBUS)

Size	Document Number	Rev
Custom	Ghibli_CFL	SC

Date: Monday, December 03, 2018 Sheet 74 of 106

N18EG1 SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	EXT IO (RSVD)	
Size A4	Document Number Ghibli_CFL	Rev SC
Date: Monday, December 03, 2018	Sheet 75 of 106	

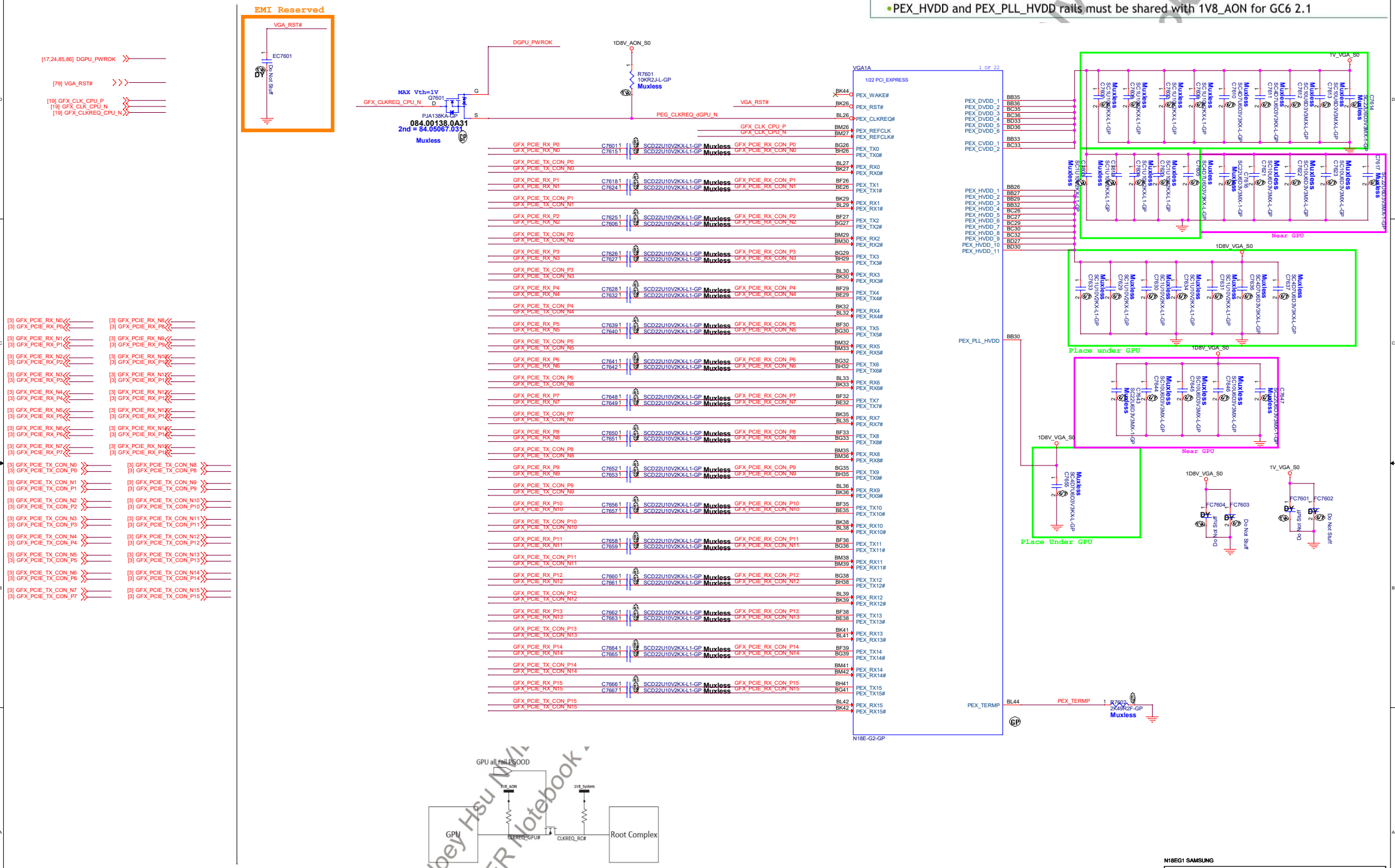
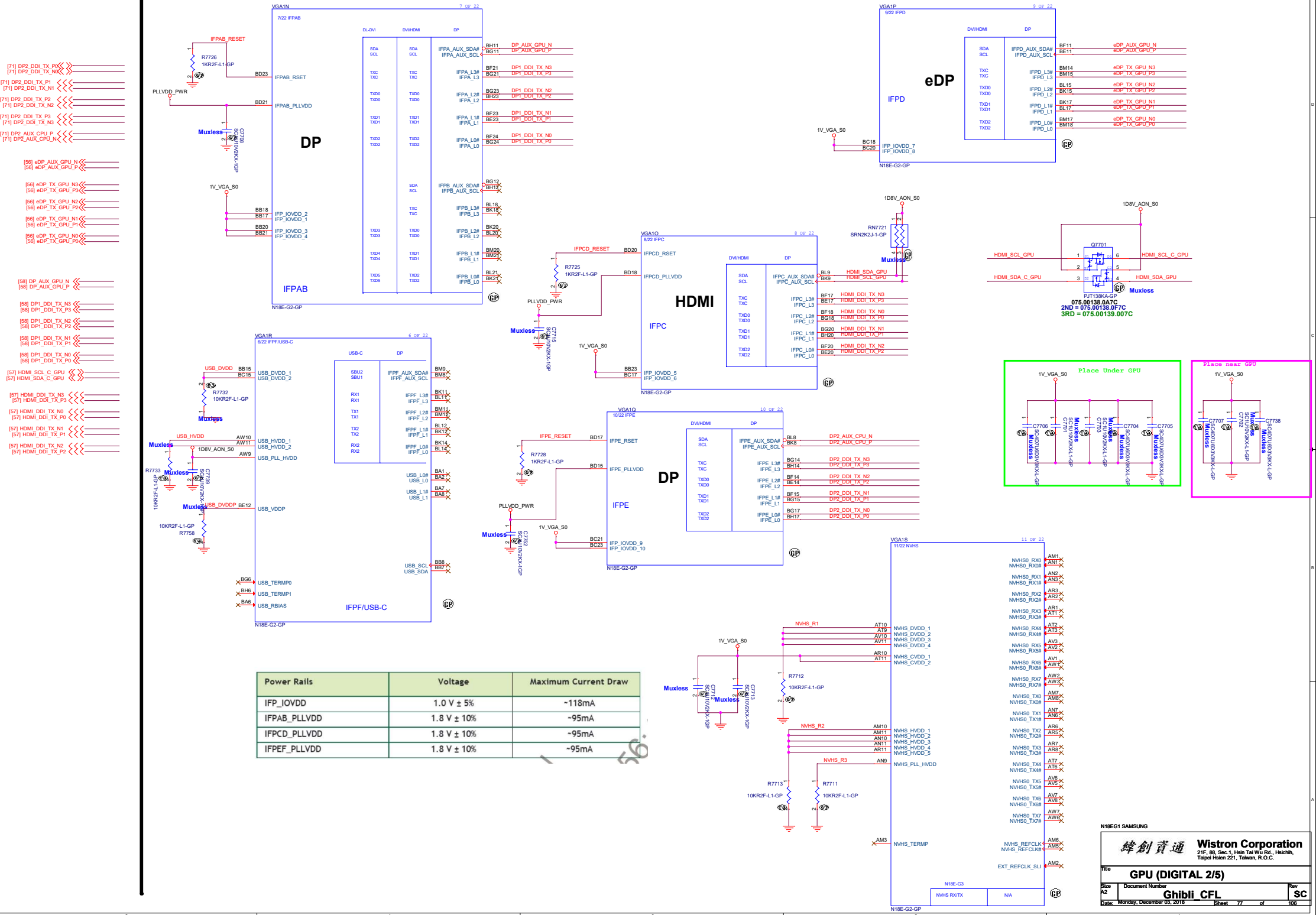


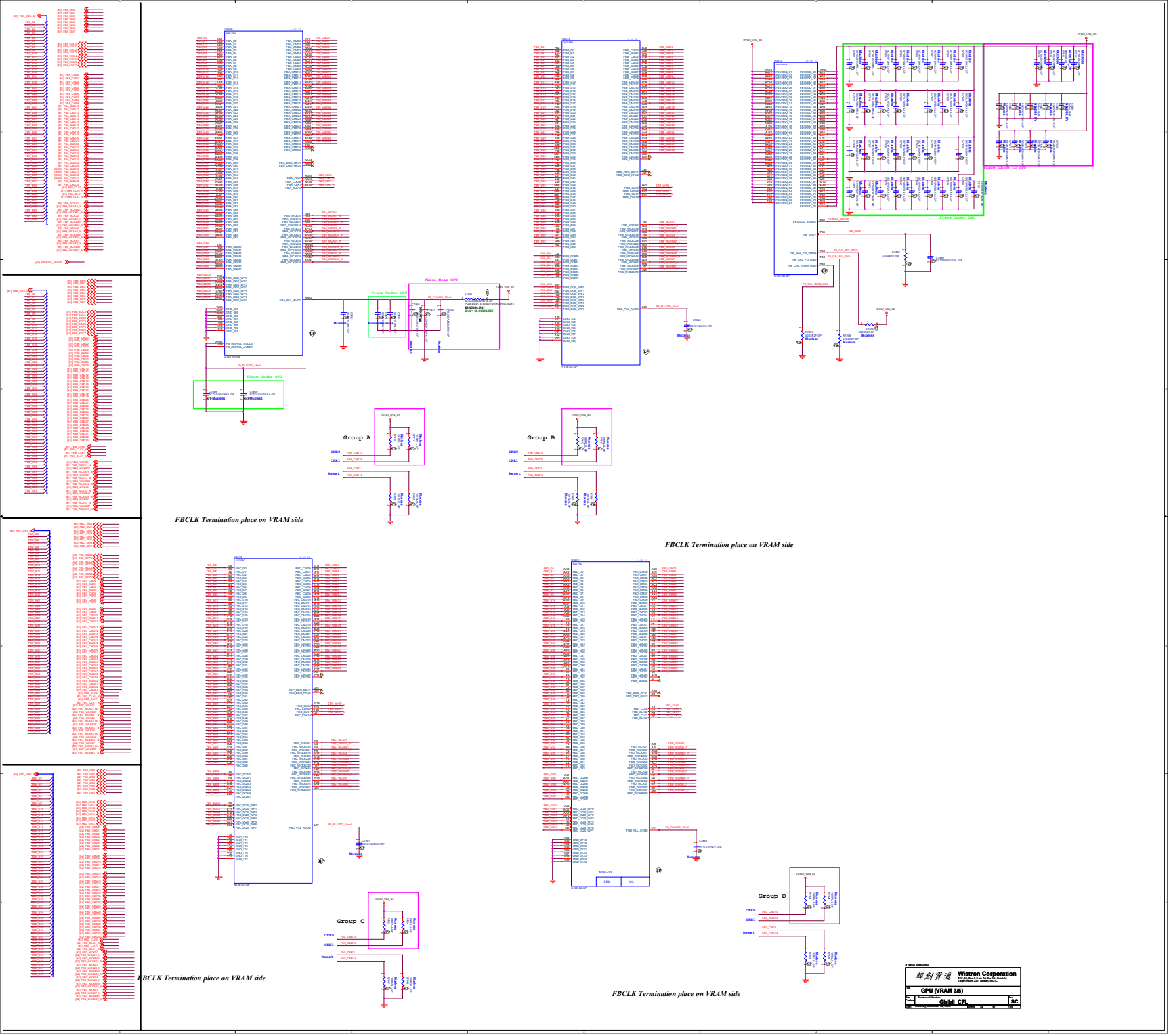
Figure 8.8 PEX_CLKREQ# Isolation Circuitry

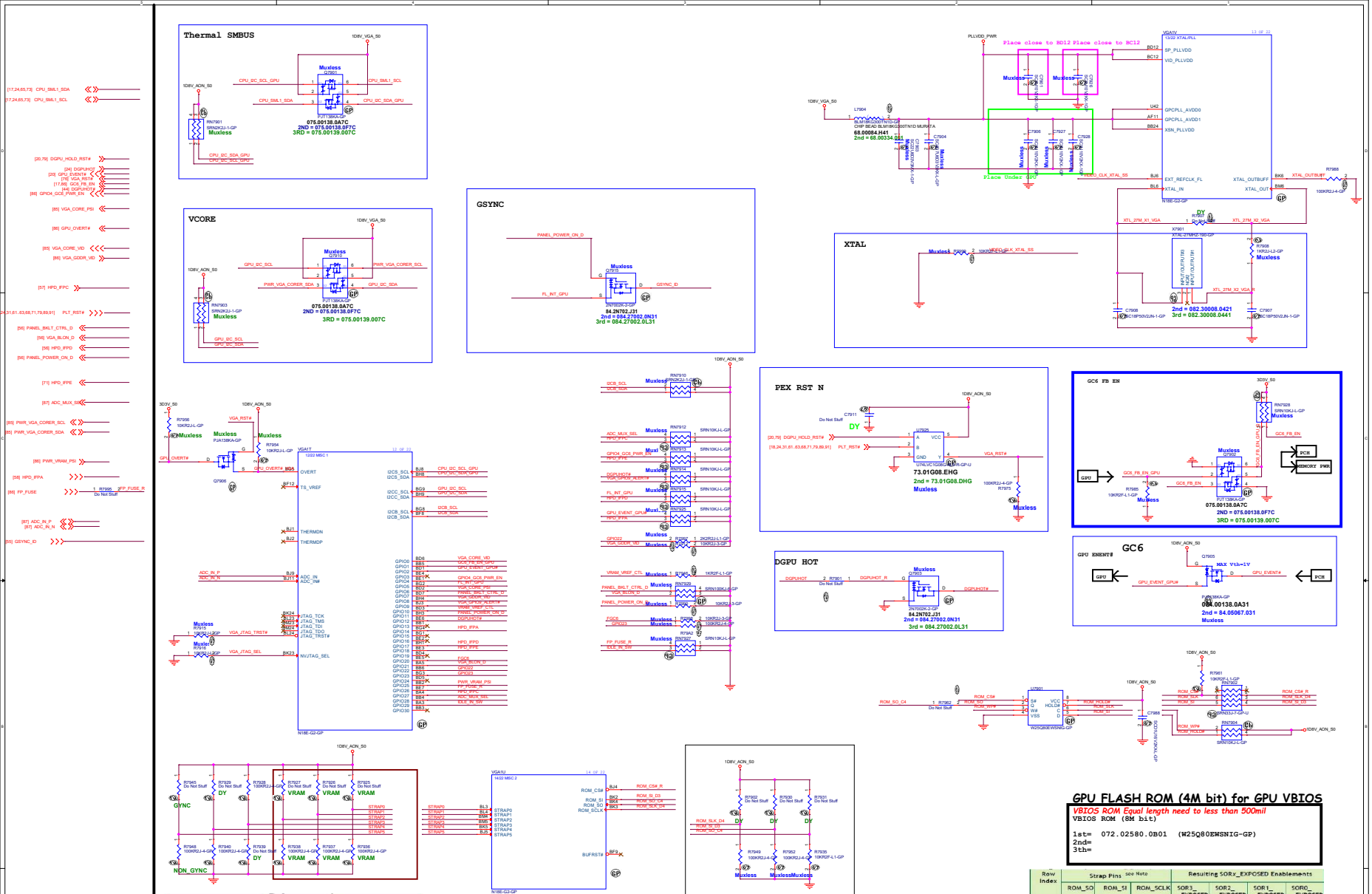
N18EG1 SAMSUNG

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	GPU (PEG 1/5)	
Size A2	Document Number Ghibli_CFL	Rev SC
Date: Tuesday, December 04, 2018	Sheet 76 of 106	



Power Rails	Voltage	Maximum Current Draw
IFP_IOVDD	1.0 V ± 5%	~118mA
IFPAB_PLLVDD	1.8 V ± 10%	~95mA
IFPCD_PLLVDD	1.8 V ± 10%	~95mA
IFPEF_PLLVDD	1.8 V ± 10%	~95mA


Group A
Group B
Group C
Group D
Place Under GPU
Place Near GPU
Place Close to GPU
FBCLK Termination place on VRAM side
FBCLK Termination place on VRAM side
FBCLK Termination place on VRAM side
FBCLK Termination place on VRAM side
Wistron Corporation
GPU (VRAM 3/5)
Ghibli CFL
SC



GPU FLASH ROM (4M bit) for GPU VBIOS

VBIOS ROM Equal length need to less than 500mil

VBIOS ROM (8M bit)

1st= 072.02580.0B01 (W25Q80EWSNIG-GP)
2nd=
3th=

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	disabled	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
11	H	L	L	ENABLED	disabled	ENABLED	ENABLED
10	H	L	H	ENABLED	disabled	ENABLED	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V[2]	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

Notes:
1. For N18E-G3, the maximum allowable memory case temperature is 95 °C.
2. DVS is required. WCK: TBD

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V[2]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

Notes:
1. For N18E-G2/G1, the maximum allowable memory case temperature is 95 °C.
2. DVS is required. WCK: TBD

Micron AC/DP Note
NVIDIA Confidential
2018-08-31 18:41:05

N18EG1 SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

GPU (GPIO 4/5)

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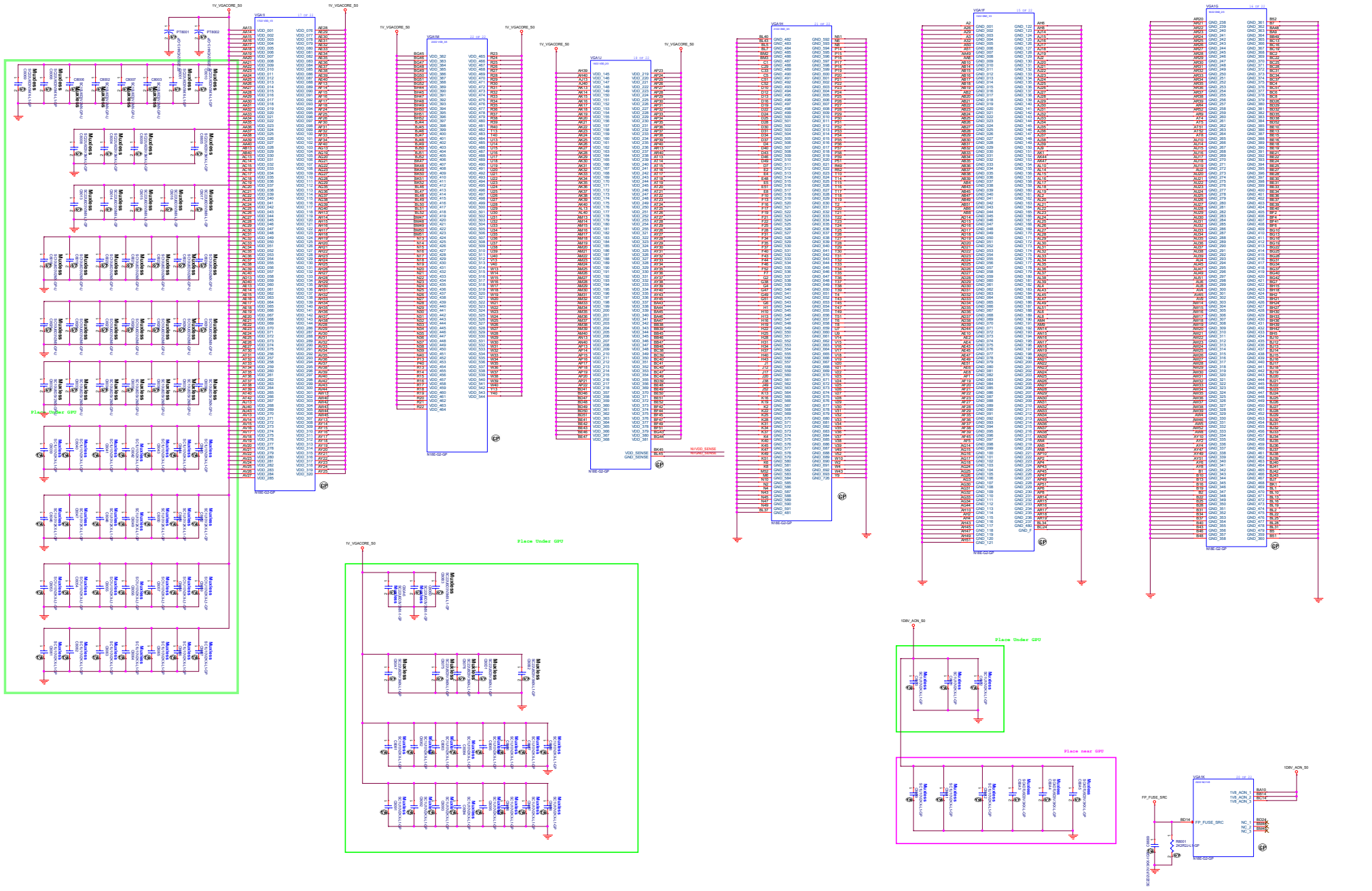

NBEG1 SAMSUNG

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**GPU (PWR/GND 5/5)**	
Size: Custom	Document Number: **Ghibli_CFL**	Rev: **SC**
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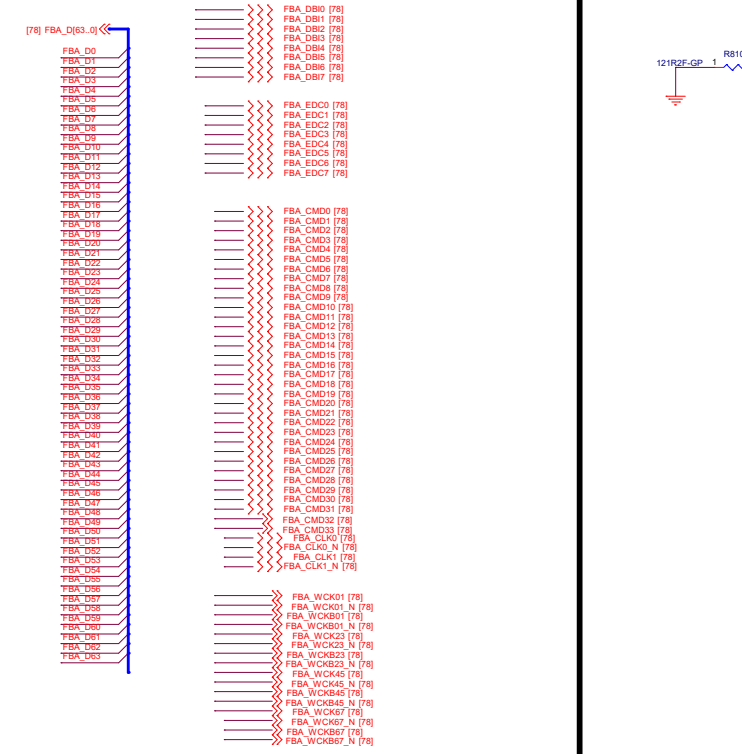

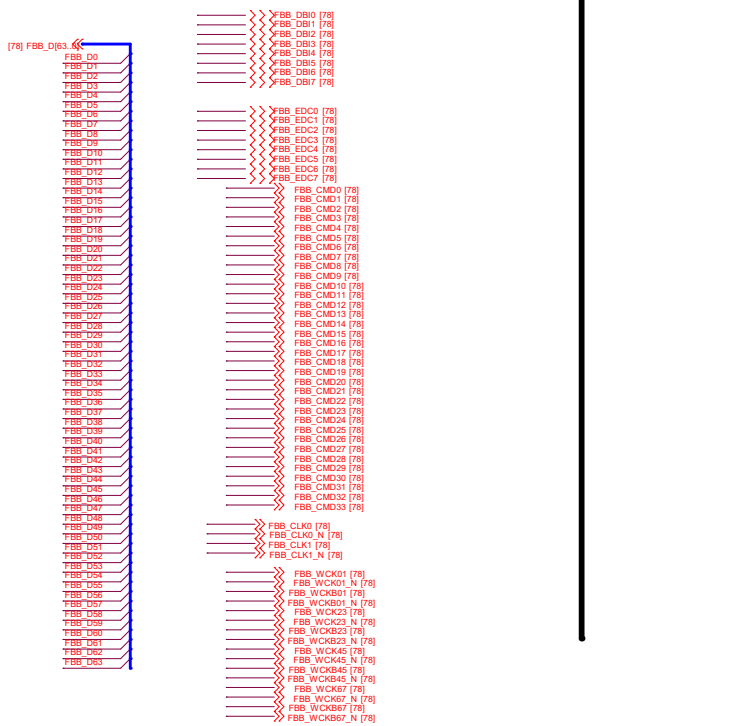

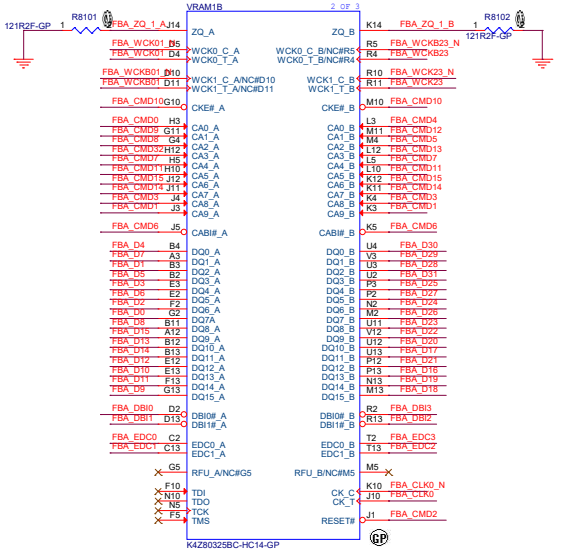

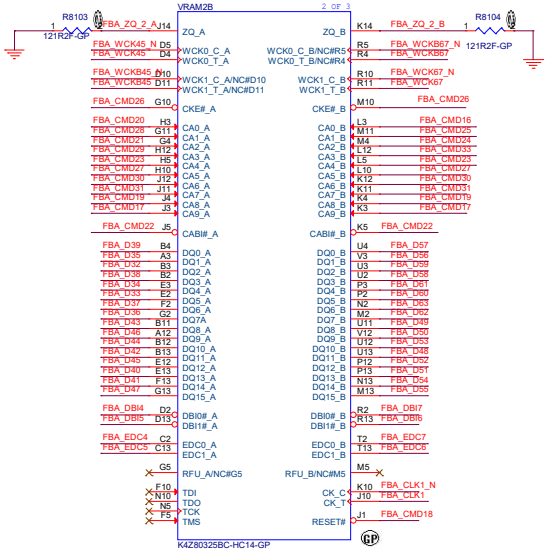

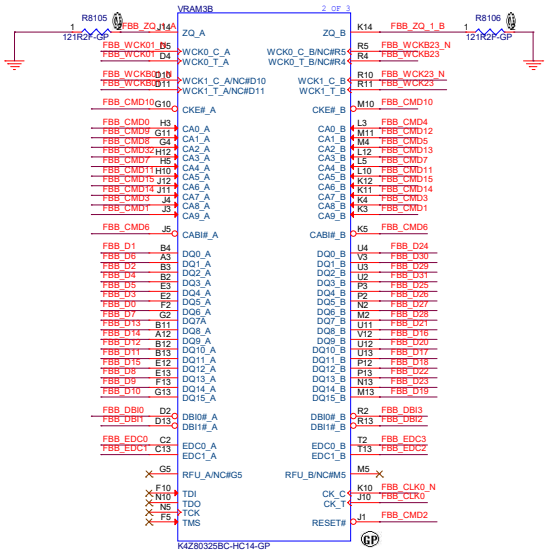

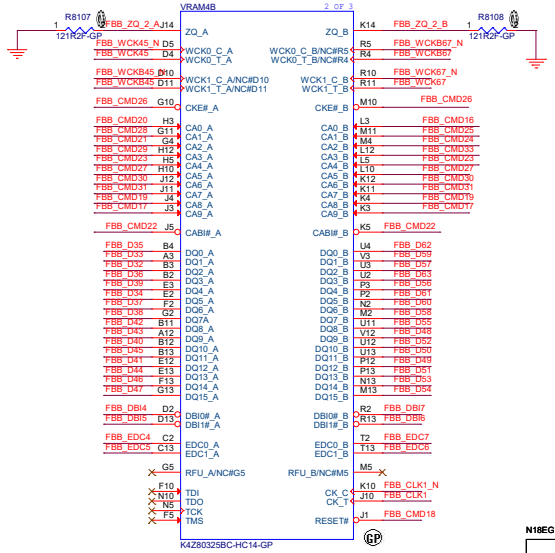

N18EG1 SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	GPU (VRAM1,2 1/4)	
Size A2	Document Number Ghibli_CFL	Rev SC
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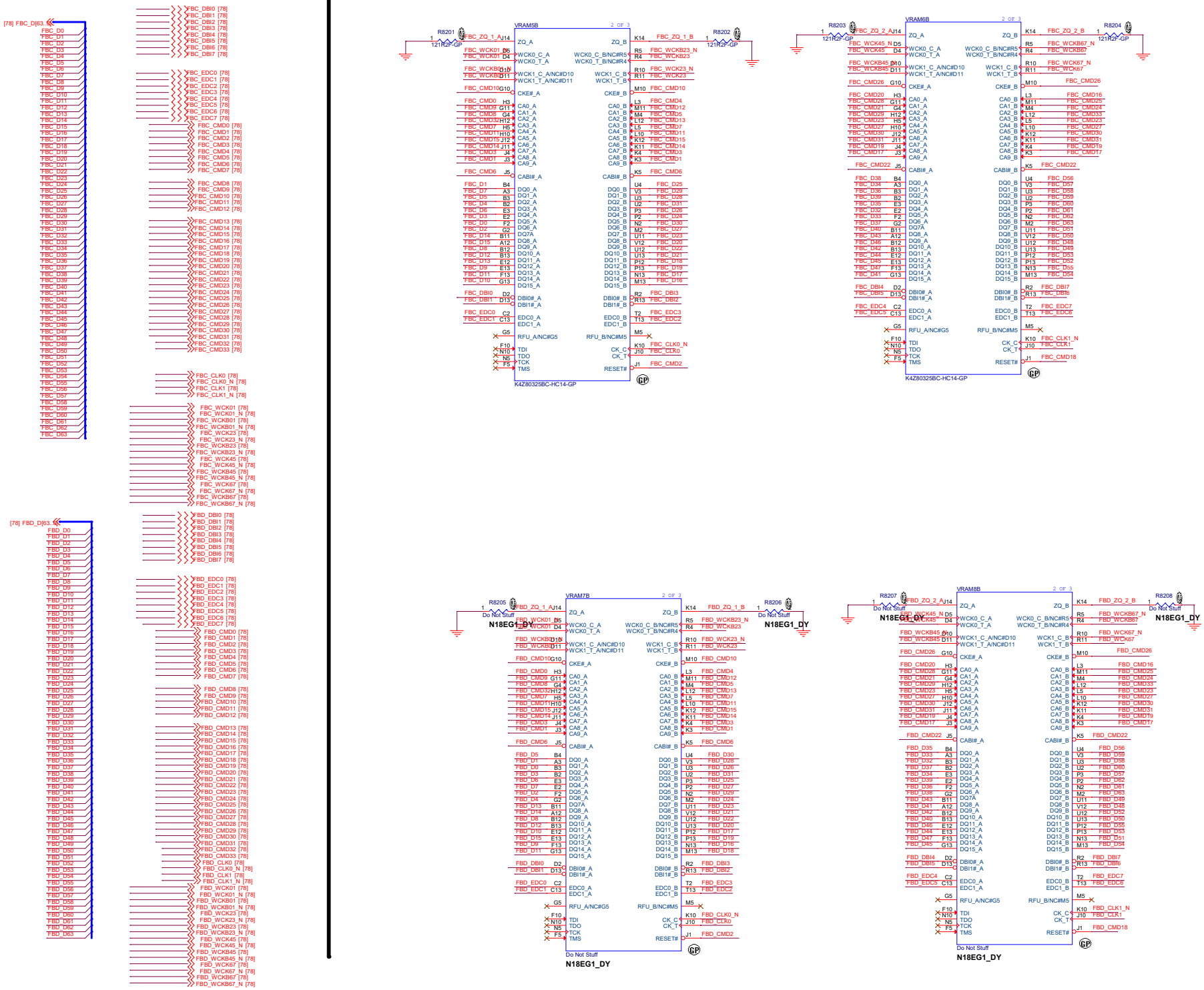
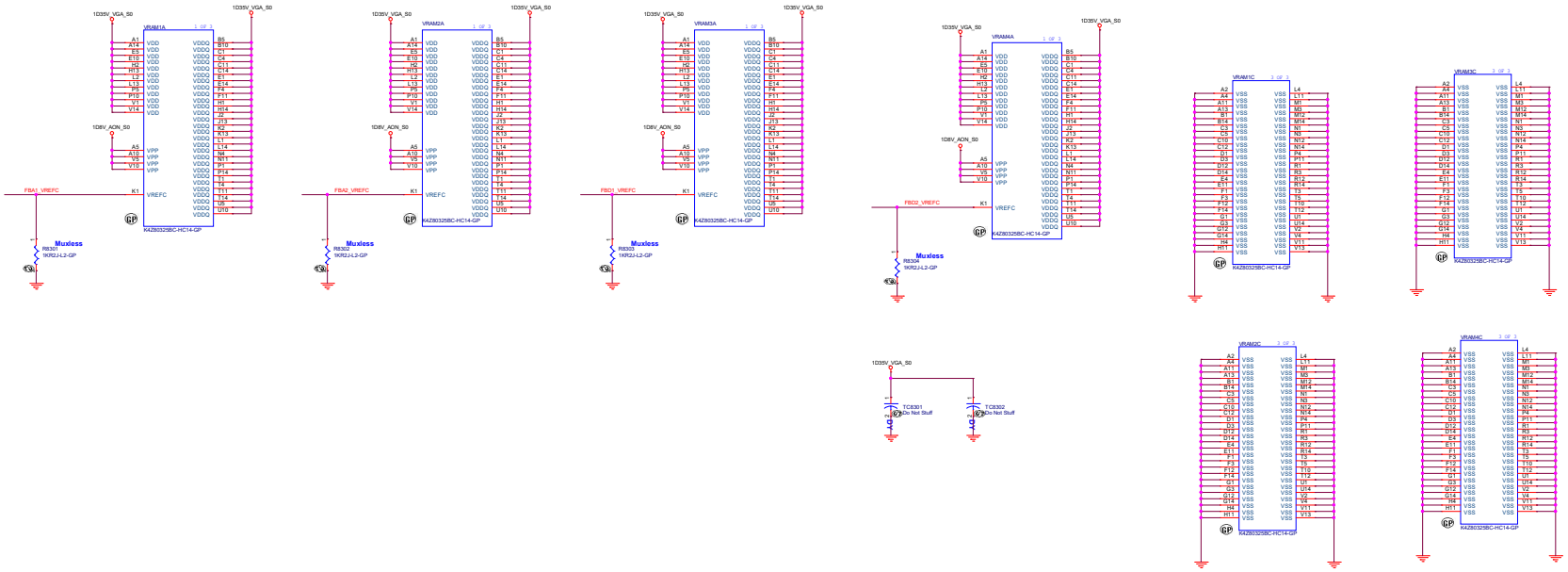
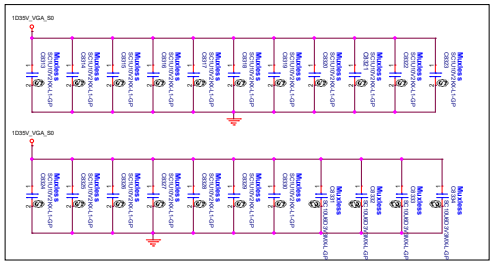


N18EG1 SAMSUNG

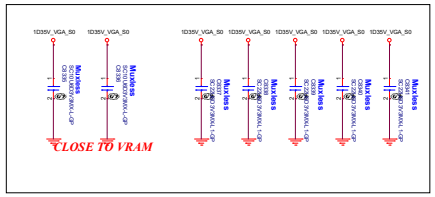
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Block Diagram	
Size A2	Document Number Ghibli_CFL	Rev SC
Date: Tuesday, December 04, 2018	Sheet 82 of 106	

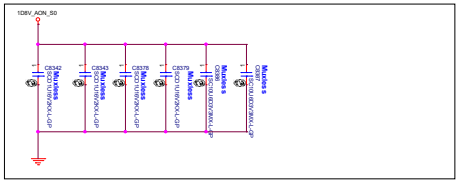


FOR VRAM1/ VRAM2



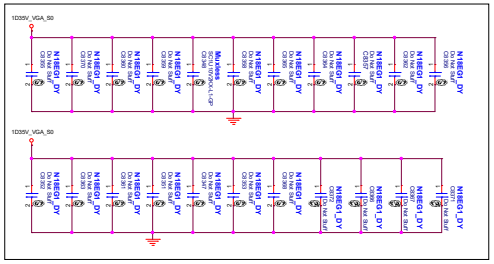
UNDER THE MEMORY



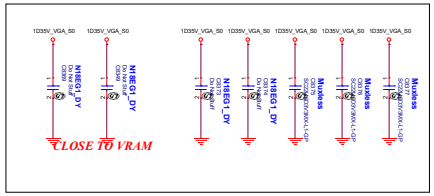


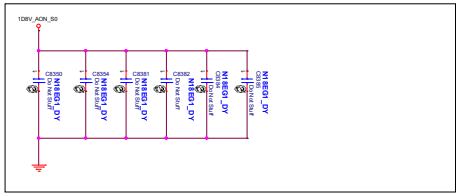
UNDER THE MEMORY

FOR VRAM7/ VRAM8



UNDER THE MEMORY

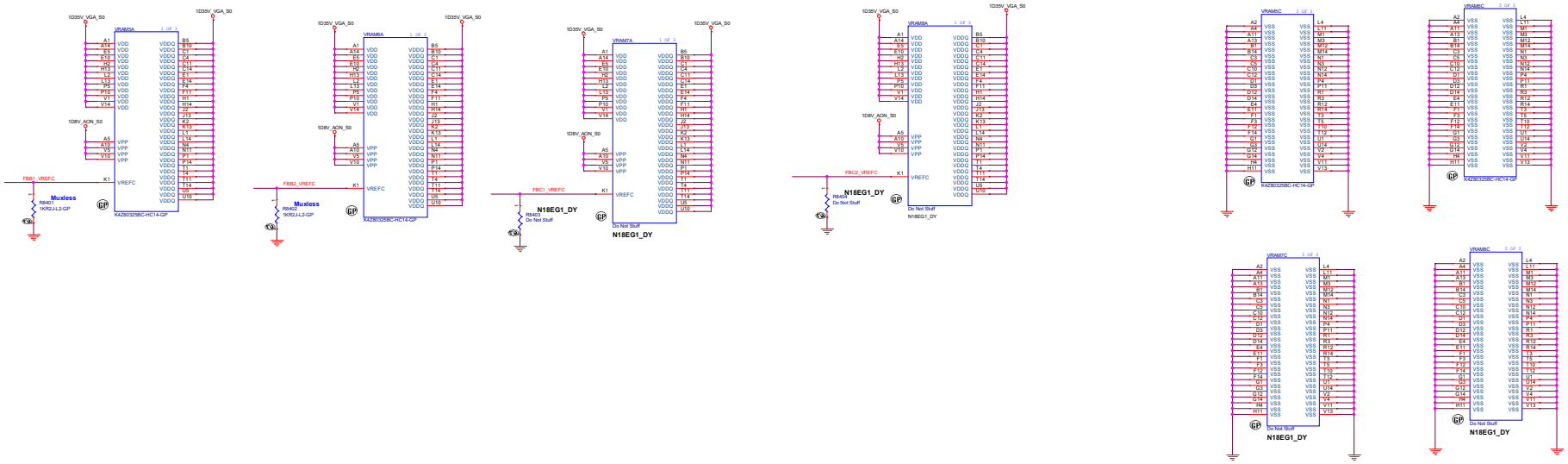




UNDER THE MEMORY

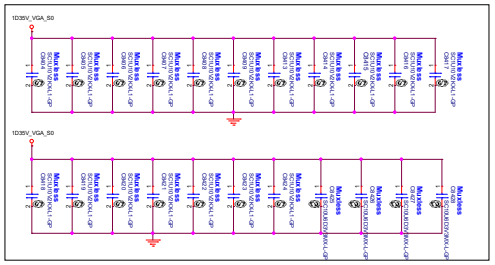
N18EG1 SAMSUNG

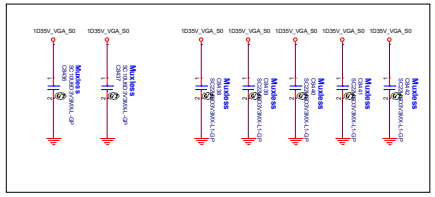
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Block Diagram**	
Size: Custom	Document Number: **Ghibli CFL**	Rev: **SC**
Date: Tuesday, December 04, 2018	Sheet 83 of 105	



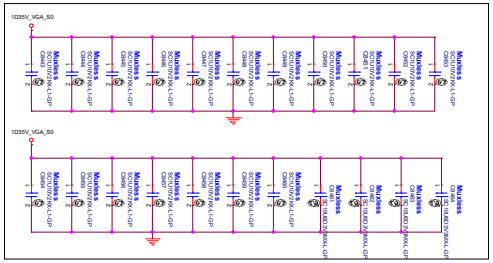
FOR VRAM3/ VRAM4

FOR VRAM5/ VRAM6

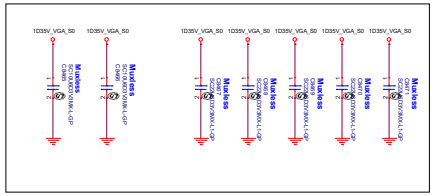




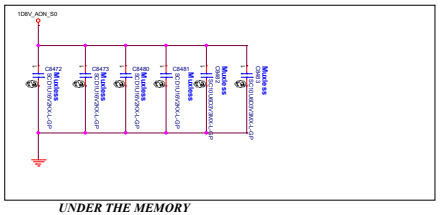
CLOSE TO THE MEMORY



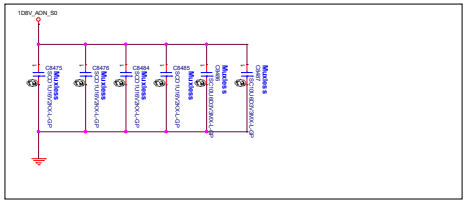
UNDER TO THE MEMORY



CLOSE TO THE MEMORY



UNDER THE MEMORY



UNDER THE MEMORY

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Title: **GPU (VRAM7,8 4/4)**

Size	Document Number	Rev
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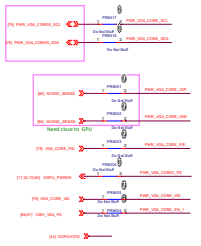

PD Type	PD
Open Drain	OD
Push Pull	PP

PSI	Mode
High	High Phase Count
Hi-Z	Auto Power Mode
Low	Low Phase Count

PWM/VID	Vout
High	VID+ 25%
Hi-Z	VID+ 25%
Low	VID+ 25%

Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification		
	Unit	Config
Number of Voltage Levels H	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{PWM}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.909
C	nF	1.3

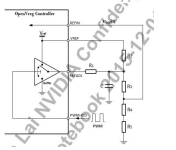

Table 7.9 PWM-VID Spec and Component Values

PWM-VID Specification		
		Config
Vmin	V	0.3
Vmax	V	1.3
Vboot	V	0.8
Voltage Step Vstep	mV	6.25
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{PWM}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.909
C	nF	1.3

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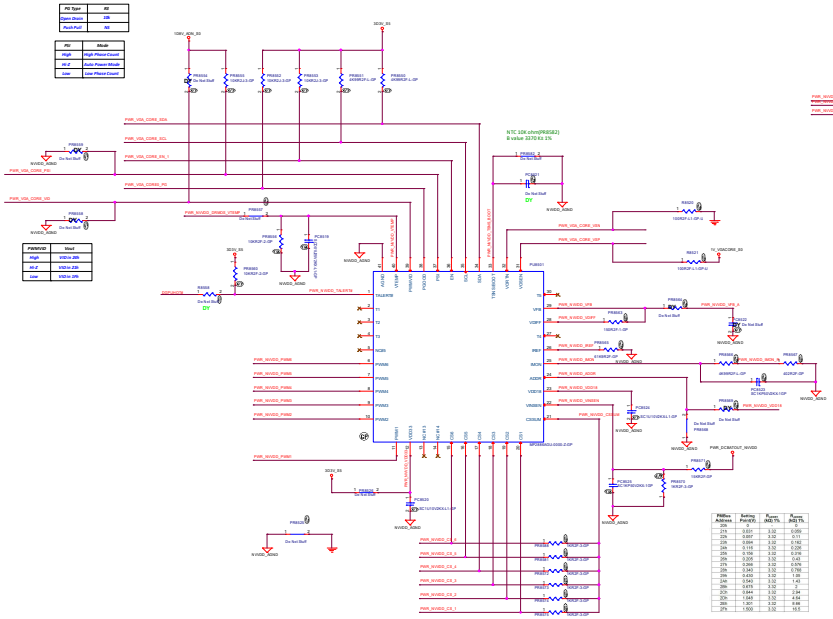
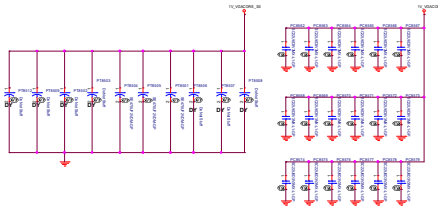
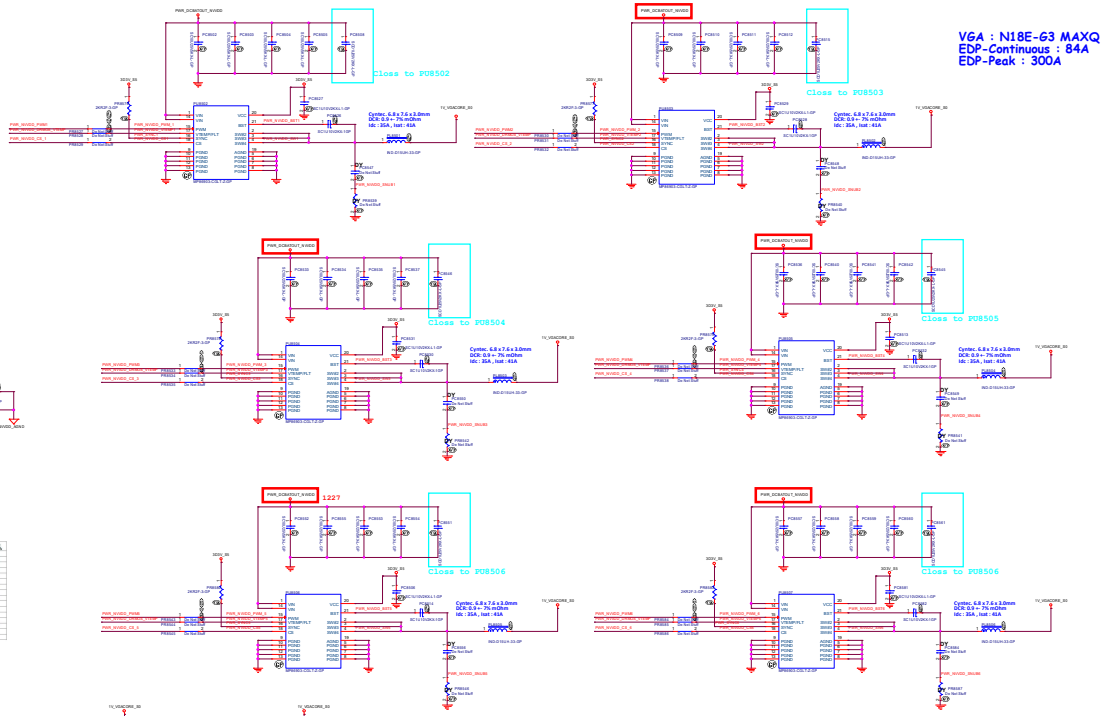


Pd(Max Power)	Rsense (mΩ)	R_{ref} (mΩ)	R_{ref} / R_{sense}
20a	0.500	3.32	0.166
21a	0.531	3.32	0.059
22a	0.497	3.32	0.11
23a	0.594	3.32	0.192
24a	0.594	3.32	0.192
25a	0.556	3.32	0.278
26a	0.505	3.32	0.43
27a	0.846	3.32	0.576
28a	0.846	3.32	0.768
29a	0.443	3.32	1.44
2aa	0.543	3.32	1.43
2ba	0.676	3.32	2
2ca	0.664	3.32	2.44
2da	0.664	3.32	2.44
2ea	1.00	3.32	8.84
2fa	1.500	3.32	18.8





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GPU (MP2886_VGA_CORE)			
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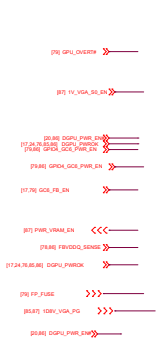
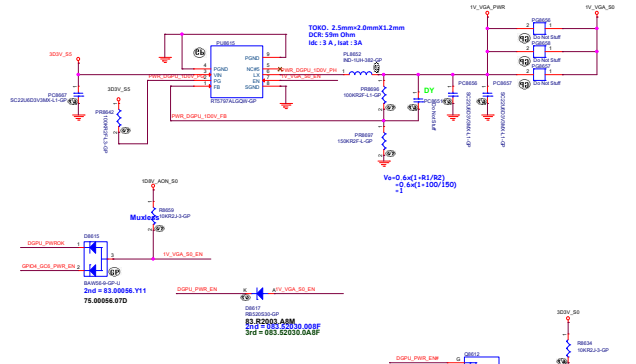
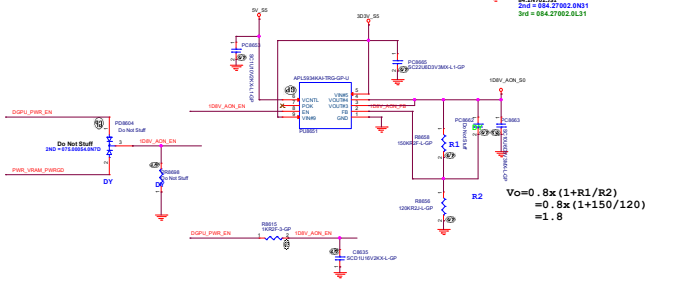


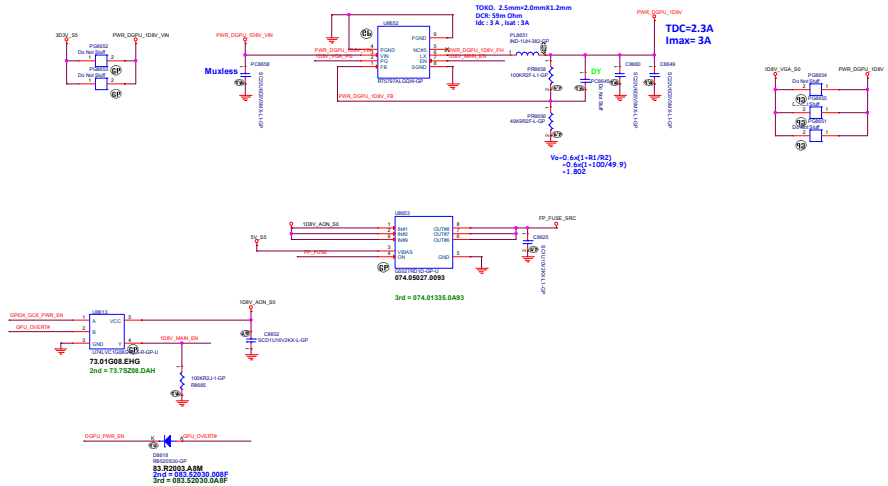
RT5797ALGQW-GP for 1V_VGA_S0



RT5797ALGQW-GP for 1D8V_AON_S0



G5027RD1D-GP-U For 1D8V_VGA_S0



RT8816B for GPU RAM

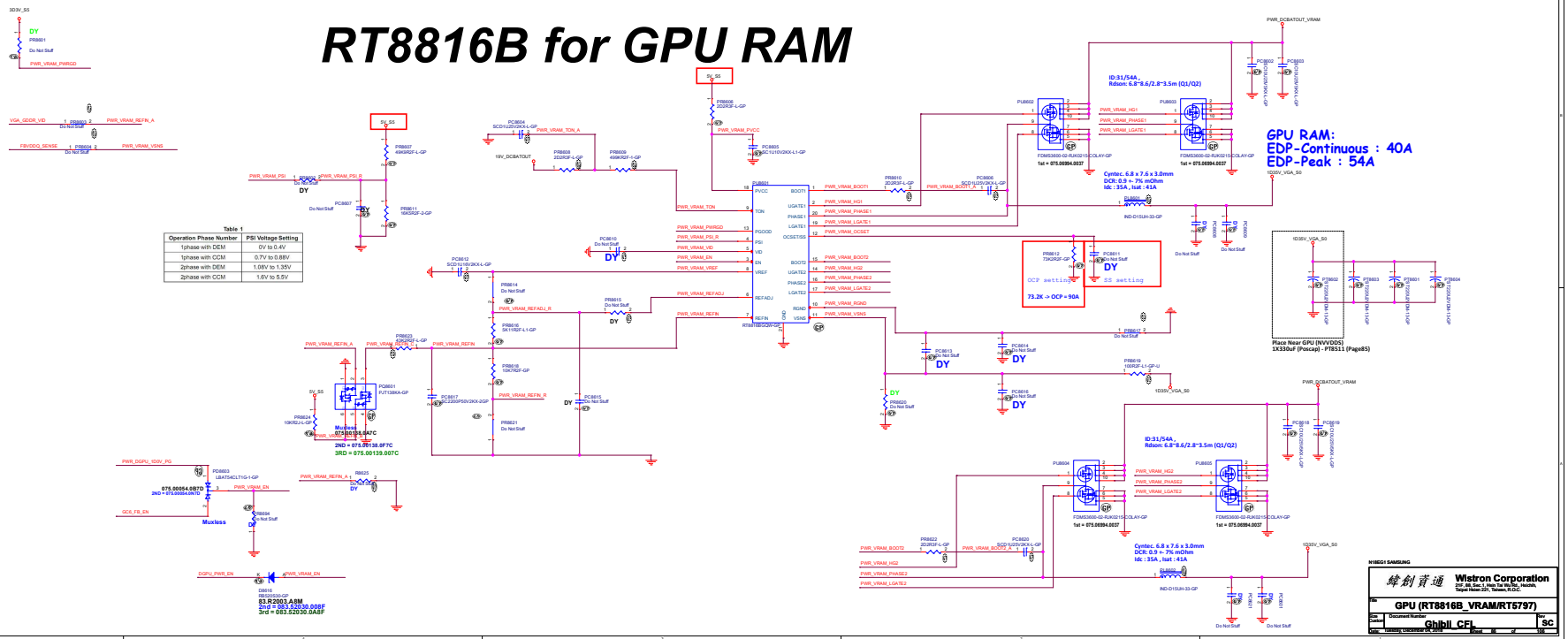


Table 1

Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

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Title: GPU (RT8816B_VRAM/RT5797)

Size: Document Number: Ghibli_CFL Rev: SC

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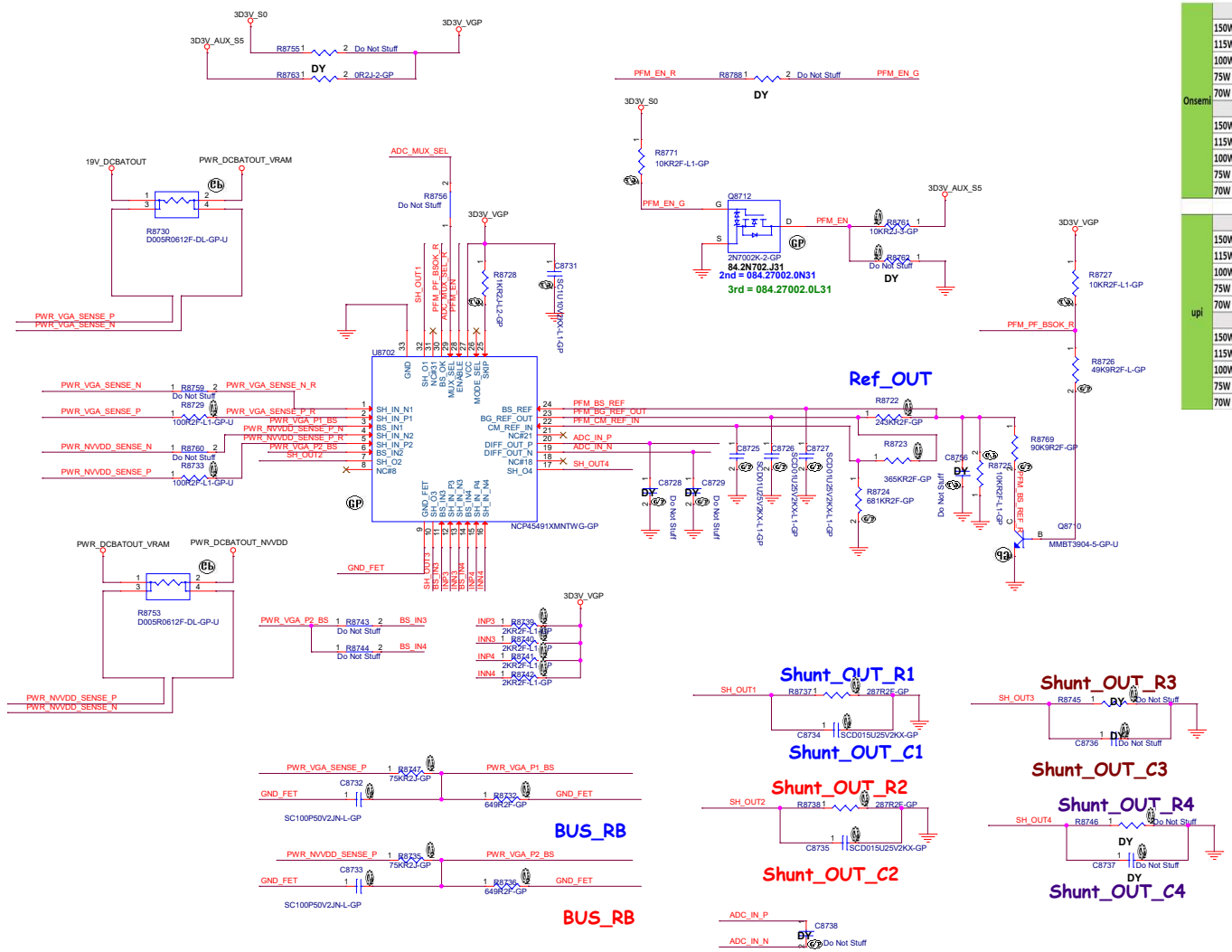

Onsemi	TGP Current	Rs1	Shunt in R1	Shunt out R1	Shunt out C1	Bus RT	Bus RB	Bus Cap	R Ref_out
	150W+	0.005Ω	100Ω	169Ω	15nF	75K	649Ω	1.0nF	243K
	115W to 130W			191Ω					
	100W to 110W			221Ω					
	75W to 90W			287Ω					
	70W or lower			475Ω					
	NVVDD Current	Rs2	Shunt in R2	Shunt out R2	Shunt out C2	Bus RT	Bus RB	Bus Cap	
	150W+	0.005Ω	100Ω	169Ω	15nF	75K	649Ω	1.0nF	
	115W to 130W			191Ω					
	100W to 110W			221Ω					
	75W to 90W			287Ω					
	70W or lower			475Ω					

upi	TGP Current	Rs1	Shunt in R1	Shunt out R1	Shunt out C1	Bus RT	Bus RB	Bus Cap	R Ref_out
	150W+	0.005Ω	100Ω	127Ω	15nF	75K	487Ω	1.0nF	324k
	115W to 130W			143Ω					
	100W to 110W			165Ω					
	75W to 90W			215Ω					
	70W or lower			357Ω					
	NVVDD Current	Rs2	Shunt in R2	Shunt out R2	Shunt out C2	Bus RT	Bus RB	Bus Cap	
	150W+	0.005Ω	100Ω	127Ω	15nF	75K	487Ω	1.0nF	
	115W to 130W			143Ω					
	100W to 110W			165Ω					
	75W to 90W			215Ω					
	70W or lower			357Ω					

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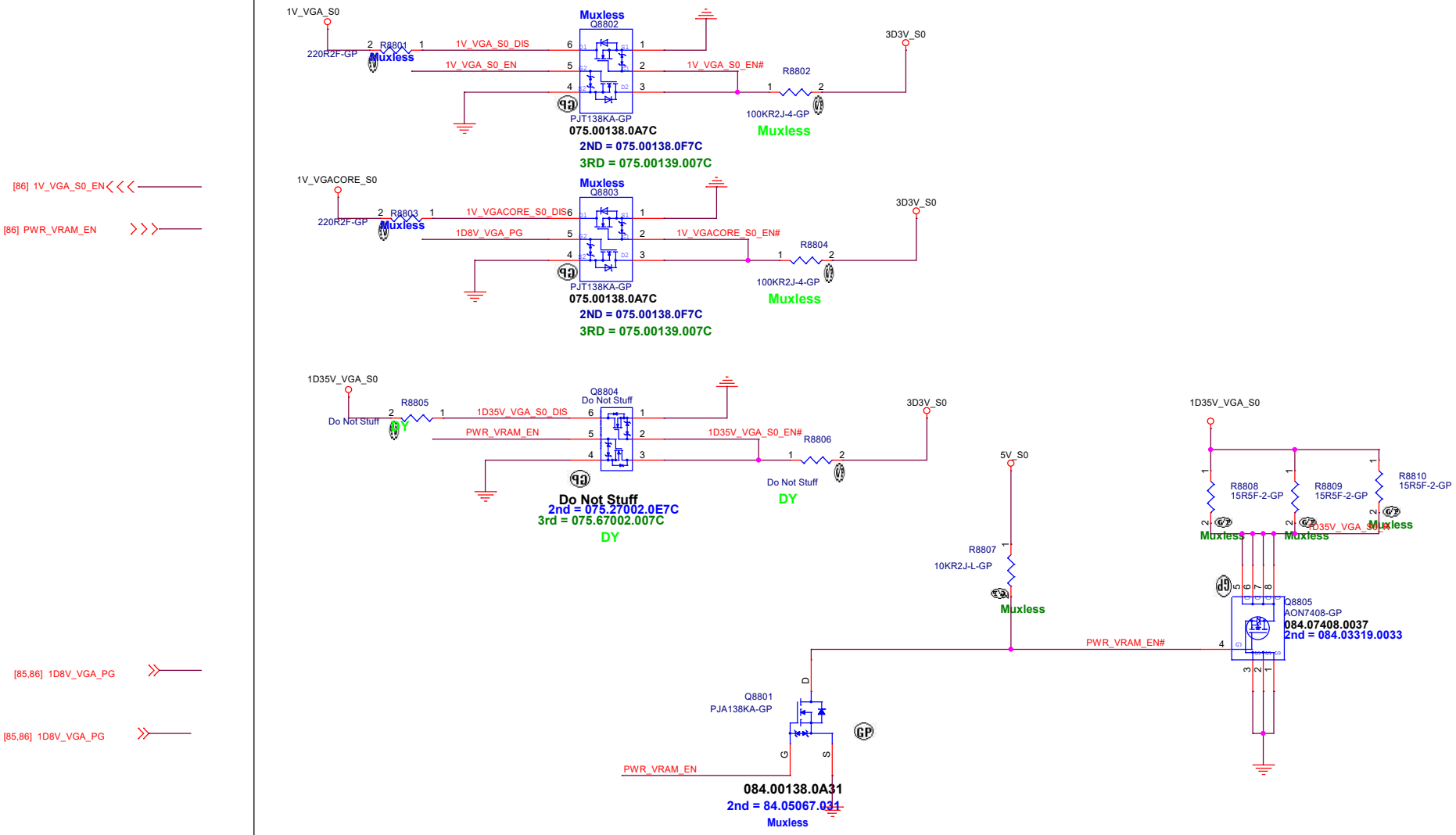

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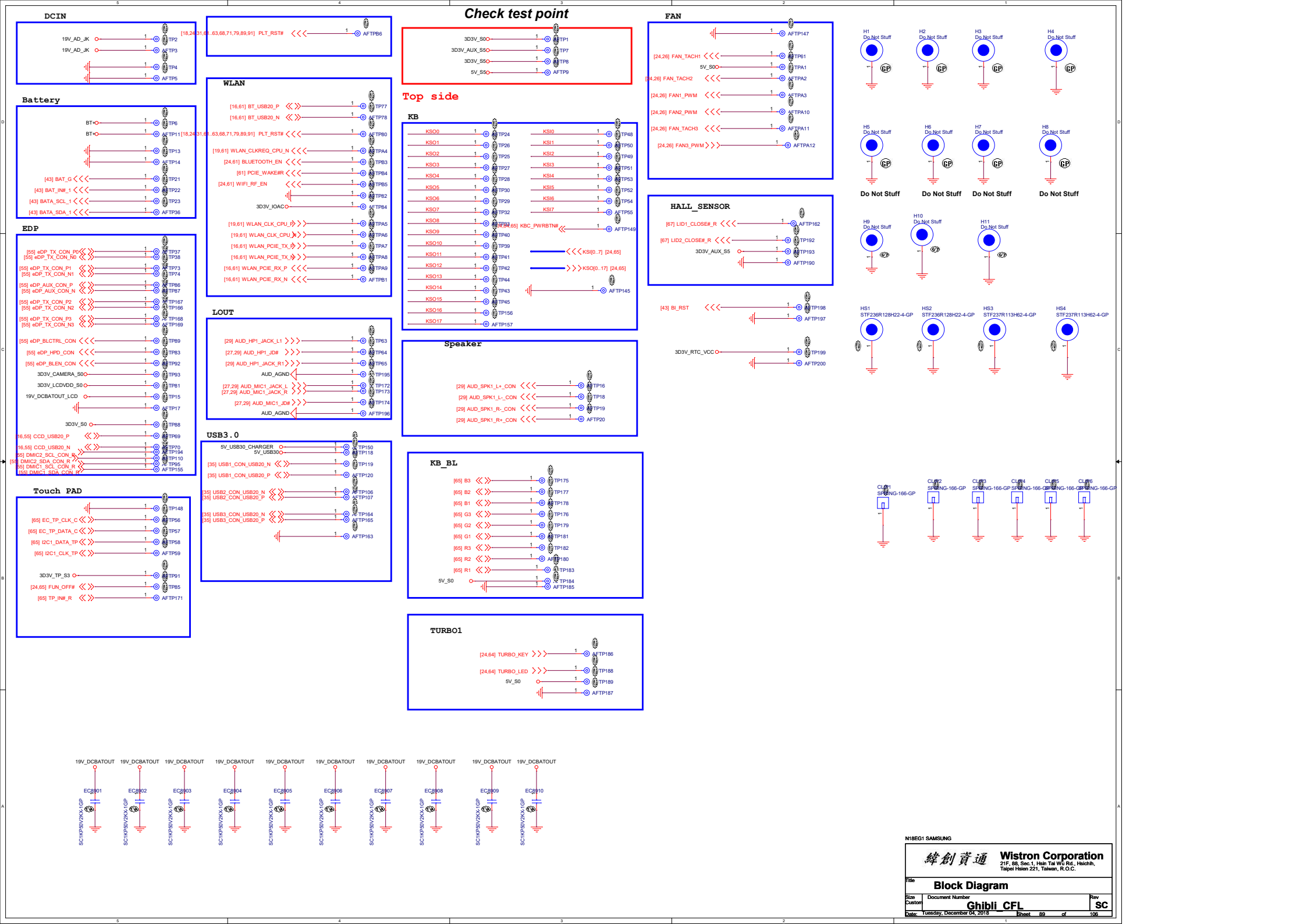
DCIN
19V_AD_JK TP2
19V_AD_JK AFTP3
TP4
AFTP5
[18,24,31,61,63,68,71,79,89,91] PLT_RST# AFTPB6
Check test point
3D3V_S0 TP1
3D3V_AUX_S5 TP7
3D3V_S5 TP8
5V_S5 AFTP9
Top side
Battery
BT+ TP6
BT+ AFTP11
TP13
AFTP14
[43] BAT_G TP21
[43] BAT_IN#_1 TP22
[43] BATA_SCL_1 TP23
[43] BATA_SDA_1 AFTP36
WLAN
[16,61] BT_USB20_P TP77
[16,61] BT_USB20_N AFTP78
[18,24,31,61,63,68,71,79,89,91] PLT_RST# AFTP80
[19,61] WLAN_CLKREQ_CPU_N TP4
[24,61] BLUETOOTH_EN TP3
[61] PCIE_WAKE#R TP4
[24,61] WIFI_RF_EN TP5
TP82
3D3V_IOAC AFTP84
[19,61] WLAN_CLK_CPU_P TP5
[19,61] WLAN_CLK_CPU_N TP6
[16,61] WLAN_PCIE_TX_P TP7
[16,61] WLAN_PCIE_TX_N TP8
[16,61] WLAN_PCIE_RX_P TP9
[16,61] WLAN_PCIE_RX_N AFTPB1
KB
KSO0 TP24
KSO1 TP26
KSO2 TP25
KSO3 TP27
KSO4 TP28
KSO5 TP30
KSO6 TP29
KSO7 TP32
KSO8 TP33
KSO9 TP40
KSO10 TP39
KSO11 TP41
KSO12 TP42
KSO13 TP44
KSO14 TP43
KSO15 TP45
KSO16 TP156
KSO17 AFTP157
KSI0 TP48
KSI1 TP50
KSI2 TP49
KSI3 TP51
KSI4 TP53
KSI5 TP52
KSI6 TP54
KSI7 TP55
[24,26,65] KBC_PWRBTN# AFTP149
KSI[0..7] [24,65]
KSO[0..17] [24,65]
AFTP145
FAN
AFTP147
[24,26] FAN_TACH1 AFTP61
5V_S0 AFTPA1
[24,26] FAN_TACH2 AFTPA2
[24,26] FAN1_PWM AFTPA3
[24,26] FAN2_PWM AFTPA10
[24,26] FAN_TACH3 AFTPA11
[24,26] FAN3_PWM AFTPA12
HALL_SENSOR
[67] LID1_CLOSE#_R AFTP162
[67] LID2_CLOSE#_R TP192
3D3V_AUX_S5 TP193
AFTP190
[43] BI_RST TP198
AFTP197
3D3V_RTC_VCC TP199
AFTP200
H1 Do Not Stuff
H2 Do Not Stuff
H3 Do Not Stuff
H4 Do Not Stuff
H5 Do Not Stuff
H6 Do Not Stuff
H7 Do Not Stuff
H8 Do Not Stuff
Do Not Stuff
Do Not Stuff
Do Not Stuff
Do Not Stuff
H9 Do Not Stuff
H10 Do Not Stuff
H11 Do Not Stuff
HS1 STF236R128H22-4-GP
HS2 STF236R128H22-4-GP
HS3 STF237R113H62-4-GP
HS4 STF237R113H62-4-GP
EDP
[55] eDP_TX_CON_P0 TP37
[55] eDP_TX_CON_N0 TP38
[55] eDP_TX_CON_P1 TP73
[55] eDP_TX_CON_N1 TP74
[55] eDP_AUX_CON_P TP86
[55] eDP_AUX_CON_N TP87
[55] eDP_TX_CON_P2 TP167
[55] eDP_TX_CON_N2 TP166
[55] eDP_TX_CON_P3 TP168
[55] eDP_TX_CON_N3 AFTP169
[55] eDP_BLCTRL_CON TP89
[55] eDP_HPD_CON TP83
[55] eDP_BLEN_CON TP92
3D3V_CAMERA_S0 TP93
3D3V_LCDVDD_S0 TP81
19V_DCBATOUT_LCD TP15
AFTP17
3D3V_S0 TP88
[16,55] CCD_USB20_P TP69
[16,55] CCD_USB20_N TP70
[55] DMIC2_SCL_CON_R TP194
[55] DMIC2_SDA_CON_R TP110
[55] DMIC1_SCL_CON_R TP95
[55] DMIC1_SDA_CON_R AFTP155
LOUT
[29] AUD_HP1_JACK_L1 TP63
[27,29] AUD_HP1_JD# TP64
[29] AUD_HP1_JACK_R1 TP65
AUD_AGND TP195
[27,29] AUD_MIC1_JACK_L TP172
[27,29] AUD_MIC1_JACK_R TP173
[27,29] AUD_MIC1_JD# TP174
AUD_AGND AFTP196
Speaker
[29] AUD_SPK1_L+_CON TP16
[29] AUD_SPK1_L-_CON TP18
[29] AUD_SPK1_R-_CON TP19
[29] AUD_SPK1_R+_CON AFTP20
Touch PAD
TP148
[65] EC_TP_CLK_C TP56
[65] EC_TP_DATA_C TP57
[65] I2C1_DATA_TP TP58
[65] I2C1_CLK_TP AFTP59
3D3V_TP_S3 TP91
[24,65] FUN_OFF# TP85
[65] TP_IN#_R AFTP171
USB3.0
5V_USB30_CHARGER TP150
5V_USB30 TP118
[35] USB1_CON_USB20_N TP119
[35] USB1_CON_USB20_P AFTP120
[35] USB2_CON_USB20_N TP106
[35] USB2_CON_USB20_P AFTP107
[35] USB3_CON_USB20_N TP164
[35] USB3_CON_USB20_P AFTP165
AFTP163
KB_BL
[65] B3 TP175
[65] B2 TP177
[65] B1 TP178
[65] G3 TP176
[65] G2 TP179
[65] G1 TP181
[65] R3 TP182
[65] R2 AFTP180
[65] R1 TP183
5V_S0 TP184
AFTP185
TURBO1
[24,64] TURBO_KEY AFTP186
[24,64] TURBO_LED TP188
5V_S0 TP189
AFTP187
CLIP1 SPRING-166-GP
CLIP2 SPRING-166-GP
CLIP3 SPRING-166-GP
CLIP4 SPRING-166-GP
CLIP5 SPRING-166-GP
CLIP6 SPRING-166-GP
19V_DCBATOUT
EC8901 EC8902 EC8903 EC8904 EC8905 EC8906 EC8907 EC8908 EC8909 EC8910
SC1KP50V2KX-1GP
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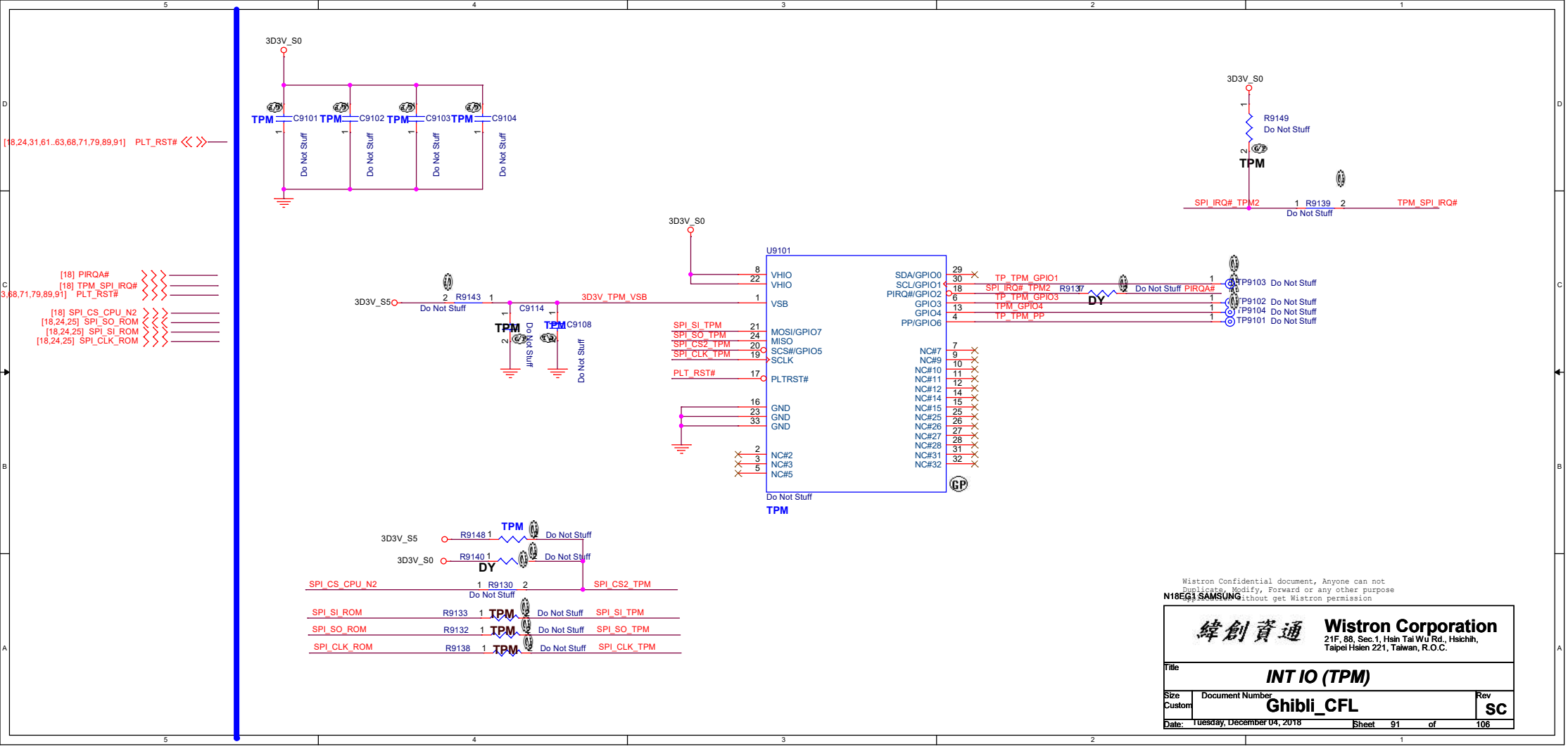

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Title: Commercial (RSVD)

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Title	**Commercial (RSVD)**	
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Title: Debug (RSVD)

Size	Document Number	Rev
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Block Diagram

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A	Ghibli_CFL	SC

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N18EG1 SAMSUNG

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Title **Block Diagram**

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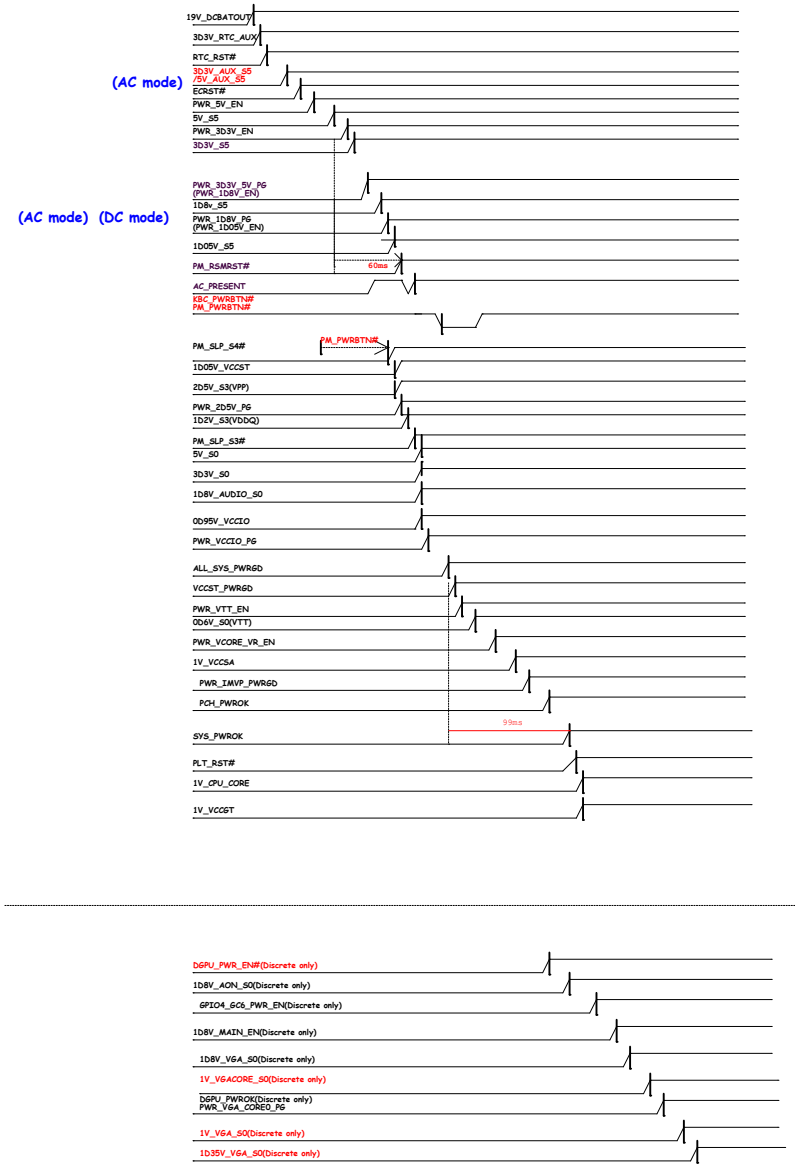
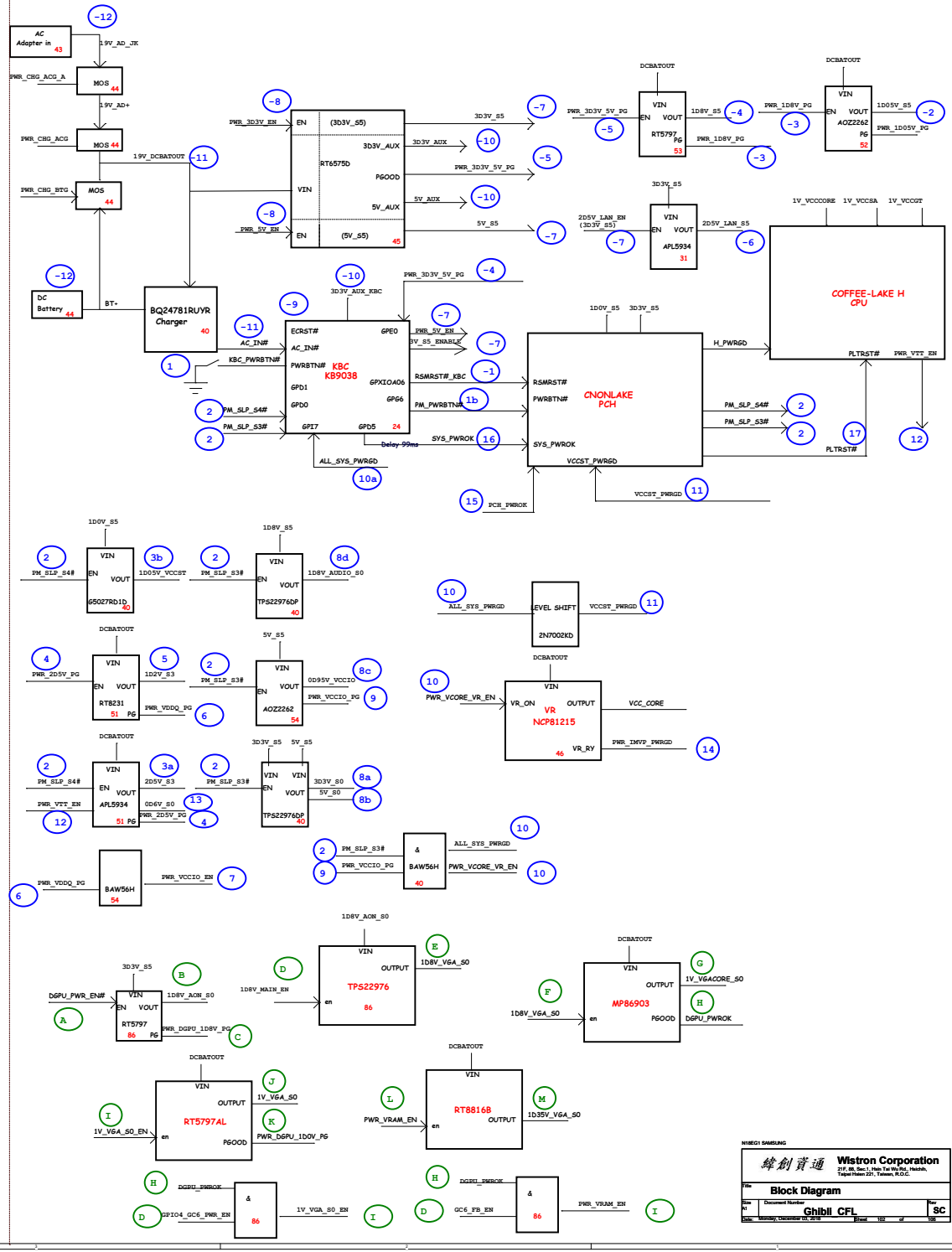
Intel-Power Up Sequence



CFL H POWER UP SEQUENCE DIAGRAM



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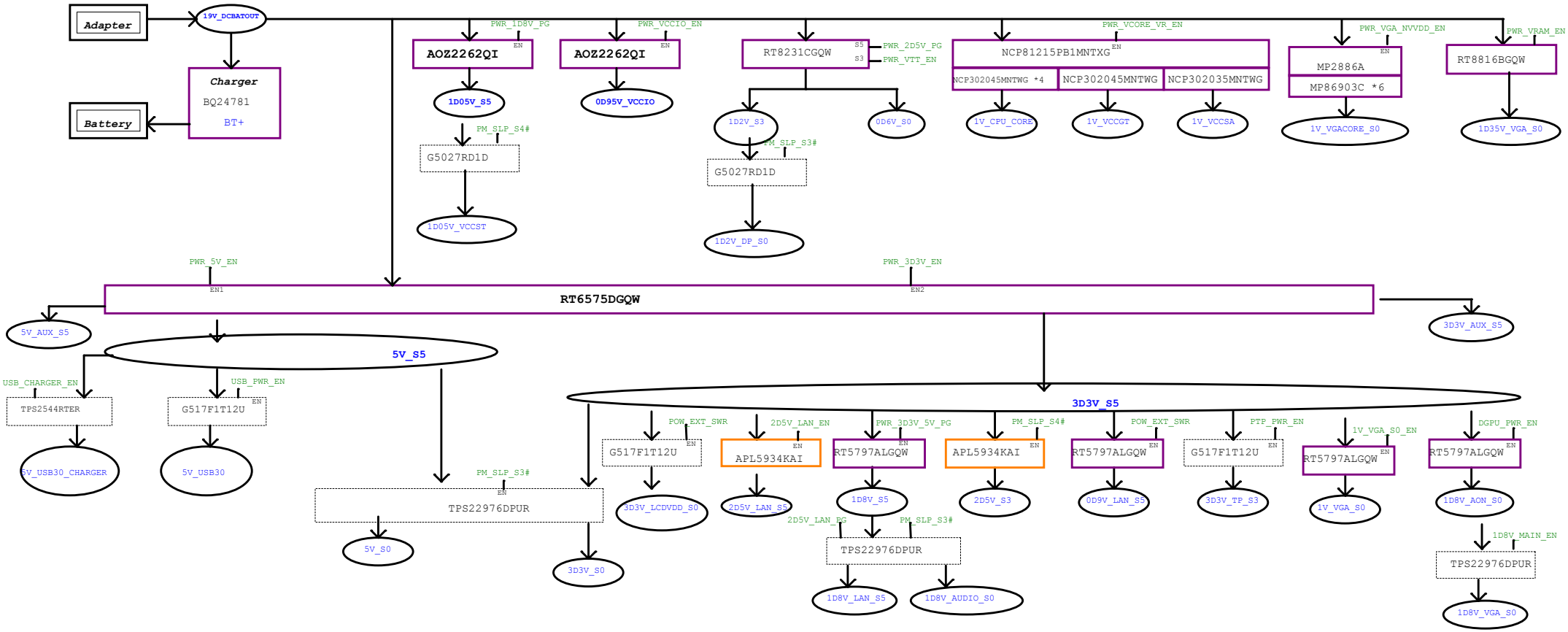

Power Shape

Regulator	LDO	Switch

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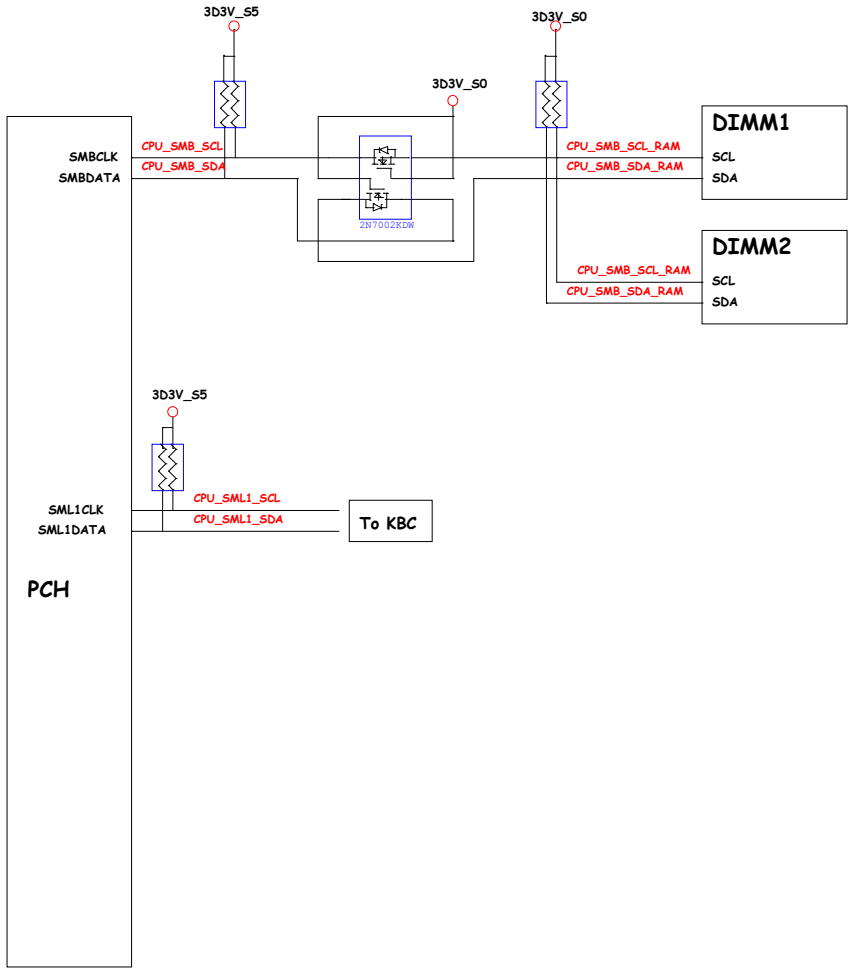
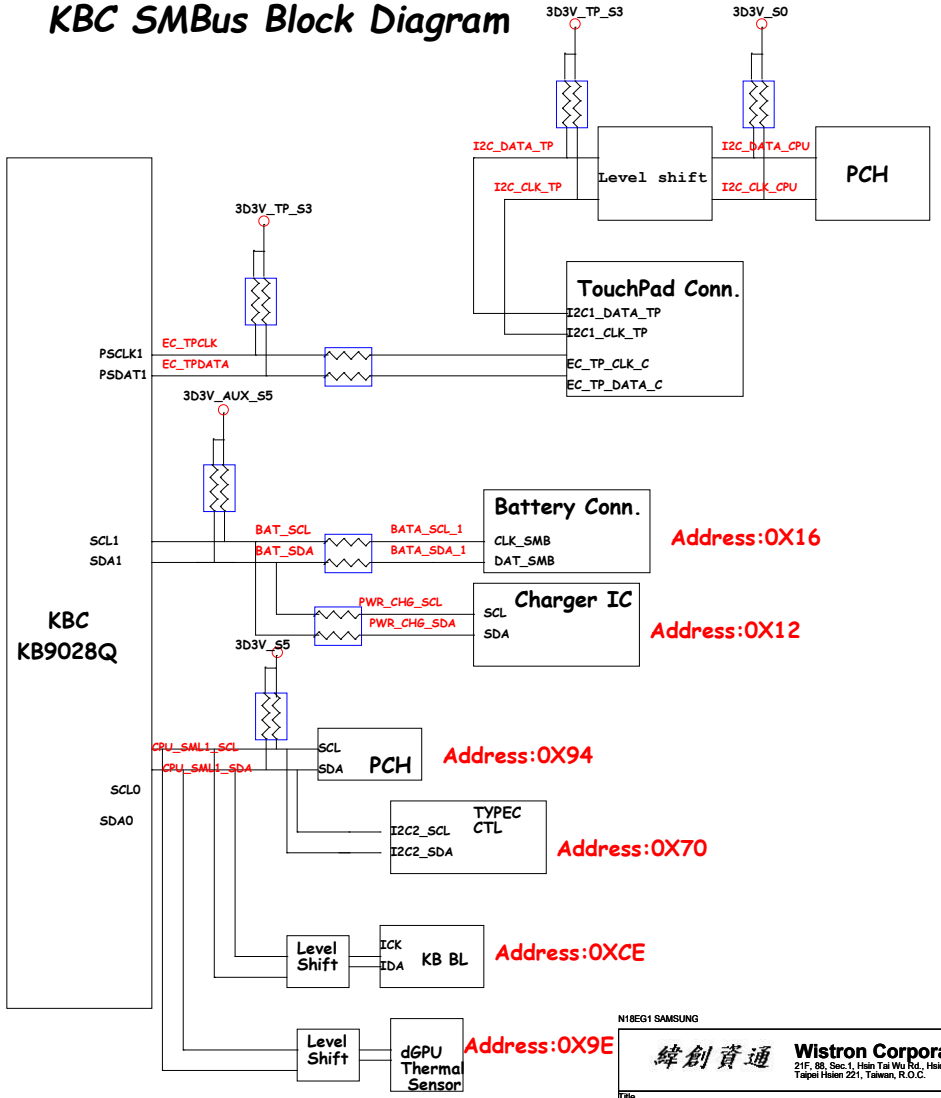
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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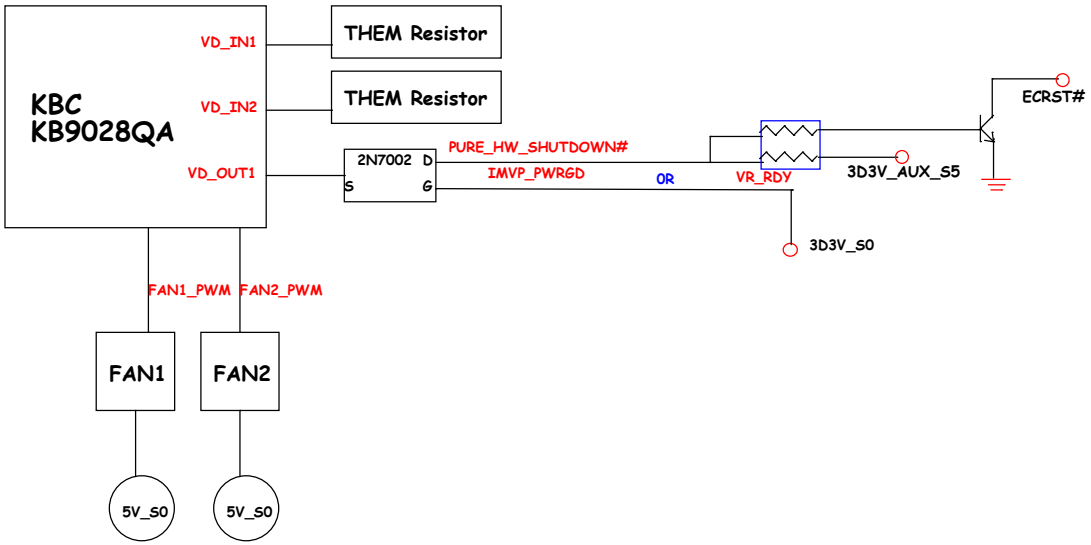
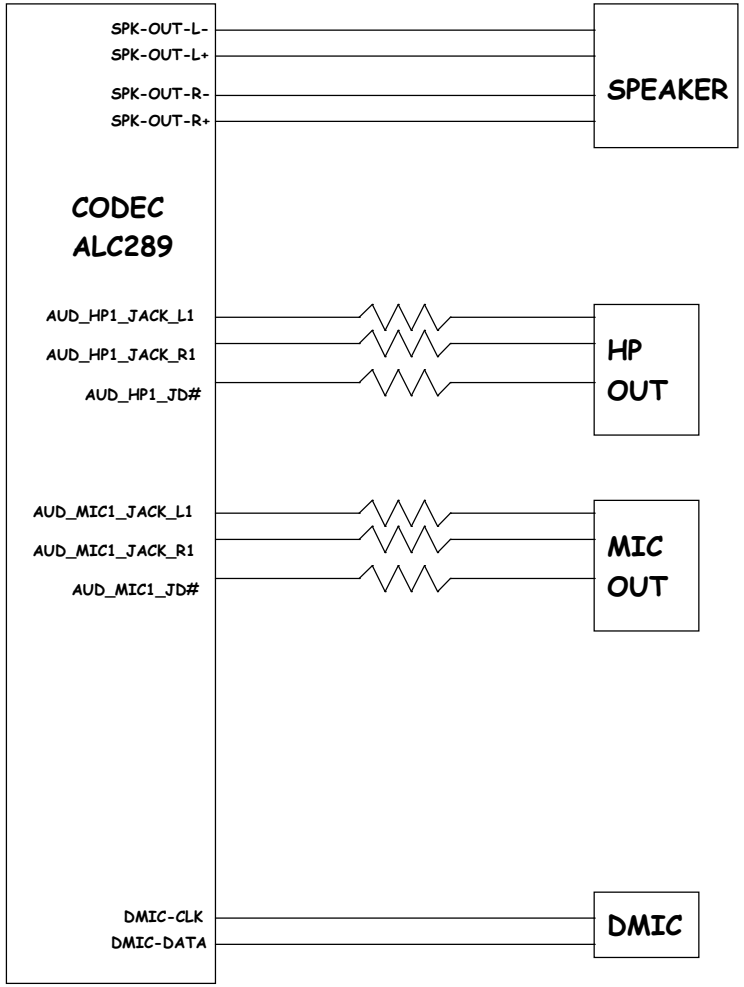
Thermal Block Diagram



Audio Block Diagram



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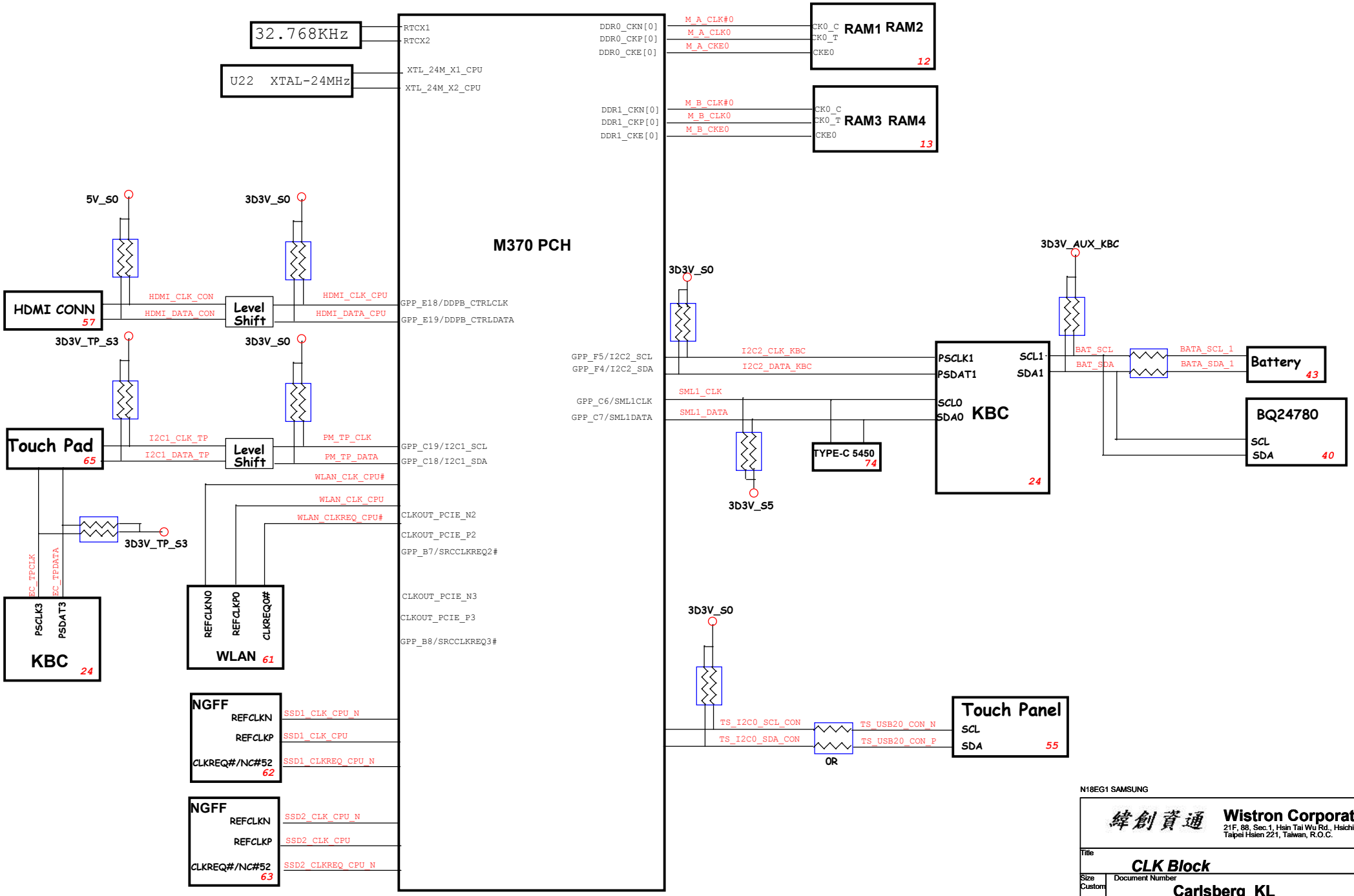
CLOCK BLOCK DIAGRAM



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Title: **CLK Block**

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