nearly proportional to the square of the velocity saturation voltage, LE_{CRIT}, or the square of channel length and E_{CRIT}. This suggests that IC_{CRIT} might be approximately 13 % ($(0.065\,\mu m/0.18\,\mu m)^2$) of the value of 25 shown in Figure 3.25 for an $L = 0.18\,\mu m$, nMOS device, or 3.3 for an $L = 0.065\,\mu m$, nMOS device. Such a critical value of IC_{CRIT} is well into moderate inversion and is likely too low since IC_{CRIT} was derived for operation in strong inversion. A modified interpolation in Equation 3.42 may be required as velocity saturation effects begin to encroach closer to moderate inversion for very short-channel devices. The designer can minimize velocity saturation reduction of g_m/I_D by increasing IC_{CRIT} by increasing channel length and using pMOS devices that have higher E_{CRIT}. Additionally, operation can be confined to lower IC values in moderate inversion.

3.8.2.3 Predicted and measured values

Figure 3.26 shows measured and predicted g_m/I_D for $L = 0.18$, 0.28, 0.48, 1, and 4 μm, nMOS devices in the 0.18 μm process described in Table 3.2. Measurements for $L = 2\,\mu m$ devices are not shown but lie essentially on the $L = 4\,\mu m$ values. g_m/I_D is predicted as described for Figure 3.24, using the process parameters previously mentioned for Figure 3.25. g_m/I_D is presented as a function of the inversion coefficient from $IC = 0.01$ (deep weak inversion) to 100 (deep strong inversion) over a wide range of channel lengths, providing a full characterization of the process for analog design.

In Figure 3.26, g_m/I_D is constant and maximum in weak inversion,[9] before decreasing modestly in moderate inversion. In strong inversion, g_m/I_D decreases as $1/\sqrt{IC}$ for the long-channel devices that

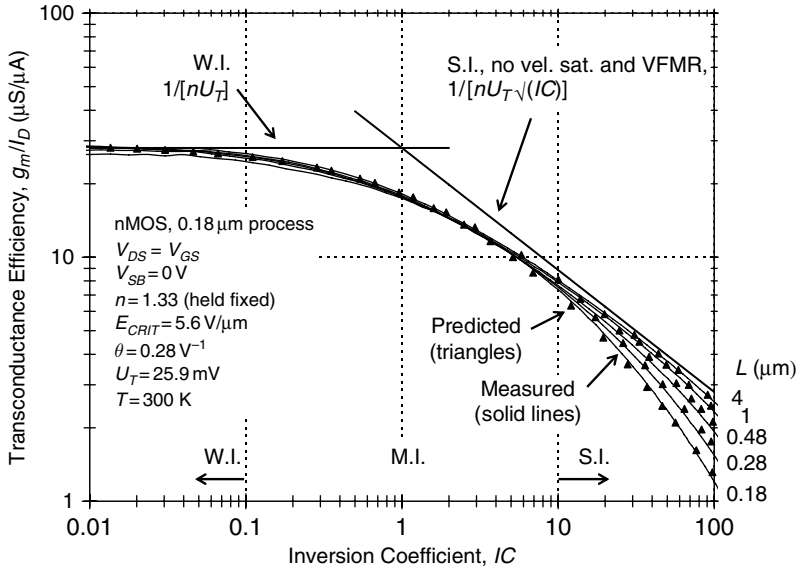

Figure 3.26 Predicted and measured transconductance efficiency, g_m/I_D, versus inversion coefficient, IC, for $L = 0.18$, 0.28, 0.48, 1, and 4 μm, nMOS devices in a 0.18 μm CMOS process. g_m/I_D is maximum in weak inversion, decreases modestly in moderate inversion, and decreases as $1/\sqrt{IC}$ in strong inversion. For short-channel devices at high IC, g_m/I_D decreases significantly due to velocity saturation and is nearly proportional to $1/IC$. At high IC, g_m/I_D decreases modestly for all channel lengths due to VFMR effects. g_m/I_D is similar for all CMOS processes

[9] g_m/I_D actually peaks very slightly in weak inversion before decreasing slightly for operation deeper into weak inversion because of the slight increase in n.

experience little velocity saturation. However, at high levels of IC, g_m/I_D decreases nearly as $1/IC$ for the short-channel devices that experience significant velocity saturation. g_m/I_D decreases more for short channel lengths due to increased velocity saturation effects, while it decreases modestly for all channel lengths due to VFMR effects. No velocity saturation decrease in g_m/I_D is observed in weak inversion and little decrease is observed in moderate inversion. Small velocity saturation effects in moderate inversion, even for short-channel devices, are a major advantage of operation here. The decrease in g_m/I_D in strong inversion for short channel lengths, however, is significant and must be considered in design.

Figure 3.27 shows measured and predicted g_m/I_D for $L = 0.18$, 0.28, and 1 μm, pMOS devices in the 0.18 μm process described in Table 3.2. Measurements for $L = 0.48$, 2, and 4 μm devices are not shown but lie essentially on the $L = 1$ μm values. g_m/I_D is predicted using a fixed value of $n = 1.33$, thermal voltage of $U_T = 25.9$ mV ($T = 300$ K), $E_{CRIT} = 14$ V/μm, and $\theta = 0.35$/V from Table 3.2. Channel length is adjusted from the drawn values given by subtracting $DL = 0.051$ μm, which is also listed in the table. The inversion coefficient for measured data is found using a technology current of $I_0 = 0.135$ μA from the table.

In weak and moderate inversion ($IC < 10$), pMOS g_m/I_D shown in Figure 3.27 is nearly identical to that of nMOS devices shown in Figure 3.26. However, the g_m/I_D decrease in deep strong inversion ($IC = 100$) at short channel lengths is significantly less for pMOS devices because of less velocity saturation resulting from a higher $E_{CRIT} = 14$ V/μm compared to 5.6 V/μm for nMOS devices. While the g_m/I_D decrease at short channel lengths is greater for nMOS devices due to velocity saturation, the g_m/I_D decrease at long channel lengths is greater for pMOS devices because of higher VFMR effects resulting from a higher mobility reduction factor of $\theta = 0.35$/V compared to 0.28/V for nMOS devices. Like the drain current shown in Figures 3.11 and 3.12, and V_{EFF} shown in Figures 3.14 and 3.15, pMOS g_m/I_D is nearly equal to that of nMOS devices shown if pMOS channel length is decreased

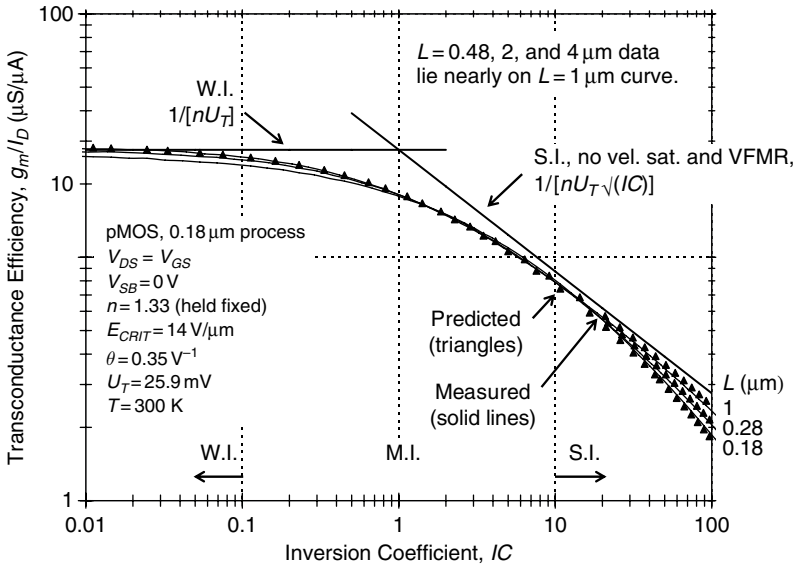

Figure 3.27 Predicted and measured transconductance efficiency, g_m/I_D, versus inversion coefficient, IC, for $L = 0.18$, 0.28, and 1 μm, pMOS devices in a 0.18 μm CMOS process. g_m/I_D decreases less at high IC for short-channel devices compared to the nMOS values shown in Figure 3.26 because of lower pMOS velocity saturation. At high IC, g_m/I_D decreases modestly for all channel lengths due to VFMR effects. Measurements not shown for $L = 0.48$, 2, and 4 μm devices lie nearly on the measured, $L = 1$ μm curve. g_m/I_D is similar for all CMOS processes