From David M. Binkley "Tradeoffs and Optimization in Analog CMOS Design"

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In weak inversion, n is approximately 1.4–1.5 for typical bulk CMOS processes, but can be as low as 1.1 [4] for fully depleted (FD) silicon-on-insulator (SOI) CMOS processes where there is little substrate effect. n drops slightly with increasing inversion level (increasing VEFF = VGS − VT) and is approximately 1.35 in moderate inversion and 1.3 in strong inversion for typical bulk CMOS processes.

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In weak inversion, n is the weak inversion slope factor that describes the degradation of exponential MOS drain current compared to bipolar transistor collector current where the equivalent value of n, the emitter injection efficiency, is very close to unity. Often the MOS weak inversion slope factor is expressed by the weak inversion or subthreshold swing given by
S=ln(10)nUT =2.303·nUT (mV/decade) (2.7)
This is the required increase in gate–source voltage for a factor-of-10 increase in drain current. The weak inversion swing is approximately 90 mV/decade for bulk CMOS processes at room temperature, assuming n = 1.5 and UT = 25.9 mV.

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Parameter	Description	nMOS	pMOS	Units
n0	Substrate factor (average moderate inversion value, Vsb=0)			
	0.5µm	1.4	1.35	
	0.35µm, PD SOI	1.4	1.35	
	0.18µm	1.35	1.35	

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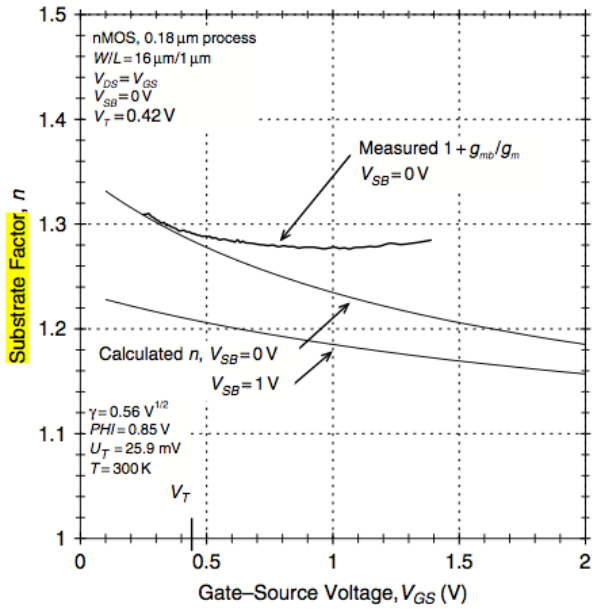

Figure 3.2 Predicted substrate factor, n, versus gate–source voltage with overlay of measured $1 + g_{mb}/g_m$ for nMOS devices in a 0.18 µm CMOS process. The measured $1 + g_{mb}/g_m$ overlay tracks n in weak inversion before leveling off in strong inversion. n decreases by 3 % from the onset of weak inversion to the onset of strong inversion and decreases by approximately 6 % for a source–body voltage of $V_{SB} = 1$ V. n is slightly higher for pMOS devices due to an increase in process γ

Table 3.8 MOS bandgap energy, thermal voltage, intrinsic carrier concentration, Fermi potential, and moderate-inversion substrate factor over the −55 to 125°C military temperature range. The Fermi potential and substrate factor are for nMOS devices in a 0.18 μm CMOS process

T (°C)	T (K)	E_g (eV)	U_T (mV)	n_i (1/cm^3)	$PHI = 2\phi_F$ (V)	n (n_0) (in MI)
−55	218	1.135	18.784	1.87×10^6	0.954	1.272
−20	253	1.127	21.800	1.69×10^8	0.911	1.276
0	273	1.122	23.524	1.35×10^9	0.885	1.279
27	300	1.115	25.850	1.45×10^{10}	0.850	1.282
50	323	1.109	27.832	8.12×10^{10}	0.819	1.286
70	343	1.103	29.555	3.04×10^{11}	0.792	1.289
100	373	1.094	32.140	1.70×10^{12}	0.750	1.294
125	398	1.086	34.294	5.94×10^{12}	0.715	1.298

Values are calculated for $n_i = 1.45 \times 10^{10}$/cm^3 ($T = 300$ K), $N_B = 2 \times 10^{17}$/cm^3, PHI ($T = 300$ K) = $2\phi_F = 0.85$ V, $\gamma = 0.56\,\text{V}^{1/2}$, $V_{SB} = 0$ V, and $V_{EFF} = V_{GS} - V_T = 40$ mV (moderate inversion) to model nMOS devices in a 0.18 μm CMOS process.

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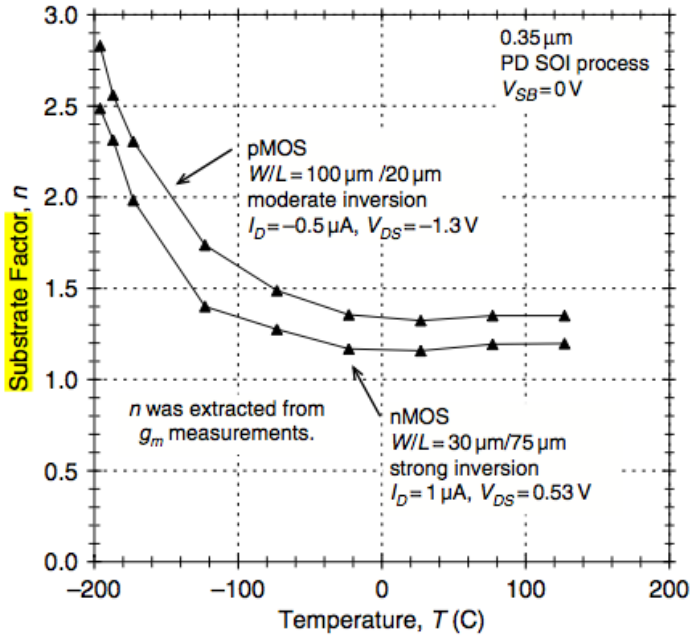

Figure 3.4 Measured substrate factor, n, from −196 to 127 °C (77 to 400 K) for nMOS and pMOS devices in a 0.35 µm PD SOI CMOS process. n is nearly independent of temperature except at very cold temperatures below −73 °C (200 K). n almost doubles at −196 °C (77 K), most likely due to increasing interface capacitance. Reproduced by permission of the Institute of Electrical and Electronic Engineers © 2004, from [20]

Table 3.9 MOS substrate factor, thermal voltage, low-field mobility, and low-field transconductance factor with resulting technology current over the −55 to 125°C military temperature range for nMOS devices in a 0.18 µm CMOS process

T (°C)	T (K)	n (n_0) (in MI)	U_T (mV)	μ_0 (cm²/V·s)	$k_0 = \mu_0 C'_{OX}$ (µA/V²)	$I_0 = 2n_0 k_0 U_T^2$ (µA)
−55	218	1.272	18.784	681.3	572.9	0.514
−20	253	1.276	21.800	544.9	458.3	0.556
0	273	1.279	23.524	486.1	408.8	0.578
27	300	1.282	25.850	422.0	354.9	0.608
50	323	1.286	27.832	377.7	317.7	0.633
70	343	1.289	29.555	345.2	290.3	0.654
100	373	1.294	32.140	304.4	256.0	0.684
125	398	1.298	34.294	276.2	232.3	0.709

Values are calculated for μ_0 $(T = 300\,\text{K}) = 422\,\text{cm}^2/\text{V}\cdot\text{s}$, $C'_{OX} = 8.41\,\text{fF}/\mu\text{m}^2$, and a mobility temperature exponent of −1.5 to model nMOS devices in a 0.18 µm CMOS process. The substrate factor is from Table 3.8.

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As mentioned earlier, the moderate inversion substrate factor, n = n0, given in Table 3.9, is nearly constant over the −55 to 125°C temperature range.

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... the substrate factor, n, which has typical values of 1.4, 1.35, and 1.3 in weak, moderate, and strong inversion for typical bulk CMOS processes.

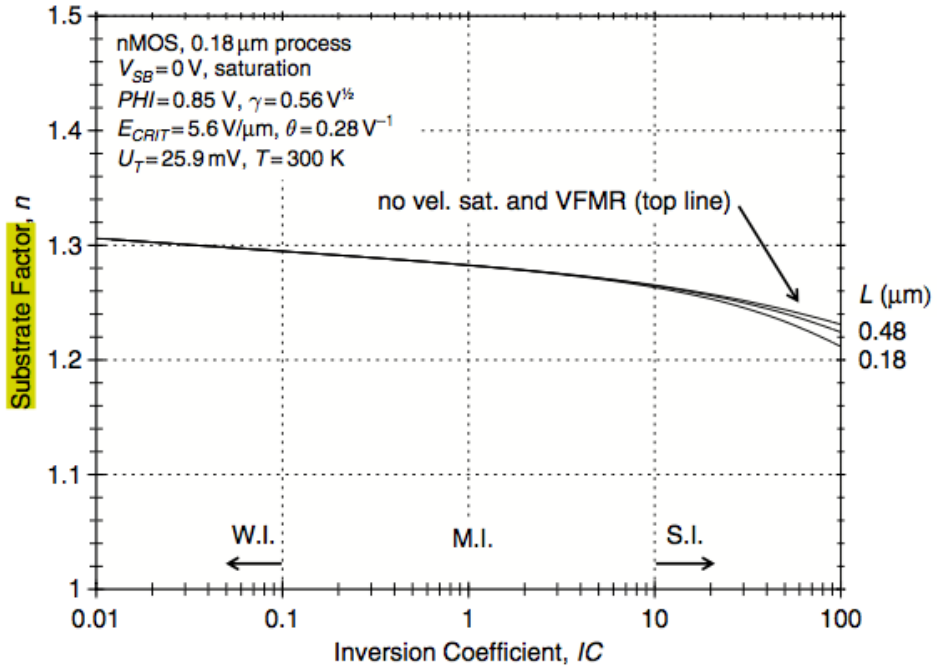

Figure 3.30 Predicted substrate factor, n, versus inversion coefficient, IC, for $L = 0.18$ and $0.48\,\mu$m, nMOS devices in a $0.18\,\mu$m CMOS process. n decreases slightly with increasing inversion coefficient and is within $\pm 3\,\%$ of an average value of 1.270, except for short-channel devices where n decreases further because of the increase in gate–source voltage due to velocity saturation effects. n decreases by approximately $6\,\%$ for a source–body voltage of $V_{SB} = 1$ V and is slightly higher for pMOS devices due to an increase in process γ. Figure 3.2 showed n versus the gate–source voltage. n is similar for all CMOS processes, increasing with γ