Expressing g_m and r_{ds} in terms of the transconductance efficiency, g_m/I_D, and Early voltage, V_A, gives A_{Vi} as

$$A_{Vi} = g_m \cdot r_{ds} = \left(\frac{g_m}{I_D} \cdot I_D\right) \cdot \left(\frac{V_A + V_{DS}}{I_D}\right) = \frac{g_m}{I_D} \cdot (V_A + V_{DS}) \approx \frac{g_m}{I_D} \cdot V_A$$
$$= \frac{g_m}{I_D} \cdot V_A \ (V_{DS} \text{ included}) \tag{3.90}$$

The rightmost approximation results from neglecting the operating V_{DS} since V_A is usually somewhat greater than V_{DS}. However, as mentioned for Equation 3.52 near the beginning of Section 3.8.4, V_A is often defined where it includes V_{DS} such that r_{ds} directly equals V_A/I_D or g_{ds} directly equals I_D/V_A. This convention is used throughout this book.

Equation 3.90 shows that A_{Vi} is equal to the product of the transconductance efficiency and Early voltage. While it is sometimes believed that maximum voltage gain is achieved at minimum drain current, A_{Vi} is independent of the drain current when evaluated in terms of the inversion coefficient and channel length. A given voltage gain can be realized at any drain current providing devices can be physically sized for the selected drain current, inversion coefficient, and channel length. For example, if a voltage gain of 200 V/V is obtained in a MOS circuit at bias currents of 1 μA, this same voltage gain can be obtained at bias currents of 10 μA by simply scaling all widths up by a factor of 10 to maintain the selected inversion coefficients and channel lengths. This is equivalent to paralleling 10 identical devices everywhere giving a factor-of-10 increase in drain current, a factor-of-10 increase in transconductance, and a factor-of-10 increase in drain–source conductance. This gives no change in voltage gain because transconductance and drain–source conductance increase equally. For voltage gain alone, there would obviously be no advantage in selecting higher drain currents. However, gate-referred noise and DC mismatch voltages are lower at higher drain current because of higher input-device g_m, lowering thermal noise, and larger device areas, lowering flicker noise and local-area DC mismatch. These topics will be summarized later in Sections 3.10.2.3, 3.10.3.7, and 3.11.1.7.

As discussed in Section 3.8.4.2, DIBL effects can significantly contribute to g_{ds}, especially for short-channel devices operating at low levels of inversion. As a result, DIBL effects can significantly affect A_{Vi}. It is useful then to separate out the CLM component of A_{Vi} that is usually dominant and the DIBL component that may be dominant. Separating A_{Vi} using CLM and DIBL components of g_{ds} gives

$$A_{Vi} = \frac{g_m}{g_{ds}(\text{CLM}) + g_{ds}(\text{DIBL})} = g_m \left(r_{ds}(\text{CLM}) \parallel r_{ds}(\text{DIBL})\right)$$
$$= A_{Vi}(\text{CLM}) \parallel A_{Vi}(\text{DIBL}) \tag{3.91}$$

where

$$A_{Vi}(\text{CLM}) = \frac{g_m}{g_{ds}(\text{CLM})} = g_m \cdot r_{ds}(\text{CLM}) = \frac{g_m}{I_D} \cdot V_A(\text{CLM}) \tag{3.92}$$

and

$$A_{Vi}(\text{DIBL}) = \frac{g_m}{g_{ds}(\text{DIBL})} = g_m \cdot r_{ds}(\text{DIBL}) = \frac{g_m}{I_D} \cdot V_A(\text{DIBL}) \tag{3.93}$$

Sections 3.8.4.1 and 3.8.4.2 described V_A (CLM) and V_A (DIBL) as normalized measures of g_{ds} (CLM) and g_{ds} (DIBL). Equation 3.91 shows that A_{Vi} can be expressed as the parallel combination of CLM and DIBL components.