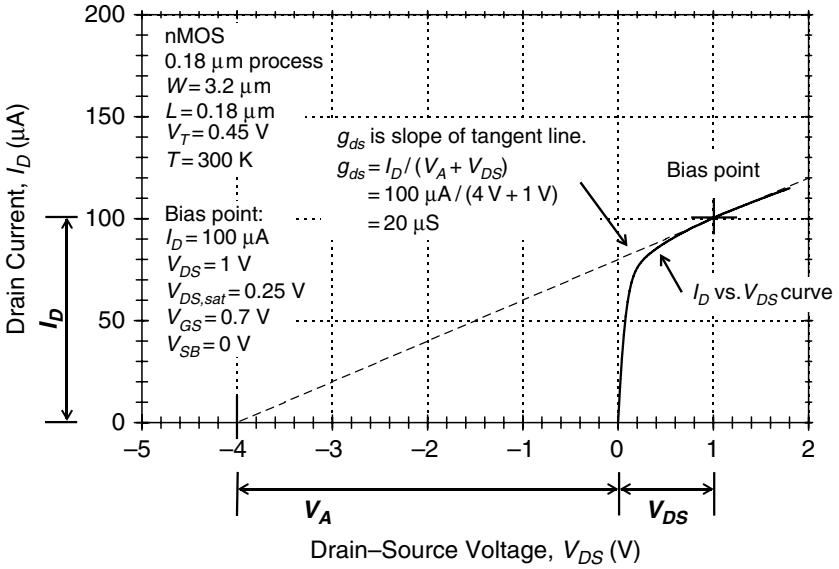

Figure 3.34 Illustration of MOS drain–source conductance calculation using the Early voltage. A tangent line is drawn touching the I_D versus V_{DS} curve at the bias point, and this line intersects the V_{DS} axis at the Early voltage. The drain–source conductance, g_{ds}, is the slope of the tangent line given by the drain bias current, I_D, divided by the sum of the Early voltage, V_A, and drain–source bias voltage, V_{DS}. Frequently, as throughout this book, V_{DS} is included in V_A such that $V_A = V_{gds} = (g_{ds}/I_D)^{-1}$, where $g_{ds} = I_D/V_A$. V_A is not a constant value for the process, but depends upon the channel length, inversion level, and V_{DS}

For the $W/L = 3.2\,\mu m/0.18\,\mu m$, nMOS device in a $0.18\,\mu m$ CMOS process shown in Figure 3.34, $V_A = 4\,V$ for the bias point of $I_D = 100\,\mu A$, $V_{GS} = 0.7\,V$, and $V_{DS} = 1\,V$. Throughout this book, we express the MOS bias point in terms of the inversion coefficient, which is near the onset of strong inversion at $IC = I_D/[I_0(W/L)] = 7.4$ from Table 3.6. This is for a shape factor of $S = W/L = 3.2\,\mu m/0.152\,\mu m$ using a technology current of $I_0 = 0.64\,\mu A$ and lateral diffusion, length reduction of $DL = 0.028\,\mu m$ listed in the process parameters of Table 3.2. At the bias point shown, the value of g_{ds} is $g_{ds} = I_D/(V_A + V_{DS}) = 100\,\mu A/(4\,V + 1\,V) = 20\,\mu S$.

Since V_A is usually somewhat greater than V_{DS}, it is customary in Equation 3.52 to neglect V_{DS} and approximate g_{ds} as the ratio of I_D to V_A ($g_{ds} = I_D/V_A$) or r_{ds} as the ratio of V_A to I_D ($r_{ds} = V_A/I_D$). Neglecting V_{DS} simplifies the estimate of g_{ds} or r_{ds}, while providing a conservatively larger or lower estimate, respectively, for design optimization.

Often, including throughout this book, the operating V_{DS} is effectively included in the value of V_A as noted in the second line of Equation 3.52. In this case, V_A corresponds to the full horizontal voltage seen in Figure 3.34, which includes V_{DS} such that g_{ds} directly equals I_D/V_A or r_{ds} directly equals V_A/I_D. When V_{DS} is included in the definition of V_A, V_A is actually the drain–source conductance, effective voltage, $V_{gds} = (g_{ds}/I_D)^{-1}$, which is the reciprocal of the drain–source conductance efficiency, g_{ds}/I_D. $g_{ds} = I_D/V_{gds}$ in an analogous way to $g_m = I_D/V_{gm}$, where $V_{gm} = (g_m/I_D)^{-1}$ is the transconductance effective voltage described earlier in Section 3.8.2.1. In applications where V_A includes the operating V_{DS} (V_A actually being V_{gds}), it is important to specify V_{DS}. Additionally, regardless of the definition of V_A, it is important to specify V_{DS} since g_{ds} or r_{ds} depends strongly on V_{DS} as discussed in the next section.

3.8.4.1 Due to channel length modulation

The primary contributor to MOS drain–source conductance for typical operating conditions is channel length modulation, commonly abbreviated as CLM. Unlike DIBL and hot-electron contributions