A High Stability Low Drop-out Regulator With Fast Transient Response

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***Abstract*—This paper presents a high stability, fast transient response, low-dropout voltage regulator (LDO) with a novel stepping several stages Miller capacitance frequency compensation and a slew-rate enhanced (SER) circuit. The proposed frequency compensation scheme can guarantee the LDO stable for the entire load. By utilizing the SRE circuit, the proposed LDO provides fast settling time and small voltage variation for a pulsed output current of 0 to I_{max}. Implemented in a 0.35-μm CMOS process, the proposed LDO achieve 80 degree phase margin and a PSR of 60 dB at 10kHZ. The proposed SRE circuit improves the transient response with 110mV voltage variation and 0.5μS settling time for a 250mA load step. The maximum output current is 250mA and the regulatered output voltage is 2.5V. The proposed LDO consumes only 20μA of ground current at no load condition. The load and line regulation are 40μV/mA (ΔI_{load}=250mA) and 2mV/V (ΔV_{DD}=2V).**

Keywords- frequency compensation; low drop-out regulator; stability; fast transient response

I. INTRODUCTION

As demand for low power operation high performance products such as mobile phones, MP3 and PDAs increase, integrated power supply regulation circuitry are widely used in battery operated applications. As one of the most versatile power converters, the low-dropout regulator (LDO) [1-4] has low static power and low noise, a small active area, a small dip at the output voltage and a fast transient response [6-7]. As a result, LDO is playing a critical role in integrated power management systems.

Fig. 1 illustrates the typical topology of the traditional LDO [1]. The regulator is composed of an error amplifier, pass transistor Mpout, high resistance feedback network R_1 and R_2. V_{ref} is voltage reference. R_L, C_{out} and R_{ESR} are the external resistor, capacitive load and equivalent series resistance of C_{out}. The associated capacitance and output resistance of pass transistor and error amplifier are depicted as C_{gd}, C_{par}, R_{ds} and R_{oa}, respectively. The traditional LDO in Fig. 1 has at least two significant poles which are located at node A and B below the unity-gain frequency [3]. Therefore, the traditional LDO is unstable. In order to improve the stability of the LDOs, plenty of research papers have been published till now. In [1-2], a large output capacitor and its equivalent series resistance are introduced to insert a zero cancel the second pole. As the unity-gain frequency increases with the load current [1] and the R_{ESR} varies with temperature, the compensation scheme based on the pole-zero cancellation can't enable the LDOs' stability. Some proposed solution [3-4] to this problem is to put a bypass path in the feedback or put two compensation capacitances. The common drawbacks are the zero moves as the output voltage of LDO changes and two compensation capacitances demands more chip area.

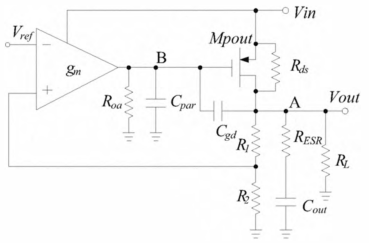

Figure 1. The typical topology of the traditional LDO.

Another problem the classical LDOs face is the transient response [6-7]. For a pulsed output current of 0 to I_{max}, the transfer of charge from the external capacitor C_{out} to the load corresponds to a voltage drop $\Delta V_{out,max}$ at the output node. The time Δt_1 of the loop to response the transient is determined by the closed loop bandwidth of the system, the voltage variation at the parasitic gate capacitance C_{par}, and the slewing current charging the parasitic pole of pass transistor of the error amplifier. In order to reduce $\Delta V_{out,max}$ and Δt_1, a large external capacitor is used on conventional LDOs to improve the transient regulation. However, large C_{out} increases the board real estate and overall cost of the design and makes it not suitable for SOC designs.

To circumvent the aforementioned problems, a novel stepping several stages Miller capacitance frequency compensation is presented to stabilize the LDOs under the entire load. Besides, a SER circuit is added between the error amplifier and the pass transistor to provide fast react time and small voltage variation.

II. THE PROPOSED LDO STRUCTURE

The proposed LDO topology is shown in Fig. 2. It is composed of a high gain error amplifier, a buffer, a PMOS pass transistor, a feedback network, a voltage reference, a SRE circuit and stepping several stages Miller capacitance frequency compensation block. The corresponding schematic of the proposed LDO is illustrated in Fig. 3.

The high gain error amplifier's circuit structure [5-6] is single-stage folded cascode architecture with transistors M1-M11, which use PMOS differential pairs as input stage to convert voltage to current. The buffer which replaces the error amplifier to drive the large capacitance of pass transistor is composed of a simple PMOS source- follower with transistors M12 and M13. The SRE circuit is made up of transistors M14-M18.

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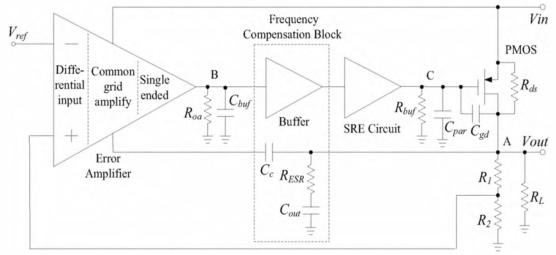

Figure 2. The structure of the proposed LDO with frequency compensation block.

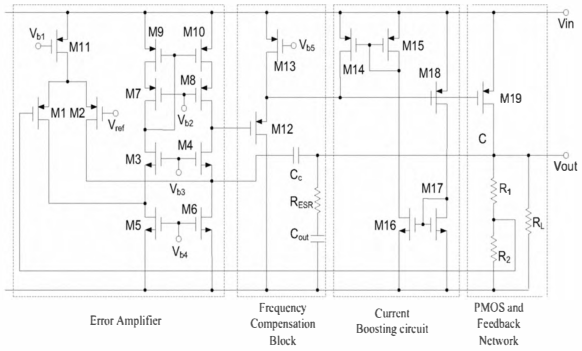

Figure 3. Schematic of the proposed LDO.

III. STABILITY AND TRANSIENT RESPONSE ANALYSIS

A. *Stability Analysis*

From the previous discussion, the traditional LDOs in Fig.1 exist one zero $Z_1 \approx 1/2\pi C_{out}R_{ESR}$ and two low frequency poles $P_1 \approx 1/2\pi C_{out}R_{out}$ located at the output of LDO and $P_2 \approx 1/2\pi C_{par}R_{oa}$ located at the output of the error amplifier. However, when the source-follower is added to driving the pass transistor in Fig. 2, the pole P_2 is split to two high frequencies poles, which are located at the node B and C, respectively. From the Fig. 2, the splitting poles can be given by the following expressions.

$$P_2' \approx 1/2\pi R_{oa}C_{buf} \tag{1}$$

$$P_2'' \approx 1/2\pi R_{buf}C_{par} \tag{2}$$

Where R_{oa} and R_{buf} are the output resistance of the error amplifier and the buffer, and C_{buf} is the parasitic capacitance at node B. In order to assure the LDO stability, the splitting pole P_2'' should be located at frequencies much higher than the unity-gain frequency to provide sufficient phase margin. Therefore, R_{buf} should be as small as possible. Increasing the transconductance of the source follower g_{m12} can reduce R_{buf} which can be expressed as follows.

$$R_{buf} = g_{m12}^{-1} = \left(2\mu_p C_{OX} I_{bias}\frac{W}{L}\right)^{-1/2} \tag{3}$$

Where μ_p is the mobility of hole, C_{ox} is the gate oxide capacitance per unit area, I_{bias} is the dc biasing current flowing through the source-follower and $(W/L)_{12}$ is the aspect ratio of the transistor M12. From the expression (3), although R_{buf} can be decrease by increasing $(W/L)_{12}$ or I_{bias} or both, larger $(W/L)_{12}$ would lead to larger equivalent capacitance C_{buf}, which in turn pushes the pole P_2' to a low frequency and affects the LDO stability. Simultaneously, increasing the current I_{bias} would increase more power consumption and the total quiescent current.

However, The SRE circuit can solve the problem. When the output load current is abruptly switched from low to high, the transistor M14's drain current increases, and the total current that flows into the output node C increase. Therefore, the current needed through the transistor M12 is greatly reduced to realize small R_{buf}. And $(W/L)_{12}$ is also reduced, which leads the capacitance C_{buf} is also decreased. So the pole P_2'' to be located at a higher frequencies without dissipating additional power and quiescent current is reduced.

In order to analysis the LDO's stability, the small-signal block diagram [3-5] of the proposed LDO is shown in Fig. 4. Due to the small R_{buf}, P_2'' is located at frequencies much higher than the unity-gain frequency. Therefore, C_{par} is neglected in the small-signal analysis. Here, g_{m1}, g_{m4}, g_{m12} and g_{mp} are the transconductance of input differential stage M1, common-gate transistor M4, the buffer stage M12 and the PMOS pass transistor M19.

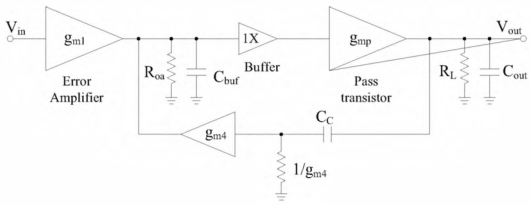

Figure 4. Small-signal block diagram of the proposed LDO.

As the trancondutance g_{mp} decreases with the load current and the dc open-loop gain A_0 is inversely proportional to the square root of the load current, the stability of the proposed LDO should be studied in two cases: I_{load}=0 and I_{load}>>0. The loop-gain transfer function is derived based on the following assumptions: (1) C_{out} and $C_c >> C_{buf}$, and (2) R_L, R_1 and $R_2 >> R_{ESR}$. As a result, the loop-gain transfer function of the proposed LDO is given as the following expression.

$$H(s) = \frac{A_0\left[1+\left(\frac{C_a}{g_{m4}}+C_{out}R_{ESR}\right)s+\frac{C_{out}R_{ESR}C_a}{g_{m4}}s^2\right]}{as^3+bs^2+cs+1} \tag{4}$$

$$A_0 = -\frac{R_2}{R_1+R_2}\cdot g_{m1}g_{m12}g_{mp}R_{oa}R_{buf}R_{out} \tag{5}$$

$$C_a = (1+g_{m4}g_{m12}g_{mp}r_{04}R_{buf}R_{out})C_C \tag{6}$$

$$a = R_{oa}R_{out}C_{buf}C_aC_{out}/g_{m4} \tag{7}$$

$$b = R_{oa}R_{out}C_{buf}C_{out} \tag{8}$$

$$c = R_{out}(C_{buf}+g_{mp}R_{oa}C_a+C_{out}) \tag{9}$$

Where A_0 is the dc open-gain and C_a is the equivalent capacitance at the source of transistor M4 by Miller effect, and r_{04} is the bulk resistance of transistor M4.

When I_{load}=0, the transconductance g_{mp} and the output resistance R_{ds} of the PMOS pass transistor is at the minimum and maximum, and $C_{out} >> (C_{buf}+g_{mp}R_{oa}C_a)$, respectively. As a

result, the loop-gain transfer function can be approximately expressed as follows.

$$H(s)|_{I_{load}=0} \approx \frac{A_0(1+sC_{out}R_{ESR})(1+C_a s/g_{m4})}{(1+C_a s/g_{m4})(1+sR_{oa}C_{buf})(1+sR_{out}C_{out})} = \frac{A_0(1+C_{out}R_{ESR}s)}{(1+sR_{oa}C_{buf})(1+sR_{out}C_{out})} \quad (10)$$

Thus, the poles and zeros are given as follows.

$$P_{-3dB|I_{load}=0} = 1/2\pi R_{out}C_{out} \quad (11)$$

$$P_{2|I_{load}=0} = 1/2\pi R_{oa}C_{buf} \quad (12)$$

$$Z_1 = 1/2\pi R_{ESR}C_{out} \quad (13)$$

As indicated in Eq. (11) and Eq. (12), the two poles $P_{-3dB|Iload=0}$ and $P_{2|Iload=0}$ are located at the output of the LDO and the error amplifier, respectively. Since C_{buf} and R_{ESR} is small, both $P_{2|Iload=0}$ and Z_1 are higher than the unity-gain frequency. Moreover, the zero Z_1 would cancel the pole $P_{2|Iload=0}$. Therefore, there is only a pole $P_{-3dB|Iload=0}$ below the unity-gain frequency, which guarantees the proposed LDO to achieve great phase margin under I_{load}=0.

When the load current increases significantly, the transconductance g_{mp} also increases. Therefore, C_{out} << (C_{buf}+$g_{mp}R_{oa}C_a$), and the loop-gain transfer function in the case of I_{load}>>0 is given as follows.

$$H(s)|_{I_{load}>>0} \approx \frac{A_0(1+sC_{out}R_{ESR})(1+C_a s/g_{m4})}{(1+\frac{C_a s}{g_{m4}})(1+s\frac{C_{buf}C_{out}}{g_{mp}C_a})(1+sg_{mp}C_aR_{oa}C_{out})} = \frac{A_0(1+sC_{out}R_{ESR})}{(1+s\frac{C_{buf}C_{out}}{g_{mp}C_a})(1+sg_{mp}C_aR_{oa}C_{out})} \quad (14)$$

From Eq. (14), when I_{load}>>0 the loop gain transfer function has also two poles and a zero which are expressed as follows.

$$P_{-3dB|I_{load}>>0} = 1/2\pi g_{mp}C_aR_{oa}C_{out} \quad (15)$$

$$P_{2|I_{load}>>0} = g_{mp}C_a/2\pi C_{buf}C_{out} \quad (16)$$

$$Z_1 = 1/2\pi R_{ESR}C_{out} \quad (13)$$

Under this condition, the LHP zero generated by the output capacitance and its equivalent series resistance would cancel the non-dominant pole $P_{2|Iload>>0}$, and both the LHP zero Z_1 and $P_{2|Iload>>0}$ are located at above the unity-gain frequency due to the small value of R_{ESR} and C_{buf}. Therefore, there is only a pole $P_{-3dB|Iload>>0}$ below the unity-gain frequency and the LDO is stable.

B. Transient Response Analysis

Fig. 5 shows the equivalent circuit and a load current step for LDO transient response. For a pulsed output current of 0 to I_{max}, the maximum output voltage variation $\Delta V_{out,max}$ and the react time Δt_1 of the loop are approximately determined as follows.

$$\Delta V_{out,\max} \cong I_{\max}\Delta t_1 / C_{out} \quad (17)$$

$$\Delta t_1 \approx 1/BW_{cl} + t_{sr} = 1/BW_{cl} + C_{par}\Delta V / I_{sr} \quad (18)$$

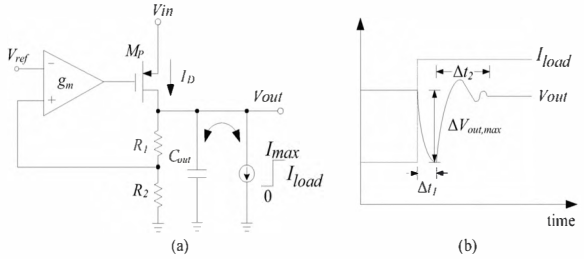

Figure 5. (a) Equivalent circuit for transient response. (b) Transient response to load current step.

Where I_{max} is the maximum current, BW_{cl} is the closed loop bandwidth of the system, t_{sr} is the slew-rate time associated with parasitic pole of the pass transistor, ΔV is the voltage variation at the parasitic gate capacitance C_{par}, and I_{sr} is the slewing current charging the parasitic pole of pass transistor of the error amplifier.

From the previous analysis, increasing BW_{cl} or I_{sr} or both can reduce the $\Delta V_{out,max}$ and Δt_1. Larger BW_{cl} is difficult to realize and in turn pushes the dc gain to a low value. Therefore, increasing I_{sr} is a great choose to improve to transient response, which can be realized by the SRE circuit. The slew-rate current I_{sr} of the error amplifier is not constant for the proposed circuit due to the SRE circuit, which can be expressed as follows.

$$I_{sr} = I_{bias} + xI_{boost} \quad (19)$$

Where I_{bias} and I_{boost} are the current flowing through transistor M12 and M18, and x is corresponds to a constant mirror ratio, which is determined by the aspect of the transistors M14-M17 and is expressed as follows.

$$x = \frac{(W/L)_{14}}{(W/L)_{15}} \bullet \frac{(W/L)_{16}}{(W/L)_{17}} \quad (20)$$

During the low load current conditions, the voltage at node C maintain unchanging and the current I_{boost} is negligible. During the transient from no load to full load, the decrease in the voltage at node C causes an increase in the transient current I_{boost} through M18, as the gate-source voltage of M18 and M19 is the same. The increasing transient current flows through M17, which then mirrors through M16 and M14. As a result, the drain current of M14 xI_{boost} then increases to charge the large gate capacitance of the pass transistor M19 until the point in which the drain current of M19 compensates the load current stepping and allows V_{out} to return back to its steady state. Therefore, I_{sr} is increased by the SRE circuit and $\Delta V_{out,max}$ and Δt_1 decrease.

IV. EXPERIMENTAL RESULT

Implemented in 0.35-μm CMOS process, the proposed LDO is tested for V_{ref} =2.5V, V_{dd} =5V and the ceramic output capacitor C_{out} and the ESR is 0.1μF and 0.5Ω. The input voltage range is designed from 4V to 6V for portable applications. The typical dropout voltage of 200mV at the maximum load current 250mA is achieved.

The simulated open-gain transfer functions of the proposed LDO under no load current and full load current are shown in Fig. 6. Simulated results of the ac response illustrates only a pole existence below the unity-gain frequency and achieves a good phase margin of approximately 80 degrade under the entire load current.

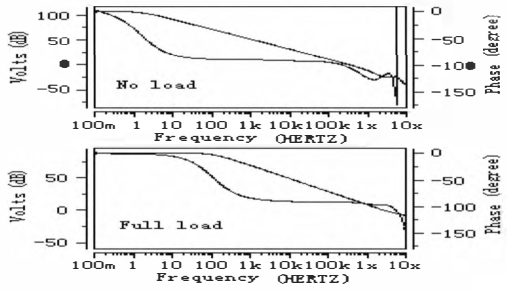

Figure 6. Simulated open-gain ac response of the proposed LDO at no load and full load.

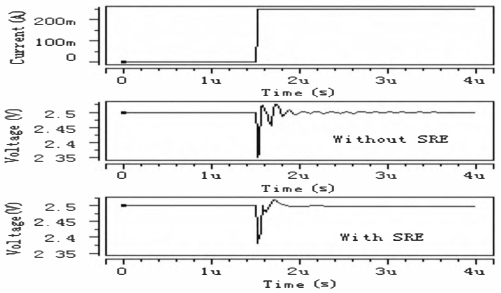

Figure 7. Measured load transient response of the proposed LDO.

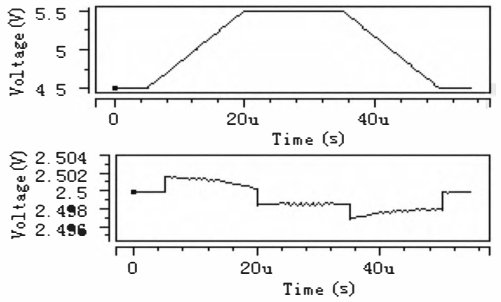

Figure 8. Measured line transient response of the proposed LDO.

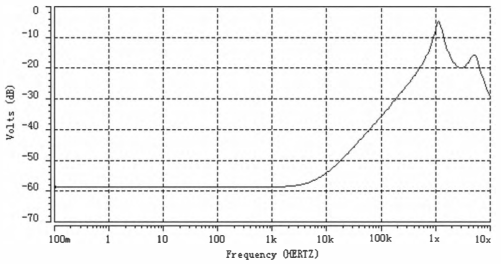

Figure 9. Measured the proposed LDO PSR at 20mA load condition.

Fig. 7 shows the load transient response of the proposed LDO when I_{load} is switching between 0mA and 250mA. The maximum output voltage variation without SRE circuit is approximate 170mV and the output voltage reaches a stable state with in 2μS. The simulation results with SRE circuit show the settling time is reduced from 2μS to 0.5μS and the maximum output voltage variation is less than 110mV.

The measured line transient response of the proposed LDO is shown in Fig. 8. When the change in the input voltage is 1V with rise and fall time of 10μS, the output voltage changes by less than 8mV at I_{load}=20mA. Fig. 9 shows the PSR of the proposed LDO for different frequencies at 20mA load condition. The LDO achieves approximately 60dB PSR in the range of 0-10KHz.

In order to provide a clear picture of the performance in the proposed LDO, the performance summary based on the simulated results is shown in Table 1.

Table 1. Simulation results of the proposed LDO

Item	Spec.
Technology	0.35-μm CMOS
Maximum load current	250mA
Quiescent current	20μA
Dropout voltage	200mV@250mA
PSRR(0-10kHz)	60dB
Load regulator	40μV/mA(ΔI_{load}=250mA)
Line regulator	2mV/V(ΔV_{DD}=2V)
Load transient response without SRE	Settling time: 2μS
	Voltage dip:170mV
Load transient response with SRE	Settling time: 0.5μS
	Voltage dip:110mV
Line transient response with SRE	Voltage dip: < 5mV

V. CONCLUSION

A fast response LDO with stepping several stages Miller capacitance frequency compensation is presented in this paper. The proposed frequency compensation scheme can guarantee the LDO stable for the entire load. By utilizing the SRE circuit, the proposed LDO provides fast settling time and small voltage variation.

ACKNOWLEDGMENT

The authors would like to thank The National High Technology Research and Development Program of China (No. 2007AA12Z332), Technology Foundation of Wuhan city for the financial support.

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