Curvature-Compensated BiCMOS Bandgap with 1-V Supply Voltage

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***Abstract*—In this paper, we present a bandgap circuit capable of generating a reference voltage of 0.54 V. The circuit, implemented in a submicron BiCMOS technology, operates with a supply voltage of 1 V, consuming 92 μW at room temperature. In the bandgap circuit proposed, we use a nonconventional operational amplifier which achieves virtually zero systematic offset, operating directly from the 1-V power supply. The bandgap architecture used allows a straightforward implementation of the curvature compensation method. The proposed circuit achieves 7.5 ppm/K of temperature coefficient and 212 ppm/V of supply voltage dependence, without requiring additional operational amplifiers or complex circuits for the curvature compensation.**

***Index Terms*—Analog integrated circuits, MiCMOS analog integrated circuits.**

I. Introduction

SUPPLY voltage is scaling down because of reducing oxide thickness and increasing demand for low-power portable equipment. Currently, 1.8-V power supplies are commonly used; soon, circuits operating with 1.2 V ($\pm$10%) or less will be introduced. The threshold voltage of MOS transistors, however, is not scaling down as much as the supply voltage. Therefore, this relatively high threshold calls for new techniques in the design of basic analog blocks. One key component for analog systems is the bandgap voltage generator. Conventional structures allow us to achieve a reference voltage of about 1.2 V with minimum sensitivity to temperature variations. Of course, when the supply voltage goes down below 1.2 V, it is no longer possible to use the conventional structures, and designing the required operational amplifier also becomes quite difficult. This paper discusses a bandgap architecture capable of operating with a 1-V supply, while using a conventional BiCMOS technology with a threshold voltage of about 0.7 V for both n-channel and p-channel transistors. The circuit also incorporates a network that, despite its simplicity, allows us to accurately correct the curvature error, thus limiting the voltage variation to 7.5 ppm/K in the temperature range from 0 °C to 80 °C.

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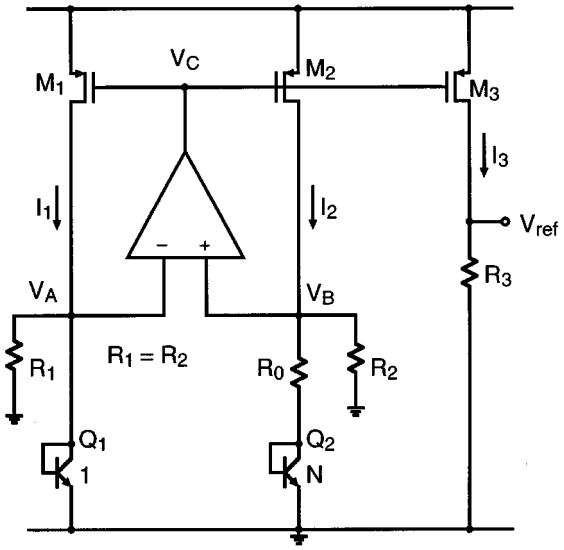

Fig. 1. Schematic of the bandgap circuit.

II. Low-Voltage Bandgap

Two components build up the output voltage of a bandgap reference. One is the voltage across a directly biased diode (base–emitter voltage $V_{\rm BE}$) and the other is a term proportional to the absolute temperature (PTAT). The negative temperature coefficient of the former term compensates for the positive temperature coefficient of the latter. If $V_T = kT/q$ is used to obtain a PTAT voltage, it is well known that we have to multiply V_T by approximately 22 to compensate for the temperature dependence of the diode voltage. If this condition is satisfied, the generated bandgap voltage becomes approximately 1.2 V. Using a supply voltage (V_{DD}) as low as 1 V, obviously 1.2 V cannot be produced; instead, we can generate a fraction of 1.2 V with similar temperature features. Since the bandgap voltage is given by

$$V_{\rm BG} = V_{\rm BE} + n\frac{kT}{q} \tag{1}$$

we achieve a fraction of the traditional bandgap voltage by scaling both terms of (1), using currents terms proportional to $V_{\rm BE}$ and to V_T, respectively. These currents are suitably added and transformed into a voltage with a resistor. We compensate for the temperature dependence of the resistors used by fabricating them with the same kind of material. Fig. 1 shows the schematic diagram of a circuit [1], which implements the described operation.

Two diode connected bipolar transistors with emitter area ratio N drain the same current, leading to a $\Delta V_{\rm BE}$ equal to $V_T \ln(N)$. Therefore, the current in R_0 is PTAT. The operational amplifier forces the two voltages V_A and V_B to be equal, thus producing a current in the nominally equal resistors R_1 and R_2 proportional to $V_{\rm BE}$. As a result, the current in M_1, M_2 and $M_3 (I_1 = I_2 = I_3)$ is given by

$$I_1 = \frac{V_T \ln(N)}{R_0} + \frac{V_{\rm BE}}{R_1}. \tag{2}$$

The output voltage is then given by

$$\begin{aligned} V_{\rm out} &= I_1 R_3 = V_T \left[\frac{R_3 \ln(N)}{R_0}\right] + V_{\rm BE}\left(\frac{R_3}{R_1}\right) \\ &= \frac{R_3}{R_1}\left[\frac{R_1 \ln(N)}{R_0} V_T + V_{\rm BE}\right]. \end{aligned} \tag{3}$$

The compensation of the temperature coefficients of V_T and $V_{\rm BE}$ is ensured by choosing values of N and of the R_1/R_0 ratio which satisfy

$$\frac{R_1 \ln(N)}{R_0} = 22. \tag{4}$$

In particular, to minimize the spread of the resistors, we chose $N = 24$.

Moreover, since transistors M_1, M_2, and M_3 maintain almost the same drain–source voltage $V_{\rm DS}$, independently of the actual supply voltage, the power supply rejection ratio of the circuit is only determined by the operational amplifier.

By inspection of the circuit, we observe that the minimum supply voltage is determined by the $V_{\rm BE}$ plus a saturation voltage of a p-channel transistor. Therefore, 1 V can be enough to operate the circuit. However, the supply voltage used must ensure proper operation of the operational amplifier and, indeed, this is the true limit of the circuit. Banba *et al.* [1] propose a similar structure, but the operational amplifier requires 1.8 V to function properly.

III. Operational Amplifier Design

The bandgap circuit needs an operational amplifier whose input common-mode voltage is around 0.65 V (the $V_{\rm BE}$). Moreover, since the output node drives p-channel current sources, its output quiescent voltage should be below $V_{DD} - V_{\rm th,\,p}$. Assuming $V_{DD} = 1$ V and $V_{\rm th,\,p} = 0.7$ V, the output voltage results as low as 0.15–0.2 V. Moreover, the gain of the operational amplifier must be around 60 dB without any bandwidth constraints. The above design conditions lead to the following considerations.

- The input common-mode voltage makes it difficult to accommodate an n-channel input differential stage. Possibly, a level shift of the input voltages by 150–200 mV toward the supply rail is necessary.
- The low output voltage prevents the use of cascode configurations. Therefore, two-stage architectures should be used.
- The required biasing conditions can lead to a significant offset, which can become the key limit to the correct operation of the bandgap circuit.

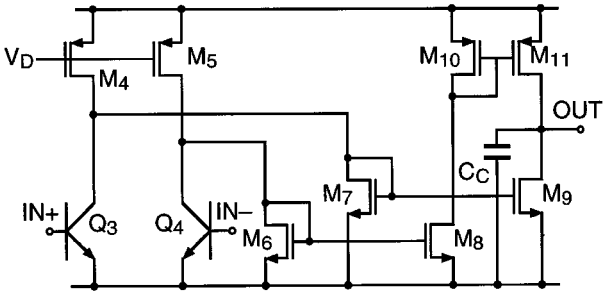

Fig. 2. Schematic of the two-stage operational amplifier used.

A careful analysis of the above issues shows that we can use a CMOS technology with a 1-V supply only if the thresholds of the n-channel and p-channel devices are 0.5 V or below. However, a BiCMOS technology (or a CMOS with lateral BJT) allows us to design an operational amplifier suitable for 1-V operation even with MOS threshold voltages as high as 0.7 V. Fig. 2 shows the circuit schematic of the proposed two-stage operational amplifier. The circuit does not use an input differential stage but two grounded bipolar transistors (Q_3 and Q_4).

The bias current in the differential stage of a conventional operational amplifier is controlled with a suitable current source. However, the current source needs at least a saturation voltage to operate properly, thus subtracting at least 0.15 V from the supply voltage budget. The circuit in Fig. 2 spares this component. The combination of the diode connected BJT in the bandgap and the BJT of the input stage constitutes a current mirror. Therefore, the currents in the input stage of the operational amplifier do not need control, being a replica of the current in the bandgap structure. The bias voltage V_D, generated within the startup circuit, is also obtained from the bandgap circuit by mirroring the PTAT current of Q_1 (Fig. 1). The signal current generated by the input differential pair Q_3–Q_4 is folded and collected by two diode connected MOS transistors (M_6 and M_7). Hence, we obtain the following differential gain

$$A_d = \frac{g_{m,\,\rm BJT}}{g_{m,\,\rm MOS}} = \frac{I_{\rm BJT}/V_T}{2I_{\rm MOS}/(V_{GS} - T_{\rm th,\,n})} \tag{5}$$

where the suffix BJT refers to the input BJT and the suffix MOS refers to the diode loads M_6 and M_7. Assuming $(V_{GS} - V_{\rm th,\,n}) = 4V_T$ and using $I_{\rm BJT} = 4I_{\rm MOS}$, we obtain a gain of 8. Since the input gain stage is fully symmetrical, its systematic offset is practically zero.

The second stage is a push–pull circuit. Since the quiescent value of the output voltage is one $V_{GS,\,p}$ below V_{DD}, the $V_{\rm DS}$ voltages of M_{10} and M_{11} match, and the systematic offset of the second stage is practically zero as well. Moreover, for the same reason, we achieve excellent power supply rejection ratio and common-mode rejection ratio. The bias current in the operational amplifier matches the current flowing in the bandgap, which in turn is designed low. However, since the bias current of the circuit has a PTAT feature, power consumption will increase proportionally to the absolute temperature. This variation is irrelevant even when using the circuit in the range from -20 °C to 120 °C.

The compensation capacitance C_C ensures the stability of the whole bandgap circuit under any operating conditions.

TABLE I
OPERATIONAL AMPLIFIER FEATURES

Parameter	*Value*
DC Gain	60 dB
Gain-Bandwidth Product	1.2 MHz
Phase Margin	63°
Output Referred Systematic Offset Voltage	625 μV
Supply Voltage	1 V
Current Consumption @ T = 25° C	35 μA

The operational amplifier was designed using a 0.8-μm BiCMOS technology. Its simulated features are summarized in Table I. The output referred systematic offset obtained is very small, as expected.

IV. STARTUP CIRCUIT

The proposed bandgap reference needs a more effective startup circuit than those usually adopted, consisting of simple pull-up or pull-down capacitors. In a conventional bandgap architecture the nonlinear I–V relationships of a diode and an N times larger diode with a resistance R_0 in series have two well-defined crossing points. Therefore, a very small current flowing for a short period of time in the diodes is sufficient to lead the circuit toward the proper operating point. By contrast, in the proposed architecture, the use of resistors in parallel to the diodes (R_1 and R_2) makes the two I–V relationships more linear, and consequently, the crossing points are much less defined. Moreover, in order to turn on the diodes (Q_1 and Q_2), a significant amount of current ($V_{\rm BE}/R_{1,2}$) has to flow in the resistors (R_1 and R_2). The startup circuit shown in Fig. 3 ensures that additional current is continuously provided to the diodes and the resistors until the bandgap circuit reaches the proper operating point.

In particular, if the current in Q_1 is zero, the current in Q_{S1} is zero as well, and the p-channel current sources (M_{S2} and M_{S3}) are off. The gate of M_{S1} is pulled down to ground, thus injecting a significant current into Q_1 and R_1. At the end of the startup phase, when the circuit reaches the normal operating conditions, the current in M_{S3} and the value of R_S used ($R_S > 2R_1$) bring the gate of M_{S1} close to V_{DD}, thus turning off the startup circuit. Observe that a weak startup current in the operational amplifier can be a source of a significant systematic offset, which could lead the bandgap to a metastable operating point. Fortunately, this is not the case in the circuit used, because we control the operational amplifier with the same reference current used in the bandgap (through Q_1 and V_D). Consequently, we achieve an exact tracking of currents in the input differential stage and in the current sources, nulling the systematic offset even during the startup phase.

V. CURVATURE COMPENSATION

The simple bandgap circuit in Fig. 1 compensates for the temperature dependences of the output voltage at the first order only. In fact, the $V_{\rm BE}$ voltage of a BJT does not change linearly with the temperature but, according to the relationship proposed in [2], it is given by

$$V_{\rm BE}(T) = V_{\rm BG} - (V_{\rm BG} - V_{\rm BE0})\frac{T}{T_0} - (\eta - \alpha)V_T \ln\frac{T}{T_0} \quad (6)$$

where η depends on the bipolar structure and is around 4, while α is equals 1 if the current in the BJT is PTAT and goes to 0 when the current is temperature independent. The simple bandgap architecture shown in Fig. 1 corrects the first term in (6) only, thus leading to a second-order temperature dependence.

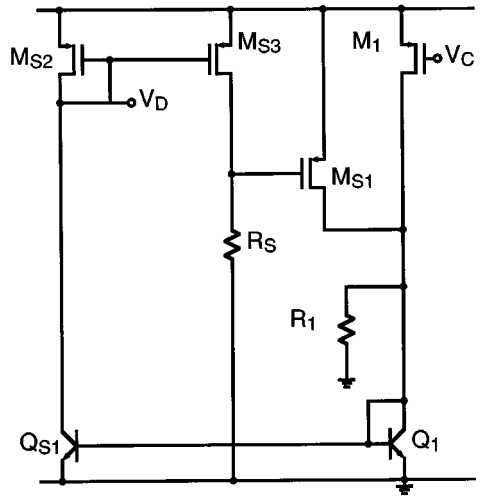

Fig. 3. Schematic of the startup circuit.

Various approaches to compensate for the nonlinear term have been proposed [3]–[7]. The solution proposed in [3] can be simply implemented in our circuit. The basic idea is to correct the nonlinear term by a proper combination of the $V_{\rm BE}$ across a junction with a temperature-independent current ($\alpha = 0$) and the $V_{\rm BE}$ across a junction with a PTAT current ($\alpha = 1$). By inspection of the circuit in Fig. 1, we observe that the current in the bipolar transistors (Q_1 and Q_2) is PTAT ($\alpha = 1$), while the current in the p-channel MOS transistors is at first-order temperature independent. Therefore, if we mirror the current flowing in p-channel MOS transistors (with M_{12}) and we inject it into a diode connected bipolar transistor (Q_3), as shown in Fig. 4, across Q_3 we produce a $V_{\rm BE}$ with a $\alpha \cong 0$. Using (6), the $V_{\rm BE}$ of bipolar transistors Q_3 and $Q_{1,2}$ can be expressed as

$$V_{{\rm BE},Q_3}(T) = V_{\rm BG} - (V_{\rm BG} - V_{\rm BE0})\frac{T}{T_0} - \eta V_T \ln\frac{T}{T_0} \quad (7)$$

and

$$V_{{\rm BE},Q_{1,2}}(T) = V_{\rm BG} - (V_{\rm BG} - V_{\rm BE0})\frac{T}{T_0} - (\eta - 1)V_T \ln\frac{T}{T_0} \quad (8)$$

respectively. The difference between $V_{{\rm BE},Q_3}(T)$ and $V_{{\rm BE},Q_{1,2}}(T)$ leads to a voltage proportional to the nonlinear term of (6), given by

$$V_{NL} \cong V_{{\rm BE},Q_3}(T) - V_{{\rm BE},Q_{1,2}}(T) = V_T \ln\frac{T}{T_0}. \quad (9)$$

Curvature compensation can now be achieved by subtracting from both I_1 and I_2 a current proportional to V_{NL}. In the com-

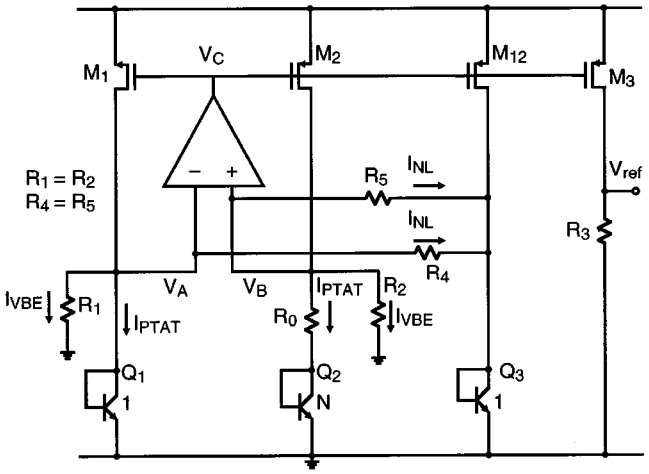

Fig. 4. Schematic of the proposed bandgap circuit with curvature compensation.

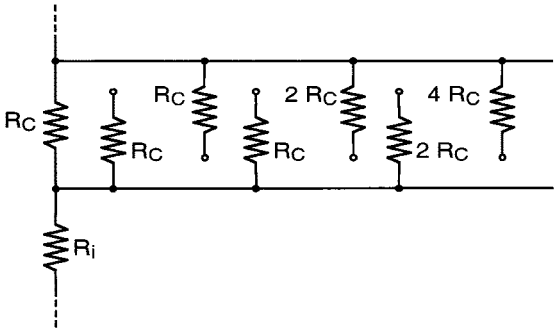

Fig. 5. Schematic of the programmable resistive network.

plete bandgap circuit shown in Fig. 4, this is obtained by introducing resistors R_4 and R_5 (nominally equal), which drain from M_1 and M_2 the required current (I_{NL}), thus leading to

$$V_{\text{out}} = V_T\left(\frac{R_3\ln(N)}{R_0}\right) + V_{\text{BE}}\left(\frac{R_3}{R_1}\right) + V_{NL}\left(\frac{R_3}{R_{4,5}}\right) = \frac{R_3}{R_1}\left(\frac{R_1\ln(N)}{R_0}V_T + V_{\text{BE}} + \frac{R_1}{R_{4,5}}V_{NL}\right). \quad (10)$$

The value of R_4 and R_5 which leads to the proper curvature correction, derived by comparing (8) and (10), is given by

$$R_{4,5} = \frac{R_1}{\eta - 1}. \quad (11)$$

The proposed implementation of the curvature compensation principle requires an additional current mirror and two resistors only. However, it is more effective than the solution presented in [3] and much less complex than other architectures [4]–[7], which use operational amplifiers or switched capacitor structures.

VI. Experimental Results

The proposed circuit was integrated using a 0.8-μm BiCMOS technology. Since we were not sure of the simulation accuracy and the variations with the process of the temperature effects, we designed resistors R_0, R_4 and R_5 using the resistive network shown in Fig. 5, to allow trimming of the linear and logarithmic compensation coefficients.

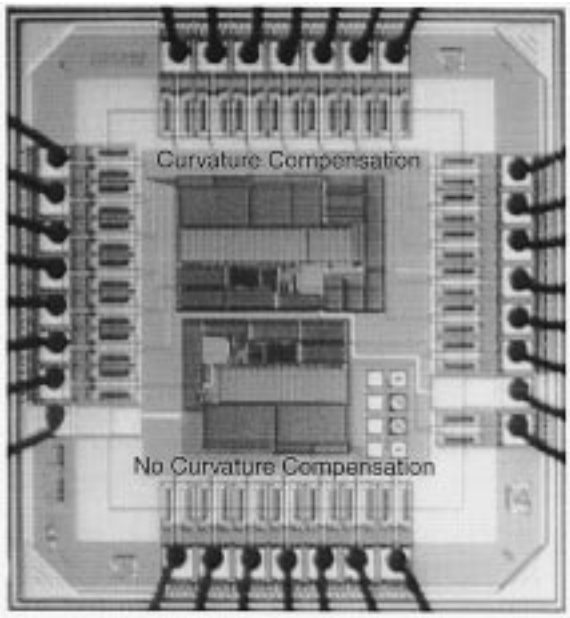

Fig. 6. Micrograph of the chip including two versions of the proposed bandgap circuit (with and without curvature correction).

In this circuit, a fixed term R_i is connected in series with an array of resistors whose value is a multiple of a given value R_C ($R_i = 12$ kΩ, $R_C = 2$ kΩ for resistor R_0 and $R_i = 30$ kΩ, $R_C = 4$ kΩ for resistor $R_{4,5}$). The eight terminals of the network are connected to external pins. With suitable external connections it is, therefore, possible to increase the value of R_i by 30% with steps of 1%. Since we use the same material for the fixed resistor and the programmable array, the resulting temperature coefficient is unchanged. With this resistive network, we could experimentally determine the optimum value of R_0 and $R_{4,5}$. Actually, experimental result performed on ten samples coming from the same wafer have shown that the optimal values of the resistances correspond to the values obtained in simulation ($R_0 = 13.5$ kΩ and $R_{4,5} = 32.25$ kΩ). The measurements reported in this section show the typical performances of the circuit. The spread among the samples is indeed negligible.

Fig. 6 shows the micrograph of the chip containing two versions of the proposed bandgap circuit, with and without curvature compensation. Obviously, the curvature compensated version has the 24 additional pins required for resistor trimming. The total chip area including pads is 3 mm^2. The values of the resistances and the transistor dimensions used, determined with extensive simulations of the circuit, are summarized in Table II.

Fig. 7 shows the typical measured output voltage of the proposed bandgap circuit as a function of temperature with and without curvature compensation. We observe that a variation of 800 μV in the temperature range from 0 °C to 80 °C is reduced by the curvature compensation to approximately 300 μV. Actually, the temperature dependence could be further reduced by placing the maximum of the V_{ref}–T curve in the middle of the temperature range by means of a more accurate adjustment of the linear correction term (resistor R_0). Fig. 7 demonstrates the effectiveness of the proposed curvature correction

TABLE II
RESISTANCE VALUES AND TRANSISTOR DIMENSIONS USED IN THE PROPOSED BANDGAP CIRCUIT

Component	*Parameter*
Q_1, Q_3, Q_{S1}	Normalized Area = 1
Q_2	Normalized Area = 24
M_1, M_2, M_3, M_{10}, M_{11}, M_{12}	W = 1000 μm, L = 10 μm
M_{S2}, M_{S3}	W = 350 μm, L = 4 μm
M_{S1}	W = 80 μm, L = 0.8 μm
M_4, M_5	W = 510 μm, L = 4 μm
M_6, M_7, M_8, M_9	W = 100 μm, L = 2 μm
R_0	12 ÷ 14 kΩ (Nominal 13.5 kΩ)
R_1, R_2	80 kΩ
R_3	35 kΩ
R_4, R_5	30 ÷ 34 kΩ (Nominal 32.25 kΩ)

TABLE III
PERFORMANCE SUMMARY OF THE PROPOSED BANDGAP CIRCUIT

Parameter	*Value*
Power Supply Voltage	1 V
Technology	0.8 μm BiCMOS
Bandgap Cell Area	
Without Curvature Compensation	0.20 mm^2
With Curvature Compensation	0.25 mm^2
Power Consumption @ T = 25° C	92 μW
Reference Voltage @ T = 25° C	536 mV
Temperature Variation (0° C ≤ T ≤ 80 ° C)	
Without Curvature Compensation	800 μV → 20 ppm / K
With Curvature Compensation	300 μV → 7.5 ppm / K
Dependence on the Supply Voltage	114 μV / V→ 212 ppm / V

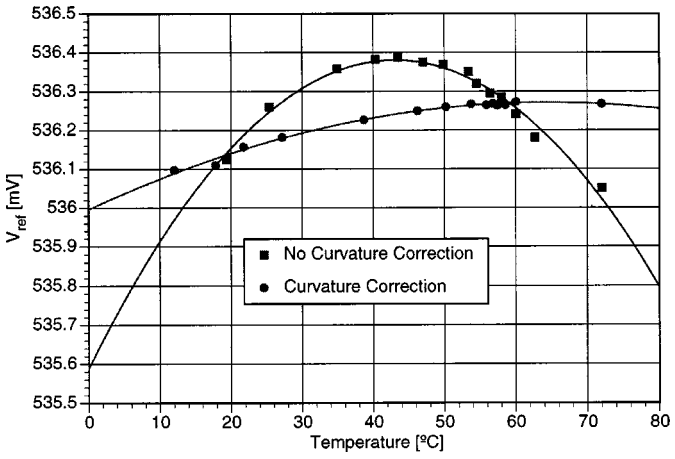

Fig. 7. Measured bandgap voltage as a function of temperature with and without curvature compensation.

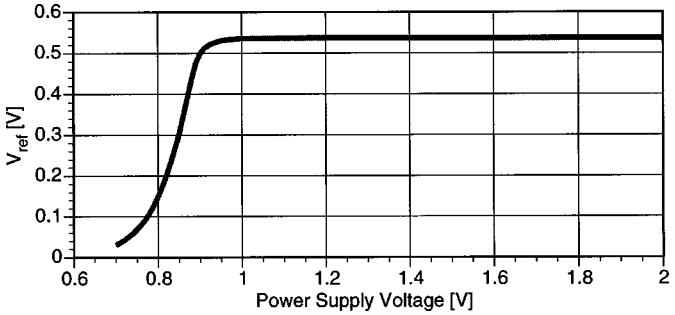

Fig. 8. Measured bandgap voltage as a function of the power supply voltage.

technique, since the nonlinear term of the temperature dependence is strongly attenuated.

The generated bandgap voltage as a function of the used supply voltage is shown in Fig. 8. The circuit operates properly with supply voltages higher than 0.95 V and achieves a dependence on the supply voltage as low as 212 ppm/V. The most significant performances of the circuit are summarized in Table III. The total current consumption of the circuit at room temperature is 92 μA.

VII. Conclusion

This paper presented a BiCMOS bandgap reference circuit which produces an output voltage of 0.54 V, starting from a supply voltage as low as 1 V. The circuit operates in the current domain and includes a nonconventional operational amplifier with virtually zero systematic offset. Accurate compensation of the output voltage temperature dependence is obtained with a simple but very effective implementation of the curvature correction technique. The circuit can be directly implemented also in a purely CMOS technology with a degradation of minimum power supply voltage due to the additional headroom required to design a CMOS operational amplifier. The proposed bandgap reference circuit, fabricated in a 0.8-μm BiCMOS technology, achieves a temperature coefficient of 7.5 ppm/K and dependence on the supply voltage of 212 ppm/V, with a power consumption of only 92 μW at room temperature.

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