True-Hspice™ Device Models Reference Manual

Release 2001.4, revision A
December 2001

True-Hspice Device Models Reference Manual, Release 2001.4, revision A, November 2001
Previous Version True-Hspice Device Models Reference Manual, Release 2001.4, November 2001

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Using This Manual

This manual describes all of the simulation devices models that Avant! Corporation provides for use with its in-circuit simulation products, including Star-Hspice, Star-Hspice XT, Star-Sim, and Star-Sim XT.

For information about which simulation device models each product supports, see the User Manual for the specific in-circuit simulator you are using. For example, to determine which of the simulation device models described in this manual are supported in the Avant! Star-Hspice in-circuit simulator, see the *Star-Hspice Manual*.

Audience

This manual is intended for design engineers who use Avant! in-circuit simulators to develop, test, analyze, and modify circuit designs.

Related Documents

The following documents pertain to this guide:

- Star-Hspice, Star-Time, and AvanWaves Installation Guide
- Star-Hspice and Star-Hspice XT Manuals
- Star-Sim, Star-Sim XT, and Star-Time User Guides
- Star-Hspice, Star-Sim, and AvanWaves Release Notes

If you have questions or suggestions about this documentation, send them to:

`techpubs@avanticorp.com`

Conventions

Avant! documents use the following conventions, unless otherwise specified:

Table 6.1: Typographical Conventions

Convention	Description
menuName > *commandName*	Indicates the name of the menu and the command name. For example: *Cell* > *Open* refers to the *Open* command in the Cell menu.
Tool: menuName > *commandName*	Indicates that a command is accessible only through an application tool. Tool is the tool through which you access the command, *menuName* is the name of the menu, and *commandName* is the name of the command. For example: *Data Prep: Pin Solution* > *Via* refers to the *Via* command on the Pin Solution menu, which you access by selecting *Data Prep* from the Tools menu in Apollo.
courier	In text, this font indicates a function or keyword that you must type exactly as shown. In examples, this font indicates system prompts, text from files, and messages printed by the system.
courier italic	Arguments appear in this font when the value of an argument is a string. The string must be enclosed with quotation marks.

Table 6.1: Typographical Conventions (Continued)

Convention	Description
times italic	Indicates commands, functions, arguments, file names, and variables within a line of text. When a variable is included in italicized text, the variable is enclosed by angle brackets (<>). For example, “the name of the technology file is <libraryName>.tf, where <libraryName> is the name of the library.”
[ ]	Denotes optional arguments, such as: *pin1* [*pin2*, ...*pinN*] In this example, you must enter at least one pin name, the other arguments are optional.
({*instanceName orientation*} ...)	Indicates that you can repeat the construction enclosed in braces.
. . .	Indicates that text was omitted.
’(item1 item2)	An apostrophe followed by parentheses indicate that the text within the parentheses enclose a list. When the list contains multiple items, the items are separated by spaces. Type this information exactly as it appears in the syntax.

Table 6.1: Typographical Conventions (Continued)

Convention	Description
|	Separates items in a list of choices. For example, on | off.
\	Indicates the continuation of a command line.

Obtaining Customer Support

If you have a maintenance contract with Avant!, you can obtain customer support by:

- Contacting your local Application Engineer (AE)
- Calling the Avant! Corporate office from 8:00 AM through 5:00 PM Pacific Standard Time (PST) at:

  `1-800-346-5953`

  Ask the receptionist for customer support.
- Emailing a description of the problem to the Hspice Support Center at:

  `hspice_nw@avanticorp.com`

Other Sources of Information

The Avant! external web site provides information for various products. You can access our web site at:

`http://www.avanticorp.com`

From our web site, you can register to become a member of the Avant! Users Research Organization for Real Applications (AURORA) user's group. By participating, you can share and exchange information pertaining to Integrated Circuit Design Automation (ICDA).

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Table of Contents

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Chapter 1
Overview of Models

A circuit *netlist* describes the basic functionality of an electronic circuit that you are designing. In HSPICE format, a netlist consists of a series of *elements*, which define the individual components of the overall circuit. You can use your Hspice-format netlist to perform an in-circuit simulation of your circuit design, before you turn that design into actual electronic circuitry. An in-circuit simulation verifies and debugs your design.

Your netlist can include several types of elements:

- Passive elements:
  - Resistors
  - Capacitors
  - Inductors
  - Mutual Inductors
- Active elements:
  - Diodes
  - Bipolar Junction Transistors (BJTs)
  - Junction Field Effect Transistors (JFETs)
  - Metal Semiconductor Field Effect Transistors (MESFETs)
  - Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)
- Transmission lines:
  - W element
  - T element
  - U element

Because there are more variations of the MOSFET model than any other type, and MOSFETs are all very detailed models, MOSFETs have their own separate volume (Volume 2) in this manual. Volume 1 describes all other model types.

Using Models to Define Netlist Elements

Avant! Corporation provides a series of standard *models*, which define various versions of each of the supported element types in an Hspice-format netlist. The individual elements in your netlist can then refer to these standard models. Using these models helps you to more quickly and efficiently create your netlist and simulate your circuit design.

For example, Avant! provides 26 different versions, or *levels*, of MOSFET models. An individual MOSFET element in your netlist can refer to one of these MOSFET models. That is, you do not need to define all of the characteristics (called *parameters*) of that MOSFET, within your netlist. Referring to standard models in this way reduces the amount of time required to:

- Create the netlist.
- Simulate and debug your circuit design.
- Turn your circuit design into actual circuit hardware.

Within your netlist, each element that refers to a model, is known as an *instance* of that model. Because your netlist refers to pre-defined device models, you reduce both the time required to create and simulate a netlist, and the risk of errors, compared to fully defining each element within your netlist.

Supported Models for Different Simulator Types

This manual describes the individual models that Avant! provides. You can use these models with several Avant! in-circuit simulators, including:

- Star-Hspice
- Star-Hspice XT
- Star-Sim
- Star-Sim XT

Each of these Avant! in-circuit simulators supports a specific sub-set of the available models. This manual describes all of the Avant! models that you can use in Hspice-format netlists.

Note: See the User Manual for the specific Avant! in-circuit simulator that you are using, for a list of the models that the simulator supports.

Selecting Models

To specify a device in your netlist, use both an element and a model statement. The element statement uses the name of the simulation device model, to reference the model statement. The following example uses the reference name MOD1, to refer to a BJT model. This example uses an NPN model type to describe an NPN transistor.

Example

```
Q3 3 2 5 MOD1 <parameters>
.MODEL MOD1 NPN <parameters>
```

You can specify parameters in both element and model statements. If you specify the same parameter in both an element and a model, then the element parameter (local to the specific instance of the model) always overrides the model parameter (global default for all instances of the model, where the parameter is not defined locally). The model statement specifies the type of device—for example, for a BJT, the device type might be NPN or PNP.

Enhancements to This Manual

The *True-Hspice Device Models Reference Manual*, Release 2001.4, revision A, provides the following enhancements compared to the previous release of this manual (Release 2001.2):

- Descriptions of all supported MOSFET models in the Avant! True-Hspice models. The previous release of this manual described only the MOSFET models that the Avant! Star-Sim XT simulator supports.
- Addition of the following new Bipolar Junction Transistor (BJT) models (see Chapter 4, "Using BJT Models"):
  - Level 9 VBIC99 Model
  - Level 10 Phillips MODELLA Bipolar Model
  - Level 11 UCSD HBT Model
- Addition of the following new Junction Field Effect Transistor (JFET) models (see Chapter 5, "Using JFET and MESFET Models"):
  - Level 7 TOM3 (TriQuint's Own Model III)
  - Level 8 Materka Model
- Addition of the following new Metal-Oxide Semiconductor Field Effect Transistor (JFET) model (see Chapter 10, "Selecting MOSFET Models: Level 47-63"):
  - Level 63 Phillips MOS11 Model
- Addition of a new section, Using the IBIS Buffer Component, in Chapter 7, "Using IBIS Models".
- Improved online navigation to specific reference information about Avant! True-Hspice device models.

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Chapter 2
Using Passive Device Models

This chapter describes model statements for passive devices. It includes statements for resistors, inductors, and capacitors.

Use the set of passive model statements, in conjunction with element definitions, to construct a wide range of board and integrated circuit-level designs. Passive device models let you include the following in any analysis:

- Transformers.
- PC board trace interconnects.
- Coaxial cables.
- Transmission lines.

The wire element model is specifically designed to model the RC delay and RC transmission line effects of interconnects, at both the IC level and the PC board level.

To aid in designing power supplies, a mutual-inductor model includes switching regulators and several other magnetic circuits, including a magnetic-core model and element. To specify precision modeling of passive elements, you can use the following types of model parameters:

- geometric
- temperature
- parasitic

This chapter describes:

Resistor Device Model and Equations

Wire RC Model

The wire element RC model is a CRC (pi) model. Use the CRATIO wire model parameter to allocate the parasitic capacitance of the wire element, between the input capacitor and the output capacitor of the model. This allows for symmetric node impedance for bidirectional circuits, such as buses.

Syntax

```
.MODEL mname R keyword=value <CRATIO=val>
```

mname — Model name. Elements use this name to reference the model.

R — Specifies a wire model.

keyword — Any model parameter name.

CRATIO — Ratio to allocate the total wire element parasitic capacitance, between the capacitor connected to the input node, and the capacitor connected to the output node, of the wire element pi model.

You can assign any value between 0 and 1, to CRATIO:

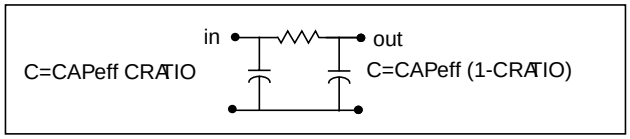
- 0 — Assigns all of the parasitic capacitance (CAPeff) to the output node.
- 0.5 — Assigns half of the parasitic capacitance to the input node, and half to the output node.
- 1 — Assigns all of the parasitic capacitance to the input node.

The default is 0.5.

CRATIO

- CRATIO values smaller than 0.5 assign more of the capacitance to the output node than to the input node.
- Values greater than 0.5 assign more of the capacitance to the input node than to the output node.

If you specify a CRATIO value outside the range of 0 to 1.0, simulation displays a warning, sets CRATIO to 0.5, and continues the analysis.



A wire-model resistor behaves like an elementary transmission line (see Chapter 6, "Using Transmission Lines"), if the `model` statement specifies an optional capacitor from the `n2` node to a bulk or ground node. The bulk node functions as a ground plane for the wire capacitance.

A wire has a *drawn length* and a *drawn width*. The resistance of the wire is the effective length, multiplied by RSH, then divided by the effective width.

To avoid syntactic conflicts, if a resistor model uses the same name as a parameter for *rval* in the element statement, then simulation uses the model name. In the following example, R1 assumes that REXX refers to the model, and not to the parameter.

```
.PARAMETER REXX=1
R1 1 2 REXX
.MODEL REXX R RES=1
```

Wire Model Parameters

Name (Alias)	Units	Default	Description
BULK	gnd		Default reference node for capacitance.
CAP	F	0	Default capacitance.
CAPSW	F/m	0	Sidewall fringing capacitance.
COX	F/m^2	0	Bottomwall capacitance.
DI		0	Relative dielectric constant.
DLR	m	0	Difference between drawn length and actual length (for resistance calculation only). Capacitance calculation uses DW. DLReff=DLR · SCALM
DW	m	0	Difference between drawn width and actual width. DWeff=DW · SCALM
L	m	0	Default length of wire. Lscaled=L · SHRINK · SCALM
LEVEL			Model selector (not used)
RAC	ohm		Default AC resistance (RACeff default is Reff).
RES	ohm	0	Default resistance.
RSH		0	Sheet resistance/square.
SHRINK		1	Shrink factor.
TC1C	1/deg	0	First-order temperature coefficient for capacitance.

Name (Alias)	Units	Default	Description
TC2C	$1/deg^2$	0	Second-order temperature coefficient for capacitance.
TC1R	1/deg	0	First-order temperature coefficient for resistance.
TC2R	$1/deg^2$	0	Second-order temperature coefficient for resistance.
THICK	m	0	Dielectric thickness.
TREF	deg C	TNOM	Temperature reference, for model parameters.
W	m	0	Default width of wire. Wscaled=W · SHRINK · SCALM

Resistor Model Equations

Wire Resistance Calculation

You can specify the wire width and length, in both the element and model statements. The element values override the model values.

- To scale the *element* width and length, use the SCALE option and the SHRINK model parameter.
- To scale the *model* width and length, use the SCALM option and the SHRINK model parameter.

The effective width and length are calculated as follows:

$$Weff = Wscaled - 2 \cdot DWeff$$
$$Leff = Lscaled - 2 \cdot DLReff$$

If you specify element resistance:

$$Reff = \frac{R \cdot SCALE(element)}{M}$$

Otherwise, if (Weff · Leff · RSH) is greater than zero, then:

$$Reff = \frac{Leff \cdot RSH \cdot SCALE(element)}{M \cdot Weff}$$

If (Weff · Leff · RSH) is zero, then:

$$Reff = \frac{RES \cdot SCALE(element)}{M}$$

If you specify AC resistance in the element, then:

$$RACeff = \frac{AC \cdot SCALE(element)}{M}$$

Otherwise, if the model specifies RAC, RAC is used:

$$RACeff = \frac{RAC \cdot SCALE(element)}{M}$$

If neither are specified, the equation defaults to:

$$RACeff = Reff$$

If the resistance is less than the `RESMIN` option, it is reset it to the `RESMIN` value, and a warning message displays.

$$RESMIN = \frac{1}{GMAX \cdot 1000 \cdot M}$$

Wire Capacitance Calculation

The effective length is the scaled drawn length, less (2 · `DLeff`).

- Leff represents the effective length of the resistor, from physical edge to physical edge.
- DWeff is the distance from the drawn edge of the resistor, to the physical edge of the resistor.

The effective width is the same as the width used in the resistor calculation.

$$Leff = Lscaled - 2 \cdot DLeff$$
$$Weff = Wscaled - 2 \cdot DWeff$$

If you specify the element capacitance, C:

$$CAPeff = C \cdot SCALE(element) \cdot M$$

Otherwise, the capacitance is calculated from the Leff, Weff, and COX.

$$CAPeff = M \cdot SCALE(element) \cdot [Leff \cdot Weff \cdot COX + 2 \cdot (Leff + Weff) \cdot CAPSW]$$

Computing the bottom-wall capacitance, COX, is based on a hierarchy of defaults and specified values, involving:

- dielectric thickness (THICK)
- relative dielectric constant (DI)
- two absolute dielectric constants, εo and εox

as follows:

1. If you specify COX=*value*, the *value* is used.
2. If you do not specify COX, but you do specify a value other than zero for THICK (the dielectric thickness):
   a) If you specify a non-zero value for DI=*value*, then:

$$COX = \frac{DI \cdot \varepsilon o}{THICK}$$

   b) If you do not specify a DI value, or if the value is zero, then:

$$COX = \frac{\varepsilon ox}{THICK}$$

where:

$$\varepsilon o = 8.8542149e\text{-}12 \ F/meter$$

$$\varepsilon ox = 3.453148e\text{-}11 \ F/meter$$

3. If you do not specify COX, and THICK= 0, this is an error.
   - If you specify only the model capacitance (CAP), then:

$$CAPeff = CAP \cdot SCALE(element) \cdot M$$

   - If you specify the capacitance, but you do not specify the bulk node, then capacitance is not evaluated, and a warning message is issued.

Resistor Noise Equation

The following equation models the thermal noise of a resistor:

$$inr = \left(NOISE \cdot \frac{4kT}{Rval}\right)^{1/2}$$

where *NOISE* is a model parameter that defaults to 1. To eliminate the contribution of resistor noise, use the NOISE parameter. To specify the NOISE parameter, use a model for the resistor.

Noise Summary Print Out Definitions

RX	Transfer the function of thermal noise to the output. This is not noise, but is a transfer coefficient, reflecting the contribution of thermal noise to the output.
TOT, V^2/Hz	Total output noise: $'OT = RX^2 \cdot inr^2$

Resistor Temperature Equations

Temperature values can modify the resistor and capacitor values, as follows:

$$R(t) = R \cdot (1.0 + TC1 \cdot \Delta t + TC2 \cdot \Delta t^2)$$
$$RAC(t) = RAC \cdot (1.0 + TC1 \cdot \Delta t + TC2 \cdot \Delta t^2)$$
$$C(t) = C \cdot (1.0 + TC1 \cdot \Delta t + TC2 \cdot \Delta t^2)$$

Δt	t - tnom
t	Element temperature in °K: t = circuit temp + DTEMP + 273.15
tnom	Nominal temperature in °K: tnom = 273.15 + TNOM

Capacitor Device Model and Equations

Capacitance Model

Syntax

```
.MODEL mname C parameter=value
```

mname	Model name.
C	Specifies a capacitance model.
parameter	Any model parameter name.

Capacitance Parameters

Name (Alias)	Units	Default	Description
CAP	F	0	Default capacitance value.
CAPSW	F/m	0	Sidewall fringing capacitance.
COX	F/m^2	0	Bottomwall capacitance.
DEL	m	0	Difference between drawn width and actual width or length. DELeff = DEL · SCALM
DI		0	Relative dielectric constant.
L	m	0	Default length of capacitor. Lscaled = L · SHRINK · SCALM
SHRINK		1	Shrink factor.
TC1	1/deg	0	First temperature coefficient for capacitance.

Name (Alias)	Units	Default	Description
TC2	1/ deg^2	0	Second temperature coefficient for capacitance.
THICK	m	0	Insulator thickness.
TREF	deg C	TNOM	Reference temperature.
W	m	0	Default width of capacitor. Wscaled = W · SHRINK · SCALM

Parameter Limit Checking

If a capacitive element value exceeds 0.1 Farad, then the output listing file receives a warning message. This feature helps you to identify elements that are missing units or have incorrect values, particularly those in automatically-produced netlists.

Capacitor Device Equations

Effective Capacitance Calculation

You can associate a model with a capacitor. You can specify some of the parameters in both the element and the model descriptions. The element values override the model values.

- To scale the *element* width and length, use the SCALE option and the SHRINK model parameter.
- To scale the *model* width and length, use the SCALM option and the SHRINK model parameter.

The effective width and length are calculated as follows:

$$Weff = Wscaled - 2 \cdot DELeff$$

$$Leff = Lscaled - 2 \cdot DELeff$$

If you specify the element capacitance:

$$CAPeff = C \cdot SCALE(element) \cdot M$$

Otherwise, the capacitance is calculated from the `Leff`, `Weff`, and `COX`.

$$CAPeff = M \cdot SCALE(element) \cdot [Leff \cdot Weff \cdot COX + 2 \cdot (Leff + Weff) \cdot CAPSW]$$

If you do not specify `COX`, but `THICK` is not zero, then:

$$COX = \frac{DI \cdot \varepsilon o}{THICK} \quad \textit{if DI not zero}$$

or

$$COX = \frac{\varepsilon ox}{THICK} \quad \textit{if DI=0}$$

where:

$$\varepsilon o = 8.8542149e\text{-}12 \ \frac{F}{meter}$$

$$\varepsilon ox = 3.453148e\text{-}11 \ \frac{F}{meter}$$

If you specify only model capacitance (`CAP`), then:

$$CAPeff = CAP \cdot SCALE(element) \cdot M$$

Capacitance Temperature Equation

The capacitance as a function of temperature is calculated as follows:

$$C(t) = C \cdot (1.0 + TC1 \cdot \Delta t + TC2 \cdot \Delta t^2)$$

Δt	t - tnom
t	Element temperature, in degrees Kelvin.
	t=circuit temp + DTEMP + 273.15
tnom	Nominal temperature, in degrees Kelvin
	tnom+273.15 + TNOM

Inductor Device Model and Equations

You can use several elements and models to analyze:

- switching regulators,
- transformers
- mutual inductive circuits

These elements include:

- magnetic winding elements
- mutual cores
- magnetic core models

You can use the saturable core model for:

- chokes
- saturable transformers
- linear transformers

To use the model, you must:

1. Provide a mutual core statement.
2. Specify the core parameters, using a `.MODEL` statement.
3. Specify the windings around each core element, using a magnetic winding element statement.

Inductor Core Models

Magnetic Core Syntax

```
.MODEL mname L (<pname1 = val1>…)
```

Jiles-Atherton Ferromagnetic Core Syntax

```
.MODEL mname CORE (LEVEL=1 <pname1 = val1>…)
```

mname	Model name. Elements use this name to refer to the model.
L	Identifies a saturable core model.
CORE	Identifies a Jiles-Atherton Ferromagnetic Core model.
level=x	Equation selection for Jiles-Atherton model.
pname1=val1	Value of the model parameter. Each core model can include several model parameters.

Example 1

```
.MODEL CHOKE L(BS=12K BR=10K HS=1 HCR=.2 HC=.3 AC=1. LC=3.)
```

To use this example, obtain the core model parameters from the manufacturer's data. Figure 2-1 on page 2-17 illustrates the required *b-h* loop parameters for the model.

The model includes:

- core area
- length
- gap size
- core growth time constant

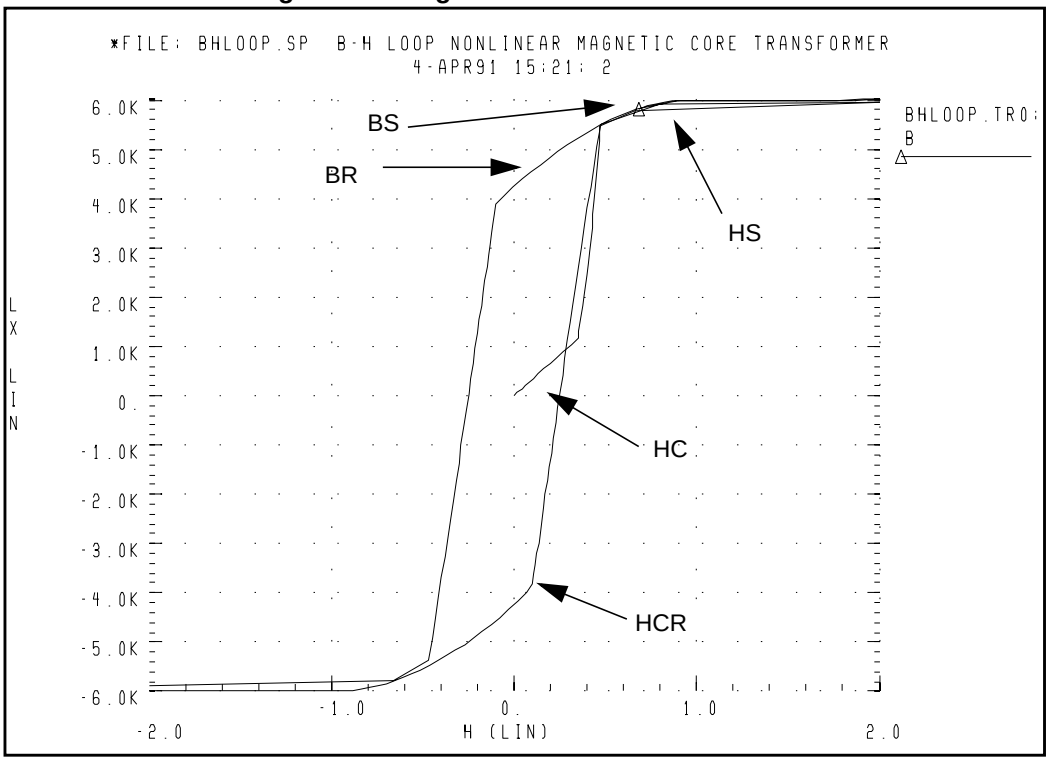
Example 2

```
*file: bhloop.sp b-h loop nonlinear magnetic core transformer
* plot in avanwaves i(l1 versus 22 to get b-h loop
.option acct method=gear post rmax=.05
.tran 1m 25m
.probe mu=lx0(k1) h=lx1(k1) b=lx2(k1) L1=lv1(l1) L2=lv1(l2)
+ i(l1)
k1 l1 l2 mag2
l1 1 0 nt=20
l2 2 0 nt=20
r11 1 11 1
v11 11 0 sin (0 5 60
r22 2 22 1
c22 22 0 1
.model mag2 l bs=6k br=3k hs=1 hcr=.1 hc=.8 ac=1 lc=16
.end
```

Magnetic Core Model Parameters

Name (Alias)	Units	Default	Description
AC	cm · 2	1.0	Core area.
BS	Gauss	13000	Magnetic flux density at saturation.
BR	Gauss	12000	Residual magnetization.
HC	Oersted	0.8	Coercive magnetizing force.
HCR	Oersted	0.6	Critical magnetizing force.
HS	Oersted	1.5	Magnetizing force at saturation.
LC	cm	3.0	Core length.
LG	cm	0.0	Gap length.
TC	s	0.0	Core growth time constant.

Figure 2-1: Magnetic Saturable Core Model



Jiles-Atherton Core Model Parameters

Name (Alias)	Units	Default	Description
LEVEL		2	Model selector. For the Jiles-Atherton model, set LEVEL=1. LEVEL=2, the default, selects the Pheno model, which is the original model.
AREA, (AC)	cm^2	1	Mean of the magnetic core cross section. AC is an alias of AREA.
PATH, (LC)	cm	3	Mean of the magnetic core path length. LC is an alias of PATH.
MS	amp/ meter	1e6	Magnetization saturation.
A	amp/ meter	1e3	Characterizes the shape of the anhysteretic magnetization.
ALPHA		1e-3	Represents the coupling between the magnetic domains.
C		0.2	Domain flexing parameter.
K	amp/ meter	500	Domain of an isotropy parameter.

Magnetic Core Element Outputs

Output Variable	Description
LX1	magnetic field, *h* (oersted)
LX2	magnetic flux density, *b* (gauss)
LX3	slope of the magnetization curve, $\frac{dm}{dh}$

Output Variable	Description
LX4	bulk magnetization, m (amp/meter)
LX5	slope of the anhysteretic magnetization curve, $\frac{dm_{an}}{dh}$
LX6	anhysteretic magnetization, m_{an} (amp/meter)
LX7	effective magnetic field, h_e (amp/meter)

Inductor Device Equations

Parameter Limit Checking

If an inductive element value exceeds 0.1 Henry, then the output listing file receives a warning message. This feature helps you to identify elements that are missing units or have incorrect values, particularly those in automatically-produced netlists.

Inductor Temperature Equation

The following equation provides the effective inductance, as a function of temperature:

$$L(t) = L \cdot (1.0 + TC1 \cdot \Delta t + TC2 \cdot \Delta t^2)$$

Δt	*t - tnom*
t	Element temperature, in degrees Kelvin.
	t=circuit temp + DTEMP + 273.15
tnom	Nominal temperature, in degrees Kelvin.
	tnom=273.15 + TNOM

1. To create coupling between inductors, use a separate coupling element.
2. To specify mutual inductance between two inductors, use the coefficient of coupling, *kvalue*. The following equation defines *kvalue*:

$$K = \frac{M}{(L_1 \cdot L_2)^{1/2}}$$

`L1, L2`	Inductances of the two coupled inductors.
`M`	Mutual inductance between the inductors.

The linear branch relation for transient analysis is:

$$v_1 = L_1 \cdot \frac{di_1}{dt} + M \cdot \frac{di_2}{dt}$$

$$v_2 = M \cdot \frac{di_1}{dt} + L_2 \cdot \frac{di_2}{dt}$$

The linear branch relation for AC analysis is:

$$V_1 = (j \cdot \omega \cdot L_1) \cdot I_1 + (j \cdot \omega \cdot M) \cdot I_2$$

$$V_2 = (j \cdot \omega \cdot M) \cdot I_1 + (j \cdot \omega \cdot L_2) \cdot I_2$$

Note: You must define an inductor reference, using a mutual inductor statement; otherwise an error message displays, and simulation terminates.

Jiles-Atherton Ferromagnetic Core Model

The Jiles-Atherton ferromagnetic core model is based on domain wall motion, including both bending and translation. A modified Langevin expression describes the hysteresis-free (anhysteretic) magnetization curve. This leads to:

$$m_{an} = MS \cdot \left(\coth\left(\frac{h_e}{A}\right) - \frac{A}{h_e} \right)$$

$$h_e = h + ALPHA \cdot m_{an}$$

where	is
m_{an}	Magnetization level, if the domain walls could move freely.
h_e	Effective magnetic field.
h	Magnetic field.
MS	Model parameter that represents the saturation magnetization.
A	Model parameter that characterizes the shape of the anhysteretic magnetization.
ALPHA	Model parameter that represents the coupling between the magnetic domains.

The above equation generates anhysteretic curves, when the model parameter ALPHA has a small value. Otherwise, it generates some elementary forms of hysteresis loops, which is not a desirable result. The following equation calculates the slope of the curve at zero (0):

$$\frac{dm_{an}}{dh} = \frac{1}{3 \cdot \frac{A}{MS} - ALPHA}$$

The slope must be positive; therefore, the denominator of the above equation must be positive. If the slope becomes negative, an error message displays.

The anhysteretic magnetization represents the global energy state of the material, if the domain walls could move freely. But the walls are displaced and bent, in the material. If you express the bulk magnetization *m* as the sum of an irreversible component (due to wall displacement), and a reversible component (due to domain wall bending), then:

$$\frac{dm}{dh} = \frac{(m_{an} - m)}{K} + C \cdot \left(\frac{dm_{an}}{dh} - \frac{dm}{dh}\right)$$

or

$$\frac{dm}{dh} = \frac{(m_{an} - m)}{(1 + C) \cdot K} + \frac{C}{1 + C} \cdot \frac{dm_{an}}{dh}$$

Solving the above differential equation obtains the bulk magnetization *m*. The flux density b is computed from *m:*

$$b = \mu_0 \cdot (h + m)$$

where μ_0, the permeability of free space, is $4\pi \cdot 10^{-7}$, and the units of *h* and *m* are in amp/meter. Then the units of *b* are in Tesla (Wb/meter^2).

Jiles-Atherton Model Examples

Effects of Varying the ALPHA, A, and K Parameters

This example demonstrates the effects of the ALPHA, A, and K model parameters on the *b*-*h* curve.

Figure 2-2 on page 2-24 shows the *b*-*h* curves for three values of ALPHA.

Figure 2-3 on page 2-24 shows the *b*-*h* curves for three values of A.

Figure 2-4 on page 2-25 shows the *b*-*h* curves for three values of K.

Input File

```
* Test the Jiles-Atherton model
.options post
* the following analysis studies the effect of parameter
   ALPHA.
*.param palpha=0.0 pk=0.0 pc=0.0 pa=26
*.tran 0.01 1 sweep palpha poi 3 0.0 5.0e-5 1.0e-4
* the following analysis studies the effects of parameter A.
*.param palpha=0.0 pk=0.0 pc=0.0 pa=26
*.tran 0.01 1 sweep pa poi 3 10 26 50
* the following analysis studies the effects of parameter K.
.param palpha=0.0 pk=5 pc=1.05 pa=26
.tran 0.01 1.25 $ sweep pk poi 2 5 50
rl 1 2 1
l1 2 0 nt=50
k1 l1 ct
igen 0 1 sin(0 0.1a 1hz 0 )
.model ct core LEVEL=1 ms=420k k=pk c=pc a=pa
+ alpha=palpha area=1.17 path=8.49
.probe b=lx2(k1) h=lx1(k1) i(rl) v(1)
.probe dmdh=lx3(k1) m=lx4(k1) man=lx6(k1)
.probe l=lv1(l1)
.alter
.param pk=50
.end
```

Plots of the b-h Curve

Figure 2-2: Variation of Anhysteretic b-h Curve: the Slope Increases as ALPHA Increases

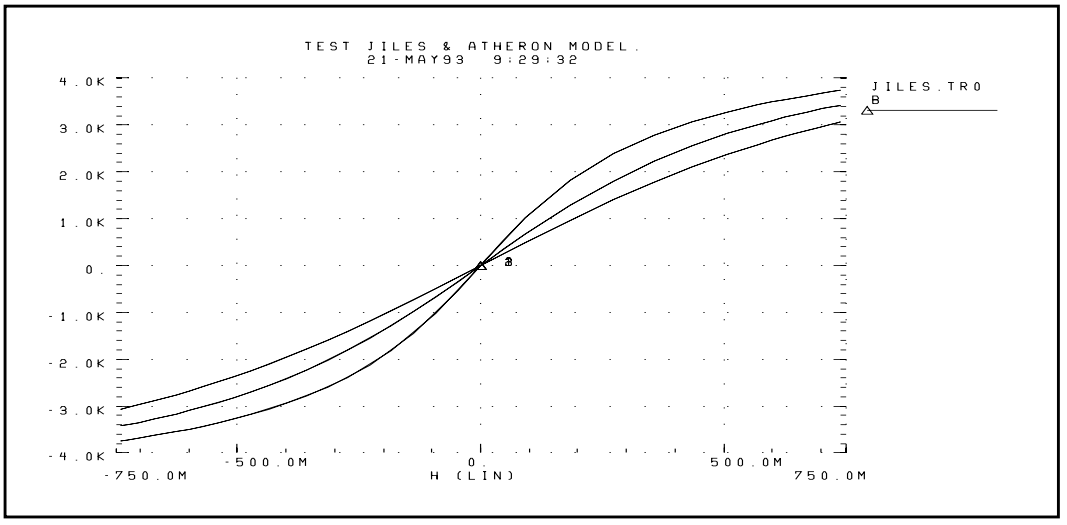


Figure 2-3: Variation of Anhysteretic b-h Curve: the Slope Decreases as A Increases

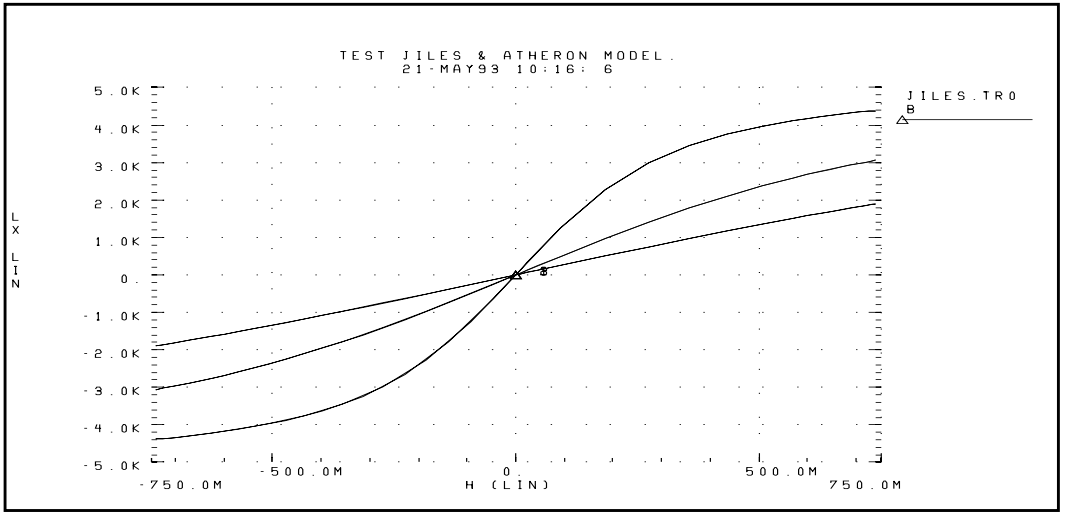
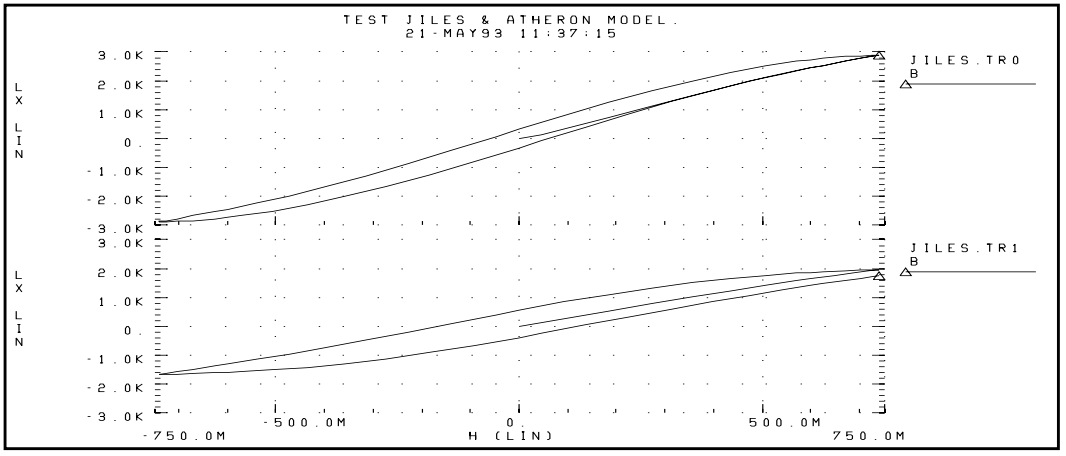


Figure 2-4: Variation of Hysteretic b-h Curve: as K Increases, the Loop Widens and Rotates Clockwise



Discontinuities in Inductance Due to Hysteresis

This example creates multi-loop hysteresis *b-h* curves for a magnetic core. Discontinuities in the inductance, which are proportional to the slope of the *b-h* curve, can cause convergence problems. Figure 2-5 demonstrates the effects of hysteresis on the inductance of the core.

Input File

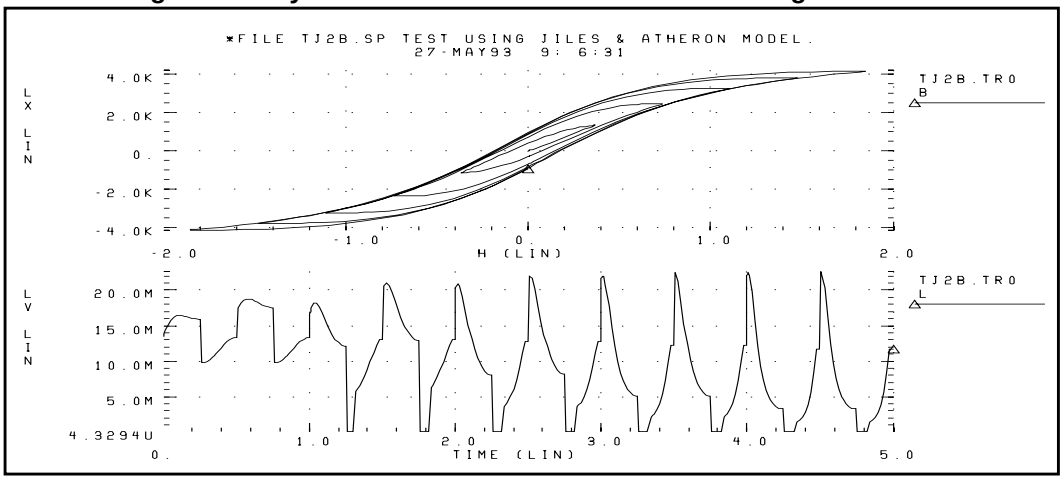
```
*file tj2b.sp Multiloop hysteresis test using Jiles-Atherton
   model.
.options post
.tran 0.01 5
rl 1 2 1
l1 2 0 nt=50
k1 l1 ct
igen 0 10 sin(0 0.1a 1hz 0 )
ipls 0 20 pwl(0,0 1m,0.5 1s,0.5
+ 1.001,1.0 2.000,1.0
+ 2.001,1.5 3.000,1.5
+ 3.001,2.0 4.000,2.0
+ 4.001,2.5 5.000,2.5)
gigen 0 1 cur='v(10)*v(20)'
rpls 0 20 1
rsin 0 10 1
```

```
.model ct core LEVEL=1 ms=420k k=18 c=1.05 a=26
+ alpha=2e-5 area=1.17 path=8.49

.probe b=lx2(k1) h=lx1(k1) i(rl) v(1)
.probe dmdh=lx3(k1) m=lx4(k1) dmandh=lx5(k1)
+ man=lx6(k1)
.probe l=lv1(l1) heff=lx7(k1)
.end
```

Plots of the Hysteresis Curve and Inductance

Figure 2-5: Hysteresis Curve and Inductance of a Magnetic Core



Optimizing the Extraction of Parameters

This example demonstrates how to optimize the process of extracting parameters from the Jiles-Atherton model. Figure 2-6 on page 2-29 shows the plots of the core output, both before and after optimization.

Input File

```
*file tj_opt.sp for Jiles-Atherton model parameter
   optimization.
.options post
+ delmax=5m
.param palpha=0.0
.param pms= opt1(150k,100k,500k)
+ pa =opt1(10,5,50)
+ pk=opt1(5,1,50)
+ pc= opt1(1,0,3)
.tran 0.01 1.0
.tran 0.01 1.0 sweep
+ optimize=opt1 results=bsat,br,hc model=optmod
.model optmod opt itropt=40
+ relin=1e-4 relout=1e-6
.meas bsat find par('abs(lx2(k1))') when lx1(k1)=5.0
   goal=3.1k
.meas br find par('abs(lx2(k1))') when lx1(k1)=0 td=.25
   goal=1k
.meas hc find par('abs(lx1(k1))') when lx2(k1)=0 td=.25
   goal=.4
rl 1 2 0.01
l1 2 0 nt=20
k1 l1 ct
igen 0 1 sin(0 2a 1hz 0 )
.model ct core LEVEL=1 ms=pms k=pk c=pc a=pa
+ alpha=palpha area=1.17 path=8.49
.probe b=lx2(k1) h=lx1(k1) i(rl) v(1)
.probe dmdh=lx3(k1) m=lx4(k1) dmandh=lx5(k1)
+ man=lx6(k1)
.probe l=lv1(l1) heff=lx7(k1)
.end
```

Analysis Results Listing

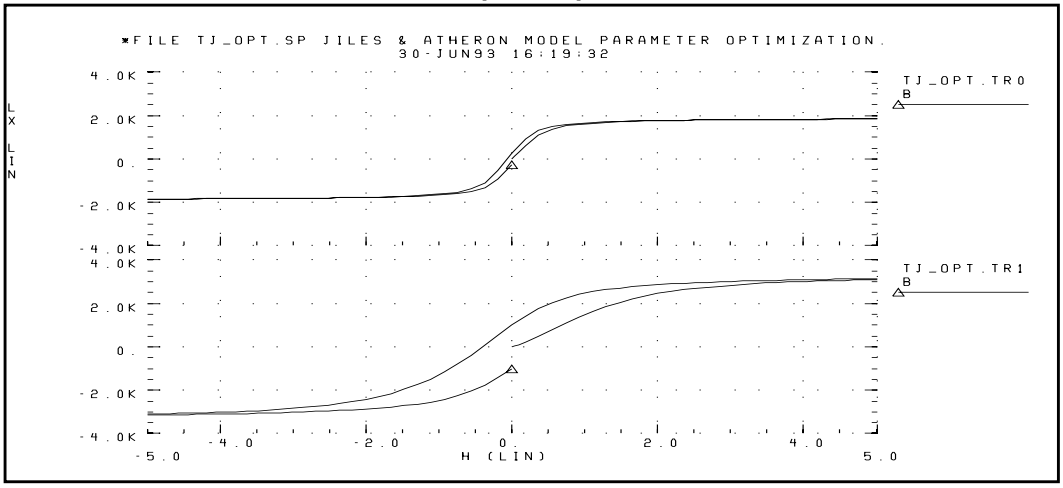
```
****** transient analysis tnom= 25.000 temp= 25.000
optimization results
 residual sum of squares = 1.043893E-12
 norm of the gradient = 1.411088E-06
 marquardt scaling parameter = 1.267004E-04
 no. of function evaluations = 30
 no. of iterations = 11
 optimization completed

 norm of gradient < grad= 1.0000E-06 on last iterations
**** optimized parameters opt1

.param pms = 267.5975k
.param pa = 27.8196
.param pk = 37.2947
.param pc = 316.4197m

*** Measure results
bsat = 3.1000E+03
 br = 9.9999E+02
 hc = 3.9880E-01
```

Figure 2-6: Output Curves Before Optimization (top), and After Optimization (bottom)



Avant!

Chapter 3
Using Diodes

Use diode models to describe pn junction diodes within MOS and bipolar integrated circuit environments and discrete devices. You can use four types of models and a wide range of parameters to model standard junction diodes:

- Zener diodes
- Silicon diffused junction diodes
- Schottky barrier diodes
- Nonvolatile memory diodes (tunneling current)

Note: See Chapter 8, "Introducing MOSFETs"; Chapter 9, "Selecting MOSFET Models: Level 1-40"; and Chapter 10, "Selecting MOSFET Models: Level 47-63" for other MOSFET and standard discrete diodes.

Diode model types include the junction diode model and the Fowler-Nordheim model. The junction diode model has two variations: geometric and nongeometric.

This chapter provides an overview of model parameters and scaling effects for the geometric and nongeometric junction diodes. It describes:

- Understanding the Diode Types
- Using Diode Model Statements
- Specifying Junction Diode Models
- Determining Temperature Effects on Junction Diodes
- Using Junction Diode Equations
- "Using the Junction Cap Model"
- Using the Fowler-Nordheim Diode
- Converting National Semiconductor Models

Understanding the Diode Types

Use the geometric junction diode to model IC-based standard silicon diffused diodes, Schottky barrier diodes, and Zener diodes. The geometric parameter lets you specify pn junction poly and metal capacitance dimensions for a particular IC process technology.

Use the nongeometric junction diode to model discrete diode devices such as standard and Zener diodes. The nongeometric model lets you scale currents, resistances, and capacitances using dimensionless area parameters.

The Fowler-Nordheim diode defines tunneling current flow through insulators. Use it to model diode effects in nonvolatile EEPROM memory.

Using Diode Model Statements

Use model and element statements to select the diode models. The model statement's LEVEL parameter selects the type of diode model used:

- LEVEL=1 selects the nongeometric junction diode model
- LEVEL=2 selects the Fowler-Nordheim diode model
- LEVEL=3 selects the geometric junction diode model

You can design Zener, Schottky barrier, and silicon diffused diodes by altering model parameters for both LEVEL 1 and LEVEL 3. LEVEL 2 does not permit modeling of these effects. For Zener diodes, the BV parameter is set for an appropriate Zener breakdown voltage.

If you do not specify the LEVEL parameter in the .MODEL statement, the model defaults to the nongeometric junction diode model, LEVEL 1.

Use control options with the diode model to scale model units, select diffusion capacitance equations, and change model parameters.

Setting Control Options

Control options related to the analysis of diode circuits, as well as other models, include DCAP, DCCAP, GMIN, GMINDC, SCALE, and SCALM. Specify these models using the .OPTIONS statement.

Setting Scaling Options

Use the scale element option, SCALE, to scale LEVELs 2 and 3 diode element parameters. Use the scale model option, SCALM, to scale LEVELs 2 and 3 diode model parameters. LEVEL 1 does not use SCALE or SCALM.

Include SCALM=<val> in the .MODEL statement to override global scaling that uses the .OPTION SCALM=<val> statement in a diode model.

Using the Capacitor Equation Selector Option — DCAP

The DCAP option selects the equations used in calculating the depletion capacitance (LEVEL 1 and LEVEL 3). The option DCCAP invokes calculation of capacitances in DC analysis.

Include the DCAP=<val> in the diode's .MODEL statement to override the global depletion capacitance equation selection with the .OPTIONS DCAP=<val> statement.

Using Control Options for Convergence

Diode convergence problems often occur at the breakdown voltage region when the diode is overdriven or in the OFF condition. To achieve convergence in such cases, include a nonzero value in the model for the series resistor parameter RS, or increase GMIN (the parallel conductance Star-Hspice automatically places in the circuit). You can specify GMIN and GMINDC in the .OPTIONS statement.

The diode control options follow:

Table 3-1: Diode Control Options

Function	Control Options
Capacitance	DCAP, DCCAP
Conductance	GMIN, GMINDC
Geometry	SCALM, SCALE

Specifying Junction Diode Models

Use the diode element statement to specify the two types of junction diodes, geometric and nongeometric. Use a different element type format for the Fowler-Nordheim model.

The diode element statement parameter fields define the connecting nodes, initialization, temperature, geometric junction, and capacitance parameters of the diode model selected in the diode .MODEL statement. Both LEVEL 1 and LEVEL 3 junction diode models share the same element parameter set. Poly and metal capacitor parameters of LM, LP, WM and WP do not share the same element parameter.

Element parameters take precedence over model parameters, if repeated in the .MODEL statement as model parameters.

Parameters common to both element and model statements are:

`AREA, PJ, M, LM, LP, WM, WP, W, and L.`

Table 3-2: Junction Diode Element Parameters

Function	Parameters
Netlist	Dxxx, n+, n-, mname
Initialization	IC, OFF
Temperature	DTEMP
Geometric junction	AREA, L, M, PJ, W
Geometric capacitance (LEVEL=3 only)	LM, LP, WM, WP

Using the Junction Model Statement

This section describes how to use the junction model statement.

Syntax

The syntax of the junction model statement is:

```
.MODEL mnameD <LEVEL = val> <keyword = val> ...
```

mname	Model name. The diode element refers to the model by this name.
D	Symbol that identifies a diode model
LEVEL	Symbol that identifies a diode model LEVEL=1 =junction diode LEVEL=2 =Fowler-Nordheim LEVEL=3 =geometric processing for junction diode
keyword	Model parameter keyword such as CJO or IS

Example

```
.MODEL D D (CO=2PF, RS=1, IS=1P)
.MODEL DFOWLER D (LEVEL=2, TOX=100, JF=1E-10, EF=1E8)
.MODEL DGEO D (LEVEL=3, JS=1E-4, JSW=1E-8)
.MODEL d1n750a D
+ LEVEL=1              XP  =0.0          EG  =1.1
+ XOI  =0.0            XOM =0.0          XM  =0.0
+ WP   =0.0            WM  =0.0          LP  =0.0
+ LM   =0.0            AF  =1.0          JSW =0.0
+ PB   =0.65           PHP =0.8          M   =0.2994
+ FC   =0.95           FCS =0.4          MJSW=0.5
+ TT   =2.446e-9       BV  =4.65         RS  =19
+ IS   =1.485e-11      CJO =1.09e-9      CJP =0.0
+ PJ   =0.0            N   =1.615        IK  =0.0
+ IKR  =1.100e-2       IBV =2.00e-2
```

Using Junction Model Parameters

The .MODEL statement is referenced by the diode element statement. The .MODEL statement contains parameters that specify the type of diode model used (LEVEL 1, 2, or 3), as well as DC, capacitance, temperature, resistance, geometric, and noise parameters.

Table 3-3: Junction Diode Model Parameters (LEVEL 1 and LEVEL 3)

Function	Parameters
model type	LEVEL
DC parameters	IBV, IK, IKR, IS, ISW, N, RS, VB, RS
geometric junction	AREA, M, PJ
geometric capacitance (LEVEL=3 only)	L, LM, LP, SHRINK, W, WM, WP, XM, XOJ, XOM, XP, XW
capacitance	CJ, CJP, FC, FCS, M, MJSW, PB, PHP, TT
noise	AK, KF

Setting Junction DC Parameters in LEVEL 1 and 3

Table 3-4: Junction DC Parameters

Name (Alias)	Units	Default	Description
AREA		1.0	Junction area For LEVEL=1 AREAeff = AREA · M, unitless For LEVEL=3 AREAeff=AREA · SCALM^2 · SHRINK^2 · M unit = meter^2 If you specify W and L: AREAeff = Weff · Leff · M unit = meter^2
EXPLI	amp/ AREAeff	1e15	Current explosion model parameter. The PN junction characteristics above the explosion current are linear, with the slope at the explosion point, which increases simulation speed and improves convergence. EXPLIeff = EXPLI · AREAeff
IB	amp/ AREAeff	1.0e-3	Current at breakdown voltage For LEVEL=3 IBVeff = IBV · AREAeff / SCALM^2
IBV	amp/ AREAeff	1.0e-3	Current at breakdown voltage For LEVEL=3 IBVeff = IBV · AREAeff / SCALM^2
IK (IKF, JBF)	amp/ AREAeff	0.0	Forward knee current (intersection of the high- and low-current asymptotes) IKeff = IK · AREAeff

Table 3-4: Junction DC Parameters *(Continued)*

Name (Alias)	Units	Default	Description
IKR (JBR)	amp/ AREAeff	0.0	Reverse knee current (intersection of the high- and low-current asymptotes) IKReff = IKR · AREAeff
IS (JS)	amp/ AREAeff	LEVEL 1= 1.0e-14 LEVEL 3= 0.0	If you use an IS value less than EPSMIN, the program resets the value of IS to EPSMIN, and displays a warning message. EPSMIN default=1.0e-28 If the value of IS is too large, the program displays a warning. For LEVEL=1 ISeff = AREAeff · IS For LEVEL=3 ISeff = AREAeff · IS/SCALM^2
JSW (ISP)	amp/ PJeff	0.0	Sidewall saturation current per unit junction periphery For LEVEL=1 JSWeff = PJeff · JSW For LEVEL=3 JSWeff = PJeff · JSW/SCALM
L			Default length of diode Leff = L · SHRINK · SCALM+ XWeff
LEVEL		1	Diode model selector LEVEL=1 or LEVEL=3 selects junction diode model LEVEL=2 selects Fowler-Nordheim model
N		1.0	Emission coefficient

Table 3-4: Junction DC Parameters *(Continued)*

Name (Alias)	Units	Default	Description
PJ		0.0	Junction periphery For LEVEL=1 PJeff = PJ · M, unitless For LEVEL=3 PJeff = PJ · SCALM · M · SHRINK, meter If *W* and *L* are specified PJeff = (2 · Weff + 2 · Leff) · M, meter
RS	ohms or ohms/m^2 (see note below)	0.0	Ohmic series resistance For LEVEL=1 RSeff = RS/AREAeff For LEVEL=3 RSeff= RS SCALM2/AREAeff
SHRINK		1.0	Shrink factor
VB (BV, VAR, VRB)	V	0.0	Reverse breakdown voltage. 0.0 indicates an infinite breakdown voltage
XW			Accounts for masking and etching effects XWeff = XW · SCALM

Note: If you use a diode model for which the AREA is not specified, AREA defaults to 1; then RS has units of ohms. If AREA is specified in the netlist in m^2, then the units of RS are ohms/m^2.

Setting Junction Capacitance Parameters

Table 3-5: Junction Capacitance Parameters

Name (Alias)	Units	Default	Description
CJ (CJA, CJO)	F/ AREAeff	0.0	Zero-bias junction capacitance per unit junction bottomwall area For LEVEL=1 $CJOeff = CJO \cdot AREAeff$ For LEVEL=3 $CJeff = CJ \cdot AREAeff/SCALM^2$
CJP (CJSW)	F/PJeff	0.0	Zero-bias junction capacitance per unit junction periphery (PJ) For LEVEL=1 $CJPeff = CJP \cdot PJeff$ For LEVEL=3 $CJPeff = CJP \cdot PJeff/SCALM$
FC		0.5	Coefficient for forward-bias depletion area capacitance formula
FCS		0.5	Coefficient for the forward-bias depletion periphery capacitance formula
M (EXA, MJ)		0.5	Area junction grading coefficient
MJSW (EXP)		0.33	Periphery junction grading coefficient
PB (PHI, VJ, PHA)	V	0.8	Area junction contact potential
PHP	V	PB	Periphery junction contact potential
TT	s	0.0	Transit time

Setting Metal and Poly Capacitor Parameters for LEVEL=3

Table 3-6: Metal and Poly Capacitor Parameters

Name (Alias)	Units	Default	Description
LM	m	0.0	Use this parameter when LM is not specified in the element statement. LMeff = LM · SCALM · SHRINK
LP	m	0.0	Use this parameter if LP is not specified in the element statement. LPeff = LP · SCALM · SHRINK
WM	m	0.0	Use this parameter if WM is not specified in the element statement. WMeff = WM · SCALM · SHRINK
WP	m	0.0	Use this parameter if WP is not specified in the element statement. WPeff = WP · SCALM · SHRINK
XM	m	0.0	XM accounts for masking and etching effects: XMeff = XM · SCALM
XOI		10k	Thickness of the poly to bulk oxide
XOM	Å	10k	Thickness of the metal to bulk oxide
XP	m	0.0	Accounts for masking and etching effects XPeff = XP · SCALM

Setting Noise Parameters for LEVEL=1 and 3

Table 3-7: Noise Parameters

Name (Alias)	Units	Default	Description
AF		1.0	Flicker noise exponent
KF		0.0	Flicker noise coefficient

Geometric Scaling for Diode Models

LEVEL=1 Scaling

Scaling for LEVEL 1 involves the use of the AREA and M Element parameters. The element and model parameters scaled with AREA and M include:

```
IK, IKR, JS, CJO, and RS. For AREA and M, default=1
```

This element is not a geometric model because both the area (AREA) and periphery (PJ) are measured in dimensionless values. These parameters are not affected by the SCALE and SCALM options.

The periphery junction parameter is multiplied by M, the multiplier parameter, to scale the dimensionless periphery junction.

$$PJeff = PJ \cdot M$$

PJeff is then used to scale CJP, the zero-bias junction capacitance, and the sidewall saturation current, JSW.

$$CJPeff = PJeff \cdot CJP$$

$$JSWeff = PJeff \cdot JSW$$

AREA and M are used to obtain AREAeff.

$$AREAeff = AREA \cdot M$$

CJO, IK, IKR, IBV, and IS are multiplied by AREAeff to obtain their effective scaled values. RS, however, is divided by AREAeff.

$$IKeff = AREAeff \cdot IK$$

$$IKReff = AREAeff \cdot IKR$$

$$IBVeff = AREAeff \cdot IBV$$

$$ISeff = AREAeff \cdot IS$$

$$RSeff = RS/AREAeff$$

$$CJOeff = CJO \cdot AREAeff$$

LEVEL=3 Scaling

LEVEL 3 scaling is affected by SCALM, SCALE, SHRINK, and M.

The LEVEL 3 element parameters affected by SCALE include:

```
AREA, LM, LP, PJ, WM, WP, W, L
```

The model parameters affected by SCALM include:

```
AREA, IBV, IK, IKR, IS, PJ, JSW, RS, CJO, CJP, LM, LP, WP,
XM, XP, W, L, XW
```

If you include the AREA as either an element parameter or a model parameter, the program uses SCALE or SCALM. The following equations use the AREA *element* parameter, instead of the AREA *model* parameter.

If the AREA and PJ model parameters are specified and the element is not, use SCALM as the scaling factor instead of SCALE. The scaled effective area and periphery junction element parameters are determined by:

$$\mathrm{AREAeff} = \mathrm{AREA} \cdot \mathrm{M} \cdot \mathrm{SCALE}^2 \cdot \mathrm{SHRINK}^2$$
$$\mathrm{PJeff} = \mathrm{PJ} \cdot \mathrm{SCALE} \cdot \mathrm{M} \cdot \mathrm{SHRINK}$$

or, if W and L are specified:

$$\mathrm{AREAeff} = \mathrm{Weff} \cdot \mathrm{Leff} \cdot \mathrm{M}$$
$$\mathrm{PJeff} = (2 \cdot \mathrm{Weff} + 2 \cdot \mathrm{Leff}) \cdot \mathrm{M}$$

where

$$\mathrm{Weff} = \mathrm{W} \cdot \mathrm{SCALE} \cdot \mathrm{SHRINK} + \mathrm{XWeff}$$
$$\mathrm{Leff} = \mathrm{L} \cdot \mathrm{SCALE} \cdot \mathrm{SHRINK} + \mathrm{XWeff}$$

To find the value of JSWeff and CJPeff use the formula:

$$\mathrm{JSWeff} = \mathrm{PJeff} \cdot (\mathrm{JSW}/\mathrm{SCALM})$$
$$\mathrm{CJPeff} = \mathrm{PJeff} \cdot (\mathrm{CJP}/\mathrm{SCALM})$$

To determine the polysilicon and metal capacitor dimensions, multiply each by SCALE or by SCALM if specified as model parameters.

$$\mathrm{LMeff} = \mathrm{LM} \cdot \mathrm{SCALE} \cdot \mathrm{SHRINK}$$
$$\mathrm{WMeff} = \mathrm{WM} \cdot \mathrm{SCALE} \cdot \mathrm{SHRINK}$$
$$\mathrm{LPeff} = \mathrm{LP} \cdot \mathrm{SCALE} \cdot \mathrm{SHRINK}$$
$$\mathrm{WPeff} = \mathrm{WP} \cdot \mathrm{SCALE} \cdot \mathrm{SHRINK}$$
$$\mathrm{XPeff} = \mathrm{XP} \cdot \mathrm{SCALM}$$
$$\mathrm{XMeff} = \mathrm{XM} \cdot \mathrm{SCALM}$$

You can determine the effective scaled model parameters, IBeff, IKeff, IKReff, IBVeff, RSeff, and CJO as follows:

$$
\begin{aligned}
\mathrm{IKeff} &= \mathrm{AREAeff} \cdot \mathrm{IK} \\
\mathrm{IKReff} &= \mathrm{AREAeff} \cdot \mathrm{IKR} \\
\mathrm{IBVeff} &= (\mathrm{AREAeff} \cdot \mathrm{IBV})/\mathrm{SCALM}^2 \\
\mathrm{ISeff} &= \mathrm{IS} \cdot (\mathrm{AREAeff}/\mathrm{SCALM}^2) \\
\mathrm{RSeff} &= \mathrm{RS}/(\mathrm{AREAeff} \cdot \mathrm{SCALM}^2) \\
\mathrm{CJOeff} &= \mathrm{AREAeff} \cdot (\mathrm{CJO}/\mathrm{SCALM}^2)
\end{aligned}
$$

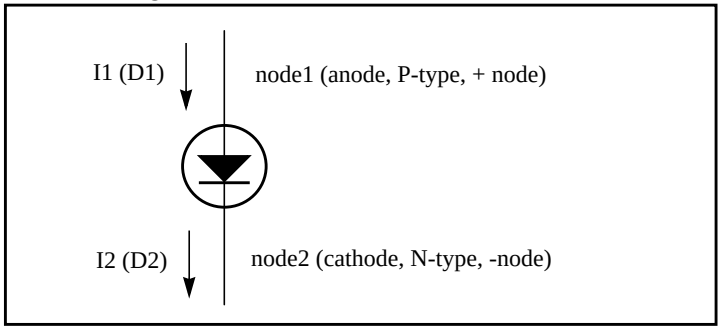
Defining Diode Models

Diode Current

Figure 3-1 shows the direction of current flow through the diode. Use either I(D1) or I1(D1) syntax to print the diode current.

If the voltage on node1 is 0.6V greater than the voltage on node2, the diode is *forward biased* or turned on. The anode is the p-doped side of a diode, and the cathode is the n-doped side.

Figure 3-1: Diode Current Convention



Using Diode Equivalent Circuits

Star-Hspice uses three equivalent circuits in diode analysis: transient, AC, and noise circuits. Components of these circuits form the basis for all element and model equations.

The fundamental component in the DC equivalent circuit is the DC diode current *(id)*. For noise and AC analyses, the actual *id* current is not used. The partial derivative of *id* with respect to the terminal voltage *vd* is used instead. The name for this partial derivative is:

Conductance

$$gd = \frac{\partial id}{\partial vd}$$

The drain current (id) equation accounts for all basic DC effects of the diodes. Star-Hspice assumes capacitance effects to be separate from the id equations.

Figure 3-2: Equivalent Circuit, Diode Transient Analysis

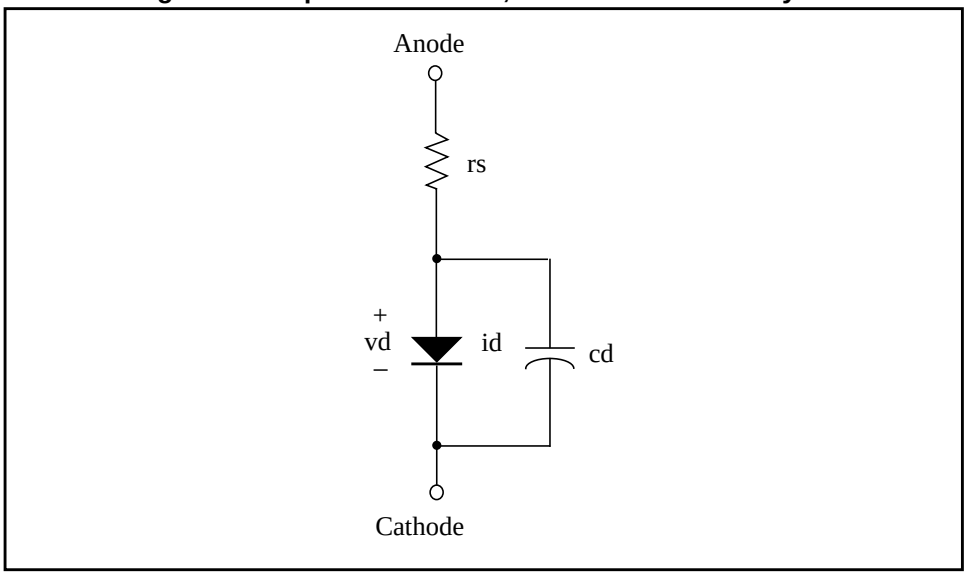


Figure 3-3: Equivalent Circuit, Diode AC Analysis

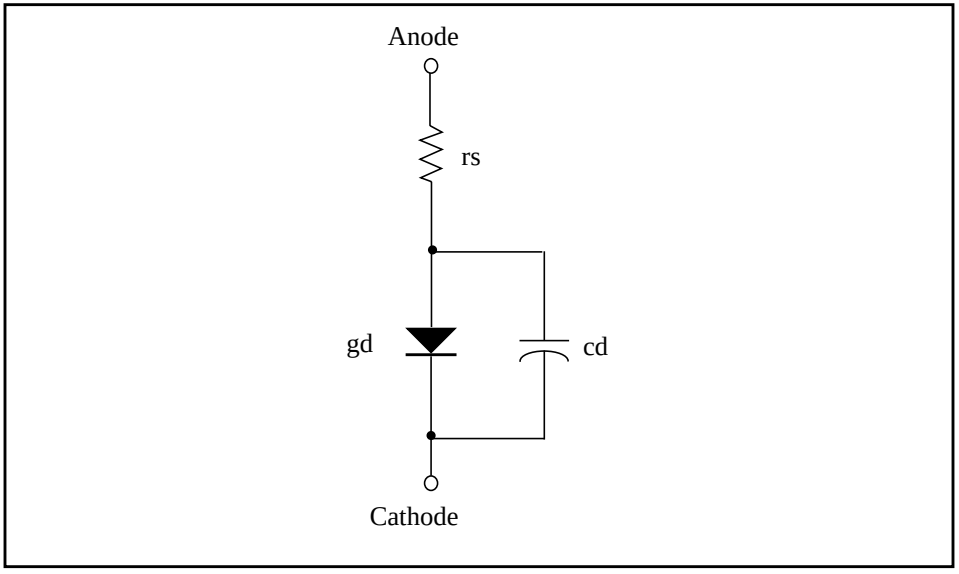
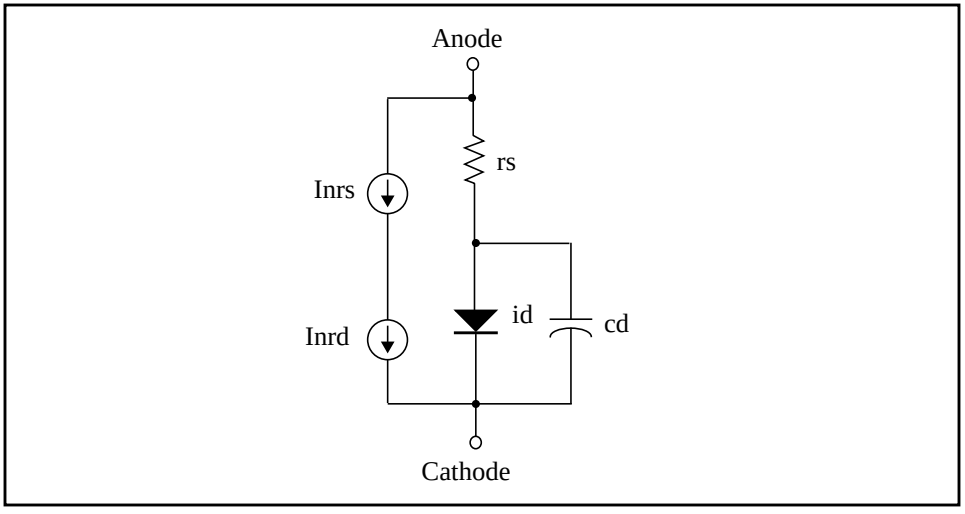


Figure 3-4: Equivalent Circuit, Diode AC Noise Analysis



Determining Temperature Effects on Junction Diodes

LEVEL 1 and LEVEL 3 model statements contain parameters for the calculation of temperature effects. TLEV and TLEVC select different temperature equations for the calculation of temperature effects on energy gap, leakage current, breakdown voltage, contact potential, junction capacitance, and grading.

Table 3-8: Junction Diode Temperature Parameters (LEVEL 1 and 3)

Variable	Parameter
Resistance coefficient	TRS
Capacitance coefficient	CTA, CTP
Energy gap	EG, GAP1, GAP2
Transit time coefficient	TTT1, TTT2
Reference temperature	TREF
Temperature selectors	TLEV, TLEVC
Miscellaneous	TM1, TM2, TPB, TPHP
Saturation current	XT1

Setting Temperature Effect Parameters LEVEL=1 and 3

Table 3-9: Junction Diode Temperature Effect Parameters

Name (Alias)	Units	Default	Description
CTA (CTC)	1/°	0.0	Temperature coefficient for area junction capacitance (CJ). Set the TLEVC parameter to 1 to let CTAl override the default temperature coefficient.

Table 3-9: Junction Diode Temperature Effect Parameters *(Continued)*

Name (Alias)	Units	Default	Description
CTP	1/°	0.0	Temperature coefficient for periphery junction capacitance (CJP). Set TLEVC to 1 to let CTP override the default temperature coefficient.
EG	eV		Energy gap for pn junction diode For TLEV=0, 1, default=1.11, for TLEV=2, default=1.16 1.17 - silicon 0.69 - Schottky barrier diode 0.67 - germanium 1.52 - gallium arsenide
GAP1	eV/°	7.02e-4	7.02e-4 - silicon (old value) 4.73e-4 - silicon 4.56e-4 - germanium 5.41e-4 - gallium arsenide
GAP2	°	1108	1108 - silicon (old value) 636 - silicon 210 - germanium 204 - gallium arsenide
TCV	1/°	0.0	Breakdown voltage temperature coefficient
TLEV		0.0	Temperature equation selector for diode; interacts with TLEVC.
TLEVC		0.0	Level selector for diode temperature, junction capacitances and contact potentials; interacts with TLEV.
TM1	1/°	0.0	First-order temperature coefficient for MJ.

Table 3-9: Junction Diode Temperature Effect Parameters *(Continued)*

Name (Alias)	Units	Default	Description
TM2	$1/°^2$	0.0	Second-order temperature coefficient for MJ.
TPB (TVJ)	V/°	0.0	Temperature coefficient for PB. Set the TLEVC parameter to 1 or 2 to enable TPB to override the default temperature compensation.
TPHP	V/°	0.0	Temperature coefficient for PHP. Set the TLEVC parameter to 1 or 2 to enable TPHP to override the default temperature compensation.
TREF		25.0	Model reference temperature (LEVEL 1 or 3 only)
TRS	1/°	0.0	Resistance temperature coefficient.
TTT1	1/°	0.0	First order temperature coefficient for TT.
TTT2	$1/°^2$	0.0	Second order temperature coefficient for TT.
XTI		3.0	Saturation current temperature exponent. ■ Set XTI=3.0 for silicon-diffused junction. ■ Set XTI=2.0 for Schottky barrier diode.

Using Junction Diode Equations

Table 3-10 shows the diode equation variable definition.

Table 3-10: Equation Variable Definitions

Variable	Definition
cd	total diode capacitance
f	frequency
gd	diode conductance
id	diode DC current
id1	current without high level injection
ind	diode equivalent noise current
inrs	series resistor equivalent noise current
vd	voltage across the diode

Table 3-11 shows the equation quantity definition.

Table 3-11: Equation Quantity Definition

Quantity	Definition
tox	3.453143e-11 F/m
k	1.38062e-23 (Boltzmann’s constant)
q	1.60212e-19 (electron charge)
t	temperature in °Kelvin
Δt	t - tnom
tnom	nominal temperature of parameter measurements in °Kelvin

Table 3-11: Equation Quantity Definition *(Continued)*

Quantity	Definition
vt(t)	$k \cdot$ t/q: thermal voltage
vt(tnom)	$k \cdot$ tnom/q: thermal voltage

Using Junction DC Equations

The basic diode is modeled in three regions:

- Forward bias
- Reverse bias
- Breakdown regions

For a forward bias diode, the anode is more positive than the cathode. The diode is turned on and conducts above 0.6 volts. Set the model parameter RS to limit conduction current. As the forward bias voltage increases past 0.6 volts, the limiting resistor prevents the value of the diode current from becoming too high and the solution from converging.

Forward Bias: vd > -10 · vt

$$id = ISeff \cdot \left(e^{\frac{vd}{N \cdot vt}} - 1 \right)$$

$$vd = v_{node1} - v_{node2}$$

For reverse bias, the anode (node1) is more negative than the cathode. The diode is turned off, and conducts a small leakage current.

Reverse Bias: BVeff < vd < -10 · vt

$$id = -ISeff$$

For breakdown, the parameter BV (VB) is set, inducing reverse breakdown or avalanche. This effect is seen in Zener diodes and occurs when the anode-cathode voltage is less than BV. Model this action by measuring the voltage (BV) and the current (IBV) at the reverse knee or onset of avalanche.

Note: BV is always described as a positive number**.**

Breakdown: vd < - BVeff

$$id = -ISeff \cdot e^{-\left(\frac{vd + BVeff}{N \cdot vt}\right)}$$

The BV parameter is adjusted as follows to obtain BVeff:

$$ibreak = -ISeff \cdot \left(e^{\frac{-BV}{N \cdot vt}} - 1\right)$$

If IBVeff > ibreak, then,

$$BVeff = BV - N \cdot vt \cdot \ln\left(\frac{IBVeff}{ibreak}\right)$$

Otherwise,

$$IBVeff = ibreak$$

Most diodes do not behave as ideal diodes. The parameters IK and IKR are called high-level injection parameters. They tend to limit the exponential current increase.

Note: The exponential equation is used in both the forward and reverse regions.

Forward Bias

$$id = \frac{id1}{1 + \left(\frac{id1}{IKeff}\right)^{1/2}}$$

Reverse Bias

$$id = \frac{id1}{1 + \left(\frac{id1}{IKReff}\right)^{1/2}}$$

where id1 is

For vd $\geq$ -BV_{eff}:

$$id1 = ISeff \cdot \left(e^{\frac{vd}{N \cdot vt}} - 1\right)$$

Otherwise:

$$id1 = ISeff \cdot \left(e^{\frac{vd}{N \cdot vt}} - 1\right) - ISeff \cdot \left[e^{-\left(\frac{vd + BVeff}{N \cdot vt}\right)} - 1\right]$$

You can estimate the reverse saturation current IS, emission coefficient N, and model parameter RS from DC measurements of the forward biased diode characteristics. You can determine N from the slope of the diode characteristic in the ideal region. In most cases, the emission coefficient is the value of unit, but is closer to 2 for MOS diodes.

In practice, at higher levels of bias, the diode current deviates from the ideal exponential characteristic. This deviation is due to the presence of ohmic resistance in the diode as well as high-level injection effects. The deviation of the actual diode voltage from the ideal exponential characteristic at a specific current determines the value of RS. In practice, RS is estimated at several values of id and averaged, since the value of RS depends upon diode current.

Using Diode Capacitance Equations

The diode capacitance is modeled by *cd* in Figure 3-2. The capacitance, *cd*, is a combination of diffusion capacitance, (*cdiff*), depletion capacitance, (*cdep*), metal, (*cmetal*), and poly capacitances, (*cpoly*).

$$cd = cdiff + cdep + cmetal + cpoly$$

Using Diffusion Capacitance Equations

The transit time (TT) models the diffusion capacitance, caused by injected minority carriers. In practice, TT is estimated from pulsed time-delay measurements.

$$\text{cdiff} = \text{TT} \cdot \frac{\partial \text{id}}{\partial \text{vd}}$$

Using Depletion Capacitance Equations

The depletion capacitance is modeled by junction bottom and junction periphery capacitances. The formula for both bottom area and periphery capacitances is similar, except each has its own model parameters. There are two equations for forward bias junction capacitance that are selected using .OPTIONS DCAP.

DCAP=1

The junction bottom area capacitance formula is:

vd < FC · **PB**

$$\text{cdepa} = \text{CJeff} \cdot \left(1 - \frac{\text{vd}}{\text{PB}}\right)^{-\text{MJ}}$$

vd FC· **PB**

$$\text{cdepa} = \text{CJeff} \cdot \frac{1 - \text{FC} \cdot (1 + \text{MJ}) + \text{MJ} \cdot \frac{\text{vd}}{\text{PB}}}{(1 - \text{FC})^{(1 + \text{MJ})}}$$

The junction periphery capacitance formula is:

vd < FCS · **PHP**

$$\text{cdepp} = \text{CJPeff} \cdot \left(1 - \frac{\text{vd}}{\text{PHP}}\right)^{-\text{MJSW}}$$

vd FCS· **PHP**

$$cdepp = CJPeff \cdot \frac{1 - FCS \cdot (1 + MJSW) + MJSW \cdot \frac{vd}{PHP}}{(1 - FCS)^{(1 + MJSW)}}$$

then,

$$cdep = cdepa + cdepp$$

DCAP=2 (default)

The total depletion capacitance formula is:

vd < 0

$$cdep = CJeff \cdot \left(1 - \frac{vd}{PB}\right)^{-MJ} + CJPeff \cdot \left(1 - \frac{vd}{PHP}\right)^{-MJSW}$$

vd 0

$$cdep = CJeff \cdot \left(1 + MJ \cdot \frac{vd}{PB}\right) + CJPeff \cdot \left(1 + MJSW \cdot \frac{vd}{PHP}\right)$$

DCAP=3

Limits peak depletion capacitance to FC · CGDeff or FC · CGSeff, with proper fall-off when forward bias exceeds PB (FC ≥ 1).

Metal and Poly Capacitance Equations (LEVEL=3 Only)

To determine the metal and poly capacitances, use the equations:

$$:metal = \left(\frac{\varepsilon_{ox}}{XOI}\right) \cdot (WPeff + XPeff) \cdot (LPeff + XPeff) \cdot M$$

$$cpoly = \left(\frac{\varepsilon_{ox}}{XOM}\right) \cdot (WMeff + XMeff) \cdot (LMeff + XMeff) \cdot M$$

Using Noise Equations

Figure 3-4 shows the noise model for a diode. An independent current source, *inrs*, in parallel with the resistor, models the thermal noise generated by a resistor. To determine the value of *inrs*, use the equation:

$$\text{inrs} = \left(\frac{4 \cdot k \cdot t}{RSeff}\right)^{1/2}$$

The unit of inrs is Amp/(Hz)$^{1/2}$.

The shot and flicker noise of the diode are modeled by the current source *ind*, which is defined by:

$$\text{ind} = \left(2 \cdot q \cdot id + \frac{KF \cdot id^{AF}}{f}\right)^{1/2}$$

Temperature Compensation Equations

This section describes the temperature compensation equations.

Energy Gap Temperature Equations

Use the following equations to determine energy gap for temperature compensation.

TLEV=0 or 1

$$\text{egnom} = 1.16 - 7.02\text{e-}4 \cdot \frac{tnom^2}{tnom + 1108.0}$$

$$\text{eg}(t) = 1.16 - 7.02\text{e-}4 \cdot \frac{t^2}{t + 1108.0}$$

TLEV=2

$$egnom = EG - GAP1 \cdot \frac{tnom^2}{tnom + GAP2}$$

$$eg(t) = EG - GAP1 \cdot \frac{t^2}{t + GAP2}$$

Leakage Current Temperature Equations

$$JS(t) = JS \cdot e^{\frac{facln}{N}}$$

$$JSW(t) = JSW \cdot e^{\frac{facln}{N}}$$

TLEV=0 or 1

$$facln = \frac{EG}{vt(tnom)} - \frac{EG}{vt(t)} + XTI \cdot \ln\left(\frac{t}{tnom}\right)$$

TLEV=2

$$facln = \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)} + XTI \cdot \ln\left(\frac{t}{tnom}\right)$$

Breakdown Voltage Temperature Equations

TLEV=0

$$BV(t) = BV - TCV \cdot \Delta t$$

TLEV=1 or 2

$$BV(t) = BV \cdot (1 - TCV \cdot \Delta t)$$

Transit Time Temperature Equations

$$TT(t) = TT \cdot (1 + TTT1 \cdot \Delta t + TTT2 \cdot \Delta t^2)$$

Junction Built-in Potential Temperature Equations

TLEVC=0

$$PB(t) = PB \cdot \left(\frac{t}{tnom}\right) - vt(t) \cdot \left[3 \cdot \ln\left(\frac{t}{tnom}\right) + \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)}\right]$$

$$PHP(t) = PHP \cdot \frac{t}{tnom} - vt(t) \cdot \left[3 \cdot \ln\left(\frac{t}{tnom}\right) + \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)}\right]$$

TLEVC=1 or 2

$$PB(t) = PB - TPB \cdot \Delta t$$
$$PHP(t) = PHP - TPHP \cdot \Delta t$$

TLEVC=3

$$PB(t) = PB + dpbdt \cdot \Delta t$$
$$PHP(t) = PHP + dphpdt \cdot \Delta t$$

where TLEV=0 or 1

$$dpbdt = \frac{-\left[egnom + 3 \cdot vt(tnom) + (1.16 - egnom) \cdot \left(2 - \frac{tnom}{tnom + 1108}\right) - PB\right]}{tnom}$$

$$dphbdt = \frac{-\left[egnom + 3 \cdot vt(tnom) + (1.16 - egnom) \cdot \left(2 - \frac{tnom}{tnom + 1108}\right) - PHB\right]}{tnom}$$

and TLEV=2

$$dpbdt = \frac{-\left[egnom + 3 \cdot vt(tnom) + (EG - egnom) \cdot \left(2 - \frac{tnom}{tnom + GAP2}\right) - PB\right]}{tnom}$$

$$dphpdt = \frac{-\left[egnom + 3 \cdot vt(tnom) + (EG - egnom) \cdot \left(2 - \frac{tnom}{tnom + GAP2}\right) - PHP\right]}{tnom}$$

Junction Capacitance Temperature Equations

TLEVC=0

$$CJ(t) = CJ \cdot \left[1 + MJ \cdot \left(4.0e\text{-}4 \cdot \Delta t - \frac{PB(t)}{PB} + 1\right)\right]$$

$$CJSW(t) = CJSW \cdot \left[1 + MJSW \cdot \left(4.0e\text{-}4 \cdot \Delta t - \frac{PHP(t)}{PHP} + 1\right)\right]$$

TLEVC=1

$$CJ(t) = CJ \cdot (1 + CTA \cdot \Delta t)$$
$$CJSW(t) = CJSW \cdot (1 + CTP \cdot \Delta t)$$

TLEVC=2

$$CJ(t) = CJ \cdot \left(\frac{PB}{PB(t)}\right)^{MJ}$$

Note: In the above equation MJ is not MJ(t).

$$CJSW(t) = CJSW \cdot \left(\frac{PHP}{PHP(t)}\right)^{MJSW}$$

TLEVC=3

$$CJ(t) = CJ \cdot \left(1 - 0.5 \cdot dpbdt \cdot \frac{\Delta t}{PB}\right)$$

$$CJSW(t) = CJSW \cdot \left(1 - 0.5 \cdot dphpdt \cdot \frac{\Delta t}{PHP}\right)$$

Grading Coefficient Temperature Equation

$$MJ(t) = MJ \cdot (1 + TM1 \cdot \Delta t + TM2 \cdot \Delta t^2)$$

Resistance Temperature Equations

$$RS(t) = RS \cdot (1 + TRS \cdot \Delta t)$$

Using the Junction Cap Model

This section describes how to use the junction cap model statement.

General Syntax

The general syntax for including a diode element in a Star-Hspice netlist is:

```
Dxxx nodeplus nodeminus modelname <<area=>val>
+ <<peri=>val> <<pgate>=val> <<dtemp>=val>
+ <<off>=val> <<IC=>val> <<m=>val>
```

where:

Dxxx	Diode element name. Must begin with “D”
nodeplus	Positive terminal (anode) node name. The series resistor of the equivalent circuit is attached to this terminal
nminus	Negative terminal (cathode) node name
mname	Diode model name reference
area	Diode area. In the model card, it can be used by AB
peri	Length of the side-wall of the diffusion area AB which is not under the gate. In the model card, it is used by LS
pgate	Length of the side-wall of the diffusion area AB which is under the gate. In the model card, it is used by LG
off	Sets initial condition to OFF for this element in DC analysis. The default is ON
M	Multiplier to simulate multiple diodes in parallel. All currents, capacitances and resistances are affected by setting M. Default=1

ic	Initial voltage across the diode element. This value is used when the UIC option is present in the .tran statement and is overridden by the .ic statement
Dtemp	The difference between the element temperature and circuit temperature in celsius. Default=0.0
.option list	Prints the updated temperature parameters for juncap diode model

Juncap Model Syntax

The juncap model statement syntax is:

```
.MODEL modelname D level=4 <keyword=val>
```

where:

modelname	Model name. The diode element refers to the model by this name
D	Symbol that identifies a diode model
LEVEL	Symbol that identifies a diode model
keywords	Model parameter keywords, listed below in the examples

Examples

```
.model MD D level=4
+AB=2E-12 LS=2E-6 LG=1.3E-6 DTA=0 TR=30 VR=0.3
+JSGBR=1.2e-3 JSDBR=1.3e-3 JSGSR=1.1e-3
+JSDSR=1.3e-3 JSGGR=1.4e-3 JSDGR=1.4e-3 NB=1.6
+NS=1.3
+NG=1.3 VB=0.9 CJBR=1.2e-12 CJSR=1.2e-12
+CJGR=1.3e-12 VDBR=1.6 VDSR=1.3 VGDR=1.2 PB=0.5
+PS=0.6 PG=0.4
```

Setting Juncap Model Parameters

Table 3-12: Juncap Model Parameters

Name	Units	Default	Clip Low	High	Description
AB	M^2	1e-12	0.0		Diffusion area
LS	M	1.0e-6	0.0		Length of side-wall of diffusion area AB which is not under gate
LG	M	0.0	0.0		Length of side-wall of diffusion area AB which is under gate
DTA	C	0.0			Temperature offset of Juncap element with respect to TA
TR	C	25	-273.15		Temperature at which parameters have been determined
VR	V	0.0			Voltage at which parameters have been determined
JSGBR	Am^{-2}	1.0E-3	0.0		Bottom saturation-current density due to electron-hole gene ration at V=VR
JSDBR	Am^{-2}	1.0E-3	0.0		Bottom saturation-current density due to diffusion from back contact

Table 3-12: Juncap Model Parameters *(Continued)*

Name	Units	Default	Clip Low	High	Description
JSGSR	Am^{-2}	1.0E-3	0.0		Sidewall saturation-current density due to electron-hole generation at V=VR
JSDSR	Am^{-2}	1.0E-3	0.0		Sidewall saturation-current density due to diffusion from back contact
JSGGR	Am^{-2}	1.0E-3	0.0		Gate edge saturation current density due to electron-hole generation at V=VR
JSDGR	Am^{-2}	1.0E-3	0.0		Gate edge saturation current density due to diffusion from back contact
JSGGR	Am^{-2}	1.0E-3	0.0		Gate edge saturation current density due to electron-hole generation at V=VR
JSDGR	Am^{-2}	1.0E-3	0.0		Gate edge saturation current density due to diffusion from back contact
NB		1.0	0.1		Emission coefficient of the bottom forward current
NS		1.0	0.1		Emission coefficient of the sidewall forward current

Table 3-12: Juncap Model Parameters *(Continued)*

Name	Units	Default	Clip Low	High	Description
NG		1.0	0.1		Emission coefficient of the gate edge forward current
VB	V	0.9			Reverse breakdown voltage
CJBR	Fm^{-2}	1.0E-12	0.0		Bottom junction capacitance at V=VR
CJSR	Fm^{-2}	1.0E-12	0.0		Sidewall junction capacitance at V=VR
CJGR	Fm^{-2}	1.0E-12	0.0		Gate edge junction capacitance at V=VR
VDBR	V	1.00	0.05		Diffusion voltage of the bottom junction at T=TR
VDSR	V	1.00	0.05		Diffusion voltage of the sidewall junction at T=TR
VDGR	V	1.00	0.05		Diffusion voltage of the gate edge junction
PB		0.40	0.05		Bottom junction grading coefficient
PS		0.40	0.05		Sidewall junction grading coefficient
PG		0.40	0.05		Gate edge junction grading coefficient

Theory

This section summarizes the elementary physics of a junction diode. Refer to semiconductor textbooks for additional information.

Generally, the current voltage characteristics can be represented as follows:

$$J = \{J_d(n_i^2 + (J_g(n_i, V))\} \cdot \left[\exp\left(\frac{qv}{kT}\right) - 1\right]$$

$$ni \sim T^{\frac{3}{2}} \cdot \exp\left(\frac{-E_g}{2kT}\right)$$

Table 3-13: Current Voltage Characteristics

Quantity	Units	Description
J	Am^{-2}	Total reverse current density
J_d	Am^{-2}	Diffusion saturation current density
J_g	Am^{-2}	Generation current density
n_i	m^{-3}	Intrinsic carrier concentration
V	V	Voltage across the diode
E_g	J	Energy gap
k	JK^{-1}	Boltzmann constant
T	K	Temperature

For $V<V_D$, the charge of the junction capacitance is described by:

$$Q = Q_j\left[1 - \left(1 - \frac{V}{V_D}\right)^{1-P}\right]$$

Table 3-14: Junction Capacitance Charge

Quantity	Units	Description
Q	C	Total diode junction charge
Q_j	C	Junction charge at built-in voltage
V	V	Voltage across the diode
Vd	V	Junction diffusion voltage
P		Junction grading coefficient

JUNCAP Model Equations

JUNCAP Model

The JUNCAP model is intended to describe formed by the source, drain or well-to-bulk junction devices, limited to the case of reverse biasing of these junctions. Similar to the MOS model, the current equations are formulated and AC effects are modeled via charge equations using the quasi-static approximation.

In order to include the effects from differences in the sidewall, bottom, and gate-edge junction profiles, these three contributions are calculated separately in the JUNCAP model.

Both the diffusion and the generation currents are treated in the model, each with individual temperature and voltage dependence.

In the JUNCAP model, a part of the total charge comes from the gate-edge junction very close to the surface. This charge is also included in the MOS model charge equations and is counted twice. However, this results in only a very minor error.

In the next section, the model equations are presented. Correct operation of the model in a circuit simulator environment requires some numerical additions, which are described in the section on implementation. Any fixed capacitance that is present on a node (e.g., metal-1-to-substrate capacitance) must appear in a fixed capacitor statement or must be included in INTCAP. They no longer form the JUNCAP model in contrast to the old NODCAP model.

Nomenclature

The following table lists the electrical variable parameters:

Table 3-15: Electrical Variable Parameters

No	Variable	Programming Name	Units	Description
1	V_a	VA	V	Potential applied to the anode
2	V_k	VK	V	Potential applied to the cathode
3	I_a	IA	A	DC current into the anode
4	I_k	IK	A	DC current into the cathode
5	Q_a	QA	C	Charge in the device attributed to the anode
6	Q_k	QK	C	Charge in the device attributed to the cathode

Note: The parameters are listed above in the model card. See ‘Setting Juncap Model Parameters” on page 3-34.

The following table lists internal variables and parameters:

Table 3-16: Internal Variables and Parameters

No	Parameter	Programming Name	Units	Description
1	V_{db}	VDB	V	Diffusion voltage of bottom area AB
2	V_{ds}	VDS	V	Diffusion voltage of Locos-edge L S
3	V_{dg}	VDG	V	Diffusion voltage of gate-edge L G
4	C_{jb}	CJB	F	Capacitance of bottom area A B

Table 3-16: Internal Variables and Parameters *(Continued)*

No	Parameter	Programming Name	Units	Description
5	C_{js}	CJS	F	Capacitance of Locos-edge L S
6	C_{jg}	CJG	F	Capacitance of gate-edge L G
7	I_{sdb}	ISDB	A	Diffusion saturation current of bottom area AB
8	I_{sds}	ISDS	A	Diffusion saturation current of Locos-edge LS
9	I_{sdg}	ISDG	A	Diffusion saturation current of gate-edge LG
10	I_{sgb}	ISGB	A	Generation saturation current of bottom area AB
11	I_{sgs}	ISGS	A	Generation saturation current of Locos-edge LS
12	I_{sgg}	ISGG	A	Generation saturation current of gate-edge LG
13	T_a	TA	C	Ambient circuit temperature
14	T_{kd}	TKD	K	Absolute temperature of the junction/ device
15	V	V	V	Diode bias voltage (V=VA - VK)
16	I	I	A	Total DC current from anode to cathode (I = IA = -IK)
17	Q	Q	C	Total junction charge (Q = QA = - QK)

ON/OFF Condition

Circuit solution involves a process of successive calculations. The calculations are started from a set of “initial guesses” for the electrical quantities of the non-linear elements. The devices start in the default state.

Example

JUNCAP	Default	ON	OFF
V_D	-0.1	0.7	-0.1

DC Operating Point Output

The DC operating point output facility gives information on the state of a device at its operation point.

Note: The conductance G min is connected in parallel to the conductance G. This conductance influences the DC operating output.

Temperature, Geometry and Voltage Dependence

The general scaling rules, which apply to all three components of the JUNCAP model, are:

$$T_{KR} = T_0 + T_R$$

$$T_{KD} = T_0 + T_A + DT_A$$

$$V_{TR} = k \cdot \frac{T_{KR}}{q}$$

$$V_{TD} = K \cdot \frac{T_{KD}}{q}$$

$$V_{gR} = 1.16 - \frac{(7.02 \cdot 10e-4 \cdot T_{KR} \cdot T_{KR})}{(1108.0 + T_{KR})}$$

$$V_{gD} = 1.16 - \frac{(7.02 \cdot 10e-4 \cdot T_{KR} \cdot T_{KD})}{(1108.0 + T_{KD})}$$

$$F_{TD} = \left(\frac{T_{KD}}{T_{KR}}\right)^{1.5} \cdot \exp\left(\frac{V_{gR}}{(2 \cdot V_{TR})} - \frac{V_{gD}}{(2 \cdot V_{TD})}\right)$$

Internal Reference

The internal reference parameters for the bottom component are specified by:

$$V_{DB} = \frac{V_{DBR} \cdot T_{KD}}{T_{KR} - 2 \cdot V_{TD} \cdot 1nF_{TD}}$$

$$C_{JB} = C_{JBR} \cdot A_B \cdot \left(\frac{(V_{DBR} - V_R)}{V_{DB}}\right)^{P_B}$$

$$I_{SGB} = J_{SGBR} \cdot F_{TD} \cdot A_B \cdot \left(\frac{V_{DB}}{(V_{DBR} - V_R)}\right)^{P_B}$$

$$I_{SDB} = J_{SDBR} \cdot F_{TD} \cdot F_{TD} \cdot A_B$$

Similar formulations hold for the locos-edge and the gate-edge components. Replace the index *B* by *S* and *G*, and the area *AB* by *LS* and *LG*.

For the locos-edge:

$$V_{DS} = \frac{V_{DSR} \cdot T_{KR}}{T_{KR} - 2 \cdot V_{TD} \cdot 1nF_{TD}}$$

$$C_{JS} = C_{JSR} \cdot L_S \cdot \left(\frac{(V_{DSR} - V_R)}{V_{DS}}\right)^{P_S}$$

$$I_{SGS} = J_{SGSR} \cdot F_{TD} \cdot L_S \cdot \left(\frac{V_{DS}}{(V_{DSR} - V_R)}\right)^{P_S}$$

$$I_{SDS} = J_{SDSR} \cdot F_{TD} \cdot F_{TD} \cdot L_S$$

For the gate-edge:

$$V_{DG} = \frac{V_{DGR} \cdot T_{KD}}{T_{KR} - 2 \cdot V_{TD} \cdot 1nF_{TD}}$$

$$C_{JG} = C_{JGR} \cdot L_G \cdot \left(\frac{(V_{DGR} - V_R)}{V_{DG}}\right)^{P_G}$$

$$I_{SGS} = J_{SGGR} \cdot F_{TD} \cdot L_G \cdot \left(\frac{V_{DG}}{(V_{DGR} - V_R)}\right)^{P_G}$$

$$I_{SDS} = J_{SDGR} \cdot F_{TD} \cdot F_{TD} \cdot L_G$$

Note: Later sections show the equations only for the bottom component.

JUNCAP Capacitor and Leakage Current Model

In the charge description, the following internal parameter is defined:

$$Q_{JDB} = C_{JB} \cdot V_{DB}(1 - P_B)$$

To prevent an unlimited increase of the voltage derivative of the charge, the charge description is in two parts: the original power function and a supplemented quadratic function. At the cross-over point between these regions, indicated by Vl, the following parameters are defined:

$$F_{CB} = 1 - \left(\frac{(1 + P_B)}{3}\right)^{\frac{1}{P_B}}$$

$$V_{LB} = F_{CB} \cdot V_{DB}$$

$$C_{LB} = C_{JB}(1 - F_{CB})^{-P_B}$$

$$Q_{LB} = Q_{JDB}(1 - (1 - F_{CB})^{(1 - P_B)})$$

$$Q_{JBV} = Q_{JCB} \cdot \left(\frac{(1 - (1 - V))}{V_{DB}}\right)^{(1 - P_B)} \quad V < V_{LB}$$

$$Q_{LB} + C_{LB}(V - V_{LB}) \cdot \left(\frac{1 + (P_B(V - V_{LB}))}{2 \cdot V_{DB} \cdot (1 - F_{CB})}\right) \quad V >= V_{LB} \qquad (12.63)$$

Similar expressions exist for the locos-edge and gate-edge charges, *Qjsv* and *Qjgv*.

The total charge characteristic can be described by:

$$Q = Q_{JBV} + Q_{JSV} + Q_{JGV}$$

Using elementary mathematics, we can derive from Equation 12.63 (above) simple equations for the capacitance of the bottom area:

$$C_{JBV} = C_{JB} \cdot \left(1 \Big/ \left(\frac{1 - v}{V_{DB}}\right)\right)^{P_B} \qquad V < V_{LB}$$

$$C_{LB} + C_{LB} \cdot P_B \cdot \left(\frac{(V - V_{LB})}{V_{DB} \cdot (1 - F_{CB})}\right) \qquad V \geq V_{LB}$$

Similar expressions exist for *Cjsv* and *Cjgv*.

Total Capacitance

The total capacitance can be described by:

$$C = C_{JBV} + C_{JSV} + C_{JGV}$$

*Bulk to source or bulk to drain diode current.

Diffusion and Generation Currents

With the scaled parameters of the preceding section, the diffusion and generation current components can be expressed as:

$$I_{DB} = I_{SDB} \cdot \exp\left(\frac{V}{(N_B \cdot V_{TD})} - 1\right)$$

$$I_{GB} = I_{SGB} \cdot \left(\frac{(V_{DB} - V)}{V_{DB}}\right)^{P_B} \cdot \left(\exp\left(\left(\frac{V}{N_B \cdot V_{TD}}\right) - 1\right)\right) \qquad V \leq V_{DB}$$

$$0 \qquad V > V_{DB}$$

The first relation concerning the diffusion component is valid over the whole operating range. The second relation, describing the generation current, shows an unlimited increase in the derivative of this function at $V=V_{DB}$. Therefore, the power function is merged at V=0.0 with a hyperbolic function in the forward bias range. The exponential part is divided by $\exp(V/(N_B \cdot V_{TD}))$. This enables a gradual decrease in the generation current component.

The hyperbolic function $I_{HYP} = F_{SB}(V + V_{AB})^{-B}$ is used. The parameter *B* controls the decrease of the current for voltages V>0.0 for all generation components. The value of *B* is fixed and set to 2 in the model. The continuity constraints of function and derivative in the merge point lead to the following relations for F_{sb} and V_{ab}:

$$V_{AB} = B \cdot \frac{V_{DB}}{P_B}$$

$$F_{SB} = I_{SGB} \cdot V_{AB}B$$

The generation current voltage characteristic in the forward region becomes:

$$I_{GB} = F_{SB}/((V + V_{AB})^B) \cdot (1 - \exp(-v)/(N_B \cdot V_{TD}))$$

Final Model Equations

The final model equations for the currents of the bottom area are:

$$I_{DB} = I_{SDB} \cdot (\exp(V/(N_B \cdot V_{TD})) - 1)$$

$$I_{GB} = I_{SGB} \cdot \left(\frac{V_{DB} - V}{V_{DB}}\right)^{P_B} \cdot \exp\left(\frac{V}{(N_B \cdot V_{TD})}\right) - 1 \qquad V \le 0$$

$$Isgb \cdot \left(\frac{Vab}{(V + Vab)}\right)^B \cdot \left(1 - \exp\left(\frac{-V}{(Nb \cdot Vtd)}\right)\right) \qquad V > 0.0$$

Similar expressions exist for the locos-edge and gate-edge components.

The total junction current can be expressed as:

$$I = (I_{DB} + I_{GB}) + (I_{DS} + I_{GS}) + (I_{DG} + I_{GG})$$

Using the Fowler-Nordheim Diode

The diode model parameter LEVEL=2 selects the Fowler-Nordheim model. Fowler- Nordheim diodes are formed as a metal-insulator-semiconductor or as a semiconductor-insulator-semiconductor layer device. The insulator is sufficiently thin (100 Angstroms) to permit tunneling of carriers. It models electrically alterable memory cells, air-gap switches, and other insulation breakdown devices.

Fowler-Nordheim Diode Model Parameters LEVEL=2

Table 3-17 shows the Fowler-Nordheim diode model parameters for LEVEL 2.

Table 3-17: Fowler-Nordheim Diode Model Parameters

Name (alias)	Units	Default	Description
EF	V/cm	1.0e8	Forward critical electric field
ER	V/cm	EF	Reverse critical electric field
JF	amp/V^2	1.0e-10	Forward Fowler-Nordheim current coefficient
JR	amp/V^2	JF	Reverse Fowler-Nordheim current coefficient
L	m	0.0	Length of diode for calculation of Fowler-Nordheim current Leff = L · SCALM · SHRINK + XWeff
TOX	Å	100.0	Thickness of oxide layer
W	m	0.0	Width of diode for calculation of Fowler-Nordheim current Weff = W · SCALM · SHRINK + XWeff
XW	m	0.0	XWeff = XW · SCALM

Using Fowler-Nordheim Diode Equations

The DC characteristics of the Fowler-Nordheim diode are modeled by the following forward and reverse nonlinear current source equations. In the following equations:

$$AREAeff = Weff \cdot Leff \cdot M$$

Forward Bias: vd 0

$$id = AREAeff \cdot JF \cdot \left(\frac{vd}{TOX}\right)^2 \cdot e^{\frac{-EF \cdot TOX}{vd}}$$

Reverse Bias: vd < 0

$$id = -AREAeff \cdot JR \cdot \left(\frac{vd}{TOX}\right)^2 \cdot e^{\frac{ER \cdot TOX}{vd}}$$

Fowler-Nordheim Diode Capacitances

The Fowler-Nordheim diode capacitance is a constant derived from:

$$cd = AREAeff \cdot \frac{\varepsilon_{ox}}{TOX}$$

Converting National Semiconductor Models

National Semiconductor's circuit simulator has a scaled diode model that is not the same as that used by Star-Hspice. To use National Semiconductor circuit models, do the following:

For a subcircuit that consists of the scaled diode model, the subcircuit name must be the same as the name of the model.

The .PARAM statement inside the subcircuit specifies the scaled diode model parameter values. Add a scaled diode model inside the subcircuit, then change the `.MODEL mname mtype` statement to a .PARAM statement.

Ensure that all the scaled diode elements are preceded by the character X.

Check that every parameter used in the .MODEL statement inside the subcircuit has a value in the .PARAM statement.

Using the Scaled Diode Subcircuit Definition

The scaled diode subcircuit definition converts the National Semiconductor scaled diode model to a form a model usable in Star-Hspice. The .PARAM parameter inside the .SUBCKT represents the .MODEL parameter in the National circuit simulator. Replace the .MODEL mname statement by a .PARAM statement. Change the model name to SDIODE.

Example

An example of scaled diode subcircuit definition is:

```
.SUBCKT SDIODE NP NN SF=1 SCJA=1 SCJP=0 SIS=1 SICS=1
+ SRS=1
D NP NN SDIODE
.PARAM IS=1.10E-18 N=1.03 EG=0.8 RS=20.7E3
+ CJA=0.19E-15 PHI=0.25 CJP=0.318E-15
+ EXA=0.5 EXP=0.325 CTC=6E-4
+ TRS=2.15M M=2
*
.MODEL SDIODE D
+ IS='IS*SIS*SF' CJA='CJA*SF*SCJA' CJP='CJP*SF*SCJP'
+ RS='RS*SRS/SF' EXA=EXA EXP=EXP
+ N=N CTA=CTC CTP=CTC
+ TRS=TRS TLEV=1 TLEVC=1 xti='m*n'
.ENDS SDIODE
```

Note that all the parameters used in the following model must have a value that comes from either a .PARAM statement or the .SUBCKT call. The diode statements are then replaced by the call to the subcircuit SDIODE:

```
XDS 14 1048 SDIODE SIS=67.32 SCJA=67.32 SRS=1.2285E-2
```

Avant!

Chapter 4
Using BJT Models

The bipolar-junction transistor (BJT) model is an adaptation of the integral charge control model of Gummel and Poon.

The Avant! BJT model extends the original Gummel-Poon model to include several effects at high bias levels. This model automatically simplifies to the Ebers-Moll model when certain parameters (VAF, VAR, IKF, and IKR) are not specified.

This chapter covers the following topics:

Using BJT Models

The BJT model is used to develop BiCMOS, TTL, and ECL circuits. For BiCMOS devices, use the high-current Beta degradation parameters, IKF and IKR, to modify high injection effects. The model parameter SUBS facilitates the modeling of both vertical and lateral geometrics.

Selecting Models

To select a BJT device, use a BJT element and model statement. The element statement uses the name of the simulation device model, to reference the model statement. The following example uses the reference name MOD1. This example uses an NPN model type to describe an NPN transistor.

Example

```
Q3 3 2 5 MOD1 <parameters>
.MODEL MOD1 NPN <parameters>
```

You can specify parameters in both element and model statements. If you specify the same parameter in both an element and a model, then the element parameter (local to the specific instance of the model) always overrides the model parameter (global default for all instances of the model, where the parameter is not defined locally). The model statement specifies the type of device—for example, for a BJT, the device type might be NPN or PNP.

Using Control Options

Control options affecting the BJT model are: DCAP, GRAMP, GMIN, and GMINDC. DCAP selects the equation that determines the BJT capacitances. GRAMP, GMIN, and GMINDC place a conductance in parallel with both the base-emitter and base-collector pn junctions. DCCAP invokes capacitance calculations in DC analysis. The BJT control options follow:

Function	Control Options
Capacitance	DCAP, DCCAP
Conductance	GMIN, GMINDC

You can override global depletion capacitance equation selection that uses the .OPTION DCAP=<*val*> statement in a BJT model by including DCAP=<val> in the BJTs .MODEL statement.

Convergence

Adding a base, collector, and emitter resistance to the BJT model improves its convergence. The resistors limit the current in the device so that the forward-biased pn junctions are not overdriven.

BJT Model Statement

Syntax

```
.MODEL mname NPN <(> <pname1 = val1> ... <)>
```

or

```
.MODEL mname PNP <pname1 = val1> ...
```

mname	Model name. Elements refer to the model by this name.
NPN	Identifies an NPN transistor model
pname1	Each BJT model can include several model parameters.
PNP	Identifies a PNP transistor model

Example

```
.MODEL t2n2222a NPN
+ ISS= 0.         XTF=  1.         NS =  1.00000
+ CJS= 0.         VJS=  0.50000    PTF=  0.
+ MJS= 0.         EG =  1.10000    AF =  1.
+ ITF= 0.50000    VTF=  1.00000
+ BR = 40.00000    IS =  1.6339e-14 VAF= 103.40529
+ VAR= 17.77498    IKF=  1.00000
+ NE = 1.31919    IKR=  1.00000    ISC=  3.6856e-13
+ NC = 1.10024    IRB=  4.3646e-05 NF =  1.00531
+ NR = 1.00688    RBM=  1.0000e-02 RB = 71.82988
+ RC = 0.42753    RE =  3.0503e-03 MJE=  0.32339
+ MJC= 0.34700    VJE=  0.67373    VJC=  0.47372
+ TF = 9.693e-10  TR = 380.00e-9    CJE=  2.6734e-11
+ CJC= 1.4040e-11 FC =  0.95000   XCJC=  0.94518
```

Using BJT Basic Model Parameters

To permit the use of model parameters from earlier versions of Star-Hspice and Star-Sim, many of the model parameters have aliases, which are included in the model parameter list in ‘Using BJT Basic DC Model Parameters” on page 4-6. The new name is always used on printouts, even if an alias is used in the model statement.

BJT model parameters are divided into several groups. The first group of DC model parameters includes the most basic Ebers-Moll parameters. This model is effective for modeling low-frequency large-signal characteristics.

Low-current Beta degradation effect parameters ISC, ISE, NC, and NE aid in modeling the drop in the observed Beta, caused by the following mechanisms:

- Recombination of carriers in the emitter-base space charge layer
- Recombination of carriers at the surface
- Formation of emitter-base channels

Low base and emitter dopant concentrations, found in some BIMOS type technologies, use the high-current Beta degradation parameters, IKF and IKR.

Use the base-width modulation parameters, that is, early effect parameters VAF and VAR, to model high-gain, narrow-base devices. The model calculates the slope of the I-V curve for the model in the active region with VAF and VAR. If VAF and VAR are not specified, the slope in the active region is zero.

The parasitic resistor parameters RE, RB, and RC are the most frequently used second-order parameters since they replace external resistors. This simplifies the input netlist file. All of the resistances are functions of the BJT multiplier M value. The resistances are divided by M to simulate parallel resistances. The base resistance is also a function of base current, as is often the case in narrow-base technologies.

Transient model parameters for BJTs are composed of two groups: junction capacitor parameters and transit time parameters. The base-emitter junction is modeled by CJE, VJE, and MJE. The base-collector junction capacitance is modeled by CJC, VJC, and MJC. The collector-substrate junction capacitance is modeled by CJS, VJS, and MJS.

TF is the forward transit time for base charge storage. TF can be modified to account for bias, current, and phase, by XTF, VTF, ITF, and PTF. The base charge storage reverse transit time is set by TR. There are several sets of temperature equations for the BJT model parameters that you can select by setting TLEV and TLEVC.

Table 4-1: BJT Model Parameters

DC	BF, BR, IBC, IBE, IS, ISS, NF, NR, NS, VAF, VAR
beta degradation	ISC, ISE, NC, NE, IKF, IKR
geometric	SUBS, BULK
resistor	RB, RBM, RE, RC, IRB
junction capacitor	CJC, CJE, CJS, FC, MJC, MJE, MJS, VJC, VJE, VJS, XCJC
parasitic capacitance	CBCP, CBEP, CCSP
transit time	ITF, PTF, TF, VT, VTF, XTF
noise	KF, AF

Using BJT Basic DC Model Parameters

Table 4-2: DC Parameters for BJT Models *(Sheet 1 of 3)*

Name (Alias)	Unit	Default	Description
BF (BFM)		100.0	Ideal maximum forward Beta
BR (BRM)		1.0	Ideal maximum reverse Beta
BULK (NSUB)		0.0	Sets the bulk node to a global node name. A substrate terminal node name (ns) in the element statement overrides BULK.

Table 4-2: DC Parameters for BJT Models *(Sheet 2 of 3)*

Name (Alias)	Unit	Default	Description
IBC	amp	0.0	Reverse saturation current between base and collector. If you specify both IBE and IBC, simulation uses them in place of IS to calculate DC current and conductance; otherwise, the simulator uses IS. IBCeff = IBC · AREAB · M AREAC replaces AREAB, depending on vertical or lateral geometry.
EXPLI	amp	1e15	Current explosion model parameter. The PN junction characteristics above the explosion current area linear, with the slope at the explosion point. This speeds up simulation and improves convergence. EXPLIeff = EXPLI · AREAeff
IBE	amp	0.0	Reverse saturation current between base and emitter. If you specify both IBE and IBC, simulation uses them in place of IS to calculate DC current and conductance; otherwise, the simulator uses IS. IBEeff = IBE · AREA · M
IS	amp	1.0e-16	Transport saturation current. If you specify both IBE and IBC, simulation uses them in place of IS to calculate DC current and conductance; otherwise, the simulator uses IS. ISeff = IS · AREA · M

Table 4-2: DC Parameters for BJT Models *(Sheet 3 of 3)*

Name (Alias)	Unit	Default	Description
ISS	amp	0.0	Reverse saturation current bulk-to-collector or bulk-to-base, depending on vertical or lateral geometry selection. $SSeff = ISS \cdot AREA \cdot M$
Level		1.0	Model selector
NF		1.0	Forward current emission coefficient
NR		1.0	Reverse current emission coefficient
NS		1.0	Substrate current emission coefficient
SUBS			Substrate connection selector: ■ +1 for vertical geometry ■ -1 for lateral geometry ■ default=1 for NPN ■ default=-1 for PNP
UPDATE		0	UPDATE = 1 selects alternate base charge equation

Using Low-Current Beta Degradation Effect Parameters

Table 4-3: Low-Current Beta Degradation Parameters

Name (Alias)	Unit	Default	Description
ISC (C4, JLC)	amp	0.0	Base-collector leakage saturation current. If ISC is greater than 1e-4, then: $ISC = IS \cdot ISC$ otherwise: $ISCeff = ISC \cdot AREAB \cdot M$ AREAC replaces AREAB, depending on vertical or lateral geometry.
ISE (C2, JLE)	amp	0.0	Base-emitter leakage saturation current. If ISE is greater than 1e-4, then: $ISE = IS \cdot ISE$ otherwise: $ISEeff = ISE \cdot AREA \cdot M$
NC (NLC)		2.0	Base-collector leakage emission coefficient
NE (NLE)		1.5	Base-emitter leakage emission coefficient

Using Base Width Modulation Parameters

Table 4-4: Base Width Modulation Parameters

Name (Alias)	Unit	Default	Description
VAF (VA, VBF)	V	0.0	Forward early voltage. Use zero to indicate an infinite value.
VAR (VB, VRB, BV)	V	0.0	Reverse early voltage. Use zero to indicate an infinite value.

Using High-Current Beta Degradation Effect Parameters

Table 4-5: High-Current Beta Degradation Parameters

Name (Alias)	Unit	Default	Description
IKF (IK, JBF)	amp	0.0	Corner for forward Beta high-current roll-off. Use zero to indicate an infinite value. $IKFeff = IKF \cdot AREA \cdot M$
IKR (JBR)	amp	0.0	Corner for reverse Beta high-current roll-off. Use zero to indicate an infinite value. $IKReff = IKR \cdot AREA \cdot M$
NKF		0.5	Exponent for high-current Beta roll-off.

Using Parasitic Resistance Parameters

Table 4-6: Parasitic Resistance Parameters

Name (Alias)	Unit	Default	Description
IRB (JRB, IOB)	amp	0.0	Base current, where base resistance falls half-way to RBM. Use zero to indicate an infinite value. IRBeff = IRB · AREA · M
RB	ohm	0.0	Base resistance RBeff = RB / (AREA · M)
RBM	ohm	RB	Minimum high-current base resistance RBMeff = RBM / (AREA · M)
RE	ohm	0.0	Emitter resistance REeff = RE / (AREA · M)
RC	ohm	0.0	Collector resistance RCeff = RC / (AREA · M)

Using Junction Capacitor Parameters

Table 4-7: Junction Capacitor Parameters

Name (Alias)	Unit	Default	Description
CJC	F	0.0	Base-collector zero-bias depletion capacitance ■ Vertical: CJCeff = CJC · AREAB · M ■ Lateral: CJCeff = CJC · AREAC · M if you specify a value other than zero, for ibc and ibe.

Table 4-7: Junction Capacitor Parameters *(Continued)*

CJE	F	0.0	Base-emitter zero-bias depletion capacitance (vertical and lateral): CJEeff = CJE · AREA · M
CJS (CCS, CSUB)	F	0.0	Zero-bias collector substrate capacitance ■ Vertical: CJSeff = CJS · AREAC · M ■ Lateral: CJSeff = CJS · AREAB · M If you specify a value other than zero, for ibc and ibe.
FC		0.5	Coefficient for forward bias depletion capacitance formula for DCAP=1 DCAP Default=2 and FC are ignored.
MJC (MC)		0.33	Base-collector junction exponent (grading factor)
MJE (ME)		0.33	Base-emitter junction exponent (grading factor)
MJS(ESUB)		0.5	Substrate junction exponent (grading factor)
VJC (PC)	V	0.75	Base-collector built-in potential
VJE (PE)	V	0.75	Base-emitter built-in potential
VJS (PSUB)	V	0.75	Substrate junction built in potential
XCJC (CDIS)		1.0	Internal base fraction of base-collector depletion capacitance

Using Parasitic Capacitances Parameters

Table 4-8: Parasitic Capacitances Parameters

Name (Alias)	Unit	Default	Description
CBCP	F	0.0	External base-collector constant capacitance CBCPeff = CBCP · AREA · M
CBEP	F	0.0	External base-emitter constant capacitance CBEPeff = CBEP · AREA · M
CCSP	F	0.0	External collector substrate constant capacitance (vertical) or base substrate (lateral) CCSPeff = CCSP · AREA · M

Using Transit Time Parameters

Table 4-9: Transit Time Parameters

Name (Alias)	Unit	Default	Description
ITF (JTF)	amp	0.0	TF high-current parameter ITFeff = ITF · AREA · M
PTF	x	0.0	Frequency multiplier to determine excess phase
TF	s	0.0	Base forward transit time
TR	s	0.0	Base reverse transit time
VTF	V	0.0	TF base-collector voltage dependence coefficient. Zero indicates an infinite value.
XTF		0.0	TF bias dependence coefficient

Using Noise Parameters

Table 4-10: Noise Parameters

Name (Alias)	Unit	Default	Description
AF		1.0	Flicker-noise exponent
KF		0.0	Flicker-noise coefficient

Using BJT Level=2 Model Parameters

Table 4-11: Level=2 Parameters

Name (Alias)	Unit	Default	Description
BRS		1.0	Reverse beta for substrate BJT.
GAMMA		0.0	Epitaxial doping factor, $GAMMA = (2 \cdot ni / n)^2$ where *n* is epitaxial impurity concentration
NEPI		1.0	Emission coefficient
QCO	Coul	0.0	Epitaxial charge factor ■ Vertical: $QCOeff=QCO \cdot AREAB \cdot M$ ■ Lateral: $QCOeff=QCO \cdot AREAC \cdot M$ if you specify a value other than zero, for ibc and ibe.
RC	ohm	0.0	Resistance of the epitaxial region under equilibrium conditions $RCeff=RC/(AREA \cdot M)$
VO	V	0.0	Carrier velocity saturation voltage. Use zero to indicate an infinite value.

Handling BJT Model Temperature Effects

Several temperature parameters control derating of the BJT model parameters. They include temperature parameters for junction capacitance, Beta degradation (DC), and base modulation (Early effect) among others.

Table 4-12: BJT Temperature Parameters

Function	Parameter
base modulation	TVAF1, TVAF2, TVAR1, TVAR2
capacitor	CTC, CTE, CTS
capacitor potentials	TVJC, TVJE, TVJS
DC	TBF1, TBF2, TBR1, TBR2, TIKF1, TIKF2, TIKR1, TIKR2, TIRB1, TIRB2, TISC1, TISC2, TIS1, TIS2, TISE1, TISE2, TISS1, TISS2, XTB, XTI
emission coefficients	TNC1, TNC2, TNE1, TNE2, TNF1, TNF2, TNR1, TNR2, TNS1, TNS2
energy gap	EG, GAP1, GAP2
equation selectors	TLEV, TLEVC
grading	MJC, MJE, MJS, TMJC1, TMJC2, TMJE1, TMJE2, TMJS1, TMJS2
resistors	TRB1, TRB2, TRC1, TRC2, TRE1, TRE2, TRM1, TRM2
transit time	TTF1, TTF2, TTR1, TTR2

Using Temperature Effect Parameters

Table 4-13: Temperature Effect Parameters *(Sheet 1 of 5)*

Name (Alias)	Unit	Default	Description
BEX		2.42	VO temperature exponent (Level 2 only).
BEXV		1.90	RC temperature exponent (Level 2 only).
CTC	1/°	0.0	Temperature coefficient for zero-bias base collector capacitance. TLEVC=1 enables CTC to override the default temperature compensation.
CTE	1/°	0.0	Temperature coefficient for zero-bias base emitter capacitance. TLEVC=1 enables CTE to override the default temperature compensation.
CTS	1/°	0.0	Temperature coefficient for zero-bias substrate capacitance. TLEVC=1 enables CTS to override the default temperature compensation.
EG	eV		Energy gap for pn junction for TLEV=0 or 1, default=1.11; for TLEV=2, default=1.16 ■ 1.17 - silicon ■ 0.69 - Schottky barrier diode ■ 0.67 - germanium ■ 1.52 - gallium arsenide
GAP1	eV/°	7.02e-4	First bandgap correction factor (from Sze, alpha term) ■ 7.02e-4 - silicon ■ 4.73e-4 - silicon ■ 4.56e-4 - germanium ■ 5.41e-4 - gallium arsenide

Table 4-13: Temperature Effect Parameters *(Sheet 2 of 5)*

Name (Alias)	Unit	Default	Description
GAP2	x	1108	Second bandgap correction factor (Sze, beta term) ■ 1108 - silicon ■ 636 - silicon ■ 210 - germanium ■ 204 - gallium arsenide
MJC(MC)		0.33	Base-collector junction exponent (grading factor).
MJE(ME)		0.33	Base-emitter junction exponent (grading factor).
MJS (ESUB)		0.5	Substrate junction exponent (grading factor).
TBF1	$1/^{\circ}$	0.0	First-order temperature coefficient for BF.
TBF2	$1/^{\circ 2}$	0.0	Second-order temperature coefficient for BF.
TBR1	$1/^{\circ}$	0.0	First-order temperature coefficient for BR.
TBR2	$1/^{\circ 2}$	0.0	Second-order temperature coefficient for BR.
TIKF1	$1/^{\circ}$	0.0	First-order temperature coefficient for IKF.
TIKF2	$1/^{\circ 2}$	0.0	Second-order temperature coefficient for IKF.
TIKR1	$1/^{\circ}$	0.0	First-order temperature coefficient for IKR.
TIKR2	$1/^{\circ 2}$		Second-order temperature coefficient for IKR.
TIRB1	$1/^{\circ}$	0.0	First-order temperature coefficient for IRB.
TIRB2	$1/^{\circ 2}$	0.0	Second-order temperature coefficient for IRB.
TISC1	$1/^{\circ}$	0.0	First-order temperature coefficient for ISC TLEV=3 enables TISC1.
TISC2	$1/^{\circ 2}$	0.0	Second-order temperature coefficient for ISC TLEV=3 enables TISC2.

Table 4-13: Temperature Effect Parameters *(Sheet 3 of 5)*

Name (Alias)	Unit	Default	Description
TIS1	1/°	0.0	First-order temperature coefficient for IS or IBE and IBC TLEV=3 enables TIS1.
TIS2	$1/°^2$	0.0	Second-order temperature coefficient for IS or IBE and IBC TLEV=3 enables TIS2.
TISE1	1/°	0.0	First-order temperature coefficient for ISE TLEV=3 enables TISE1.
TISE2	$1/°^2$	0.0	Second-order temperature coefficient for ISE. TLEV=3 enables TISE2.
TISS1	1/°	0.0	First-order temperature coefficient for ISS TLEV=3 enables TISS1.
TISS2	$1/°^2$	0.0	Second-order temperature coefficient for ISS TLEV=3 enables TISS2.
TITF1			First-order temperature coefficient for ITF.
TITF2			Second-order temperature coefficient for ITF.
TLEV		1	Temperature equation level selector for BJTs (interacts with TLEVC).
TLEVC		1	Temperature equation level selector: BJTs, junction capacitances, and potentials (interacts with TLEV).
TMJC1	1/°	0.0	First-order temperature coefficient for MJC.
TMJC2	$1/°^2$	0.0	Second-order temperature coefficient for MJC.
TMJE1	1/°	0.0	First order temperature coefficient for MJE.
TMJE2	$1/°^2$	0.0	Second-order temperature coefficient for MJE.
TMJS1	1/°	0.0	First-order temperature coefficient for MJS.

Table 4-13: Temperature Effect Parameters *(Sheet 4 of 5)*

Name (Alias)	Unit	Default	Description
TMJS2	$1/°^2$	0.0	Second-order temperature coefficient for MJS.
TNC1	$1/°$	0.0	First-order temperature coefficient for NC.
TNC2		0.0	Second-order temperature coefficient for NC.
TNE1	$1/°$	0.0	First-order temperature coefficient for NE.
TNE2	$1/°^2$	0.0	Second-order temperature coefficient for NE.
TNF1	$1/°$	0.0	First-order temperature coefficient for NF.
TNF2	$1/°^2$	0.0	Second-order temperature coefficient for NF.
TNR1	$1/°$	0.0	First-order temperature coefficient for NR.
TNR2	$1/°^2$	0.0	Second-order temperature coefficient for NR.
TNS1	$1/°$	0.0	First-order temperature coefficient for NS.
TNS2	$1/°^2$	0.0	Second-order temperature coefficient for NS.
TRB1 (TRB)	$1/°$	0.0	First-order temperature coefficient for RB.
TRB2	$1/°^2$	0.0	Second-order temperature coefficient for RB.
TRC1 (TRC)	$1/°$	0.0	First-order temperature coefficient for RC.
TRC2	$1/°^2$	0.0	Second-order temperature coefficient for RC.
TRE1 (TRE)	$1/°$	0.0	First-order temperature coefficient for RE.
TRE2	$1/°^2$	0.0	Second-order temperature coefficient for RE.
TRM1	$1/°$	TRB1	Firs-order temperature coefficient for RBM.
TRM2	$1/°^2$	TRB2	Second-order temperature coefficient for RBM.

Table 4-13: Temperature Effect Parameters *(Sheet 5 of 5)*

Name (Alias)	Unit	Default	Description
TTF1	1/°	0.0	First-order temperature coefficient for TF.
TTF2	$1/°^2$	0.0	Second-order temperature coefficient for TF.
TTR1	1/°	0.0	First-order temperature coefficient for TR.
TTR2	$1/°^2$	0.0	Second-order temperature coefficient for TR.
TVAF1	1/°	0.0	First-order temperature coefficient for VAF.
TVAF2	$1/°^2$	0.0	Second-order temperature coefficient for VAF.
TVAR1	1/°	0.0	First-order temperature coefficient for VAR.
TVAR2	$1/°^2$	0.0	Second-order temperature coefficient for VAR.
TVJC	V/°	0.0	Temperature coefficient for VJC. TLEVC=1 or 2 enables TVJC to override the default temperature compensation.
TVJE	V/°	0.0	Temperature coefficient for VJE. TLEVC=1 or 2 enables TVJE to override the default temperature compensation.
TVJS	V/°	0.0	Temperature coefficient for VJS. TLEVC=1 or 2 enables TVJS to override the default temperature compensation.
XTB(TBTCB)		0.0	Forward and reverse Beta temperature exponent (used with TLEV=0, 1, or 2).
XTI		3.0	Saturation current temperature exponent. ■ Use XTI=3.0 for silicon diffused junction. ■ Set XTI=2.0 for Schottky barrier diode.

BJT Device Equivalent Circuits

Scaling

Scaling is controlled by the element parameters AREA, AREAB, AREAC, and M. The AREA parameter, the normalized emitter area, divides all resistors and multiplies all currents and capacitors. AREAB and AREAC scale the size of the base area and collector area. Either AREAB or AREAC is used for scaling, depending on whether vertical or lateral geometry is selected (using the SUBS model parameter). For vertical geometry, AREAB is the scaling factor for IBC, ISC, and CJC. For lateral geometry, AREAC is the scaling factor. The scaling factor is AREA for all other parameters.

The scaling of the DC model parameters (IBE, IS, ISE, IKF, IKR, and IRB) for both vertical and lateral BJT transistors, is determined by the following formula:

$$Ieff = AREA \cdot M \cdot I$$

where I is either IBE, IS, ISE, IKF, IKR, or IRB.

For both the vertical and lateral, the resistor model parameters, RB, RBM, RE, and RC are scaled by the following equation.

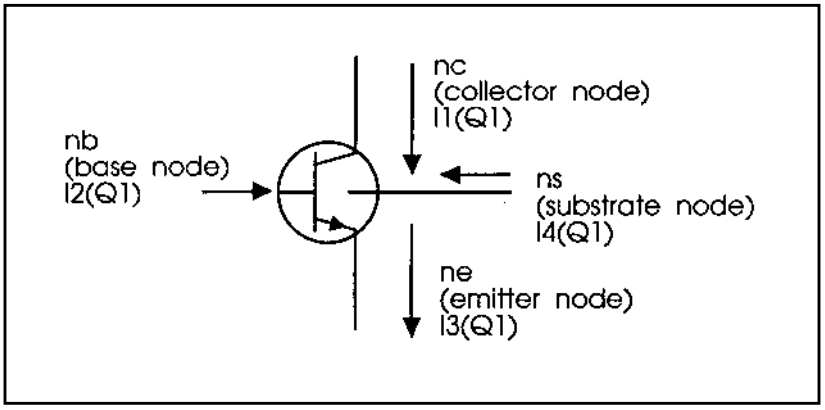
$$Reff = \frac{R}{AREA \cdot M}$$

where R is either RB, RBM, RE, or RC.

Understanding the BJT Current Convention

The direction of current flow through the BJT is assumed in the example Figure 4-1. Use either I(Q1) or I1(Q1) syntax to print the collector current. I2(Q1) refers to the base current, I3(Q1) refers to the emitter current, and I4(Q1) refers to the substrate current.

Figure 4-1: BJT Current Convention



Using BJT Equivalent Circuits

In-circuit simulation uses four equivalent circuits to analyze BJTs: DC, transient, AC, and AC noise circuits. The components of these circuits form the basis for all element and model equations. Because these circuits represent the entire BJT during simulation, every effort has been made to demonstrate the relationship between the equivalent circuit and the element/model parameters.

The fundamental components in the equivalent circuit are the base current (ib) and the collector current (ic). For noise and AC analyses, the actual ib and ic currents are not used. Instead, the partial derivatives of ib and ic with respect to the terminal voltages vbe and vbc are used. The names for these partial derivatives are:

Reverse Base Conductance

$$g\mu = \left.\frac{\partial ib}{\partial vbc}\right|_{vbe = const.}$$

Forward Base Conductance

$$g\pi = \left.\frac{\partial ib}{\partial vbe}\right|_{vbc = const.}$$

Collector Conductance

$$g_o = \left.\frac{\partial ic}{\partial vce}\right|_{vbe = const.} = -\left.\frac{\partial ic}{\partial vbc}\right|_{vbe = const.}$$

Transconductance

$$gm = \left.\frac{\partial ic}{\partial vbe}\right|_{vce = con}$$

$$= \frac{\partial ic}{\partial vbe} + \frac{\partial ic}{\partial vbc}$$

$$= \frac{\partial ic}{\partial vbe} - g_o$$

The ib and ic equations account for all DC effects of the BJT.

Figure 4-2: Lateral Transistor, BJT Transient Analysis

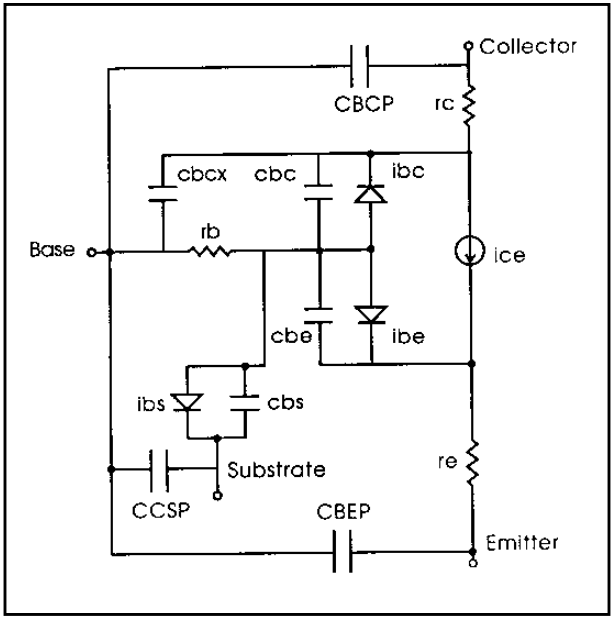


Figure 4-3: Vertical Transistor, BJT Transient Analysis

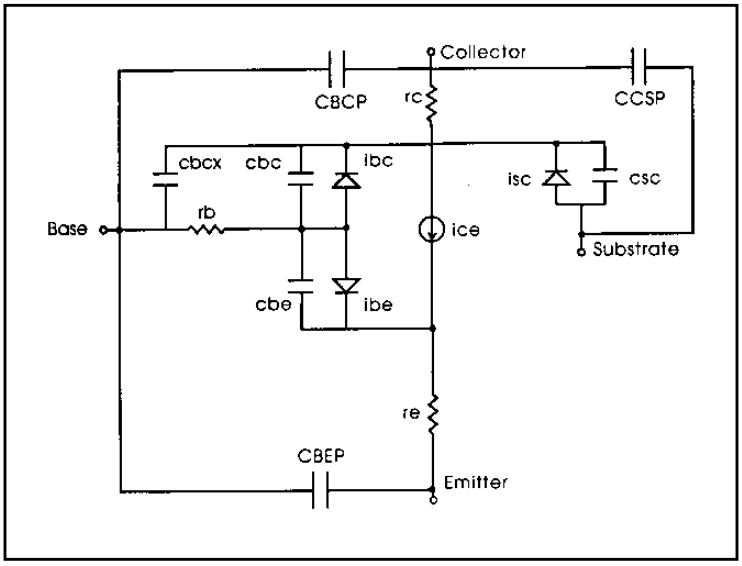


Figure 4-4: Lateral Transistor, BJT AC Analysis

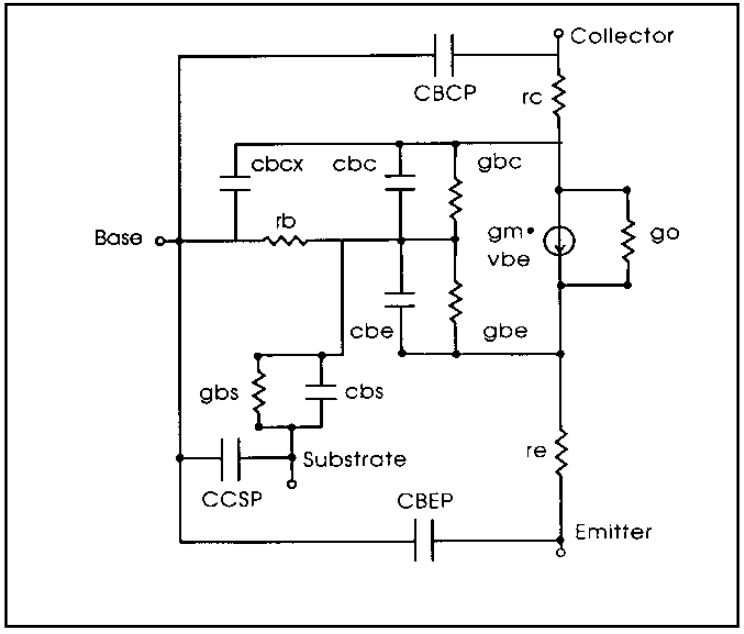


Figure 4-5: Vertical Transistor, BJT AC Analysis

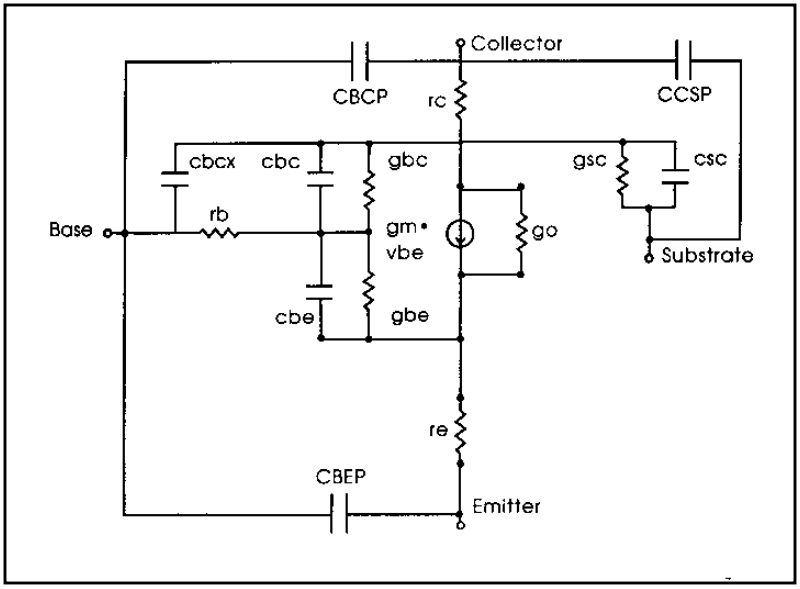


Figure 4-6: Lateral Transistor, BJT AC Noise Analysis

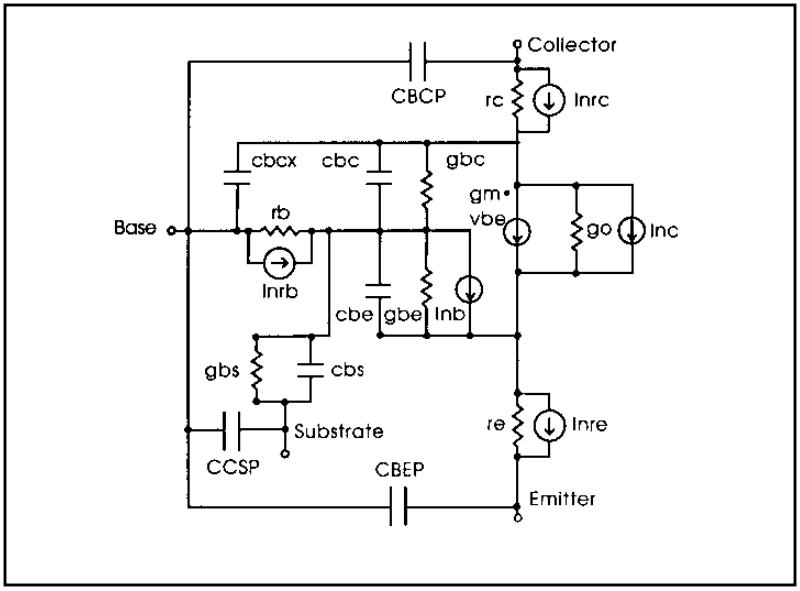


Figure 4-7: Vertical Transistor, BJT AC Noise Analysis

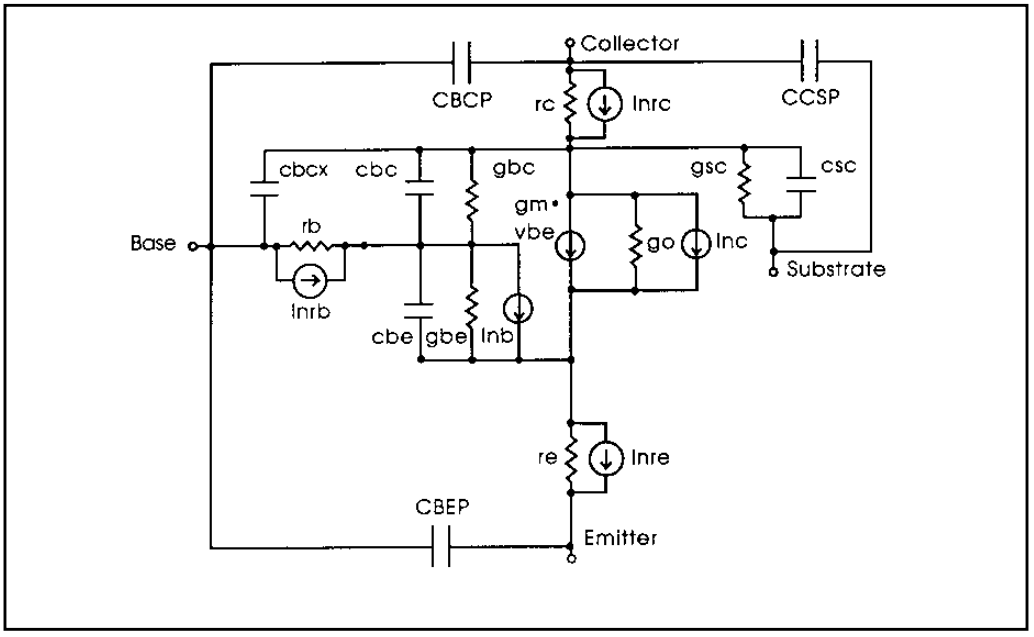


Table 4-14: Equation Variable Names

Variable	Definitions
cbc	Internal base to collector capacitance
cbcx	External base to collector capacitance
cbe	Internal base to emitter capacitance
csc	Substrate to collector capacitance (vertical transistor only)
cbs	Base to substrate capacitance (lateral transistor only)
f	Frequency
gbc	Reverse base conductance
gbe	Forward base conductance
gm	Transconductance

Table 4-14: Equation Variable Names *(Continued)*

Variable	Definitions
gsc	Substrate to collector conductance (vertical transistor only)
go	Collector conductance
gbs	Base to substrate conductance (lateral transistor only)
ib	External base terminal current
ibc	DC current base to collector
ibe	DC current base to emitter
ic	External collector terminal current
ice	DC current collector to emitter
inb	Base current equivalent noise
inc	Collector current equivalent noise
inrb	Base resistor current equivalent noise
inrc	Collector resistor equivalent noise
inre	Emitter resistor current equivalent noise
ibs	DC current base to substrate (lateral transistor only)
isc	DC current substrate to collector (vertical transistor only)
qb	Normalized base charge
rb	Base resistance
rbb	Short-circuit base resistance
vbs	Internal base substrate voltage
vsc	Internal substrate collector voltage

Table 4-15: Equation Constants

Quantities	Definitions
k	1.38062e-23 (Boltzmann's constant)
q	1.60212e-19 (electron charge)
t	temperature in °Kelvin
Δt	t - tnom
tnom	tnom = 273.15 + TNOM in °Kelvin
vt(t)	$k \cdot t/q$
vt(tmon)	$k \cdot tnom/q$

BJT Model Equations (NPN and PNP)

This section describes the NPN and PNP BJT models.

Understanding Transistor Geometry in Substrate Diodes

The substrate diode is connected to either the collector or the base depending on whether the transistor has a lateral or vertical geometry. Lateral geometry is implied when the model parameter SUBS=-1, and vertical geometry when SUBS=+1. The lateral transistor substrate diode is connected to the internal base and the vertical transistor substrate diode is connected to the internal collector. Figure 4-8 and Figure 4-9 show vertical and lateral transistor geometries.

Figure 4-8: Vertical Transistor (SUBS = +1)

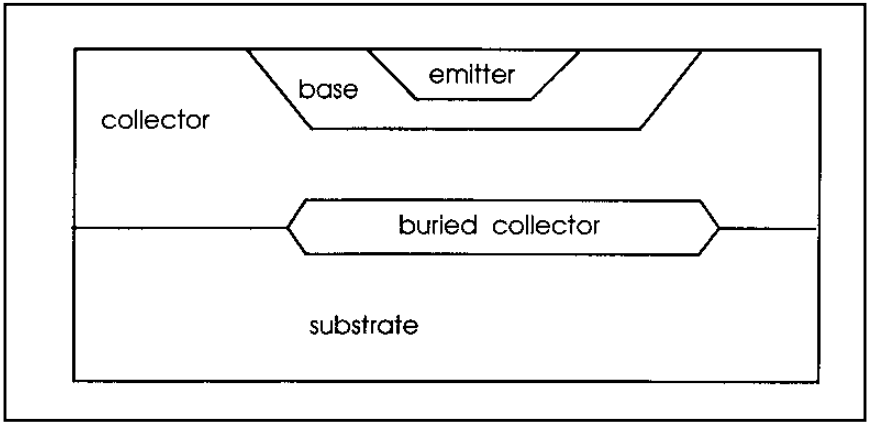
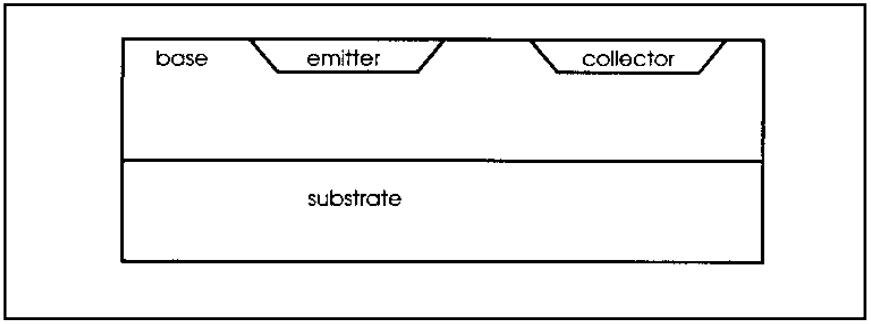
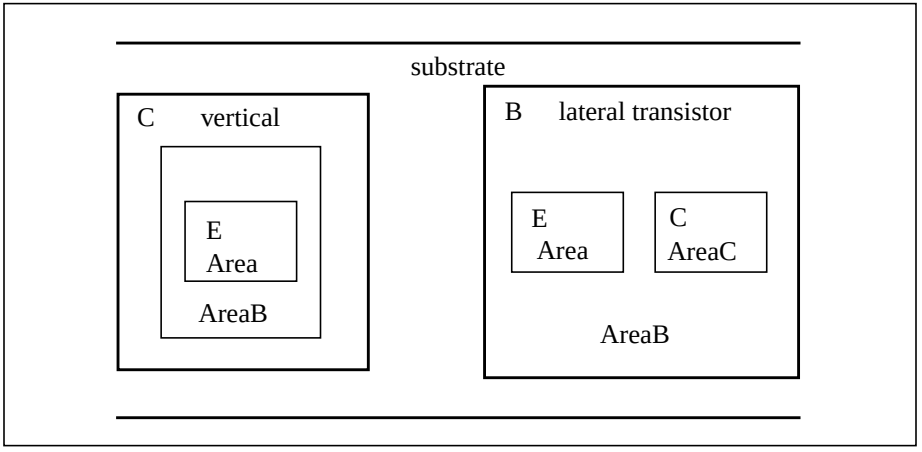


Figure 4-9: Lateral Transistor (SUBS = -1)



In Figure 4-10, the views from the top demonstrate how IBE is multiplied by either base area, AREAB, or collector area, AREAC.

Figure 4-10: Base, AREAB, Collector, AREAC



Using DC Model Equations

DC model equations are for the DC component of the collector current (ic) and the base current (ib).

Current Equations - IS Only

If only IS is specified, without IBE and IBC:

$$ic = \frac{ISeff}{qb} \cdot \left(e^{\frac{vbe}{NF \cdot vt}} - e^{\frac{vbc}{NR \cdot vt}}\right) - \frac{ISeff}{BR} \cdot \left(e^{\frac{vbc}{NR \cdot vt}} - 1\right) - ISCeff \cdot \left(e^{\frac{vbc}{NC \cdot vt}} - 1\right)$$

$$ib = \frac{ISeff}{BF} \cdot \left(e^{\frac{vbe}{NF \cdot vt}} - 1\right) + \frac{ISeff}{BR} \cdot \left(e^{\frac{vbc}{NR \cdot vt}} - 1\right) + ISEeff \cdot \left(e^{\frac{vbe}{NE \cdot vt}} - 1\right) + ISCeff \cdot \left(e^{\frac{vbc}{NC \cdot vt}} - 1\right)$$

Current Equations - IBE and IBC

If IBE and IBC are specified, instead of IS:

$$c = \frac{IBEeff}{qb} \cdot \left(e^{\frac{vbe}{NF \cdot vt}} - 1\right) - \frac{IBCeff}{qb} \cdot \left(e^{\frac{vbc}{NR \cdot vt}} - 1\right) - \frac{IBCeff}{BR} \cdot \left(e^{\frac{vbc}{NR \cdot vt}} - 1\right) - ISCeff \cdot \left(e^{\frac{vbc}{NC \cdot vt}} - 1\right)$$

$$b = \frac{IBEeff}{BF} \cdot \left(e^{\frac{vbe}{NF \cdot vt}} - 1\right) + \frac{IBCeff}{BR} \cdot \left(e^{\frac{vbc}{NR \cdot vt}} - 1\right) + ISEeff \cdot \left(e^{\frac{vbe}{NE \cdot vt}} - 1\right)$$

$$+ ISCeff \cdot \left(e^{\frac{vbc}{NC \cdot vt}} - 1\right)$$

$$IBCeff = IBC \cdot AREAB \cdot M \quad \textit{Vertical}$$

$$IBCeff = IBC \cdot AREAC \cdot M \quad \textit{Lateral}$$

$$IBEeff = IBE \cdot AREA \cdot M \quad \textit{Vertical or Lateral}$$

$$ISCeff = ISC \cdot AREAB \cdot M \quad \textit{Vertical}$$

$$ISCeff = ISC \cdot AREAC \cdot M \quad \textit{Lateral}$$

$$ISEeff = ISE \cdot AREA \cdot M \quad \textit{Vertical or Lateral}$$

The last two terms in the expression of the base current represent the components due to recombination in the base-emitter and base collector space charge regions at low injection.

Using Substrate Current Equations

The substrate current is substrate to collector for vertical transistors and substrate to base for lateral transistors.

Vertical Transistors

$$isc = ISSeff \cdot \left(e^{\frac{vsc}{NS \cdot vt}} - 1\right) \quad vsc > -10 \cdot NS \cdot vt$$

$$isc = -ISSeff \quad vsc \leq -10 \cdot NS \cdot vt$$

Lateral Transistors

$$ibs = ISSeff \cdot \left(e^{\frac{vbs}{NS \cdot vt}} - 1 \right) \quad vbs > -10 \cdot NS \cdot vt$$

$$ibs = -ISSeff \quad vbs \leq -10 \cdot NS \cdot vt$$

If both IBE and IBC are *not* specified:

$$ISSeff = ISS \cdot AREA \cdot M$$

If both IBE and IBC are specified:

$$ISSeff = ISS \cdot AREAC \cdot M \quad \textit{vertical}$$

$$ISSeff = ISS \cdot AREAB \cdot M \quad \textit{lateral}$$

Using Base Charge Equations

VAF and VAR are, respectively, forward and reverse early voltages. IKF and IKR determine the high-current Beta roll-off. ISE, ISC, NE, and NC determine the low-current Beta roll-off with ic.

If UPDATE=0 or $\frac{vbc}{VAF} + \frac{vbe}{VAR} < 0$, then

$$q1 = \frac{1}{\left(1 - \frac{vbc}{VAF} - \frac{vbe}{VAR}\right)}$$

Otherwise, if UPDATE=1 and $\frac{vbc}{VAF} + \frac{vbe}{VAR} \geq 0$, then

$$q1 = 1 + \frac{vbc}{VAF} + \frac{vbe}{VAR}$$

$$q2 = \frac{ISEeff}{IKFeff} \cdot \left(e^{\frac{vbe}{NF \cdot vt}} - 1\right) + \frac{ISCeff}{IKReff} \cdot \left(e^{\frac{vbc}{NR \cdot vt}} - 1\right)$$

$$qb = \frac{q1}{2} \cdot [1 + (1 + 4 \cdot q2)^{NKF}]$$

Using Variable Base Resistance Equations

A variable base resistance BJT model consists of a low-current maximum resistance (set using RB), and a high-current minimum resistance (set using RBM). IRB is the current when the base resistance is halfway to its minimum value. If RBM is not specified, it is set to RB.

If IRB is not specified:

$$rbb = RBMeff + \frac{RBeff - RBMeff}{qb}$$

If IRB is specified:

$$rbb = RBMeff + 3 \cdot (RBeff - RBMeff) \cdot \frac{\tan(z) - z}{z \cdot \tan(z) \cdot \tan(z)}$$

$$z = \frac{-1 + [1 + 144 \cdot ib / (\pi^2 \cdot IRBeff)]^{1/2}}{\frac{24}{\pi^2} \cdot \left(\frac{ib}{IRBeff}\right)^{1/2}}$$

Using BJT Capacitance Equations

This section describes BJT capacitances.

Using Base-Emitter Capacitance Equations

The base-emitter capacitance contains a complex diffusion term with the standard depletion capacitance formula. The diffusion capacitance is modified by model parameters TF, XTF, ITF, and VTF.

Determine the base-emitter capacitance cbe by the following formula:

$$\mathrm{cbe} = \mathrm{cbediff} + \mathrm{cbedep}$$

where *cbediff* and *cbedep* are the base-emitter diffusion and depletion capacitances, respectively.

Note: When you run a DC sweep on a BJT, use .OPTIONS DCCAP to force the evaluation of the voltage-variable capacitances during the DC sweep.

Determining Base-Emitter Diffusion Capacitance

Determine diffusion capacitance as follows:

ibe ≤ 0

$$\mathrm{cbediff} = \frac{\partial}{\partial \mathrm{vbe}}\left(\mathrm{TF} \cdot \frac{\mathrm{ibe}}{\mathrm{qb}}\right)$$

ibe > 0

$$\mathrm{cbediff} = \frac{\partial}{\partial \mathrm{vbe}}\left[\mathrm{TF} \cdot (1 + \mathrm{argtf}) \cdot \frac{\mathrm{ibe}}{\mathrm{qb}}\right]$$

where:

$$\text{argtf} = \text{XTF} \cdot \left(\frac{\text{ibe}}{\text{ibe} + \text{ITF}}\right)^2 \cdot e^{\frac{\text{vbc}}{1.44 \cdot \text{VTF}}}$$

The forward part of the collector-emitter branch current is determined as follows:

$$\text{ibe} = \text{ISeff} \cdot \left(e^{\frac{\text{vbe}}{\text{NF} \cdot \text{vt}}} - 1\right)$$

Determining Base-Emitter Depletion Capacitance

There are two different equations for modeling the depletion capacitance. Select the proper equation by specifying option DCAP in an OPTIONS statement.

DCAP=1

The base-emitter depletion capacitance is determined as follows:

vbe < FC · VJE

$$\text{cbedep} = \text{CJEeff} \cdot \left(1 - \frac{\text{vbe}}{\text{VJE}}\right)^{-\text{MJE}}$$

vbe ≥ FC · VJE

$$\text{cbedep} = \text{CJEeff} \cdot \frac{1 - \text{FC} \cdot (1 + \text{MJE}) + \text{MJE} \cdot \frac{\text{vbe}}{\text{VJE}}}{(1 - \text{FC})^{(1 + \text{MJE})}}$$

DCAP=2

The base-emitter depletion capacitance is determined as follows:

vbe < 0

$$\text{cbedep} = \text{CJEeff} \cdot \left(1 - \frac{\text{vbe}}{\text{VJE}}\right)^{-\text{MJE}}$$

vbe ≥ 0

$$\text{cbedep} = \text{CJEeff} \cdot \left(1 + \text{MJE} \cdot \frac{\text{vbe}}{\text{VJE}}\right)$$

DCAP=3

Limits peak depletion capacitance to FC · CJCeff or FC · CJEeff, with proper fall-off when forward bias exceeds PB (FC ≥ 1).

Determining Base Collector Capacitance

Determine the base collector capacitance cbc as follows:

$$\text{cbc} = \text{cbcdiff} + \text{cbcdep}$$

where *cbcdiff* and *cbcdep* are the base-collector diffusion and depletion capacitances, respectively.

Determining Base Collector Diffusion Capacitance

$$\text{cbcdiff} = \frac{\partial}{\partial \text{vbc}}(\text{TR} \cdot \text{ibc})$$

where the internal base-collector current ibc is:

$$\text{ibc} = \text{ISeff} \cdot \left(e^{\frac{\text{vbc}}{\text{NR} \cdot \text{vt}}} - 1\right)$$

Determining Base Collector Depletion Capacitance

There are two different equations for modeling the depletion capacitance. Select the proper equation by specifying option DCAP in an .OPTIONS statement.

DCAP=1

Specify DCAP=1 to select one of the following equations:

vbc < FC · VJC

$$cbcdep = XCJC \cdot CJCeff \cdot \left(1 - \frac{vbc}{VJC}\right)^{-MJC}$$

vbc ≥ FC · VJC

$$cbcdep = XCJC \cdot CJCeff \cdot \frac{1 - FC \cdot (1 + MJC) + MJC \cdot \frac{vbc}{VJC}}{(1 - FC)^{(1 + MJC)}}$$

DCAP=2

Specify DCAP=2 to select one of the following equations:

vbc < 0

$$cbcdep = XCJC \cdot CJCeff \cdot \left(1 - \frac{vbc}{VJC}\right)^{-MJC}$$

vbc ≥ 0

$$cbcdep = XCJC \cdot CJCeff \cdot \left(1 + MJC \cdot \frac{vbc}{VJC}\right)$$

External Base — Internal Collector Junction Capacitance

The base-collector capacitance is modeled as a distributed capacitance when the model parameter XCJC is set. Since the default setting of XCJC is one, the entire base-collector capacitance is on the internal base node cbc.

DCAP=1

Specify DCAP=1 to select one of the following equations:

vbcx < FC · VJC

$$cbcx = CJCeff \cdot (1 - XCJC) \cdot \left(1 - \frac{vbcx}{VJC}\right)^{-MJC}$$

vbcx ≥ FC · VJC

$$cbcx = CJCeff \cdot (1 - XCJC) \cdot \frac{1 - FC \cdot (1 + MJC) + MJC \cdot \frac{vbcx}{VJC}}{(1 - FC)^{(1 + MJC)}}$$

DCAP=2

Specify DCAP=2 to select one of the following equations:

vbcx < 0

$$cbcx = CJCeff \cdot (1 - XCJC) \cdot \left(1 - \frac{vbcx}{VJC}\right)^{-MJC}$$

vbcx ≥ 0

$$cbcx = CJCeff \cdot (1 - XCJC) \cdot \left(1 + MJC \cdot \frac{vbcx}{VJC}\right)$$

where *vbcx* is the voltage between the external base node and the internal collector node.

Using Substrate Capacitance

The function of substrate capacitance is similar to that of the substrate diode. Switch it from the collector to the base by setting the model parameter, SUBS.

Using Substrate Capacitance Equation — Lateral

Base to Substrate Diode

Reverse Bias vbs < 0

$$cbs = CJSeff \cdot \left(1 - \frac{vbs}{VJS}\right)^{-MJS}$$

Forward Bias vbs ≥ 0

$$cbs = CJSeff \cdot \left(1 + MJS \cdot \frac{vbs}{VJS}\right)$$

Using Substrate Capacitance Equation — Vertical

Substrate to Collector Diode

Reverse Bias vsc < 0

$$csc = CJSeff \cdot \left(1 - \frac{vsc}{VJS}\right)^{-MJS}$$

Forward Bias vsc ≥ 0

$$csc = CJSeff \cdot \left(1 + MJS \cdot \frac{vsc}{VJS}\right)$$

Using Excess Phase Equation

The model parameter, PTF, models excess phase. It is defined as extra degrees of phase delay (introduced by the BJT) at any frequency and is determined by the equation:

$$excess\ phase = \left(2 \cdot \pi \cdot PTF \cdot \frac{TF}{360}\right) \cdot (2 \cdot \pi \cdot f)$$

where f is in Hertz, and you can set PTF and TF. The excess phase is a delay (linear phase) in the transconductance generator for AC analysis. Use it also in transient analysis.

Defining BJT Noise Equations

Equations for modeling BJT thermal, shot, and flicker noise are as follows.

Defining Noise Equations

The mean square short-circuit base resistance noise current equation is:

$$\mathrm{inrb} = \left(\frac{4 \cdot k \cdot t}{rbb}\right)^{1/2}$$

The mean square short-circuit collector resistance noise current equation is:

$$\mathrm{inrc} = \left(\frac{4 \cdot k \cdot t}{RCeff}\right)^{1/2}$$

The mean square short-circuit emitter resistance noise current equation is:

$$\mathrm{inre} = \left(\frac{4 \cdot k \cdot t}{REeff}\right)^{1/2}$$

The noise associated with the base current is composed of two parts: shot noise and flicker noise. Typical values for the flicker noise coefficient, KF, are 1e-17 to 1e-12. They are calculated as:

$$2 \cdot q \cdot fknee$$

where fknee is noise knee frequency (typically 100 Hz to 10 MHz) and q is electron charge.

$$\mathrm{inb}^2 = (2 \cdot q \cdot ib) + \left(\frac{KF \cdot ib^{AF}}{f}\right)$$

$$\mathrm{inb}^2 = shot\ \ noise^2 + flicker\ \ noise^2$$

$$shot\ \ noise = (2 \cdot q \cdot ib)^{1/2}$$

$$flicker\ \ noise\ = \left(\frac{\mathrm{KF}\cdot \mathrm{ib}^{\mathrm{AF}}}{\mathrm{f}}\right)^{1/2}$$

The noise associated with the collector current is modeled as shot noise only.

$$\mathrm{inc}\ = (2\cdot \mathrm{q}\cdot \mathrm{ic})^{1/2}$$

Noise Summary Printout Definitions

RB, V^2/Hz	output thermal noise due to base resistor
RC, V^2/Hz	output thermal noise due to collector resistor
RE, V^2/Hz	output thermal noise due to emitter resistor
IB, V^2/Hz	output shot noise due to base current
FN, V^2/Hz	output flicker noise due to base current
IC, V^2/Hz	output shot noise due to collector current
TOT, V^2/Hz	total output noise: *TOT= RB + RC + RE + IB + IC + FN*

BJT Temperature Compensation Equations

This section describes how to use temperature compensation equations.

Using Energy Gap Temperature Equations

To determine energy gap for temperature compensation, use the equations:

TLEV = 0, 1 or 3

$$egnom = 1.16 - 7.02e{-}4 \cdot \frac{tnom^2}{tnom + 1108.0}$$

$$eg(t) = 1.16 - 7.02e{-}4 \cdot \frac{t^2}{t + 1108.0}$$

TLEV=2

$$egnom = EG - GAP1 \cdot \frac{tnom^2}{tnom + GAP2}$$

$$eg(t) = EG - GAP1 \cdot \frac{t^2}{t + GAP2}$$

Saturation and Beta Temperature Equations, TLEV=0 or 2

The basic BJT temperature compensation equations for beta and the saturation currents when TLEV=0 or 2 (default is TLEV=0):

$$BF(t) = BF \cdot \left(\frac{t}{tnom}\right)^{XTB}$$

$$BR(t) = BR \cdot \left(\frac{t}{tnom}\right)^{XTB}$$

$$ISE(t) = \frac{ISE}{\left(\frac{t}{tnom}\right)^{XTB}} \cdot e^{\frac{facln}{NE}}$$

$$ISC(t) = \frac{ISC}{\left(\frac{t}{tnom}\right)^{XTB}} \cdot e^{\frac{facln}{NC}}$$

$$ISS(t) = \frac{ISS}{\left(\frac{t}{tnom}\right)^{XTB}} \cdot e^{\frac{facln}{NS}}$$

The parameter XTB usually should be set to zero for TLEV=2.

$$IS(t) = IS \cdot e^{facln}$$

$$IBE(t) = IBE \cdot e^{\frac{facln}{NF}}$$

$$IBC(t) = IBC \cdot e^{\frac{facln}{NR}}$$

TLEV=0, 1 or 3

$$facln = \frac{EG}{vt(tnom)} - \frac{EG}{vt(t)} + XTI \cdot \ln\left(\frac{t}{tnom}\right)$$

TLEV=2

$$facln = \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)} + XTI \cdot \ln\left(\frac{t}{tnom}\right)$$

Using Saturation and Temperature Equations, TLEV=1

The basic BJT temperature compensation equations for beta and the saturation currents when TLEV=1:

$$BF(t) = BF \cdot (1 + XTB \cdot \Delta t)$$

$$BR(t) = BR \cdot (1 + XTB \cdot \Delta t)$$

$$ISE(t) = \frac{ISE}{1 + XTB \cdot \Delta t} \cdot e^{\frac{facln}{NE}}$$

$$ISC(t) = \frac{ISC}{1 + XTB \cdot \Delta t} \cdot e^{\frac{facln}{NC}}$$

$$ISS(t) = \frac{ISS}{1 + XTB \cdot \Delta t} \cdot e^{\frac{facln}{NS}}$$

$$IS(t) = IS \cdot e^{facln}$$

$$IBE(t) = IBE \cdot e^{\frac{facln}{NF}}$$

$$IBC(t) = IBC \cdot e^{\frac{facln}{NR}}$$

where:

$$facln = \frac{EG}{vt(tnom)} - \frac{EG}{vt(t)} + XTI \cdot \ln\left(\frac{t}{tnom}\right)$$

TLEV=0, 1, 2

The parameters IKF, IKR, and IRB are also modified as:

$$IKF(t) = IKF \cdot (1 + TIKF1 \cdot \Delta t + TIKF2 \cdot \Delta t^2)$$

$$IKR(t) = IKR \cdot (1 + TIKR1 \cdot \Delta t + TIKR2 \cdot \Delta t^2)$$

$$IRB(t) = IRB \cdot (1 + TIRB1 \cdot \Delta t + TIRB2 \cdot \Delta t^2)$$

Using Saturation Temperature Equations, TLEV=3

The basic BJT temperature compensation equations for the saturation currents when TLEV=3

$$IS(t) = IS^{(1 + TIS1 \cdot \Delta t + TIS2 \cdot \Delta t^2)}$$

$$IBE(t) = IBE^{(1 + TIS1 \cdot \Delta t + TIS2 \cdot \Delta t^2)}$$

$$IBC(t) = IBC^{(1 + TIS1 \cdot \Delta t + TIS2 \cdot \Delta t^2)}$$

$$ISE(t) = ISE^{(1 + TISE1 \cdot \Delta t + TISE2 \cdot \Delta t^2)}$$

$$ISC(t) = ISC^{(1 + TISC1 \cdot \Delta t + TISC2 \cdot \Delta t^2)}$$

$$ISS(t) = ISS^{(1 + TISS1 \cdot \Delta t + TISS2 \cdot \Delta t^2)}$$

The parameters IKF, IKR, and IRB are also modified as:

$$IKF(t) = IKF^{(1 + TIKF1 \cdot \Delta t + TIKF2 \cdot \Delta t^2)}$$

$$IKR(t) = IKR^{(1 + TIKR1 \cdot \Delta t + TIKR2 \cdot \Delta t^2)}$$

$$IRB(t) = IRB^{(1 + TIRB1 \cdot \Delta t + TIRB2 \cdot \Delta t^2)}$$

The following parameters are also modified when corresponding temperature coefficients are specified, regardless of the TLEV value.

$$BF(t) = BF \cdot (1 + TBF1 \cdot \Delta t + TBF2 \cdot \Delta t^2)$$

$$BR(t) = BR \cdot (1 + TBR1 \cdot \Delta t + TBR2 \cdot \Delta t^2)$$

$$VAF(t) = VAF \cdot (1 + TVAF1 \cdot \Delta t + TVAF2 \cdot \Delta t^2)$$

$$VAR(t) = VAR \cdot (1 + TVAR1 \cdot \Delta t + TVAR2 \cdot \Delta t^2$$

$$ITF(t) = ITF \cdot (1 + TITF1 \cdot \Delta t + TITF2 \cdot \Delta t^2)$$

$$TF(t) = TF \cdot (1 + TTF1 \cdot \Delta t + TTF2 \cdot \Delta t^2)$$

$$TR(t) = TR \cdot (1 + TTR1 \cdot \Delta t + TTR2 \cdot \Delta t^2)$$

$$NF(t) = NF \cdot (1 + TNF1 \cdot \Delta t + TNF2 \cdot \Delta t^2)$$

$$NR(t) = NR \cdot (1 + TNR1 \cdot \Delta t + TNR2 \cdot \Delta t^2)$$

$$NE(t) = NE \cdot (1 + TNE1 \cdot \Delta t + TNE2 \cdot \Delta t^2)$$

$$NC(t) = NC \cdot (1 + TNC1 \cdot \Delta t + TNC2 \cdot \Delta t^2)$$

$$NS(t) = NS \cdot (1 + TNS1 \cdot \Delta t + TNS2 \cdot \Delta t^2)$$

$$MJE(t) = MJE \cdot (1 + TMJE1 \cdot \Delta t + TMJE2 \cdot \Delta t^2)$$

$$MJC(t) = MJC \cdot (1 + TMJC1 \cdot \Delta t + TMJC2 \cdot \Delta t^2)$$

$$MJS(t) = MJS \cdot (1 + TMJS1 \cdot \Delta t + TMJS2 \cdot \Delta t^2)$$

Using Capacitance Temperature Equations

TLEVC=0

$$CJE(t) = CJE \cdot \left[1 + MJE \cdot \left(4.0e{-}4 \cdot \Delta t - \frac{VJE(t)}{VJE} + 1\right)\right]$$

$$CJC(t) = CJC \cdot \left[1 + MJC \cdot \left(4.0e{-}4 \cdot \Delta t - \frac{VJC(t)}{VJC} + 1\right)\right]$$

$$CJS(t) = CJS \cdot \left[1 + MJS \cdot \left(4.0e{-}4 \cdot \Delta t - \frac{VJS(t)}{VJS} + 1\right)\right]$$

where:

$$VJE(t) = VJE \cdot \frac{t}{tnom} - vt(t) \cdot \left[3 \cdot \ln\left(\frac{t}{tnom}\right) + \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)}\right]$$

$$VJC(t) = VJC \cdot \frac{t}{tnom} - vt(t) \cdot \left[3 \cdot \ln\left(\frac{t}{tnom}\right) + \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)}\right]$$

$$VJS(t) = VJS \cdot \frac{t}{tnom} - vt(t) \cdot \left[3 \cdot \ln\left(\frac{t}{tnom}\right) + \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)}\right]$$

TLEVC=1

$$CJE(t) = CJE \cdot (1 + CTE \cdot \Delta t)$$

$$CJC(t) = CJC \cdot (1 + CTC \cdot \Delta t)$$

$$CJS(t) = CJS \cdot (1 + CTS \cdot \Delta t)$$

and built-in potentials determined as:

$$VJE(t) = VJE - TVJE \cdot \Delta t$$

$$VJC(t) = VJC - TVJC \cdot \Delta t$$

$$VJS(t) = VJS - TVJS \cdot \Delta t$$

TLEVC=2

$$CJE(t) = CJE \cdot \left(\frac{VJE}{VJE(t)}\right)^{MJE}$$

$$CJC(t) = CJC \cdot \left(\frac{VJC}{VJC(t)}\right)^{MJC}$$

$$CJS(t) = CJS \cdot \left(\frac{VJS}{VJS(t)}\right)^{MJS}$$

where:

$$VJE(t) = VJE - TVJE \cdot \Delta t$$

$$VJC(t) = VJC - TVJC \cdot \Delta t$$

$$VJS(t) = VJS - TVJS \cdot \Delta t$$

TLEVC=3

$$CJE(t) = CJE \cdot \left(1 - 0.5 \cdot dvjedt \cdot \frac{\Delta t}{VJE}\right)$$

$$CJC(t) = CJC \cdot \left(1 - 0.5 \cdot dvjcdt \cdot \frac{\Delta t}{VJC}\right)$$

$$CJS(t) = CJS \cdot \left(1 - 0.5 \cdot dvjsdt \cdot \frac{\Delta t}{VJS}\right)$$

$$VJE(t) = VJE + dvjedt \cdot \Delta t$$

$$VJC(t) = VJC + dvjcdt \cdot \Delta t$$

$$VJS(t) = VJS + dvjsdt \cdot \Delta t$$

where TLEV= 0, 1, or 3

$$dvjedt = -\frac{egnom + 3 \cdot vt(tnom) + (1.16 - egnom) \cdot \left(2 - \frac{tnom}{tnom + 1108}\right) - VJE}{tnom}$$

$$dvjcdt = -\frac{egnom + 3 \cdot vt(tnom) + (1.16 - egnom) \cdot \left(2 - \frac{tnom}{tnom + 1108}\right) - VJC}{tnom}$$

$$dvjsdt = -\frac{egnom + 3 \cdot vt(tnom) + (1.16 - egnom) \cdot \left(2 - \frac{tnom}{tnom + 1108}\right) - VJS}{tnom}$$

and TLEV=2

$$dvjedt = -\frac{egnom + 3 \cdot vt(tnom) + (EG - egnom) \cdot \left(2 - \frac{tnom}{tnom + GAP2}\right) - VJE}{tnom}$$

$$dvjcdt = -\frac{egnom + 3 \cdot vt(tnom) + (EG - egnom) \cdot \left(2 - \frac{tnom}{tnom + GAP2}\right) - VJC}{tnom}$$

$$dvjsdt = -\frac{egnom + 3 \cdot vt(tnom) + (EG - egnom) \cdot \left(2 - \frac{tnom}{tnom + GAP2}\right) - VJS}{tnom}$$

Parasitic Resistor Temperature Equations

The parasitic resistors, as a function of temperature regardless of TLEV value, are determined as:

$$RE(t) = RE \cdot (1 + TRE1 \cdot \Delta t + TRE2 \cdot \Delta t^2)$$

$$RB(t) = RB \cdot (1 + TRB1 \cdot \Delta t + TRB2 \cdot \Delta t^2)$$

$$RBM(t) = RBM \cdot (1 + TRM1 \cdot \Delta t + TRM2 \cdot \Delta t^2)$$

$$RC(t) = RC \cdot (1 + TRC1 \cdot \Delta t + TRC2 \cdot \Delta t^2)$$

Using BJT Level=2 Temperature Equations

The model parameters of BJT Level 2 model are modified for temperature compensation as:

$$GAMMA(t) = GAMMA \cdot e^{(facln)}$$

$$RC(t) = RC \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$VO(t) = VO \cdot \left(\frac{t}{tnom}\right)^{BEXV}$$

BJT Quasi-Saturation Model

Use the BJT quasi-saturation model (Level=2), an extension of the Gummel-Poon model (Level 1 model), to model bipolar junction transistors that exhibit quasi-saturation or base push-out effects. When a device with lightly doped collector regions operates at high injection levels, the internal base-collector junction is forward biased, while the external base-collector junction is reversed biased; DC current gain and the unity gain frequency fT falls sharply. Such an operation regime is referred to as quasi-saturation, and its effects have been included in this model.

Figure 4-11 show the additional elements of the Level 2 model. The current source *Iepi* and charge storage elements *Ci* and *Cx* model the quasi-saturation effects. The parasitic substrate bipolar transistor is also included in the vertical transistor by the diode D and current source *Ibs*.

Figure 4-11: Vertical npn Bipolar Transistor (SUBS=+1)

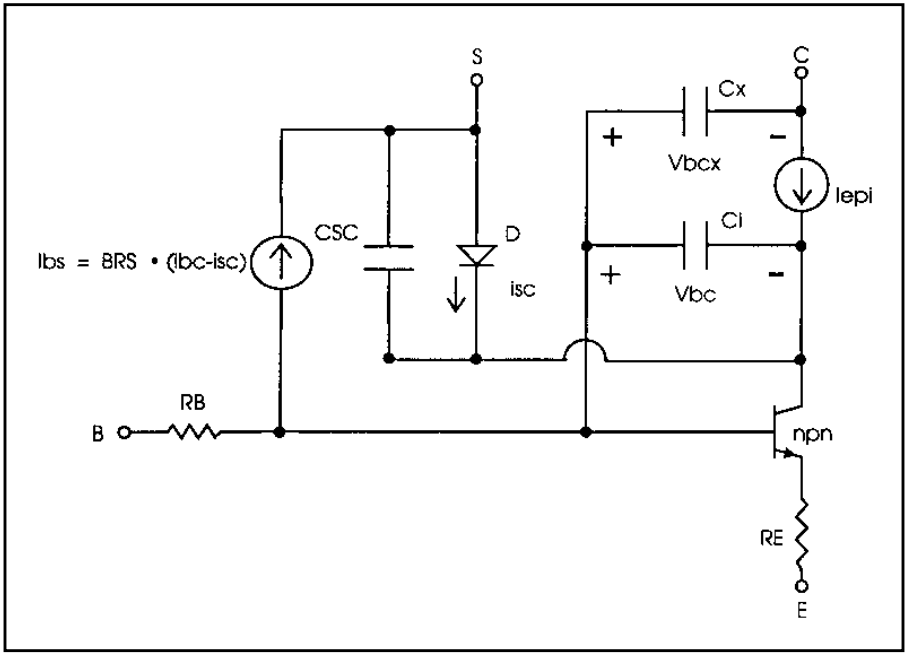
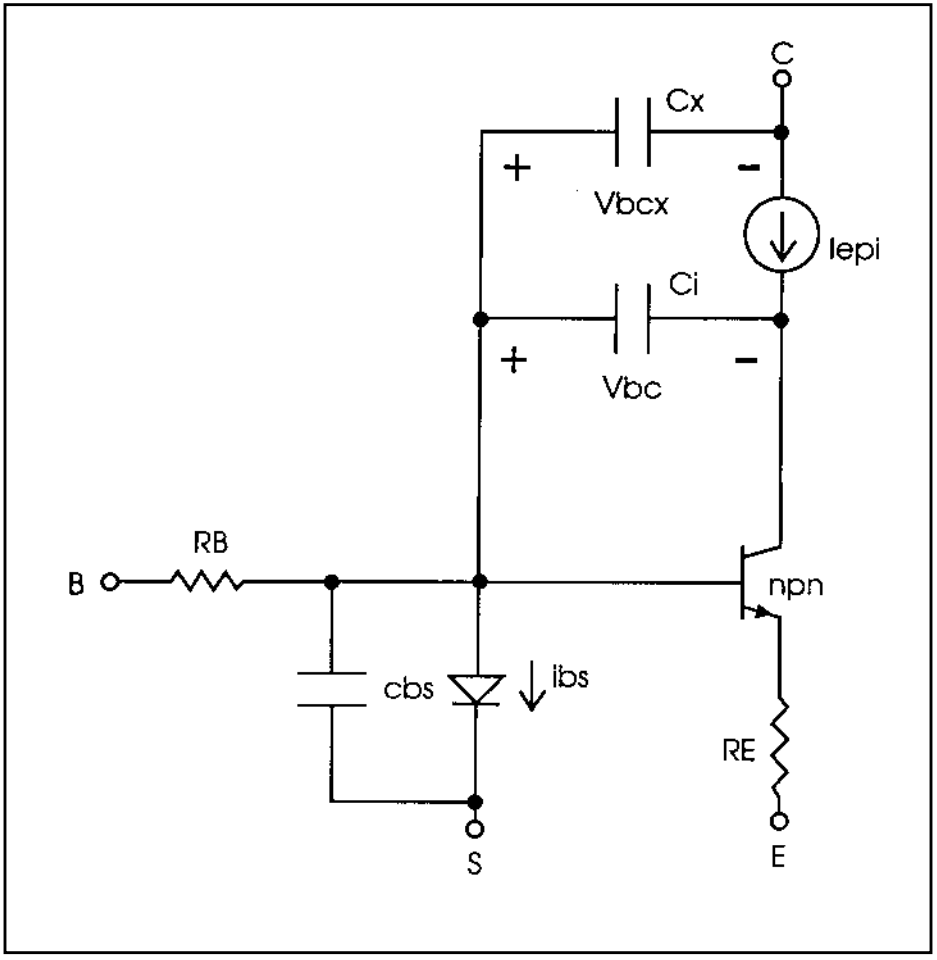


Figure 4-12: Lateral npn Bipolar Transistor (SUBS=-1)



Using Epitaxial Current Source Iepi

The epitaxial current value, Iepi, is determined by the equation:

$$Iepi = \frac{ki - kx - \ln\left(\frac{1+ki}{1+kx}\right) + \frac{vbc - vbcx}{NEPI \cdot vt}}{\left(\frac{RCeff}{NEPI \cdot vt}\right) \cdot \left(1 + \frac{|vbc - vbcx|}{VO}\right)}$$

where:

$$ki = [1 + GAMMA \cdot e^{vbc/(NEPI \cdot vt)}]^{1/2}$$

$$kx = [1 + GAMMA \cdot e^{vbcx/(NEPI \cdot vt)}]^{1/2}$$

In special cases when the model parameter GAMMA is set to zero, ki and kx become one and,

$$Iepi = \frac{vbc - vbcx}{RCeff \cdot \left(1 + \frac{|vbc - vbcx|}{VO}\right)}$$

Epitaxial Charge Storage Elements Ci and Cx

The epitaxial charges are determined by:

$$qi = QCOeff \cdot \left(ki - 1 - \frac{GAMMA}{2}\right)$$

and:

$$qx = QCOeff \cdot \left(kx - 1 - \frac{GAMMA}{2}\right)$$

The corresponding capacitances are calculated as:

$$Ci = \frac{\partial}{\partial vbc}(qi) = \left(\frac{GAMMA \cdot QCOeff}{2 \cdot NEPI \cdot vt \cdot kx}\right) \cdot e^{vbc/(NEPI \cdot vt)}$$

and:

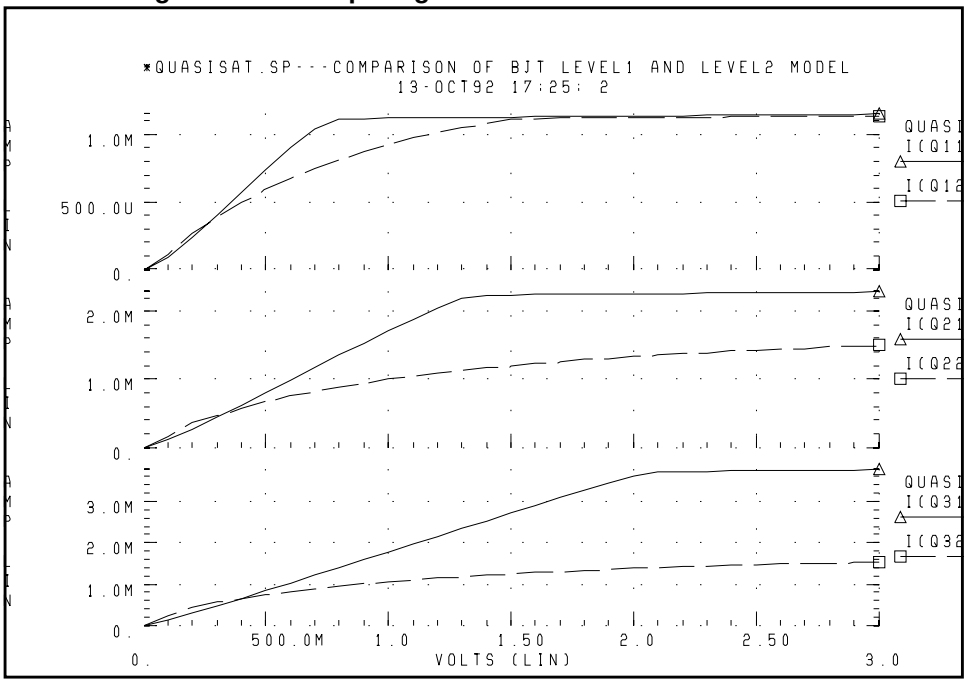
$$Cx = \frac{\partial}{\partial vbcx}(qx) = \left(\frac{GAMMA \cdot QCOeff}{2 \cdot NEPI \cdot vt \cdot kx}\right) \cdot e^{vbcx/(NEPI \cdot vt)}$$

In the special case where GAMMA=0 the Ci and Cx become zero.

Example

```
*quasisat.sp comparison of bjt Level1 and Level2
*model
.options nomod relv=.001 reli=.001 absv=.1u absi=1p
.options post
q11 10 11 0 mod1
q12 10 12 0 mod2
q21 10 21 0 mod1
q22 10 22 0 mod2
q31 10 31 0 mod1
q32 10 32 0 mod2
vcc 10 0 .7
i11 0 11 15u
i12 0 12 15u
i21 0 21 30u
i22 0 22 30u
i31 0 31 50u
i32 0 32 50u
.dc vcc 0 3 .1
.print dc vce=par('v(10)') i(q11) i(q12) i(q21)
+ i(q22) i(q31) i(q32)
*.graph dc i(q11) i(q12) i(q21) i(q22)
*.graph dc i(q11) i(q12)
.MODEL MOD1 NPn IS=4.0E-16 BF=75 VAF=75
+ Level=1 rc=500 SUBS=+1
.MODEL MOD2 NPn IS=4.0E-16 BF=75 VAF=75
+ Level=2 rc=500 vo=1 qco=1e-10
+ gamma=1e-9 SUBS=+1
.end
```

Figure 4-13: Comparing BJT Level 1 and Level 2 Models



Converting National Semiconductor Models

National Semiconductor's SNAP circuit simulator has a scaled BJT model that is not the same as the Avant! BJT models. To use this model, make the following changes.

For a subcircuit that consists of the scaled BJT model, the subcircuit name must be the same as the name of the model. Inside the subcircuit there is a .PARAM statement that specifies the scaled BJT model parameter values. Put a scaled BJT model inside the subcircuit, then change the ".MODEL mname mtype" statement to a .PARAM statement. Ensure that each parameter in the .MODEL statement within the subcircuit has a value in the .PARAM statement.

Defining Scaled BJT Subcircuits

The following subcircuit definition converts the National Semiconductor scaled BJT model to a form usable in Avant! in-circuit simulators. The .PARAM parameter inside the .SUBCKT represents the .MODEL parameter in the National circuit simulator. Therefore, replace the ".MODEL mname" statement with a .PARAM statement. Change the model name to SBJT.

Note: All parameters used in the following model must have a value that comes either from a .PARAM statement or the subcircuit call.

Example

```
.SUBCKT SBJT NC NB NE SF=1 SCBC=1 SCBE=1 SCCS=1 SIES=1 SICS=1
+ SRB=1 SRC=1 SRE=1 SIC=0 SVCE=0 SBET=1
Q NC NB NE SBJT IC=SIC VCE=SVCE
.PARAM IES=1   10E-18         ICS=5.77E-18  NE=1.02  NC=1.03
+ ME=3.61     MC=1.24         EG=1.12       NSUB=0
+ CJE=1E-15   CJC=1E-15       CSUB=1E-15  EXE=0.501
+ EXC=0.222   ESUB=0.709      PE=1.16     PC=0.37
+ PSUB=0.698  RE=75           RC=0.0      RB=1.0
+ TRE=2E-3    TRC=6E-3        TRB=1.9E-3  VA=25
+ FTF=2.8E9   FTR=40E6        BR=1.5      TCB=5.3E-3
```

```
+ TCB2=1.6E-6  BF1=9.93       BF2=45.7    BF3=55.1
+ BF4=56.5     BF5=53.5       BF6=33.8
+ IBF1=4.8P    IBF2=1.57N     IBF3=74N
+ IBF4=3.13U   IBF5=64.2U     IBF6=516U
*

.MODEL SBJT NPN
+ IBE='IES*SF*SIES' IBC='ICS*SF*SICS'
+ CJE='CJE*SF*SCBE' CJC='CJC*SF*SCBC'
+ CJS='CSUB*SF*SCCS' RB='RB*SRB/SF'
+ RC='RC*SRC/SF' RE='RE*SRE/SF'
+ TF='1/(6.28*FTF)' TR='1/(6.28*FTR)'
+ MJE=EXE MJC=EXC
+ MJS=ESUB VJE=PE
+ VJC=PC VJS=PSUB
+ NF=NE NR=NC
+ EG=EG BR=BR VAF=VA
+ TRE1=TRE TRC1=TRC TRB1=TRB
+ TBF1=TCB TBF2=TCB2
+ BF0=BF1 IB0=IBF1
+ BF1=BF2 IB1=IBF2
+ BF2=BF3 IB2=IBF3
+ BF3=BF4 IB3=IBF4
+ BF4=BF5 IB4=IBF5
+ BF5=BF6 IB5=IBF6
+ NSUB=0 sbet=sbet
+ TLEV=1 TLEVC=1
+ XTIR='MC*NC' XTI='ME*NE'
.ENDS SBJT
```

The BJT statement is replaced by:

```
XQ1 1046 1047 8 SBJT SIES=25.5 SICS=25.5 SRC=3.92157E-2
+ SRE=3.92157E-2 SBET=3.92157E-2 SRB=4.8823E+2 SCBE=94.5234
+ SCBC=41.3745 SCCS=75.1679 SIC=1M SVCE=1
```

VBIC Bipolar Transistor Model

The VBIC (Vertical Bipolar Inter-Company) model is a bipolar transistor model. You can use VBIC by specifying parameter Level=4 for the bipolar transistor model.

VBIC addresses many problems of the Gummel-Poon model:

- More accurate modeling of Early effect
- Parasitic substrate transistor
- Modulation of collector resistance
- Avalanche multiplication in collector junction, parasitic capacitances of base-emitter overlap in double poly BJTs, and self heating.

Understanding the History of VBIC

VBIC was developed by engineers at several companies. The detailed equations[1] for all elements are given in the referenced publication. Recent information and source code can be found on the web site:

```
http://www-sm.rz.fht-esslingen.de/institute/iafgp/neu/VBIC/
index.html
```

The Avant! implementation is compliant to standard VBIC. Self-heating and excess phases have been implemented or enabled in this version 2001.4

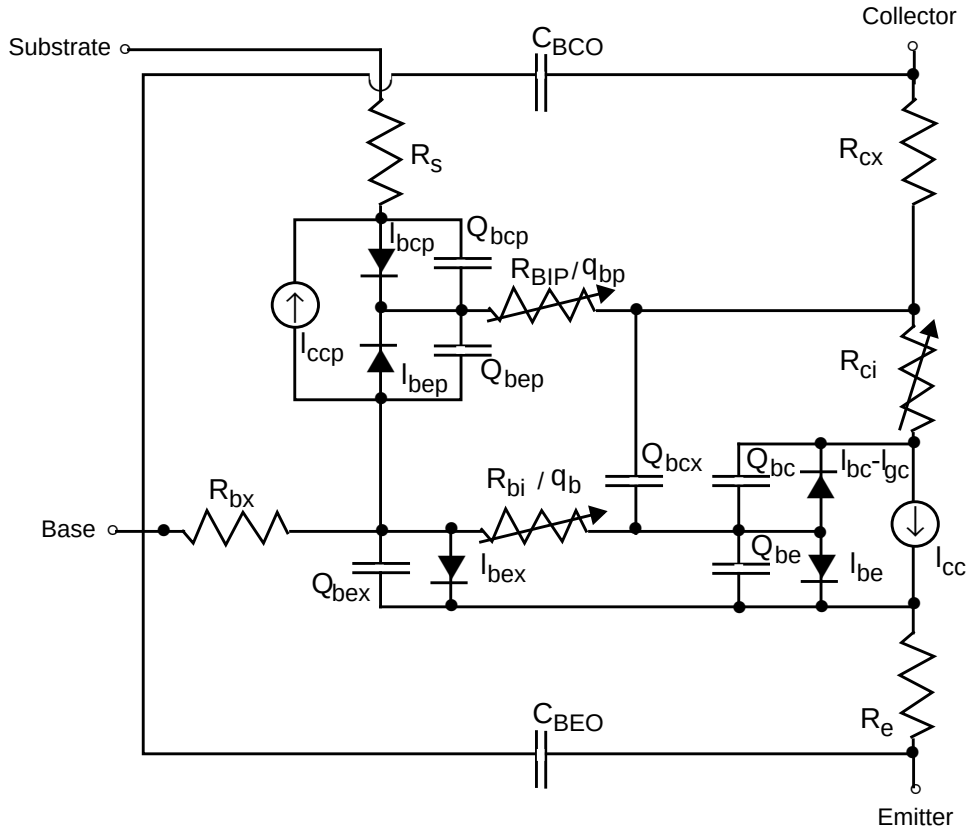
The large signal equivalent circuit for VBIC is shown in Figure 4-14. Capacitors CBCO, CBEO and resistors RCX, RBX, RE, and RS are linear elements, all other elements of the equivalent circuit are nonlinear.

[1]C. McAndrew, J. Seitchik, D. Bowers, M. Dunn, M. Foisy, I. Getreu, M. McSwain, S. Moinian, J. Parker, D. Roulston, M. Schroter, P. van Wijnen, and L. Wagner, “VBIC95: The vertical bipolar intercompany model,” *IEEE Journal of Solid State Circuits*, vol.31, p.1476-1483, 1996.

VBIC Parameters

Table 4-16 on page 4-64 lists the parameters for the model that you can set. Table 4-16 also contains the default values for the parameters. The same parameter names are used in the table and the previous referenced publication.

Figure 4-14: Transient Analysis



If values of parameters given by the user are beyond their ranges, those parameters will be reset to new values and warnings will be printed unless the option NOWARN is set.

Noise Analysis

The following sources of noise are taken into account:

- The thermal noise of resistors RBX, RCX, RE, RS, RBP, RCI, RBI
- Shot noise of currents IBE, IBEP, ICC, ICCP
- Flicker noise due to currents IBE, IBEP

The noise due to IBEX and IGC is not included in this preliminary version (nor in the standard VBIC), but will be included in the next release.

Accounting for Self-heating and excess phase

After self-heating effect is accounted for, the device element syntax becomes:

```
Qxxx nc nb ne <ns> <nT> mname <regular parameters> <tnodeout>
```

where nT is the node for temperature. If this node is given, but ns is not given, the flag “tnodeout” must be specified to indicate the fourth node is temperature node instead of substrate node. To turn on self-heating, in addition to giving the T node, the `Rth` model parameter must be not zero in the model card.

Excess phase has only effects on ac and transient characteristics analysis. To turn on this effect, the model parameter TD must be non-zero. But for transient analysis, to turn on excess phase is not recommended due to model’s convergence very sensitive to TD value.

Example

Example with no self-heating effect.

Usage:

```
Q1 21 22 22 22 VBIC <parameters>
.MODEL VBIC NPN <parameters>
```

Complete netlist:

```
*VBIC example, DC analysis
.OPTIONS NODE POST NOPAGE
.WIDTH OUT=80
.DC QVcolem 0 5 0.1 SWEEP QVbasem 0.7 0.86 0.05
.TEMP -20.0 +25. +100.
.PRINT DC I1(Q1) I2(Q1) I3(Q1) I4(Q1)
.PRINT DC V(102) V(202)
```

```
Vbas 101 0 QVbasem
Vcol 102 0 QVcolem
Vsub 104 0 0.
Vemi 103 0 0.
R1   101 201 10
R2   102 202 10
R4   104 204 10
R3   103 203 10
Q1 202 201 203 204 VBIC_EXAMPLE
.model VBIC_EXAMPLE npn Level=4
+ afn=1 ajc=-0.5 aje=0.5 ajs=0.5
+ avc1=0 avc2=0 bfn=1 cbco=0 cbeo=0 cjc=2e-14
+ cjcp=4e-13 cje=le-13 cjep=le-13 cth=0
+ ea=1.12 eaic=1.12 eaie=1.12 eais=1.12 eanc=1.12
+ eane=1.12 eans=1.12 fc=0.9 gamm=2e-11 hrcf=2
+ ibci=2e-17 ibcip=0 ibcn=5e-15 ibcnp=0
+ ibei=1e-18 ibeip=0 iben=5e-15 ibenp=0
+ ikf=2e-3 ikp=2e-4 ikr=2e-4 is=le-16 isp=le-15 itf=8e-2
+ kfn=0 mc=0.33 me=0.33 ms=0.33
+ nci=1 ncip=1 ncn=2 ncnp=2 nei=1 nen=2
+ nf=1 nfp=1 nr=1 pc=0.75 pe=0.75 ps=0.75 qco=le-12 qtf=0
+ rbi=4 rbp=4 rbx=1 rci=6 rcx=1 re=0.2 rs=2
+ rth=300 tavc=0 td=2e-11 tf=10e-12 tnf=0 tr=100e-12
+ tnom=25 tref=25 vef=10 ver=4 vo=2
+ vtf=0 wbe=1 wsp=1
+ xii=3 xin=3 xis=3 xrb=0 xrc=0 xre=0 xrs=0 xtf=20 xvo=0
*.END
```

Example with self-heating effects.

```
*# VERSION:     99.4
.option absmos=1e-12 relmos=1e-6 relv=1e-6 absv=1e-9
vc c 0 0
vb b 0 0
ve e 0 0
vs s 0 0
vc1 c1 c 0
vb1 b1 b 0
ve1 e1 e 0
vs1 s1 s 0
*vt t 0 1meg
.temp 27
Q1 c1 b1 e1 s1 t mod1 area=1 tnodeout
```

```
.model mod1 npn Level=4
+ Tnom=27 RCX=10 RCI=60 VO=2 GAMM=2.e-11
+ HRCF=2 RBX=10 RBI=40 RE=2
+ RS=20 RBP=40 IS=1e-16 NF=1.00000e+00
+ NR=1.00000e+00 FC=9.00000e-01 CBEO=0
+ CJE=1.e-13 PE=0.75 ME=0.33
+ AJE=-5.00000e-01 CBCO=0 CJC=2e-14
+ QCO=1e-12 CJEP=1e-13 PC=7.50000e-01
+ MC=3.30000e-01 AJC=-5.00000e-01 CJCP=4e-13
+ PS=7.50000e-01 MS=3.30000e-01 AJS=-5.00000e-01
+ IBEI=1e-18 WBE=1.0000 NEI=1.00000e+00
+ IBEN=5e-15 NEN=2.00000e+00 IBCI=2e-17
+ NCI=1.00000e+00 IBCN=5e-15 NCN=2.00000e+00
+ AVC1=2 AVC2=15 ISP=1e-15
+ WSP=1.000e+00 NFP=1.00000e+00 IBEIP=0
+ IBENP=0 IBCIP=0 NCIP=1.00000e+00
+ IBCNP=0 NCNP=2.00000e+00 VEF=10
+ VER=4 IKF=0.002 IKR=0.0002 IKP=0.0002
+ TF=1.e-11 QTF=0 XTF=20
+ VTF=0 ITF=0.08 TR=1e-10
+ KFN=0 AFN=1.0e+00
+ BFN=1.0000e+00 XRE=0 XRB=0
+ XRC=0 XRS=0 XVO=0
+ EA=1.12000e+00 EAIE=1.12000e+00
+ EANE=1.12000e+00 EANC=1.12000e+00
+ EANS=1.12000e+00 XIS=3.00000e+00
+ XII=3.00000e+00 XIN=3.00000e+00
+ TNF=0 TAVC=0
+ RTH=300 CTH=0
+ TD=0
*+ TD=2.e-11
.dc vc 0.0 5.0001 0.05 vb 0.7 1.0001 0.05
.print i(vc) i(vb) v(t)
.end
```

where v(t) prints the device temperature, using the T node.

Table 4-16: Default Model Parameters for BJT, Level 4 ***(Sheet 1 of 5)***

Name (Alias)	Unit	Default	Description
AFN		1	Flicker noise exponent for current
AJC		-0.5	Base-collector capacitance switching parameter
AJE		-0.5	Base-emitter capacitance switching parameter
AJS		-0.5	Substrate-collector capacitance switching parameter
AVC1	V^{-1}	0	Base-collector weak avalanche parameter 1
AVC2	V^{-1}	0	Base-collector weak avalanche parameter 2
BFN		1	Flicker noise exponent for 1/f dependence
CBCO (CBC0)	F	0	Extrinsic base-collector overlap capacitance
CBEO (CBE0)	F	0	Extrinsic base-emitter overlap capacitance
CJC	F	0	Base-collector intrinsic zero bias capacitance
CJCP	F	0	Substrate-collector zero bias capacitance
CJE	F	0	Base-emitter zero bias capacitance
CJEP	F	0	Base-collector extrinsic zero bias capacitance
CTH	J/K	0	Thermal capacitance
EA	eV	1.12	Activation energy for IS
EAIC	eV	1.12	Activation energy for IBCI/IBEIP
EAIE	eV	1.12	Activation energy for IBEI
EAIS	eV	1.12	Activation energy for IBCIP
EANC	eV	1.12	Activation energy for IBCN/IBENP
EANE	eV	1.12	Activation energy for IBEN

Table 4-16: Default Model Parameters for BJT, Level 4 *(Sheet 2 of 5)*

Name (Alias)	Unit	Default	Description
EANS	eV	1.12	Activation energy for IBCNP
FC		0.9	Forward bias depletion capacitance limit
GAMM		0	Epi doping parameter
HRCF		1	High-current RC factor
IBCI	A	1e-16	Ideal base-collector saturation current
IBCIP	A	0	Ideal parasitic base-collector saturation current
IBCN	A	1e-15	Non-ideal base-collector saturation current
IBCNP	A	0	Non-ideal parasitic base-collector saturation current
IBEI	A	1e-18	Ideal base-emitter saturation current
IBEIP	A	0	Ideal parasitic base-emitter saturation current
IBEN	A	1e-15	Non-ideal base-emitter saturation current
IBENP	A	0	Non-ideal parasitic base-emitter saturation current
IKF	A	2e-3	Forward knee current
IKP	A	2e-4	Parasitic knee current
IKR	A	2e-4	Reverse knee current
IS	A	1e-16	Transport saturation current
ISP	A	1e-16	Parasitic transport saturation current
ITF	A	1e-3	Coefficient of TF dependence in Ic
KFN		0	Base-emitter flicker noise constant
MC		0.33	Base-collector grading coefficient

Table 4-16: Default Model Parameters for BJT, Level 4 ***(Sheet 3 of 5)***

Name (Alias)	Unit	Default	Description
ME		0.33	Base-emitter grading coefficient
MS		0.33	Substrate-collector grading coefficient
NCI		1	Ideal base-collector emission coefficient
NCIP		1	Ideal parasitic base-collector emission coefficient
NCN		2	Non-ideal base-collector emission coefficient
NCNP		2	Non-ideal parasitic base-collector emission coefficient
NEI		1	Ideal base-emitter emission coefficient
NEN		2	Non-ideal base-emitter emission coefficient
NF		1	Forward emission coefficient
NFP		1	Parasitic forward emission coefficient
NR		1	Reverse emission coefficient
PC	V	0.75	Base-collector built-in potential
PE	V	0.75	Base-emitter built-in potential
PS	V	0.75	Substrate-collector built-in potential
QCO (QC0)	C	0	Epi charge parameter
QTF		0	Variation of TF with base-width modulation
RBI	Ohm	1e-1	Intrinsic base resistance
RBP	Ohm	1e-1	Parasitic base resistance
RBX	Ohm	1e-1	Extrinsic base resistance
RCI	Ohm	1e-1	Intrinsic collector resistance

Table 4-16: Default Model Parameters for BJT, Level 4 *(Sheet 4 of 5)*

Name (Alias)	Unit	Default	Description
RCX	Ohm	1e-1	Extrinsic collector resistance
RE	Ohm	1e-1	Emitter resistance
RS	Ohm	1e-1	Substrate resistance
RTH	K/W	0	Thermal resistance
TAVC	1/K	0	Temperature coefficient of AVC2
TD	s	0	Forward excess-phase delay time
TF	s	1e-11	Forward transit time
TNF	1/K	0	Temperature coefficient of NF
TR	s	1e-11	Reverse transit time
TREF (TNOM)	^{o}C	27	Nominal measurement temperature of parameters (do not use TNOM alias)
VEF	V	0	Forward Early voltage
VER	V	0	Reverse Early voltage
VO (V0)	V	0	Epi drift saturation voltage
VTF	V	0	Coefficient of TF dependence on Vbc
WBE		1	Portion of IBEI from Vbei, 1-WBE from Vbex
WSP		1	Portion of ICCP from Vbep, 1-WSP from Vbci
XII		3	Temperature exponent of IBEI/IBCI/IBEIP/ IBCIP
XIN		3	Temperature exponent of IBEN/IBCN/IBENP/ IBCNP
XIS		3	Temperature exponent of IS

Table 4-16: Default Model Parameters for BJT, Level 4 ***(Sheet 5 of 5)***

Name (Alias)	Unit	Default	Description
XRB		1	Temperature exponent of base resistance
XRC		1	Temperature exponent of collector resistance
XRE		1	Temperature exponent of emitter resistance
XRS		1	Temperature exponent of substrate resistance
XTF		0	Coefficient of TF bias dependence
XVO (XV0)		0	Temperature exponent of VO

Notes on Using VBIC

1. Set Level=4 to identify the model as a VBIC bipolar junction transistor.
2. The Level 4 model does not scale with any area terms, and does not yet scale with M.
3. Setting these parameters to zero infers a value of infinity: HRCF, IKF, IKP, IKR, ITF, VEF, VER, VO, VTF.
4. Parameters CBC0, CBE0, QC0, TNOM, V0, and XV0 are aliases for CBCO, CBEO, QCO, TREF, VO, and XVO, respectively. Avant! discourages use of TNOM as a model parameter name, as it is used as the name of the default room temperature.
5. The default room temperature is 25 degrees in Avant! in-circuit simulation, but is 27 in some other simulators. If the VBIC bipolar junction transistor model parameters are specified at 27 degrees, TREF=27 should be added to the model, so that the model parameters will be interpreted correctly. It is a matter of choice whether you set the nominal simulation temperature to 27, by adding .OPTION TNOM=27 to the netlist. Do this when testing Avant! in-circuit simulators, versus other simulators that use 27 as the default room temperature.
6. Pole-zero simulation of this model is not supported.
7. For this version of implementation, all seven internal resistors should have values greater than or equal to $1.0e^{-3}$. Values smaller than this will be reassigned a value of $1.0e^{-3.}$

Level 6 Philips Bipolar Model (MEXTRAM Level 503)

The Philips bipolar model (MEXTRAM Level 503) is the BJT Level 6 model. The MEXTRAM covers several effects that are not included in, e.g., the original Gummel-Poon model. These effects include:

- Temperature
- Charge storage
- Substrate
- Parasitic PNP
- High-injection
- Built-in electric field in base region
- Bias-dependent Early effect
- Low-level, non-ideal base currents
- Hard- and quasi-saturation
- Weak avalanche
- Hot carrier effects in the collector epilayer
- Explicit modeling of inactive regions
- Split base-collector depletion capacitance
- Current crowding and conductivity modulation for base resistance
- First order approximation of distributed high frequency effects in the intrinsic base (high frequency current crowding and excess phase shift)

The description for this model can be found at “http://www-us.semiconductors.com/Philips_Models/”.

Level 6 Element Syntax

General Form

```
Qxxx nc nb ne <ns> mname <AREA=val>
+ <OFF<VBE=val><VCE=val> <M=val>
+ <DTEMP=val>
```

where the angle brackets indicate optional parameters.

The arguments are as follows:

Qxxx	BJT element name. Must begin with Q, which can be followed by up to 1023 alphanumeric characters.
nc	Collector terminal node name or number.
nb	Base node name or number.
ne	Emitter terminal node name or number.
ns	Substrate node name or number.
mname	BJT model name reference.
AREA	The normalized emitter area.
OFF	Sets initial condition to OFF for this element in DC analysis.
VBE	Initial internal base to emitter voltage.
VCE	Initial internal collector to emitter voltage.
M	Multiplier to simulate multiple BJTs in parallel.
DTEMP	The difference between element and circuit temperature.

Level 6 Model Parameters

The following tables describe MEXTRAM as Level 6 model parameters including parameters name, descriptions, units, default values and notes.

Table 4-17: Flags

Parameter	Unit	Default	Description
Level	-	-	Level 6 for MEXTRAM
EXAVL	-	0	Flag for extended modeling of avalanche currents
EXMOD	-	0	Flag for extended modeling of the reverse current gain
EXPHI	-	1	Flag for distributed high frequency effects

Table 4-18: Basic Parameters *(Sheet 1 of 4)*

Parameter	Unit	Default	Description
TREF	^{o}C	0.0	Model nominal temperature
IS	A	5.E-17	Collector-emitter saturation current
BF	A	140.0	Ideal forward current gain
XIBI	-	0.0	Fraction of ideal base current that belongs to the sidewall
IBF	A	2.0E-14	Saturation current of the non-ideal forward base current
VLF	V	0.5	Cross-over voltage of the non-ideal forward base current
IK	A	15.E-3	High-injection knee current
BRI	-	16.0	Ideal reverse current gain
IBR	A	8.0e-15	Saturation current of the non-ideal reverse base current

Table 4-18: Basic Parameters *(Sheet 2 of 4)*

Parameter	Unit	Default	Description
VLR	V	0.5	Cross-over voltage of the non-ideal reverse base current
XEXT	-	0.5	Part of I EX,Q EX, Q TEX. and I SUB that depends on the base-collector voltage VBC1
QBO	C	1.2e-12	Base charge at zero bias
ETA	-	4.0	Factor of the built-in field of the base
AVL	-	50.	Weak avalanche parameter
EFI	-	0.7	Electric field intercept (with EXAVL=1)
IHC	A	3.e-3	Critical current for hot carriers
RCC	ohm	25.	Constant part of the collector resistance
RCV	ohm	750.	Resistance of the unmodulated epilayer
SCRCV	ohm	1000.0	Space charge resistance of the epilayer
SFH	-	0.6	Current spreading factor epilayer
RBC	ohm	50.	Constant part of the base resistance
RBV	ohm	100.	Variable part of the base resistance at zero bias
RE	ohm	2.0	Emitter series resistance
TAUNE	s	3.e-10	Minimum delay time of neutral and emitter charge
MTAU	-	1.18	Non-ideality factor of the neutral and emitter charge

Table 4-18: Basic Parameters *(Sheet 3 of 4)*

Parameter	Unit	Default	Description
CJE	F	2.5e-13	Zero bias collector-base depletion capacitance
VDE	V	0.9	Emitter-base diffusion voltage
PE	-	0.33	Emitter-base grading coefficient
XCJE	F	0.5	Fraction of the emitter-base depletion capacitance that belongs to the sidewall
CJC	F	1.3e-13	Zero bias collector-base depletion capacitance
VDC	V	0.6	Collector-base diffusion voltage
PC	-	0.4	Collector-base grading coefficient variable part
XP	F	0.2	Constant part of CJC
MC	-	0.5	Collector current modulation coefficient
XCJC	-	0.1	Fraction of the collector-base depletion capacitance under the emitter area
VGE	V	1.01	Band-gap voltage of the emitter
VGB	V	1.18	Band-gap voltage of the base
VGC	V	1.205	Band-gap voltage of the collector
VGJ	V	1.1	Band-gap voltage recombination emitter-base junction
VI	V	0.040	Ionization voltage base dope
NA	cm^-3	3.0E17	Maximum base dope concentration

Table 4-18: Basic Parameters *(Sheet 4 of 4)*

Parameter	Unit	Default	Description
ER	-	2.E-3	Temperature coefficient of VLF and VLR
AB	-	1.35	Temperature coefficient resistivity of the base
AEPI	-	2.15	Temperature coefficient resistivity of the epilayer
AEX	-	1.	Temperature coefficient resistivity of the extrinsic base
AC	-	0.4	Temperature coefficient resistivity of the buried layer
KF	-	2.E-16	Flicker noise coefficient ideal base current
KFN	-	2.E-16	Flicker noise coefficient non-ideal base current
AF	-	1.0	Flicker noise exponent
ISS	A	6.E-16	Base-substrate saturation current
IKS	A	5.E-6	Knee current of the substrate
CJS	F	1.e-12	Zero bias collector-substrate depletion capacitance
VDS	V	0.5	Collector-substrate diffusion voltage
PS	-	0.33	Collector-substrate grading coefficient
VGS	V	1.15	Band-gap voltage of the substrate
AS	-	2.15	For a closed buried layer: AS=AC For an open buried layer: AS=AEPI

Example

```
*Simulation Input File
.options gmin=1e-13 gmindc=1e-13 POST=1 converge=1
QCKT 1 2 3 4 mextram area=1.0 m=1

* START SOURCES
VE 3 0 DC 0
VB 2 0 DC 0
VC 1 0 DC 0.1
VS 4 0 DC 0
.DC Vb 0.1 0.90001 0.1
.op

.PRINT DC I(VC) I(VB) I(VE) I(VS)
.temp 22
.model mextram npn Level=6
+ TREF = 2.200000e+01
+ EXMOD= 1.000000e+00 EXPHI= 0.000000e+00
+ EXAVL= 1.000000e+00 IS = 9.602000e-18 BF = 1.381000e+02
+ XIBI = 0.000000e+00 IBF = 2.614800e-15 VLF = 6.164000e-01
+ IK = 1.500000e-02 BRI = 5.951000e+00 IBR = 4.606600e-14
+ VLR = 5.473000e-01 XEXT = 6.016000e-01 QBO = 9.439600e-14
+ ETA = 4.800000e+00 AVL = 6.329000e+01 EFI = 7.306000e-01
+ IHC = 4.541900e-04 RCV = 9.819000e+02 RCC=1.91e+01
+ SCRCV= 1.899000e+03 SFH = 3.556000e-01 RBC = 1.165000e+02
+ RBV = 3.077000e+02 RE = 2.525000e+00 TAUNE= 4.126600e-12
+ MTAU = 1.000000e+00 CJE = 4.909400e-14 VDE = 8.764000e-01
+ PE = 3.242000e-01 XCJE = 2.600000e-01 CJC = 8.539400e-14
+ VDC = 6.390000e-01 PC = 5.237000e-01 XP = 6.561000e-01
+ MC = 5.000000e-01 XCJC= 2.759700e-02 VGE = 1.129000e+00
+ VGB = 1.206000e+00 VGC = 1.120000e+00 VGJ = 1.129000e+00
+ VI = 2.100000e-02 NA = 4.400000e+17 ER = 2.000000e-03
+ AB = 1.000000e+00 AEPI =1.900000e+00 AEX= 3.100000e-01
+ AC = 2.600000e-01 KF =2.000000e-16 KFN = 2.000000e-16
+ AF = 1.000000e+00 ISS = 5.860200e-17 IKS = 6.481200e-06
+ CJS = 2.219600e-13 VDS = 5.156000e-01 PS = 3.299000e-01
+ VGS = 1.120000e+00 AS   = 1.900000e+00
.END
```

Level 6 Philips Bipolar Model (MEXTRAM Level 504)

Level 504 of the MEXTRAM model is also available as BJT Level 6, as is Level 503 of MEXTRAM. Use the VERS parameter to choose MEXTRAM level 503 or 504. The default value of the VERS parameter is 504.

MEXTRAM 504 gives better results for the description of first and higher-order characteristic derivatives than MEXTRAM 503. This effect is noticeable in the output-conductance, the cut-off frequency, and the low-frequency third order distortion.

The MEXTRAM Level 504 covers several effects that are not included in the original Gummel-Poon model. These effects include:

- Temperature
- Charge storage
- Substrate
- Parasitic PNP
- High-injection
- Bias-dependent early effect
- Low-level, non-ideal base currents
- Hard- and quasi-saturation (including Kirk Effect)
- Weak avalanche (optionally including snap-back behavior)
- Explicit modeling of inactive regions
- Split base-collector and base-emitter depletion capacitance
- Current crowding and conductivity modulation of the base resistance
- First order approximation of distributed high frequency effects in the intrinsic base (high frequency current crowding and excess phase shift)
- Ohmic resistance of epilayer
- Velocity saturation effects on the resistance of the epilayer
- Recombination in the base (meant for SiGe transistors)
- Early effects in the case of a graded bandgap (SiGe)
- Thermal noise, shot noise, and 1/f-noise
- Self-heating

The description for this model can be found at:

```
http://www.semiconductors.philips.com/Philips_Models/
newsflash/mextram504
```

Notes for HSPICE Users

The following information should be considered when using MEXTRAM 504 with Hspice:

- Set Level 6 to identify the model as a MEXTRAM bipolar junction transistor model
- Set VERS parameter to 503 to use MEXTRAM 503
- Set VERS parameter to 504 to use MEXTRAM 504
- Consider that all internal resistors are limited to greater than or equal to 1.0e-6
- Reference temperature, TREF, is equal to 25 degrees
- MEXTRAM does not contain extensive geometrical or process scaling rules (it has a multiplication factor to put transistors in parallel)
- MEXTRAM does not contain a substrate resistance
- Constant overlap capacitances are not modelled within MEXTRAM
- MEXTRAM 504 has better convergence than 503
- MEXTRAM is more complex than Gummel-Poon (the computation time will be longer and the convergence will be less)
- No reverse emitter-base breakdown mechanism
- Forward current of the parasitic PNP transistor is modelled
- Output conductance dIc/dVce at the point where hard saturation starts seems to be too abrupt for high current levels, compared to measurements
- Clarity of extrinsic current model describing Xiex and Xisub could be improved by adding an extra node and an extra contact base resistance. In this case, parameter extraction would be more difficult
- Self-heating is not enabled for this model, so model parameters RTH and CTH have no influence

Level 6 Model Parameters (504)

The following tables describe MEXTRAM 504 as Level 6 model parameters including parameter name, unit, default, description and notes.

- TAUNE in MEXTRAM 503 acts as TAUE in the 504 model.
- Parameters noted with a '*' are not used in the DC model.

The following nine parameters are deleted from MEXTRAM 503:

- QBO
- VGE
- VLF
- VI
- AVL
- NA
- ETA
- ER
- EFI

The following 18 parameters have been added to MEXTRAM 504:

- VEF
- VER
- MLF
- WAVL
- VAVL
- AXI
- TAUE
- TAUB
- TEPI
- TAUR
- DEG
- XREC
- AE
- DVGBF
- DVGBR
- DVGTE
- RTH
- CTH

Table 4-19: Flags

Parameter	Unit	Default	Description
Level	-	6	Model level
VERS	-	504	Flag for choosing MEXTRAM model (level 503 or 504)
EXMOD	-	1	Flag for extended modeling of the reverse current gain
EXPHI	-	1	*Flag for distributed high frequency effects in transient
EXAVL	-	0	Flag for extended modeling of avalanche currents
TREF	^{o}C	25.0	Reference temperature

Table 4-20: Basic Parameters

Parameter	Unit	Default	Description
IS	A	2.2e-17	Collector-emitter saturation current
VER		2.5	Reverse early voltage
VEF		44.0	Forward early voltage
BF	-	215.0	Ideal forward current gain
XIBI	-	0.0	Fraction of ideal base current that belongs to the sidewall
IBF	A	2.7e-15	Saturation current of the non-ideal forward base current

Table 4-20: Basic Parameters *(Continued)*

Parameter	Unit	Default	Description
MLF	V	2.0	Non-ideality factor of the non-ideal forward base current
IK	A	0.1	Collector-emitter high injection knee current
BRI	-	7.0	Ideal reverse current gain
IBR	A	1.0e-15	Saturation current of the non-ideal reverse base current
VLR	V	0.2	Cross-over voltage of the non-ideal reverse base current
XEXT	-	0.63	Part of Iex, Qex, Qtex, and Isub that depends on the base-collector voltage Vbc1

Table 4-21: Avalanche Model Parameters

Parameter	Unit	Default	Description
WAVL	m	1.1e-6	Epilayer thickness used in weak-avalanche model
VAVL	V	3.0	Voltage determining the curvature of avalanche current
SFH	-	0.3	Current spreading factor of avalanche model (when EXAVL=1)

Table 4-22: Resistance and Epilayer Parameters

Parameter	Unit	Default	Description
RE	Ohm	5.0	Emitter resistance
RBC	Ohm	23.0	Constant part of the base resistance
RBV	Ohm	18.0	Zero-bias value of the variable part of the base resistance
RCC	Ohm	12.0	Constant part of the collector resistance
RCV	Ohm	150.0	Resistance of the un-modulated epilayer
SCRCV	Ohm	1250.0	Space charge resistance of the epilayer
IHC	A	4.0e-3	Critical current for velocity saturation in the epilayer
AXI	-	0.3	Smoothness parameter for the onset of quasi-saturation

Table 4-23: Base-Emitter Capacitances

Parameter	Unit	Default	Description
CJE	F	7.3e-14	*Zero bias emitter-base depletion capacitance
VDE	V	0.95	Emitter-base diffusion voltage
PE	-	0.4	Emitter-base grading coefficient
XCJE	-	0.4	*Fraction of the emitter-base depletion capacitance that belongs to the sidewall

Table 4-24: Base-Collector Capacitances

Parameter	Unit	Default	Description
CJC	F	7.8e-14	*Zero bias collector-base depletion capacitance
VDC	V	0.68	Collector-base diffusion voltage
PC	-	0.5	Collector-base grading coefficient
XP	-	0.35	Constant part of CJC
MC	-	0.5	Coefficient for the current modulation of the collector-base depletion capacitance
XCJC	-	3.2e-2	*Fraction of the collector-base depletion capacitance under the emitter

Table 4-25: Transit Time Parameters

Parameter	Unit	Default	Description
MTAU	-	1.0	*Non-ideality of the emitter stored charge
TAUE	S	2.0e-12	*Minimum transit time of stored emitter charge
TAUB	S	4.2e-12	*Transit time of stored base charge
TEPI	S	4.1e-11	*Transit time of stored epilayer charge
TAUR	S	5.2e-10	*Transit time of reverse extrinsic stored base charge
DEG	EV	0.0	Bandgap difference over the base
XREC	-	0.0	Pre-factor of the recombination part of Ib1

Table 4-26: Temperature Parameters

Parameter	Unit	Default	Description
AQBO	-	0.3	Temperature coefficient of the zero-bias base charge
AE	-	0.0	Temperature coefficient of the resistivity of the emitter
AB	-	1.0	Temperature coefficient of the resistivity of the base
AEPI	-	2.5	Temperature coefficient of the resistivity of the epilayer
AEX	-	0.62	Temperature coefficient of the resistivity of the extrinsic base
AC	-	2.0	Temperature coefficient of the resistivity of the buried layer
DVGBF	V	5.0e-2	Bandgap voltage difference of forward current gain
CVGBR	V	4.5e-2	Bandgap voltage difference of reverse current gain
VGB	V	1.17	Bandgap voltage of the base
VGC	V	1.18	Bandgap voltage of the collector
VGJ	V	1.15	Bandgap voltage recombination emitter-base junction
DVGTE	V	0.05	*Bandgap voltage difference of emitter stored charge

Table 4-27: Noise Parameters

Parameter	Unit	Default	Description
AF	-	2.0	Exponent of the flicker-noise
KF	-	2.0e-11	Flicker-noise coefficient for ideal base current
KFN	-	2.0e-11	Flicker-noise coefficient, non-ideal base current

Table 4-28: Substrate Parameters

Parameter	Unit	Default	Description
ISS	A	4.8e-17	Base-substrate saturation current
IKS	A	2.5e-4	Base-substrate high injection knee current
CJS	F	3.15e-13	*Zero bias collector-substrate depletion capacitance
VDS	V	0.62	*Collector-substrate diffusion voltage
PS	-	0.34	*Collector-substrate grading coefficient
VGS	V	1.2	Bandgap voltage of the substrate
AS	-	1.58	For a closed buried layer: AS=AC For an open buried layer: AS=AEPI

Table 4-29: Self-Heating Parameters

Parameter	Unit	Default	Description
RTH	^{o}C/W	300.0	Thermal resistance
CTH	J/^C	3.0e-9	*Thermal capacitance

MEXTRAM Level 504 DC OP Analysis Example

```
**** DC OP analysis of mextram 504 model ****
.OPTIONs GMIN=1.0e-13
Q1 1 2 3 4 m504 area=1 m=1

* Start sources
VB 2 0 DC 1.2
VC 1 0 DC 2.2
VE 3 0 DC 0.0
VS 4 0 DC 0.0
.DC VB 0.4 1.2 0.1
.DC VC 1.4 2.2 0.1
.op

.PRINT DC I(VC) I(VB) I(VE) I(VS)
.TEMP 25

.Model m504 npn level=6
    + VERS       = 504
    + TREF       = 25.0
    + EXMOD      = 1.0
    + EXPHI      = 1.0
    + EXAVL      = 0.0
    + IS         = 22.0E-18
    + IK         = 0.1
    + VER        = 2.5
    + VEF        = 44.0
    + BF         = 215.0
    + IBF        = 2.7E-15
    + MLF        = 2.0
    + XIBI       = 0.0
    + BRI        = 7.0
    + IBR        = 1.0e-15
    + VLR        = 0.2
    + XEXT       = 0.63
    + WAVL       = 1.1E-6
    + VAVL       = 3.0
    + SFH        = 0.3
    + RE         = 5.0
    + RBC        = 23.
    + RBV        = 18.
    + RCC        = 12.
    + RCV        = 150.
```

```
+ SCRCV      = 1250.0
+ IHC        = 4.e-3
+ AXI        = 0.3
+ CJE        = 73.0e-15
+ VDE        = 0.95
+ PE         = 0.4
+ XCJE       = 0.4
+ CJC        = 78.0E-15
+ VDC        = 0.68
+ PC         = 0.5
+ XP         = 0.35
+ MC         = 0.5
+ XCJC       = 32.E-3
+ MTAU       = 1.0
+ TAUB       = 4.2E-12
+ TEPI       = 41.E-12
+ TAUR       = 520.E-12
+ DEG        = 0.01
+ XREC       = 0.1
+ AQBO       = 0.3
+ AE         = 0.0
+ AB         = 1.0
+ AEPI       = 2.5
+ AEX        = 0.62
+ AC         = 2.0
+ DVGBF      = 0.05
+ DVGBR      = 0.045
+ VGB        = 1.17
+ VGC        = 1.18
+ VGJ        = 1.15
+ DVGTE      = 0.05
+ AF         = 2.0
+ KF         = 2.E-11
+ KFN        = 2.E-11
+ ISS        = 48.E-18
+ IKS        = 250.E-6
+ CJS        = 315.E-15
+ VDS        = 0.62
+ PS         = 0.34
+ VGS        = 1.20
+ AS         = 1.58
.END
```

MEXTRAM Level 504 Transient Analysis Example

```
*** Transient analysis of Mextram 504 model ***
.options gmin=1e-13 dccap POST=1
QCKT 1 2 0 0 m504 area=1.0 m=1

* START SOURCES
VC 3 0 DC 2
VB 2 0 DC 0 PULSE (0 0.8 0 1n 1n 10n 25n)
R 1 3 0.1

.temp 100
.TRAN 10p 50n
.op
.PRINT tran I(VC) I(VB)
.Model m504 npn level=6
    + VERS       = 504
    + TREF       = 25.0
    + EXMOD      = 1.0
    + EXPHI      = 1.0

    + EXAVL      = 0.0
    + IS         = 22.0E-18
    + IK         = 0.1
    + VER        = 2.5
    + VEF        = 44.0
    + BF         = 215.0
    + IBF        = 2.7E-15
    + MLF        = 2.0
    + XIBI       = 0.0
    + BRI        = 7.0
    + IBR        = 1.0e-15
    + VLR        = 0.2
    + XEXT       = 0.63
    + WAVL       = 1.1E-6
    + VAVL       = 3.0
    + SFH        = 0.3
    + RE         = 5.0
    + RBC        = 23.
    + RBV        = 18.
    + RCC        = 12.
    + RCV        = 150.
    + SCRCV      = 1250.0
    + IHC        = 4.e-3
```

```
+ AXI        = 0.3
+ CJE        = 73.0e-15
+ VDE        = 0.95
+ PE         = 0.4
+ XCJE       = 0.4
+ CJC        = 78.0E-15
+ VDC        = 0.68
+ PC         = 0.5
+ XP         = 0.35
+ MC         = 0.5
+ XCJC       = 32.E-3
+ MTAU       = 1.0
+ TAUE       = 2.0E-12
+ TAUB       = 4.2E-12
+ TEPI       = 41.E-12
+ TAUR       = 520.E-12
+ DEG        = 0.01
+ XREC       = 0.1
+ AQBO       = 0.3
+ AE         = 0.0
+ AB         = 1.0
+ AEPI       = 2.5
+ AEX        = 0.62
+ AC         = 2.0
+ DVGBF      = 0.05
+ DVGBR      = 0.045
+ VGB        = 1.17
+ VGC        = 1.18
+ VGJ        = 1.15
+ DVGTE      = 0.05
+ AF         = 2.0
+ KF         = 2.E-11
+ KFN        = 2.E-11
+ ISS        = 48.E-18
+ IKS        = 250.E-6
+ CJS        = 315.E-15
+ VDS        = 0.62
+ PS         = 0.34
+ VGS        = 1.20
+ AS         = 1.58
.END
```

MEXTRAM Level 504 AC Analysis Example

```
*** AC analysis of Mextram 504 model ***
.options gmin=1e-13 POST=1 converge=1 relv=1.e-6 absv=1.e-9
QCKT 11 22 33 44 m504 area=1.0 m=1
* START SOURCES
VE 3 0 DC 0
VB 2 0 DC 0.7
VC 1 0 DC 1.0
VS 4 0 DC 0
.DC VB 0.7 1.0 0.02
.ac dec 1 1.e4 1.e11
vc1 11 1 0
vb1 22 2 0 ac=0.001
ve1 33 3 0
vs1 44 4 0
.op
.print ac ir(vc1) ii(vc1) ir(vb1) ii(vb1)
.temp 25
.Model m504 npn level=6
    + VERS       = 504
    + TREF       = 25.0
    + EXMOD      = 1.0
    + EXPHI      = 1.0
    + EXAVL      = 0.0
    + IS         = 22.0E-18
    + IK         = 0.1
    + VER        = 2.5
    + VEF        = 44.0
    + BF         = 215.0
    + IBF        = 2.7E-15
    + MLF        = 2.0
    + XIBI       = 0.0
    + BRI        = 7.0
    + IBR        = 1.0e-15
    + VLR        = 0.2
    + XEXT       = 0.63
    + WAVL       = 1.1E-6
    + VAVL       = 3.0
    + SFH        = 0.3
    + RE         = 5.0
    + RBC        = 23.
    + RBV        = 18.
    + RCC        = 12.
    + RCV        = 150.
    + SCRCV      = 1250.0
```

```
      + IHC        = 4.e-3
      + AXI        = 0.3
      + CJE        = 73.0e-15
      + VDE        = 0.95
      + PE         = 0.4
      + XCJE       = 0.4
      + CJC        = 78.0E-15
      + VDC        = 0.68
      + PC         = 0.5
      + XP         = 0.35
      + MC         = 0.5
      + XCJC       = 32.E-3
      + MTAU       = 1.0
      + TAUE       = 2.0E-12
      + TAUB       = 4.2E-12
      + TEPI       = 41.E-12
      + TAUR       = 520.E-12
      + DEG        = 0.01
      + XREC       = 0.1
      + AQBO       = 0.3
      + AE         = 0.0
      + AB         = 1.0
      + AEPI       = 2.5
      + AEX        = 0.62
      + AC         = 2.0
      + DVGBF      = 0.05
      + DVGBR      = 0.045
      + VGB        = 1.17
      + VGC        = 1.18
      + VGJ        = 1.15
      + DVGTE      = 0.05
      + AF         = 2.0
      + KF         = 2.E-11
      + KFN        = 2.E-11
      + ISS        = 48.E-18
      + IKS        = 250.E-6
      + CJS        = 315.E-15
      + VDS        = 0.62
      + PS         = 0.34
      + VGS        = 1.20
      + AS         = 1.58
.END
```

Level 8 HiCUM Model

What is the HiCUM Model?

HiCUM is an advanced transistor model for bipolar transistors, with a primary emphasis on circuit design for high-speed/high-frequency applications. HiCUM development was spurred by the SPICE Gummel-Poon model's (SGPM) inadequate level of accuracy for high-speed large-signal transient applications and the required high-collector current densities. Other major disadvantages of the SGPM are:

- A lack of sufficient physical background
- Poor descriptions of base resistance and junction capacitances in the regions of interest
- Inadequate description of both Si- and III-V material-based HBTs.

The HiCUM model is implemented as Level 8 in the BJT models.

HiCUM Model Advantages

Major features of HiCUM are:

- Accurate description of the high-current operating region (including quasi-saturation and saturation).
- Distributed modelling of external base-collector region.
- Proper handling of emitter periphery injection and charge storage.
- Internal base resistance as a function of operating point (conductivity modulation *and* emitter current crowding), and emitter geometry.
- Sufficiently physical model equations allowing predictions of temperature and process variations, as well as scalability, even at high current densities.
- Parasitic capacitances, independent on operating point, are available in the equivalent circuit, representing base-emitter and base-collector oxide overlaps, that become significant for small-size transistors.
- Weak avalanche breakdown is available.
- Self-heating effects are included. Non-quasi-static effects, resulting in a delay of collector current AND stored minority charge, are modelled as function of bias.

- Collector current spreading is included in minority charge and collector current formulation.
- Extensions for graded-base SiGe HBTs have been derived using the Generalized Integral Charge-Control Relation (GICCR); the GICCR also permits modelling of HBTs with (graded) bandgap differences within the junctions.
- Base-emitter tunneling model is available (e.g., for simulation of varactor leakage).
- Simple parasitic substrate transistor is included in the equivalent circuit.
- Simple parallel RC network taking into account the frequency dependent coupling between buried layer and substrate terminal.
- Parameter extraction is closely related to the process enabling parametric yield simulation; parameter extraction procedure and list of test structures are available; HiCUM parameters can be determined using standard measurement equipment and mostly simple, decoupled extraction procedures.
- Simple equivalent circuit and numerical formulation of model equations result in easy implementation and relatively fast execution time.

These features together with the choice of easily measurable basic variables such as junction capacitances and transit time provide - compared to the SGPM - high accuracy for digital circuit, small-signal high-frequency and, in particular, high-speed large-signal transient simulation. Also, HiCUM is laterally scaleable over a wide range of emitter widths and lengths up to high collector current densities; the scaling algorithm is generic and has been applied to the SGPM (within its validity limits).

In summary, HiCUM’s major advantages over other bipolar compact models are:

- Scalability
- Process-based and relatively simple parameter extraction
- Predictive capability in terms of process and layout variations
- Fairly simple numerical formulation facilitating easy implementation and resulting in still reasonable simulation time compared to the (too) simple SGPM at high current densities

Avant! HiCUM Model vs. Public HiCUM Model

Difference Highlights

To maintain flexibility, the Level 8 HiCUM model uses FBCS, IS, KRBI, MCF, MSR, and ZETACX as additional model parameters. See ‘Other Parameters” on page 4-102.

Model Implementation

Table 4-30: Model Parameters

Parameter	Unit	Default	Description
Level		8	HiCUM BJT level
TREF	C	26.85	Temperature in simulation

Internal Transistors

Table 4-31: Transfer Current Parameters

Parameter	Unit	Default	Factor	Description
C10	A^2s	3.76e-32	M^2	Constant(IS*QP0)
Qp0	As	2.78e-14		Zero-bias hole charge
ICH	A	2.09e-0Z		High-current correction for 2D/3D
HFC	-	1.0		Weighting factor for Qfc (mainly for HBTs)
HFE	-	1.0		Weighting factor for Qef in HBTs
HJCI	-	1.0		Weighting factor for Qjci in HBTs
HJEI	-	0.0		Weighting factor for Qjei in HBTs
ALIT	-	0.45		Factor for additional delay time of iT

Table 4-32: BE Depletion Capacitance Parameters

Parameter	Unit	Default	Factor	Description
VDEI	V	0.95		Built-in voltage
CJEI0	F	8.11e-15		Zero-bias value
ZEI	-	0.5		Exponent coefficient
ALJEI	-	1.8		Ratio of max. to zero-bias value

Table 4-33: BC Depletion Capacitance Parameters

Parameter	Unit	Default	Factor	Description
CJCI0	F	1.16e-15	M^2	Zero-bias value
VDCI	V	0.8		Built-in voltage
ZCI	-	0.333		Exponent coefficient
VPTCI	V	416		Punch-through voltage (=q Nci w^2ci /(2epsilion))

Table 4-34: Forward Transit Time Parameters

Parameter	Unit	Default	Factor	Description
T0	s	4.75e-12		Low current transit time at $V_{B'C'}$=0
DT0H	s	2.1e-12		Time constant for base and BC SCR width modulation
TBVL	s	40e-12		Voltage for modeling carrier jam at low $V_{C'E'}$
TEF0	s	1.8e-12		Storage time in neutral emitter
GTFE	-	1.4		Exponent factor for current dep. emitter transit time
THCS	s	3.0e-11		Saturation time constant at high current densities
ALHC	-	0.75		Smoothing factor for current dep. C and B transit time
FTHC	-	0.6		Partitioning factor for base and collection portion
ALQF	-	0.225		Factor for additional delay time of Q_f

Table 4-35: Critical Current Parameters

Parameter	Unit	Default	Factor	Description
RCI0	Ohm	127.8	1/M	Low-field resistance of internal collector region
VLIM	V	0.7		Voltage separating ohmic and SCR regime
VPT	V	5.0		Epi punch-through vtg. of BC SCR
VCES	V	0.1		Internal CE sat. vtg.

Table 4-36: Inverse Transit Time Parameter

Parameter	Unit	Default	Factor	Description
TR	s	1.0e-9		Time constant for inverse operation

Table 4-37: Base Current Components Parameters

Parameter	Unit	Default	Factor	Description
IBEIS	A	1.16e-20	M	BE saturation current
MBEI	-	1.015		BE saturation current
IREIS	A	1.16e-6	M	BE recombination saturation current
MREI	-	2.0		BE recombination non-ideality factor
IBCIS	A	1.16e-20	M	BC saturation current
MBCI	-	1.015		BC non-ideality factor

Table 4-38: Weak BC Avalanche Breakdown Parameters

Parameter	Unit	Default	Factor	Description
FAVL	1/V	1.186		Prefactor for CB avalanche effect
QAVL	As	1.11e-14	M	Exponent factor for CB avalanche effect

Table 4-39: Internal Base Resistance Parameters

Parameter	Unit	Default	Factor	Description
RBI0	Ohm	0	1/M	Value at zero-bias
FDQR0	-	0.0		Correction factor for modulation by BE abd BC SCR
FGEO	-	0.73		Geometry factor (value corresponding to long emitter stripe)
FQI	-	0.9055		Ratio of internal to total minority charge
FCRBI	-	0.0		Ratio of h.f. shunt to total internal capacitance.

Table 4-40: Lateral Scaling

Parameter	Unit	Default	Factor	Description
LATB	-	3.765		Scaling factor for Qfc in 1_E
LATL	-	0.342		Scaling factor for Qfc in l_E direction

Peripheral Elements

Table 4-41: BE Depletion Capacitance

Parameter	Unit	Default	Factor	Description
CJEP0	F	2.07e-15	M	Zero-bias value
VDEP	V	1.05		Built-in voltage
ZEP	-	0.4		Depletion coeff
ALJEP	-	2.4		Ratio of max. to zero-bias value

Table 4-42: Base Current

Parameter	Unit	Default	Factor	Description
IBEPS	A	3.72e-21	M	Saturation current
MBEP	-	1.015		Non-ideality factor
IREPS	A	1e-30	M	Recombination saturation factor
MREP	-	2.0		Recombination non-ideality factor

Table 4-43: BE Tunneling

Parameter	Unit	Default	Factor	Description
IBETS	A	0	M	Saturation current
ABET	-	0.0		Exponent coefficient

External Elements

Table 4-44: BC Capacitance

Parameter	Unit	Default	Factor	Description
CJCX0	F	5.393e-15	M	Zero-bias depletion value
VDCX	V	0.7		Built-in voltage
ZCX	-	0.333		Exponent coefficient
VPTCX	V	100		Punch-through voltage
CCOX	F	2.97e-15	M	Collector oxide capacitance
FBC	-	0.1526		Partitioning factor for C_BCX =C'_BCx+C"_BCx

Table 4-45: BC Base Current Component

Parameter	Unit	Default	Factor	Description
IBCXS	A	4.39e-20	M	Saturation current
MBCX	-	1.03		Non-ideality factor

Table 4-46: Other External Elements

Parameter	Unit	Default	Factor	Description
CEOX	F	1.13e-15	M	Emitter-base isolation overlap cap
RBX	Ohm	0	1/M	External base series resistance
RE	Ohm	0	1/M	Emitter series resistance
RCX	Ohm	0	1/M	External collector series resistance

Table 4-47: Substrate Transistor Parameters

Parameter	Unit	Default	Factor	Description
ITSS	A	0.0	M	Transfer saturation current
MSF	-	0.0		Non-ideality factor (forward transfer current)
TSF	-	0.0		Minority charge storage transit time
ISCS	A	0.0	M	Saturation current of CS diode
MSC	-	0.0		Non-ideality factor of CS diode

Table 4-48: Collector-Substrate Depletion Capacitance

Parameter	Unit	Default	Factor	Description
CJS0	F	3.64e-14	M	Zero-bias value of CS depletion cap
VDS	V	0.6		Built-in voltage
ZS	-	0.447		Exponent coefficient
VPTS	V	1000		Punch-through voltage

Table 4-49: Substrate Coupling Network

Parameter	Unit	Default	Factor	Description
RSU	Ohm	0	1/M	Substrate series resistance
CSU	F	0		Substrate capacitance from permittivity of bulk material

Table 4-50: Noise Parameters

Parameter	Unit	Default	Factor	Description
KF	-	1.43e-8		Flicker noise factor (no unit only for AF=2!)
AF	-	2.0		Flicker noise exponent factor
KRBI	-	1.17		Factor for internal base resistance

Table 4-51: Temperature Dependence Parameters

Parameter	Unit	Default	Factor	Description
VGB	V	1.17		Bandgap-voltage
ALB	1/K	6.3e-3		Relative temperature coefficient of forward current gain
ALT0	1/K	0		First-order relative temperature coefficient of TEF0
KT0	1/K	0		Second-order relative temperature coefficient of TEF0
ZETACI	-	1.6		Temperature exponent factor RCI0
ALVS	1/K	1e-3		Relative temperature coefficient of saturation drift velocity
ALCES	1/K	0.4e-3		Relative temperature coefficient of VCES
ZETARBI	-	0.588		Temperature exponent factor of RBI0
ZETARBX	-	0.2060		Temperature exponent factor of RBX
ZETARCX	-	0.2230		Temperature exponent factor of RCX

Table 4-51: Temperature Dependence Parameters *(Continued)*

Parameter	Unit	Default	Factor	Description
ZETARE	-	0		Temperature exponent factor of RE
ALFAV	1/K	8.25e-5		Relative temperature coefficient for avalanche breakdown
ALQAV	1/K	1.96e-4		Relative temperature coefficient for avalanche breakdown

Table 4-52: Self-Heating Parameters

Parameter	Unit	Default	Factor	Description
RTH	K/W	0	1/M	Thermal resistance (not supported)
CTH	Ws/K	0	M	Thermal resistance (not supported)

Table 4-53: Other Parameters

Parameter	Unit	Default	Factor	Description
FBCS	-	-1.0		Determine external BC capacitance partitioning
IS	-1.0	A		Ideal saturation current
KRBI	-	1.0		Noise analysis of internal resistance
MCF	-	1.0		Non-ideal factor of reverse current between base and collector. VT=VT*MCF
MSR	-	1.0		Non-ideal factor of reverse current in substrate transistor. VT=VT*MSR
ZETACX	-	1.0		Temperature exponent factor (epi-layer)

Netlist Input and Output Formats

This section provides the syntax for Level 8 and an example of an input netlist and output format.

Syntax

```
Qxxx nc nb ne <ns> mname <area> <M=val> <DTEMP=val>
```

Table 4-54: Netlist Parameters for Level 8

Qxxx	BJT element name
nc	Collector terminal node
nb	Base terminal node, connected to 1 => 2
ne	Emitter terminal node, connected to 1 => 0
ns	Substrate terminal node
mname	BJT model name reference
area	Emitter area multiplying factor which affects currents, resistances and capacitances(default=1)
M	Multiplier to simulate multiple BJTs in parallel
DTEMP	Difference between the element temperature and the circuit temperature in Celsisu. (Default=0.0)

Example

The following is an example of a BJT `Q1` model:

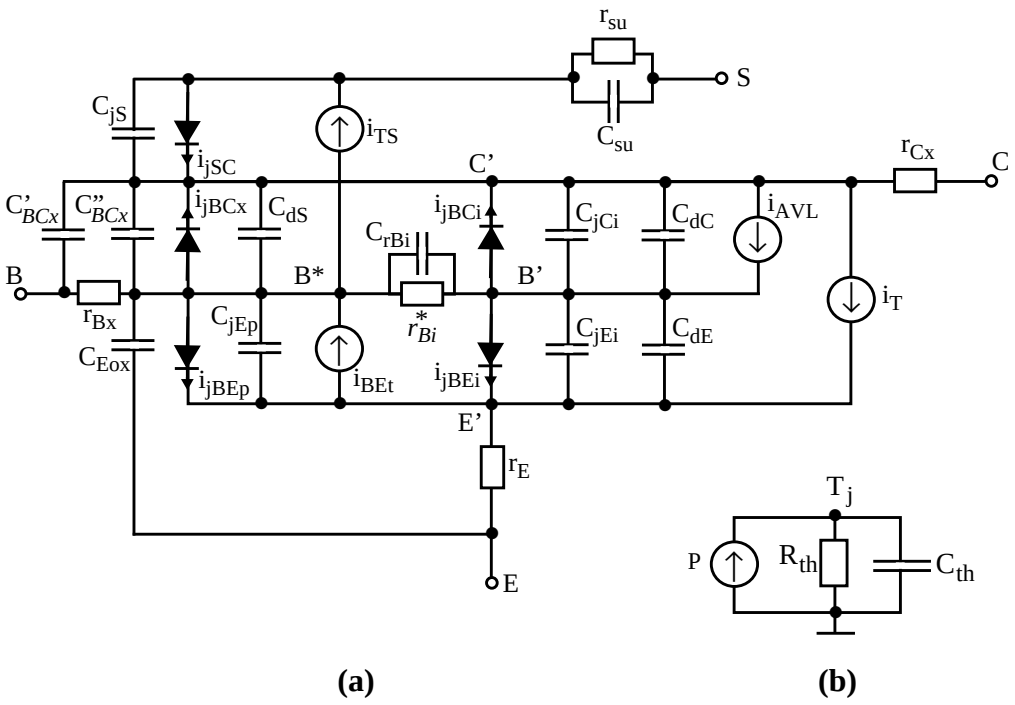
```
Q1 1 2 0 4 QM area=1*0.5*5 dtemp=0.002
```

where:

- Collector is connected to node 1.
- Base is connected to node 1.
- Emitter is connected to node 1.
- Substrate is connected to node 4.
- QM references the name of the BJT model.

Circuit Diagram

Figure 4-15: Large-signal HiCUM/Level2 equivalent circuit



(a) The external BC capacitance consists of a depletion and a bias independent (e.g., oxide) capacitance with the ratio C'_{BCx} / C''_{BCx} being adjusted with respect to proper modelling of the h.f. behavior.
(b) Thermal network used for self-heating calculation.

Input Netlist

```
.DATA test_data vbe vce vsub
0.0 0.0 0.0
0.1 0.0 0.0
0.2 0.0 0.0
0.3 0.0 0.0
0.4 0.0 0.0
0.5 0.0 0.0
0.6 0.0 0.0
0.7 0.0 0.0
0.8 0.0 0.0
0.9 0.0 0.0
1.0 0.0 0.0
.ENDDATA

.OPTIONS
.TEMP 26.85
VIN 2 0 vbe
VC 1 0 vce
VS 4 0 vsub
VE 3 0 0

Q1 1 2 3 4 hicum
.DC data= test_data
.PRINT DC I(VIN) i2(q1) I(VC) i1(q1) I(VCS) i4(q1)

.MODEL hicum NPN Level=8
+        tref = 26.85
+        c10=.3760000E-31 qp0=.2780000E-13 ich=.2090000E-01
+        hfc=.1000000E+01
+        hfe=1.0000000E+00 hjei=.000000E+00
+        hjci=.100000E+01 tr=1.00000000E-9
+        cjei0=.81100E-14 vdei=.950000E+00 zei=.5000000E+00
+        aljei=.18000E+01
+        cjci0=.11600E-14 vdci=.800000E+00 zci=.3330000E+00
+        vptci=.41600E+03
+        rci0=.127800E+03 vlim=.700000E+00 vpt=.5000000E+01
+        vces=.100000E+00
+        t0=.47500000E-11 dt0h=.210000E-11 tbvl=.400000E-11
+        tef0=.180000E-11 gtfe=.140000E+01 thcs=.300000E-10
+        alhc=.750000E+00
+        fthc=.600000E+00
+        latb=.376500E+01 latl=.342000E+00 fqi=.9055000E+00
```

```
+        alit=.450000E+00 alqf=.225000E+00
+        favl=.118600E+01 qavl=.111000E-13 alfav=.82500E-04
+        alqav=.19600E-03
+        ibeis=.11600E-19 mbei=.101500E+01 ibeps=.10000E-29
+        mbep=.200000E+01
+        ireis=.11600E-15 mrei=.200000E+01 ireps=.10000E-29
+        mrep=.200000E+01
+        rbi0=.000000E+00 fdqr0=.00000E+00 fgeo=.730000E+00
+        fcrbi=.00000E+00
+        cjep0=.00000E+00 vdep=.105000E+01 zep=.4000000E+00
+        aljep=.24000E+01
+        ceox=.000000E+00
+        cjcx0=.00000E+00 vdcx=.700000E+00 zcx=.3330000E+00
+        vptcx=.10000E+03
+        ccox=.000000E+00 fbc=.1526000E+00
+        ibcxs=.10000E-29 mbcx=.200000E+01 ibcis=.11600E-19
+        mbci=.101500E+01
+        cjs0=.000000E+00 vds=.6000000E+00 zs=.44700000E+00
+        vpts=.100000E+04
+        rcx=.0000000E+00 rbx=.0000000E+00 re=.00000000E+00
+        kf=.00000000E+00 af=.00000000E+00
+        vgb=.1170000E+01 alb=.6300000E-02 alt0=.000000E+00
+        kt0=.0000000E+00
+        zetaci=.1600E+01 alvs=.100000E-02 alces=.40000E-03
+        zetarbi=0.5880E+00              zetarcx=0.2230E+00
+       zetarbx=0.2060E+00                zetare=0.0000E+00
+        rth=0.0 cth=0.0
+        ibets=.00000E+00 abet=.000000E+00
+        itss=.000000E+00 msf=.0000000E+00 tsf=0.000000E+00
+        iscs=.000000E+00
+        msc=.0000000E+00
+        rsu=.0000000E+00 csu=.0000000E+00
.END
```

Level 9 VBIC99 Model

The VBIC 95(Vertical Bipolar Inter-Company Model) for Motorola bipolar transistor device was already installed in the Avant! True-Hspice models as BJT level 4. VBIC99 is a newer version of the VBIC model, and is implemented in the True-Hspice models as BJT level 9.

To use the VBIC99 model, set the LEVEL parameter to 9 for the bipolar transistor model.

The VBIC99 model includes several effects that are improved compared to the VBIC95 model.

- In VBIC99, the temperature coefficients of the base and collector resistances are split.
- The temperature dependence of the built-in potential is also improved.

Element Syntax of BJT Level 9

General form

```
Qxxx nc nb ne <ns> mname <AREA=val><OFF><VBE=val><VCE=val>
+ <M=val><DTEMP=val>
```

where the angle bracket indicate optional parameters.

Arguments

Qxxx	BJT element name. Must begin with Q, followed by up to 1023 alphanumeric characters.
Nc	Collector terminal node name or number.
Nb	Base terminal node name and number.
Ne	Emitter terminal node name or number.
Ns	Substrate node name or number.

t	Self heating node name or number.
Mname	BJT model name reference.
AREA	The normalized emitter area. VBIC99 level 9 model has no area effect. Default value=1. Area is used only as an alias of the multiplication factor (M).
OFF	Sets the initial condition to OFF, for this element in DC analysis. You cannot use OFF with VBE or VCE.
VBE	Initial internal base-emitter voltage.
VCE	Initial internal collector-emitter voltage.
M	Multiplier to simulate multiple BJTs in parallel.
DTEMP	The temperature difference between the element and the circuit.

Effects of VBIC99

The VBIC99 model includes several effects that are improved compared to the VBIC95 model**:**

- The addition of temperature dependency for several parameters.
- Base-emitter breakdown model.
- Reach-through model, for base-collector depletion capacitance.
- High-current beta rolloff effect.
- Fixed collector-substrate capacitance,
- Reverse transport saturation current.

Model Implementation

The following parameters were added to the VBIC99 model, that are not in the VBIC95 model.

ISRR	IKF	VRT	ART	QBM
DEAR	EAP	VBBE	NBBE	IBBE
TVBBE1	TVBBE2	TNBBE	EBBE	CCSO
XRCX	XRBX	XRBP	XIXF	XISR

The following tables describe VBIC99 as HSPICE BJT level 9 model parameters, including parameter names, descriptions, units, default values, and notes.

Table 4-55: VBIC99 Basic Parameters *(Sheet 1 of 5)*

Parameters	Units	Defaults	Descriptions
LEVEL	-	9	Model level
TREF	W	27.0	Nominal measurement temperature of parameters
RCX	W	0.0	Extrinsic collector Resistance

Table 4-55: VBIC99 Basic Parameters *(Sheet 2 of 5)*

Parameters	Units	Defaults	Descriptions
RCI	W	0.0	Intrinsic collector Resistance
RBI	W	0.0	Intrinsic collector Resistance
RBX	W	0.0	Extrinsic collector Resistance
RBP	W	0.0	Parasitic base Resistance
RE	W	0.0	Emitter Resistance
RS	W	0.0	Substrate Resistance
IS	A	1.0e-16	Transport saturation current
IBEI	A	1.0e-18	Ideal base-emitter saturation current
IBEN	A	0.0	Non-Ideal base-emitter saturation current
IBCI	A	1.0e-16	Ideal base-collector saturation current
IBCN	A	0.0	Non-Ideal base-collector saturation current
ISP	A	0.0	Parasitic transport saturation current
IBEIP	A	0.0	Ideal parasitic base-emitter saturation current
IBENP	A	0.0	Non-Ideal parasitic base-emitter saturation current
IBCIP	A	0.0	Ideal parasitic base-collector saturation current
IBCNP	A	0.0	Non-Ideal base-collector saturation current
ISRR	A	1.0	*Reverse transport saturation current
NF	-	1.0	Forward emission coefficient
NR	-	1.0	Reverse emission coefficient

Table 4-55: VBIC99 Basic Parameters *(Sheet 3 of 5)*

Parameters	Units	Defaults	Descriptions
NEI	-	1.0	Ideal base-emitter emission coefficient
NEN	-	2.0	Non-ideal base-emitter emission coefficient
NCI	-	1.0	Ideal base-collector emission coefficient
NCN	-	2.0	Non-ideal base-collector emission coefficient
NFP	-	1.0	Parasitic forward emission coefficient
NCIP	-	1.0	Ideal parasitic base-collector emission coefficient
NCNP	-	2.0	Ideal parasitic base-collector emission coefficient
NKF	-	0.5	*high current beta roll off parameter
ME	-	0.33	Base-emitter Grading coefficient
MC	-	0.33	Base-collector Grading coefficient
MS	-	0.33	Substrate-collector Grading coefficient
PE	V	0.75	Base-emitter built-in potential
PC	V	0.75	Base-collector built-in potential
PS	V	0.75	Substrate-collector built-in potential
WBE	-	1.0	Portion of IBEI from Vbei, 1-WBE from Vbex
WSP	-	1.0	Portion of ICCP from Vbep, 1-WBE from Vbci
AVC1	1/V	0.0	Base-collector avalanche parameter 1
AVC2	1/V	0.0	Base-collector avalanche parameter 2

Table 4-55: VBIC99 Basic Parameters *(Sheet 4 of 5)*

Parameters	Units	Defaults	Descriptions
VEF	V	0.0	Forward early voltage, zero means infinity
VER	V	0.0	Reverse early voltage, zero means infinity
IKF	A	0.0	Forward knee current, zero means infinity
IKR	A	0.0	Reverse knee current, zero means infinity
IKP	A	0.0	Parasitic knee current, zero means infinity
TF	S	0.0	Forward transit time
QTF	-	0.0	Variation of TF with base-width modulation
XTF	-	0.0	Coefficient of TF bias dependence
VTF	V	0.0	Coefficient of TF dependence on Vbc
ITF	A	0.0	Coefficient of TF dependence on Ic
TR	S	0.0	Reverse transit time
EA	EV	1.12	Activation energy for IS
EAIE	EV	1.12	Activation energy for IBEI
EAIC	EV	1.12	Activation energy for IBCI/IBEIP
EAIS	EV	1.12	Activation energy for IBCIP
EANE	EV	1.12	Activation energy for IBEN
EANC	EV	1.12	Activation energy for IBCN/IBENP
EANS	EV	1.12	Activation energy for IBCNP
VO	V	0.0	Epi drift saturation voltage
GAMM	-	0.0	Epi doping parameter
HRCF	-	0.0	High current RC factor

Table 4-55: VBIC99 Basic Parameters *(Sheet 5 of 5)*

Parameters	Units	Defaults	Descriptions
VRT	V	0.0	*reach-through voltage for Cbc limiting
ART	-	0.1	*smoothing parameter for reach-through
QBM	-	0.0	*base charge model selection
DEAR	-	0.0	*delta activation energy for ISRR
EAP	-	1.12	*activation energy for ISP
VBBE	-	0.0	*base-emitter breakdown voltage
NBBE	-	1.0	* base-emitter breakdown emission coefficient
IBBE	-	1.0e-6	* base-emitter breakdown current
TVBBE1	-	0.0	*linear temperature coefficient of VBBE
TVBBE2	-	0.0	*quadratic temperature coefficient of VBBE
TNBBE	-	0.0	*temperature coefficient of NBBE
EBBE	-	0.0	exp(-VBBE/(NBBE*Vtv))

Table 4-56: VBIC99 Capacitance and Charge Parameters

Parameters	Units	Defaults	Descriptions
FC	-	0.9	Forward bias depletion cap. Limit
CBEO	F	0.0	Extrinsic base-emitter overlap cap.
CJE	F	0.0	Base-emitter zero bias cap.
AJE	-	-0.5	Base-emitter cap. Smoothing factor
CBCO	F	0.0	Extrinsic base-collector overlap cap.

Table 4-56: VBIC99 Capacitance and Charge Parameters *(Continued)*

Parameters	Units	Defaults	Descriptions
CJC	F	0.0	Base-collector zero bias cap.
QCO	Coul	0.0	Epi. charge parameter
CJEP	F	0.0	Base-collector extrinsic zero bias cap
AJC	-	-0.5	Base-collector cap. Smoothing factor
CJCP	F	0.0	Substrate-collector zero bias cap.
AJS	-	-0.5	Substrate-collector cap. Smoothing factor
CCSO	F	0.0	*Fixed collector-substrate capacitance

Table 4-57: VBIC99 Temperature Coefficients

Parameters	Units	Defaults	Descriptions
XRE	-	0.0	Temperature exponent of emitter resistance
XRBI	-	0.0	Temperature exponent of intrinsic base resistance
XRCI	-	0.0	Temperature exponent of intrinsic collector resistance
XRS	-	0.0	Temperature exponent of substrate resistance
XRCX	-	0.0	*Temperature exponent of extrinsic base resistance
XRBX	-	0.0	*Temperature exponent of extrinsic collector resistance
XRBP	-	0.0	*Temperature exponent of parasitic base resistance
XIKF	-	0.0	*Temperature exponent of IKF

Table 4-57: VBIC99 Temperature Coefficients *(Continued)*

Parameters	Units	Defaults	Descriptions
XISR	-	0.0	*Temperature exponent of ISRR
XVO	-	0.0	Temperature exponent of VO
XIS	-	3.0	Temperature exponent of IS
XII	-	3.0	Temperature exponent of IBEI/IBCI/IBEIP/ IBCIP
XIN	-	3.0	Temperature exponent of IBEN/IBCN/ IBENP/IBCNP
TNF	1/K	0.0	Temperature exponent of NF
TAVC	1/K	0.0	Temperature coefficient of AVC2

Table 4-58: VBIC99 Noise Parameters

Parameters	Units	Defaults	Descriptions
AFN	-	1.0	Base-emitter Flicker noise exponent
KFN	-	0.0	Base-emitter Flicker noise constant
BFN	-	1.0	Base-emitter Flicker noise 1/f dependence

Table 4-59: VBIC99 Self-heating Parameters

Parameters	Units	Defaults	Descriptions
RTH	K/W	0.0	Thermal resistance
CTH	J/K	0.0	Thermal capacitance

Table 4-60: VBIC99 Excess Phase Parameter

Parameters	Units	Defaults	Descriptions
TD	S	0.0	Forward excess-phase delay time

Example

```
***** VBIC99 level 9 AC test ******
.option nopage list post=2
+        newtol reli=1e-5 absi=1e-10 relv=1e-5 relvdc=1e-7
+        post gmindc=1e-12

*** common emitter ***
 rt1 t1 0 1meg
 vce1 c1 0 1.9
 vb1 b1 0 dc=0.9 ac=0.01
 vee e1 0 0
 vss s1 0 0
 qe   c1 b1 e1 s1 t1 vbic99

.net i(vce1) vb1 rin=50 rout=50
.model vbic99 npn level=9
+   LEVEL =       9        REF = 300.15          RCX   =   10.26
+   RCI   =   0.001        VO    =       0         GAMM =       0
+   HRCF =       0        RBX   = 122.23         RBI   =   0.001
+   RE    =   17.61        RS    =       1         RBP   =       1
+   IS    =4.70047e-25      NF    = 1.09575         NR    =    1.02
+   FC    =     0.9        CBEO =       0         CJE   =   7e-15
+   PE    =    0.75        ME    =    0.33         AJE   =    -0.5
+   CBCO =       0       CJC   = 1.1e-14          QCO   =       0
+   CJEP =       0        PC    =    0.75         MC    =    0.33
+   AJC   =    -0.5        CJCP =   3e-15         PS    =    0.75
+   MS    =    0.33        AJS   =    -0.5         IBEI =1.484e-23
+   WBE   =       1        NEI   =   1.302         IBEN =6.096e-18
+   NEN   =   2.081        IBCI =5.618e-24         NCI   =    1.11
+   IBCN =3.297e-14        NCN   =       2         AVC1 =       0
+   AVC2 =       0        ISP   =       0         WSP   =       1
+   NFP   =       1        IBEIP =       0         IBENP =       0
+   IBCIP =       0        NCIP =       1         IBCNP =       0
+   NCNP =       2        VEF   =     800         VER   =     700
+   IKF   =       0        IKR   =       0         IKP   =       0
```

```
+   TF    = 2.3e-12         QTF   =       0         XTF   =       0
+   VTF   =       0        ITF   =       0         TR    =       0
+   TD    =   1e-15         KFN   =       0         AFN   =       1
+   BFN   =       1         XRE   =       2         XRBI  =       2
+   XRCI  =       2        XRS   =       2         XVO   =       0
+   EA    = 1.1095          EAIE  =1.489271         EAIC  =1.489271
+   EAIS  =    1.12         EANE  =1.489271         EANC  =1.489271
+   EANS  =    1.12         XIS   =       3         XII   =       3
+   XIN   =       3         TNF   =       0         TAVC  =       0
+   RTH   = 159.177         CTH   =       0         VRT   =       0
+   ART   =     0.1         CCSO  =       0         QBM   =       0
+   NKF   =     0.5         XIKF  =       0         XRCX  =       2
+   XRBX  =       2         XRBP  =       0         ISRR  =       1
+   XISR  =       0         DEAR  =       0         EAP   =    1.12
+   VBBE  =       0         NBBE  =       1         IBBE  =   1e-06
+   TVBBE1=       0         TVBBE2=       0         TNBBE =       0
+   EBBE  =       0

.ac dec 10 100x 20g
.print ac y11(r) y11(i) y11(m) y11(p)
.print ac y12(r) y12(i) y12(m) y12(p)
.print ac y21(r) y21(i) y21(m) y21(p)
.print ac y22(r) y22(i) y22(m) y22(p)
.print v(t1)
.end

---------------------------------------------------------------

***** VBIC99 level9 DC test *****
.options gmin=1.0e-13

vbe bx 0 0
vcb cx bx 0
vib bx b 0
vic cx c 0
rxth dt 0 1e12

ve ex 0 0
vie ex e 0
vs sx 0 0
vis sx s 0

.temp 27
q1 c b e s dt vbic area=1 m=1
.model vbic npn level=9
```

```
+tref = 27.0    rcx = 10.0    rci = 60.0     vo = 2.0
+gamm = 2e-11 hrcf = 2.0    rbx = 10.0     rbi = 40.0
+re = 2.0       rs = 20.0     rbp = 40.0     is = 1.0e-16
+nf = 1.0       nr = 1.0      fc = 0.9       cbeo = 0.0
+cje = 1.0e-13   pe = 0.75     me = 0.33      aje = -0.5
+cbco = 0.0     cjc = 2e-14   qco = 1e-12    cjep = 1e-13
+pc = 0.75      mc = 0.33     ajc = -0.5     cjcp = 4e-13
+ps = 0.75      ms = 0.33     ajs = -0.5     ibei = 1.0e-18
+wbe = 1.0      nei = 1.0     iben = 5.0e-15 nen = 2.0
+ibci = 2.0e-17   nci = 1.0     ibcn = 5.0e-15 ncn = 2.0
+avc1 = 2.0     avc2 = 15.0   isp = 1.0e-15 wsp = 1.0
+nfp = 1.0      ibeip = 0.0   ibenp = 0.0    ibcip = 0.0
+ncip = 1.0     ibcnp = 0.0   ncnp = 2.0     vef = 10.0
+ver = 4.0      ikf = 2e-3    ikr = 2e-4     ikp = 2e-4
+tf = 10e-12    qtf = 0.0     xtf = 20.0     vtf = 0.0
+itf = 8e-2      tr = 100e-12 td = 1e-20
+kfn = 0.0      afn = 1.0     bfn = 1.0      xre = 0
+xrbi = 0       xrci = 0      xrs = 0        xvo = 0
+ea = 1.12      eaie = 1.12   eaic = 1.12    eais = 1.12
+eane = 1.12    eanc = 1.12   eans = 1.12    xis = 3.0
+xii = 3.0      xin = 3.0     tnf = 0.0      tavc = 0.0
+rth = 300.0    cth = 0.0     vrt = 0.0      art = 0.1
+ccso = 0.0     qbm = 0.0     nkf = 0.5
+xikf = 0       xrcx = 0      xrbx = 0       xrbp = 0
+isrr = 1.0     xisr = 0.0    dear = 0.0     eap = 1.12
+vbbe = 0.0     nbbe = 1.0    ibbe = 1.0e-6 tvbbe1 = 0.0
+tvbbe2 = 0.0   tnbbe = 0.0   ebbe = 0.0

.dc vbe 0.5 1.0 0.02
.print dc i(vib) i(vic) i(vie) i(vis) v(dt)

.end

------------------------------------------------------------

***** VBIC99 level 9 Transient test *****
.options numdgt=5 itl1=500 list node post
+ $ i use this line to invoke mwaves

.width out=80
q1 3 2 0 0 t vbic99 tnodeout
.op
.tran 50p 50n
.print tran v(1) v(2) v(3) v(4) v(t)
```

```
v 4 0 dc 5.0
vin 1 0 dc 2.5 pulse (0 5 0 1n 1n 10n 25n)
r1 1 2 100
r2 3 4 10k
rxth t 0 1e12
.model vbic99 npn level=9
+   LEVEL =       9          TREF = 300.15          RCX   =   10.26
+   RCI   =   0.001          VO    =       0         GAMM =       0
+   HRCF =       0          RBX   = 122.23          RBI   =   0.001
+   RE    =   17.61          RS    =       1         RBP   =       1
+   IS    =4.70047e-25       NF    = 1.09575         NR    =    1.02
+   FC    =     0.9          CBEO =       0         CJE   =   7e-15
+   PE    =    0.75          ME    =    0.33         AJE   =    -0.5
+   CBCO =       0          CJC   = 1.1e-14         QCO   =       0
+   CJEP =       0          PC    =    0.75         MC    =    0.33
+   AJC   =    -0.5          CJCP =   3e-15         PS    =    0.75
+   MS    =    0.33          AJS   =    -0.5        IBEI =1.484e-23
+   WBE   =       1          NEI   =   1.302        IBEN =6.096e-18
+   NEN   =   2.081          IBCI =5.618e-24         NCI   =    1.11
+   IBCN =3.297e-14          NCN   =       2          AVC1 =       0
+   AVC2 =       0          ISP   =       0         WSP   =       1
+   NFP   =       1          IBEIP =       0         IBENP =       0
+   IBCIP =       0          NCIP =       1         IBCNP =       0
+   NCNP =       2          VEF   =     800         VER   =     700
+   IKF   =       0          IKR   =       0         IKP   =       0
+   TF    = 2.3e-12          QTF   =       0         XTF   =       0
+   VTF   =       0          ITF   =       0         TR    =       0
+   TD    =   1e-15          KFN   =       0         AFN   =       1
+   BFN   =       1          XRE   =       2          XRBI =       2
+   XRCI =       2          XRS   =       2         XVO   =       0
+   EA    = 1.1095           EAIE =1.489271          EAIC =1.489271
+   EAIS =    1.12           EANE =1.489271          EANC =1.489271
+   EANS =    1.12          XIS   =       3         XII   =       3
+   XIN   =       3          TNF   =       0          TAVC =       0
+   RTH   = 159.177          CTH   =       0         VRT   =       0
+   ART   =     0.1          CCSO =       0         QBM   =       0
+   NKF   =     0.5          XIKF =       0          XRCX =       2
+   XRBX =       2          XRBP =       0          ISRR =       1
+   XISR =       0          DEAR =       0         EAP   =    1.12
+   VBBE =       0          NBBE =       1          IBBE =   1e-06
+   TVBBE1=      0          TVBBE2=      0         TNBBE =       0
+   EBBE =       0
.end
```

VBIC99 Notes for HSPICE Users

1. Set Level to 9, to identify the model as a VBIC99 bipolar junction transistor model.
2. The reference temperature, TREF, equals 27 degrees.
3. The VBIC99 model is not supported with AREA scaling, Multiplication scaling is supported. In HSPICE, the default AREA value is 1.0.
4. Self-heating is enabled for this model. Model parameters are RTH and CTH.

Level 10 Phillips MODELLA Bipolar Model

The Philips MODELLA, Level 10 provides a highly-accurate compact model for lateral pnp integrated circuit transistors. This model is based directly on device physics. It uses a physical modelling approach where the main currents and charges are independently related to bias-dependent minority carrier concentrations. It also models current crowding effects, high injection effect, and a bias-dependent output impedance.

Model Parameters

Table 4-61: BJT Level 10 Transistor Parameters *(Sheet 1 of 5)*

Name (Alias)	Units	Default	Description
LEVEL		10	Model level
IS	A	1.80e-16	A Collector-emitter saturation current
BF		131.00	Ideal forward common-emitter current gain
IBF	A	2.60e-14	A Saturation current of non-ideal forward base current
VLF	V	0.54	V Cross-over voltage of non-ideal forward base current
IK	A	1.10e-4	A High injection knee current
XIFV		0.43	Vertical fraction of forward current
EAFL	V	20.50	Early voltage of the lateral forward current component at zero collector-base bias
EAFV	V	75.00	Early voltage of the vertical forward current component at zero collector-base bias

Table 4-61: BJT Level 10 Transistor Parameters *(Sheet 2 of 5)*

Name (Alias)	Units	Default	Description
BR		25.00	Ideal reverse common-emitter current gain
IBR	A	1.20e-13	Saturation current of non-ideal reverse base current
VLR	V	0.48	Cross-over voltage of non-ideal reverse base current
XIRV		0.43	Vertical fraction of reverse current
EARL	V	13.10	Early voltage of the lateral reverse current component at zero emitter-base bias
EARV	V	104.00	Early voltage of the vertical reverse current component at zero emitter-base bias
XES		2.70e-3	Ratio between saturation current of e-b-s transistor and e-b-c transistor
XHES		0.70	Fraction of substrate current of e-b-s transistor subject to high injection
XCS		3.00	Ratio between the saturation current of c-b-s transistor and c-b-e transistor
XHCS		1.00	Fraction of substrate current of c-b-s transistor subject to high injection
ISS	A	4.00e-13	Saturation current of substrate-base diode
RCEX	W	5.00	External part of the collector resistance
RCIN	W	47.00	Internal part of the collector resistance
RBCC	W	10.00	Constant part of the base resistance RBC
RBCV	W	10.00	Variable part of the base resistance RBC

Table 4-61: BJT Level 10 Transistor Parameters *(Sheet 3 of 5)*

Name (Alias)	Units	Default	Description
RBEC	W	10.00	Constant part of the base resistance RBE
RBEV	W	50.00	Variable part of the base resistance RBE
REEX	W	27.00	External part of the emitter resistance
REIN	W	66.00	Internal part of the emitter resistance
RSB	W	1.00e15	Substrate-base leakage resistance
TLAT	S	2.40e-9	Low injection (forward and reverse) transit time of charge stored in the epilayer between emitter and collector
TFVR	S	3.00e-8	Low injection forward transit time due to charge stored in the epilayer under the emitter
TFN	S	2.00e-10	Low injection forward transit time due to charge stored in the emitter and the buried layer under the emitter
CJE	F	6.10e-14	Zero-bias emitter-base depletion capacitance
VDE	V	0.52	Emitter-base diffusion voltage
PE		0.30	Emitter-base grading coefficient
TRVR	S	1.00e-9	Low injection reverse transit time due to charge stored in the epilayer under the collector
TRN	S	3.00e-9	Low injection reverse transit time due to charge stored in the collector and the buried layer under the collector
CJC	F	3.90e-13	Zero-bias collector-base depletion capacitance
VDC	V	0.57	Collector-base diffusion voltage

Table 4-61: BJT Level 10 Transistor Parameters *(Sheet 4 of 5)*

Name (Alias)	Units	Default	Description
PC		0.36	Collector-base grading coefficient
CJS	F	1.30e-12	Zero-bias substrate-base depletion capacitance
VDS	V	0.52	Substrate-base diffusion voltage
PS		0.35	Substrate-base grading coefficient
TREF	^{o}C	25.00	Reference temperature of the parameter set
DTA	^{o}C	0.00	Difference between the device temperature and the ambient analysis temperature
VGEB	V	1.206	Bandgap voltage of the emitter-base depletion region
VGCB	V	1.206	Bandgap voltage of the collector-base depletion region
VGSB	V	1.206	Bandgap voltage of the substrate-base depletion region
VGB	V	1.206	Bandgap voltage of the base between emitter and collector
VGE	V	1.206	Bandgap voltage of the emitter
VGJE	V	1.123	Bandgap voltage recombination emitter-base junction
AE		4.48	Temperature coefficient of BF
SPB		2.853	Temperature coefficient of the epitaxial base hole mobility
SNB		2.60	Temperature coefficient of the epitaxial base electron mobility

Table 4-61: BJT Level 10 Transistor Parameters *(Sheet 5 of 5)*

Name (Alias)	Units	Default	Description
SNBN		0.30	Temperature coefficient of buried layer electron mobility
SPE		0.73	Temperature coefficient of emitter hole mobility
SPC		0.73	Temperature coefficient of collector hole mobility
SX		1.00	Temperature coefficient of combined minority carrier mobilities in emitter and buried layer
KF		0.00	Flicker noise coefficient
AF		1.00	Flicker noise exponent
EXPHI		0.00	rad Excess phase shift

Equivalent Circuits

Figure 4-16: Large-signal Equivalent Circuit

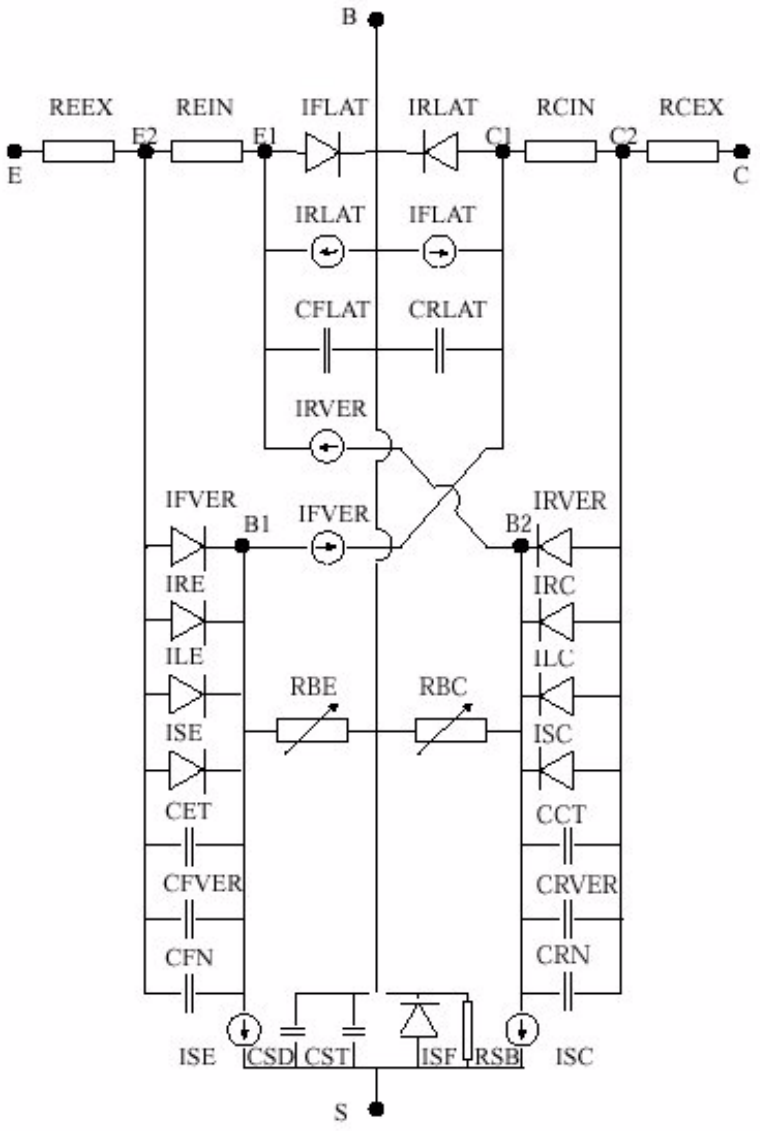
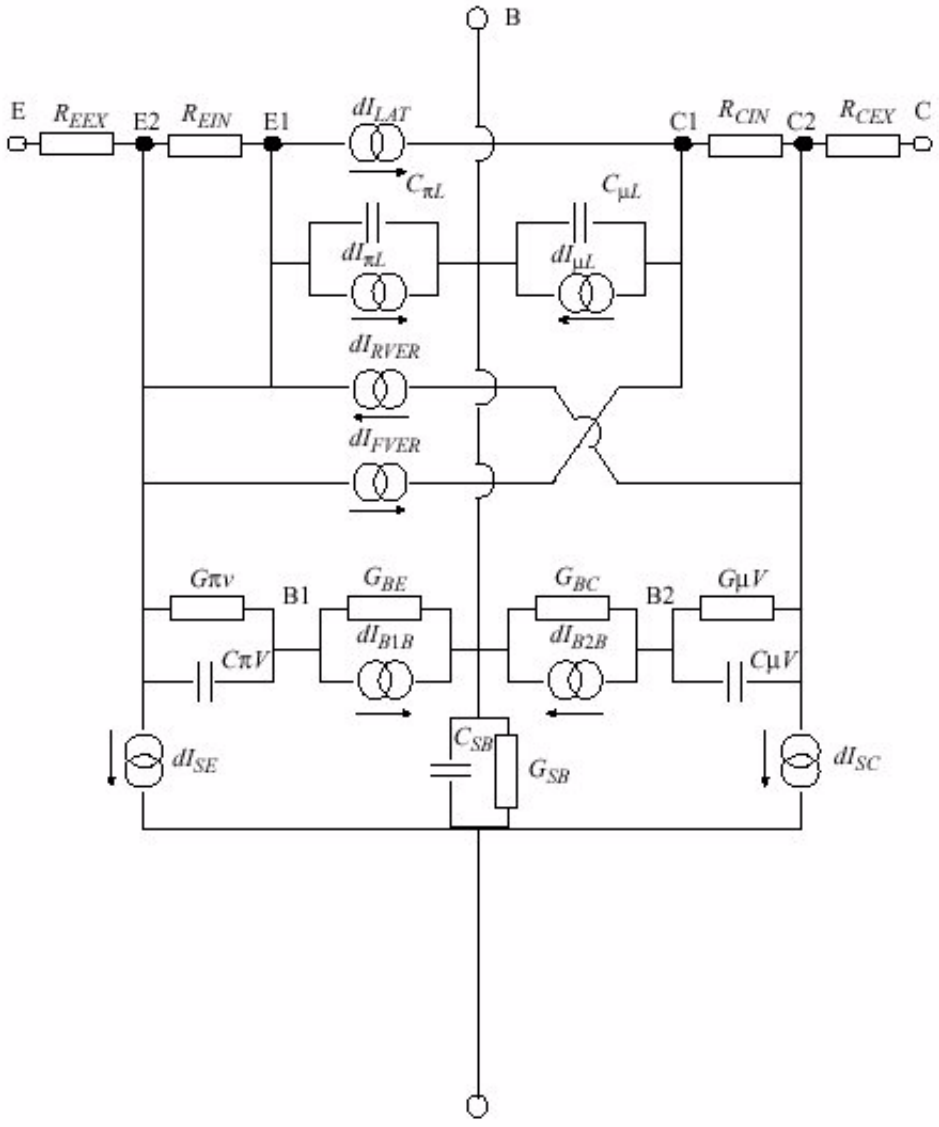


Figure 4-17: Small-signal Equivalent Circuit



DC Operating Point Output

The DC operating point output facility gives information on the state of a device at its operation point. Figure 1 shows the DC large signal equivalent circuit. The small signal equivalent circuit is given in figure 2.

REEX, *REIN*, *RCIN* and *RCEX* are constant resistors.

$$dILAT = g_{fL}\, dV_{E1B} - g_{rL}\, dV_{C1B}$$

$$dIFVER = g_{11}\, dV_{E2B1} + g_{12}\, dV_{C1B}$$

$$dIRVER = g_{21}\, dV_{E1B} + g_{22}\, dV_{C2B2}$$

$$dI_{B1B} = G_{IBE}\, dV_{E2B1}$$

$$dI_{B2B} = G_{IBC}\, dV_{C2B2}$$

$$dI_{\Pi L} = jw\, C_{\Pi L}\, dV_{C1B}$$

$$dI_{\mu L} = jwC_{I\mu L}\, dV_{E1B}$$

$$dISE = G_{ISE}\, dV_{E2B1}$$

$$dISC = G_{ISC}\, dV_{C2B2}$$

Name (Alias)	Description
GFL	Forward conductance, lateral path.: $\partial I_{FLAT} / \partial V_{E1B1}$
GRL	Reverse conductance, lateral path.: $\partial I_{RLAT} / \partial V_{C1B}$
G11	Forward conductance, vertical path.: $\partial I_{FVER} / \partial V_{E2B1}$
G12	Collector Early-effect on I FVER: $\partial I_{FVER} / \partial V_{C1B}$
G21	Emitter Early-effect on I RVER: $\partial I_{RVER} / \partial V_{E1B}$
G22	Reverse conductance, vertical path.: $\partial I_{RVER} / \partial V_{C2B2}$
GPI	Conductance e-b junction: $\partial (I_{RE} + I_{LE}) / \partial V_{E2B1}$
GMU	Conductance c-b junction: $\partial (I_{RC} + I_{LC}) / \partial V_{C2B2}$
GSB	Conductance s-b junction: $\partial I_{SF} / \partial V_{SB} + 1/R_{SB}$

Name (Alias)	Description
CPIL	Forward diffusion cap., lateral path: $\partial Q_{FLAT} / \partial V_{E1B}$
CPIV	Forward total capacitance, vertical path: $\partial (Q_{TE} + Q_{FVER} + Q_{FN}) / \partial V_{E2B1}$
CMUL	Reverse diffusion capacitance, lateral path: $\partial Q_{RLAT} / \partial V_{C1B}$
CMUV	Reverse total capacitance, vertical path: $\partial (Q_{tc} + Q_{rver} + Q_{rn}) / \partial V_{C2B2}$
CSB	Total capacitance s-b junction: $\partial Q_{TS} / \partial V_{SB} + \partial Q_{SD} / \partial V_{SB}$

Model Equations

Early Factors

The Early factors for the components of the main current I_p are derived from the variation of the depletion widths in the base relative to the base width itself.

Early factor of the lateral current components

$$FLAT = hyp_1 \left\{ 1 - \left(\frac{\sqrt[4]{\left(1 - \frac{V_{E1B}}{VD_T}\right)^2 + \delta}}{1 + \frac{EARL}{2VD_T}} - \frac{\sqrt[4]{\left(1 - \frac{V_{C1B}}{VD_T}\right)^2 + \delta}}{1 + \frac{EAFL}{2VD_T}} \right) \cdot \delta_E \right\}$$

Early factor of the forward vertical current component

$$FFVER = hyp_1 \left\{ 1 - \left(\frac{\sqrt[4]{\left(1 - \frac{V_{E2B1}}{VD_T}\right)^2 + \delta}}{1 + \frac{EARV}{2VD_T}} - \frac{\sqrt[4]{\left(1 - \frac{V_{C1B}}{VD_T}\right)^2 + \delta}}{1 + \frac{EAFV}{2VD_T}} \right) \cdot \delta_E \right\}$$

Early factor of the reverse vertical current component

$$FRVER = hyp_1\left\{1-\left(\frac{\sqrt[4]{\left(1-\frac{V_{E1B}}{VD_T}\right)^2+\delta}}{1+\frac{EARV}{2VD_T}}-\frac{\sqrt[4]{\left(1-\frac{V_{C2B2}}{VD_T}\right)^2+\delta}}{1+\frac{EAFV}{2VD_T}}\right)\cdot\delta_E\right\}$$

Model parameters:

- EAFL
- EAFV
- EARL
- EARV

Currents

Ideal diodes

The ideal diode equations are as follows.

$$If1 = Is\left(e^{Ve1b/Vt}-1\right)$$

$$If2 = Is\left(e^{Ve2b1/Vt}-1\right)$$

$$Ir1 = Is\left(e^{Vc1b/Vt}-1\right)$$

$$Ir2 = Is\left(e^{Vc2b2/Vt}-1\right)$$

model parameter: Is

Main current Ip

The main current is as follows.

$$Ip = I_{flat} + I_{fver} - I_{rlat} - I_{rver}$$

Forward currents—Iflat and Ifver

The main forward current is separated into lateral and vertical components, originating from the emitter-base junction sidewall and bottom, respectively. These formulations include Early and high injection effects. Because the two currents depend on different internal emitter-base junction voltages, emitter current crowding is also modelled. The lateral forward current component (Iflat) is:

$$I_{flat} = \left(\frac{4 \times (1 - Xifv) \times If1}{3 + \sqrt{1 + 16 \times \frac{If1}{Ik}}} \right) \div Flat$$

The vertical forward current component (Ifver) is;

$$I_{fver} = \left(\frac{4 \times Xifv \times If2}{3 + \sqrt{1 + 16 \times \frac{If2}{Ik}}} \right) \div Ffver$$

Model parameters:

- Xifv
- Ik

Reverse currents—Irlat and Irver

The main reverse current is separated into lateral and vertical components, originating from the collector-base junction sidewall and bottom, respectively. These formulations include Early and high injection effects. Because the two currents depend on different internal collector-base junction voltages, collector current crowding is also modelled.

The lateral reverse current component (Irlat) is:

$$I_{rlatt} = \left(\frac{4 \times (1 - Xirv) \times Ir1}{3 + \sqrt{1 + 16 \times \frac{Ir1}{Ik}}} \right) \div Flat$$

The vertical reverse current component (Irver) is:

$$I_{rver} = \left(\frac{4 \times Xirv \times Ir2}{3 + \sqrt{1 + 16 \times \frac{Ir2}{Ik}}} \right) \div Frver$$

Model parameter: Xirv

Base Current

Forward components

The total forward base current is composed of an ideal and a non-ideal component. Both components depend on the bottom part of the emitter-base junction.

Ideal component:

$$Ire = \frac{If2}{Bf}$$

Non-ideal component:

$$Ile = \frac{Ibf \times \left(e^{Ve2b1/Vt} - 1 \right)}{e^{Ve2b1/2Vt} + e^{Vlf/2Vt}}$$

Model parameters:

- Bf
- Ibf
- Vif

Reverse components

The total reverse base current is composed of an ideal and a non-ideal component. Both components depend on the bottom part of the collector-base junction.

Ideal component:

$$Irc = \frac{Ir2}{Br}$$

Non-ideal component:

$$Ilc = \frac{Ibr \times \left(e^{Vc2b2/Vt} - 1\right)}{e^{Vc2b2/2Vt} + e^{Vlt/2Vt}}$$

Model parameters:

- Br
- Ibr
- Vlr

Substrate current

Forward components

The forward substrate component depends on the bottom part of the emitter-base junction. It consists of an ideal component, and a component subject to high injection effects. The *XHES* parameter determines the fraction that is subject to high injection.

$$Ise = (1 - Xhes) \times Xes \times If2 + \frac{4 \times Xhes \times Xes \times If2}{3 + \sqrt{1 + 16 \times \frac{If2}{Ik}}}$$

Model parameters:

- Xes
- Xhes

Reverse components

The reverse substrate component depends on the bottom part of the collector-base junction. It consists of an ideal component, and a component subject to high injection effects. The *XHCS* parameter determines the fraction that is subject to high injection.

$$Isc = (1 - Xhcs) \times Xcs \times Ir2 + \frac{4 \times Xhcs \times Xcs \times Ir2}{3 + \sqrt{1 + 16 \times \frac{Ir2}{Ik}}}$$

Model parameters:

- Xcs
- Xhcs

Additional Substrate and Base current

An ideal diode models the substrate-base junction. You can use the reverse leakage current of this junction to model the zero-crossover phenomena, sometimes observed in the base current at low bias conditions and high temperatures.

$$Isf = Iss \times \left(e^{Vsb/Vt} - 1\right)$$

Model parameter: Iss

Charges

Depletion Charges

The Poon-Gummel formulation is used to model the depletion charges.

Emitter-base depletion charge

$$Qte = \frac{-Cje}{1 - Pe} \times \left\{ \frac{Vde - Ve2b1}{\left[\left(1 - \frac{Ve2b1}{Vde}\right)^2 + \delta\right]^{\frac{Pe}{2}}} \right\}$$

Model parameters:

- Cje
- Vde
- Pe

Collector-base depletion charge

$$Qtc = \frac{-Cjc}{1-Pc} \times \left\{ \frac{Vdc - Vc2b2}{\left[\left(1 - \frac{Vc2b2}{Vdc} \right)^2 + \delta \right]^{\frac{Pc}{2}}} \right\}$$

Model parameters:

- Cje
- Vdc
- Pc

Substrate-base depletion charge

$$Qts = \frac{-Cjs}{1-Ps} \times \left\{ \frac{Vds - Vsb}{\left[\left(1 - \frac{Vsb}{Vds} \right)^2 + \delta \right]^{\frac{Ps}{2}}} \right\}$$

Model parameters:

- Cjs
- Vds
- Ps

Forward Stored Charges

Storing forward-active charges consists of three main components.

1. Charge stored in epitaxial base region between emitter and collector:

$$Qflat = Tlat \times Ik \times \left(\sqrt{1 + 16 \times \frac{If1}{Ik}} - 1 \right) \times \frac{Flat}{8}$$

2. Charge stored in epitaxial base region under emitter:

$$Qfver = Tfvr \times Ik \times \left(\sqrt{1 + 16 \times \frac{If2}{Ik}} - 1 \right) \times \frac{1}{8}$$

3. Charge stored in emitter and buried layer under emitter:

$$Qfn = Tfn \times If2$$

Reverse Stored Charges

Storing reverse-active charges consists of three main components.

1. Charge stored in epitaxial base region between emitter and collector:

$$Qrlat = Tlat \times Ik \times \left(\sqrt{1 + 16 \times \frac{Ir1}{Ik}} - 1 \right) \times \frac{Flat}{8}$$

2. Charge stored in epitaxial base region under collector:

$$Qrver = Trvr \times Ik \times \left(\sqrt{1 + 16 \times \frac{Ir2}{Ik}} - 1 \right) \times \frac{1}{8}$$

3. Charge stored in collector and buried layer under collector:

$$Qrn = Trn \times Ir2$$

Substrate-base Stored Charge

Charge stored in the substrate and the base, due to the substrate-base junction. This charge storage occurs only when the substrate-base junction is forward biased:

$$Qsd = Tsd \times Isf$$

Note: Tsd is a constant.

Series Resistances

The emitter includes the following series resistance:

- Reex—constant
- Rein—constant

The collector includes the following series resistance:

- Rcex—constant
- Rcin—constant

The conductivity modulation of the base resistances is derived from the fact that the voltage drop across the epitaxial layer, is inversely proportional to the electron concentration under the emitter and collector.

Base resistance under the emitter:

$$Rbe = Rbec + \frac{2 \times Rbev}{\sqrt{1 + 16 \times \frac{If\,2}{Ik}}}$$

Base resistance under the collector:

$$Rbc = Rbcc + \frac{2 \times Rbcv}{\sqrt{1 + 16 \times \frac{Ir2}{Ik}}}$$

The Rb resistance models the ohmic leakage, across the substrate-base junction.

Noise Equations

For noise analysis current sources are added to the small signal equivalent circuit. In these equations:

- f represents the operation frequency of the transistor.
- Δf is the bandwidth.

When measured at 1 Hz, a noise density is obtained.

Thermal Noise

$$\overline{iN^2_{REEX}} = \frac{4 \cdot k \cdot Tk}{REEX} \cdot \Delta f$$

$$\overline{iN^2_{REIN}} = \frac{4 \cdot k \cdot Tk}{REIN} \cdot \Delta f$$

$$\overline{iN^2_{RCIN}} = \frac{4 \cdot k \cdot Tk}{RCIN} \cdot \Delta f$$

$$\overline{iN^2_{RCEX}} = \frac{4 \cdot k \cdot Tk}{RCEX} \cdot \Delta f$$

$$\overline{iN^2_{RBE}} = \frac{4 \cdot k \cdot Tk}{RBE} \cdot \Delta f$$

$$\overline{iN^2_{RBC}} = \frac{4 \cdot k \cdot Tk}{RBC} \cdot \Delta f$$

$$\overline{iN^2_{RSB}} = \frac{4 \cdot k \cdot Tk}{RSB} \cdot \Delta f$$

Lateral Collector Current Shot Noise

$$\overline{iN^2_{CLAT}} = 2 \cdot q \cdot \left| I_{FLAT} - I_{RLAT} \right| \cdot \Delta f$$

Vertical Collector Current Shot Noise

$$\overline{iN^2_{CVER}} = 2 \cdot q \cdot \left| I_{FVER} - I_{RVER} \right| \cdot \Delta f$$

Forward-base Current Shot Noise and 1/f Noise

$$\overline{iN^2{}_B} = 2 \cdot q \cdot \left| I_{RE} + I_{LE} \right| \cdot \Delta f + \frac{KF \cdot MULT^{1-AF} \cdot \left| I_{RE} + I_{LE} \right|^{AF}}{f} \cdot \Delta f$$

Temperature Dependence of the Parameters

$$Tk = Tref + 273.16$$

$$Tn = \frac{Temp}{Tref + 273.16}$$

$$Ti = \frac{1}{Tref + 273.16} - \frac{1}{Temp}$$

Series Resistance

$$RCIN_T = RCIN \times T_N{}^{SPC}$$

$$RBCC_T = RBCC \times T_N{}^{SNBN}$$

$$RBCV_T = RBCV \times T_N{}^{SNB}$$

$$RBEC_T = RBEC \times T_N{}^{SNBN}$$

$$RBEV_T = RBEV \times T_N{}^{SNB}$$

REEX and RCEX are assumed to be temperature independent.

Depletion Capacitances

$$VDxt = -3k\frac{TEMP}{q}\cdot\ln(T_N) + VDx\cdot T_N + (1-T_N)\cdot Vgap$$

$$CJ_{XT} = CJx\cdot\left(\frac{VDx}{VD_{XT}}\right)^{PX}$$

Emitter-base Junction

Vgap = VGEB, x = E

Collector-base Junction

Vgap = VGCB, x = C

Substrate-base Junction

Vgap = VGSB, x = S

Temperature Dependence of the Other Parameters

$$VD_T = -3k\frac{TEMP}{q}\cdot\ln(T_N) + VD\cdot T_N + (1-T_N)\cdot VGB$$

$$EAFL_T = EAFL\cdot\sqrt{\frac{VD_T}{VD}}$$

$$EARL_T = EARL\cdot\sqrt{\frac{VD_T}{VD}}$$

$$EAFV_T = EAFV\cdot\sqrt{\frac{VD_T}{VD}}$$

$$EARV_T = EARV\cdot\sqrt{\frac{VD_T}{VD}}$$

$$IS_T = IS\cdot T_N^{(4.0-SPB)}\cdot\exp\left(q\cdot VGB\cdot {}^{T_I}\!/_{k}\right)$$

$$BF_T = BF\cdot T_N^{(AE-SPB)}\cdot\exp\left\{q\cdot(VGB-VGE)\cdot {}^{T_I}\!/_{k}\right\}$$

$$IBF_T = IBF\cdot T_N^{2}\cdot\exp\left\{q\cdot(VGJE/2)\cdot {}^{T_I}\!/_{k}\right\}$$

$$IK_T = IK\cdot T_N^{(1-SPB)}$$

$$BR_T = BR\cdot\frac{BF_T}{BF}$$

$$IBR_T = IBR\cdot\frac{IBF_T}{IBF}$$

$$ISS_T = ISS \cdot T_N{}^2 \cdot \exp\left\{q \cdot VGSB \cdot {T_I}/{k}\right\}$$

$$TLAT_T = TLAT \cdot T_N{}^{(SPB-1.0)}$$

$$TFVR_T = TFVR \cdot \frac{TLAT_T}{TLAT}$$

$$TFN_T = TFN \cdot T_N{}^{(SX-1.0)}$$

$$TRVR_T = TRVR \cdot \frac{TLAT_T}{TLAT}$$

$$TRN_T = TRN \cdot \frac{TFN_T}{TFN}$$

All other model parameters are assumed to be temperature-independent.

Level 11 UCSD HBT Model

The UCSD High Speed Devices Group, in collaboration with the HBT Model Working Group, has been developing better SPICE models for heterojunction bipolar transistors (HBTs). The HSPICE implementation of the UCSD HBT MODEL is based on the web site:

http://hbt.ucsd.edu

Using the UCSD HBT Model

1. Set BJT Level=11.
2. The default room temperature is 25^{o} C in the Avant! Star-Hspice and Star-Sim simulators (and their XT versions), but is 27^{o} C in most other simulators. When comparing to other simulators, do one of the following:
   - set the simulation temperature to 27, or
   - set TEMP 27, or
   - set .OPTIONS TNOM=27
3. The *set* model parameter should always include the model reference temperature, TREF. The default value for TREF is 27.
4. You can use DTEMP with this model, to increase the temperature of individual elements, relative to the circuit temperature. Set its value on the element line.
5. The self-heating calculation and thermal terminals have been added in the UCSD HBT Model, but not in the Avant! True-Hspice model.

Description of Parameters

Parameter	Significance	Units	Default
BKDN	flag denoting that BC breakdown should be included	logic	false
TREF	temperature at which model parameters are given	C	27
IS	saturation value for forward collector current	A	1e-25
NF	forward collector current ideality factor	-	1
NR	reverse current ideality factor	-	1
ISA	collector current EB barrier limiting current	A	1e10
NA	collector current EB barrier ideality factor	-	2
ISB	collector current BC barrier limiting current	A	1e10
NB	collector current BC barrier ideality factor	-	2
VAF	forward Early voltage	V	1000
VAR	reverse Early voltage	V	1000
IK	knee current for dc high injection effect	A	1e10
BF	forward ideal current gain	-	10000
BR	reverse ideal current gain	-	10000
ISE	saturation value for non-ideal base current	A	1e-30
NE	ideality factor for non-ideal forward base current	-	2
ISEX	saturation value for emitter leakage diode	A	1e-30
NEX	ideality factor for emitter leakage diode	-	2
ISC	saturation value for intrinsic bc junction current	A	1e-30

Parameter	Significance	Units	Default
NC	ideality factor for intrinsic bc junction current	-	2
ISCX	saturation value for extrinsic bc junction current	A	1e-30
NCX	ideality factor for extrinsic bc junction current	-	2
FA	Factor for specification of avalanche voltage	-	0.9
BVC	collector-base breakdown voltage BVcbo	V	1000
NBC	exponent for BC multiplication factor vs voltage	-	8
ICS	saturation value for collector-substrate current	A	1e-30
NCS	ideality factor for collector-substrate current	-	2
RE	Emitter resistance	ohm	0
REX	Extrinsic emitter leakage diode series resistance	ohm	0
RBX	Extrinsic base resistance	ohm	0
RBI	Intrinsic base resistance	ohm	0
RCX	Extrinsic collector resistance	ohm	0
RCI	Intrinsic collector resistance	ohm	0
CJE	BE depletion capacitance at zero bias	F	0
VJE	BE diode built-in potential for Cj estimation	V	1.6
MJE	Exponent for voltage variation of BE Cj	-	0.5
CEMIN	Minimum BE capacitance	F	0
FCE	Factor for start of high bias BE Cj approximation	-	0.8
CJC	Intrinsic BC depletion capacitance at zero bias	F	0

Parameter	Significance	Units	Default
VJC	Intrinsic BC diode built-in potential for Cj estimation	V	1.4
MJC	Exponent for voltage variation of Intrinsic BC Cj	-	0.33
CCMIN	Minimum value of intrinsic BC Cj	F	0
FC	Factor for start of high bias BC Cj approximation	-	0.8
CJCX	Extrinsic BC depletion capacitance at zero bias	F	0
VJCX	Extrinsic BC diode built-in potential for Cj estimation	V	1.4
MJCX	Exponent for voltage variation of Extrinsic BC Cj	-	0.33
CXMIN	Minimum extrinsic Cbc	F	0
XCJC	Factor for partitioning extrinsic BC Cj	-	1
CJS	Collector-substrate depletion capacitance (0 bias)	F	0
VJS	CS diode built-in potential for Cj estimation	V	1.4
MJS	Exponent for voltage variation of CS Cj	-	0.5
TFB	Base transit time	S	0
TBEXS	Excess BE heterojunction transit time	S	0
TBCXS	Excess BC heterojunction transit time	S	0
TFC0	Collector forward transit time	S	0
ICRIT0	Critical current for intrinsic Cj variation	A	1e3

Parameter	Significance	Units	Default
ITC	Characteristic current for TFC	A	0
ITC2	Characteristic current for TFC	A	0
VTC	Characteristic voltage for TFC	V	1e3
TKRK	Forward transit time for Kirk effect	S	0
VKRK	Characteristic Voltage for Kirk effect	V	1e3
IKRK	Characteristic current for Kirk effect	A	1e3
TR	Reverse charge storage time, intrinsic BC diode	S	0
TRX	Reverse charge storage time, extrinsic BC diode	S	0
FEX	Factor to determine excess phase	-	0
KFN	BE flicker noise constant	-	0
AFN	BE flicker noise exponent for current	-	1
BFN	BE flicker noise exponent for frequency	-	1
XTI	Exponent for IS temperature dependence	-	2
XTB	Exponent for beta temperature dependence	-	2
TNE	Coefficient for NE temperature dependence	-	0
TNC	Coefficient for NC temperature dependence	-	0
TNEX	Coefficient for NEX temperature dependence	-	0
EG	Activation energy for IS temperature dependence	V	1.5
EAE	Activation energy for ISA temperature dependence	V	0

Parameter	Significance	Units	Default
EAC	Activation energy for ISB temperature dependence	V	0
EAA	Added activation energy for ISE temp dependence	V	0
EAB	Added activation energy for ISC temp dependence	V	0
EAX	Added activation energy for ISEX temp dependence	V	0
XRE	Exponent for RE temperature dependence	-	0
XREX	Exponent for REX temperature dependence	-	0
XRB	Exponent for RB temperature dependence	-	0
XRC	Exponent for RC temperature dependence	-	0
TVJE	Coefficient for VJE temperature dependence	V/C	0
TVJCX	Coefficient for VJCX temperature dependence	V/C	0
TVJC	Coefficient for VJC temperature dependence	V/C	0
TVJS	Coefficient for VJS temperature dependence	V/C	0
XTITC	Exponent for ITC temperature dependence	-	0
XTITC2	Exponent for ITC2 temperature dependence	-	0
XTTF	Exponent for TF temperature dependence	-	0
XTTKRK	Exponent for TKRK temperature dependence	-	0
XTVKRK	Exponent for VKRK temperature dependence	-	0
XTIKRK	Exponent for IKRK temperature dependence	-	0

Model Equations

Current Flow

This section describes seven different current flow calculations for the Avant! True-Hspice Level 11 BJT model.

Intrinsic collector current contributions

This model computes the electron flow between Ei and Ci nodes, using equations similar to the Gummel-Poon model, with modifications to take into account the potential spike that can appear at the base-emitter or base-collector junctions of HBTs. This model separates the electron current into forward and reverse components, Icf and Icr.

$$Icf = IS * [\exp(qVbei/NF/KT) - 1] / D$$

$$Icr = IS * [\exp(qVbci/NR/KT) -1] / D$$

In these equations:

$$D= qb + IS* \exp(qVbei/NA/KT) / ISA + IS*\exp(qVbci/NB/KT)/ISB$$

ISA, ISB, NA and NB are new parameters. ISA and ISB approximate the transition currents, from base-transport controlled, to potential-barrier controlled, current flow.

qb partially retains the form of the standard BJT model (representing a fractional increase in the base charge associated with the bias changes).

$$qb= q1/2 * [1+(1+4*q2)^{0.5}]$$

$$q1=1/ [1 - Vbci/VAF -Vbei/VAR]$$

$$q2=IS/IK*[\exp(qVbei/NF/KT)-1]$$

qb omits the reverse knee current contribution. As noted below, qb is not used to define the ac model in the fashion of the Gummel-Poon model.

The total collector current Icc is:

$$Icc=Icf - Icr$$

This formulation uses the IS, NF, VAF, VAR, and IK parameters, established in the SPICE BJT model, in addition to the ISA, ISB, NA, and NB parameters described above.

Intrinsic Base-Emitter Diode

Ideal and non-ideal components are included:

$$Ibei = Icf / BF + ISE * [\exp (q\ Vbei / NE / KT) - 1]$$

Extrinsic Base-Emitter Diode

The Level 11 model includes a diode connected between the Ex and E nodes, and an associated series resistance, Rex. You can use the diode and its resistance together, to model contributions from emitter edges.

$$Ibex = ISEX * [\exp (q\ Vbex / NEX / KT) - 1]$$

Intrinsic Base-Collector Diode

Ideal and non-ideal components are included:

$$Ibci = Icr / BR + ISC * [\exp (q\ Vbci / NC / KT) - 1]$$

Intrinsic Base-Collector Breakdown Current

Ibk is current between the collector and base nodes, generated due to avalanche breakdown of the base-collector junction. If you set the BKDN parameter to **true**, then *Ibk* is determined according to:

$$Ibk = (Mf - 1) * Icf$$

Otherwise, $Ibk = 0$

where:

- Mf is the multiplication factor associated with the BC junction at the specified voltage.
- Icf is the forward electron current (as computed above, in the absence of multiplication).

Mf is calculated with a physically based expression, modified to avoid the singularity at Vbci=-BVC.

Mf depends exclusively on the intrinsic base-intrinsic collector voltage, Vbci. If -Vbci closely approaches or exceeds BVC (-Vbci>FA*BVC, with FA typically chosen to be 0.95), then the multiplication factor is computed according to a constant slope expression.

$$Mf = 1 / [1- (-Vbci/BVC)^NBC] \text{ for } KTop/q< -Vbci < FA*BVC$$

$$Mf = 1 \text{ for } -Vbci > KTop/q$$

$$Mf = Mfl + gl *(-Vbci-FA*BVC) \text{ for } -Vbci > FA*BVC$$

where Mfl and gl are the values of Mf and its derivative, with respect to voltage, evaluated at the voltage -Vbci=FA*BVC:

$$Mfl=1 / (1-FA^NBC)$$

$$gl = Mfl*(Mfl-1)*NBC/(FA*BVC)$$

Extrinsic Base-Collector Diode

This diode has customary I-V characteristics, with its own saturation current and ideality factor.

$$Ibcx= ISCX * [exp(q Vbcx/ NCX /KTop) - 1]$$

Substrate-Extrinsic Collector Diode

This diode allows for conducting substrates, and is primarily of interest for SiGe HBTs.

$$Ics= ICS * [exp(-q Vcs/ NCS /KTop) - 1]$$

In accordance with the model topology, the external currents through the E,B, and C nodes are:

$$Ib= Ibei + Ibex - Ibk + Ibci + Ibcx$$

$$Ic= Icc + Ibk -Ibci-Ibcx - Ics$$

Charge Storage

This section describes five different charge storage calculations for the Avant! True-Hspice Level 11 BJT model.

Base-Emitter Charge

The overall charge stored at the base-emitter junction has components associated with the base-emitter depletion layer:

- Qbej, which is current independent.
- Qbediff, a collector current-dependent charge. Qbediff corresponds to a portion of the base charge, and the (collector-current dependent) base-collector charge.

$$Qbe = Qbej + Qbediff$$

.Base-Emitter Depletion Charge, Qbej

The depletion charge, Qbej, follows equations standard for SPICE, modified to allow specification of a minimum capacitance CEMIN (corresponding to reach-through to an n+ layer). It should be noted that (as studied by Chris Grossman) there is frequently an extra component of charge storage at the base-emitter heterojunction of HBTs, associated with a minimum in the conduction band energy profile.

Qbej is computed using DepletionCapMod.

Define

$$Vmin = VJE*[1-(CJE/CEMIN)^{(1/MJE)}]$$

(the critical voltage for attaining the minimum capacitance value)

If Vbei<FCE*VJE and Vbei<Vmin:

$$Qbej=CEMIN*(Vbei-VJE)+CEMIN*VJE*MJE/(MJE-1) * (CJE/CEMIN)^{(1/MJE)}$$

$$Cbej=dQbej/dVbei=CEMIN$$

If Vbei<FCE*VJE and Vbei>Vmin:

$$Qbej= -CJE*VJE*(1-Vbei/VJE)^{(1-MJE)} / (1-MJE)$$

$$Cbej= CJE*(1-Vbei/VJE)^{(-MJE)}$$

If Vbei>FCE*VJE, and CJE>CEMIN*(1-FCE)^{MJE}:

$$Qbej=-CJE*VJE/(1-FCE)^{MJE}*[(1-FCE)/(1-MJE)+FCE-Vbei/VJE$$

$$-MJE*(FCE-Vbei/VJE)^2/2/(1-FCE)]$$

$$Cbej=CJE/(1-FCE)^{MJE}*[1+MJE*(Vbei/VJE-FCE)/(1-FCE)]$$

If Vbei>FCE*VJE, and CJE<CEMIN*(1-FCE)^{MJE},

$$Qbej=CEMIN*(Vbei-VJE)+CEMIN*VJE*MJE/(MJE-1)$$

$$*(CJE/CEMIN)^{(1/MJE)}+CJE*VJE*(Vbei/VJE-FCE)^2*MJE/2/(1-FCE)^{(MJE+1)}$$

$$Cbej=CEMIN + CJE*VJE*MJE*(Vbei/VJE-FC)/(1-FCE)^{(MJE+1)}$$

.Base-Emitter Diffusion Charge, Qbediff

The diffusion charge in HBTs is associated with contributions from minority carriers in the base, and from mobile charge in the collector depletion region. In homojunction transistors, diffusion charge storage in the emitter is also present. The Level 11 model evaluates the base and collector-depletion region contributions separately (if necessary, the emitter charge storage can be associated with the base contribution).

The base charge is specified through the base transit time, TFB. This transit time varies with bias through several mechanisms:

1. The Early effect causes a change in transit time with junction voltage.
2. In heterojunction transistors, there is frequently a minimum in the conduction band, on the base side of the base-emitter (and potentially base-collector) heterojunction. Minority carriers tend to accumulate in these potential wells.

The stored charge adds to the base charge (to a good approximation). In the lowest order, the charge stored is directly proportional to the collector current, and thus contributes to TFB. For a greater degree of accuracy, the depth of the potential well on the emitter side varies with Vbe. Similarly, the amount of charge stored at the base-collector side varies with Vbc.

The equations used to describe the effects are:

$$TFBt=TFB*(1+Vbei/VAR+Vbci/VAF) + TBEXS*exp(-q(Vbei-VJE)/NA/KTop)$$

$$+ TBCXS*exp(q(Vbci-VJC)/NB/KTop)$$

Note: Different signs are associated with the BE and BC junction effects. The value of the T temperature to describe these effects is assumed to be Top.

The collector charge is specified through three separate mechanisms:

1. A part is specified by the TFC0 transit time parameter, modified by the qcc velocity modulation factor to account for voltage and current dependences.
2. A part of the mobile charge is specified in the calculation of base-collector depletion region charge. To calculate this part, Qbcm, an expression for the collector current-dependent base-collector depletion charge is developed. Then the current-independent part is subtracted off (as discussed in the next section).
3. A separate charge term, Qkrk, is associated with the Kirk effect.

$$Qfdiff = Icf*ftt*(TFBt + TFC0/qcc) + Qbcm + Qkrk$$

$$ftt=rT^{XTTF}$$

qcc is a factor describing bias dependence of electron velocity in the BC depletion region:

$$qcc= [1 + (Icf/ITC)^2] / [1 + (Icf/ITC2)^3 + (VJCI-Vbci)/VTC]$$

- ITC is the threshold current for the velocity profile modulation effect.
- ITC2 is a higher current at which the velocity profile modulation peaks (and the cutoff frequency begins to roll-off).
- VTC provides a voltage (or electric field) dependence of the carrier velocity.

$$ITC=ITC@Tnom* rT^{XTITC}$$

$$ITC2=ITC2@Tnom* rT^{XTITC2}$$

The following expression calculates the charge storage associated with the Kirk effect:

$$Qkrk=TKRK*Icf*exp[Vbci/VKRK+Icf/IKRK]$$

To account for excess phase, a fraction (1-FEX) of the current-dependent forward charge (Qfdiff) is associated with the BE junction, while the remainder is associated with the intrinsic BC junction.

$$Qbediff= (1-FEX)*Qfdiff$$

Note: Qfdiff (and thus Qbediff) depends on Vbci, through the terms involving Icf, qcc, Qkrk and Qbcm. As a result, a trans-capacitance is implied in the ac model. Similarly, Qbcdiff depends on Vbei, implying another trans-capacitance.

Intrinsic Base-Collector Charge, Qbci

Charge stored at the intrinsic base-collector junction includes:

- Depletion charge from the junction region.
- Diffusion charge associated with normal operation of the transistor.
- Diffusion charge associated with reverse operation of the device.

$$Qbci=Qbcj + TRI* Icr + FEX*Qfdiff$$

Although the charge in the depletion region is dependent on Ic, this section this section describes the portion corresponding to the condition Ic=0. Subsequently, the proper Ic dependent contribution will be considered, and included in Qbcm (a charge that is part of Qfdiff).

.Intrinsic base-collector depletion charge, Qbcj

When Ic=0, the depletion charge is calculated using the same algorithm as applied to Qbej (which accounts for a minimum of capacitance when the n-collector is depleted).

.Intrinsic base-collector diffusion charge

For reverse operation, a diffusion capacitance is implied by the TRI term in the Qbci equation. Here TRI is the effective reverse transit time, which is assumed to be bias-independent. The associated reverse diffusion capacitance is:

$$Cbcrdiff = TRI * dIbci/dVbci$$

For forward operation, diffusion capacitance is also included, in a manner similar to base-emitter capacitance, with a partitioning specified by the excess phase factor, FEX. The terms associated with

$$Icf*ftt*(TFB + TFC0/qcc) + Qkrk$$

have already been discussed above for the calculation of Qbediff. The next section considers the Qbcm portion.

.Qbcm

This charge is the difference between the “proper” Icf-dependent charge in the BCi depletion region (called Qbcf), and the BCi depletion charge computed above (Qbcj) under the assumption that Icf=0.

$$Qbcm=Qbcf - Qbcj$$

To properly compute Qbcf, a formulation of the depletion region charge (similar to that used above) is used, with the modification that the CJ parameter (zero bias capacitance) can depend on the Icf collector current. This corresponds to the physical phenomenon of varying charge density in the depletion region, as a result of the mobile electron charge in that region.

The current-dependent CJ parameter is termed CJCH, and has the form:

$$CJCH= CJC*sign(1-Icf/ICRIT)*ABS(1-Icf/ICRIT)^{MJC}$$

In this equation, ICRIT is a critical current, at which the effective charge density in the BC depletion region vanishes (and the capacitance Cbci drops dramatically). ICRIT is dependent on temperature and bias conditions, according to:

$$ICRIT=ICRIT0*qcc/ftt$$

where `ftt` and `qcc` are the temperature-dependence, and `Icf` and `Vcb` are the dependence parameters described above.

Using this formulation, the current dependence of the BC capacitance is included (although it is partially assigned to the BE junction charge, and partially to the BC junction, through the FEX excess-phase parameter).

You can extract ICRIT and associated parameters from measurements of Cbc vs Ic.

Note: These parameters also control some of the components of the forward transit time.

A delay time is associated with specifying ICRIT:

$$TFC1 = CJC*VJC*MJC/(MJC-1)/ICRIT$$

Use the ICRIT parameter carefully, generally in conjunction with selecting TFC0 and CJCI, in such a way that the sum TFB + TFC0 + TFC1 provide a reasonable estimate of charge storage, similar to TF in Gummel-Poon SPICE.

Extrinsic Base-Collector Charge, Qbcx

The Qbcx stored charge consists of a depletion charge and a diffusion charge.

Standard SPICE does not use the diffusion charge component. However, this component can be an important contribution to saturation stored-charge in many HBTs (in addition to the contribution associated with the intrinsic base-collector junction).

The corresponding charge storage time, TRX, might be different from the intrinsic time, TRI. This difference occurs because of implant-induced recombination, surfaces, or other structural changes.

The depletion charge is corresponds to a standard depletion region expression (without considering charge density modulation due to current), modified to allow for a minimum value of capacitance under a reach-through condition. Furthermore, as indicated below, if you assign a value other than unity to the XCJC variable, then the depletion charge is partitioned between the Bx-Cx capacitance and the B-Cx capacitance.

$$Qbcx= TRX*Ibcx + XCJC*Qbcxo$$

where Qbcxo is the depletion charge.

As a result the dependences of Ibcx on Vbcx, a diffusion capacitance results from the formulation:

$$Cbcxdiff= TRX* dIbcx/dVbcx$$

Base-Extrinsic Collector Charge (Qbcxx), and Treatment of XCJC

In standard Spice, XCJC indicates the fraction of overall Cbc depletion capacitance that should be associated with the intrinsic base node. The remaining fraction (1-XCJC) is attached to the base terminal. HBT Spice uses a similar assignment: the depletion charge associated with the extrinsic base-collector junction is partitioned between the Bx node and the B node:

$$Qbcx= TRX*Ibcx + XCJC* Qbcxo$$

has been defined above, between the Bx and Cx nodes, and charge

$$Qbcxx= (1-XCJC)*Qbcxxo$$

is assigned between the B and Cx nodes. The Qbcxxo charge is computed with the same algorithm as for Qbcxo, using Vbcxx (rather than Vbcx) as the voltage.

Collector-Substrate Charge, Qcs

This corresponds to a depletion charge, formulated in the standard SPICE fashion:

For Vcs>-FC*VJS,

$$Qcs= - CJS*VJS*(1+Vcs/VJS)^{(1-MJS)} / (1-MJS)$$

$$Ccs=CJS*(1+Vcs/VJS)^{(-MJS)}$$

For Vcs<-FC*VJS,

$$Qcs= -CJS*VJS/(1-FC)^{MJS}*$$
$$[(1-FC)/(1-MJS) + FC +Vcs/VJS -MJS/2/(1-FC) *(FC+Vcs/VJS)^2]$$

$$Ccs=CJS*(1-FC)^{(-MJS)}*[1-MJS/(1-FC)*(FC+Vcs/VJS)\}$$

Noise

The Level 11 model includes noise current generators, similar to those in standard Spice. The noise current generators have magnitudes in units of A^2/Hz, and are computed based on 1Hz bandwidth. The noise sources are placed in parallel with corresponding linearized elements, in the small signal model. Sources of 1/f noise have magnitudes that vary with the frequency (f); you can use a BFN exponent, if you do not observe the exact f^{-1} behavior.

$$inc2 = 2*q*Icc$$

$$inb2= 2 * q *Ibe + KFN * Ibe^{AFN} / f^{BFN}$$

$$inre2= 4 * K* Td / RE$$

$$inrbx2= 4 * K * Td / RBX$$

$$inrbi2= 4 * K * Td / RBI$$

$$inrcx2= 4 * K * Td / RCX$$

$$inrci2= 4 * K * Td / RCI$$

$$inrex2= 4 * K * Td / REX$$

Equivalent Circuit

Figure 4-18: Circuit Diagram for Large-signal HBT Model

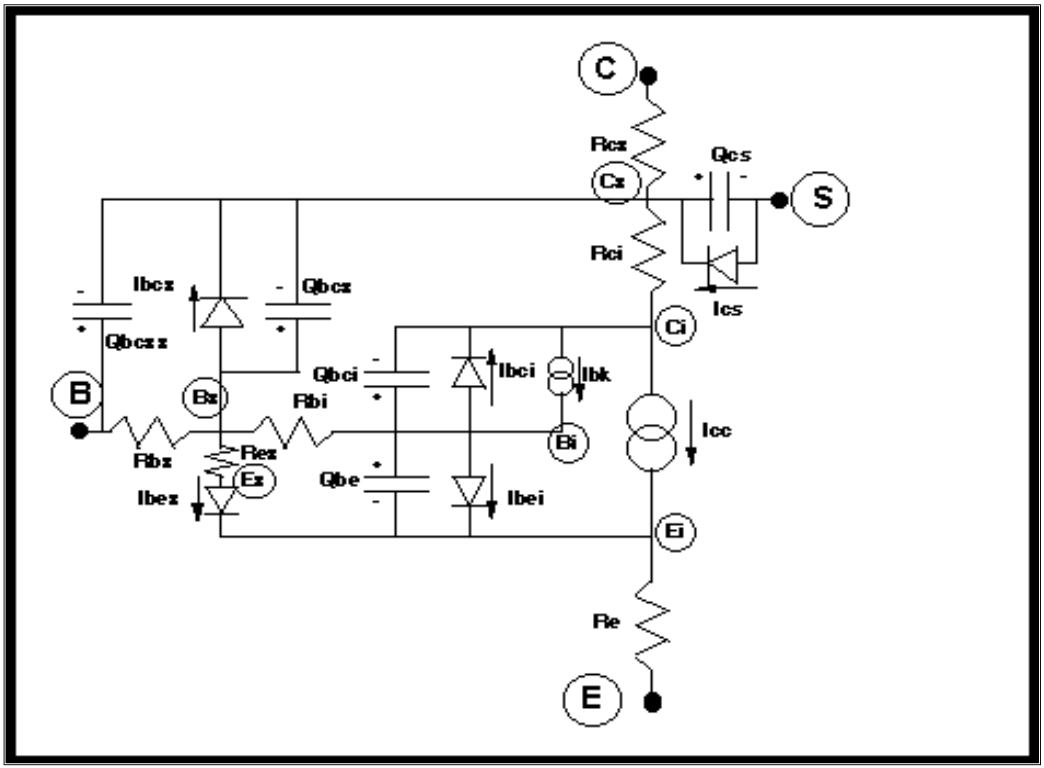
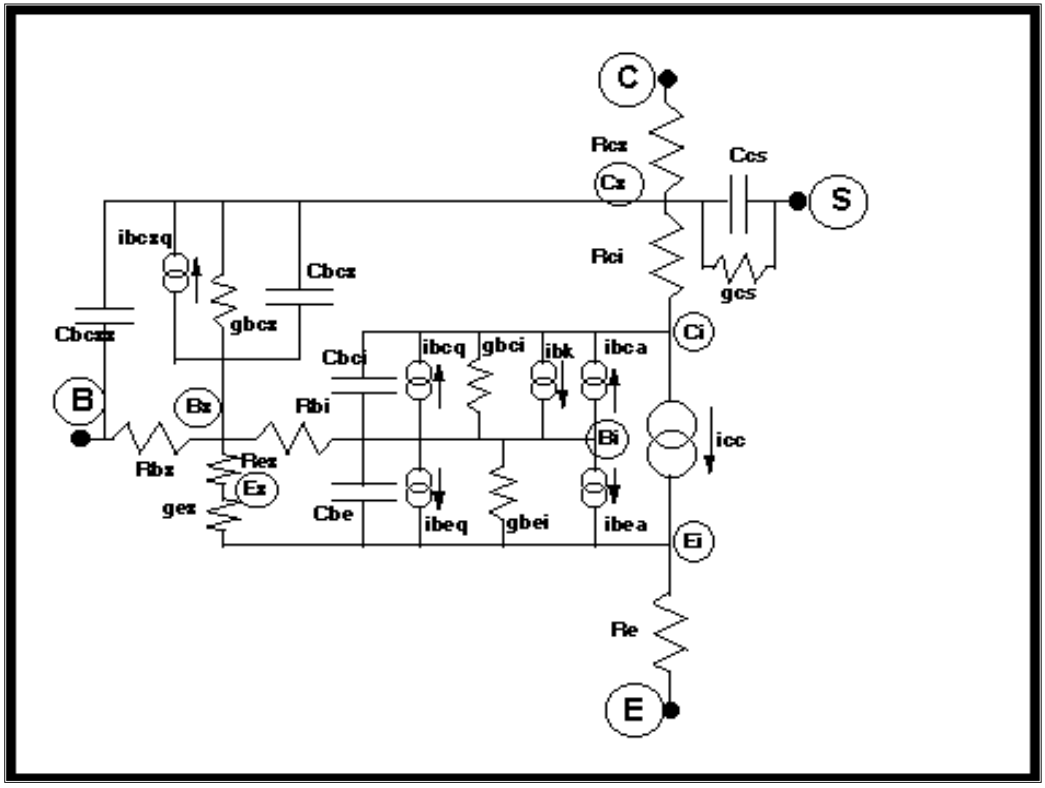


Figure 4-19: Circuit Diagram for Small-signal HBT Model



Example Avant! True-Hspice Model Statement

```
.model hbt npn level=11
+IS     = 1.2E-18  NF     = 1      NR   = 1       BF    = 200
+BR     = 5        VAF    = 60     VAR  = 20      ISE   = 1E-17
+NE     = 1.4      ISEX   = 4E-24  NEX  = 1.3     ISCX  = 1E-14
+NCX    = 2        ISC    = 1E-16  NC   = 2       NA    = 10
+ISA    = 2.18E-10 NB     = 10     ISB  = 1E10    RE    = 16
+REX    = 20       RBI    = 20     BVC  = 28      NBC   = 6
+FA     = 0.995    RCX    = 30     RCI  = 20      CJE   = 1.8E-14
+VJE    = 1.45     CXMIN  = 1E-16  MJE  = 0.5     FC    = 0.8
+ICRIT0 = 0.23     CCMIN  = 3E-15  TR   = 3.5E-10 VJCX  = 1.4
+CJCX   = 8E-15    MJCX   = 0.35   XCJC = 1       VJS   = 1.4
+CJS    = 5E-16    MJS    = 0.01   CTH  = 1E-6    RTH   = 0
+EG     = 1.645    XTI    = 0      XTB  = -1.8    EAA   = -0.495
+EAB    = -0.1     EAE    = 0.105  TNE  = 0       EAC   = 0.34
+XTTF   = 1.5      ICS    = 1E-30  NCS  = 2       CEMIN = 1E-15
+FCE    = 0.8      TFB    = 2E-12  TFC0 = 2.5E-11 TBEXS = 1E-14
+ITC    = 7E-3     ITC2   = 0.014  VTC  = 40      TKRK  = 5E-13
+VKRK   = 10       IKRK   = 0.012  TRX  = 3.5E-10 FEX   = 0
+XTITC  = 1.5      XTITC2 = 1      TREF = 25      CJC   = 7E-15
+VJC    = 1.4      MJC    = 0.35
```

Avant!

Chapter 5
Using JFET and MESFET Models

Avant! provides three JFET/MESFET DC model levels for in-circuit simulation. The same basic equations are used for both gallium arsenide MESFETs and silicon-based JFETs. This is possible because special materials definition parameters are included in these models. These models are also useful in modeling indium phosphide MESFETs.

This chapter covers the following topics:

Understanding JFETs

JFETs are formed by diffusing a gate diode between the source and drain, while MESFETs are formed by applying a metal layer over the gate region, and creating a Schottky diode. Both technologies control the flow of carriers by modulating the gate diode depletion region. These field effect devices are called bulk semiconductor devices and are in the same category as bipolar transistors. Compared to surface effect devices such as MOSFETs, bulk semiconductor devices tend to have higher gain because bulk semiconductor mobility is always higher than surface mobility.

Enhanced characteristics of JFETs and MESFETs, relative to surface effect devices, include lower noise generation rates and higher immunity to radiation. These advantages have created the need for newer and more advanced models.

Features for JFET and MESFET modeling include:

- Charge-conserving gate capacitors
- Backgating substrate node
- Mobility degradation due to gate field
- Computationally efficient DC model (Curtice and Statz)
- Subthreshold equation
- Physically correct width and length (ACM)

The GaAs model Level=3[1] assumes that GaAs device velocity saturates at very low drain voltages. This model includes drain voltage induced threshold modulation and user-selectable materials constants. These features let you use the model for other materials such as silicon, indium phosphide, and gallium aluminum arsenide.

The Curtice model[2] has been revised, and the TriQuint model (TOM) is implemented as an extension of the earlier Statz model.

---

[1]GaAs FET Device and Circuit Simulation in SPICE, *IEEE Transactions on Electron Devices*, Volume ED-34.

[2]A MESFET Model for Use in the Design of GaAs Integrated Circuits, *IEEE Transactions on Microwave Theory*, Vol. MTT-28 No. 5.

Specifying a Model

To specify a JFET or MESFET model use a JFET element statement and a JFET model statement. The model parameter Level selects either the JFET or MESFET model. Level=1 and Level=2 select the JFET, and Level=3 selects the MESFET. Different submodels for the MESFET Level=3 equations are selected using the parameter SAT.

Level=1	SPICE model
Level=2	Modified SPICE model, gate modulation of LAMBDA
Level=3	Hyperbolic tangent MESFET model (Curtice, Statz, Meta, TriQuint Models)
SAT=0	Curtice model (Default)
SAT=1	Curtice model with user defined VGST exponent
SAT=2	Cubic approximation of Curtice model with gate field degradation (Statz model)
SAT=3	Avant! variable saturation model

The CAPOP model parameter selects the type of capacitor model:

CAPOP=0	SPICE depletion capacitor model
CAPOP=1	Charge conserving, symmetric capacitor model (Statz)
CAPOP=2	Avant! improvements to CAPOP=1

You can use CAPOP=0, 1, 2 for any model level. CAPOP=1 and 2 are most often used for the MESFET Level 3 model.

The model parameter ACM selects the area calculation method:

ACM=0	SPICE method (default)
ACM=1	Physically based method

Example

1. The following example selects the n channel MESFET model, Level=3. It uses the SAT, ALPHA, and CAPOP=1 parameter:

```
J1 7 2 3 GAASFET
.MODEL GAASFET NJF Level=3 CAPOP=1 SAT=1 VTO=-2.5
+ BETA=2.8E-3 LAMBDA=2.2M RS=70 RD=70 IS=1.7E-14
+ CGS=14P CGD=5P UCRIT=1.5 ALPHA=2
```

2. The following example selects an n-channel JFET:

```
J2 7 1 4 JM1
.MODEL JM1 NJF (VTO=-1.5, BETA=5E-3, CGS=5P, CGD=1P,
+ CAPOP=1 ALPHA=2)
```

3. The following example selects a p-channel JFET:

```
J3 8 3 5 JX
.MODEL JX PJF (VTO=-1.2, BETA=.179M, LAMBDA=2.2M
+ CGS=100P CGD=20P CAPOP=1 ALPHA=2)
```

Understanding the Capacitor Model

The SPICE depletion capacitor model (CAPOP=0) uses a diode-like capacitance between source and gate, where the depletion region thickness (and therefore the capacitance) is determined by the gate-to-source voltage. A similar diode model is often used to describe the normally much smaller gate-to-drain capacitance.

These approximations have serious shortcomings such as:

1. *Zero source-to-drain voltage:* The symmetry of the FET physics gives the conclusion that the gate-to-source and gate-to-drain capacitances should be
equal, but in fact they can be very different.
2. *Inverse-biased transistor:* Where the drain acts like the source and the source acts like the drain. According to the model, the large capacitance should be between the original source and gate; but in this circumstance, the large capacitance is between the original drain and gate.

When low source-to-drain voltages inverse biased transistors are involved, large errors can be introduced into simulations. To overcome these limitations, use the Statz charge-conserving model by selecting model parameter CAPOP=1. The model selected by CAPOP=2 contains further improvements.

Model Applications

MESFETs are used to model GaAs transistors for high speed applications. Using MESFET models, transimpedance amplifiers for fiber optic transmitters up to 50 GHz can be designed and simulated.

Control Options

Control options that affect the simulation and design of both JFETs and MESFETs include:

DCAP	Capacitance equation selector
GMIN, GRAMP, GMINDC	Conductance options
SCALM	Model scaling option
DCCAP	Invokes capacitance calculation in DC analysis

Table 5-1: JFET Options

Function	Control Options
capacitance	DCAP, DCCAP
conductance	GMIN, GMINDC, GRAMP
scaling	SCALM

Override a global depletion capacitance equation selection that uses the .OPTION DCAP=<*val*> statement in a JFET or MESFET model by including DCAP=<*val*> in the device's .MODEL statement.

Convergence

Enhance convergence for JFET and MESFET by using the GEAR method of computation (.OPTIONS METHOD=GEAR), when you include the transit time model parameter. Use the options GMIN, GMINDC, and GRAMP to increase the parasitic conductance value in parallel with pn junctions of the device.

Capacitor Equations

The DCAP option selects the equation used to calculate the gate-to-source and gate-to-drain capacitance for CAPOP=0. DCAP can be set to 1, 2 or 3. The default is 2.

JFET and MESFET Equivalent Circuits

Scaling

The AREA and M Element parameters, together with the SCALE and SCALM control options, control scaling. For all three model levels, the model parameters IS, CGD, CGS, RD, RS, BETA, LDEL, and WDEL, are scaled using the same equations.

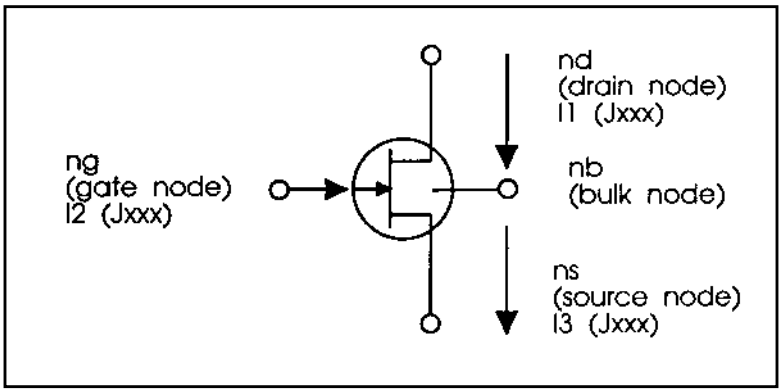
Scaled parameters A, L, W, LDEL, and WDEL, are affected by the SCALM option. SCALM defaults to 1.0. To enter the W parameter with units in microns, for example, set SCALM to 1e-6, then enter W=5. The default setting is W=5e-6 meters, or 5 microns.

Override global scaling that uses the .OPTION SCALM=<val> statement in a JFET or MESFET model by including SCALM=<val> in the .MODEL statement.

Understanding JFET Current Convention

The direction of current flow through the JFET is assumed in Figure 5-1. You can use either I(Jxxx) or I1(Jxxx) syntax when printing the drain current. I2 references the gate current and I3 references the source current. Jxxx is the device name. Figure 5-1 represents the current convention for an n channel JFET.

Figure 5-1: JFET Current Convention, N-Channel



For a p-channel device, the following must be reversed:

- Polarities of the terminal voltages vgd, vgs, and vds
- Direction of the two gate junctions
- Direction of the nonlinear current source id

JFET Equivalent Circuits

Avant! in-circuit simulation uses three equivalent circuits to analyze JFETs: transient, AC, and noise circuits. The components of these circuits form the basis for all element and model equation discussion.

The fundamental component in the equivalent circuit is the drain to source current (ids). For noise and AC analyses, the actual ids current is not used. Instead, the partial derivatives of ids with respect to the terminal voltages, vgs, and vds are used.

The names for these partial derivatives are:

Transconductance

$$gm = \left.\frac{\partial(ids)}{\partial(vgs)}\right|_{vds = const.}$$

Output Conductance

$$gds = \left.\frac{\partial(ids)}{\partial(vds)}\right|_{vgs = const.}$$

The ids equation accounts for all DC currents of the JFET. The gate capacitances are assumed to account for transient currents of the JFET equations. The two diodes shown in Figure 5-2 are modeled by these ideal diode equations:

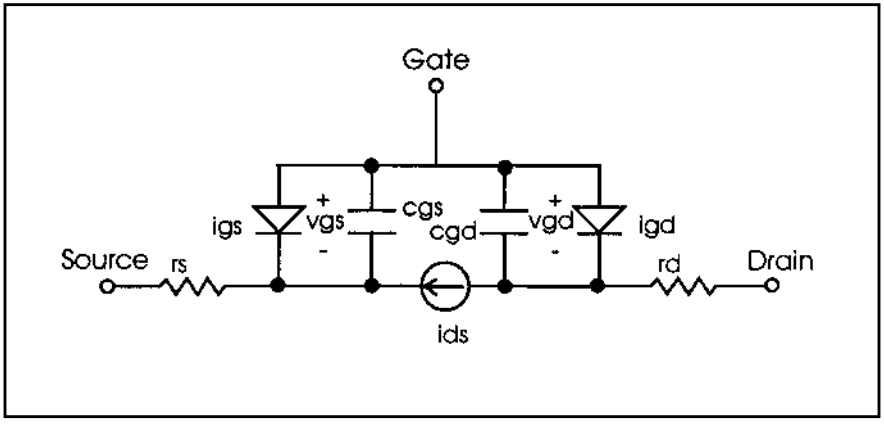
$$igd = ISeff \cdot \left(e^{\frac{vgd}{N \cdot vt}} - 1\right) \quad vgd > -10 \cdot N \cdot vt$$

$$igd = -ISeff \quad vgd \leq -10 \cdot N \cdot vt$$

$$igs = ISeff \cdot \left(e^{\frac{vgs}{N \cdot vt}} - 1\right) \quad vgs > -10 \cdot N \cdot vt$$

$$igs = -ISeff \quad vgs \leq -10 \cdot N \cdot vt$$

Figure 5-2: JFET/MESFET Transient Analysis



Note: For DC analysis, the capacitances are not part of the model.

Figure 5-3: JFET/MESFET AC Analysis

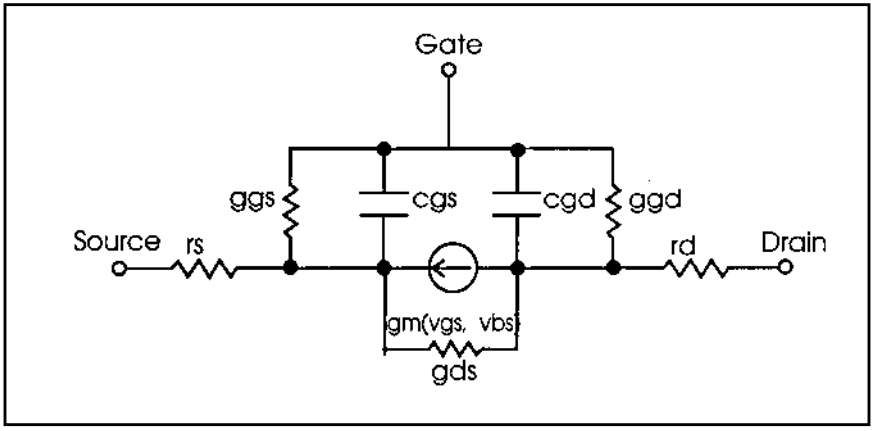


Figure 5-4: JFET/MESFET AC Noise Analysis

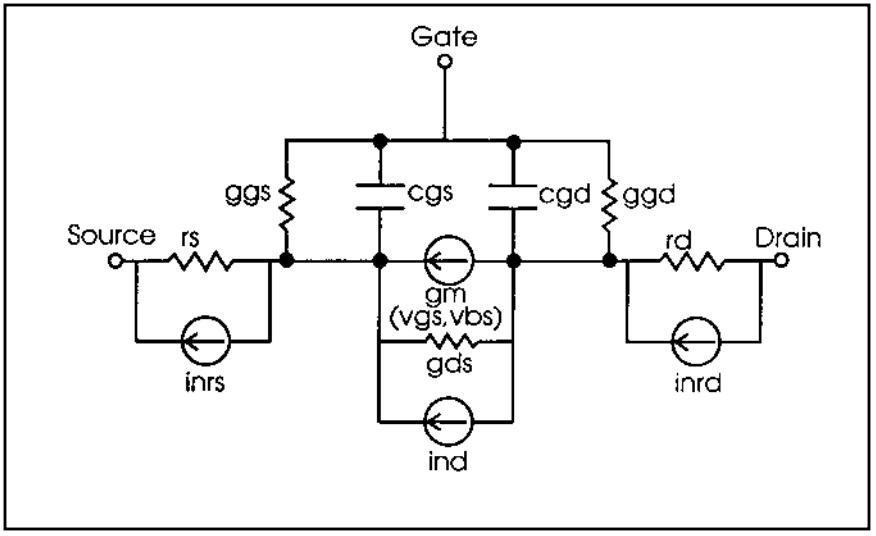


Table 5-2: Equation Variable Names and Constants

Variable/ Quantity	Definitions
cgd	Gate to drain capacitance
cgs	Gate to source capacitance
ggd	Gate to drain AC conductance
ggs	Gate to source AC conductance
gds	Drain to source AC conductance controlled by vds
gm	Drain to source AC transconductance controlled by vgs
igd	Gate to drain current
igs	Gate to source current
ids	DC drain to source current
ind	Equivalent noise current drain to source
inrd	Equivalent noise current drain resistor
inrs	Equivalent noise current source resistor
rd	Drain resistance
rs	Source resistance
vgd	Internal gate-drain voltage
vgs	Internal gate-source voltage
f	Frequency
ε_0	Vacuum permittivity = 8.854e-12 F/m
k	1.38062e-23 (Boltzmann’s constant)
q	1.60212e-19 (electron charge)

Table 5-2: Equation Variable Names and Constants *(Continued)*

Variable/ Quantity	Definitions
t	Temperature in °K
Dt	t - tnom
tnom	Nominal temperature of parameter measurements in °K (user-input in °C). Tnom = 273.15 + TNOM
vt(t)	k · t/q
vt(tnom)	k · tnom/q

JFET and MESFET Model Statements

Syntax

```
.MODEL mname NJF <Level = val> <pname1 = val1> ...
.MODEL mname PJF <Level = val> <pname1 = val1> ...
```

mname	Model name. Elements refer to the model by this name.
NJF	Identifies an N-channel JFET or MESFET model
Level	The Level parameter selects different DC model equations.
pname1=val1	Each JFET or MESFET model can include several model parameters.
PJF	Identifies a P-channel JFET or MESFET model

JFET and MESFET Model Parameters

DC characteristics are defined by the model parameters VTO and BETA. These parameters determine the variation of drain current with gate voltage. LAMBDA determines the output conductance, and IS, the saturation current, of the two gate junctions. Two ohmic resistances, RD and RS, are included. The charge storage is modeled by nonlinear depletion-layer capacitances for both gate junctions that vary as the -M power of junction voltage, and are defined by the parameters CGS, CGD, and PB.

Use parameters KF and AF to model noise, which is also a function of the series source and drain resistances (RS and RD), in addition to temperature. Use the parameters ALPHA and A to model MESFETs.

The AREA model parameter is common to both the element and model parameters. The AREA element parameter always overrides the AREA model parameter.

Table 5-3: JFET and MESFET Model Parameters

Model Parameters Common to All Levels	
Geometric	ACM, ALIGN, AREA, HDIF, L, LDEL, LDIF, RD, RG, RS, RSH, RSHG, RSHL, W, WDEL
Capacitance	CAPOP, CGD, CGS, FC, M, PB, TT
Subthreshold	ND, NG
Noise	AF, KF
Level=1 Model Parameters (JFET)	
DC	BETA, IS, LAMBDA, N, VTO
Level=2 Model Parameters (JFET)	
DC	BETA, IS, LAMBDA, LAM1, N, VTO
Level=3 Model Parameters (MESFET)	
DC	ALPHA, BETA, D, GAMDS, IS, N, K1, LAMBDA, NCHAN, SAT, SATEXP, UCRIT, VBI, VGEXP, VP, VTO

The following subsections provide information about:

- Gate Diode DC Parameters
- DC Model Level 1 Parameters
- DC Model Level 2 Parameters
- DC Model Level 3 Parameters
- ACM (Area Calculation Method) Parameter Equations

Gate Diode DC Parameters

Table 5-4: Gate Diode DC Parameters

Name (Alias)	Units	Default	Description
ACM			Area calculation method. Use this parameter to select between traditional SPICE unitless gate area calculations, and the newer style of area calculations (see the ACM section). If W and L are specified, AREA becomes: ACM=0 AREA=Weff/Leff ACM=1 AREA=Weff · Leff
ALIGN	m	0	Misalignment of gate
AREA			Default area multiplier. This parameter affects the BETA, RD, RS, IS, CGS, and CGD model parameters. AREAeff=M · AREA Override this parameter using the element effective area.
HDIF	m	0	Distance of the heavily diffused or low resistance region from source or drain contact to lightly doped region
IS	amp	1.0e-14	Gate junction saturation current ISeff = IS · AREAeff
L	m	0.0	Default length of FET. Override this parameter using the element L. Leff = L · SCALM + LDELeff
LDEL	m	0.0	Difference between drawn and actual or optical device length LDELeff = LDEL · SCALM

Table 5-4: Gate Diode DC Parameters *(Continued)*

Name (Alias)	Units	Default	Description
LDIF	m	0	Distance of the lightly doped region from heavily doped region to transistor edge
N		1.0	Emission coefficient for gate-drain and gate-source diodes
RD	ohm	0.0	Drain ohmic resistance (see the ACM section) RDeff = RD /AREAeff, ACM=0
RG	ohm	0.0	Gate resistance (see the ACM section) RGeff = RG · AREAeff, ACM=0
RS	ohm	0.0	Source ohmic resistance (see the ACM section) RSeff = RS /AREAeff, ACM=0
RSH	ohm/sq	0	Heavily doped region, sheet resistance
RSHG	ohm/sq	0	Gate sheet resistance
RSHL	ohm/sq	0	Lightly doped region, sheet resistance
W	m	0.0	Default width of FET. Override this parameter using the element W. Weff = W · SCALM + WDELeff
WDEL	m	0.0	Difference between drawn and actual or optical device width WDELeff = WDEL · SCALM

Gate Capacitance Level 1, 2, and 3 Parameters

Table 5-5: Gate Capacitance Parameters

Name (Alias)	Units	Default	Description
CAPOP		0.0	Capacitor model selector: ■ CAPOP=0 – default capacitance equation based on diode depletion layer ■ CAPOP=1 – symmetric capacitance equations (Statz) ■ CAPOP=2 – Avant! improvement to CAPOP=1
CALPHA	ALPHA		Saturation factor for capacitance model (CAPOP=2 only)
CAPDS	F	0	Drain to source capacitance for TriQuint model $\text{CAPDSeff}=\text{CAPDS}\cdot\frac{\text{Weff}}{\text{Leff}}\cdot\text{M}$
CGAMDS	GAMDS		Threshold lowering factor for capacitance (CAPOP=2 only)
CGD	F	0.0	Zero-bias gate-drain junction capacitance CGDeff = CGD · AREAeff Override this parameter by specifying GCAP.
CGS	F	0.0	Zero-bias gate-source junction capacitance $\texttt{CGSeff} = \texttt{CGS}\cdot\texttt{AREAeff}$ Override this parameter by specifying GCAP

Table 5-5: Gate Capacitance Parameters *(Continued)*

Name (Alias)	Units	Default	Description
CRAT		0.666	Source fraction of gate capacitance (used with GCAP)

GCAP	F		Zero-bias gate capacitance. If specified,
			`CGSeff = GCAP · CRAT · AREAeff`
			and
			`CGDeff = GCAP · (1-CRAT) · AREAeff`

FC		0.5	Coefficient for forward-bias depletion capacitance formulas (CAPOP=0 and 2 only)
CVTO	VTO		Threshold voltage for capacitance model (CAPOP=2 only)
M (MJ)		0.50	Grading coefficient for gate-drain and gate-source diodes (CAPOP=0 and 2 only) 0.50 - step junction 0.33 - linear graded junction
PB	V	0.8	Gate junction potential
TT	s	0	Transit time – option METHOD=GEAR is recommended when using transit time for JFET and MESFET

Note: Many DC parameters (such as VTO, GAMDS, ALPHA) can also affect capacitance.

DC Model Level 1 Parameters

Table 5-6: DC Level 1 Parameters

Name (Alias)	Units	Default	Description
Level		1.0	Level=1 invokes the SPICE JFET model
BETA	amp/ V^2	1.0e-4	Transconductance parameter, gain $BETAeff = BETA \cdot \frac{Weff \cdot M}{Leff}$
LAMBDA	1/V	0.0	Channel length modulation parameter
ND	1/V	0.0	Drain subthreshold factor (typical value=1)
NG		0.0	Gate subthreshold factor (typical value=1)
VTO	V	-2.0	Threshold voltage. If set, it overrides internal calculation. A negative VTO is a depletion transistor regardless of NJF or PJF. A positive VTO is always an enhancement transistor.

DC Model Level 2 Parameters

Table 5-7: DC Level 2 Parameters

Name (Alias)	Units	Default	Description
Level		1.0	Level of FET DC model. Level=2 is based on modifications to the SPICE model for gate modulation of LAMBDA.
BETA	amp / V^2	1.0e-4	Transconductance parameter, gain $BETAeff = BETA \cdot \frac{Weff \cdot M}{Leff}$

Table 5-7: DC Level 2 Parameters *(Continued)*

Name (Alias)	Units	Default	Description
LAMBDA	1/V	0.0	Channel length modulation parameter
LAM1	1/V	0.0	Channel length modulation gate voltage parameter
ND	1/V	0.0	Drain subthreshold factor (typical value=1)
NG		0.0	Gate subthreshold factor (typical value=1)
VTO	V	-2.0	Threshold voltage. When set, VTO overrides internal calculation. A negative VTO is a depletion transistor regardless of NJF or PJF. A positive VTO is always an enhancement transistor.

DC Model Level 3 Parameters

Table 5-8: DC Level 3 Parameters

Name (Alias)	Units	Default	Description
Level		1.0	Level of FET DC model. Level=3 is the Curtice MESFET model.
A	m	0.5µ	Active layer thickness $Aeff = A \cdot SCALM$
ALPHA	1/V	2.0	Saturation factor
BETA	amp / V^2	1.0e-4	Transconductance parameter, gain $BETAeff = BETA \cdot \frac{Weff \cdot M}{Leff}$
D		11.7	Semiconductor dielectric constant: Si=11.7, GaAs=10.9
DELTA		0	Ids feedback parameter of TriQuint model
GAMDS *(GAMMA)*		0	Drain voltage, induced threshold voltage lowering coefficient
LAMBDA	1/V	0.0	Channel length modulation parameter
K1	$V^{1/2}$	0.0	Threshold voltage sensitivity to bulk node
NCHAN	atom/ cm^3	1.552e16	Effective dopant concentration in the channel
ND	1/V	0.0	Drain subthreshold factor
NG		0.0	Gate subthreshold factor (typical value=1)

Table 5-8: DC Level 3 Parameters *(Continued)*

Name (Alias)	Units	Default	Description
SAT		0.0	Saturation factor ■ SAT=0 (standard Curtice model) ■ SAT= (Curtice model with hyperbolic tangent coefficient) ■ SAT=2 (cubic approximation of Curtice model (Statz))
SATEXP		3	Drain voltage exponent
UCRIT	V/cm	0	Critical field for mobility degradation
VBI		1.0	Gate diode built-in voltage
VGEXP (Q)		2.0	Gate voltage exponent
VP			Dinch-off voltage (default is calculated)
VTO	V	-2.0	Threshold voltage. If set, it overrides internal calculation. A negative VTO is a depletion transistor regardless of NJF or PJF. A positive VTO is always an enhancement transistor.

ACM (Area Calculation Method) Parameter Equations

The JFET model parameter ACM lets you select between traditional SPICE unitless gate area calculations and the newer style of area calculations. The ACM=0 method (SPICE) uses the ratio of W/L to keep AREA unitless. The ACM=1 (Avant!) model requires parameters such as IS, CGS, CGD, and BETA to have proper physics-based units.

In the following equations, lower case “m” indicates the element multiplier.

ACM=0

$$AREAeff = \frac{Weff}{Leff} \cdot m$$

$$RDeff = \frac{RD}{AREAeff}$$

$$RSeff = \frac{RS}{AREAeff}$$

$$RGeff = RG \cdot \frac{AREAeff}{m^2}$$

ACM=1

$$AREAeff = Weff \cdot Leff \cdot m$$

$$RDeff = \frac{RD}{m}$$

Or if RD=0,

$$RDeff = RSH \cdot \frac{HDIF}{Weff \cdot m} + RSHL \cdot \frac{LDIF + ALIGN}{Weff \cdot m}$$

$$RGeff = \frac{RG}{m}$$

or if RG=0,

$$RGeff = RSHG \cdot \frac{Weff}{Leff \cdot m}$$

$$RSeff = \frac{RS}{m}$$

or if RS=0,

$$RSeff = RSH \cdot \frac{HDIF}{Weff \cdot m} + RSHL \cdot \frac{LDIF - ALIGN}{Weff \cdot m}$$

Resulting calculations

$$ISeff = IS \cdot AREAeff$$

$$CGSeff = CGS \cdot AREAeff$$

$$CGDeff = CGD \cdot AREAeff$$

$$BETAeff = BETA \cdot \frac{Weff}{Leff} \cdot m$$

Note: The model parameter units for IS, CGS, CGD, are unitless in ACM=0 and per square meter for ACM=1.

Example

```
j1 10 20 0 40 nj_acm0 w=10u l=1u
j2a 10 20 0 41 nj_acm1 w=10u l=1u

.model nj_acm0 njf Level=3 capop=1 sat=3 acm=0
+ is=1e-14 cgs=1e-15 cgd=.3e-15
$$$note different units for is,cgs,cgd
+ rs=100 rd=100 rg=5 beta=5e-4
+ vto=.3 n=1 ng=1.4 nd=1
+ k1=.2 vgexp=2 alpha=4 ucrit=1e-4 lambda=.1
+ satexp=2
+ eg=1.5 gap1=5e-4 gap2=200 d=13

.model nj_acm1 njf Level=3 capop=1 sat=3 acm=1
+ is=1e-2 cgs=1e-3 cgd=.3e-3
$$$note different units for is,cgs,cgd
+ rs=100 rd=100 rg=5 beta=5e-4
+ vto=.3 n=1 ng=1.4 nd=1
+ k1=.2 vgexp=2 alpha=4 ucrit=1e-4 lambda=.1
+ satexp=2
+ eg=1.5 gap1=5e-4 gap2=200 d=13
```

JFET and MESFET Capacitances

Gate Capacitance CAPOP=0

The DCAP option switch selects the diode forward bias capacitance equation:

DCAP=1

- Reverse Bias:

vgd < FC · PB

$$cgd = CGDeff \cdot \left(1 - \frac{vgd}{PB}\right)^{-M}$$

vgs < FC · PB

$$cgs = CGSeff \cdot \left(1 - \frac{vgs}{PB}\right)^{-M}$$

- Forward Bias:

vgd FC· PB

$$cgd = TT \cdot \frac{\partial igd}{\partial vgd} + CGDeff \cdot \frac{1 - FC \cdot (1 + M) + M \cdot \frac{vgd}{PB}}{(1 - FC)^{M+1}}$$

vgs FC· PB

$$cgs = TT \cdot \frac{\partial igs}{\partial vgs} + CGSeff \cdot \frac{1 - FC \cdot (1 + M) + M \cdot \frac{vgs}{PB}}{(1 - FC)^{M+1}}$$

DCAP=2 (Default)

- Reverse Bias:

vgd < 0

$$cgd = CGDeff \cdot \left(1 - \frac{vgd}{PB}\right)^{-M}$$

vgs < 0

$$cgs = CGSeff \cdot \left(1 - \frac{vgs}{PB}\right)^{-M}$$

■ Forward Bias:

vgd 0

$$cgd = TT \cdot \frac{\partial igd}{\partial vgd} + CGDeff \cdot \left(1 + M \cdot \frac{vgd}{PB}\right)$$

vgs 0

$$cgs = TT \cdot \frac{\partial igs}{\partial vgs} + CGSeff \cdot \left(1 + M \cdot \frac{vgs}{PB}\right)$$

DCAP=3

Limits peak depletion capacitance to FC · CGDeff or FC · CGSeff, with proper fall-off when forward bias exceeds PB (FC ≥ 1).

Gate Capacitance CAPOP=1

Gate capacitance CAPOP=1 is a charge conserving symmetric capacitor model most often used for MESFET model Level 3.

$$Cgs = \frac{CGS}{4\sqrt{1 - \frac{vnew}{PB}}} \cdot \left[1 + \frac{veff - vte}{\sqrt{(veff - vte)^2 + (0.2)^2}}\right] \cdot$$

$$\left[1 + \frac{vds}{\sqrt{vds^2 + \left(\frac{1}{ALPHA}\right)^2}}\right] + \left[\frac{CGD}{2} \cdot \left(1 - \frac{vds}{\sqrt{vds^2 + \left(\frac{1}{ALPHA}\right)^2}}\right)\right]$$

$$Cgd = \left(\frac{CGS}{4\sqrt{1-\frac{vnew}{PB}}} \cdot \left[1 + \frac{veff - vte}{\sqrt{(veff - vte)^2 + (0.2)^2}} \right] \cdot \left[1 - \frac{vds}{\sqrt{vds^2 + \left(\frac{1}{ALPHA}\right)^2}} \right] \right) +$$

$$\left(\frac{CGD}{2} \cdot \left[1 + \frac{vds}{\sqrt{vds^2 + \left(\frac{1}{ALPHA}\right)^2}} \right] \right)$$

where:

$$vte = VTO + GAMDS \cdot vds + K1(vbs) = \text{effective threshold}$$

$$veff = \frac{1}{2}\left[vgs + vgd + \sqrt{vds^2 + \left(\frac{1}{ALPHA}\right)^2} \right]$$

and:

$$vnew = \frac{1}{2}[veff + vte + \sqrt{(veff - vte)^2 + (0.2)^2}]$$

```
CGD = High -vds Cgd at vgs = 0
CGS = High -vds Cgs at vgs = 0
CGD - CGDeff
CGS - CGSeff
```

Gate Capacitance CAPOP=2

The Statz capacitance equations[3] (CAPOP=1) contain mathematical behavior that has been found to be problematic when trying to fit data.

- For vgs below the threshold voltage and Vds>0 (normal bias condition), Cgd is greater than Cgs and rises with Vds, while Cgs drops with Vds.

[3]H. Statz, P.Newman, I.W.Smith, R.A. Pucel, and H.A. Haus, *GaAs FET Device and Circuit Simulation in Spice.*

- Although Cgd properly goes to a small constant representing a sidewall capacitance, Cgs drops asymptotically to zero with decreasing Vgs.
- (For the behavior for Vds<0, interchange Cgs and Cgd and replace Vds with -Vds in the above descriptions.)
- It can be difficult to simultaneously fit the DC characteristics and the gate capacitances (measured by S-parameters) with the parameters that are shared between the DC model and the capacitance model.
- The capacitance model in the CAPOP=1 implementation also lacks a junction grading coefficient and an adjustable width for the Vgs transition to the threshold voltage. The width is fixed at 0.2.
- Finally, an internal parameter for limiting forward gate voltage is set to $0.8 \cdot PB$ in the CAPOP=1 implementation. This is not always consistent with a good fit.

The CAPOP=2 capacitance equations help to solve the problems described above.

CAPOP=2 Parameters

Parameter	Default	Description
CALPHA	ALPHA	Saturation factor for capacitance model
CGAMDS	GAMDS	Threshold lowering factor for capacitance
CVTO	VTO	Threshold voltage for capacitance model
FC	0.5	PB multiplier – typical value 0.9 gate diode limiting voltage=FC · PB.
M (MJ)	0.5	Junction grading coefficient
VDEL	0.2	Transition width for Vgs

Capacitance Comparison (CAPOP=1 and CAPOP=2)

Figure 5-5 and Figure 5-6 show comparisons of CAPOP=1 and CAPOP=2. Note in Figure 5-5 that below threshold (-0.6 v) Cgs for CAPOP=2 drops towards the same value as Cgd, while for CAPOP=1, CGS $\rightarrow$ 0.

In Figure 5-6, the Cgs-Cgd characteristic curve “flips over” below the threshold for CAPOP=1, whereas for CAPOP=2, it is well-behaved.

Figure 5-5: CAPOP=1 vs. CAPOP=2. Cgs, Cgd vs. Vgs for Vds=0, 1, 2, 3, 4

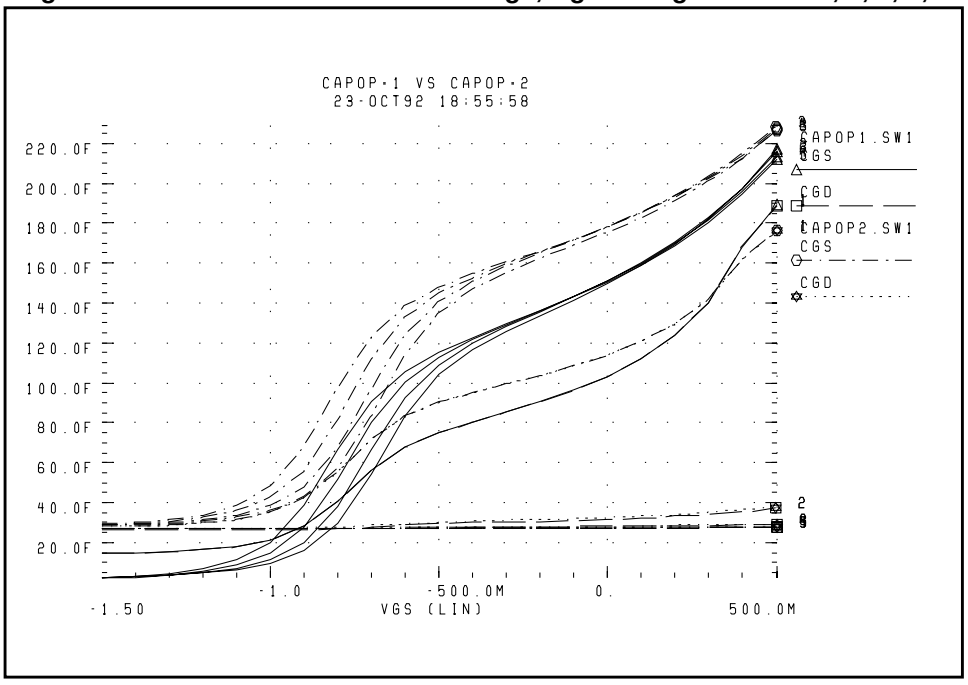
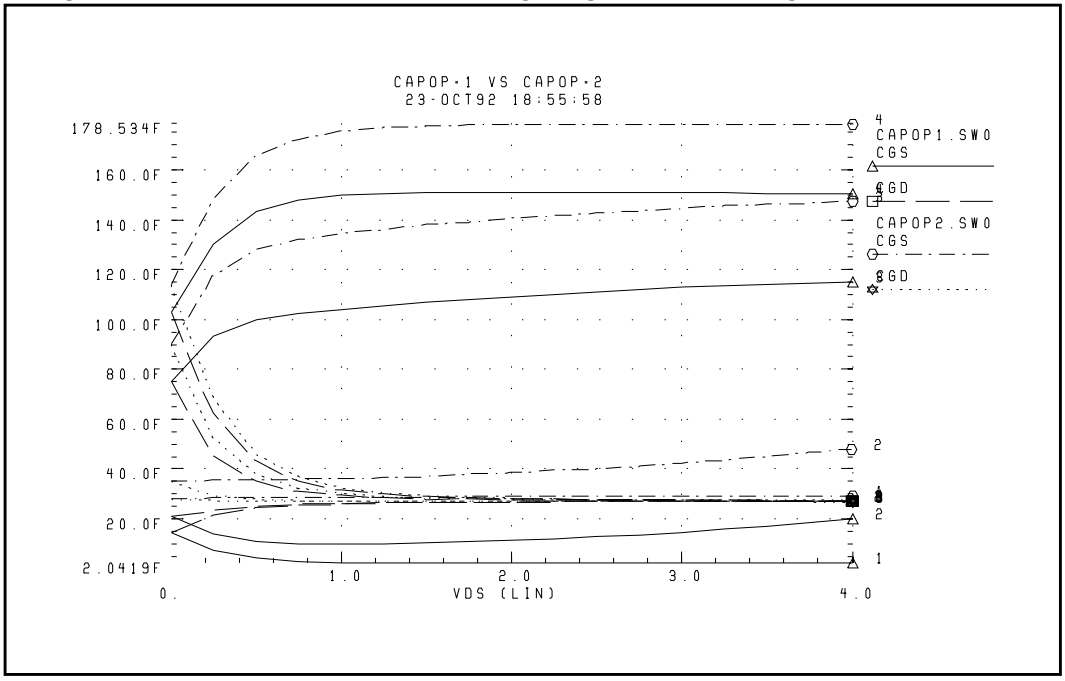


Figure 5-6: CAPOP=1 vs. CAPOP=2. Cgs, Cgd vs. Vds for Vgs=-1.5, -1.0, -0.5, 0



JFET and MESFET DC Equations

DC Model Level 1

JFET DC characteristics are represented by the nonlinear current source, ids. The value of ids is determined by the equations:

$$vgst = vgs - VTO$$

vgst< 0 Channel pinched off

$$ids = 0$$

0<vgst<vds Saturated region

$$ds = BETAeff \cdot vgst^2 \cdot (1 + LAMBDA \cdot vds)$$

0<vds<vgst Linear region

$$ds = BETAeff \cdot vds \cdot (2 \cdot vgst - vds) \cdot (1 + LAMBDA \cdot vds)$$

The drain current at zero vgs bias (ids) is related to VTO and BETA by the equation:

$$idss = BETAeff \cdot VTO^2$$

At a given vgs, LAMBDA can be determined from a pair of drain current and drain voltage points measured in the saturation region where vgst<vds:

$$LAMBDA = \left(\frac{ids2 - ids1}{ids1 \cdot vds2 - ids2 \cdot vds1}\right)$$

DC Model Level 2

The DC characteristics of the JFET Level 2 model are represented by the nonlinear current source (ids). The value of ids is determined by the equations:

$$vgst = vgs - VTO$$

vgst<0 Channel pinched off

$$ids = 0$$

0<vgst ≤ vds, vgs 0 Saturated region, forward bias

$$ids = BETAeff \cdot vgst^2 \cdot [1 + LAMBDA \cdot (vds - vgst) \cdot (1 + LAM1 \cdot vgs)]$$

0<vgst<vds, vgs<0 Saturated region, reverse bias

$$ds = BETAeff \cdot vgst^2 \cdot \left[1 - LAMBDA \cdot (vds - vgst) \cdot \frac{vgst}{VTO}\right.$$

0<vds<vgst Linear region

$$ids = BETAeff \cdot vds(2 \cdot vgst - vds)$$

DC Model Level 3

The DC characteristics of the MESFET Level 3 model are represented by the nonlinear hyperbolic tangent current source (ids). The value of ids is determined by the equations:

vds>0 Forward region

If model parameters VP and VTO are not specified they are calculated as:

$$VP = -\frac{q \cdot NCHAN \cdot Aeff^2}{2 \cdot D \cdot \varepsilon_o}$$

$$VTO = VP + VBI$$

then,

$$vgst = vgs - [VTO + GAMDS \cdot vds + K1(vbs)]$$

$$beteff = \frac{BETAeff}{(1 + UCRIT \cdot vgst)}$$

vgst<0 Channel pinched off

$$ids = idsubthreshold(N0, ND, vds, vgs)$$

vgst>0, SAT=0 On region

$$ids = beteff \cdot (vgst^{VGEXP}) \cdot (1 + LAMBDA \cdot vds) \cdot \tanh(ALPHA \cdot vds) + idsubthreshold(N0, ND, vds, vgs)$$

vgst>0, SAT=1 On region

$$ids = beteff \cdot (vgst^{VGEXP}) \cdot (1 + LAMBDA \cdot vds) \cdot \tanh\left(ALPHA \cdot \frac{vds}{vgst}\right) + idsubthreshold(N0, ND, vds, vgs)$$

vgst>0, SAT=2, vds<3/ALPHA On region

$$ids = beteff \cdot vgst^2 \cdot (1 + LAMBDA \cdot vds) \cdot \left[1 - \left(1 - ALPHA \cdot \frac{vds}{3}\right)^3\right]$$

$$+ idsubthreshold(N0, ND, vds, vgs)$$

vgst>0, SAT=2, vds>3/ALPHA On region

$$ids = beteff \cdot vgst^2 \cdot (1 + LAMBDA \cdot vds)$$

$$+ idsubthreshold(N0, ND, vds, vgs)$$

If vgst >0, SAT=3 is the same as SAT=2, except exponent 3 and denominator 3 are parameterized as SATEXP, and exponent 2 of vgst is parameterized as VGEXP.

Note: *idsubthreshold* is a special function that calculates the subthreshold currents given the model parameters N0 and ND.

JFET and MESFET Noise Models

Noise Parameters

Name (Alias)	Default	Description
AF	1.0	Flicker noise exponent
KF	0.0	Flicker noise coefficient. Reasonable values for KF are in the range 1e-19 to 1e-25 V^2 F.
NLEV	2.0	Noise equation selector
GDSNOI	1.0	Channel noise coefficient. Use with NLEV=3.

Noise Equations

The JFET noise model is shown in Figure 5-4. Thermal noise generation in the drain and source regions (RD and RS resistances) is modeled by the two current sources, *inrd* and *inrs*. The units of *inrd* and *inrs* are:

$$\mathrm{inrd} = \left(\frac{4 \cdot k \cdot t}{rd}\right)^{1/2}$$

$$\mathrm{inrs} = \left(\frac{4 \cdot k \cdot t}{rs}\right)^{1/2}$$

Channel thermal and flicker noise are modeled by the current source *ind* and defined by the equation:

$$\mathrm{ind} = \mathrm{channelthermalnoise} + \mathrm{flickernoise}$$

If the model parameter NLEV is less than 3, then:

$$\mathrm{channelthermalnoise} = \left(\frac{8 \cdot k \cdot t \cdot gm}{3}\right)^{1/2}$$

The previous formula, used in saturation and linear regions, can lead to wrong results in the linear region. For example, at VDS=0, channel thermal noise becomes zero, because gm=0. This is physically impossible. If you set the NLEV model parameter to 3, simulation uses a different equation, which is valid in both linear and saturation regions[4].

For NLEV=3

$$\text{channelthermalnoise} = \left(\frac{8kt}{3} \cdot \text{BETAeff} \cdot (\text{vgs} - \text{VTO}) \cdot \frac{1 + a + a^2}{a} \cdot \text{GDSNOI}\right)$$

where

$$\alpha = 1 - \frac{\text{vds}}{\text{vgs} - \text{VTO}}, \quad \textit{Linear region}$$

$$\alpha = 0 \quad \textit{Saturation region}$$

The flicker noise is calculated as:

$$\text{flickernoise} = \left(\frac{\text{KF} \cdot \text{ids}^{\text{AF}}}{f}\right)^{1/2}$$

Noise Summary Printout Definitions

RD, V^2/HZ	output thermal noise due to drain resistor
RS, V^2/HZ	output thermal noise due to source resistor
RG, V^2/HZ	output thermal noise due to gate resistor
ID, V^2/HZ	output thermal noise due to channel
FN, V^2/HZ	output flicker noise
TOT, V^2/HZ	total output noise (TOT = RD + RS + RG + ID + FN)
ONOISE	output noise
INOISE	input noise

[4]Tsividis, Yanis P., *Operation and Modeling of the MOS Transistor*, McGraw-Hill, 1987, p. 340.

JFET and MESFET Temperature Equations

Table 5-9 lists temperature effect parameters. The temperature effect parameters apply to Levels 1, 2, and 3. They include temperature parameters for the effect of temperature on resistance, capacitance, energy gap, and a number of other model parameters. The temperature equation selectors, TLEV and TLEVC, select different temperature equations for the calculation of energy gap, saturation current, and gate capacitance. TLEV is either 0, 1, or 2 while TLEVC is either 0, 1, 2, or 3.

Table 5-9: Temperature Parameters (Levels 1, 2, and 3)

Function	Parameter
capacitance	CTD, CTS
DC	M, TCV, XTI
energy gap	EG, GAP1, GAP2
equation selections	TLEV, TLEVC
grading	M
mobility	BEX
resistance	TRD, TRS

Temperature Effect Parameters

Table 5-10: Temperature Effect Parameters *(Sheet 1 of 3)*

Name (Alias)	Units	Default	Description
BETATCE	1/°	0.0	Beta temperature coefficient for TriQuint model
BEX		0.0	Mobility temperature exponent, correction for low field mobility
CTD	1/°	0.0	Temperature coefficient for gate-drain junction capacitance. TLEVC=1 enables CTD to override the default temperature compensation.
CTS	1/°	0.0	Temperature coefficient for gate-source junction capacitance. TLEVC=1 enables CTS to override the default temperature compensation.
EG	eV	1.16	Energy gap for the gate to drain and gate to source diodes at 0 °K ■ 1.17 - silicon ■ 0.69 - Schottky barrier diode ■ 0.67 - germanium ■ 1.52 - gallium arsenide
GAP1	eV/°	7.02e-4	First bandgap correction factor, from Sze, alpha term ■ 7.02e-4 - silicon ■ 4.73e-4 - silicon ■ 4.56e-4 - germanium ■ 5.41e-4 - gallium arsenide

Table 5-10: Temperature Effect Parameters *(Sheet 2 of 3)*

Name (Alias)	Units	Default	Description
GAP2	x	1108	Second bandgap correction factor, from Sze, beta term ■ 1108 - silicon ■ 636 - silicon ■ 210 - germanium ■ 204 - gallium arsenide
M (MJ)		0.50	Grading coefficient for gate-drain and gate-source diodes ■ 0.50 - step junction ■ 0.33 - linear graded junction
N		1.0	Emission coefficient for gate-drain and gate-source diodes
TCV (VTOTC)	1/°	0.0	Temperature compensation coefficient for VTO (threshold voltage)
TLEV		0.0	Temperature equation selector for junction diodes. Interacts with the TLEVC parameter.
TLEVC		0.0	Temperature equation selector for junction capacitances and potential. Interacts with the TLEV parameter.
TPB	V/°	0.0	Temperature coefficient for PB. TLEVC=1 or 2 overrides the default temperature compensation.
TRD (TDR1)	1/°	0.0	Temperature coefficient for drain resistance

Table 5-10: Temperature Effect Parameters *(Sheet 3 of 3)*

Name (Alias)	Units	Default	Description
TRG (TRG1)	1/°	0	Temperature coefficient for gate resistance
TRS (TRS1)	1/°	0.0	Temperature coefficient for source resistance
XTI		0.0	Saturation current temperature exponent XTI=3 for silicon diffused junction or XTI=2 for Schottky barrier diode

Temperature Compensation Equations

Energy Gap Temperature Equations

To determine energy gap for temperature compensation, use the equation:

TLEV = 0 or 1

$$egnom = 1.16 - 7.02e{-}4 \cdot \frac{tnom^2}{tnom + 1108.0}$$

$$eg(t) = 1.16 - 7.02e{-}4 \cdot \frac{t^2}{t + 1108.0}$$

TLEV = 2

$$egnom = EG - GAP1 \cdot \frac{tnom^2}{tnom + GAP2}$$

$$eg(t) = EG - GAP1 \cdot \frac{t^2}{t + GAP2}$$

Saturation Current Temperature Equations

The saturation current of the gate junctions of the JFET varies with temperature according to the equation:

$$is(t) = IS \cdot e^{\frac{facln}{N}}$$

TLEV=0 or 1

$$facln = \frac{EG}{vt(tnom)} - \frac{EG}{vt(t)} + XTI \cdot \ln\left(\frac{t}{tnom}\right)$$

TLEV=2

$$facln = \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)} + XTI \cdot \ln\left(\frac{t}{tnom}\right)$$

Gate Capacitance Temperature Equations

Temperature equations calculate the gate capacitances. The CTS and CTD parameters are the linear coefficients. If you set TLEVC to zero, simulation uses these equations. To achieve a zero capacitance variation, set the coefficients to a very small value (such as 1e-6), and set TLEVC=1 or 2.

TLEVC=0

$$CGS(t) = CGS \cdot \left[1 + M \cdot \left(4.0e\text{-}4 \cdot \Delta t - \frac{PB(t)}{PB} + 1\right)\right]$$

$$CGD(t) = CGD \cdot \left[1 + M \cdot \left(4.0e\text{-}4 \cdot \Delta t - \frac{PB(t)}{PB} + 1\right)\right]$$

where:

$$PB(t) = PB \cdot \left(\frac{t}{tnom}\right) - vt(t) \cdot \left[3\ln\left(\frac{t}{tnom}\right) + \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)}\right]$$

TLEVC=1

$$CGS(t) = CGS \cdot (1 + CTS \cdot \Delta t)$$

$$CGD(t) = CGD \cdot (1 + CTD \cdot \Delta t)$$

where:

$$PB(t) = PB - TPB \cdot \Delta t$$

TLEVC=2

$$CGS(t) = CGS \cdot \left(\frac{PB}{PB(t)}\right)^{M}$$

$$CGD(t) = CGD \cdot \left(\frac{PB}{PB(t)}\right)^{M}$$

where:

$$PB(t) = PB - TPB \cdot \Delta t$$

TLEVC=3

$$CGS(t) = CGS \cdot \left(1 - 0.5 \cdot dpbdt \cdot \frac{\Delta t}{PB}\right)$$

$$CGD(t) = CGD \cdot \left(1 - 0.5 \cdot dpbdt \cdot \frac{\Delta t}{PB}\right)$$

where:

$$PB(t) = PB + dpbdt \cdot \Delta t$$

TLEV=0 or 1

$$dpbdt = \frac{-\left[egnom + 3 \cdot vt(tnom) + (1.16 - egnom) \cdot \left(2 - \frac{tnom}{tnom + 1108}\right) - PB\right]}{tnom}$$

TLEV=2

$$dpbdt = \frac{-\left[egnom + 3 \cdot vt(tnom) + (EG - egnom) \cdot \left(2 - \frac{tnom}{tnom + GAP2}\right) - PB\right]}{tnom}$$

Threshold Voltage Temperature Equation

The threshold voltage of the JFET varies with temperature according to the equation:

$$VTO(t) = VTO - TCV \cdot \Delta t$$

$$CVTO(t) = CVTO - TCV \cdot \Delta t$$

Mobility Temperature Equation

The mobility temperature compensation equation is updated as:

$$BETA(t) = BETA \cdot \left(\frac{t}{tnom}\right)^{BEX} \quad \textit{If BETATCE=0}$$

Otherwise (TriQuint model):

$$BETA(T) = BETA \cdot 1.01^{BETATCE(t - tnom)}$$

Parasitic Resistor Temperature Equations

The RD and RS resistances in JFET vary with temperature according to the equations:

$$RD(t) = RD \cdot (1 + TRD \cdot \Delta t)$$

$$RS(t) = RS \cdot (1 + TRS \cdot \Delta t)$$

$$RG(t) = RG \cdot (1 + TRG \cdot \Delta t)$$

TriQuint Model (TOM) Extensions to Level=3

TOM "TriQuint's Own Model"[5] is implemented as part of the existing GaAs Level 3 model. [6].

There are a few differences from the original implementation. The Avant! version of the TOM model takes advantage of existing Level 3 features to provide:

- Subthreshold model (NG, ND)
- Channel and source/drain resistances, geometrically derived from width and length (RD, RG, RS, RSH, RSHG, RSHL, HDIF, LDIF) (ACM=1)
- Photolithographic compensation (LDEL, WDEL, ALIGN)
- Substrate terminal
- Geometric model with width and length specified in the element (ACM=1)
- Automatic model selection as a function of width and length (WMIN, WMAX, LMIN, LMAX)
- User-defined band-gap coefficients (EG, GAP1, GAP2)

Several alias TOM parameters are defined for existing Level 3 parameters to make the conversion easier. An alias allows the original name or the alias name to be used in the .MODEL statement. However, the model parameter printout is in the original name. Please note that in two cases, a sign reversal is needed, even when using the TOM parameter name.

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[5]A.J. McCamant, G.D. Mc Cormack, and D.H.Smith, *An Improved GaAs MESFET Model for SPICE*, IEEE.

[6]W.Curtice, A MESFET Model For Use In the Design of GaAs Integrated Circuits, *IEEE Tran, Microwave*, and H.Statz, P.Newman, I.W.Smith, R.A. Pucel, and H.A. Haus, "GaAs FET Device And Circuit Simulation in SPICE".

Alias	Printout Name	Note
Q	*VGEXP*	
GAMMA	*GAMDS*	sign opposite of TriQuint's original
VTOTC	*TCV*	sign opposite of TriQuint's original
TRG1	*TRG*	
TRD1	*TRD*	
TRS1	*TRS*	

TOM Model Parameters

Name (Alias)	Description
BETATCE	Temperature coefficient for BETA If betatce is set to a nonzero value: $$BETA(temp) = BETA(tnom) \cdot 1.01^{(BETATCE \cdot (temp - tnom))}$$ The more common Beta temperature update is: $$BETA(temp) = BETA(tnom) \cdot \left(\frac{temp}{tnom}\right)^{BEX}$$
DELTA	Ids feedback parameter of the TOM model. This parameter is not used if its value is zero. DELTA can be negative or positive. $$i_{ds} \Rightarrow \frac{i_{ds}}{\max[(-1 + v_{ntol}),(DELTA + v_{ds} \cdot i_{ds})]}$$
CAPDS	Drain-to-source capacitance $$CAPDSeff = CAPDS \cdot \frac{Weff}{Leff} \cdot M$$

Note: In the original TOM implementation by TriQuint, parameters LAMBDA and UCRIT do not exist. Therefore, they must remain zero (their default value) in Level 3 in order to reproduce the TOM model. Use of nonzero values for these parameters with nonzero BETATCE, DELTA, or CAPDS results in a hybrid model.

Level 7 TOM3 (TriQuint's Own Model III)

TOM3 is available as JFET/MESFET Level 7 in the Avant! True-Hspice models. It was developed by TriQuint to improve the accuracy of the capacitance equations, using quasi-static charge conservation in the implanted layer of a MESFET.

Using the TOM3 Model

1. Set Level=7, to identify the model as the TOM3 model.
2. The default room temperature is 25 in the Avant! True-Hspice models, but is 27 in most other simulators. When comparing to other simulators, set the simulation temperature to 27, using either .TEMP 27 or .OPTIONS TNOM=27.
3. The set of model parameters should always include the model reference temperature, TNOM, which corresponds to TREF in other levels in the Avant! True-Hspice models. The default for TR is 25.
4. TOM3 has its own charge-based capacitance model. This model ignores the CAPOP parameter, which selects different capacitance models.
5. The model uses the analytical derivatives for the conductances. This model ignores the DERIV parameter, which selects the finite difference method.
6. You can use DTEMP with this model. DTEMP increases the temperature of individual elements, relative to the circuit temperature. Set DTEMP on the element line.
7. The general syntax for the element is the same as the other standard JFET/MESFET models.
8. The model is defined by a specific sub-circuit, and a set of device equations. The topology uses local feedback, which decreases the DC output conductance to model drain, model dispersion, and self-heating effects.

Note: For more informations, refer to "TOM3 Equations, Revised: 2 December 1999" by Robert B. Hallgren and David S. Smith.

Model Description

DC Equations

Drain to Source Current (I_{DS})

$$I_{DS} = I_0 \cdot (1 + \mathbf{LAMBDA} \cdot V_{DS})$$

$$I_0 = \beta \cdot V_G^{\mathbf{Q}} \cdot f_K$$

$$f_K = \frac{\alpha \cdot V_{DS}}{\left[1 + (\alpha \cdot V_{DS})^{\kappa}\right]^{1/K}}$$

$$V_G = \mathbf{Q} \cdot V_{ST} \cdot \log[\exp(u) + 1]$$

$$u = \frac{V_{GS} - V_{TO} + \gamma \cdot V_{DS}}{\mathbf{Q} \cdot V_{ST}}$$

$$V_{ST} = V_{ST0} \cdot (1 + M_{ST0} \cdot V_{DS})$$

Trans-conductance

$$G_M = \left(\frac{\mathbf{Q} \cdot \beta \cdot f_K \cdot V_G^{\mathbf{Q}-1}}{1 + \exp(-u)} \right) \cdot (1 + \mathbf{LAMBDA} \cdot V_{DS})$$

Output Conductance

$$G_{DS} = \mathbf{LAMBDA} \cdot I_0 + G_M \cdot \left(\gamma - \frac{(V_{GS} - V_{TO} + \gamma \cdot V_{DS}) \cdot M_{ST0}}{1 + M_{ST0} \cdot V_{DS}} \right)$$

$$+ \left[\left(\frac{\mathbf{Q} \cdot I_0 \cdot M_{ST0}}{1 + M_{ST0} \cdot V_{DS}} \right) + \left(\frac{\alpha \cdot \beta \cdot V_G^{\mathbf{Q}}}{\left[1 + (\alpha \cdot V_{DS})^{\kappa}\right]^{1+1/K}} \right) \right] \cdot (1 + \mathbf{LAMBDA} \cdot V_{DS})$$

Gate Leakage Diode Current

ILK and PLK have no temperature dependence.

$$I_{LS} = ILK \cdot \left(1 - \exp\frac{-V_{GS}}{PLK}\right) \qquad G_{LS} = \left(\frac{\mathbf{ILK}}{\mathbf{PLK}}\right) \cdot \left(\exp\frac{-V_{GS}}{\mathbf{PLK}}\right)$$

$$I_{LD} = ILK \cdot \left(1 - \exp\frac{-V_{GD}}{PLK}\right) \qquad G_{LD} = \left(\frac{\mathbf{ILK}}{\mathbf{PLK}}\right) \cdot \left(\exp\frac{-V_{GD}}{\mathbf{PLK}}\right)$$

Temperature and Geometry Dependence

$$\beta = AREA \cdot \mathbf{BETA} \cdot 1.01^{\mathbf{BETATCE} \cdot (T - T_{NOM})}$$

$$\alpha = \mathbf{ALPHA} \cdot 1.01^{\mathbf{ALPHATCE} \cdot (T - T_{NOM})}$$

$$V_{TO} = \mathbf{VTO} + \mathbf{VTOTC} \cdot (T - T_{NOM})$$

$$\gamma = GAMMA + GAMMATC \cdot (T - T_{NOM})$$

$$V_{ST0} = \mathbf{VST} + \mathbf{VSTTC} \cdot (T - T_{NOM})$$

$$V_{MT0} = \mathbf{MST} + \mathbf{MSTTC} \cdot (T - T_{NOM})$$

Capacitance Equations

Combined Gate Charge

$$Q_{GG} = Q_{GL} \cdot f_T + Q_{GH} \cdot (1 - f_T) + \mathbf{QGG0} \cdot (V_{GSI} + V_{GDI})$$

$$C_{GS} = C_{GSL} \cdot f_T + C_{GSH} \cdot (1 - f_T) + (Q_{GL} - Q_{GH}) \cdot \frac{\partial f_T}{\partial V_{GSI}} + \mathbf{QGG0}$$

$$C_{GD} = C_{GDL} \cdot f_T + C_{GDH} \cdot (1 - f_T) + (Q_{GL} - Q_{GH}) \cdot \frac{\partial f_T}{\partial V_{GDI}} + \mathbf{QGG0}$$

$$f_T = \exp(-\mathbf{QGGB} \cdot I_{DS} \cdot V_{DS})$$

$$\frac{\partial f_T}{\partial V_{GSI}} = -\mathbf{QGGB} \cdot [I_{DS} + (g_m + g_{ds}) \cdot V_{DS}] \cdot f_T$$

$$\frac{\partial f_T}{\partial V_{GD}} = \mathbf{QGGB} \cdot [I_{DS} + g_{ds} \cdot V_{DS}] \cdot f_T$$

Lower Power Gate Charge

$$Q_{GL} = qgl + \mathbf{QGCL} \cdot (V_{GS} + V_{GD})$$

$$qgl = \mathbf{QGQL} \cdot \exp[\mathbf{QGAG} \cdot (V_{GS} + V_{GD})] \cdot \cosh(\mathbf{QGAD} \cdot V_{DS})$$

$$C_{GSL} = qgl \cdot [\mathbf{QGAG} + \mathbf{QGAD} \cdot \tanh(\mathbf{QGAD} \cdot V_{DS})] + \mathbf{QGCL}$$

$$C_{GDL} = qgl \cdot [\mathbf{QGAG} - \mathbf{QGAD} \cdot \tanh(\mathbf{QGAD} \cdot V_{DS})] + \mathbf{QGCL}$$

High Power Gate Charge

$$Q_{GH} = \mathbf{QGQH} \cdot \log\left(1 + \frac{I_{DS}}{\mathbf{QGI0}}\right) + \mathbf{QGSH} \cdot V_{GS} + \mathbf{QGDH} \cdot V_{GD}$$

$$C_{GSH} = (G_M + G_{DS}) \cdot \left(\frac{QGQH}{I_{DS} + QGI0}\right) + QGSH$$

$$C_{GDH} = -G_{DS} \cdot \left(\frac{QGQH}{I_{DS} + QGI0}\right) + QGDH$$

Parameters

Table 5-11: TOM3 Parameters *(Sheet 1 of 3)*

Name (Alias)	Description	Units	Default
LEVEL	Model Index (7 for TOM3)	-	1
TNOM	Reference temperature		25
VTO	Threshold voltage	V	-2
VTOTC	Threshold voltage temperature coefficient	V/K	0
ALPHA	Saturation factor	1/V	2
BETA	Transconductance parameter	A/V^{-Q}	0.1
LAMBDA	Channel length modulation parameter	1/V	0
VBI	Gate diode built-in potential	V	1
CDS	Drain to source capacitance	F	1E-12
IS	Forward gate diode saturation current	A	1E-14
KF	Flicker noise coefficient	-	0
AF	Flicker noise exponent	-	1
GAMMA	Drain voltage-induced threshold voltage lowering coefficient	-	0
Q	Parameter Q to model the non-square-law of the drain current	-	2
EG	Barrier height at 0K(used for capacitance model)	V	1.11
XTI	Diode saturation current temperature coefficient	-	0

Table 5-11: TOM3 Parameters *(Sheet 2 of 3)*

Name (Alias)	Description	Units	Default
VST	Sub-threshold slope	V	1
ALPHATCE	ALPHA temperature coefficient (exponential)	K^{-1}	0
ILK	Leakage diode current parameter	A	0
PLK	Leakage diode potential parameter	V	1
K	Knee-function parameter	-	2
VSTTC	Linear temperature coefficient of VST	VK^{-1}	0
QGQL	Charge parameter	FV	5E-16
QGQH	Charge parameter	FV	-2E-16
QGI0	Charge parameter	A	1E-6
QGAG	Charge parameter	V^{-1}	1
QGAD	Charge parameter	V^{-1}	1
QGGB	Charge parameter	$A^{-1}V^{-1}$	100
QGCL	Charge parameter	F	2E-16
QGSH	Sidewall capacitance	F	1E-16
QGDH	Sidewall capacitance	F	0
QGG0	Charge parameter	F	0
MST	Sub-threshold slope – drain parameter	V^{-1}	0
N	Forward gate diode ideality factor	-	1
GAMMATC	Linear temperature coefficient for GAMMA	K^{-1}	0

Table 5-11: TOM3 Parameters *(Sheet 3 of 3)*

Name (Alias)	Description	Units	Default
VBITC	Linear temperature coefficient for VBI	VK^{-1}	0
CGSTCE	Linear temperature coefficient for C_{GS}	K^{-1}	0
CGDTCE	Linear temperature coefficient for C_{GD}	K^{-1}	0
MSTTC	Linear temperature coefficient for MST	$V^{-1}K^{-1}$	0
BETATCE	Linear temperature coefficient for BETA	K^{-1}	0

Level 8 Materka Model

This section describes the Avant! True-Hspice JFET&MESFET model Level=8.

For more information about this model, see Compact dc Model of GaAs FETs for Large-Signal Computer Calculation, *IEEE Journal of Solid-State Circuits*, Vol, SC-18, No.2, April 1983, and Computer Calculation of Large-Signal GaAs FET Amplifier Characteristics, *IEEE Transactions on Microwave Theory and Techniques*, Vol. MTT-33, No. 2, February 1985.

Using the Materka Model

1. Set Level=8.
2. The default room temperature is 25 in the Avant! True-Hspice model, but is 27 in most other simulators. When comparing to other simulators, set the simulation temperature to 27, using either .TEMP 27 or .OPTIONS TNOM=27.
3. The model has its own charge-based capacitance model. This model ignores the CAPOP parameter, which selects difference capacitance.
4. The ACM parameter is not supported.

Description of Parameters

DC Model

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 \tanh\left(\frac{\alpha 1 * V_{DS}}{V_{GS}-V_P}\right)$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = I_{DSS}\left[-\frac{2}{V_P}\left(1-\frac{V_{GS}}{V_P}\right)\cdot\tanh\left(\frac{\alpha 1\cdot V_{DS}}{V_{GS}-V_P}\right)\right.$$

$$\left.+\left(1-\frac{V_{GS}}{V_P}\right)\cdot\sec h^2\left(\frac{\alpha 1\cdot V_{DS}}{V_{GS}-V_P}\right)\cdot\frac{-\alpha 1\cdot V_{DS}}{(V_{GS}-V_P)^2}\right]$$

$$g_{DS} = \frac{\partial I_D}{\partial V_{DS}} = I_{DSS}\cdot\left(1-\frac{V_{GS}}{V_P}\right)\cdot\left[-\frac{2\gamma V_{GS}}{{V_P}^2}\cdot\tanh\left(\frac{\alpha 1\cdot V_{DS}}{V_{GS}-V_P}\right)\right.$$

$$\left.+\left(1-\frac{V_{GS}}{V_P}\right)\cdot\sec h^2\left(\frac{\alpha 1\cdot V_{DS}}{V_{GS}-V_P}\right)\cdot\frac{\alpha 1\cdot(V_{GS}-V_{PO})}{(V_{GS}-V_P)^2}\right]$$

$$V_P = V_{TO} + \gamma V_{DS}$$

Table 5-12: DC Model Parameters

Name (Alias)	Units	Default	Description
LEVEL		1.0	Level=8 is the Materka MESFET model.
ALPHA1			Empirical constant
VTO	V	-2.0	Threshold voltage. If set, it overrides internal calculation. A negative VTO is a depletion transistor regardless of NJF or PJF. A positive VTO is always an enhancement transistor.
VP	V		Pinch-off voltage (default is calculated)
IDSS	A	0.1	Drain saturation current for Vgs=0
GAMMA	1/V	0.0	Voltage slope parameter of pinch-off voltage

Gate Capacitance Model

$$C_{GS} = \frac{CGS}{4\sqrt{1-\frac{vnew}{PB}}}\left[1+\frac{veff-vte}{\sqrt{(veff-vte)^2+(0.2)^2}}\right]\cdot\left[1+\frac{vds}{\sqrt{vds^2+\left(\frac{1}{ALPHA1}\right)^2}}\right]$$

$$+\left[\frac{CGD}{2}\left(1-\frac{vds}{\sqrt{vds^2+\left(\frac{1}{ALPHA1}\right)^2}}\right)\right]$$

$$C_{GD} = \frac{CGS}{4\sqrt{1-\frac{vnew}{PB}}}\left[1+\frac{veff-vte}{\sqrt{(veff-vte)^2+(0.2)^2}}\right]\cdot\left[1-\frac{vds}{\sqrt{vds^2+\left(\frac{1}{ALPHA1}\right)^2}}\right]$$

$$+\left[\frac{CGD}{2}\left(1+\frac{vds}{\sqrt{vds^2+\left(\frac{1}{ALPHA1}\right)^2}}\right)\right]$$

$$vte = VTO + GAMMA\cdot vds = effective\,threshold$$

$$veff = \frac{1}{2}\left[vgs+vgd+\sqrt{vds^2+\left(\frac{1}{ALPHA1}\right)^2}\right]$$

$$vnew = \frac{1}{2}\left[veff+vte+\sqrt{(veff-vte)^2+(0.2)^2}\right]$$

Table 5-13: Gate Capacitance Model Parameters

Name (Alias)	Units	Default	Description
CGS	F	0.0	Zero-bias gate-source junction capacitance
CGD	F	0.0	Zero-bias gate-drain junction capacitance
PB	V	0.8	Gate Junction Potential
N		1.0	Emission coefficient for gate-drain and gate-source diodes

Noise Model

Two current sources model the thermal noise generation in the drain and source regions (RD and RS resistances):

- inrd
- *inr*s

inrd and *inrs* are modeled by:

$$inrs = \left(\frac{4kt}{rs} \right)^{1/2}$$

$$inrd = \left(\frac{4kt}{rd} \right)^{1/2}$$

Channel thermal and flicker noise are modeled by the *ind* current source, and defined by the equation:

ind = channel thermal noise+ flicker noise

$$\text{chanel thermal noise} = \left(\frac{8kt \cdot g_m}{3} \right)^{1/2}$$

$$\text{flicker noise} = \left(\frac{KF \cdot ids^{AF}}{f} \right)^{1/2}$$

Table 5-14: Noise Model Parameters

Name (Alias)	Units	Default	Description
AF		1.0	Flicker noise exponent
KF		0.0	Flicker noise coefficient. Reasonable values for KF are in the range 1e-19 to 1e-25 V2 F.

Example

```
.MODEL      NCH          NJF   LEVEL=8
+ IDSS      = 69.8e-3    VTO   = -2        GAMMA  = 0
+ ALPHA1    = 1          RS    = 0         RD     = 0
+ CGS       = 1e-15      CGD   = 2e-16     PB     = 0.8
+ IS        = 5e-16      AF    = 1         KF     = 0
+ FC        = 0.5
.END
```

Avant!

Chapter 6
Using Transmission Lines

A transmission line is a passive element that connects any two conductors, at any distance apart. One conductor sends the input signal through the transmission line, and the other conductor receives the output signal from the transmission line. The signal that is transmitted from one end of the pair to the other end, is voltage between the conductors.

Examples of transmission lines include:

- Power transmission lines.
- Telephone lines.
- Waveguides.
- Traces on printed circuit boards and multi-chip modules (MCMs).
- Bonding wires in semiconductor IC packages.
- On-chip interconnections.

This chapter describes the basic transmission line simulation equations. It explains how to use these equations as an input to the transmission line model, the *W* element.[1]

This chapter also shows you an optional method for computing the parameters of the transmission line equations, using the *field solver* model.

[1]For more information about the *W* element, see Dmitri Kuznetsov, "Optimal Transient Simulation of Transmission Lines," *IEEE Trans., Circuits Syst.*, vol.43, pp. 110-121, Feb., 1996.

The W element is a versatile transmission line model, which you can apply to efficiently and accurately simulate transmission lines, ranging from a simple lossless line, to complex frequency-dependent lossy-coupled lines. Unlike the *U* Element (see Appendix A, "Ideal and Lumped Transmission Lines"), the *W* Element can output accurate simulation results, without fine-tuning optional parameters.

Transmission line simulation is challenging and time-consuming, because extracting transmission line parameters from physical geometry requires a significant effort. To minimize this effort, you can use a simple (but efficient and accurate) 2-D electromagnetic field solver, which calculates the electrical parameters of a transmission line system, based on its cross-section.

This chapter includes the following topics:

Equations and Parameters

Maxwell's equations, for the transverse electromagnetic (TEM) waves on multi-conductor transmission lines, reduce to the telegrapher's equations. The general form of the telegrapher's equation in the frequency domain is:

$$-\frac{\partial}{\partial z}\mathbf{v}(z, \omega) = [\mathbf{R}(\omega) + j\omega\mathbf{L}(\omega)]\mathbf{i}(z, \omega)$$

$$-\frac{\partial}{\partial z}\mathbf{i}(z, \omega) = [\mathbf{G}(\omega) + j\omega\mathbf{C}(\omega)]\mathbf{v}(z, \omega)$$

where:

- Boldface lower-case symbols denote vectors.
- Boldface upper-case symbols denote matrices.
- *v* is the voltage vector across the lines.
- *i* is the current vector along the lines.

For the TEM mode, the transverse distribution of electromagnetic fields at any instant of time, is identical to that for the static solution. From a static analysis, you can derive the four parameters for multi-conductor TEM transmission lines:

- resistance matrix *R*
- inductance matrix *L*
- conductance matrix *G*
- capacitance matrix *C*

The telegrapher's equations, and the four parameter matrices from a static analysis, completely and accurately describe TEM lines.

Unfortunately, not all transmission lines support pure TEM waves; some multi-conductor systems inherently produce longitudinal field components. In particular, waves propagating in either the presence of conductor losses or the absence of dielectric homogeneity (but not dielectric losses), must have longitudinal components.

However, if the transverse components of the fields are significantly larger than the longitudinal components, the telegrapher's equations (and the four parameter matrices obtained from a static analysis) still provide a good approximation. This is known as a *quasi-static approximation*.

Multi-conductor systems, in which this approximation is valid, are called *quasi-TEM lines*. For typical micro-strip systems, the quasi-static approximation holds, up to a few gigahertz.

Frequency-Dependent Matrices

The static (constant) L and C matrices are accurate for a wide range of frequencies. In contrast, the static (DC) R matrix applies to only a limited frequency range, mainly due to the skin effect. A good approximate expression of the R resistance matrix, with the skin effect, is:

$$\mathbf{R}(f) \cong \mathbf{R_o} + \sqrt{f}(1 + j)\mathbf{R_s}$$

where:

- R_o is the DC resistance matrix.
- R_s is the skin effect matrix.

The imaginary term depicts the correct frequency response at high frequency; however, it might cause significant errors for low-frequency applications. In the *W* element, you can optionally exclude this imaginary term:

```
Wxxx i1 i2 ... iN iR o1 o2 ... oN oR N=val L=val
   INCLUDERSIMAG=NO
```

In contrast, the G (loss) conductance matrix is often approximated as:

$$\mathbf{G}(f) \cong \mathbf{G_o} + \frac{f}{\sqrt{1 + (f / f_{gd})^2}}\mathbf{G_d}$$

where:

- G_o models the shunt current, due to free electrons in imperfect dielectrics.
- G_d models the power loss, due to the rotation of dipoles under the alternating field.[2]
- f_{gd} is a cut-off frequency.

When you set f_{gd}, G(f) keeps linear dependency on the frequency, where the frequency is higher than f_{gd}. In the *W* element, the default f_{gd} is zero—that is, G(f) does not use the f_{gd} value.

---

[2]C. A. Balanis, *Advanced Engineering Electromagnetics*, New York: Wiley, 1989.

You can specify an alternate value in the W Element statement:

```
Wxxx i1 i2 ... iN iR o1 o2 ... oN oR N=val L=val fgd=val
```

If you prefer to use the previous linear dependency, set `fgd` to 0.

Determining Matrix Properties

All matrices in the previous description are symmetric.

- The diagonal terms of `L` and `C` are positive, non-zero.
- The diagonal terms of R_o, R_s, G_o, and G_d are non-negative (can be zero).
- Off-diagonal terms of the `L`, R_o impedance matrices are non-negative[3].
- Off-diagonal terms of admittance matrices `C`, G_o, and G_d are non-positive.
- Off-diagonal terms of all matrices can be zero.

The elements of admittance matrices are related to the self/mutual admittances (such as those that the U element generates):

$$Y_{ii} = \sum_{j=1}^{N} Y_{ij}^{(self)/(mutual)}$$

$$Y_{ij} = -Y_{ij}^{mutual}, i \neq j$$

where *Y* stands for either `C`, G_o, or G_d.

A diagonal term of an admittance matrix is the sum of all self and mutual admittance in this row. This term is larger (in absolute value) than the sum of all off-diagonal terms in its row or column. Admittance matrices are strictly diagonally dominant (except for a zero matrix).

[3] R_o can have negative off-diagonal terms, but a warning appears. Negative off-diagonal terms normally appear when you characterize R_o at a frequency higher than zero. Theoretically, R_o should not contain negative off-diagonal terms, because these might cause errors during analysis.

You can obtain loop impedance matrix terms from the partial impedance matrix:

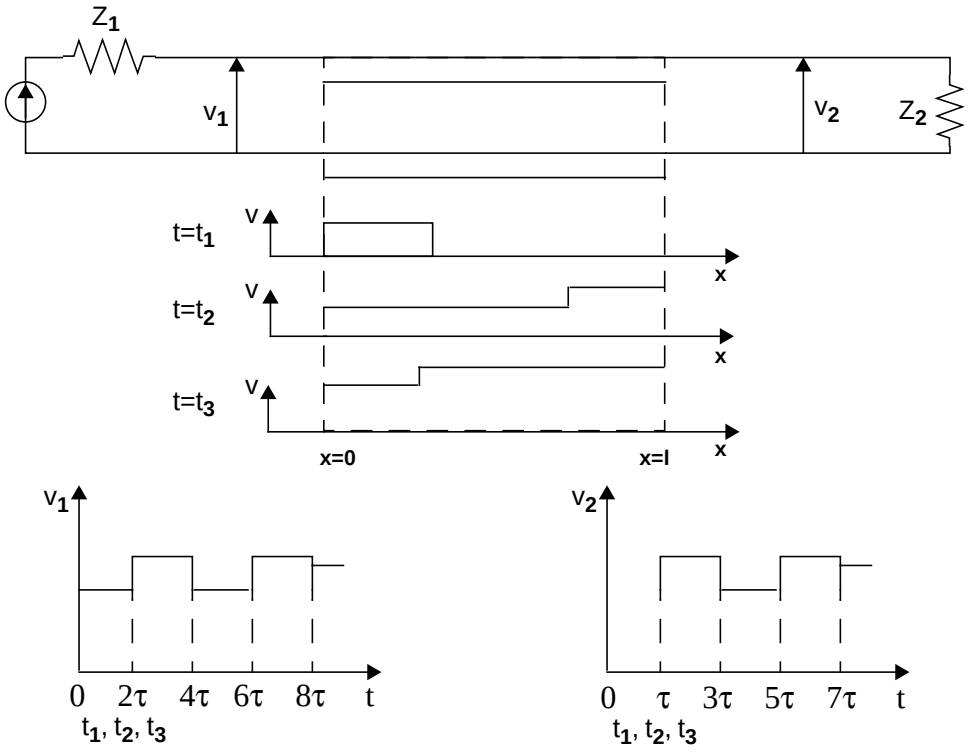
$$Z_{ij}^{(loop)} = Z_{ij}^{(partial)} - Z_{io}^{(partial)} - Z_{jo}^{(partial)} + Z_{oo}^{(partial)}$$

where the o index denotes a reference node.

Wave Propagation

To illustrate the physical process of wave propagation and reflection in transmission lines[4], Figure 6-1 shows lines where simple termination is excited with the voltage step.

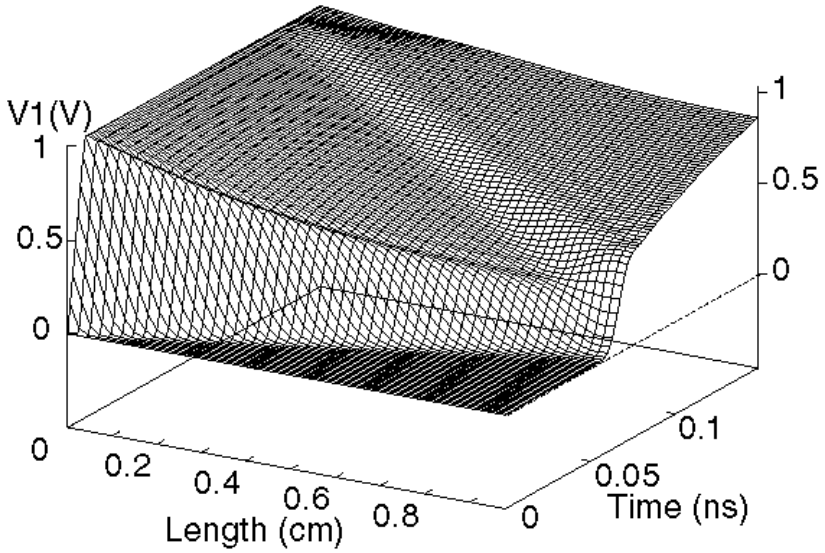
Figure 6-1: Propagation of a Voltage Step in a Transmission Line



[4]A good source for information about transmission lines is: H.B. Bakoglu, *Circuits, Interconnections and Packaging for VLSI*. Reading, MA: Addison-Wesley, 1990.

- At the time $t=t_1$, a voltage step from the e_1 source, attenuated by the Z_1 impedance, propagates along the transmission line.
- At $t=t_2$, the voltage wave arrives at the far end of the transmission line, is reflected, and propagates in the backward direction. The voltage at the load end is the sum of the incident and reflected waves.
- At $t=t_3$, the reflected wave arrives back at the near end, is reflected again, and again propagates in the forward direction. The voltage at the source end is the sum of attenuated voltage from the e_1 source, the backward wave, and the reflected forward wave.

Figure 6-2: Surface Plot, for the Transmission Line in Figure 6-1



The surface plot in Figure 6-2 shows voltage at each point in the transmission line. The input incident propagates from the left (length = 0) to the right. You can observe both reflection at the end of the line (length = 1), and a reflected wave that goes backward to the near end.

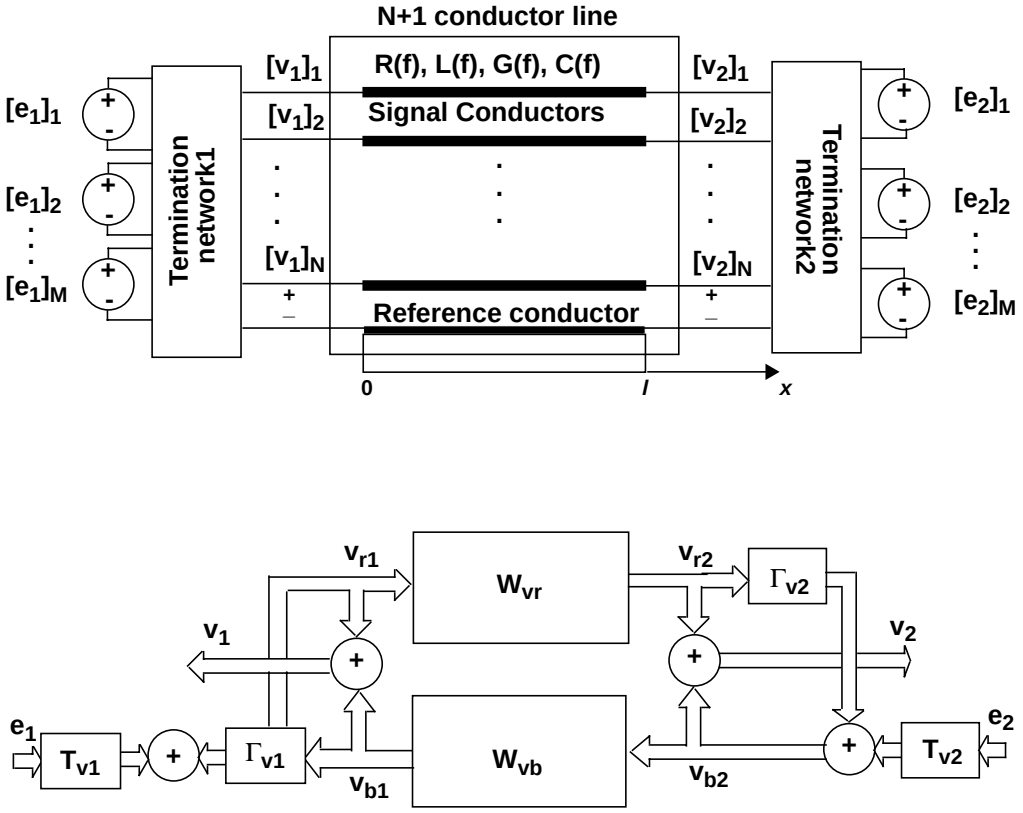
Propagating a Voltage Step

This section is a summary of the process in Figure 6-1 on page 6-8, to propagate a voltage step in a transmission line.

- Signals from the excitation source spread-out in the termination networks, and propagate along the line.
- As the forward wave reaches the far-end termination, it does the following:
  1. Reflects.
  2. Propagates backward.
  3. Reflects from the near-end termination.
  4. Propagates forward again.
  5. Continues in a loop.
- The voltage at any point along the line, including the terminals, is a superposition of the forward and backward propagating waves.

Figure 6-3 shows the system diagram for this process.

Figure 6-3: System Model for Transmission Lines



This model reproduces the general relationship between the physical phenomena of wave propagation, transmission, reflection, and coupling in a distributed system. It can represent an arbitrarily-distributed system, such as:

- Transmission lines.
- Waveguides.
- Plane-wave propagation.

You can use this model for:

- System analysis of distributed systems, or
- Writing a macro solution for a distributed system, without complicated mathematical derivations.

In this model:

- W_{vr} and W_{vb} are forward and backward matrix propagation functions for voltage waves.
- T_1, T_2 stand for the near-end matrix transmission and reflection coefficients.
- Γ_1, Γ_2 (`Gamma_1`,`Gamma_2`) stand for the far-end matrix transmission and reflection coefficients.

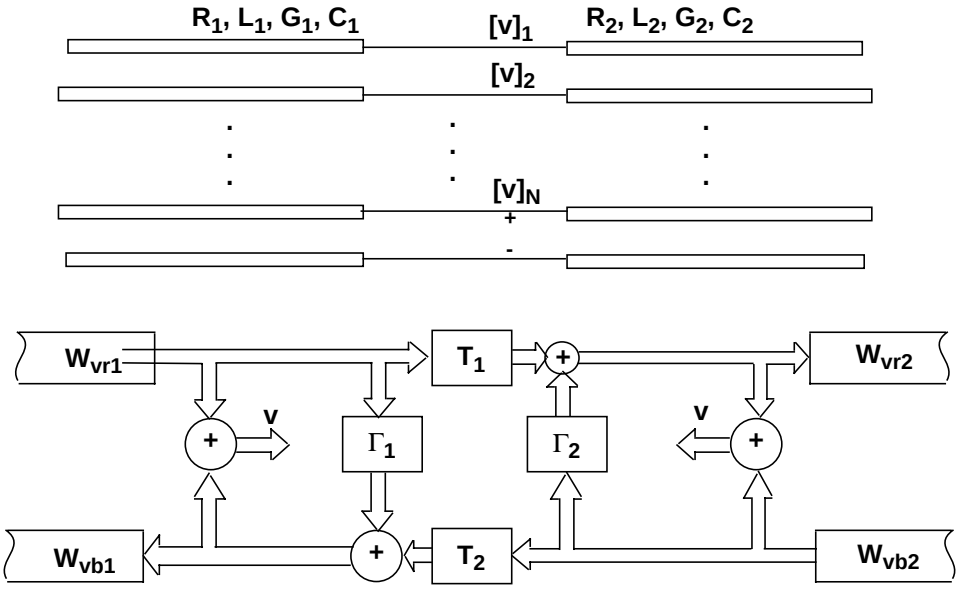
Transmission lines and terminations form a feedback system (as shown in Figure 6-3 on page 6-11). Because the feedback loop contains a delay, both the phase shift, and the sign of the feedback, change periodically, with the frequency. This causes oscillations in the frequency-domain response of the transmission lines, such as those shown in (b) in Figure 6-8 on page 6-23.

Handling Line-to-Line Junctions

An important special case occurs when the line terminates in another line. Figure 6-4 shows the system diagram for a line-to-line junction. You can use this diagram to:

- Solve multi-layered plane-wave propagation problems.
- Analyze common waveguide structures.
- Derive generalized transmission and reflection coefficient formulas.
- Derive scattering parameter formulas.

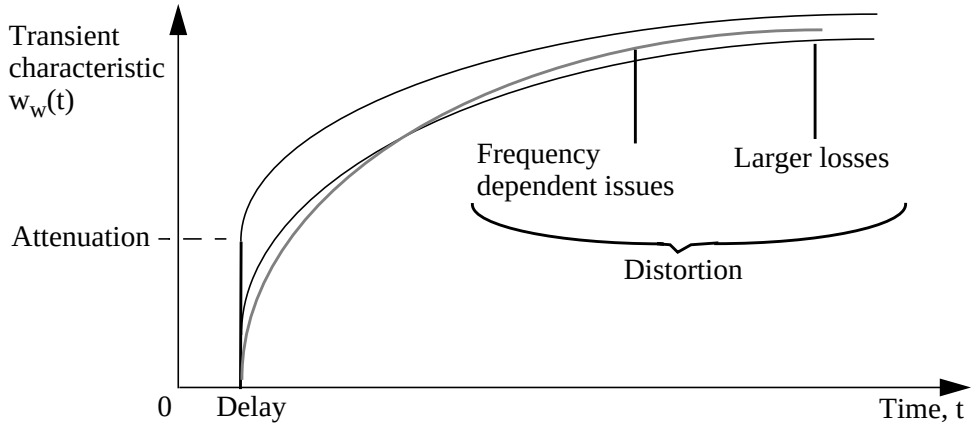
Figure 6-4: System Model for a Line-to-Line Junction



The W_{vr} and W_{vb} propagation functions describe how propagation (from one termination to another) affects a wave. These functions are equal for the forward (W_{vr}) and backward (W_{vb}) directions. The off-diagonal terms of the propagation functions represent the coupling between the conductors of a multi-conductor line.

As a wave propagates along the line, it experiences delay, attenuation, and distortion (see Figure 6-5). Lines with frequency-dependent parameters (that is, all real lines) do not contain the frequency-independent attenuation component.

Figure 6-5: Propagation Function Transient Characteristics (unit-step response)



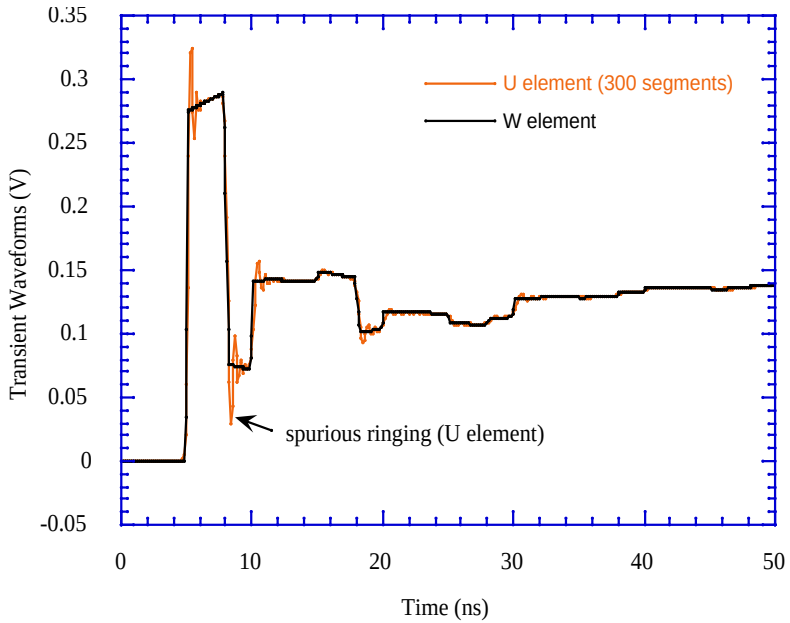
Using the W Element

The *W* element is a multi-conductor lossy frequency-dependent transmission line. It provides advanced modeling capabilities for transmission lines.

The *W* element provides:

- Ability to extract analytical solutions for AC and DC.
- No limit on the number of coupled conductors.
- No restriction on the structure of RLGC matrices; all matrices can be full.
- No spurious ringing, such as the lumped model produces (see Figure 6-6).
- Accurate modeling of frequency-dependent loss, in the transient analysis.
- Built-in 2D field solver, which you can use to specify the physical line shape.

Figure 6-6: Spurious Ringing in U Element



The *W* element supports the following types of analysis:

- DC
- AC
- Transient
- RF analyses (HB, HPAC, HPACNOISE, PHASENOISE, LIN)
- Parameter sweeps
- Optimization
- Monte-Carlo

Using Time-Step Control

The *W* Element provides accurate results with just 1-2 time steps per excitation transient (0.1 ns in the above example). This element supports iteration count (the `LVLTIM`=0 option) and `DVDT` (`LVLTIM`=1 or 3) time step control algorithms. It does not support the LTE (`LVLTIM`=2) algorithm yet. The default time-step control algorithm is `DVDT`.

The *W* Element limits the maximum time step by the smallest transmission line delay in the circuit.

The *W* Element supports the `TLINLIMIT` option, as the *T* Element does. The default value of `TLINLIMIT`=0 enables special breakpoint building. This improves transient accuracy for short lines, but reduces efficiency. To disable this special breakpoint building, set `TLINLIMIT`=1.

Longer transmission lines might experience prolonged time intervals when nothing happens at the terminals, while the wave propagates along the line. if you increase the time step, when the wave finally reaches the terminal, the accuracy of the simulation decreases To prevent this, for longer lines excited with short pulses, set the `.option DELMAX` to limit the time step to 0.5-1 of the excitation transient.

.OPTION RISETIME Setting

The *W* element uses the `.OPTION RISETIME` parameter to compute the maximum frequency range, for the transient analysis of the *W* Element. Depending on the value of this parameter, analysis uses one of the following methods to determine the maximum frequency:

- Positive value: The maximum frequency is the inverse of the value that you specify.
- No setting (recommended): Automatically determines the rise time from source statements. This method works for *most* cases. However, if the netlist contains the dependent source (which scales or shifts the frequency information), then you must explicitly set the rise time.
- Zero: The internal *W* element-bound algorithm computes the maximum frequency for each individual transmission line, and does **not** use the frequency information contained in source statements.

Input Syntax for the W Element

The W element supports four different formats, to specify the transmission line properties:

- Model 1: RLGC-Model specification
  - Internally specified in a `.model` statement.
  - Externally specified in a different file.
- Model 2: U-Model specification
  - RLGC input for up to five coupled conductors
  - Geometric input (planer, coax, twin-lead)
  - Measured-parameter input
  - Skin effect
- Model 3: Built-in field solver model
- Model 4: Frequency-dependent tabular model.

Syntax

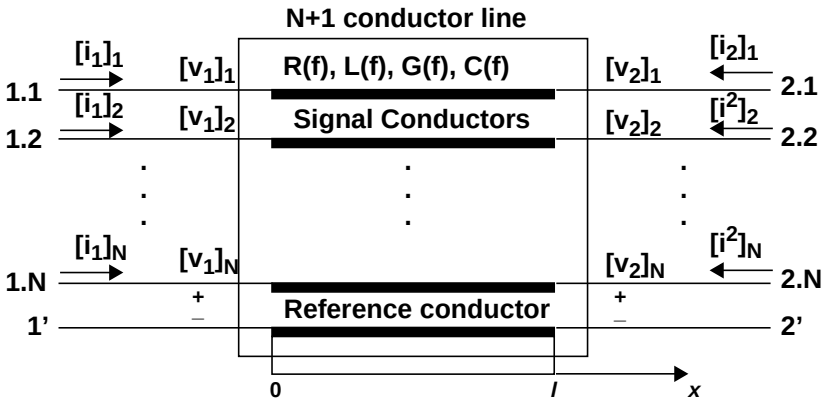
The syntax of the *W* Element statement is:

```
Wxxx i1 i2 ... iN iR o1 o2 ... oN oR N=val L=val
+ <RLGCMODEL=name or ROGCFILE=name or UMODEL=name
    FSMODEL=name
+ or TABLEMODEL=name> [ INCLUDERSIMAG=YES|NO FGD=val ]
```

where	specifies the
N	Number of signal conductors (excluding the reference conductor).
i1...iN	Node names for the near-end signal-conductor terminal (see Figure 6-7).
iR	Node name for the near-end reference-conductor terminal.
o1...oN	Node names for the far-end signal-conductor terminal (see Figure 6-7).
oR	Node name for the far-end reference-conductor terminal.
L	Length of the transmission line.
RLGCMODEL	Name of the RLGC model.
RLGCFILE	Name of the external file with RLGC parameters (see Input Model 1: W Element, RLGC Model on page 6-20).
UMODEL	Name of the U model (see Input Model 2: U Element, RLGC Model on page 6-28).
FSMODEL	Name of the field solver model.

where	specifies the
TABLEMODEL	Name of the frequency-dependent tabular model.
INCLUDERSIMAG	Imaginary term of the skin effect to be considered. The default value is YES. (see Frequency-Dependent Matrices on page 6-5).
FGD	Specifies the cut-off frequency of dielectric loss (see Handling Dielectrics on page 6-40).

Figure 6-7: Terminal Node Numbering



Normally, you can specify parameters in the W Element card in any order. Specify the number of signal conductors, *N*, after the list of nodes. You can intermix the nodes and parameters in the W Element card.

You can specify only one `RLGCmodel`, `FSmodel`, `Umodel`, or `RLGCfile` in a single W Element card.

Input Model 1: W Element, RLGC Model

Equations and Parameters on page 6-3 describes the inputs of the *W* element per unit length matrices:

- R_o
- L
- G
- C
- R_s (skin effect)
- G_d (dielectric loss)

The *W* element does not limit any of the following parameters:

- Number of coupled conductors.
- Shape of the matrices.
- Line loss.
- Length or amount of frequency dependence.

The RLGC text file contains frequency-dependent RLGC matrices per unit length.

The *W* element also handles frequency-independent RLGC, and lossless (LC) lines. It does not support RC lines.

Because RLGC matrices are symmetrical, the RLGC model specifies *only* the lower triangular parts of the matrices. The syntax of the RLGC model for the *W* element is:

```
.MODEL name W MODELTYPE=RLGC N=val Lo=matrix_entries
+ Co=matrix_entries [ Ro=matrix_entries
    Go=matrix_entries
+ Rs=matrix_entries Gd=matrix_entries Rognd=val
    Rsgnd=val
+ Lgnd=val ]
```

where	specifies the
N	Number of conductors (same as in the element card).
L	DC *inductance* matrix, per unit length $\left[\frac{H}{m}\right]$.
C	DC *capacitance* matrix, per unit length $\left[\frac{F}{m}\right]$.
R_o	DC *resistance* matrix, per unit length $\left[\frac{\Omega}{m}\right]$.
G_o	DC shunt *conductance* matrix, per unit length $\left[\frac{S}{m}\right]$.
R_s	Skin effect *resistance* matrix, per unit length $\left[\frac{\Omega}{m\sqrt{Hz}}\right]$.
G_d	Dielectric loss *conductance* matrix, per unit length $\left[\frac{S}{m \cdot Hz}\right]$.
L_{gnd}	DC *inductance* value, per unit length, for grounds $\left[\frac{H}{m}\right]$ (reference line).
R_{ognd}	DC *resistance* value, per unit length, for ground $\left[\frac{\Omega}{m}\right]$.
R_{sgnd}	Skin effect *resistance* value, per unit length, for ground $\left[\frac{\Omega}{m\sqrt{Hz}}\right]$.

Example

The following in an example of an input netlist file, showing the RLGC input usage for the *W* element:

```
* W-Element example, four-conductor line
W1 N=3 1 3 5 0 2 4 6 0 RLGCMODEL=example_rlc l=0.97
V1 1 0 AC=1v DC=0v pulse(4.82v 0v 5ns 0.1ns 0.1ns 25ns)

.AC lin 1000 0Hz 1GHz
.DC v1 0v 5v 0.1v
.tran 0.1ns 200ns

* RLGC matrices for a four-conductor lossy
.MODEL example_rlc W MODELTYPE=RLGC N=3

+ Lo=
+ 2.311e-6
+ 4.14e-7 2.988e-6
+ 8.42e-8 5.27e-7 2.813e-6
+ Co=
+ 2.392e-11
+ -5.41e-12 2.123e-11
+ -1.08e-12 -5.72e-12 2.447e-11

+ Ro=
+ 42.5
+ 0 41.0 + 0 0 33.5
+ Go= + 0.000609
+ -0.0001419 0.000599
+ -0.00002323 -0.00009 0.000502

+ Rs=
+ 0.00135
+ 0 0.001303
+ 0 0 0.001064

+ Gd=
+ 5.242e-13
+ -1.221e-13 5.164e-13
+ -1.999e-14 -7.747e-14 4.321e-13

.end
```

Figure 6-8 shows plots of the simulation results:

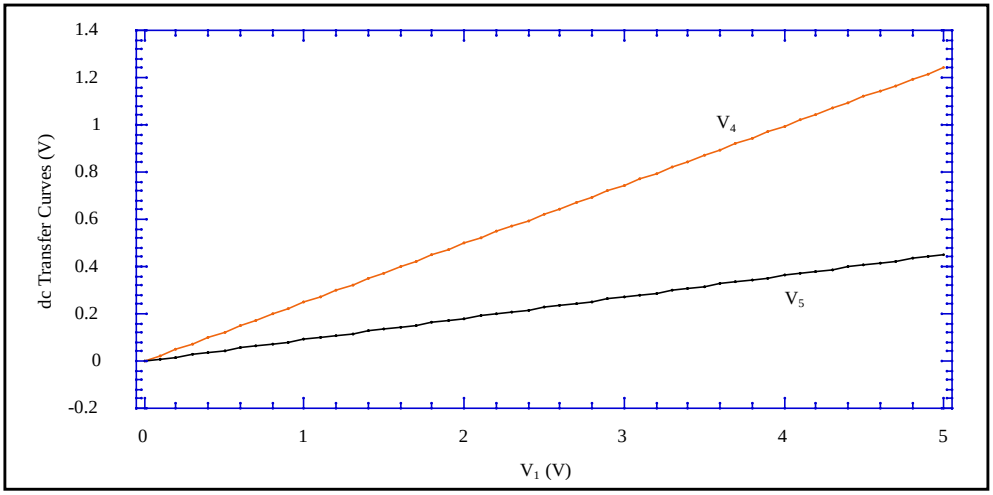
a) DC Sweep.

b) AC response.

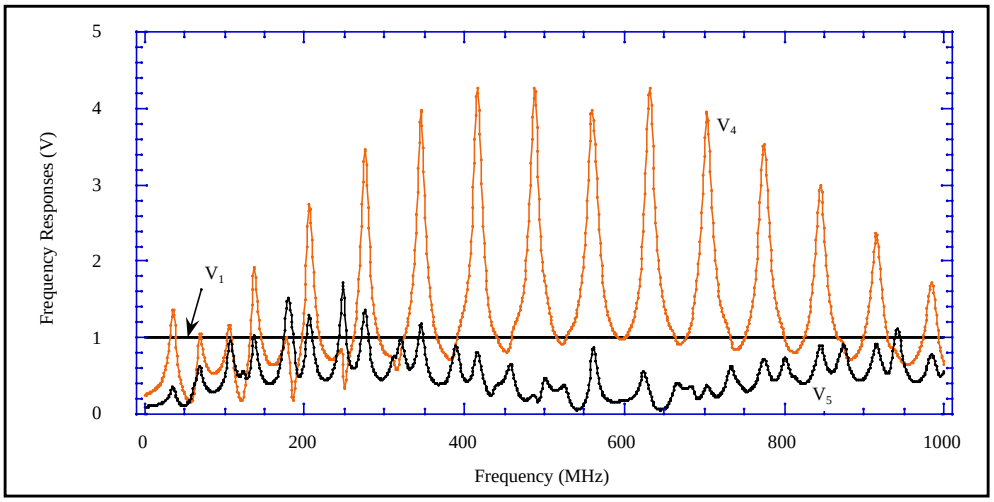
c) Transient waveforms.

Figure 6-8 also shows that the transmission line behavior of interconnects has a significant and complicated effect on the integrity of a signal. This is why it is very important to accurately model transmission lines when you verify high-speed designs.

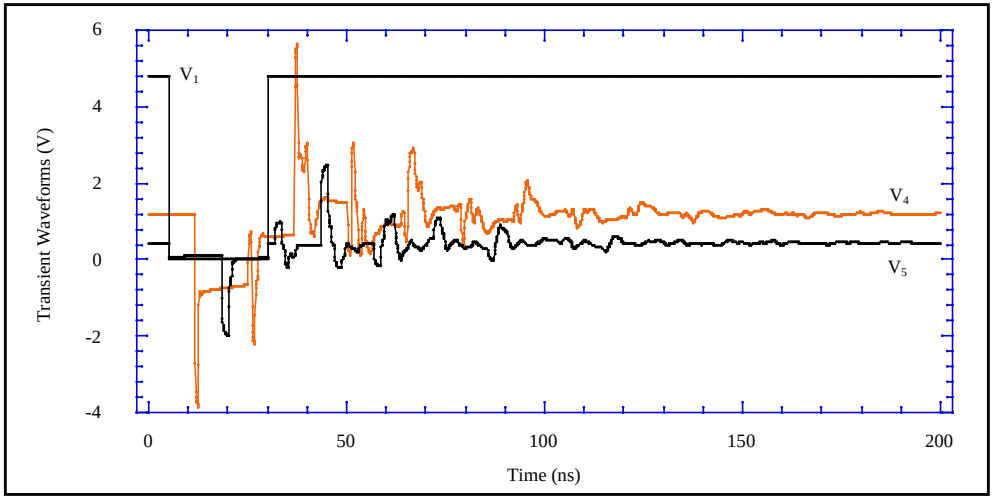
Figure 6-8: Simulation Results
(a) DC Sweep



(b) AC Response



(c) Transient Waveforms



Specifying the RLGC Model in an External File

You can also specify RLGC matrices in an external file (RLGC file). This external file format is more restricted than the RLGC model; for example:

- You cannot include any parameters.
- The file does not support ground inductance and resistance.

Note: This format does not provide any advantage over the RLGC model, so do not use it unless you already have an RLGC file. (It is supported *only* for backward-compatibility.)

The RLGC file specifies only the lower-triangular parts of the matrices. However, in external input, the RLGC file is order-dependent.

The parameters in the RLGC file are in the following order:

N	Number of conductors (same as in the element card).
L	DC *inductance* matrix, per unit length $\left[\frac{H}{m}\right]$.
C	DC *capacitance* matrix, per unit length $\left[\frac{F}{m}\right]$.
R_o (Optional)	DC *resistance* matrix, per unit length $\left[\frac{\Omega}{m}\right]$.
G_o (Optional)	DC shunt *conductance* matrix, per unit length $\left[\frac{S}{m}\right]$.
R_s (Optional)	Skin effect *resistance* matrix, per unit length $\left[\frac{\Omega}{m\sqrt{Hz}}\right]$.
G_d (Optional)	Dielectric loss *conductance* matrix, per unit length $\left[\frac{S}{m \cdot Hz}\right]$.

Note: You can skip optional parameters (they default to zero). But if you specify one of the optional parameters, then you must specify *all* of the preceding parameters, even if they are zero.

Comments and Separators

An asterisk * comments out everything until the end of its line. You can use any of the following characters to separate numbers:

space
tab
newline

,
;
(
)
[
]
{
}

Example

The following example of an RLGC file, is for the same netlist example used for the RLGC model (in the previous section):

```
* W- Element example, four-conductor line

W1 N=3 1 3 5 0 2 4 6 0 RLGCfile=example.rlc l=0.97
V1 1 0 AC=1v DC=0v pulse(4.82v 0v 5ns 0.1ns 0.1ns 25ns)

.AC lin 1000 0Hz 1GHz
.DC v1 0v 5v 0.1v
.tran 0.1ns 200ns

.end
```

This calls the following `example.rlc` RLGC file:

```
* RLGC parameters for a four-conductor lossy
* frequency-dependent line
* N (number of signal conductors)

3
* Lo
2.311e-6
4.14e-7 2.988e-6
8.42e-8 5.27e-7 2.813e-6

* Co
2.392e-11
-5.41e-12 2.123e-11
-1.08e-12 -5.72e-12 2.447e-11

* Ro
42.5
0 41.0
0 0 33.5

* Go
0.000609
-0.0001419 0.000599
-0.00002323 -0.00009 0.000502

* Rs
0.00135
0 0.001303
0 0 0.001064

* Gd
5.242e-13
-1.221e-13 5.164e-13
-1.999e-14 -7.747e-14 4.321e-13
```

The RLGC file does not support scale suffixes, such as:

```
n (10^-9) or p (10^-12)
```

Input Model 2: U Element, RLGC Model

The *W* Element accepts the *U* model as an input, to provide backward compatibility with the *U* Element. It also uses the geometric and measured-parameter interfaces of the *U* model.

To use the *W* Element with the *U* model, on the *W* Element card, specify:

```
Umodel=U-model_name
```

The *W* Element supports all *U*-model modes, including:

- Geometric, `Elev=1`
  - planar geometry, `Plev=1`
  - coax, `Plev=2`
  - twin-lead, `Plev=3`
- RLGC, `Elev=2`
- Measured parameters, `Elev=3`
- Skin-effect, `Nlay=2`

The only exception is `Llev=1`, which adds the second ground plane to the *U* model. The *W* Element does not support this. To model the extra ground plane, add an extra conductor to the *W* Element in `Elev=2`, or use an external lumped capacitor in `Elev=1` or `Elev=3`. For information about the U model, see Appendix A, “Ideal and Lumped Transmission Lines”.

Using RLGC Matrices

RLGC matrices, in the RLGC model of the W element, are in the Maxwellian format. In the *U* model, they are in self/mutual format. For conversion information, see Determining Matrix Properties on page 6-6. When you use the *U* model, the W element performs the conversion internally. Table 6-1 on page 6-30 shows how the RLGC matrices in the *U*-model are related to the RLGC matrices in the *W* element, and how the *W* element uses these matrices.

Handling the Dielectric-loss Matrix

Because the *U* model does not input the G_d dielectric loss matrix, the *W* element defaults G_d to zero when it uses the *U*-model input.

Handling the Skin-effect Matrix

The *U* and *W* elements use the R_S skin-effect resistance in different ways.

- In a *W* Element, the R_S matrix specifies the square-root dependence of the frequency-dependent resistance:

$$\mathbf{R}(f) \cong \mathbf{R_o} + \sqrt{f}(1 + j)\mathbf{R_s}$$

- In a *U* element, *R* is the value of skin resistance at the frequency:

$$\mathbf{R} \cong \mathbf{R_c} + \mathbf{R_s}$$

where the core resistance (R_C) is equivalent to the DC resistance (R_O) in the *W* element. The frequency at which the *U* element computes the *R* matrix is:

$$f_{skin} = \frac{1}{15 \cdot \text{RISETIME}}$$

For U models with	W Element
RLGC input; `Elev=2`	Uses the R_S values that you specify in the *U* model.
Geometric input; `Elev=1`	Divides the R_S (which the U model computes internally), by $\sqrt{f_{skin}}$, to obtain the R_S value. For `Elev=1`, the value of R_S in the *U* model printout is not the same as the R_S value that the *W* element actually uses.
Measured-parameter input; `Elev=3`	Does not support the skin effect.

If you do not specify the RISETIME option, the *U* element uses *Tstep* from the `.tran` card.

Table 6-1: RLGC Matrices in the W Element and the U Model

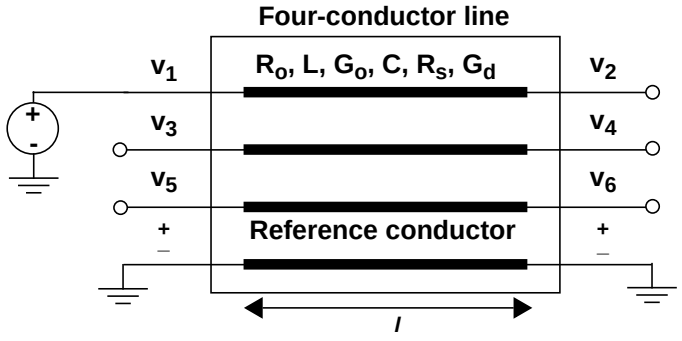
W Element Parameters	U Model Parameters
L, C	$\begin{bmatrix} L_{11} & & \\ L_{12} & L_{22} & \\ L_{13} & L_{23} & L_{33} \end{bmatrix}$	$\begin{bmatrix} C_{r1}+C_{12}+C_{13} & & \\ -C_{12} & C_{r2}+C_{12}+C_{23} & \\ -C_{13} & -C_{23} & C_{r3}+C_{13}+C_{23} \end{bmatrix}$
G_o, G_d	$\begin{bmatrix} G_{r1}+G_{12}+G_{13} & & \\ -G_{12} & G_{r2}+G_{12}+G_{23} & \\ -G_{13} & -G_{23} & G_{r3}+G_{13}+G_{23} \end{bmatrix}$	$\begin{bmatrix} 0 & & \\ 0 & 0 & \\ 0 & 0 & 0 \end{bmatrix}$
	`Nlay`=1 (no skin effect)	`Nlay`=2 (skin effect present)
R_o	$\begin{bmatrix} R_{11}+R_{rr} & & \\ R_{rr} & R_{22}+R_{rr} & \\ R_{rr} & R_{rr} & R_{33}+R_{rr} \end{bmatrix}$	$\begin{bmatrix} R_{1c}+R_{rc} & & \\ R_{rc} & R_{2c}+R_{rc} & \\ R_{rc} & R_{rc} & R_{3c}+R_{rc} \end{bmatrix}$
	`Nlay`=1 (no skin effect)	`Nlay`=2 (skin effect present)
R_s	$\begin{bmatrix} 0 & & \\ 0 & 0 & \\ 0 & 0 & 0 \end{bmatrix}$	$\frac{1}{\sqrt{f_{skin}}}\begin{bmatrix} R_{1s}+R_{rs} & & \\ R_{rs} & R_{2s}+R_{rs} & \\ R_{rs} & R_{rs} & R_{3s}+R_{rs} \end{bmatrix}$

Example

The following netlist is for a 4-conductor line, shown in Figure 6-9.

```
* W Element example, four-conductor line, U model
W1 1 3 5 0 2 4 6 0 Umodel=example N=3 l=0.97
.MODEL example U LEVEL=3 NL=3 Elev=2 Llev=0 Plev=1
   Nlay=2
+
+ L11=2.311uH
+ L12=0.414uH L22=2.988uH
+ L13=84.2nH L23=0.527uH L33=2.813uH
+
+ Cr1=17.43pF
+ C12=5.41pF Cr2=10.1pF
+ C13=1.08pF C23=5.72pF Cr3=17.67pF
+
+ R1c=42.5 R2c=41.0 R3c=33.5
+
+ Gr1=0.44387mS
+ G12=0.1419mS Gr2=0.3671mS
+ G13=23.23uS G23=90uS Gr3=0.38877mS
+
+ R1s=0.00135 R2s=0.001303 R3s=0.001064
V1 1 0 AC=1v DC=0v pulse(4.82v 0v 5ns 0.1ns 0.1ns 25ns)
.AC lin 1000 0Hz 1GHz
.DC v1 0v 5v 0.1v
.TRAN 0.1ns 200ns
.END
```

Figure 6-9: 4-Conductor Line



Input Model 3: Built-in Field-Solver Model

Instead of RLGC matrices, you can directly use geometric data with the *W* Element, using a built-in field solver. To use the *W* element with a field solver, specify `FSmodel=<model_name>` on the *W* element card. For a description of the built-in field solver, see Extracting Transmission Line Parameters (Field Solver) on page 6-37.

Input Model 4: Frequency-Dependent Tabular Model

You can use the tabular RLGC model as an extension of the analytical RLGC model, to model any arbitrary, frequency-dependent behavior of transmission lines (this model does not support RC lines).

You can use this extension of the *W* element syntax to specify a table model (use a `.MODEL` statement of type `w`). To accomplish this, the `.MODEL` statement refers to `.MODEL` statements where the *type* is `SP` (described in Frequency Table Model on page 6-60), which contain the *actual* table data for the RLGC matrices.

Notation Used

- Lower-case variable: Scalar quantity
- Upper-case variable: Matrix quantity
- All upper-case words: Keyword
- Parentheses and commas: Optional

Syntax for Table Model Card

```
.MODEL name W MODELTYPE=TABLE N=val LMODEL=l_freq_model
+ CMODEL=c_freq_model [ RMODEL=r_freq_model
+ GMODEL=g_freq_model ]
```

where	specifies the
N	Number of signal conductors (excluding the reference conductor).
LMODEL	SP model name for the *inductance* matrix array.
CMODEL	SP model name for the *capacitance* matrix array.
RLMODEL	SP model name for the *resistance* matrix array. By default, it is zero.
GMODEL	SP model name for the *conductance* matrix array. By default, it is zero.

Example 1

This is an example of a 2-line system.

```
.MODEL ex1 W MODELTYPE=TABLE N=2 LMODEL=lmod1
+ CMODEL=cmod1 RMODEL=rmod1 GMODEL=gmod1
.MODEL lmod1 sp N=2 SPACING=NONUNIFORM VALTYPE=REAL
+ DATA=( 1,
+ (0.000000e+00 5.602360e-11 -7.047240e-12)
+ )
.MODEL lmod1 N=2 SPACING=NONUNIFORM VALTYPE=REAL
+ INFINITY=(3.93346e-7 4.93701e-8 3.93346e-7)
+ DATA=( 34,
+ (0.000000e+00 3.933460e-07 4.937010e-08 3.933460e-07)
+ (3.746488e+06 4.152139e-07 4.937010e-08 4.151959e-07)
........
+ (4.000000e+09 3.940153e-07 4.937010e-08 3.940147e-07)
+ )
```

```
.MODEL rmod1 N=2 SPACING=NONUNIFORM VALTYPE=REAL
+ DATA=( 34,
+ (0.000000e+00 8.779530e-02 6.299210e-03 8.779530e-02)
+ (3.746488e+06 6.025640e-01 6.299210e-03 6.021382e-01)
........
+ (4.000000e+09 1.690795e+01 6.299210e-03 1.689404e+01)
+ )
.MODEL gmod1 N=2 SPACING=NONUNIFORM VALTYPE=REAL
+ DATA=( 34,
+ (0.000000e+00 5.967166e-11 0.000000e+00 5.967166e-11)
+ (3.746488e+06 1.451137e-05 -1.821096e-06 1.451043e-05)
........
+ (4.000000e+09 1.549324e-02 -1.944324e-03 1.549224e-02)
+ )
```

SP .MODEL Syntax

See Frequency Table Model on page 6-60.

Example 2

This is an example of a 4-conductor transmission line system.

Table 6-2: Input File Listing

Header, options and sources	`W Element Tabular Model Example`
	`.OPTIONS POST`
	`V1 7 0 ac=1v dc=0.5v pulse(0.5v 1.5v 0ns 0.1ns)`
	`V2 8 0 dc=1v`

Analysis	`.DC v1 0.5v 5.5v 0.1v SWEEP length POI 2 1.2 2`
	`.AC lin 200 0Hz 1GHz SWEEP Ro POI 3 400 41.6667 400`
	`.TRAN 0.1ns 50ns`

Termination	`R1 7 1 50`
	`R2 4 0 450`
	`R3 5 0 450`
	`R8 6 0 450`
	`R5 4 5 10800`
	`R6 5 6 10800`
	`R7 4 6 1393.5`

Analytical RLGC model (*W* Element)	.SUBCKT sub 1 2 3 4 5 6 7 8 W1 n=3 1 2 3 4 5 6 7 8 l=0.1 fgd=5e6 RLGCMODEL=analymod .MODEL analymod W MODELTYPE=RLGC N=3 + Lo=2.41667e-6 + 0.694444e-6 2.36111e-6 + 0.638889e-6 0.694444e-6 2.41667e-6 + Co=20.9877e-12 + -12.3457e-12 29.3210e-12 + -4.01235e-12 -12.3457e-12 20.9877e-12 + Ro=41.6667 + 0 41.6667 + 0 0 41.6667 + Go=0.585937e-3 + 0 0.585937e-3 + 0 0 0.585937e-3 + Rs=0.785e-5 + 0 0.785e-5 + 0 0 0.785e-5 + Gd=0.285e-6 + 0 0.285e-6 + 0 0 0.285e-6 .ENDS sub
Tabular RLGC model (*W* Element)	.ALTER Tabular Model .SUBCKT sub 1 2 3 4 5 6 7 8 W1 n=3 1 2 3 4 5 6 7 8 l=0.1 fgd=5e6 tablem odel=trmod .INCLUDE table.txt .ENDS sub

Table 6-3: Tabular RLGC Model

RLGC table model definition	.MODEL trmod W MODELTYPE=TABLE N=3 + LMODEL=lmod CMODEL=cmod RMODEL=rmod GMODEL=gmod
C model	.MODEL cmod sp N=3 VALTYPE=REAL INTERPOLATION=LINEAR + DATA=(1 2.09877e-11 -1.23457e-11 2.9321e-11 + -4.01235e-12 -1.23457e-11 2.09877e-11)
L model	.MODEL lmod sp N=3 VALTYPE=REAL INTERPOLATION=LINEAR + INFINITY= 2.41667e-06 6.94444e-07 2.36111e-06 + 6.38889e-07 6.94444e-07 2.41667e-06 FSTOP=1e+07 + DATA=(25 + 2.41667e-06 6.94444e-07 2.36111e-06 6.38889e-07 + 6.94444e-07 2.41667e-06 2.41861e-06 6.94444e-07 ... + 2.41707e-06 6.94444e-07 2.36151e-06 6.38889e-07 + 6.94444e-07 2.41707e-06)
R model	.MODEL rmod sp N=3 VALTYPE=REAL INTERPOLATION=LINEAR + FSTOP=1e+10 + DATA=(200 + 41.6667 0 41.6667 0 0 41.6667 + 41.7223 0 41.7223 0 0 41.7223 ... + 42.4497 0 42.4497 0 0 42.4497 + 42.4517 0 42.4517 0 0 42.4517)
G model	.MODEL gmod sp N=3 VALTYPE=REAL INTERPOLATION=LINEAR + FSTOP=1e+08 + DATA=(100 + 0.000585937 0 0.000585937 0 0 0.000585937 + 0.282764 0 0.282764 0 0 0.282764 ... + 1.42377 0 1.42377 0 0 1.42377 + 1.42381 0 1.42381 0 0 1.42381)

Extracting Transmission Line Parameters (Field Solver)

The built-in 2-D electromagnetic field solver is highly-optimized for interconnects in stratified media. This field solver uses the *W* element, and it supports optimization and statistical analysis within transient simulation.

The solver is based on:

- An improved version of the boundary-element method[5], and
- The filament method that is also implemented in Raphael[6].

Filament Method

This section describes the filament method, for the skin-effect resistance and inductance solver.

The 2D filament method uses data about magnetic coupling when it extracts frequency-dependent resistance and inductance. To use this solver, set **COMPUTERS=yes** in the `.fsoption`.

1. The filament method divides the original conductor system into thin filaments.
2. From the coupling of these filaments, this method then derives the distributed magnetic coupling of the inside and outside of the conductor.
3. After dividing the conductors into thin filaments, this method creates the impedance matrix of the filament system:

   $\mathbf{Z}_f \quad (= \mathbf{R}_f + j\omega\mathbf{L}_f)$

[5]K. S. Oh, D. B. Kuznetsov, and J. E. Schutt-Aine, “Capacitance computations in a multi-layered dielectric medium using closed-form spatial Green s functions,” *IEEE Trans. Microwave Theory and Tech.*, vol. 42, pp. 1443-1453, August 1994. 2.

[6]*Raphael Reference Manual*, Avant! Corporation, December 1998.

4. This method use the following equation to solve the current matrix (i_f):

   $$\mathbf{v}_f = \mathbf{Z}_f \mathbf{i}_f$$

   Where v_f is an excitation vector for the filament system.

5. The filament method uses the result of this equation to calculate the partial current matrix of the conductor system i_p, as a sum of all filament currents:

   $$i_{p(j,k)} = \sum_{\text{filaments in conductor j}} i_f \quad (@ \text{ k-th excitation vector})$$

6. The filament method use the following equation to solve the partial impedance matrix (Z_p):

   $$\mathbf{v}_p = \mathbf{Z}_p \mathbf{i}_p$$

7. From the components of the partial impedance matrix, the filament method uses the following relationship to calculate the components of the loop $z_{p(j,k)}[j, k:0\sim n]$ impedance matrix:

   $$z_{l(j,k)} = z_{p(j,k)} - z_{p(j,0)} - z_{p(k,0)} + z_{p(0,0)}$$

   Where *n* is the number of signal (non-reference) conductors in the system.

Note: *W* element analysis uses these loop impedance components.

Modeling Geometries

In geometry modeling:

- The number of dielectric layers is arbitrary.
- You can arbitrarily shape the conductor cross-section, including an infinitely-thin strip.
- The number of conductors is unlimited.
- The current dielectric region must be planar.
- Conductors must not overlap each other.
- Magnetic materials are not supported.

Geometric modeling outputs the Maxwellian (short-circuit) transmission line matrices: **C**, **L**, $\mathbf{R_o}$, $\mathbf{R_s}$, $\mathbf{G_o}$, and $\mathbf{G_d}$ (see Equations and Parameters on page 6-3).

Solver Limitation

When the field solver computes the conductance matrices (G_o and G_d), if the media are not homogeneous, then the solver uses the arithmetic average values of conductivities and loss tangents.

Field-Solver Statement Syntax

The netlist input syntax contains five statements that specifically relate to the field solver:

Statement	Defines
`.MATERIAL`	Material properties.
`.LAYERSTACK`	Stacking of materials.
`.SHAPE`	Material shapes.
`.FSOPTIONS`	Field solver options.
`.MODEL W MODELTYPE=FieldSolver`	Type of transmission-line model.

Defining Material Properties (.MATERIAL)

Use the `.MATERIAL` statement to define the properties of a material.

Syntax

```
.MATERIAL mname METAL|DIELECTRIC <ER=val> <UR=val>
+ <CONDUCTIVITY=val> <LOSSTANGENT=val>
```

Parameter	Specifies
mname	Material name.
METAL|DIELECTRIC	Material type: METAL or DIELECTRIC.
ER	Dielectric constant (relative permittivity).
UR	Relative permeability.
CONDUCTIVITY	Static field conductivity of conductor or lossy dielectric (S/m).
LOSSTANGENT	Alternating field loss tangent of dielectric (tan δ).

Handling Metals

The field solver assigns the following default values for metal:

- CONDUCTIVITY = -1 (perfect conductor)
- ER = 1
- UR = 1

PEC is a pre-defined metal name. You cannot redefine its default values.

Handling Dielectrics

The field solver assigns the following default values for dielectrics:

- CONDUCTIVITY = 0 (lossless dielectric)
- LOSSTANGENT = 0 (lossless dielectric)
- ER = 1
- UR = 1

AIR is a pre-defined dielectric name. You cannot redefine its default values.

Note: Because the field solver does not currently support magnetic materials, it ignores UR values.

Creating Layer Stacks (.LAYERSTACK)

A layer stack defines a stack of dielectric or/and metal layers. You must associate each transmission line system with *one*, and *only* one, layer stack. However, you can associate a single-layer stack with *many* transmission line systems.

Syntax

```
.LAYERSTACK sname <BACKGROUND=mname>
+ <LAYER=(mname,thickness) ...>
```

Parameter	Specifies
sname	Layer stack name.
mname	Material name.
BACKGROUND	Background dielectric material name. By default, the Field Solver assumes AIR for the background.
thickness	Layer thickness.

In the layer stack:

- Layers are listed from bottom to top.
- Metal layers (ground planes) are located only at the bottom, only at the top, or both at the top and bottom.
- Layers are stacked in the y-direction, and the bottom of a layer stack is at y=0.
- All conductors must be located above y=0.
- Background material must be dielectric.

Limiting Cases

- Free space without ground:

  ```
  .LAYERSTACK mystack
  ```

- Free space with a (bottom) ground plane:

  ```
  .LAYERSTACK halfSpace PEC 0.1mm
  ```

Defining Shapes (.SHAPE)

Use the .SHAPE statement to define a shape. The Field Solver uses the shape to describe a cross-section of the conductor.

Syntax

```
.SHAPE sname Shape_Descriptor
```

Parameter	Specifies
sname	Shape name.
Shape_Descriptor	One of the following: ■ Rectangle. ■ Circle. ■ Strip. ■ Polygon.

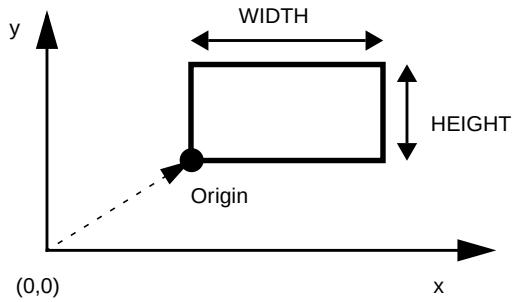
Defining Rectangles

Use a shape descriptor that defines a rectangle:

```
RECTANGLE WIDTH=val HEIGHT=val <NW=val> <NH=val>
```

Parameter	Specifies
WIDTH	Width of the rectangle (size in the *x*-direction).
HEIGHT	Height of the rectangle (size in the *y*-direction).
NW	Number of horizontal (x) segments that define the rectangle, with the specified width.
NH	Number of vertical (y) segments that define the rectangle, with the specified height.

Figure 6-10: Coordinates of a Rectangle



Note: Normally, you do not need to specify the NW and NH values, because the field solver automatically sets these values, depending on the **accuracy** mode. But you can specify both values, or specify only *one* of these values and let the solver determine the other.

Defining Circles

Use a shape descriptor that defines a circle:

```
CIRCLE RADIUS=val <N=val>
```

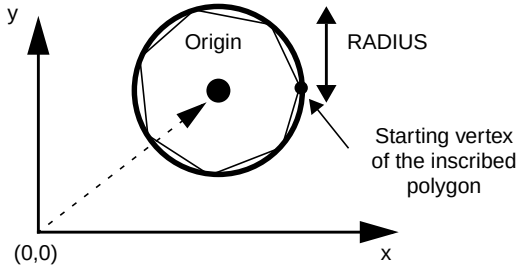
The Field Solver approximates a circle as an inscribed regular polygon, with *N* edges. The more edges, the more accurate the circle approximation is.

Note: Do not use the `CIRCLE` descriptor to model actual polygons; instead use the `POLYGON` descriptor.

Parameter	Specifies
RADIUS	Radius of the circle.
N	Number of segments to use, to approximate the circle, with the specified radius.

Note: Normally, you do not need to specify the N value, because the field solver automatically sets this value, depending on the **accuracy** mode. But you can specify this value if you need to.

Figure 6-11: Coordinates of a Circle



Defining Strips

This shape descriptor defines an infinitesimally-thin strip:

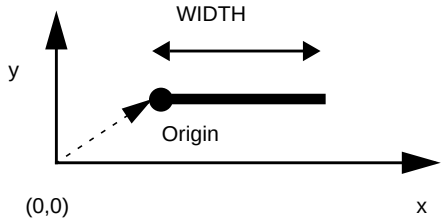
```
STRIP WIDTH=val <N=val>
```

Note: The field solver (filament method) does not support this shape.

Parameter	Specifies
WIDTH	Width of the strip (size in the *x*-direction).
N	Number of segments that define the strip shape, with the specified width.

Note: Normally, you do not need to specify the N value, because the field solver automatically sets this value, depending on the **accuracy** mode. But you can specify this value if you need to.

Figure 6-12: Coordinates of a Strip Polygon



Defining Polygons

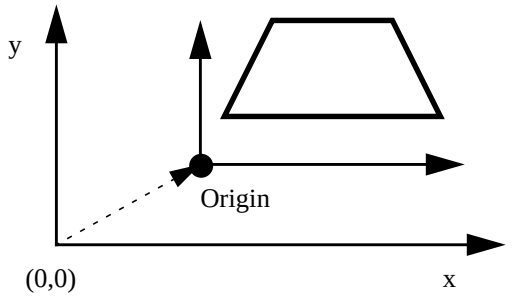
Use a shape descriptor that defines a polygon:

```
POLYGON VERTEX=(x1 y1 x2 y2 ...) <N=(n1,n2,...)>
```

The specified coordinates are within the local coordinate, with respect to the origin of a conductor.

Parameter	Specifies
VERTEX	(*x*, *y*) coordinates of vertices. Listed either in clockwise or counter-clockwise direction.
N	Number of segments that define the polygon, with the specified *X* and *Y* coordinates. You can specify a different *N* value for each edge. If you specify only one *N* value, then the Field Solver uses this value for *all* edges. For example, the first value of *N*, *n1*, corresponds to the number of segments for the edge from (*x1 y1*) to (*x2 y2*).

Figure 6-13: Coordinates of a Polygon



Examples

- Rectangular polygon, using the default number of segments:

```
POLYGON VERTEX=(1 10 1 11 5 11 5 10)
```

- Rectangular polygon, using five segments for each edge:

```
POLYGON VERTEX=(1 10 1 11 5 11 5 10) N=5
```

- Rectangular polygon, using the different number of segments for each edge:

```
POLYGON VERTEX=(1 10 1 11 5 11 5 10) N=(5 3 5 3)
```

Field-Solver Options (.FSOPTIONS)

Use the FSOPTIONS statement to set various options for the field solver.

Syntax

```
.FSOPTIONS name <ACCURACY=LOW|MEDIUM|HIGH>
+ <GRIDFACTOR=val> <PRINTDATA=YES|NO> <COMPUTEG0=YES|NO>
+ <COMPUTEGD=YES|NO> <COMPUTERO=YES|NO> <COMPUTERS=YES|NO>
```

Option	Description	Default Value
name	Option name.	
ACCURACY	Sets the solver accuracy to one of the following: ■ LOW ■ MEDIUM ■ HIGH	HIGH
GRIDFACTOR	Multiplication factor (integer) to determine the final number of segments used to define the shape. **Note:** The field solver does not currently use this parameter.	1
PRINTDATA	Specifies that the solver prints output matrices.	NO
COMPUTEGO	Specifies that the solver computes the static conductance matrix.	YES
COMPUTEGD	Specifies that the solver computes the dielectric los matrix.	NO
COMPUTERO	Specifies that the solver computes the DC resistance matrix.	YES

Option	Description	Default Value
COMPUTERS	Specifies that the solver computes the skin-effect resistance matrix.	NO

Note: This parameter invokes the field solver.

- The field solver always computes the L and C matrices.
- If COMPUTERS=YES, then the field solver starts, and calculates L_o, R_o, and R_s.
- For each accuracy mode, the field solver uses either the pre-defined number of segments, or the number of segments that you specified. It then multiplies this number times the GRIDFACTOR, to obtain the final number of segments.

Note: Because a wide range of applications are available, the pre-defined accuracy level might not be accurate enough for certain applications. If you need a higher accuracy than the value that the HIGH option sets, then increase either the GRIDFACTOR value, or the N/NH/NW values, to increase the mesh density.

Using the Field Solver Model (.MODEL W MODELTYPE=FieldSolver)

Use the field-solver model to specify a geometry model for the W Element transmission line. In the field-solver model:

- The list of conductors must appear last.
- Conductors cannot overlap each other.
- The Field Solver assumes that floating conductors are electrically disconnected, and does not support non-zero fixed charges. Because the field solver is designed as 2D, it ignores displacement current in floating conductors.

- The Field Solver treats metal layers in the layer stack, as the reference node.
- Conductors defined as REFERENCE are all electrically-connected, and correspond to the reference node in the *W* Element.
- You must place signal conductors in the same order as the terminal list in the W Element statement. For example, the i^{th} signal conductor (not counting reference and floating conductors), is associated with the i^{th} input and output terminals, specified in the corresponding *W* Element.
- Floating and reference conductors can appear in any order.

Syntax

```
.MODEL mname W MODELTYPE=FieldSolver LAYERSTACK=name
+ <FSOPTIONS=name> <RLGCFILE=name>
+ <OUTPUTFORMAT=RLGC|RLGCFILE>
+ CONDUCTOR=( SHAPE=name <MATERIAL=name> <ORIGIN=(x,y)>
+ <TYPE=SIGNAL|REFERENCE|FLOATING> ) ...
```

Parameter	Specifies
mname	Model name.
LAYERSTACK	Name of the associated layer stack.
FSOPTIONS	Associated option name. If you do not specify this entry, the field solver uses the default options.
RLGCFILE	Use the output file for RLGC matrices, instead of the standard error output device. If the specified file already exists, then the Field Solver appends the output.

Note: To generate output, you must set PRINTDATA in .FSOPTIONS to **YES** (which is the default).

Parameter	Specifies
OUTPUTFORMAT	Model syntax format for RLGC matrices, in the *W* Element. Specified in the RLGCFILE. The default format is an RLGC model.
SHAPE	Shape name.
x y	Coordinates of the local origin.
MATERIAL	Conductor material name. If you do not specify this entry, the Field Solves uses PEC by default.
TYPE	One of the following conductor types: ■ SIGNAL: a signal node in the *W* Element. ■ REFERENCE: the reference node in the *W* Element. ■ FLOATING: floating conductor, no reference to the *W* Element. The default value of **TYPE** is SIGNAL.

Field Solver Examples

The following examples show you how to use the field solver. All of the examples shown in this section run with the HIGH accuracy mode and GRIDFACTOR = 1.

Example 1: Cylindrical Conductor Above a Ground Plane

The first example is a copper cylindrical conductor, above an ideal (lossless) ground plane.

- Figure 6-14 shows the geometry.
- Table 6-4 on page 6-52 lists the corresponding netlist.

In this example, you can derive the exact analytical formulas for all of the transmission line parameters[7]:

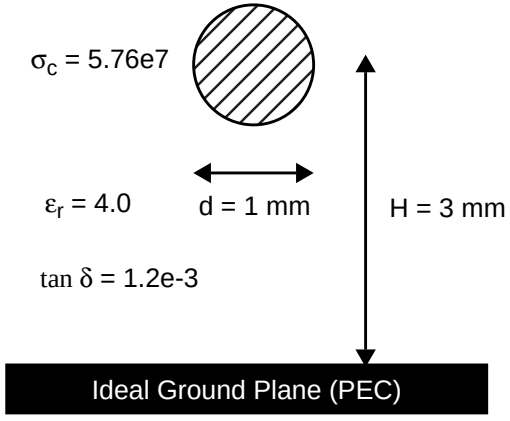
$$L = \frac{1}{\mu\varepsilon}C^{-1}$$

$$G = \frac{\sigma_d}{\varepsilon}C = \omega \cdot \tan(\delta) \cdot C$$

$$R = \frac{1}{\sigma_c \delta \pi d}\left[\frac{2H/d}{\sqrt{(2H/d)^2 - 1}}\right] = \sqrt{f}\sqrt{\frac{\pi\mu}{\sigma_c}}\frac{1}{\pi d}\left[\frac{2H/d}{\sqrt{(2H/d)^2 - 1}}\right]$$

Figure 6-14: Cylindrical Conductor Above a Ground Plane

$$C = \frac{2\pi\varepsilon}{\operatorname{acosh}\left(\frac{2H}{d}\right)}$$



[7]S. Ramo, J. R. Whinnery, and T. V. Duzer, *Fields and Waves in Communication Electronics*, 2nd ed. New York: Wiley, 1984.

Table 6-4: Input File Listing for Example 1

Header, options and sources	`*Example 1: cylindrical conductor`
	`.OPTION PROBE POST`
	`VIMPULSE in1 gnd PULSE 4.82v 0v 5n 0.5n 0.5n 25n`

W Element	`W1 in1 gnd out1 gnd FSmodel=cir_trans N=1 l=0.5`

Materials	`.MATERIAL diel_1 DIELECTRIC ER=4,`
	`+ LOSSTANGENT=1.2e-3`
	`.MATERIAL copper METAL`
	`+ CONDUCTIVITY=57.6meg`

Shapes	`.SHAPE circle_1 CIRCLE RADIUS=0.5mm`
Defines a half-space	`.LAYERSTACK halfSpace BACKGROUND=diel_1,` `+ LAYER=(PEC,1mm)`
Option settings	`.FSOPTIONS opt1 PRINTDATA=YES,` `+ COMPUTERS=yes, COMPUTEGD=yes`

Model definition	`.MODEL cir_trans W MODELTYPE=FieldSolver`
	`+ LAYERSTACK=halfSpace, FSOPTIONS=opt1,`
	`+ RLGCFILE=ex1.rlgc`
	`+ CONDUCTOR=(SHAPE=circle_1,`
	`+ ORIGIN=(0,4mm), MATERIAL=copper)`

Analysis, outputs and end	`.TRAN 0.5n 100n`
	`.PROBE v(out1)`
	`.END`

Compare the computed results with the analytical solutions in Table 6-5. The Field Solver computes the resistance and conductance at the frequency of 200 MHz, but does not include the DC resistance (R_o) and conductance (G_o) in the computed values.

Table 6-5: Comparison Result for Example 1

Value	Exact	Computed
C (pF/m)	89.81	89.66
L (nH/m)	494.9	495.7
G (mS/m)	0.1354	0.1352
R (Ω/m)	1.194	1.178

Example 2: Stratified Dielectric Media

Figure 6-15 shows an example of three traces immersed in stratified dielectric media. Table 6-6 shows the input file. Table 6-7 compares the computed capacitance matrix with the results from two other numerical methods.

Figure 6-15: Three Traces Immersed in Stratified Dielectric Media

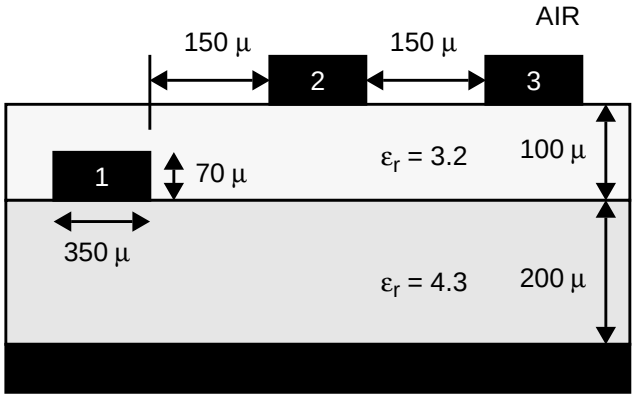


Table 6-6: Input File Listing for Example 2

Header, options and sources	`*Example 2, three traces in dielectric`
	`.OPTION PROBE POST`
	`+ VIMPULSE in1 gnd PULSE 4.82v 0v 5n 0.5n 0.5n`
	`+ 25n`

W Element	`W1 in1 in2 in3 gnd out1 out2 out3 gnd` `+ FSmodel=cond3_sys N=3 l=0.5`
Materials	`.MATERIAL diel_1 DIELECTRIC ER=4.3` `.MATERIAL diel_2 DIELECTRIC ER=3.2`
Shapes	`.SHAPE rect_1 RECTANGLE WIDTH=0.35mm,` `+ HEIGHT=0.07mm`

Uses the default AIR background	`.LAYERSTACK stack_1`
	`+ LAYER=(PEC,1um),LAYER=(diel_1,0.2mm),`
	`+ LAYER=(diel_2,0.1mm)`

Option settings	`.FSOPTIONS opt1 PRINTDATA=YES`

Three conductors share the same shape	`.MODEL cond3_sys W MODELTYPE=FieldSolver,`
	`+ LAYERSTACK=stack1, FSOPTIONS=opt1,`
	`+ RLGCFILE=ex2.rlgc`
	`+ CONDUCTOR=(SHAPE=rect_1,ORIGIN=`
	`+ (0,0.201mm)),`
	`+ CONDUCTOR=(SHAPE=rect_1,`
	`+ ORIGIN=(0.5mm,0.301mm)),`
	`+ CONDUCTOR=(SHAPE=rect_1,ORIGIN=`
	`+ (1mm,0.301mm))`

Analysis, outputs and end	`.TRAN 0.5n 100n`
	`.PROBE v(out1)`
	`.END`

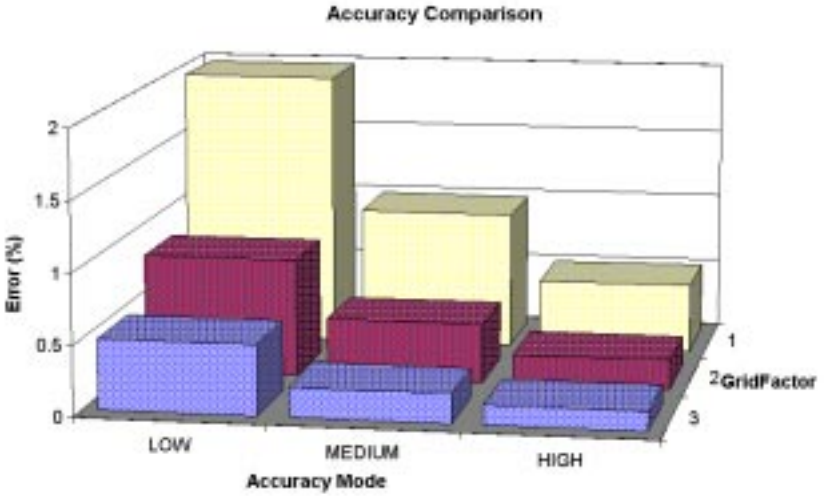
Table 6-7: Comparison Result for Example 2

Computed	$\begin{bmatrix} 141.1 & -21.36 & -0.90 \\ -21.36 & 92.66 & -17.72 \\ -0.90 & -17.72 & 87.26 \end{bmatrix}$ (pF/m)
Raphael (Finite-Difference Solver)	$\begin{bmatrix} 139.5 & -23.46 & -1.89 \\ -23.69 & 94.60 & -19.89 \\ -1.82 & -19.52 & 85.48 \end{bmatrix}$ (pF/m)
Reference[a]	$\begin{bmatrix} 142.1 & -21.76 & -0.89 \\ -21.73 & 93.53 & -18.10 \\ -0.89 & -18.10 & 87.96 \end{bmatrix}$ (pF/m)

a. W. Delbare and D. D. Zutter, “Space-domain Green’s function approach to the capacitance calculation of multi-conductor lines in multi-layered dielectrics with improved surface charge modeling,” *IEEE Trans. Microwave Theory and Tech.*, vol. 37, pp. 1562-1568, October 1989.

Figure 6-16 shows the results of convergence analysis, based on the total capacitance of the first conductor, with respect to the `GRIDFACTOR` parameter.

Figure 6-16: -Convergence of Accuracy Modes



Example 3: Two Traces Between Two Ground Planes

The following example is a coupled strip line, shown in Figure 6-17. Table 6-8 lists the complete input netlist. Table 6-9 shows the comparison between the computed result and the Finite Element (FEM) solver result.

Figure 6-17: Two Traces Between Two Ground Planes

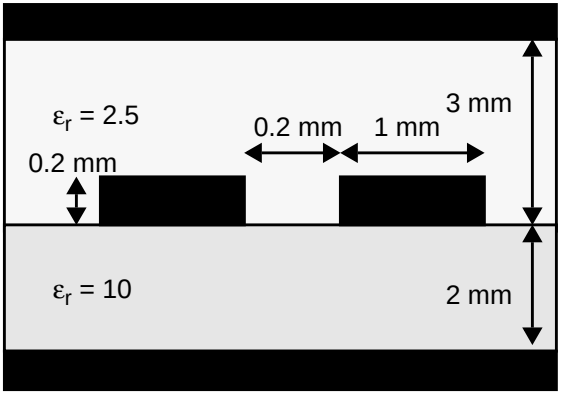


Table 6-8: Input File Listing for Example 3

Header, options and sources	`*Example 3: two traces between gnd planes`
	`.OPTION PROBE POST`
	`+ IMPULSE in1 gnd PULSE 4.82v 0v 5n 0.5n`
	`0.5n`
	`+ 25n`

W Element	`W1 in1 in2 gnd out1 out2 gnd`
	`FSmodel=cond2_sys`
	`+N=2 l=0.5`

Materials	`.MATERIAL diel_1 DIELECTRIC ER=10.0` `.MATERIAL diel_2 DIELECTRIC ER=2.5`
Shapes	`.SHAPE rect RECTANGLE WIDTH=1mm,` `+ HEIGHT=0.2mm,`

Top and bottom ground planes	`.LAYERSTACK stack_1,`
	`+ LAYER=(PEC,1mm), LAYER=(diel_1,2mm),`
	`+ LAYER=(diel_2,3mm), LAYER=(PEC,1mm)`

Option settings	`.FSOPTIONS opt1 PRINTDATA=YES`

Two conductors share the same shape	`.MODEL cond2_sys W MODELTYPE=FieldSolver,`
	`+ LAYERSTACK=stack1, FSOPTIONS=opt1`
	`+ RLGCFILE=ex3.rlgc`
	`+ CONDUCTOR=(SHAPE=rect, ORIGIN=`
	`+ (0,3mm)),`
	`+ CONDUCTOR=(SHAPE=rect,`
	`+ ORIGIN=(1.2mm,3mm))`

Analysis, outputs and end	`.TRAN 0.5n 100n`
	`.PROBE v(out1)`
	`.END`

Table 6-9: Comparison Result for Example 3

Computed	$\begin{bmatrix} 214.1 & -105.2 \\ -105.2 & 214.1 \end{bmatrix}$ (pF/m)
FEM Solver	$\begin{bmatrix} 217.7 & -108.2 \\ -108.2 & 217.7 \end{bmatrix}$ (pF/m)

Example 4: Using Field Solver with Monte Carlo Analysis

The following example shows how to use Monte Carlo transient analysis to model variations in the manufacturing of a microstrip. Table 6-10 shows the input listing with the *W* Element. Figure 6-18 shows the transient output waveforms.

Note: In Version 2001.4, only Star-Hspice supports Example 4. You cannot use this example with Star-Hspice XT, Star-Sim, or Star-Sim XT

Figure 6-18: Monte Carlo Analysis with a Field Solver and W Element

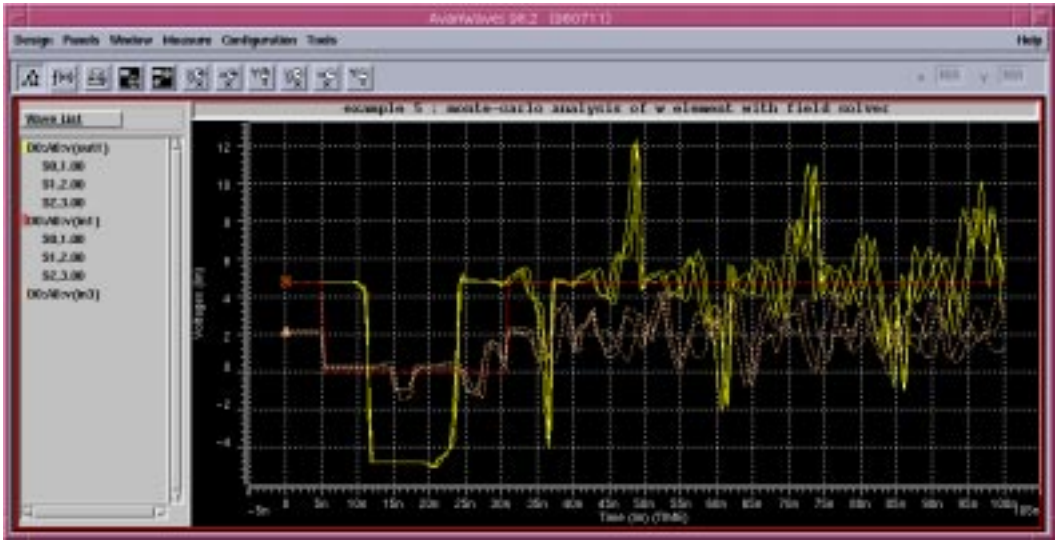


Table 6-10: Input File Listing for Example 4

Header, options and sources	`*PETL Example 4: example 2 with Monte-Carlo`
	`.OPTION PROBE POST`
	`+ VIMPULSE in1 gnd AC=1v PULSE 4.82v 0v 5ns`
	`+ 0.5ns 0.5ns 25ns`

Parameter definitions	`.PARAM x1=Gauss(0,0.02,1)`
	`+ x2=Gauss(0.5mm,0.02,1) x3=Gauss(1mm,0.02,1)`
	`.PARAM dRef=1u dY1=Gauss(2mm,0.02,1)`
	`+ dY2=Gauss(1mm,0.02,1)`

W Element	`W1 in1 in2 in3 0 out1 out2 out3 0` `+ FSMODEL=cond3_sys N=3 l=0.5`
Materials	`.MATERIAL diel_1 DIELECTRIC ER=4.3` `.MATERIAL diel_2 DIELECTRIC ER=3.2`
Shapes	`.SHAPE r1 RECTANGLE WIDTH=0.35mm,` `+ HEIGHT=0.070mm`

Uses the default AIR background	`.LAYERSTACK stack_1`
	`+ LAYER= (PEC,dRef),LAYER=(diel_1,dY1),`
	`+ LAYER= (diel_2,dY2)`

Three conductors share the same shape	`.MODEL cond3_sys W MODELTYPE=FieldSolver,`
	`+ LAYERSTACK=stack1,`
	`+ CONDUCTOR=(SHAPE=r1,ORIGIN=`
	`+ (x1,'dRef+dY1')),`
	`+ CONDUCTOR=(SHAPE=r1,ORIGIN=`
	`+ (x2,'dRef+dY1+dY2')),`
	`+ CONDUCTOR=(SHAPE=r1,ORIGIN=`
	`+ (x3,'dRef+dY1+dY2'))`

Analysis, outputs and end	`.PROBE TRAN v(in1) v(out1) v(in3)`
	`.PROBE AC v(out1) v(out3)`
	`.PROBE DC v(in1) v(out1) v(out3)`
	`.AC LIN 200 0Hz 0.3GHz`
	`.DC v1 0v 5v 0.01v`
	`.TRAN 0.5ns 100ns SWEEP MONTE=3`
	`.END`

Frequency Table Model

The Frequency Table Model is a generic model that you can use to describe frequency-varying behavior. Currently, the *S* element and `.sp` use this model.

Syntax

The syntax of the `.MODEL` model card is:

```
.MODEL name sp [N=val FSTART=val FSTOP=val NI=val
   SPACING=val MATRIX=val VALTYPE=val    INFINITY=matrixval
INTERPOLATION=val
   EXTRAPOLATION=val] [DATA=(npts ...)]
   [DATAFILE=filename]
```

Note: Interpolation and extrapolation occur *after* the simulator internally converts the **Z** and **S** parameter data to the **Y** parameter.

Parameter	Specifies
`name`	Model name.
`N`	Matrix dimension (number of signal terminals). The default value is `1`. If you use a value other than the default, then you must specify that value *before* you set `INFINITY` and `DATA`.
`FSTART`	Starting frequency point for data. Default=0.
`FSTOP`	Final frequency point for data (use this parameter only for the `LINEAR` and `LOG` spacing formats).

Parameter	Specifies	
NI	Number of frequency points per interval. Use this parameter only for the DEC and OCT spacing formats. Default=10.	
npts	Number of data points.	
SPACING	Data sample spacing format:	
	LIN (LINEAR):	uniform spacing, with the frequency step of (FSTOP-FSTART)/(npts-1). This is the default.
	OCT:	octave variation, with FSTART as the starting frequency, and NI points per octave. npts determines the final frequency.
	DEC:	decade variation, with FSTART as the starting frequency, and NI points per decade. npts determines the final frequency.
	LOG:	logarithmic spacing, with FSTART and FSTOP as the starting and final frequencies.
	POI: (NONUNIFORM)	non-uniform spacing. Pairs data points with frequency points.

Parameter	Specifies	
MATRIX	Matrix (data point) format:	
	SYMMETRIC:	symmetric matrix. Specifies only the lower-half triangle portion of a matrix. This is the default.
	HERMITIAN:	similar to SYMMETRIC, but off-diagonal terms are complex-conjugates of each other.
	NONSYMMETRIC:	non-symmetric matrix. Specifies a full matrix.
VALTYPE	Data type of matrix elements:	
	REAL:	real entry.
	CARTESIAN:	complex number in real/imaginary format. This is the default.
	POLAR:	complex number in polar format. Specify angles in radian.
INFINITY	Data point at infinity. Typically real-valued. This data format must be consistent with MATRIX and VALTYPE specifications. npts does not count this point.	
DC	Data port at DC. Typically real-valued. This data format must be consistent with MATRIX and VALTYPE specifications. npts does not count this point. You must specify either the DC point or the data point at frequency=0.	
INTERPOLATION	Interpolation scheme:	
	STEP:	piecewise step. This is the default.
	LINEAR:	piecewise linear.
	SPLINE:	b-spline curve fit.

Parameter	Specifies
EXTRAPOLATION	Extrapolation scheme during simulation: NONE: no extrapolation is allowed. Simulation terminates if a required data point is outside of the specified range. STEP: uses the last boundary point. This is the default. LINEAR: linear extrapolation, using the last two boundary points. If you specify the data point at infinity, then simulation does not extrapolate, and uses the infinity value.

DATA	Data points.
	■ Syntax for LIN spacing:
	`.MODEL name sp SPACING=LIN [N=dim]`
	`+ FSTART=f0 DF=f1 DATA=npts d1 d2 ...`
	■ Syntax for OCT or DEC spacing:
	`.MODEL name sp SPACING=DEC or OCT`
	`+ [N=dim] FSTART=f0`
	`+ NI=n_per_intval DATA=npts d1`
	`+ d2 ...`
	■ Syntax for POI spacing:
	`.MODEL name sp SPACING=NONUNIFORM`
	`+ [N=dim] DATA=npts f1 d1 f2 d2`
	`+ ...`

DATAFILE	Data points, using an external file. The content of this file must be *only* raw numbers, without any suffixes, comments, or continuation letters. The order of data must be the same as in the DATA statement. This data file has no limitation on line length, so you can enter a large number of data points.

Frequency Table Model Examples

Example 1

```
.MODEL fmod SP N=2 FSTOP=30MegHz
+ DATA = 2
*
* matrix at f=0
*
+  0.02      0.0
* Re(Y11) Im(Y11)
+ -0.02     0.0              0.02    0.0
* Im(Y21) Im(Y21) (= Y21)   Re(Y22) Im(Y22)
*
* matrix at f=30MHz
*
+ 0.02     0.0
* Re(Y11) Im(Y11)
+ -0.02    0.0              0.02    0.0
* Im(Y21) Im(Y21) (= Y21) Re(Y22) Im(Y22)
```

Example 2

```
.MODEL fmod SP N=2 FSTOP=30MegHz MATRIX=NONSYMMETRIC
+ DATA = 2
*
* matrix at f=0
*
+ 0.02     0.0     -0.02   0.0
* Re(Y11) Im(Y11) Re(Y12) Im(Y12)
+ -0.02    0.0     0.02    0.0
* Im(Y21) Im(Y21) Re(Y22) Im(Y22)
*
* matrix at f=30MHz
*
+ 0.02     0.0     -0.02   0.0
* Re(Y11) Im(Y11) Re(Y12) Im(Y12)
+ -0.02    0.0     0.02    0.0
* Im(Y21) Im(Y21) Re(Y22) Im(Y22)
```

Example 3

```
.MODEL fmod SP N=2 SPACING=POI
+ DATA = 1
+ 0.0 * first frequency point
*
* matrix at f=0
*
+ 0.02      0.0
* Re(Y11) Im(Y11)
+ -0.02     0.0              0.02    0.0
* Im(Y21) Im(Y21) (= Y21)   Re(Y22) Im(Y22)
*
+ 30e+6 * second frequency point
*
* matrix at f=30MHz
*
+ 0.02      0.0
* Re(Y11) Im(Y11)
+ -0.02     0.0              0.02    0.0
* Im(Y21) Im(Y21) (= Y21)   Re(Y22) Im(Y22)
```

Example 4

```
.MODEL fmod SP N=2 FSTOP=30MegHz VALTYPE=REAL
+ DATA = 2
*
* matrix at f=0
*
+ 0.02 -0.02
* Y11    Y12
+  -0.02 0.02
* Y21    Y22
*
* matrix at f=30MHz
*
+ 0.02 -0.02
* Y11    Y12
+ -0.02 0.02
* Y21    Y22
```

Avant!

Chapter 7
Using IBIS Models

The Input/Output Buffer Information Specification (IBIS) is being developed by the IBIS Open Forum, which is affiliated with the Electronic Industries Alliance (EIA). IBIS specifies a standard form for presentation of information in ASCII format in special files. This information describes behavior of various I/O buffers that send electrical signals outside the silicon chip or receive such signals. The type of information includes output I-V curves for output buffers in LOW and HIGH states, V(t) curves describing the exact form of transitions from LOW to HIGH states and from HIGH to LOW states for a given load, values for die capacitance, electrical parameters of the packages, and so on. The IBIS standard specifies only the "form" of information, and does not specify how the information should be processed or used by the simulator.

However, the IBIS standard contains a section devoted to recommendations on how information should be derived through the simulation or from the silicon measurement. In addition, the IBIS Open Forum has sponsored development of a parser for IBIS files—called the golden parser. The golden parser is freely available as an executable and should be used for verification of IBIS files. The golden parser is incorporated into Avant! in-circuit simulators. When the golden parser processes an IBIS file, it produces warnings and/or error messages which by default appear in the Hspice output.

The I/O buffer element type is called *buffer*. The name of this element starts with the letter *b*. Using buffers is similar to using other simulation elements, such as transistors: give a name to the buffer, specify a list of nodes that are used to connect the buffer to the rest of the circuit, and specify parameters. Only parameters that specify a model for the buffer (file name and model name) are required.

Two significant differences from the use of other elements are:

1. The number of external nodes is variable depending on the buffer type and can be from 4 to 8; and
2. Nodes that are suppose to connect to power/ground rails must not be connected in the netlist, because simulation does this connection by default.

This chapter is not intended to introduce the IBIS standard, because it is a large document; familiarity with the standard is assumed. A significant amount of information is available on the Internet, and appropriate links to other sites are listed in "References" on page 7-56.

Three types of analysis are supported for input/output buffers:

- DC analysis
- Transient analysis
- AC analysis

This chapter covers the following topics:

IBIS Conventions

The general syntax of an element card for I/O buffers is:

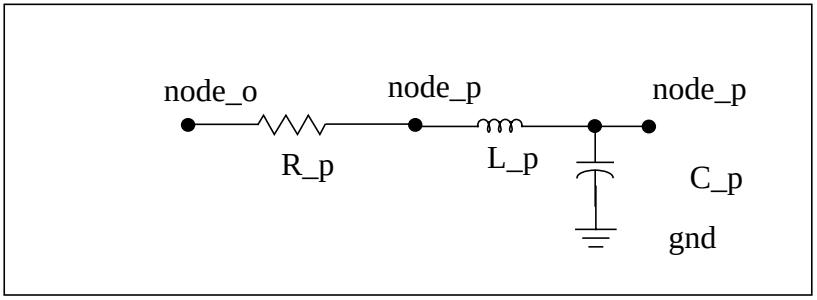
General Form:

```
bname node_1 node_2 ... node_N
+ keyword_1=value_1 ... [keyword_M=value_M]
```

where:

bname	Buffer element name. Must begin with B, which can be followed by up to 1023 alphanumeric characters.
node_1 node_2 ... node_N	List of I/O buffer external nodes. The number of nodes and corresponding rules are specific to different buffer types (see later sections in this chapter).
keyword_i=value_i	Assigns value, *value_i*, to the keyword, *keyword_i*. Optional keywords are given in square brackets (see *"Specifying Common Keywords" on page 7-27* for more information).

Figure 7-1: Circuit Diagram for Package



The *gnd* node on the circuit diagram for buffers denotes the ideal SPICE ground node (the notation *node 0* [zero] is also used). This node is always available in the simulation device models. Do not include this node in the node list on the buffer card. If the *gnd* node appears on a circuit diagram, simulation makes the node connection to the ideal ground. Node *gnd* is used on circuit diagrams to explain the connection of individual parts inside buffers.

In some cases, buffer nodes have different rules than nodes for other elements. Some nodes may already be connected to voltage sources (simulation makes such connections) so it is incorrect to connect a voltage source to such nodes. Conversely, some nodes should be connected to voltage sources and it is incorrect not to connect voltage sources to these nodes.

Note: See "Specifying Common Keywords" on page 7-27, and the sections about individual buffer types, for detailed explanations of how to use these nodes.

Buffers correspond to models in IBIS files and do not include packages. At this time, corresponding packages should be added manually. For example, if *node_out* and *node_pin* are nodes for output of the output buffer and corresponding pin, then add the following lines to the netlist:

```
R_pkg node_out node_pkg R_pkg_value
L_pkg node_pkg node_pin L_pkg_value
C_pkg node_pin gnd  C_pkgvalue
```

where values for *R_pkg*, *L_pkg*, and *C_pkg* are taken from the IBIS file (see Figure 7-1 on page 7-3 for the circuit diagram).

Terminology

The following are definitions of terms used frequently in this chapter:

card, buffer card	Used to denote a line(s) from the netlist that specifies the buffer name (should begin with the letter b), a list of external nodes, required keyword, and optional keywords.
buffer, I/O buffer, input/output buffer	One of 14 IBIS models as specified in the standard, version 3.2, and implemented in the Avant! simulation device models.
RWF, FWF	Rising waveform, falling waveform
I/O	Input/Output
I/V curve	Current-voltage curve
PU, PD	Pullup, pulldown
PC, GC	Power clamp, ground clamp

Limitations and Restrictions

The series, series switch, and terminator buffers are not implemented.

You can simulate the terminator by using other existing elements: resistors, capacitors, and voltage dependent current sources.

Buffers

This section describes the buffers as implemented in Avant! simulation device models. Please refer to "Specifying Common Keywords" on page 7-27 for details on using keywords shown in the syntax examples in the following sections.

Input Buffer

The syntax of an input buffer element card is:

```
B_INPUT nd_pc nd_gc nd_in nd_out_of_in
+ file='filename' model='model_name'
+ [typ={typ|min|max|fast|slow}] [power={on|off}]
+ [buffer={1|input}]
+ [interpol={1|2}]
+ [nowarn]
+ [c_com_pc=c_com_pc_value]
+ [c_com_gc=c_com_gc_value]
+ [pc_scal=pc_scal_value]
+ [gc_scal=gc_scal_value]
```

where the total number of external nodes is equal to 4.

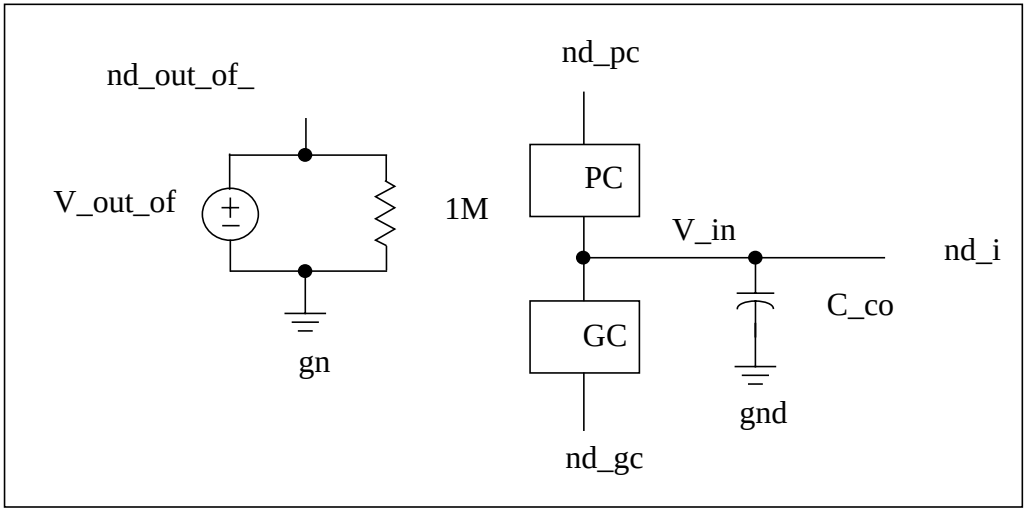
If keyword *power=on* (default) is specified, nodes *nd_pc* and *nd_gc* are connected to voltage sources with values taken from the IBIS file. You should not connect these nodes to voltage sources. However, names for these nodes should be provided, so you can print out the voltage values if required. For example:

```
.PRINT V(nd_pc) V(nd_gc)
```

If you specify the *power=off* keyword, simulation does not connect these nodes to voltage sources. You should connect the nodes to voltage sources either directly or through an RLC network, or a transmission line.

There are no special rules for *node_in* and *node_in* can connect to I, E, F, G, and H elements. The buffer measures and processes the voltage on this node and sends a response to node *nd_out_of_in*. The node *nd_out_of_in* is connected to the voltage source as shown in Figure 7-2. It is an error to connect this node to a voltage source. If *power=off*, nodes *nd_pc*, *nd_gc* can be connected to the ground is the intention is to specify voltage zero on these nodes.

Figure 7-2: Input Buffer



V_out_of_in is a digital signal that assumes values of either 0 or 1 depending on the voltages *V_in*, *Vinh*, *Vinl*, and *Polarity*. Simulation processes *V_out_of_in* according to the following rules.

If:	
Polarity=Non-Inverting	Initially *V_out_of_in* is set to 0 if V_in < (Vinh+Vinl)/2 and to 1 in the opposite case.
and if V_out_of_in=1	then it goes to 0 only if V_in < Vinl
and if V_out_of_in=0	then it goes to 1 only if V_in>Vinh
Polarity=Inverting	Initially *V_out_of_in* is set to 0 if V_in > (Vinh+Vinl)/2 and to 1 in the opposite case
and if V_out_of_in=1	then it goes to 0 only if V_in > Vinh
and if V_out_of_in=0	then it goes to 1 only if V_in <Vinl

Figure 7-2 on page 7-7 shows a single circuit specified on a single element card. *V_out_of_in* is a voltage source whose value is a function of *V_in* (as well as of thresholds Vinl, Vinh, and parameter Polarity). It can be used to drive other circuits.

If pc_scal or gc_scal arguments exist and pc_scal_value or gc_scal_value do not equal 1.0, then PC or GC iv curve will be adjusted using the pc_scal_value or gc_scal_value.

Output Buffer

The syntax for an output buffer element card is:

```
B_OUTPUT nd_pu nd_pd nd_out nd_in [nd_pc nd_gc]
+ file='file_name' model='model_name'
+ [typ={typ|min|max|fast|slow}] [power={on|off}]
+ [buffer={2|output}]
+ [xv_pu=state_pu] [xv_pd=state_pd]
+ [interpol={1|2}]
+ [ramp_fwf={0|1|2}] [ramp_rwf={0|1|2}]
+ [fwf_tune=fwf_tune_value] [rwf_tune=rwf_tune_value]
+ [nowarn]
+ [c_com_pu=c_com_pu_value]
+ [c_com_pd=c_com_pd_value]
```

```
+ [c_com_pc=c_com_pc_value]
+ [c_com_gc=c_com_gc_value]
+ [pu_scal=pu_scal_value]
+ [pd_scal=pd_scal_value]
+ [pc_scal=pc_scal_value]
+ [gc_scal=gc_scal_value]
+ [rwf_scal=rwf_scal_value]
+ [fwf_scal=fwf_scal_value]
+ [spu_scal=spu_scal_value]
+ [spd_scal=spd_scal_value]
```

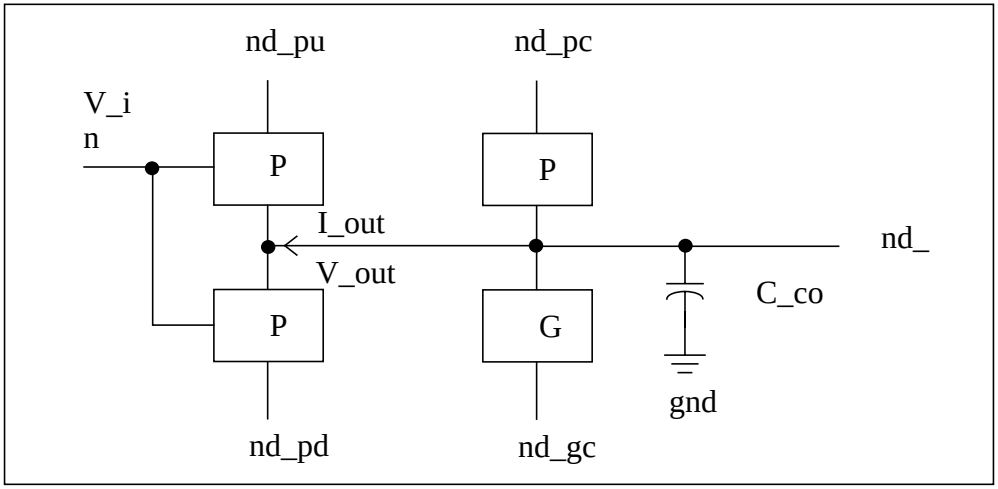
The *nd_pc* and *nd_gc* nodes are optional. However, either both or none can be specified. The total number of external nodes is either 4 or 6, any other number is an error. If you do not specify the *nd_pc* and *nd_gc* nodes on the element card, but Power_Clamp and/or Ground_Clamp I-V curves are present in the model in question, then the simulator simply connects Power_Clamp and/or Ground_Clamp to the corresponding nd_pu (pullup) and/or nd_pd (pulldown).

However, the optional nodes *nd_pc* and *nd_gc* are needed if:

- IBIS keywords *POWER Clamp Reference* and *GND Clamp Reference* are present in the IBIS model and have different values than the IBIS keywords *Pullup Reference* and *Pulldown Reference*, or
- IBIS keywords *Pullup Reference* and *Pulldown Reference* do not exist and *POWER Clamp Reference* and *GND Clamp Reference* have different values than those determined by the *Voltage Range* IBIS keyword.

If optional nodes *nd_pc* and *nd_gc* are needed, but omitted from the element card, simulation issues a warning and connects *nd_pc* to *nd_pu* and *nd_gc* to *nd_pd*.

Figure 7-3: Output Buffer



If keyword *power=on* (default) is specified, nodes *nd_pu*, *nd_pd*, and if specified, *nd_pc* and *nd_gc*, are connected to voltage sources with values taken from the IBIS file. You should not connect these nodes to voltage sources. However, names for these nodes should be provided, so you can print out the voltage values if required. For example:

```
.PRINT V(nd_pu) V(nd_pd)
```

If you specify the *power=off* keyword, simulation does not connect these nodes to voltage sources. You should connect the nodes to voltage sources either directly or through an RLC network or a transmission line.

There are no special rules for node *nd_out*. The voltage on this node is controlled by the digital signal on the node *nd_in*. Now any voltage source, current source, voltage controlled voltage source, voltage controlled current source, current controlled voltage source, or current controlled current source can be connected to the nd_in as shown in the following example:

```
V_in nd_in gnd 0V pulse( 0V 1V 1n 0.1n 0.1n 7.5n 15n )]
```

If *power=off*, nodes *nd_pu*, *nd_pd*, *nd_pc*, *nd_gc* can be connected to the ground if the intention is to have zero voltage on these nodes.

V_in is a controlling signal representing a digital signal with values 0 and 1. However, simulation can use any signal and process, according to the following rules:

If:

Polarity=Non-Inverting	At t=0 for transient analysis (or for DC analysis), the buffer goes to HIGH state if V_in > 0.5 and to LOW in the opposite case. Next, if the buffer is in HIGH state, it will go to LOW state if V_in < 0.2. If the buffer is in LOW state, it will go to HIGH state if V_in > 0.8.
Polarity=Inverting	At t=0 for transient analysis (or for DC analysis), the buffer goes to HIGH state if V_in < 0.5 and to LOW in the opposite case. Next, if the buffer is in HIGH state, it will go to LOW state if V_in > 0.8. If the buffer is in LOW state, it will go to HIGH state if V_in < 0.2.

If pc_scal (or gc_scal, pu_scal, pd_scal) argument exists and pc_scal_value (or gc_scal_value, pu_scal_value, pd_scal_value) does not equal to 1.0, the PC (or GC, PU, PD) iv curve will be adjusted using the pc_scal_value (or gc_scal_value, pu_scal_value, pd_scal_value).

If rwf_scal (or fwf_scal) argument exists and rwf_scal_value (or fwf_scal_value) does not equal to 1.0, rising and falling vt curves will be adjusted using rwf_scal_value (or fwf_scal_value).

If spu_scal (or spd_scal) argument exists and spu_scal_value (or spd_scal_value) does not equal to 0.0, but at the same time power is equal to off and (spu_scal_value-spd_scal_value) does not equal to the corresponding value in the .ibs file, then the iv curves of PU (or PD) will be adjusted using spu_scal_value (or spd_scal_value).

Tristate Buffer

The syntax for a tristate buffer element card is:

```
B_3STATE nd_pu nd_pd nd_out nd_in nd_en [nd_pc nd_gc]
+ file='file_name' model='model_name'
+ [typ={typ|min|max|fast|slow}] [power={on|off}]
+ [buffer={4|three_state}]
+ [xv_pu=state_pu] [xv_pd=state_pd]
+ [interpol={1|2}]
+ [ramp_fwf={0|1|2}] [ramp_rwf={0|1|2}]
+ [fwf_tune=fwf_tune_value] [rwf_tune=rwf_tune_value]
+ [nowarn]
+ [c_com_pu=c_com_pu_value]
+ [c_com_pd=c_com_pd_value]
+ [c_com_pc=c_com_pc_value]
+ [c_com_gc=c_com_gc_value]
+ [pu_scal=pu_scal_value]
+ [pd_scal=pd_scal_value]
+ [pc_scal=pc_scal_value]
+ [gc_scal=gc_scal_value]
+ [rwf_scal=rwf_scal_value]
+ [fwf_scal=fwf_scal_value]
+ [spu_scal=spu_scal_value]
+ [spd_scal=spd_scal_value]
```

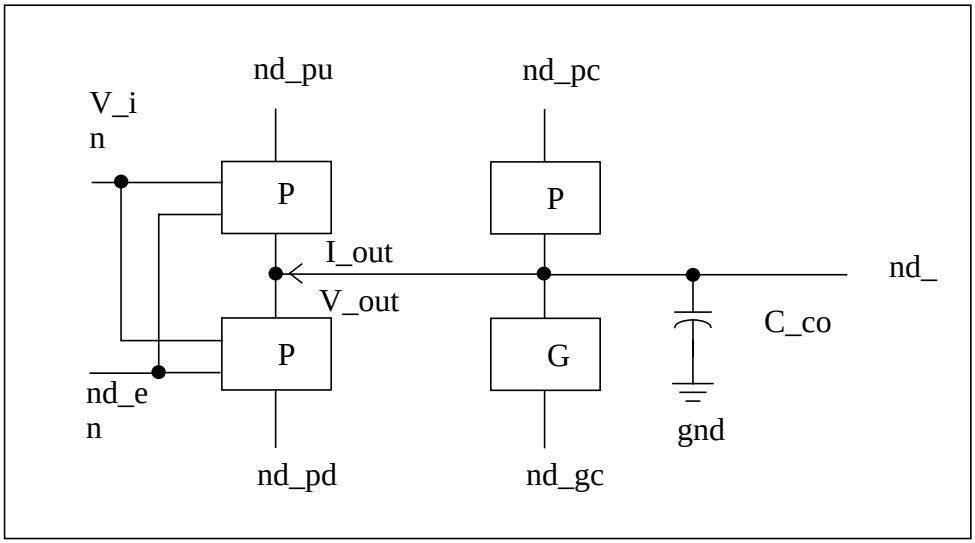
The *nd_pc* and *nd_gc* nodes are optional. However, either both or none can be specified. The total number of external nodes is either 5 or 7; any other number is an error. If nodes *nd_pc* and *nd_gc* are not given on the element card but Power_Clamp and/or Ground_Clamp I-V curves are present in the model in question, then the simulator will simply add Power_Clamp and/or Ground_Clamp I-V curves data to corresponding Pull_Up and/or Pull_Down I-V curves data.

However, the optional nodes *nd_pc* and *nd_gc* are needed if:

- IBIS keywords *POWER Clamp Reference* and *GND Clamp Reference* are present in the IBIS model and have different values than the IBIS keywords *Pullup Reference* and *Pulldown Reference*, or
- IBIS keywords *Pullup Reference* and *Pulldown Reference* do not exist and *POWER Clamp Reference* and *GND Clamp Reference* have different values than those determined by the *Voltage Range* IBIS keyword.

If optional nodes *nd_pc* and *nd_gc* are needed, but omitted from the element card, simulation issues a warning and connects *nd_pc* to *nd_pu* and *nd_gc* to *nd_pd*.

Figure 7-4: Tristate Buffer



If you specify the *power=on* (default) keyword, then the *nd_pu*, *nd_pd* nodes, and if specified, *nd_pc* and *nd_gc*, are connected to voltage sources with values taken from the IBIS file. You should not connect these nodes to voltage sources.

However, names for these nodes should be provided in the netlist, so you can print out the voltage values if required. For example:

```
.PRINT V(nd_pu) V(nd_pd)
```

If you specify the *power=off* keyword, simulation does not connect these nodes to voltage sources. You should connect the nodes to voltage sources either directly or through an RLC network, or a transmission line.

There are no special rules for *nd_out*. The voltage on this node is controlled by the digital signal on the nodes *nd_in, nd_en*. Voltage sources must be connected to the nodes *nd_in, nd_en* as shown in the following example:

```
V_in nd_in gnd 0V pulse( 0V 1V 1n 0.1n 0.1n 7.5n 15n )
V_en nd_en gnd 0V pulse( 0V 1V 3n 0.1n 0.1n 7.5n 15n ) ].
```

The *nd_pu*, *nd_pd*, *nd_pc*, and *nd_gc nodes* can be connected to the ground if the intention is to have zero voltage on these nodes. Nodes *nd_in*, *nd_en* can not be connected to the ground.

V_in and *V_en* are controlling signals representing digital signals with values 0 and 1. Simulation can use any signal and process according to the following rules:

The enable signal, *V_en*, supersedes the input signal, *V_in.*
If:

ENABLE = Active-High	At t=0 for transient analysis (or for DC analysis), the buffer goes to the ENABLE state if V_en > 0.5 and to DISABLE in the opposite case.
ENABLE = Active-Low	At t=0 for transient analysis (or for DC analysis), the buffer goes to ENABLE state if V_en < 0.5 and to DISABLE in the opposite case.
The buffer is in ENABLE state	Begins transition to DISABLE state if V_en < 0.2 (where Enable = Active-High) and if V_en > 0.8 (where Enable = Active-Low).
The buffer is in DISABLE state or in the process of transition from ENABLE state to DISABLE state	Begins transition to ENABLE state if V_en > 0.8 (where Enable = Active-High) and if V_en < 0.2 (where Enable = Active-Low).
The buffer is in ENABLE state	Response to the input signal, *V_in*, is the same as the output buffer.
Polarity=Non-Inverting	At t=0 for transient analysis (or for DC analysis), the buffer goes to HIGH state if V_in > 0.5 and to LOW in the opposite case. Next, if the buffer is in HIGH state, it will go to LOW state if V_in < 0.2. If the buffer is in LOW state, it will go to HIGH state if V_in > 0.8.
Polarity=Inverting	At t=0 for transient analysis (or for DC analysis), the buffer goes to HIGH state if V_in < 0.5 and to LOW in the opposite case. Next, if the buffer is in HIGH state, it will go to LOW state if V_in > 0.8. If the buffer is in LOW state, it will go to HIGH state if V_in < 0.2.

Note: After the buffer begins a transition from ENABLE state to DISABLE state, all memory about previous HIGH/LOW states is lost. If the buffer later goes to the ENABLE state, it compares the controlling signal, V_in, against the threshold 0.5 to decide whether to go to HIGH state or LOW state similar to the time moment t=0, rather than against the thresholds 0.2 and 0.8.

Input/Output Buffer

The syntax of an input/output buffer element card is:

```
B_IO nd_pu nd_pd nd_out nd_in nd_en V_out_of_in [nd_pc nd_gc]
+ file='file_name' model='model_name'
+ [typ={typ|min|max|fast|slow}] [power={on|off}]
+ [buffer={3|input_output}]
+ [xv_pu=state_pu] [xv_pd=state_pd]
+ [interpol={1|2}]
+ [ramp_fwf={0|1|2}] [ramp_rwf={0|1|2}]
+ [fwf_tune=fwf_tune_value] [rwf_tune=rwf_tune_value]
+ [nowarn]
+ [c_com_pu=c_com_pu_value]
+ [c_com_pd=c_com_pd_value]
+ [c_com_pc=c_com_pc_value]
+ [c_com_gc=c_com_gc_value]
+ [pu_scal=pu_scal_value]
+ [pd_scal=pd_scal_value]
+ [pc_scal=pc_scal_value]
+ [gc_scal=gc_scal_value]
+ [rwf_scal=rwf_scal_value]
+ [fwf_scal=fwf_scal_value]
+ [spu_scal=spu_scal_value]
+ [spd_scal=spd_scal_value]
```

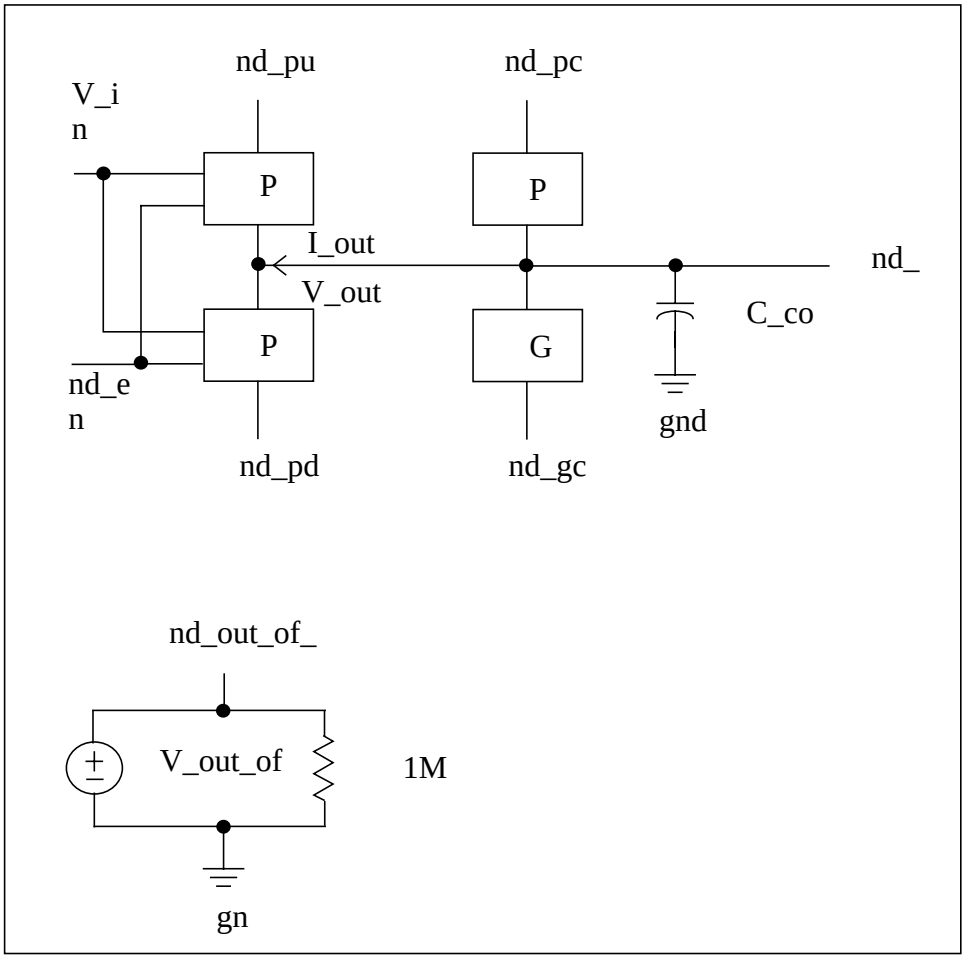
The *nd_pc* and *nd_gc* nodes are optional. However, either both or none can be specified. The total number of external nodes is either 6 or 8; any other number is an error. If nodes *nd_pc* and *nd_gc* are not given on the element card but Power_Clamp and/or Ground_Clamp I-V curves are present in the model in question, then the simulator will simply add Power_Clamp and/or Ground_Clamp I-V curves data to corresponding Pull_Up and/or Pull_Down I-V curves data.

However, the optional nodes *nd_pc* and *nd_gc* are needed if:

- IBIS keywords *POWER Clamp Reference* and *GND Clamp Reference* are present in the IBIS model and have different values than the IBIS keywords *Pullup Reference* and *Pulldown Reference*, or
- IBIS keywords *Pullup Reference* and *Pulldown Reference* do not exist and *POWER Clamp Reference* and *GND Clamp Reference* have different values than those determined by the *Voltage Range* IBIS keyword.

If you need the *nd_pc* and *nd_gc* optional nodes, but you omitted them from the element card, simulation issues a warning and connects *nd_pc* to *nd_pu* and *nd_gc* to *nd_pd*.

Figure 7-5: Input-Output Buffer



If you specify the *power=on* (default) keyword, then the *nd_pu* and *nd_pd* nodes, and if specified, *nd_pc* and *nd_gc*, are connected to voltage sources with values taken from the IBIS file. You should not connect these nodes to voltage sources. However, names for these nodes should be provided in the netlist, so you can print out the voltage values if required. For example:

```
.PRINT V(nd_pu) V(nd_pd)
```

If you specify the *power=off* keyword, simulation does not connect these nodes to voltage sources. You should connect the nodes to voltage sources either directly or through an RLC network or a transmission line.

There are no special rules for node *nd_out*. The voltage on this node is controlled by the digital signal on the nodes *nd_in*, *nd_en*. Voltage sources must be connected to the nodes *nd_in*, *nd_en* as shown in the following example:

```
V_in nd_in gnd 0V pulse (0V 1V 1n 0.1n 0.1n 7.5n 15n)
V_en nd_en gnd 0V pulse (0V 1V 3n 0.1n 0.1n 7.5n 15n).
```

The *nd_pu*, *nd_pd*, *nd_pc*, and *nd_gc nodes* can be connected to the ground if the intention is to have zero voltage on these nodes.

The *nd_out_of_in* node is connected to a voltage source (see Figure). It is an error to connect this node to a voltage source or the ground.

The input-output buffer is a combination of the tristate buffer and the input buffer. See “Input Buffer” on page 7-6 and “Tristate Buffer” on page 7-12 for more information.

The input-output buffer can function as an input buffer. In this case, the resultant digital signal *V_out_of_in* on the node *nd_out_of_in* is controlled by the voltage *V_out* on the node *nd_out.*

For the input buffer, this controlling voltage is called *V_in* and any corresponding node is *nd_in.*

The input-output buffer uses *V_in*, *nd_in* notations to denote the controlling voltage and controlling input node for the output part of the buffer.

If the input-output buffer is not in the DISABLE state (this includes ENABLE state and transitions to ENABLE->DISABLE and DISABLE->ENABLE), then it functions as a tristate buffer. If input-output buffer is in the DISABLE state, it functions as an input buffer.

However, there is a difference in the digital output of the input part of the buffer (voltage *V_out_of_in*). Because *V_out_of_in* is not always defined (e.g. the buffer is in ENABLE state, or Vinl < V_out < Vinh at the time moment, when the transition to DISABLE state is completed) and because we want to preserve logical LEVELs 0 and 1 for LOW and HIGH states, *V_out_of_in* takes the value 0.5 when it is undefined.

Figure 7-5 on page 7-18 shows a single circuit specified on a single element card. The *V_out_of_in* is a voltage source whose value is a function of *V_out* (as well as of thresholds Vinl, Vinh and parameter Polarity). It can be used to drive other circuits.

Open Drain, Open Sink, Open Source Buffers

Open drain and open sink buffers do not have pullup circuitry. Open source buffers do not have pulldown circuitry. However, the element cards for these three buffers coincide with the element card for the output buffer. Accordingly, you should always specify names for pullup and pulldown nodes, *nd_pu* and *nd_pd*, even if the buffer does not have pullup or pulldown circuitry.

All rules given in "Output Buffer" on page 7-8 apply to open drain, open sink, and open source buffers with the following exceptions:

- Because open drain and open sink buffers do not have pullup circuitry, the option *xv_pu=nd_state_pu* should not be specified.
- Similarly, because open source buffers do not have pulldown circuitry, the option *xv_pd=nd_state_pd* should not be specified.

I/O Open Drain, I/O Open Sink, I/O Open Source Buffers

I/O open drain and I/O open sink buffers do not have pullup circuitry. I/O open source buffers do not have pulldown circuitry. However, the element cards for these three buffers coincide with the element card for the input-output buffer. Accordingly, you should always specify names for pullup and pulldown nodes, *nd_pu* and *nd_pd*, even if the buffer does not have pullup or pulldown circuitry.

All rules given in "Input/Output Buffer" on page 7-16 are applicable to I/O open drain, I/O open sink, and I/O open source buffers with the following exceptions:

- Because I/O open drain and I/O open sink buffers do not have pullup circuitry, the option *xv_pu=nd_state_pu* should not be specified.
- Similarly, because I/O open source buffers do not have pulldown circuitry, the option *xv_pd=nd_state_pd* should not be specified.

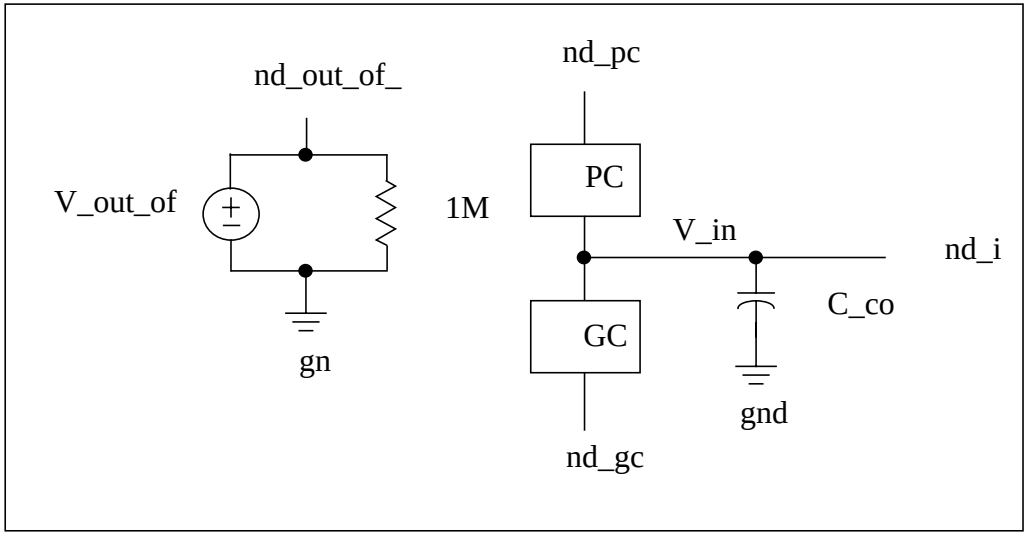
Input ECL Buffer

The syntax of the input ECL buffer element card is:

```
B_INPUT_ECL nd_pc nd_gc nd_in nd_out_of_in
+ file='file_name' model='model_name'
+ [typ={typ|min|max|fast|slow}] [power={on|off}]
+ [buffer={11|input_ecl}]
+ [interpol={1|2}]
+ [nowarn]
+ [c_com_pc=c_com_pc_value]
+ [c_com_gc=c_com_gc_value]
+ [pc_scal=pc_scal_value]
+ [gc_scal=gc_scal_value]
```

The input ECL buffer is similar to the input buffer. The only difference is in default values for *Vinl* and *Vinh*.

Figure 7-6: Input ECL Buffer



Output ECL Buffer

The syntax of the output ECL buffer element card is:

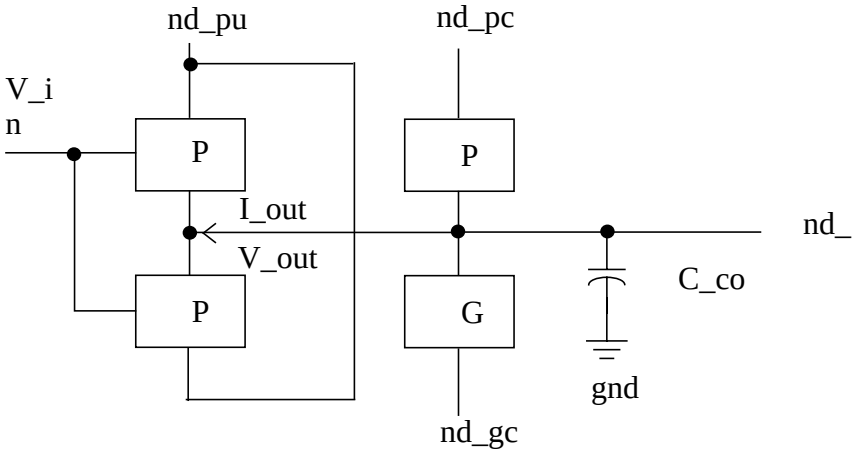
```
B_OUTPUT_ECL nd_pu nd_out nd_in [nd_pc nd_gc]
+ file='file_name' model='model_name'
+ [typ={typ|min|max|fast|slow}] [power={on|off}]
+ [buffer={12|output_ecl}]
+ [xv_pu=state_pu] [xv_pd=state_pd]
+ [interpol={1|2}]
+ [ramp_fwf={0|1|2}] [ramp_rwf={0|1|2}]
+ [fwf_tune=fwf_tune_value] [rwf_tune=rwf_tune_value]
+ [nowarn]
+ [c_com_pu=c_com_pu_value]
+ [c_com_pc=c_com_pc_value]
+ [c_com_gc=c_com_gc_value]
+ [pu_scal=pu_scal_value]
+ [pd_scal=pd_scal_value]
+ [pc_scal=pc_scal_value]
+ [gc_scal=gc_scal_value]
+ [rwf_scal=rwf_scal_value]
+ [fwf_scal=fwf_scal_value]
+ [spu_scal=spu_scal_value]
+ [spd_scal=spd_scal_value]
```

Nodes *nd_pc* and *nd_gc* are optional. However, either both or none can be specified. The total number of external nodes is either 3 or 5, any other number is an error. The output ECL buffer does not have a pulldown node. The pulldown table in the IBIS file is referenced in respect to pullup voltage.

If nodes *nd_pc* and *nd_gc* are not given on the element card but Power_Clamp and/or Ground_Clamp I-V curves are present in the model in question, then the simulator will issue an error message (this simulator behavior is different from that for the output buffer).

In other respects, the output ECL buffer is similar to the output buffer. For more information, see “Output Buffer” on page 7-8.

Figure 7-7: Output ECL Buffer



Tristate ECL Buffer

The syntax for the tristate ECL buffer element card is:

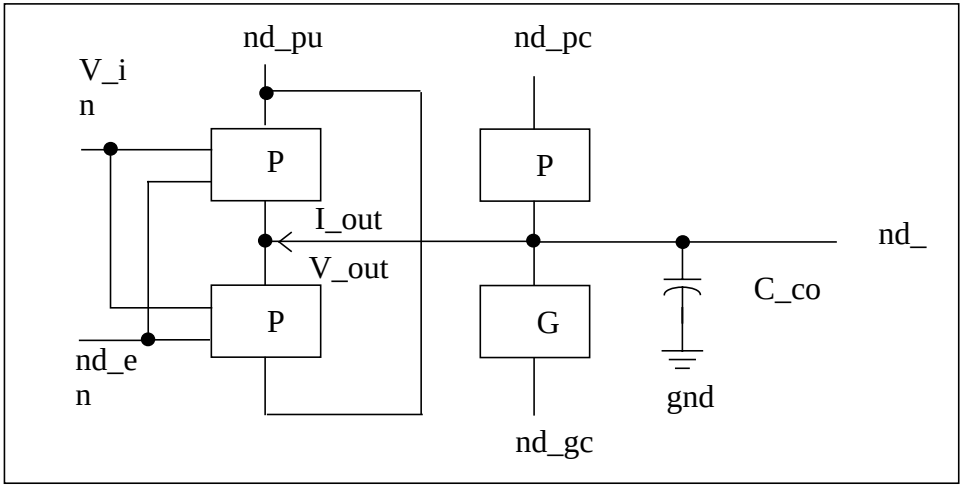
```
B_3STATE_ECL nd_pu nd_out nd_in nd_en [nd_pc nd_gc]
+ file='file_name' model='model_name'
+ [typ={typ|min|max|fast|slow}] [power={on|off}]
+ [buffer={14|three_state_ecl}]
+ [xv_pu=state_pu] [xv_pd=state_pd]
+ [interpol={1|2}]
+ [ramp_fwf={0|1|2}] [ramp_rwf={0|1|2}]
+ [fwf_tune=fwf_tune_value] [rwf_tune=rwf_tune_value]
+ [nowarn]
+ [c_com_pu=c_com_pu_value]
+ [c_com_pc=c_com_pc_value]
+ [c_com_gc=c_com_gc_value]
+ [pu_scal=pu_scal_value]
+ [pd_scal=pd_scal_value]
+ [pc_scal=pc_scal_value]
+ [gc_scal=gc_scal_value]
+ [rwf_scal=rwf_scal_value]
+ [fwf_scal=fwf_scal_value]
+ [spu_scal=spu_scal_value]
+ [spd_scal=spd_scal_value]
```

The *nd_pc* and *nd_gc* nodes are optional. However, either both or none can be specified. The total number of external nodes is either 4 or 6, any other number is an error. The tristate ECL buffer does not have a pulldown node. The pulldown table in the IBIS file is referenced in respect to pullup voltage.

If nodes *nd_pc* and *nd_gc* are not given on the element card but Power_Clamp and/or Ground_Clamp I-V curves are present in the model in question, then the simulator will issue an error message (this simulator behavior is different from that for the tristate buffer).

In other respects, the tristate ECL buffer is similar to the tristate buffer. See "Tristate Buffer" on page 7-12 for more information.

Figure 7-8: Tristate ECL Buffer



Input-Output ECL Buffer

The syntax for the input-output ECL buffer element card is:

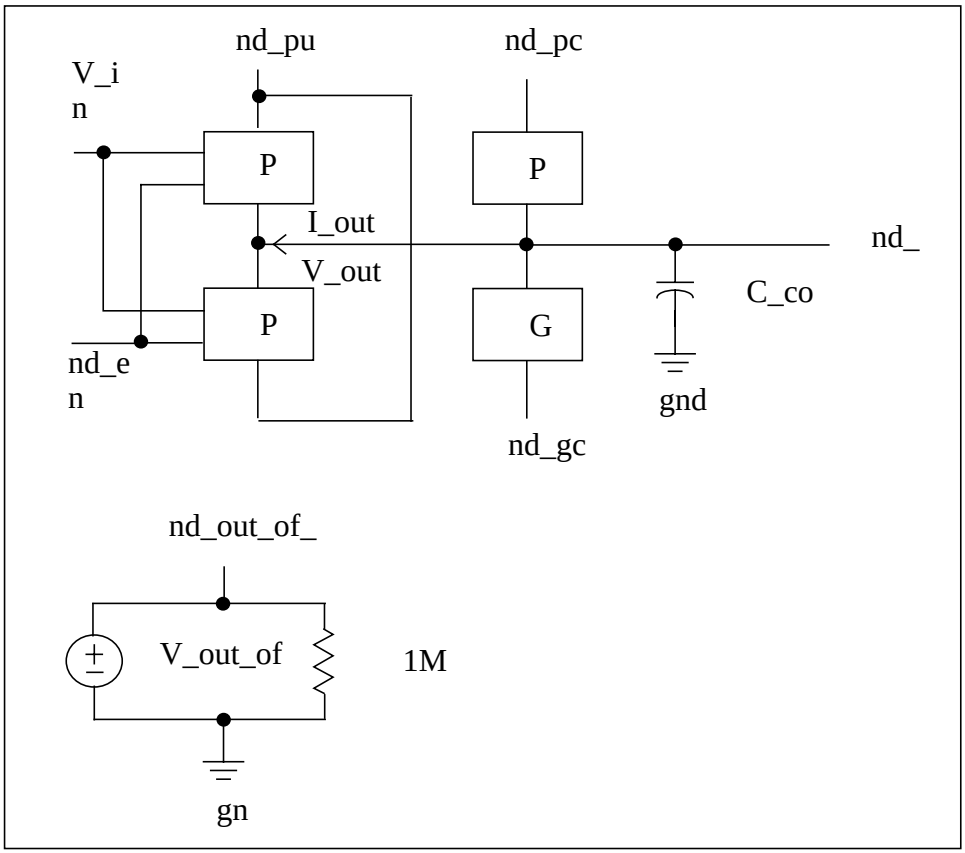
```
B_IO_ECL nd_pu nd_out nd_in nd_en nd_out_of_in [nd_pc nd_gc]
+ file='file_name' model='model_name'
+ [typ={typ|min|max|fast|slow}] [power={on|off}]
+ [buffer={13|io_ecl}]
+ [xv_pu=state_pu] [xv_pd=state_pd]
+ [interpol={1|2}]
+ [ramp_fwf={0|1|2}] [ramp_rwf={0|1|2}]
+ [fwf_tune=fwf_tune_value] [rwf_tune=rwf_tune_value]
+ [nowarn]
+ [c_com_pu=c_com_pu_value]
+ [c_com_pc=c_com_pc_value]
+ [c_com_gc=c_com_gc_value]
+ [pu_scal=pu_scal_value]
+ [pd_scal=pd_scal_value]
+ [pc_scal=pc_scal_value]
+ [gc_scal=gc_scal_value]
+ [rwf_scal=rwf_scal_value]
+ [fwf_scal=fwf_scal_value]
+ [spu_scal=spu_scal_value]
+ [spd_scal=spd_scal_value]
```

Nodes *nd_pc* and *nd_gc* are optional. However, either both or none can be specified. The total number of external nodes is either 5 or 7, any other number is an error. The tristate ECL buffer does not have a pulldown node. The pulldown table in the IBIS file is referenced in respect to pullup voltage.

If nodes *nd_pc* and *nd_gc* are not given on the element card but Power_Clamp and/or Ground_Clamp I-V curves are present in the model in question, then the simulator will issue an error message (this simulator behavior is different from that for Input-Output buffer).

In other respects, the input-output ECL buffer is similar to the input-output buffer. See “Input/Output Buffer” on page 7-16 for more information.

Figure 7-9: Input-Output ECL Buffer



Specifying Common Keywords

Required Keywords

file='file_name'

Identifies the IBIS file. *file_name* must be lower case and specify either the absolute path for the file or the relative path in respect to the directory from which you run the simulator.

Example

```
file = '.ibis/at16245.ibs'
file = '/home/oneuser/ibis/models/abc.ibs'
```

model='model_name'

Identifies the model for a buffer from the IBIS file, specified with keyword file='...'. The keyword *model_name* is case sensitive and must match one of the models from the IBIS file.

Example

```
model = 'ABC_1234_out'
model = 'abc_1234_IN'
```

Optional Keywords

All other keywords are optional; if not used, default values will be selected. Optional keywords are enclosed in square brackets [ ] in the buffer cards.

The notation keyword={val_1|val_2|...|val_n} is used to denote that the keyword takes a value from the set *val_1*, *val_2*, ... , *val_n*. The order of the keywords is not important.

buffer= {Buffer_Number | Buffer_Type}

Where *buffer_number* is an integer from the range $1 \leq N \leq 17$. Each buffer has an assigned number as follows:

Buffer Type	Buffer Number	Number of nodes (nominal or min/max)	Notes
INPUT	1	4	
OUTPUT	2	4/6	
INPUT_OUTPUT	3	6/8	
THREE_STATE	4	5/7	
OPEN_DRAIN	5	4/6	
IO_OPEN_DRAIN	6	6/8	
OPEN_SINK	7	4/6	
IO_OPEN_SINK	8	6/8	
OPEN_SOURCE	9	4/6	
IO_OPEN_SOURCE	10	6/8	
INPUT_ECL	11	4	
OUTPUT_ECL	12	3/5	
IO_ECL	13	5/7	
THREE_STATE_ECL	14	4/6	was 17
SERIES	15	not implemented	
SERIES_SWITCH	16	not implemented	
TERMINATOR	17	not implemented	was 14

The value of *buffer_number* and *buffer_type* should match the buffer type specified by keyword *model='...'*. The keyword *buffer= {Buffer_Number | Buffer_Type}* provides an extra check for the input netlist. If the keyword is omitted, this checking is not performed.

typ={typ|min|max|fast|slow}

If the value of the buffer parameter *typ* is either *typ*, or *min*, or *max*, then this value signifies the column in the IBIS file from which the data are used for the current simulation. The default is *typ=typ*. If *min* or *max* data are not available, *typ* data are used instead.

If the value of the buffer parameter *typ* is *fast* or *slow*, then certain combinations of *min* and *max* data are used. The following table specifies the exact type of data used for *fast* and *slow* values. Note that the table lists all the parameters and data types for all implemented buffers. Specific buffers use relevant data only. No buffer uses all the data given in the table (for example, the Rgnd, Rpower, Rac, Cac parameters are specified and used only for the terminator).

hsp_ver=hspice_version

The default is the current version of the Star-Hspice simulator. If you prefer the previous version of the IBIS buffer, then you can use the following statement:

```
hsp_ver = 2001.2
```

Parameter/Data	Fast	Slow
C_comp	min	max
Temp_Range	max	min
Voltage_Range	max	min
Pullup_Ref	max	min
Pulldown_Ref	min	max
POWER_Clamp_Ref	max	min
GND_Clamp_Ref	min	max
Rgnd	max	min
Rpower	max	min
Rac	max	min
Cac	min	max
Pulldown	max	min
Pullup	max	min
GND_ Clamp	max	min
POWER_Clamp	max	min
Ramp	max	min
Rising_waveform	max	min
Falling_waveform	max	min
V_fixture	max	min

power={on|off}

Default is *power=on.* Connect buffers to power sources that are specified in the IBIS file with keywords *Voltage Range*, *Pullup Reference*, *Pulldown Reference*, *POWER Clamp Reference*, and *GND Clamp Reference*.

By default, simulation connects required voltage sources for such external nodes as *Pullup*, *Pulldown*, *Power_Clamp*, and *Ground_Clamp* if applicable. You should not connect these nodes to voltage sources. However, names for these nodes should be provided, so you can print out the voltage values if required. For example:

```
.PRINT V(node_pullup)
```

If *power=off* is used, then the internal voltage sources are not included in the buffer and you are responsible for adding external voltage sources. Use this option if the voltage source is not connected directly to buffer nodes but through a circuit to account for parasitic RLC, to simulate power/ground bounce, and so on.

interpol={1|2}

Default is *interpol=1* (recommended). The I/V curves and V(t) curves need to be interpolated. Keyword *interpol=1* uses linear interpolation and *interpol=2* uses quadratic bi-spline interpolation.

xv_pu=nd_state_pu
xv_pd=nd_state_pd

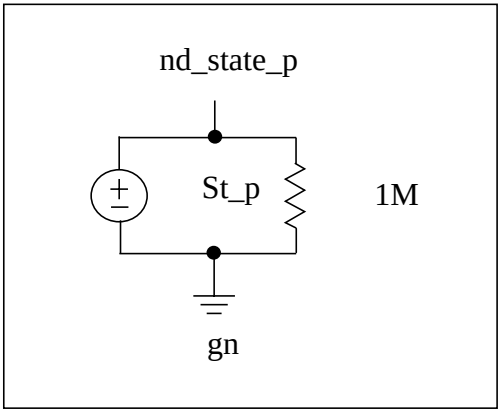
The buffers with output function (output, input-output, tristate, and so on) are controlled by one (input) or two (input and enable) controlling signals. Describe the state of a buffer at any moment with two state variables, *St_pu* and *St_pd*, which vary from 0 to 1. For example, if the output buffer is in LOW state, then *St_pu=0*, *St_pd=1*. If the output buffer transitions from a LOW state to HIGH state, then *St_pu* continuously changes from 0 to 1, while *St_pd* goes from 1 to 0. The actual time dependence for such a transition is derived from either ramp data or waveform(s).

You might want to know exactly how the transition takes place. The keywords *xv_pu=nd_state_pu*, *xv_pd=nd_state_pd* provide such information. Here *nd_state_pu* and *nd_state_pd* are names of additional nodes (which must be unique, and are treated as any other node from the netlist, except for a 16-character limitation). If the keyword(s) are included, then simulation adds voltage source(s) (with 1MOhm parallel resistor).

The values of the voltages are equal to *St_pu* and *St_pd*. They can be printed or displayed as follows:

```
.PRINT V(nd_state_pu) V(nd_state_pd)].
```

Figure 7-10: Equivalent Circuit for xv_pu=nd_state_pu Keyword



ramp_fwf={0|1|2}
ramp_rwf={0|1|2}

Default is *ramp_fwf=0*, *ramp*_rwf=0. If ramp and/or waveform(s) data are available, then these options allow you to choose which data to use.

The *ramp_fwf* parameter controls falling waveform(s)/ramp. The *ramp_rwf* parameter controls rising waveform(s)/ramp.

- Value 0 denotes use ramp data.
- Value 1 denotes use one waveform:
  - For ramp_fwf=1, if more than one falling waveform is available, the first falling waveform found for the model in question will be used.
  - For ramp_rwf=1, if more than one rising waveform is available, the first rising waveform found for the model in question will be used.
- Value 2 denotes use two waveforms:
  - For ramp_fwf=2, if more than two falling waveforms are available, the first two falling waveforms found for the model in question will be used.
  - For ramp_rwf=2, if more than two rising waveforms are available, the first two rising waveforms found for the model in question will be used.

If in-circuit simulation cannot perform a specified type of processing (for example, if *ramp_fwf=2* is specified, but only one falling waveform is found), it decrements values of *ramp_fwf* and/or *ramp_rwf* by one and attempts to process the new value(s) of *ramp_fwf* and/or *ramp_rwf*. In this case, a warning is printed (unless the nowarn option is set).

Note: The ramp_fwf and ramp_rwf parameters are independent, and can have different values.

---

fwf_tune=fwf_tune_value rwf_tune=rwf_tune_value

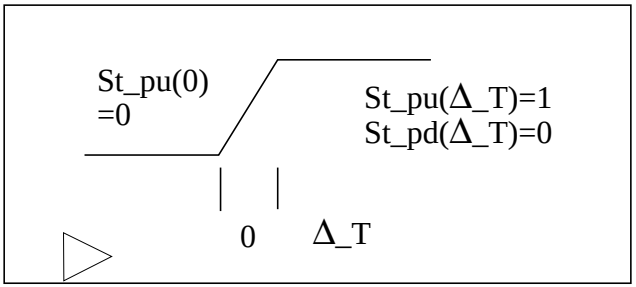
The *fwf_tune_value* and *rwf_tune_value* keywords are numbers between 0 and 1. The default is *fwf_tune=0.1, rwf_tune=0.1*.

The following two parameters control the algorithm for processing ramp and waveforms:

- fwf_tune is used only if ramp_fwf is 0 or 1.
- rwf_tune is used only if ramp_rwf is 0 or 1.

The effect of these parameters when switching the output buffer from `LOW` to `HIGH` is illustrated in Figure 7-11.

Figure 7-11: Change in Values of St_pu(t) and St_pd(t) When a Buffer is Switched from LOW to HIGH



Initially, *St_pd=1, St_pu=0*. Both ramp data and a single rising waveform provide information about the switching process and, in particular, a time interval, *delta_T*, during which the transition from LOW -> HIGH occurs. The difference between the two data types (ramp and a single rising waveform) is that the shape of the waveform for ramp is fixed as a linearly growing function from LOW to HIGH, while an actual waveform accounts for an arbitrary time dependence.

However, this is not enough information to determine St_pu(t) and St_pd(t) [recall that St_pu(0)=0, St_pd(0)=1, St_pu(delta_T)=1, St_pd(delta_T)=0]. Mathematically, we have one linear equation with two unknowns that have an infinite number of solutions. To resolve this problem, additional conditions on St_pu, St_pd should be imposed (some use St_pu+St_pd=1).

Avant! simulation device models use the following approach.

Because the circuitry that goes from ON to OFF (for rising waveforms, pulldown circuitry) usually undergoes this transition much faster than the circuitry that goes from OFF to ON (for rising waveforms, pullup circuitry), we specify a fraction of time in units of *delta_T* during which the circuitry that goes from ON to OFF undergoes the transition.

Therefore, if rwf_tune=0.1, then during 0.1*delta_T the pulldown circuitry switches from ON to OFF. The transition is a linear function of time. After imposing this additional condition, we can uniquely find the rate of transition for the circuitry that goes from the OFF state to ON state.

This approach is also valid for the *fwf_tune* parameter.

Parameters *fwf_tune* and *rwf_tune* should be considered tuning parameters. The significance of these parameters strongly depends on I/V curves for pullup and pulldown circuitries. A change in *fwf_tune* and *rwf_tune* can be insignificant or very significant depending on the I/V curves. We recommend that you adjust these parameters slightly to evaluate the accuracy of the model.

Note, that in the case of two waveforms, the corresponding system of equations is completely defined mathematically and parameters *fwf_tune* and *rwf_tune* are not used (ignored if specified). However, if data given in two waveforms are inaccurate or inconsistent with other data, in-circuit simulation can use single waveform or ramp data instead of two waveforms (giving a warning). If this occurs, fwf_tune and/or rwf_tune are used even if ramp_fwf=2, ramp_rwf=2.

If the two-waveform data are inconsistent or inaccurate, the results can be less accurate than ramp or one-waveform results. We recommend that two-waveform results be compared against ramp and one-waveform results.

The algorithm used to find the evolution of states in the case of ramp data and single waveform can be augmented by other algorithms if there are such requests from the users.

The keywords, *xv_pu=nd_state_pu* and *xv_pd=nd_state_pd*, can be used to print and/or view the state evolution functions *St_pu(t)* and *St_pd(t)*.

nowarn

The keyword *nowarn* suppresses warning messages from the IBIS parser. Note that there is no equal sign "=" and value after the *nowarn* keyword. Do not use *nowarn* as the first keyword after the nodes list. There should be at least one keyword followed by "=" and a value between the list of nodes and the nowarn keyword.

```
c_com_pu = c_com_pu_value
c_com_pd = c_com_pd_value
c_com_pc = c_com_pc_value
c_com_gc = c_com_gc_value
```

By default (default 1) the die capacitance C_comp is connected between *node_out (nd_in* for input buffer) and ideal ground. For simulating power bounce and ground bounce it may be desirable to split C_comp into several parts and connect between *node_out (nd_in* for input buffer) and some (or all) of the *node_pu*, *node_pd*, *node_pc*, *node_gc* nodes.

If you specify at least one of the optional parameters (c_com_pu, c_com_pd, c_com_pc, c_com_gc), then the default 1 does not apply, and unspecified parameters have a value of zero (default 2). The c_com_pu, c_com_pd, c_com_pc, c_com_gc values are dimensionless, and denote fractions of C_comp connected between *node_out (nd_in* for input buffer) and respective nodes (either *node_pu, node_pd, node_pc*, or *node_gc)*. For example, C_comp*c_com_pu is capacitance connected between *node_out* and *node_pu*.

If given, values of c_com_pu , c_com_pd , c_com_pc , and c_com_gc should be nonnegative.

It is expected that c_com_pu + c_com_pd + c_com_pc + c_com_gc = 1, however Hspice-based simulators do not enforce this requirement, and warn you only if the requirement is not satisfied. In this case, the states are derived under the assumption that the die has C_comp specified in the IBIS files while during simulation different value of C_comp used, namely C_comp*(c_com_pu+c_com_pd+c_com_pc+c_com_gc). Effectively it means that some additional capacitance is connected in parallel to C_comp (possibly negative).

In the case of buffer types: output, input-output, 3-state, if nodes *node_pc* and *node_gc* are not specified in the netlist, c_com_pc is added to c_com_pu and c_com_gc is added to c_com_pd (after that c_com_pc and c_com_gc are not used anymore).

In the case of buffer types: open drain, open sink, input-output open drain, input-output open sink if nodes *node_pc* and *node_gc* are not specified in the netlist, c_com_pc if given is ignored, c_com_gc is added to c_com_pd (after that c_com_gc is not used anymore).

In the case of buffer types: open source, input-output open source, if nodes *node_pc* and *node_gc* are not specified in the netlist, c_com_gc if given is ignored, c_com_pc is added to c_com_pu (after that c_com_pc is not used anymore).

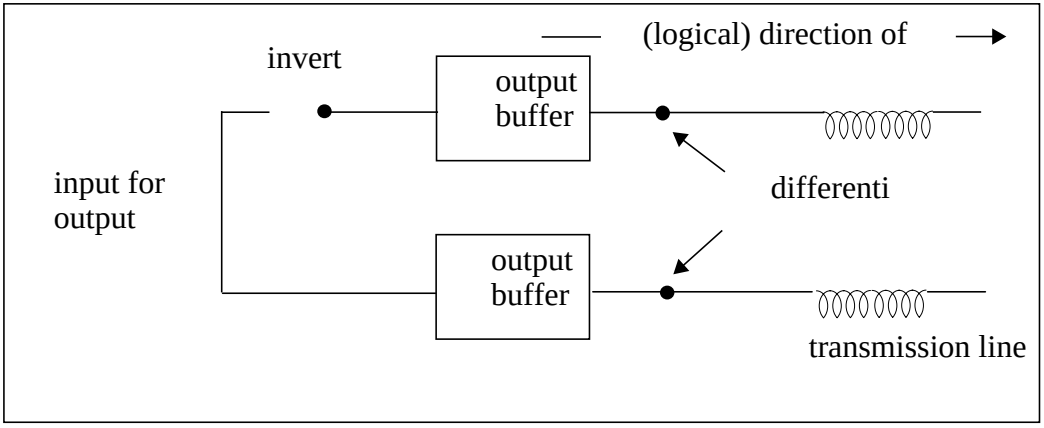
In the case of buffer types: output ECL, input-output ECL, 3-state ECL if nodes *node_pc* and *node_gc* are not specified in the netlist, c_com_pc and c_com_gc are ignored (assign zero values).

In the case of buffer types: output ECL, input-output ECL, 3-state ECL if c_com_pd is not zero, it is added to c_com_pu (c_com_pd is not used after that).

Differential Pins

Differential pins refer to the relationship between buffers. Differential pins are specified in the “Component Description” section of the IBIS standard. Figure 7-12 and Figure 7-13, and the examples that follow these figures, explain how you can simulate differential pins, using the Avant! implementation of IBIS.

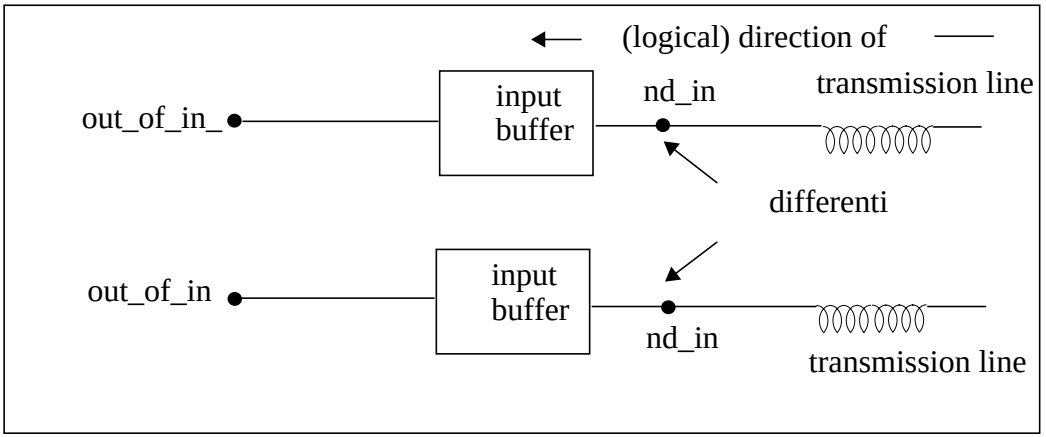
Figure 7-12: Output buffers



You must use two separate buffers, each of which is specified by a separate card in the netlist. They are related only through their input, which is differential.

The only way the inverter can implement in this situation is by specifying two independent voltage sources that have opposite polarity.

Figure 7-13: Input Buffers



Nodes *out_of_in_1*, *out_of_in_2* must be specified but are not used. In the case of differential input buffers, the voltage will be probed between *nd_in_1* and *nd_in_2* and processed by a voltage dependent voltage source as described below.

V_diff is a differential voltage parameter from the IBIS file (default is 200 mV). Add definition of parameter *V_diff*, voltage controlled voltage source *E_diff_out_of_in*, and a resistor *R_diff_out_of_in.*

Example

```
.PARAM V_diff = 0.2
E_diff_out_of_in diff_out_of_in 0 PWL(1) nd_in_1 nd_in_2
+ '- V_diff' 0 '+ V_diff' 1 R_diff_out_of_in
   + diff_out_of_in 0 1x
```

Use the voltage across *R_diff_out_of_in* as the output of the differential input buffer.

```
If V(nd_in_1) - V(nd_in_2) < V_diff, V(diff_out_of_in) = 0
if V(nd_in_1) - V(nd_in_2) > V_diff, V(diff_out_of_in) = 1
```

Scaling Buffer Strength

Sometimes there is a need to scale buffer strength (that is, increase or decrease current for output type buffers for a given value of the output voltage). This enables the same IBIS file to be used to simulate buffers of different strengths. Let us designate K as a factor for current multiplication. For the original buffer, the value of K=1. This section describes how to accomplish this scaling using the F-element for a single output buffer and differential output buffer.

The original circuit for a single output buffer is as follows:

```
Buffer nd_pu nd_pd nd_out nd_pc nd_gc
+  file=<filename> model=<modelname>
+ Rload nd_out gnd Rload_val
```

The scaled circuit for a single output buffer is as follows:

```
Buffer nd_pu nd_pd nd_out nd_pc nd_gc
+ file=<filename> model=<modelname>
+ Vsenser nd_out  nd_out_prime V=0
+ Rload nd_out_prime gnd Rload_val
+ Felement gnd nd_out_prime Vsenser K-1
```

The original circuit for a differential output buffer is as follows:

```
Buffer1 nd_pu1 nd_pd1 nd_out1 nd_pc1 nd_gc1
+ file=<filename1> model=<modelname1>
Buffer2 nd_pu2 nd_pd2 nd_out2 nd_pc2 nd_gc2
+ file=<filename2> model=<modelname2>
+ R_load  n_out1 n_out2 R_load_value
```

The scaled circuit for a differential output buffer is as follows:

```
Buffer1 nd_pu1 nd_pd1 nd_out1 nd_pc1 nd_gc1
+ file=<filename1> model=<modelname1>
Buffer2 nd_pu2 nd_pd2 nd_out2 nd_pc2 nd_gc2
+ file=<filename2> model=<modelname2>
+ V_sense n_out1 n_out1_prime 0V
+ F_element n_out2 n_out1_prime v_sense K-1
+ R_load  n_out1_prime n_out2 R_load_value
```

Notice the polarity of the F-element. For the K=1 scaling factor, the current-controlled current source does not supply any current, so effectively you are still using the original circuit.

Buffers in subcircuits

```
*********************************************
* example 1 * buffers in subcircuit, power=on
*********************************************

v_in1 nd_in1 0 pulse
+ ( 0V 1.0V CLK_Q_PRD DLT_TIME DLT_TIME CLK_H_PRD CLK_PRD )
v_en1 nd_en1 0 1V
v_in2 nd_in2 0 pulse
+ ( 1.1V 0V CLK_Q_PRD DLT_TIME DLT_TIME CLK_H_PRD CLK_PRD )
v_en2 nd_en2 0 1V

x1 nd_out1 nd_in1 nd_en1 nd_outofin1 buffer11
x2 nd_out2 nd_in2 nd_en2 nd_outofin2 buffer11

R_load nd_out1 nd_out2 50

.subckt buffer11 nd_out0 nd_in0 nd_en0 nd_outofin0
b_io_0 nd_pu0 nd_pd0 nd_out nd_in0 nd_en0 nd_outofin0 nd_pc0
   nd_gc0
+ file = '92lv090b.ibs'
+ model = 'DS92LV090A_DOUT'
+ typ=typ power=on
+ buffer=3
+ interpol=1
+ xpin nd_out nd_out0 pin22
.ends

.subckt pin22 nd_out nd_out0
R_pin nd_out_c nd_out0 50m
C_pin nd_out_c 0  0.3p
L_pin nd_out nd_out_c 2n
.ends
```

In this example buffers are connected to power sources implicitly, inside the subcircuit. Subcircuit external terminals does not need to include *nd_pu*, *nd_pd*, *nd_pc*, *nd_gc*.

```
*******************************************
* example 2* buffers in subcircuit, power=off
*******************************************
v_in1 nd_in1 0 pulse
+ ( 0V 1.0V CLK_Q_PRD DLT_TIME DLT_TIME CLK_H_PRD CLK_PRD )
v_en1 nd_en1 0 1V
v_in2 nd_in2 0 pulse
+ ( 1.1V 0V CLK_Q_PRD DLT_TIME DLT_TIME CLK_H_PRD CLK_PRD )
v_en2 nd_en2 0 1V

x1 nd_power 0 nd_out1 nd_in1 nd_en1 nd_outofin1 nd_power 0
   buffer11
x2 nd_power 0 nd_out2 nd_in2 nd_en2 nd_outofin2 nd_power 0
   buffer11

R_load nd_out1 nd_out2 50

.subckt buffer11 nd_pu0 nd_pd0 nd_out0 nd_in0 nd_en0
   nd_outofin0 nd_pc0 nd_gc0
r_0 nd_pu0 nd_pd0 1.23456789x
b_io_0 nd_pu0 nd_pd0 nd_out nd_in0 nd_en0 nd_outofin0 nd_pc0
   nd_gc0
+ file = '92lv090b.ibs'
+ model = 'DS92LV090A_DOUT'
+ typ=typ power=off
+ buffer=3
+ interpol=1
+ xpin nd_out nd_out0 pin22
.ends

.subckt pin22 nd_out nd_out0
R_pin nd_out_c nd_out0 50m
C_pin nd_out_c 0  0.3p
L_pin nd_out nd_out_c 2n
.ends

V_power nd_power 0 3.3V
```

In this example, only one voltage source, V_power, is used to power all buffers. All power nodes, *nd_pu*, *nd_pd*, *nd_pc*, *nd_gc*, should be explicitly provided.

Example

Below is a complete example of the netlist that contains an output buffer, transmission line, and input buffer.

A digital signal is supplied to the node *nd_in*. It is transmitted by the output buffer to a network, goes through a transmission line, is received by an input buffer, and transformed into digital form and available on node *nd_out_of_in_1*. IBIS file at16245a.ibs resides in the directory .ibis, which is located in the directory from which you run the simulator.

```
*********************************************************
* test for iob: output buffer—transmission line—input buffer
*********************************************************

.option post probe
*********************************************************
* Analysis
*********************************************************

.tran 0.05n 20n
*********************************************************
* Stimuli
*********************************************************

V_in nd_in 0 1V pulse ( 0V 1V 1n 1n 1n 4n 10n )
*********************************************************
* Output
*********************************************************

.print tran v(nd_pu) v(nd_pd) v(nd_out) v(nd_in)
+ v(nd_in_1) v(nd_out_of_in_1)
*********************************************************
* OUTPUT BUFFER
*********************************************************

b2 nd_pu nd_pd nd_out nd_in nd_pc nd_gc
+ file = '.ibis/at16245a.ibs'
+ model = 'AT16245_OUT'
```

```
*********************************************************
* TRANSMISSION LINE
*********************************************************

.PARAM Z_0=50
.PARAM T_delay=10ns
.PARAM Length=1mm

W1 N=1 nd_out GND nd_in_1 GND Umodel=Uname L=Length
.model Uname u nl=1 LEVEL=3 elev=3 llev=0 plev=1 nlay=2
+ zk=Z_0 delay=T_delay

*********************************************************
* INPUT BUFFER
*********************************************************

b1 nd_pc_1 nd_gc_1 nd_in_1 nd_out_of_in_1
+ file = '.ibis/at16245a.ibs'
+ model = 'AT16245_IN'

*********************************************************
.end
```

Using the IBIS Buffer Component

The Input/Output Buffer Information Specification (IBIS) is being developed by the IBIS Open Forum, which is affiliated with the Electronic Industries Alliance (EIA).

IBIS specifies a standard form to present information in ASCII format, using special files. This information describes the behavior of various I/O buffers that send electrical signals outside the silicon chip, or receive such signals. The type of information includes:

- Output I-V curves for output buffers, in LOWand HIGH states.
- V(t) curves, describing the exact form of transitions from LOW to HIGH states, and from HIGH to LOW states, for a specified load.
- Values for die capacitance.
- Electrical parameters of the packages.

The Avant! True-Hspice models implement buffers as a standard *b* element. But to support simulation of IBIS models using .ebd and .pkg, True-Hspice IBIS models include another component that *creates* buffers for an integrated circuit.

Understanding the .ibis Command

The general syntax of the .ibis command for a component is :

```
.ibis cname keyword_1 = value_1 ...    [keyword_M=value_M]
```

where:

cname	Instance name of this `ibis` command
keyword_i=value_i	Assigns the *value_i* value, to the *keyword_i* keyword. Optional keywords are in the square brackets.

Required Keywords

file='*file_name*'

Identifies the IBIS file. *file_name* must be lower case, and must specify either the absolute path for the file, or the relative path in respect to the directory from which you run simulation.

Examples

```
file = '.ibis/at16245.ibs'
file = '/home/oneuser/ibis/models/abc.ibs'
```

component='*component_name*'

Identifies the component for a .ibis command from the IBIS file, specified using the `file='...'` keyword. The `component_name` keyword is case-sensitive, and must match one of the components from the IBIS file.

Examples

```
component = 'procfast'
component = 'Virtex_SSTL_3-I_BG432'
```

subname='*subckt_name*'

Identifies the subname to which you add the component buffers. The '*subckt_name*' must be the name of a sub-circuit that you defined in your Hspice netlist. The sub-circuit pins must also match the component in the .ibs file.

Note: The component name and file name are defined in the *component* and *file* keywords.

Optional Keywords

The following keywords are the same as for the *b*-element (I/O buffer). For more information, see Specifying Common Keywords on page 7-27.

- typ
- interpo
- ramp_rwf
- ramp_fwf
- rwf_tune
- fwf_tune
- pd_scal
- pu_scal
- pc_scal
- gc_scal
- rwf_scal
- fwf_scal
- nowarn
- hsp_ver
- c_com_pu
- c_com_pd
- c_com_pc
- c_com_gc

How .ibis Creates Buffers

The .ibis command adds a buffer to the netlist for every pin, according to the signal_name and model_name defined in the [Pin] keyword in the .ibs file.

Note: .ibis does not create a buffer if the pin name is a reserved model name, such as POWER, GND, or NC.

```
buffer_name = 'cname'_'signal_name'
```

- *cname* is defined in the .ibis card in the .sp netlist.
- *signal_name* is defined in the [Pin] keyword in the .ibs file

The pins, and the elements that connect to these pins in the sub-circuit, are divided. The node name of the elements are changed from subcircuit's pins to

'bufn_<*pin_number*>'

- <*pin_number*> is 1 if this pin is the first pin defined in the [Pin] keyword.
- <*pin_number*> is 2 if this pin is the second pin.

and so on.

The buffers are inserted between the 'bufn_<*pin_number*>' node and the pin.

Example

A file named `test.ibs` contains the following messages:

```
[Component]  TEST
[Manufacturer] Intel Corporation
[Package]
|           typ               min            max
R_pkg       50.000mOhm        40.000mOhm     60.000mOhm
L_pkg       5.00nH            4.00nH         6.00nH
C_pkg       2.00pF            1.00pF         3.00pF
[PIN]     signal_name   model_name  R_pin   L_pin   C_pin
  a1      Vcc           Power
  a2      GND           GND
  ai      Inbuf         in_buf5
  ao      IO50buf       io50v
```

A netlist named `test.sp` contains the following commands:

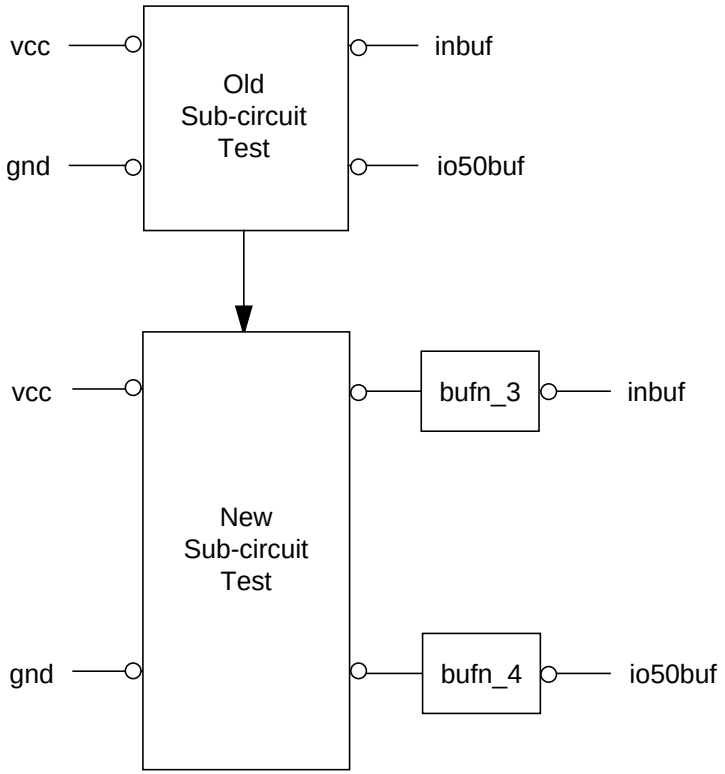
```
.ibis comp component='TEST'
+  file='test.ibs' subname= 'test'
+  [typ=fast]
+  [interpol={1}]
+  [nowarn]
+  ......
.subckt test vcc1 gnd1 inbuf io50buf
......
.ends
xtest vcc gnd in out test
.......
```

For this example, the `.ibis` command creates two buffers: `ptest_inbuf` and `ptest_io50buf`.

The subcircuit test changes, as shown in Figure 7-14:

- The `bufn_3` node connects to the elements in the sub-circuit test, to which the `inbuf` node previously connected.
- The `bufn_4` node connects to the elements in the sub-circuit test, to which the `io50buf` node previously connected.

Figure 7-14: Altered Sub-circuuit Test



Using the Buffer Component

The component creates buffers that are always connected to the power sources that you specified in the IBIS file. To specify power sources, use the Voltage Range, Pullup Reference, Pulldown Reference, POWER Clamp Reference, and GND Clamp Reference keywords.

The nodes of buffers expect input and output node names in the following format:

'buffer_name'_<node_name>
buffer_name = 'cname'_'signal_name'

where:

- *cname* is defined in the .ibis card in the the .sp netlist.
- *signal_name* is defined in the [Pin] keyword in the .ibs file
- <*node_name*> is different for different types of buffers:

```
INPUT             'pc', 'gc',
OUTPUT            'pu', 'pd', 'pc', 'gc'
INPUT_OUTPUT      'pu', 'pd', 'en', 'outofin', 'pc', 'gc'
THREE_STATE       'pu', 'pd', 'en', 'pc', 'gc'
OPEN_DRAIN        'pu', 'pd', 'pc', 'gc'
IO_OPEN_DRAIN     'pu', 'pd', 'en', 'outofin', 'pc', 'gc'
OPEN_SINK         'pu', 'pd', 'pc', 'gc'
IO_OPEN_SINK      'pu', 'pd', 'en', 'outofin', 'pc', 'gc',
OPEN_SOURCE       'pu', 'pd', , 'pc', 'gc'
IO_OPEN_SOURCE    'pu', 'pd', 'en', 'outofin', 'pc', 'gc',
INPUT_ECL         'pc', 'gc',
OUTPUT_ECL        'pu', 'pc', 'gc'
IO_ECL            'pu', 'en', 'outofin', 'pc', 'gc'
THREE_STATE_ECL   'pu', 'en', 'pc', 'gc'
```

Note: For more information about nodes for different buffers, see Buffers on page 7-6.

The names of the input and output nodes for the buffers are:

INPUT and INPUT_ECL buffers	signal name of pin ('in') ' bufn_<*pin_number*>' ('outofin')
Other types of buffers	'bufn_<*pin_number*>'('in') signal name of pin ('out')

- <*pin_number*> is 1 if this pin is the first pin defined in the [Pin] keyword.
- <*pin_number*> is 2 if this pin is the second pin.

and so on.

Note: If the buffer has an enable terminal, you must create a node named *buffer_name*_en to enable the buffer.

Example

The .ibis command creates an input buffer named `ptest_inbuf`, and an input-output buffer named `ptest_io50buf`.

```
.subckt test vcc1 gnd1 inbuf io50buf
......
ven1 ptest_io50buf_en vcc1 0v
.ends
xtest vcc gnd in out test
  rout out gnd 50
  ......
.print v(xtest.ptest_inbuf_pc)       $ pc node of ptest_inbuf
+      v(xtest.ptest_inbuf_gc)       $ gc node of ptest_inbuf
+      v(in)                         $ in node of ptest_inbuf
+      v(bufn_3)                     $ outofin node of ptest_inbuf
+      v(xtest.ptest_io50buf_pu)     $ pu node of ptest_io50buf
+      v(xtest.ptest_io50buf_pd)     $ pd node of ptest_io50buf
+      v(xtest.ptest_io50buf_outofin)$ outofin node of ptest_io50buf
+      v(xtest.ptest_io50buf_pc)     $ pc node of ptest_io50buf
+      v(xtest.ptest_io50buf_gc)     $ gc node of ptest_io50buf
+      v(xtest.ptest_io50buf_en)     $ enable node of ptest_io50buf
+      v(out)                        $ out node of ptest_io50buf
+      v(bufn_4)                     $ in node of ptest_io50buf
```

Simulating the Component with pkg and ebd

If you want to simulate the IBIS buffer component with .pkg and .ebd, add the following option:

```
pkgmap,pkgtyp,ebdmap,ebdtyp
```

For more information, see the "PKG and EBD Simulation" section in Chapter 3, "Specifying Simulation Input and Controls", in the *Star-Hspice Manual*.

Additional Notes

This section provides some additional notes about IBIS models, to clarify technical issues. Most of this information was developed as a result of customer interaction.

Keywords

The *fwf_tune*, *rwf_tune* parameters specify transition time for circuitry (either pullup or pulldown) that goes from the ON to OFF state as a fraction of time, *delta_T*, for a transition for the opposite circuitry (either pulldown or pullup) from OFF to ON state. The *delta_T* value for ramp data transition time is different from the value for single waveform transition time (*delta_T* depends on parameters *ramp_fwf* and *ramp_rwf).* Consequently, the absolute values for transition time from the ON to OFF state are different for ramp data and single waveform data.

Voltage Thresholds

Voltages applied to the input node and enable node are digital signals. They should be either 0 or 1. It is acceptable to specify input voltage as:

```
V_in nd_in 0 pulse (0 3.3 0 0.5n 0.5n 4n 8n)
```

However, in-circuit simulation currently detects only two thresholds, 20% and 80% of [0,1] swing, i.e., 0.2V and 0.8V. If a buffer is non-inverting and in a LOW state, it will start transition to a HIGH state, if V_in > 0.8V. If the buffer is in HIGH state, it will start the transition to LOW state, if V_in < 0.2V. Specifying input voltage in the range [0, 3.3V] as in the above example does not make LOW -> HIGH transitions better in any way, but can add uncertainty over time interval 0.5ns, when the transition actually occurs.

.OPTION D_IBIS

The d_ibis option specifies the directory where IBIS files are located. Example of usage:

```
.OPTION d_ibis='/home/user/ibis/models'
```

If several directories are specified, then simulation looks for IBIS files in the local directory (the directory from which you run the simulation), then in the directories specified through .option d_ibis in the order that .option cards appear in the netlist. At most, four directories can be specified through d_ibis option. Examples of usage:

```
.OPTION d_ibis='/nfs/port/user/hspice/run/subckt/optd'
+ buffer nd_pu nd_pd nd_out nd_in
+ file = 'opt.ibs'
+ model = 'DS92LV090A_DOUT'
```

The d_ibis option is case-sensitive.

Sub-model

Each buffer can call one Dynamic_clamp or one Bus_hold.

- Dynamic_clamp is automatically set to the *All* mode.
- Bus_hold is automatically set to the *Non-driving* mode.

Note: If you use more than one Bus_hold, combine them to acquire the accurate result.

You can define the *Off_delay* parameter on both the rising edge and the falling edge. You can use this parameter with both the *V_trigger_r* and the *V_trigger_f* parameters.

Driver Schedule

Driver schedule connects the buffers together, to form the more complicated buffer behavior. The scheduled buffer should have the same node list as the top buffer.

For example, you can use the *output* buffer to schedule the *open_drain* buffer.

The delay parameter, such as *rise_on_dly*, should be consistent with the polarity of the scheduled driver. If the buffer inverts, then the rising edge turns on the pulldown device, and the *rise_on_dly* parameter means that the pulldown device automatically turns off after the *rise_on_dly-rise_off_dly* period.

Warning and Error Messages

If certain conditions are met (or not met), simulation prints warnings or error messages. Some examples of these messages are described below.

Warnings are issued if the input data is inconsistent. In this case, simulation modifies data to make consistent and runs the simulation with modified data. Static I/V curves take precedence over V(t) curves and ramp data. If simulation modifies your data, it is unlikely the results of simulation with a test load will match V(t) curves specified in the IBIS file. To achieve high accuracy, input data should be consistent. Pay close attention to warnings and understand the causes.

Errors are issued if the simulation cannot continue, using the specified data.

Example

An example of a warning:

```
** warning** iob_eles2:205:
   text of the warning, line1
   text of the warning, line2
```

An example of an error:

```
** error** iob_eles2:205:
   text of the error, line1
   text of the error, line2
```

Text that follows the comments '`** warning**`' and '`** error**`', such as '`iob_eles2:205:`' identifies the location where the problem occurs. It is intended to help the developer solve the problem.

The following information is intended for users. A list of selected warnings follows.

1. I/V Curves

   PC and GC I-V curves should be equal to zero at zero voltage, I(V=0)=0. If different values are found, a warning is issued. For example, for a PC I/V curve the following warning is issued.

```
** warning** ffffffff:NNN:
    POWER_Clamp curve should be zero at origin
    found value 1.85800E-01
    I/V curve is not modified
```

This warning occurs for Power_Clamp and Ground_Clamp I/V curves. Simulation takes these I/V curves as given, but an error is likely to occur if I(V=0) is not zero.

2. I-V curves and rising/falling waveforms (RWF, FWF) should be consistent.

   Simulation verifies consistency for the end points of RWF, FWF. If inconsistency is detected, the I/V curves take precedence over V(t) curves, and V(t) curves are modified to make them consistent with I-V curves.

```
** warning** ffffffff:NNN:
    Falling WF min estimate and given value differ
    estimate = 3.3540E-01 given = 6.6000E-01
```

   In this example, I/V curves give a value of 3.3540E-01V for minimum voltage when pullup is OFF (if pullup is available) and pulldown is ON (if pulldown is available) for load specified for FWF. The minimum voltage value of FWF in the IBIS file is 6.6000E-01V. In this case, simulation modifies the FWF to be consistent with I-V curves.

1. I/V curves and ramp data should be consistent (if ramp is used).

   In-circuit simulation verifies consistency for end points of rising edge and falling edge. The IBIS standard requires that ramp data correspond to 20% to 80% transition of the total voltage change. If inconsistency is detected, the following warning appears:

```
** warning** ffffffff:NNN:
Inconsistency between Ramp and PD/PU data is detected.
dV_r=1.5900E+00 V_rwf_max=3.3000E+00 V_rwf_min=3.3540E-01
transition from 20% to 80% is not satisfied
FILE = gtl-plus.ibs
MODEL = io_buf
```

   In this example, voltage changes from 0.3354 V to 3.3 V on the rising edge, as calculated from I/V curves. 60% of this range is 1.78 V. The IBIS file gives 1.59 V. Simulation issues warnings, assumes that the derivative for the ramp is specified in the IBIS file, and the voltage range as calculated from I/V curves.

References

The official IBIS Open Forum web site is located at:

http://www.eia.org/EIG/IBIS/ibis.htm

This site contains articles introducing IBIS, text of the IBIS standard, examples of IBIS files, and tools such as the golden parser. The site also links to other web sites devoted to IBIS.

Other web and ftp sites that have information about IBIS are:

http://www.eda.org/pub/ibis/

http://www.vhdl.org/pub/ibis/

ftp://ftp.eda.org/pub/ibis/

ftp://ftp.vhdl.org/pub/ibis/

Avant!

Chapter 8
Introducing MOSFETs

A MOSFET is defined by the MOSFET model and element parameters, and two submodels selected by the CAPOP and ACM model parameters.

- The CAPOP model parameter specifies the model for the MOSFET gate capacitances.
- The ACM (Area Calculation Method) parameter selects the type of diode model to be used for the MOSFET bulk diodes.

Each of these submodels has associated parameters that define the characteristics of the gate capacitances and bulk diodes.

MOSFET models are either p-channel or n-channel models; they are classified according to level such as LEVEL 1 or LEVEL 50.

This chapter covers the design model and simulation aspects of MOSFET models, parameters of each model level, and associated equations. MOSFET diode and MOSFET capacitor model parameters and equations are also described.

For information about individual models and their parameters, see Chapter 9, “Selecting MOSFET Models: Level 1-40” and Chapter 10, “Selecting MOSFET Models: Level 47-63”.

This chapter describes:

- Understanding MOSFET Models
- Selecting Models
- General MOSFET Model Statement
- Nonplanar and Planar Technologies
- MOSFET Equivalent Circuits
- MOSFET Diode Models
- MOS Diode Equations
- Common Threshold Voltage Equations
- MOSFET Impact Ionization
- MOS Gate Capacitance Models
- Noise Models
- Temperature Parameters and Equations

Understanding MOSFET Models

The selection of the MOSFET model type for use in analysis usually depends on the electrical parameters critical to the application. LEVEL 1 models are most often used for simulation of large digital circuits where detailed analog models are not needed. LEVEL 1 models offer low simulation time and a relatively high level of accuracy with regard to timing calculations. When precision is required, as for analog data acquisition circuitry, use the more detailed models, such as the LEVEL 6 IDS model or one of the BSIM models (LEVEL 13, 39, or 49).

For precision modeling of integrated circuits, the BSIM models consider the variation of model parameters as a function of sensitivity of the geometric parameters. The BSIM models also reference a MOS charge conservation model for precision modeling of MOS capacitor effects.

Use the SOSFET model (LEVEL 27) to model silicon-on-sapphire MOS devices. You can include photocurrent effects at this level.

Use LEVELs 5 and LEVEL 38 for depletion MOS devices.

LEVEL 2 models consider bulk charge effects on current. LEVEL 3 models require less simulation time and provides as much accuracy as LEVEL 2 and have a greater tendency to converge. LEVEL 6 models are compatible with models originally developed with ASPEC. Use LEVEL 6 models to model ion-implanted devices.

Selecting Models

A MOS transistor is described by use of an element statement and a .MODEL statement.

The element statement defines the connectivity of the transistor and references the .MODEL statement. The .MODEL statement specifies either an n- or p-channel device, the level of the model, and a number of user-selectable model parameters.

Example

The following example specifies a PMOS MOSFET with a model reference name, PCH. The transistor is modeled using the LEVEL 13 BSIM model. The parameters are selected from the model parameter lists in this chapter.

```
M3 3 2 1 0 PCH <parameters>
.MODEL PCH PMOS LEVEL=13 <parameters>
```

Selecting MOSFET Model LEVELs

MOSFET models consist of client private and public models selected by the parameter .MODEL statement LEVEL parameter. Avant! constantly adds new models to the True-Hspice device models.

Not all MOSFET models are available in the PC version. The following table shows what is available for PC users. Models listed are either on all platforms, including PC, as indicated in the third column, or they are available on all platforms *except* the PC, as indicated in the last column.

Level	MOSFET Model Description	All Platforms including PC	All Platforms except PC
1	Schichman-Hodges model	X	
2	MOS2 Grove-Frohman model (SPICE 2G)	X	
3	MOS3 empirical model (SPICE 2G)	X	
4	Grove-Frohman: LEVEL 2 model derived from SPICE 2E.3	X	

Level	MOSFET Model Description	All Platforms including PC	All Platforms except PC
5	AMI-ASPEC depletion and enhancement (Taylor-Huang)	X	
6	Lattin-Jenkins-Grove (ASPEC style parasitics)	X	
7	Lattin-Jenkins-Grove (SPICE style parasitics)	X	
8	advanced LEVEL 2 model	X	
9 **	AMD		X
10 **	AMD		X
11	Fluke-Mosaid model		X
12 **	CASMOS model (GTE style)		X
13	BSIM model	X	
14 **	Siemens LEVEL=4		X
15	user-defined model based on LEVEL 3		X
16	not used	–	–
17	Cypress model		X
18 **	Sierra 1		X
19 ***	Dallas Semiconductor model		X
20 **	GE-CRD FRANZ		X
21 **	STC-ITT		X
22 **	CASMOS (GEC style)		X
23	Siliconix		X
24 **	GE-Intersil advanced		X
25 **	CASMOS (Rutherford)		X
26 **	Sierra 2		X

Level	MOSFET Model Description	All Platforms including PC	All Platforms except PC
27	SOSFET		X
28	BSIM derivative; Avant! proprietary model	X	
29 ***	not used	–	–
30 ***	VTI		X
31***	Motorola		X
32 ***	AMD		X
33 ***	National Semiconductor		X
34*	(EPFL) not used		X
35 **	Siemens		X
36 ***	Sharp		X
37 ***	TI		X
38	IDS: Cypress depletion model		X
39	BSIM2	X	
41	TI Analog	X	
46 ***	SGS-Thomson MOS LEVEL 3		X
47	BSIM3 Version 2.0		X
49	BSIM3 Version 3 (Enhanced)	X	
50	Philips MOS9	X	
53	BSIM3 Version 3 (Berkeley)	X	
54	UC Berkeley BSIM4 Model	X	
55	EPFL-EKV Model Ver 2.6, R 11	X	
57	UC Berkeley BSIM3-SOI MOSFET Model Ver 2.0.1	X	

Level	MOSFET Model Description	All Platforms including PC	All Platforms except PC
58	University of Florida SOI Model Ver 4.5 (Beta-98.4)	X	
59	UC Berkeley BSIM3-501 FD Model	X	
61	RPI a-Si TFT Model	X	
62	RPI Poli-Si TFT Model	X	

* not officially released
** equations are proprietary – documentation not provided
*** requires a license and equations are proprietary – documentation not provided

Selecting MOSFET Capacitors

The MOSFET capacitance model parameter, CAPOP, is associated with the MOS model. Depending on the value of CAPOP, different capacitor models are used to model the MOS gate capacitance, that is, the gate-to-drain capacitance, the gate-to-source capacitance, and the gate-to-bulk capacitance. CAPOP allows for the selection of several versions of the Meyer and charge conservation model.

Some of the capacitor models are tied to specific DC models; they are stated as such. Others are for general use by any DC model.

CAPOP=0	SPICE original Meyer model (general)
CAPOP=1	Modified Meyer model (general)
CAPOP=2	Parameterized modified Meyer model (general default)
CAPOP=3	Parameterized Modified Meyer model with Simpson integration (general)
CAPOP=4	Charge conservation model (analytic), LEVELs 2, 3, 6, 7, 13, 28, and 39 only

CAPOP=5	No capacitor model
CAPOP=6	AMI capacitor model (LEVEL 5)
CAPOP=9	Charge conservation model (LEVEL 3)
CAPOP=13	Generic BSIM model (Default for 13, 28, 39)
CAPOP=11	Ward-Dutton model specialized (LEVEL 2)
CAPOP=12	Ward-Dutton model specialized (LEVEL 3)
CAPOP=39	BSIM2 Capacitance Model (LEVEL 39)

CAPOP=4 selects the recommended charge-conserving model (from among CAPOP=11, 12, or 13) for the given DC model.

Table 8-1: CAPOP=4 Selections

MOS Level	Default CAPOP	CAPOP=4 selects:
2	2	11
3	2	12
13, 28, 39	13	13
others	2	11

LEVELs 49 and 53 use the Berkeley capacitance-model parameter CAPMOD. The proprietary models, as well as LEVELs 5, 17, 21, 22, 25, 27, 31, 33, 49, 53, 55, and 58 have their own built-in capacitance routines.

Selecting MOS Diodes

The model parameter ACM (Area Calculation Method), which controls the geometry of the source and drain diffusions, selects the modeling of the bulk-to-source and bulk-to-drain diodes of the MOSFET model. The diode model includes the diffusion resistance, capacitance, and DC currents to the substrate.

ACM=0	SPICE model, parameters determined by element areas
ACM=1	ASPEC model, parameters function of element width
ACM=2	Avant! model, combination of ACM=0,1 and provisions for lightly doped drain technology
ACM=3	Extension of ACM=2 model that deals with stacked devices (shared source/drains) and source/drain periphery capacitance along gate edge.

Searching Models as Function of W, L

Model parameters are often the same for MOSFETs having width and length dimensions within specific ranges. To take advantage of this, create a MOSFET model for a specific range of width and length. These MOSFET model parameters help the simulator to select the appropriate model for the given width and length.

The automatic model selection program searches a data file for a MOSFET model with the width and length range specified in the MOSFET element statement. This model statement is then used in the simulation.

To search a data file for MOSFET models within a given range of width and length, provide a root extension for the model reference name (in the .MODEL statement). Also, use the model geometric range parameters LMIN, LMAX, WMIN, and WMAX. These model parameters give the range of the physical length and width dimensions to which the MOSFET model applies. For example, if the model reference name in the element statement is NCH, the model selection program examines the models with the same root model reference name NCH such as NCH.1, NCH.2 or NCH.A. The model selection program selects the first MOSFET model statement whose geometric range

parameters include the width and length specified in the associated MOSFET element statement.

The following example shows how to call the MOSFET model selection program from a data file. The model selector program examines the .MODEL statements that have the model reference names with root extensions NCHAN.2, NCHAN.3, NCHY.20, and NCHY.50.

Example

```
*FILE: SELECTOR.SP TEST OF MOS MODEL SELECTOR
.OPTION LIST WL SCALE=1U SCALM=1U NOMOD
.OP
V1 1 0 5
V2 2 0 4
V3 3 0 1
V4 4 0 -1
M1 1 2 3 4 NCHAN 10 2
M2 1 2 3 4 NCHAN 10 3
M3 1 2 3 4 NCH 10 4
M4 1 2 3 4 NCHX 10 5
M5 1 2 3 4 NCHY 20 5
M6 1 2 3 4 NCHY 50 5
$$$$$$$ FOR CHANNEL LENGTH SELECTION
.MODEL NCHAN.2 NMOS LEVEL=2 VTO=2.0 UO=800 TOX=500 NSUB=1E15
+    RD=10 RS=10 CAPOP=5
+    LMIN=1 LMAX=2.5 WMIN=2 WMAX=15
.MODEL NCHAN.3 NMOS LEVEL=2 VTO=2.2 UO=800 TOX=500 NSUB=1E15
+    RD=10 RS=10 CAPOP=5
+    LMIN=2.5 LMAX=3.5 WMIN=2 WMAX=15
$$$$$$$ NO SELECTION FOR CHANNEL LENGTH AND WIDTH
.MODEL NCH NMOS LEVEL=2 VTO=2.3 UO=800 TOX=500 NSUB=1E15
+    RD=10 RS=10 CAPOP=5
$+   LMIN=3.5 LMAX=4.5 WMIN=2 WMAX=15
.MODEL NCHX NMOS LEVEL=2 VTO=2.4 UO=800 TOX=500 NSUB=1E15
+    RD=10 RS=10 CAPOP=5
$+   LMIN=4.5 LMAX=100 WMIN=2 WMAX=15
$$$$$$$ FOR CHANNEL WIDTH SELECTION
.MODEL NCHY.20 NMOS LEVEL=2 VTO=2.5 UO=800 TOX=500 NSUB=1E15
+    RD=10 RS=10 CAPOP=5
+    LMIN=4.5 LMAX=100 WMIN=15 WMAX=30
.MODEL NCHY.50 NMOS LEVEL=2 VTO=2.5 UO=800 TOX=500 NSUB=1E15
+    RD=10 RS=10 CAPOP=5
```

```
+    LMIN=4.5 LMAX=100 WMIN=30 WMAX=500
.END
```

Setting MOSFET Control Options

Specific control options (set in the .OPTIONS statement) used for MOSFET models include the following. For flag-type options, 0 is unset (off) and 1 is set (on).

ASPEC	This option uses ASPEC MOSFET model defaults and set units. Default=0.
BYPASS	This option avoids recomputation of nonlinear functions that do not change with iterations. Default=1.
MBYPAS	BYPASS tolerance multiplier. Default=1.
DEFAD	Default drain diode area. Default=0.
DEFAS	Default source diode area. Default=0.
DEFL	Default channel length. Default=$1e^{-4}$m.
DEFW	Default channel width. Default=$1e^{-4}$m.
DEFNRD	Default number of squares for drain resistor. Default=0.
DEFNRS	Default number of squares for source resistor. Default=0.
DEFPD	Default drain diode periphery. Default=0.
DEFPS	Default source diode periphery. Default=0.
GMIN	Pn junction parallel transient conductance. Default=$1e^{-12}$mho.
GMINDC	Pn junction parallel DC conductance. Default=$1e^{-12}$mho.
SCALE	Element scaling factor. Default=1.
SCALM	Model scaling factor. Default=1.

WL This option changes the order of specifying MOS element VSIZE from the default order, length-width, to width-length. Default=0.

Override the defaults DEFAD, DEFAS, DEFL, DEFNRD, DEFNRS, DEFPD, DEFPS, and DEFW in the MOSFET element statement by specifying AD, AS, L, NRD, NRS, PD, PS, and W, respectively.

Scaling Units

Units are controlled by the options SCALE and SCALM. SCALE scales element statement parameters, and SCALM scales model statement parameters. SCALM also affects the MOSFET gate capacitance and diode model parameters. In this chapter, scaling applies only to those parameters specified as scaled. If SCALM is specified as a parameter in a .MODEL statement, it overrides the option SCALM. In this way, models using different values of SCALM can be used in the same simulation. MOSFET parameter scaling follows the same rules as for other model parameters, for example:

Table 8-2: Model Parameter Scaling

Parameter Units	Parameter Value
meter	multiplied by SCALM
$meter^2$	multiplied by $SCALM^2$
$meter^{-1}$	divided by SCALM
$meter^{-2}$	divided by $SCALM^2$

Override global model size scaling for individual MOSFET, diode, and BJT models that uses the .OPTION SCALM=<*val*> statement by including SCALM=<*val*> in the .MODEL statement. .OPTION SCALM=<*val*> applies globally for JFETs, resistors, transmission lines, and all models other than MOSFET, diode, and BJT models, and cannot be overridden in the model.

Scaling for LEVEL 25 and 33

When using the proprietary LEVEL 25 (Rutherford CASMOS) or LEVEL 33 (National) models, the SCALE and SCALM options are automatically set to 1e-6. If you use these models together with other scalable models, however, set the options, SCALE=1e-6 and SCALM=1e-6, explicitly.

Bypassing Latent Devices

Use the BYPASS (latency) option to decrease simulation time in large designs. It speeds simulation time by not recalculating currents, capacitances, and conductances if the voltages at the terminal device nodes have not changed. The BYPASS option applies to MOSFETs, MESFETs, JFETs, BJTs, and diodes. Use .OPTION BYPASS to set BYPASS.

BYPASS can result in a reduction in accuracy of the simulation for tightly coupled circuits such as op-amps, high gain ring oscillators, and so on. Use .OPTION MBYPAS to set MBYPAS to a smaller value to improve the accuracy of the results.

General MOSFET Model Statement

Following is the syntax for all model specifications. All related parameter levels are covered in their respective sections.

Syntax

```
.MODEL mname [PMOS | NMOS] (<LEVEL=val> <keyname1=val1>
+ <keyname2=val2>…) <VERSION=version_number>
```

or

```
.MODEL mname NMOS(<LEVEL = val> <keyname1 = val1>
+ <keyname2=val2>…) <VERSION=version_number> …)
```

mname	Model name. Elements refer to the model by this name.
PMOS	Identifies a p-channel MOSFET model
NMOS	Identifies an n-channel MOSFET model
LEVEL	The MOSFET model includes several device model types. Use the LEVEL parameter for selection. Default=1.0.
VERSION	This parameter specifies the version number of the model, for LEVEL=13 BSIM and LEVEL=39 BSIM2 models only. See the .MODEL statement description for information about the effects of the VERSION parameter.

Example

```
.MODEL MODP PMOS LEVEL=7 VTO=-3.25 GAMMA=1.0)
.MODEL MODN NMOS LEVEL=2 VTO=1.85 TOX=735e-10)
.MODEL MODN NMOS LEVEL=39 TOX=2.0e-02 TEMP=2.5e+01
   VERSION=95.1
```

Nonplanar and Planar Technologies

Two MOSFET fabrication technologies have dominated integrated circuit design: nonplanar and planar technologies. Nonplanar technology uses metal gates. The simplicity of the process generally provides acceptable yields. The primary problem with metal gates is metal breakage across the field oxide steps. Field oxide is grown by oxidizing the silicon surface. When the surface is cut, it forms a sharp edge. Since metal must be affixed to these edges in order to contact the diffusion or make a gate, it is necessary to apply thicker metal to compensate for the sharp edges. This metal tends to gather in the cuts, making etching difficult. The inability to accurately control the metal width necessitates very conservative design rules and results in low transistor gains.

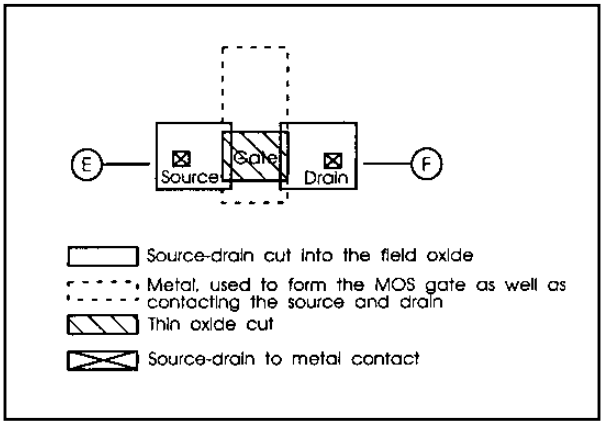
In planar technology, the oxide edges are smooth, with a minimal variance in metal thickness. Shifting to nitride was accomplished by using polysilicon gates. Adding a chemical reactor to the MOS fabrication process enables not only the deposition of silicon nitride, but also that of silicon oxide and polysilicon. The ion implanter is the key element in this processing, using implanters with beam currents greater than 10 milliamperes.

Because implanters define threshold voltages and “diffusions” as well as field thresholds, processes require a minimum number of high temperature oven steps. This enables low temperature processing and maskless pattern generation. The new wave processes are more similar to the older nonplanar metal gate technologies.

Using Field Effect Transistors

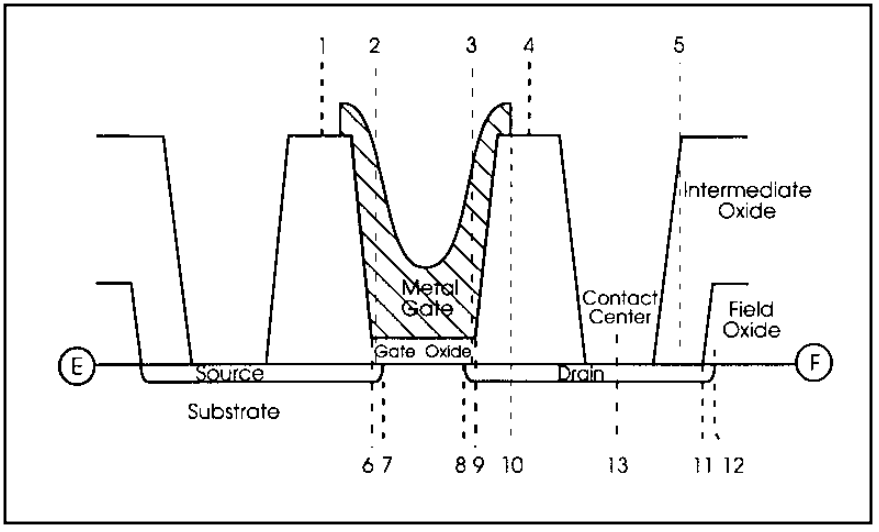
The metal gate MOSFET is nonisoplanar as shown in Figure 8-1 and Figure 8-2.

Figure 8-1: Field Effect Transistor



Looking at the actual geometry, from source-to-drain, Figure 8-2 shows a perspective of the nonisoplanar MOSFET.

Figure 8-2: Field Effect Transistor Geometry



1 - 4	Drawn metal gate channel length
2 - 3	Drawn oxide cut
7 - 8	Effective channel length
6 - 9	Etched channel length
8 - 9	Lateral diffusion
5	Drawn diffusion edge
11	Actual diffusion edge

To visualize the construction of the silicon gate MOSFET, observe how a source or drain to field cuts (Figure 8-3.) The cut A-B shows a drain contact (Figure 8-4).

Figure 8-3: Isoplanar Silicon Gate Transistor

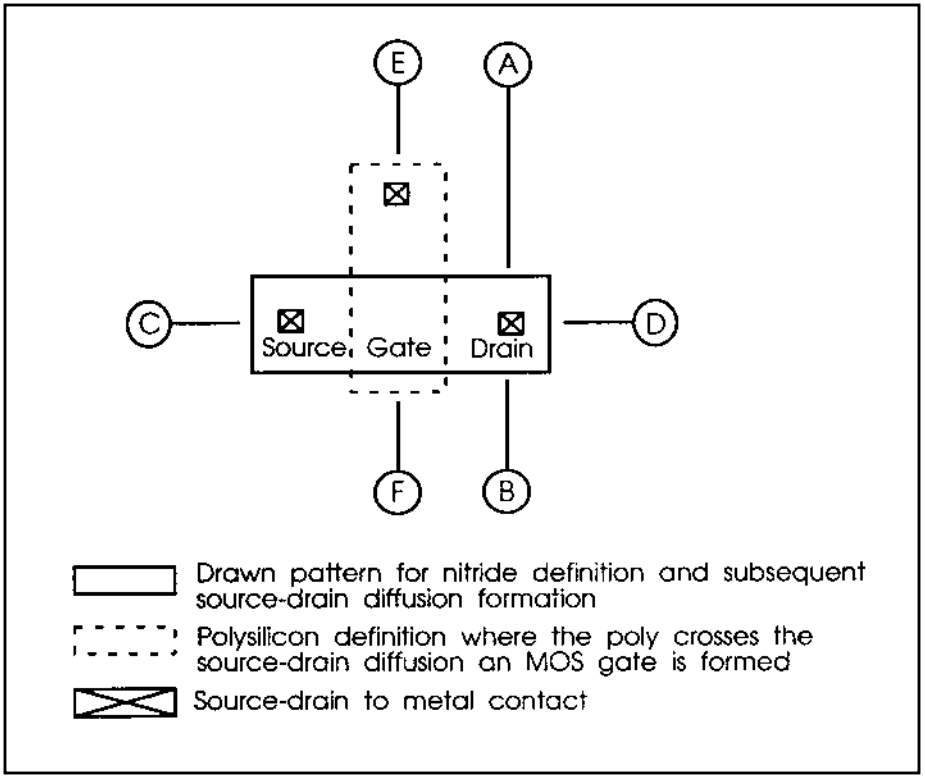
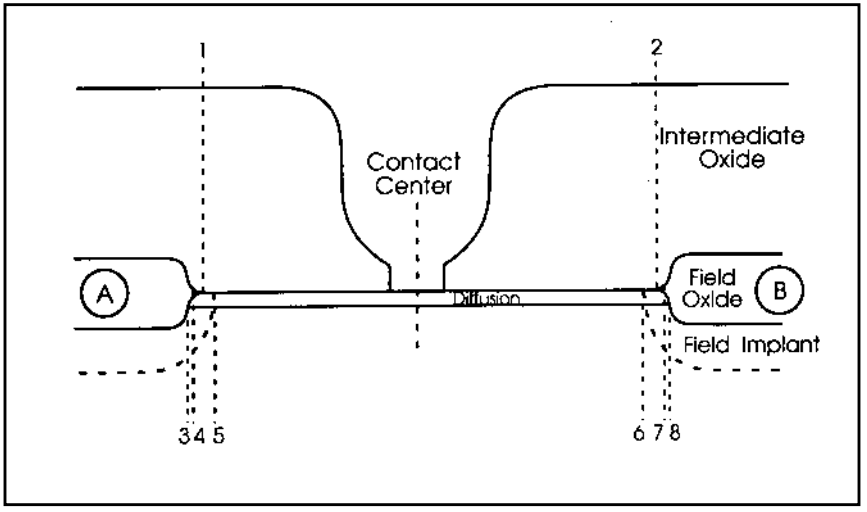


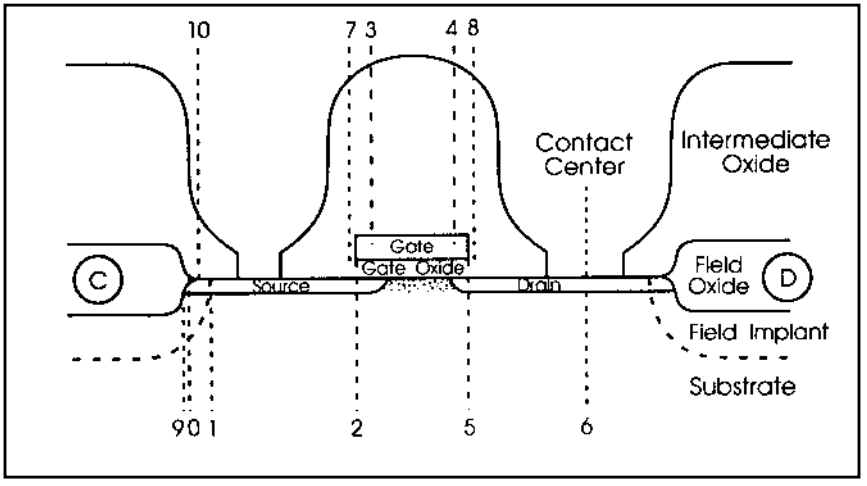
Figure 8-4: Isoplanar MOSFET Construction, Part A



1 - 2	Diffusion drawn dimension for nitride
4 - 7	Nitride layer width after etch
3 - 1	Periphery of the diode

The cut from the source to the drain is represented by C - D (Figure 8-5), which includes the contacts.

Figure 8-5: Isoplanar MOSFET Construction, Part B

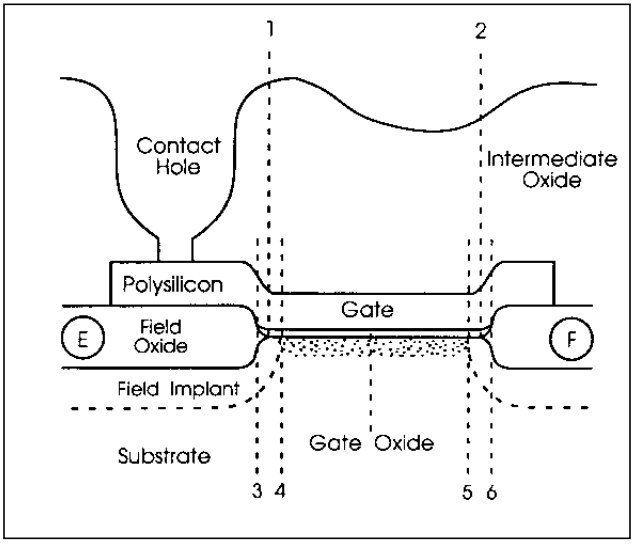


7 - 8	Drawn channel length L
2 - 5	Actual poly width after etching L + XL where XL<0
3 - 4	Effective channel length after diffusion L + XL - LD
4 - 5	Lateral diffusion LD
9 - 10	Diffusion periphery for diode calculations
5-6	Gate edge to center contact for ACM=1 and ACM=2 calculations

The planar process produces parasitic capacitances at the poly to field edges of the device. The cut along the width of the device demonstrates the importance of these parasitics (Figure 8-6).

The encroachment of the field implant into the channel not only narrows the channel width, but also increases the gate to bulk parasitic capacitance.

Figure 8-6: Isoplanar MOSFET, Width Cut



1 - 2	Drawn width of the gate W
3 - 4	Depleted or accumulated channel (parameter WD)
4 - 5	Effective channel width W+ XW -2 WD
3 - 6	Physical channel width W + XW

MOSFET Equivalent Circuits

Equation Variables

This section lists the equation variables and constants.

Table 8-3: Equation Variables and Constants

Variable/ Quantity	Definition
cbd	Bulk-to-drain capacitance
cbs	Bulk-to-source capacitance
cbg	Gate-to-bulk capacitance
cgd	Gate-to-drain capacitance
cgs	Gate-to-source capacitance
f	Frequency
gbd	Bulk-to-drain dynamic conductance
gbs	Bulk-to source dynamic conductance
gds	Drain-to-source dynamic conductance controlled by vds
gdb	Drain-to bulk impact ionization conductance
gm	Drain-to-source dynamic transconductance controlled by vgs
gmbs	Drain-to-source dynamic bulk transconductance controlled by vsb
ibd	Bulk-to-drain DC current
ibs	Bulk-to-source DC current
ids	Drain-to-source DC current

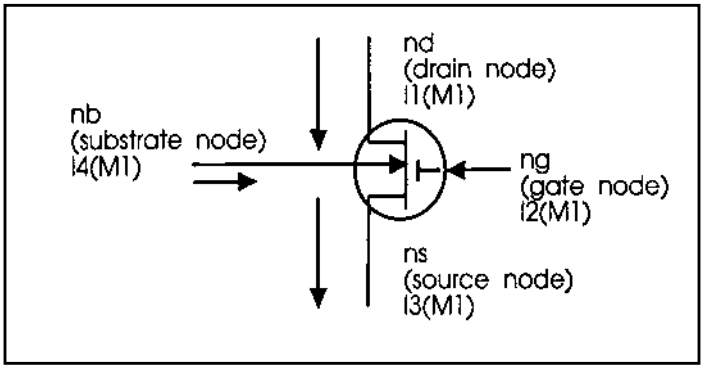
Table 8-3: Equation Variables and Constants

Variable/ Quantity	Definition
idb	Drain-to-bulk impact ionization current
ind	Drain-to-source equivalent noise circuit
inrd	Drain resistor equivalent noise circuit
inrs	Source resistor equivalent noise circuit
rd	Drain resistance
rs	Source resistance
vsb	Source-to-bulk voltage
vds	Drain-to-source voltage
vgs	Gate-to-source voltage
Δt	t-tnom
εsi	1.0359e-10F/m dielectric constant of silicon
k	1.38062e-23 (Boltzmann's constant)
q	1.60212e-19 (electron charge)
t	New temperature of model or element in °K
tnom	tnom = TNOM + 273.15. This variable represents the nominal temperature of parameter measurements in °K (user input in °C).
vt	k · t/q
vt(tnom)	k · tnom/q

Using the MOSFET Current Convention

Figure 8-7 shows the assumed direction of current flow through a MOS transistor. When printing the drain current, use either I(M1) or I1(M1) syntax. I2 produces the gate current, I3 produces the source current, and I4 produces the substrate current. References to bulk are the same as references to the substrate.

Figure 8-7: MOSFET Current Convention, N-channel



Using MOSFET Equivalent Circuits

Simulators use three equivalent circuits to analyze MOSFETs:

- DC
- Transient,
- AC and noise-equivalent circuits.

The components of these circuits form the basis for all element and model equation discussion. The equivalent circuit for DC sweep is the same as the one used for transient analysis, except capacitances are not included. Figures 8-8 through Figure 8-10 display the MOSFET equivalent circuits.

The fundamental component in the equivalent circuit is the DC drain-to-source current (ids). For the noise and AC analyses, the actual ids current is not used. Instead, the model uses the partial derivatives of ids with respect to the terminal voltages vgs, vds, and vbs. The names for these partial derivatives are as follows.

Transconductance

$$gm = \frac{\partial(ids)}{\partial(vgs)}$$

Conductance

$$gds = \frac{\partial(ids)}{\partial(vds)}$$

Bulk Transconductance

$$gmbs = \frac{\partial(ids)}{\partial(vbs)}$$

The ids equation describes the basic DC effects of the MOSFET. The effects of gate capacitance and of source and drain diodes are considered separately from the DC ids equations. In addition, the impact ionization equations are treated separately from the DC ids equation, even though its effects are added to ids.

Figure 8-8: Equivalent Circuit, MOSFET Transient Analysis

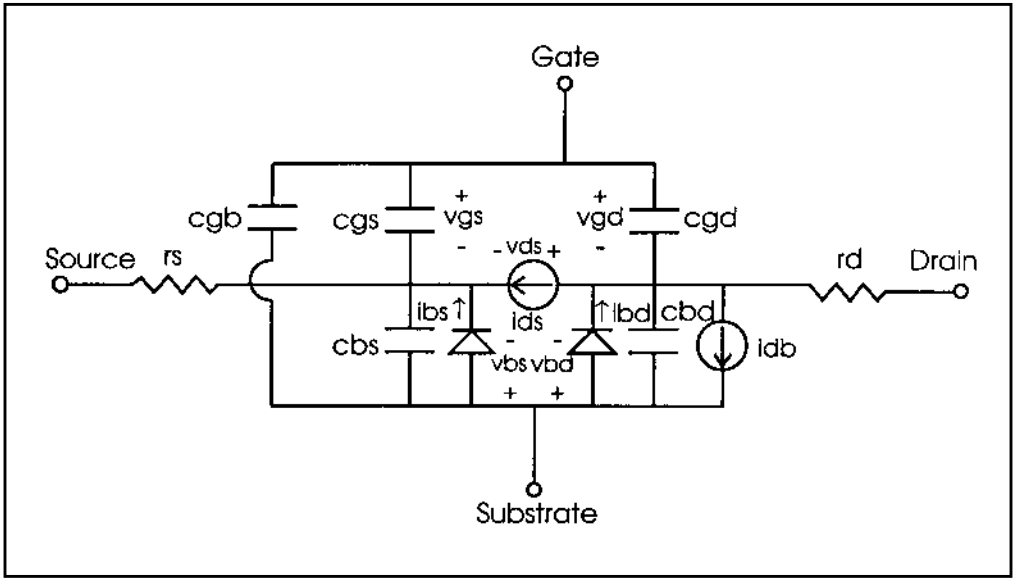


Figure 8-9: Equivalent Circuit, MOSFET AC Analysis

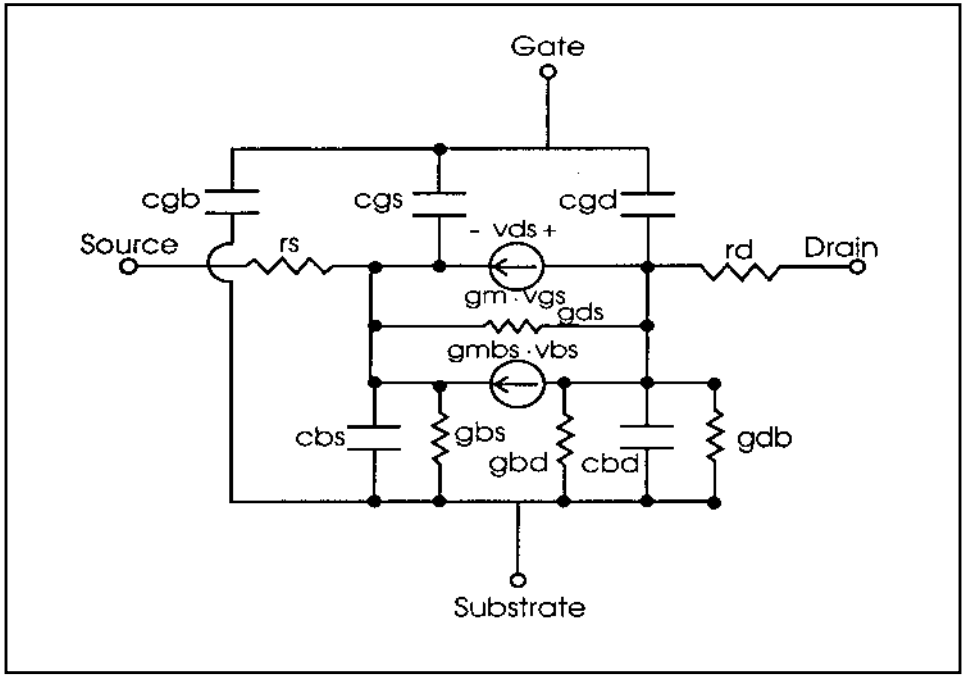
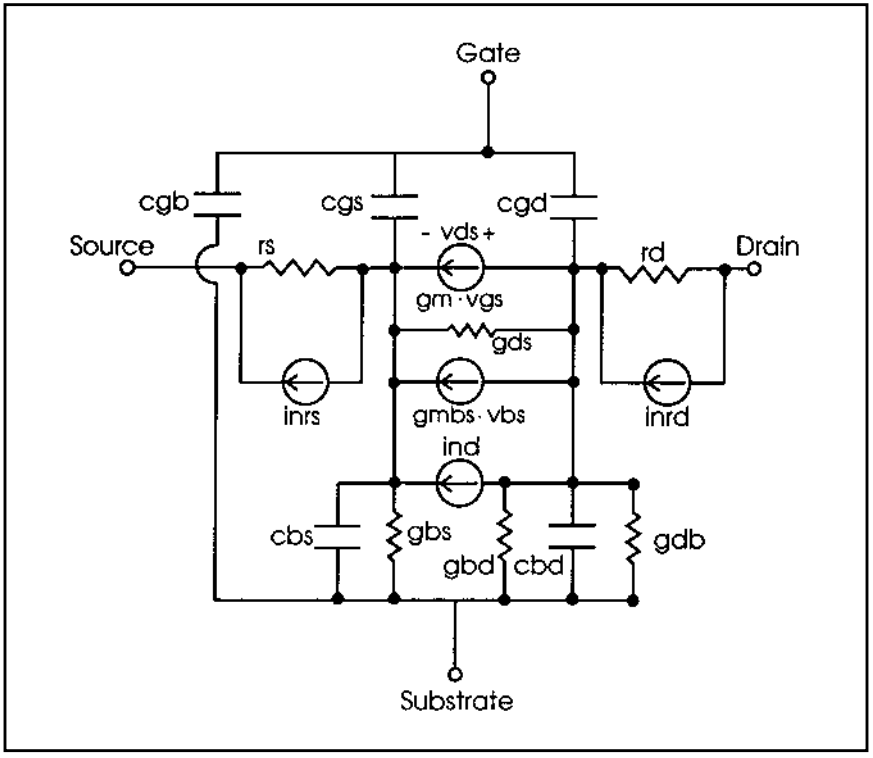


Figure 8-10: Equivalent Circuit, MOSFET AC Noise Analysis



MOSFET Diode Models

The Area Calculation Method (ACM) parameter allows for the precise control of modeling bulk-to-source and bulk-to-drain diodes within MOSFET models. The ACM model parameter is used to select one of three different modeling schemes for the MOSFET bulk diodes. This section discusses the model parameters and model equations used for the different MOSFET diode models.

Selecting MOSFET Diode Models

To select a MOSFET diode model, set the ACM parameter within the MOSFET model statements. If ACM=0, the pn bulk junctions of the MOSFET are modeled in the SPICE-style. The ACM=1 diode model is the original ASPEC model. The ACM=2 model parameter specifies the improved diode model, which is based on a model similar to the ASPEC MOSFET diode model. The ACM=3 diode model is a further improvement that deals with capacitances of shared sources and drains and gate edge source/drain-to-bulk periphery capacitance. If the ACM model parameter is not set, the diode model defaults to the ACM=0 model. ACM=0 and ACM=1 models do not permit the specification of HDIF. ACM=0 does not permit specification of LDIF. Furthermore, the geometric element parameters AD, AS, PD, and PS are not used for the ACM=1 model.

Enhancing Convergence

The GMIN and GMINDC options parallel a conductance across the bulk diodes and drain-source for transient and DC analysis, respectively. Use these options to enhance the convergence properties of the diode model, especially when the model has a high off resistance. Use the parameters RSH, RS, and RD to keep the diode from being overdriven in either a DC or transient forward bias condition. These parameters also enhance the convergence properties of the diode model.

Using MOSFET Diode Model Parameters

This section describes the diode model parameters for MOSFET.

DC Model Parameters

Name (Alias)	Units	Default	Description
ACM		0	Area calculation method
JS	amp/m^2	0	Bulk junction saturation current JSscaled = JS/$SCALM^2$ – for ACM=1, unit is amp/m and JSscaled = JS/SCALM.
JSW	amp/m	0	Sidewall bulk junction saturation current JSWscaled = JSW/SCALM.
IS	amp	1e-14	Bulk junction saturation current. For the option ASPEC=1, default=0.
N		1	Emission coefficient
NDS		1	Reverse bias slope coefficient
VNDS	V	-1	Reverse diode current transition point

Using Capacitance Model Parameters

Name (Alias)	Units	Default	Description
CBD	F	0	Zero bias bulk-drain junction capacitance. Used only when CJ and CJSW are 0.
CBS	F	0	Zero bias bulk-source junction capacitance. Used only when CJ and CJSW are 0.

Name (Alias)	Units	Default	Description
CJ (CDB, CSB, CJA)	F/m^2	579.11 $\mu F/m^2$	Zero-bias bulk junction capacitance: CJscaled = $CJ/SCALM^2$ For ACM=1 the unit is F/m and CJscaled = CJ/SCALM Default for option ASPEC=0 is: $CJ = \left(\frac{\varepsilon si \cdot q \cdot NSUB}{2 \cdot PB}\right)^{1/2}$
CJSW (CJP)	F/m	0	Zero-bias sidewall bulk junction capacitance CJSWscaled = CJSW/SCALM Default = 0
CJGATE	F/m	CSJW	Zero-bias gate-edge sidewall bulk junction capacitance (ACM=3 only) CJGATEscaled=CJGATE/SCALM Default = CJSW for Hspice releases later than H9007D. Default = 0 for HSPICE releases H9007D and earlier, or if CJSW is not specified.
FC		0.5	Forward-bias depletion capacitance coefficient (not used)
MJ (EXA, EXJ, EXS, EXD)		0.5	Bulk junction grading coefficient
MJSW (EXP)		0.33	Bulk sidewall junction grading coefficient
NSUB (DNB, NB)	$1/cm^3$	1.0e15	Substrate doping

Name (Alias)	Units	Default	Description
PB (PHA, PHS, PHD)	V	0.8	Bulk junction contact potential
PHP	V	PB	Bulk sidewall junction contact potential
TT	s	0	Transit time

Using Drain and Source Resistance Model Parameters

Name (Alias)	Units	Default	Description
RD	ohm/sq	0.0	Drain ohmic resistance. This parameter is usually lightly doped regions' sheet resistance for ACM 1.
RDC	ohm	0.0	Additional drain resistance due to contact resistance
LRD	ohm/m	0	Drain resistance length sensitivity. Use this parameter with automatic model selection in conjunction with WRD and PRD to factor model for device size.
WRD	ohm/m	0	Drain resistance length sensitivity (used with LRD)
PRD	ohm/m^2	0	Drain resistance product (area) sensitivity (used with LRD)
RS	ohm/sq	0.0	Source ohmic resistance. This parameter is usually lightly doped regions' sheet resistance for ACM 1.

Name (Alias)	Units	Default	Description
LRS	ohm/m	0	Source resistance length sensitivity. Use this parameter with automatic model selection in conjunction with WRS and PRS to factor model for device size.
WRS	ohm/m	0	Source resistance width sensitivity (used with LRS)
PRS	ohm/m^2	0	Source resistance product (area) sensitivity (used with LRS)
RSC	ohm	0.0	Additional source resistance due to contact resistance
RSH (RL)	ohm/sq	0.0	Drain and source diffusion sheet resistance

Using MOS Geometry Model Parameters

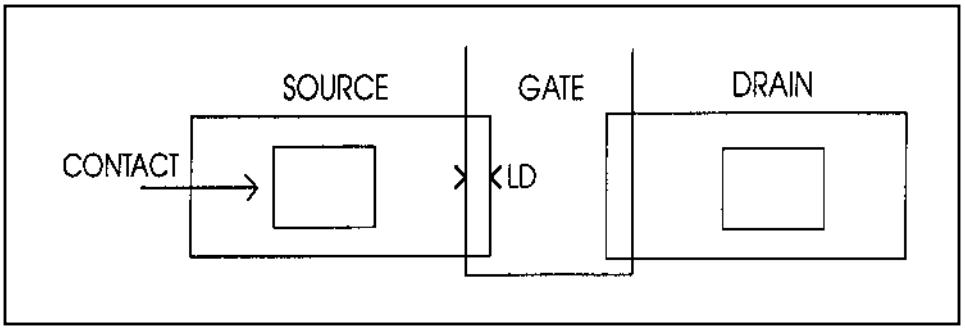
Name (Alias)	Units	Default	Description
HDIF	m	0	Length of heavily doped diffusion, from contact to lightly doped region (ACM=2, 3 only) HDIFwscaled = HDIF · SCALM

Name (Alias)	Units	Default	Description
LD (DLAT,LATD)	m		Lateral diffusion into channel from source and drain diffusion. If LD and XJ are unspecified, LD default=0.0. When LD is unspecified, but XJ is specified, LD is calculated from XJ. LD default=0.75 · XJ. For LEVEL 4 only, lateral diffusion is derived from LD · XJ. LDscaled = LD · SCALM
LDIF	m	0	Length of lightly doped diffusion adjacent to gate (ACM=1, 2) LDIFscaled = LDIF · SCALM
WMLT		1	Width diffusion layer shrink reduction factor
XJ	m	0	Metallurgical junction depth XJscaled = XJ · SCALM
XW (WDEL, DW)	m	0	Accounts for masking and etching effects XWscaled = XW · SCALM

Using an ACM=0 MOS Diode

Figure 8-11 shows the parameter value settings for a MOSFET diode, designed with a MOSFET that has a channel length of 3 µm and a channel width of 10 µm.

Figure 8-11: ACM=0 MOS Diode



Example

Consider a transistor with:

```
LD=.5µm    W=10µm    L=3µm
```

AD	area of drain (about 80 pm^2)
AS	area of source (about 80 pm^2)
CJ	4e-4 F/m^2
CJSW	1e-10 F/m
JS	1e-8 A/m^2
JSW	1e-13 A/m
NRD	number of squares for drain resistance
NRS	number of squares for source resistance
PD	sidewall of drain (about 36 µm)
PS	sidewall of source (about 36 µm)

Calculating Effective Areas and Peripheries

For ACM=0, the effective areas and peripheries are calculated as:

$$ADeff = M \cdot AD \cdot WMLT^2 \cdot SCALE^2$$
$$ASeff = M \cdot AS \cdot WMLT^2 \cdot SCALE^2$$
$$PDeff = M \cdot PD \cdot WMLT \cdot SCALE$$
$$PSeff = M \cdot PS \cdot WMLT \cdot SCALE$$

Calculating Effective Saturation Current

For ACM=0, the MOS diode effective saturation currents are calculated as:

Source Diode Saturation Current

Define:

$$val = JSscaled \cdot ASeff + JSWscaled \cdot PSeff$$

If val > 0 then,

$$isbs = val$$

Otherwise,

$$isbd = M \cdot IS$$

Drain Diode Saturation Current

Define:

$$val = JSscaled \cdot ADeff + JSWscaled \cdot PDeff$$

If val > 0 then,

$$isbd = val$$

Otherwise,

$$isbd = M \cdot IS$$

Calculating Effective Drain and Source Resistances

For ACM=0, the effective drain and source resistances are calculated as:

Source Resistance

Define:

$$val = NRS \cdot RSH$$

If val > 0 then,

$$RSeff = \frac{val + RSC}{M}$$

Otherwise:

$$RSeff = \frac{RS + RSC}{M}$$

Drain Resistance

Define:

$$val = NRD \cdot RSH$$

If val > then,

$$RDeff = \frac{val + RDC}{M}$$

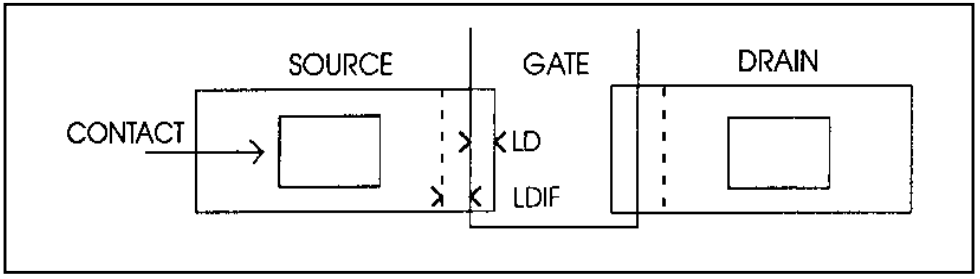
Otherwise:

$$RDeff = \frac{RD + RDC}{M}$$

Using an ACM=1 MOS Diode

Simulation uses ASPEC-style diodes when you specify the ACM=1 model parameter. The AD, PD, AS, and PS parameters are not used, and the JS and CJ units differ from the SPICE style diodes (ACM=0).

Figure 8-12: ACM=1 MOS Diode



Example

The listings below are typical parameter value settings for a transistor with: LD=0.5 µm W=10 µm L=3 µm LDIF=0.5 µm

CJ	1e-10 F/m of gate width
	Note the change from F/m^2 (in ACM=0) to F/m.
CJSW	2e-10 F/m of gate width
JS	1e-14 A/m of gate width
	Note the change from A/m^2 (in ACM=0) to A/m
JSW	1e-13 A/m of gate width
NRD	number of squares for drain resistance
NRS	number of squares for source resistance

Calculating Effective Areas and Peripheries

For ACM=1, the effective areas and peripheries are calculated as follows:

$$ADeff = Weff \cdot WMLT$$
$$ASeff = Weff \cdot WMLT$$
$$PDff = Weff$$
$$PSeff = Weff$$

where:

$$Weff = M \cdot (Wscaled \cdot WMLT + XWscaled)$$

Note: The Weff is not quite the same as the weff given in the models LEVEL 1, 2, 3, 6, and 13 sections. The term $2 \cdot WDscaled$ is not subtracted.

Calculating Effective Saturation Current

For ACM=1, the MOS diode effective saturation currents are calculated as follows:

Source Diode Saturation Current

Define:

$$val = JSscaled \cdot ASeff + JSWscaled \cdot PSeff$$

If val > 0 then,

$$isbs = val$$

Otherwise:

$$isbs = M \cdot IS$$

Drain Diode Saturation Current

Define:

$$val = JSscaled \cdot ADeff + JSWscaled \cdot PDeff$$

If val > 0 then,

$$isbd = val$$

Otherwise,

$$isbd = M \cdot IS$$

Calculating Effective Drain and Source Resistances

For ACM=1, the effective drain and source resistances are calculated as follows:

Source Resistance

For UPDATE=0,

$$RSeff = \frac{LDscaled + LDIFscaled}{Weff} \cdot RS + \frac{NRS \cdot RSH + RSC}{M}$$

If UPDATE ≥ 1 and LDIF=0 and the ASPEC option is also specified then:

$$RSeff = \frac{1}{M} \cdot (RS + NRS \cdot RSH + RSC)$$

Drain Resistance

For UPDATE=0:

$$RDeff = \frac{LDscaled + LDIFscaled}{Weff} \cdot RD + \frac{NRD \cdot RSH + RDC}{M}$$

If UPDATE ≥ 1 and LDIF=0 and the ASPEC option is also specified then:

$$RDeff = \frac{1}{M} \cdot (RD + NRD \cdot RSH + RDC)$$

Note: See LEVELs 6 and 7 for more possibilities.

Using an ACM=2 MOS Diode

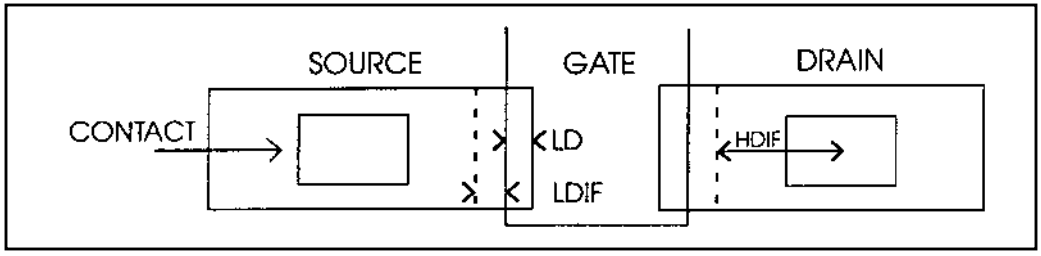
Simulation uses HSPICE style MOS diodes when you specify theACM=2 model parameter. This allows a fold-back calculation scheme similar to the ASPEC method, retaining full model-parameter compatibility with the SPICE procedure. This method also supports both lightly and heavily doped diffusions (by setting the LD, LDIF, and HDIF parameters). The JS, JSW, CJ, and CJSW units, used in SPICE are preserved, permitting full compatibility.

ACM=2 automatically generates more reasonable diode parameter values than those for ACM=1. The ACM=2 geometry can be generated one of two ways:

- Element parameters: AD, AS, PD, and PS can be used for parasitic generation when specified in the element statement. Default options values for these parameters are not applicable.
- If the diode is to be suppressed, set IS=0, AD=0, and AS=0.

The source diode is suppressed if AS=0 is set in the element and IS=0 is set in the model. This setting is useful for shared contacts.

Figure 8-13: ACM=2 MOS Diode



Example

Transistor with LD=0.07μm W=10 μm L=2 μm LDIF=1 μm HDIF= 4 μm, typical MOSFET diode parameter values are:

AD	Area of drain. Default option value for AD is not applicable.
AS	Area of source. Default option value for AS is not applicable.
CJ	1e-4 F/m^2
CJSW	1e-10 F/m
JS	1e-4 A/m^2
JSW	1e-10 A/m
HDIF	Length of heavy doped diffusion contact to gate (about 2 μm)
	HDIFeff=HDIF · WMLT · SCALM
LDIF+LD	Length of lightly doped diffusion (about 0.4μm)
NRD	Number of squares drain resistance. Default option value for NRD is not applicable.
NRS	Number of squares source resistance. Default option value for NRS is not applicable.
PD	Periphery of drain, including gate width for ACM=2. No default.
PS	Periphery of source, including gate width for ACM=2. No default.
RD	Resistance (ohm/square) of lightly doped drain diffusion (about 2000)
RS	Resistance (ohm/square) of lightly doped source diffusion (about 2000)
RSH	Diffusion sheet resistance (about 35)

Calculating Effective Areas and Peripheries

For ACM=2, the effective areas and peripheries are calculated as:

If AD is not specified then,

$$ADeff = 2 \cdot HDIFeff \cdot Weff$$

Otherwise,

$$ADeff = M \cdot AD \cdot WMLT^2 \cdot SCALE^2$$

If AS is not specified then,

$$ASeff = 2 \cdot HDIFscaled \cdot Weff$$

Otherwise,

$$ASeff = M \cdot AS \cdot WMLT^2 \cdot SCALE^2$$

If PD is not specified then,

$$PDeff = 4 \cdot HDIFeff + 2 \cdot Weff$$

Otherwise,

$$PDeff = M \cdot PD \cdot WMLT \cdot SCALE$$

If PS is not specified then,

$$PSeff = 4 \cdot HDIFeff + 2 \cdot Weff$$

Otherwise:

$$PSeff = M \cdot PS \cdot WMLT \cdot SCALE$$

where:

$$Weff = M \cdot (Wscaled \cdot WMLT + XWscaled)$$

$$HDIFeff = HDIFscaled$$

$$HDIFscaled = HDIF \cdot SCALM \cdot WMLT$$

Note: The Weff is not quite the same as the Weff given in the model LEVEL 1, 2, 3, and 6 sections. The term $2 \cdot WDscaled$ is not subtracted.

Calculating Effective Saturation Currents

For ACM=2, the MOS diode effective saturation currents are calculated as:

Source Diode Saturation Current

Define:

$$val = JSscaled \cdot ASeff + JSWscaled \cdot PSeff$$

If val > 0 then,

$$isbs = val$$

Otherwise:

$$isbs = M \cdot IS$$

Drain Diode Saturation Current

Define:

$$val = JSscaled \cdot ADeff + JSWscaled \cdot PDeff$$

If val > 0 then,

$$isbd = val$$

Otherwise:

$$isbd = M \cdot IS$$

Calculating Effective Drain and Source Resistances

For ACM=2, the effective drain and source resistances are calculated as:

Source Resistance

If NRS is specified then,

$$RSeff = \frac{LDscaled + LDIFscaled}{Weff} \cdot RS + \left(\frac{NRS \cdot RSH + RSC}{M}\right)$$

Otherwise:

$$RSeff = \frac{RSC}{M} + \frac{HDIFeff \cdot RSH + (LDscaled + LDIFscaled) \cdot RS}{Weff}$$

Drain Resistance

If NRD is specified then,

$$RDeff = \frac{LDscaled + LDIFscaled}{Weff} \cdot RD + \left(\frac{NRD \cdot RSH + RDC}{M}\right)$$

Otherwise:

$$RDeff = \frac{RDC}{M} + \frac{HDIFeff \cdot RSH + (LDscaled + LDIFscaled) \cdot RD}{Weff}$$

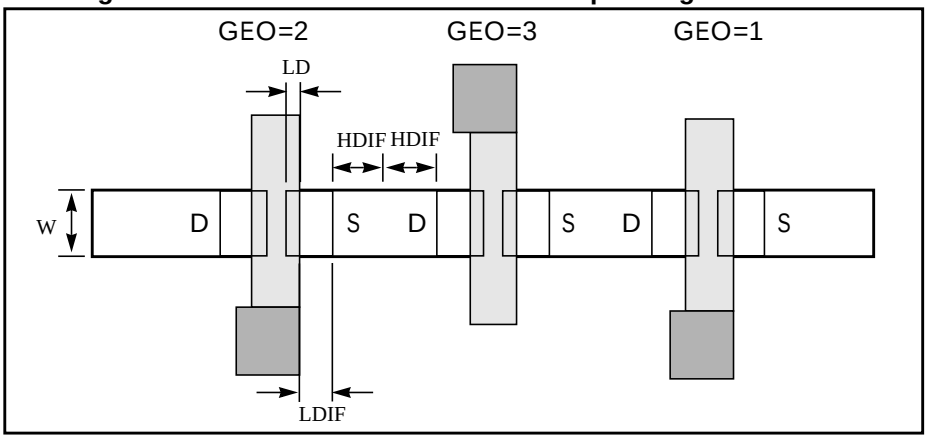
Using an ACM=3 MOS Diode

Use ACM=3 to model MOS diodes of the stacked devices properly. In addition, the CJGATE model parameter separately models the drain and source periphery capacitances along the gate edge. Therefore, the PD and PS calculations do not include the gate periphery length. CJGATE defaults to CJSW, which, in turn, defaults to 0.

The AD, AS, PD, PS calculations depend on the layout of the device, which is determined by the value of element parameter GEO. The GEO can be specified on the MOS element description. It can have the following values:

- GEO=0: indicates the drain and source of the device are not shared by other devices (default).
- GEO=1: indicates the drain is shared with another device.
- GEO=2: indicates the source is shared with another device.
- GEO=3: indicates the drain and source are shared with another device.

Figure 8-14: Stacked Devices and Corresponding GEO Values



Calculating Effective Areas and Peripheries

For ACM=3, the effective areas and peripheries are calculated differently, depending on the value of GEO.

If AD is not specified, then,

For GEO=0 or 2,

$$ADeff = 2 \cdot HDIFeff \cdot Weff$$

For GEO=1 or 3,

$$ADeff = HDIFeff \cdot Weff$$

Otherwise:

$$ADeff = M \cdot AD \cdot WMLT^2 \cdot SCALE^2$$

If AS is not specified, then,

For GEO=0 or 1,

$$ASeff = 2 \cdot HDIFeff \cdot Weff$$

For GEO=2 or 3,

$$ASeff = HDIFeff \cdot Weff$$

Otherwise:

$$ASeff = M \cdot AS \cdot WMLT^2 \cdot SCALE^2$$

If PD is not specified, then,

For GEO=0 or 2,

$$PDeff = 4 \cdot HDIFeff + Weff$$

For GEO=1 or 3,

$$PDeff = 2 \cdot HDIFeff$$

Otherwise:

$$PDeff = M \cdot PD \cdot WMLT \cdot SCALE$$

If PS is not specified, then,

For GEO=0 or 1,

$$PSeff = 4 \cdot HDIFeff + Weff$$

For GEO=2 or 3,

$$PSeff = 2 \cdot HDIFeff$$

Otherwise:

$$PSeff = M \cdot PS \cdot WMLT \cdot SCALE$$

The Weff and HDIFeff is calculated as follows:

$$Weff = M \cdot (Wscaled \cdot WMLT + XWscaled)$$

$$HDIFeff = HDIFscaled \cdot WMLT$$

Note: The Weff is not quite the same as the Weff given in the model LEVEL 1, 2, 3, and 6 sections. The term $2 \cdot WDscaled$ is not subtracted.

Effective Saturation Current Calculations

The ACM=3 model calculates the MOS diode effective saturation currents the same as ACM=2.

Effective Drain and Source Resistances

The ACM=3 model calculates the effective drain and source resistances the same as ACM=2.

MOS Diode Equations

This section describes the MOS diode equations.

DC Current

The drain and source MOS diodes are paralleled with GMINDC conductance in the DC analysis and with GMIN in the transient analysis. The total DC current is the sum of diode current and the conductance current. The diode current is calculated as follows.

Drain and Source Diodes Forward Biased

vbs > 0,

$$ibs = isbs \cdot (e^{vbs/(N \cdot vt)} - 1)$$

vbd > 0,

$$ibd = isbd \cdot (e^{vbd/(N \cdot vt)} - 1)$$

Drain and Source Diodes Reverse Biased

For 0>vbs>VNDS,

$$ibs = gsbs \cdot vbs$$

For vbs < VNDS,

$$bs = gsbs \cdot VNDS + \left(\frac{gsbs}{NDS}\right) \cdot (vbs - VNDS)$$

For 0 > vbd > VNDS,

$$ibd = gsbd \cdot vbd$$

For vbd < VNDS,

$$ibd = gsbd \cdot VNDS + \left(\frac{gsbd}{NDS}\right) \cdot (vbd - VNDS)$$

where

$$|gsbs| = |isbs|, \text{ and } |gdbd| = |isbd|$$

Using MOS Diode Capacitance Equations

Each MOS diode capacitance is the sum of diffusion and depletion capacitance. The diffusion capacitance is evaluated in terms of the small signal conductance of the diode and a model parameter TT, representing the transit time of the diode. The depletion capacitance depends on the choice of ACM, and is discussed below.

Calculate the bias-dependent depletion capacitance by defining the intermediate quantities: C0BS, C0BD, C0BS_SW, and C0BD_SW, which depend on geometric parameters, such as ASeff and PSeff calculated under various ACM specifications.

When ACM=3, the intermediate quantities C0BS_SW, and C0BD_SW include an extra term to account for CJGATE.

For ACM=2, the parameter CJGATE has been added in a backward compatible manner. Therefore, the default behavior of CJGATE makes the intermediate quantities C0BS_SW and C0BD_SW the same as for previous versions. The default patterns are:

- If neither CJSW nor CJGATE is specified, both default to zero.
- If CJGATE is not specified, it defaults to CJSW, which in turn defaults to zero.
- If CJGATE is specified, and CJSW is not specified, then CJSW defaults to zero.

The intermediate quantities C0BS, C0BS_SW, C0BD, and C0BD_SW are calculated as follows.

```
C0BS = CJscaled*ASeff
C0BD = CJscaled*ADeff
```

If (ACM= 0 or 1), then:

```
C0BS_SW = CJSWscaled*PSeff
C0BD_SW = CJSWscaled*PDeff
```

If (ACM=2):

If (PSeff < Weff), then:

```
C0BS_SW = CJGATEscaled*PSeff
```

Otherwise:

```
C0BS_SW = CJSWscaled*(PSeff-Weff) + CJGATEscaled*Weff
```

If (PDeff < Weff), then:

```
C0BD_SW = CJGATEscaled*PDeff
```

Otherwise:

```
C0BD_SW = CJSWscaled*(PDeff-Weff) + CJGATEscaled*Weff
```

If (ACM=3), then:

```
C0BS_SW = CJSWscaled*PSeff + CJGATEscaled*Weff
C0BD_SW = CJSWscaled*PDeff + CJGATEscaled*Weff
```

Source Diode Capacitance

If (C0BS + C0BS_SW) > 0, then:

For vbs < 0,

$$\text{capbs} = \text{TT} \cdot \frac{\partial \text{ibs}}{\partial \text{vbs}} + \text{C0BS} \cdot \left(1 - \frac{\text{vbs}}{\text{PB}}\right)^{-\text{MJ}}$$

$$+ \text{C0BS\_SW} \cdot \left(1 - \frac{\text{vbs}}{\text{PHP}}\right)^{-\text{MJSW}}$$

For vbs > 0,

$$capbs = TT \cdot \frac{\partial ibs}{\partial vbs} + C0BS \cdot \left(1 + MJ \cdot \frac{vbs}{PB}\right) + C0BS\_SW \cdot \left(1 + MJSW \cdot \frac{vbs}{PHP}\right)$$

Otherwise, if (C0BS + C0BS_SW) ≤ 0, then:

For vbs < 0,

$$capbs = TT \cdot \frac{\partial ibs}{\partial vbs} + M \cdot CBS \cdot \left(1 - \frac{vbs}{PB}\right)^{-MJ}$$

For vbs > 0,

$$capbs = TT \cdot \frac{\partial ibs}{\partial vbs} + M \cdot CBS \cdot \left(1 + MJ \cdot \frac{vbs}{PB}\right)$$

Drain Diode Capacitance

If (C0BD + C0BD_SW) > 0, then:

For vbd < 0,

$$capbd = TT \cdot \frac{\partial ibd}{\partial vbd} + C0BD \cdot \left(1 - \frac{vbd}{PB}\right)^{-MJ} + PDeff \cdot C0BD\_SW \cdot \left(1 - \frac{vbd}{PHP}\right)^{-MJSW}$$

For vbd > 0,

$$capbd = TT \cdot \frac{\partial ibd}{\partial vbd} + C0BD \cdot \left(1 + MJ \cdot \frac{vbd}{PB}\right) + C0BD\_SW \cdot \left(1 + MJSW \cdot \frac{vbd}{PHP}\right)$$

Otherwise, if (ADeff · CJscaled + PDeff · CJSWscaled) ≤ 0, then:

For vbd < 0,

$$\text{capbd} = \text{TT} \cdot \frac{\partial \text{ibd}}{\partial \text{vbd}} + \text{M} \cdot \text{CBD} \cdot \left(1 - \frac{\text{vbd}}{\text{PB}}\right)^{-\text{MJ}}$$

For vbd > 0,

$$\text{capbd} = \text{TT} \cdot \frac{\partial \text{ibd}}{\partial \text{vbd}} + \text{M} \cdot \text{CBD} \cdot \left(1 + \text{MJ} \cdot \frac{\text{vbd}}{\text{PB}}\right)$$

Common Threshold Voltage Equations

This section describes the common threshold voltage equations.

Common Threshold Voltage Parameters

The parameters described in this section are applicable to all MOSFET models except LEVELs 5 and 13.

Name (Alias)	Units	Default	Description
DELVTO	V	0.0	Zero-bias threshold voltage shift
GAMMA	$V^{1/2}$	0.527625	Body effect factor. If GAMMA is not set, it is calculated from NSUB.
NGATE	$1/cm^3$		Polysilicon gate doping, used for analytical model only. Undoped polysilicon is represented by a small value. If NGATE ≤ 0.0, it is set to 1e+18.
NSS	$1/cm^2$	1.0	Surface state density
NSUB (DNB, NB)	$1/cm^3$	1e15	Substrate doping
PHI	V	0.576036	Surface potential. NSUB default=1e15.

Name (Alias)	Units	Default	Description
TPG (TPS)		1.0	Type of gate material, used for analytical model only LEVEL 4 TPG default=0 where TPG = 0 al-gate TPG = 1 gate type same as source-drain diffusion TPG = -1 fate type opposite to source-drain diffusion
VTO (VT)	V		Zero-bias threshold voltage

Calculating PHI, GAMMA, and VTO

The model parameters PHI, GAMMA, and VTO are used in threshold voltage calculations. If these parameters are not user-specified, they are calculated as follows, except for the LEVEL 5 model.

If PHI is not specified, then,

$$PHI = 2 \cdot vt \cdot \ln\left(\frac{NSUB}{ni}\right)$$

If GAMMA is not specified, then,

$$GAMMA = \frac{(2 \cdot q \cdot \varepsilon si \cdot NSUB)^{1/2}}{COX}$$

The energy gap, eg, and intrinsic carrier concentration for the above equations are determined by:

$$eg = 1.16 - 7.02e\text{-}4 \cdot \frac{tnom^2}{tnom + 1108}$$

$$ni = 1.45e{+}10 \cdot \left(\frac{tnom}{300}\right)^{3/2} \cdot e^{\left[\frac{q \cdot eg}{2 \cdot k} \cdot \left(\frac{1}{300} - \frac{1}{tnom}\right)\right]} (1/cm^3)$$

where,

$$tnom = TNOM + 273.15$$

If VTO is not specified, then for Al-Gate (TPG=0), the work function Φms is determined by:

$$\Phi ms = -\frac{eg}{2} - type \cdot \frac{PHI}{2} - 0.05$$

where type is +1 for n-channel and -1 for p-channel.

For Poly-Gate (TPG=±1), the work function is determined by:

If the model parameter NGATE is not specified,

$$\Phi ms = type \cdot \left(- TPG \cdot \frac{eg}{2} - \frac{PHI}{2} \right)$$

Otherwise,

$$\Phi ms = type \cdot \left[- TPG \cdot vt \cdot \ln\left(\frac{NGATE}{ni} \right) - \frac{PHI}{2} \right]$$

Then VTO voltage is determined by:

$$VTO = vfb + type \cdot (GAMMA \cdot PHI^{1/2} + PHI)$$

where,

$$vfb = \Phi ms - \frac{q \cdot NSS}{COX} + DELVTO$$

If VTO is specified, then,

$$VTO = VTO + DELVTO$$

MOSFET Impact Ionization

The impact ionization current for MOSFETs is available for all levels. The controlling parameters are ALPHA, VCR, and IIRAT. The parameter IIRAT sets the fraction of the impact ionization current that goes to the source.

$$I_{ds} = I_{ds\_}\texttt{normal} + \texttt{IIRAT}\cdot\texttt{I\_impact}$$

$$I_{db} = I_{db\_}\texttt{diode} + \texttt{(1-IIRAT)}\cdot\texttt{I\_impact}$$

IIRAT defaults to zero, which sends all impact ionization current to bulk. Leave IIRAT at its default value unless data is available for both drain and bulk current.

Using Impact Ionization Model Parameters

Name (Alias)	Units	Default	Description
ALPHA	1/V	0.0	Impact ionization current coefficient
LALPHA	µm/V	0.0	ALPHA length sensitivity
WALPHA	µm/V	0.0	ALPHA width sensitivity
VCR	V	0.0	Critical voltage
LVCR	µm V	0.0	VCR length sensitivity
WVCR	µm V	0.0	VCR width sensitivity
IIRAT		0.0	Portion of impact ionization current that goes to source

Calculating the Impact Ionization Equations

The current I_impact due to impact ionization effect is calculated as follows:

$$\text{I\_impact} = \text{Ids} \cdot \text{ALPHAeff} \cdot (\text{vds} - \text{vdsat}) \cdot e^{\frac{-\text{VCReff}}{\text{vds} - \text{vdsat}}}$$

where:

$$ALPHAeff = ALPHA + LALPHA \cdot 1e\text{-}6 \cdot \left(\frac{1}{Leff} - \frac{1}{LREFeff}\right) + WALPHA \cdot 1e\text{-}6 \cdot \left(\frac{1}{Weff} - \frac{1}{WREFeff}\right)$$

$$VCReff = VCR + LVCR \cdot 1e\text{-}6 \cdot \left(\frac{1}{Leff} - \frac{1}{LREFeff}\right) + WVCR \cdot 1e\text{-}6 \cdot \left(\frac{1}{Weff} - \frac{1}{WREFeff}\right)$$

where:

$$LREFeff = LREF + XLREF - 2 \cdot LD \text{ and}$$

$$WREFeff = WREF + XWREF - 2 \cdot WD$$

Calculating Effective Output Conductance

The element template output allows *gds* to be output directly, for example:

```
.PRINT I(M1) gds=LX8(M1)
```

When using impact ionization current, it is important to note that gds is the derivative of I_{ds} only, rather than the total drain current, which is I_{ds}+I_{db}. The complete drain output conductance is:

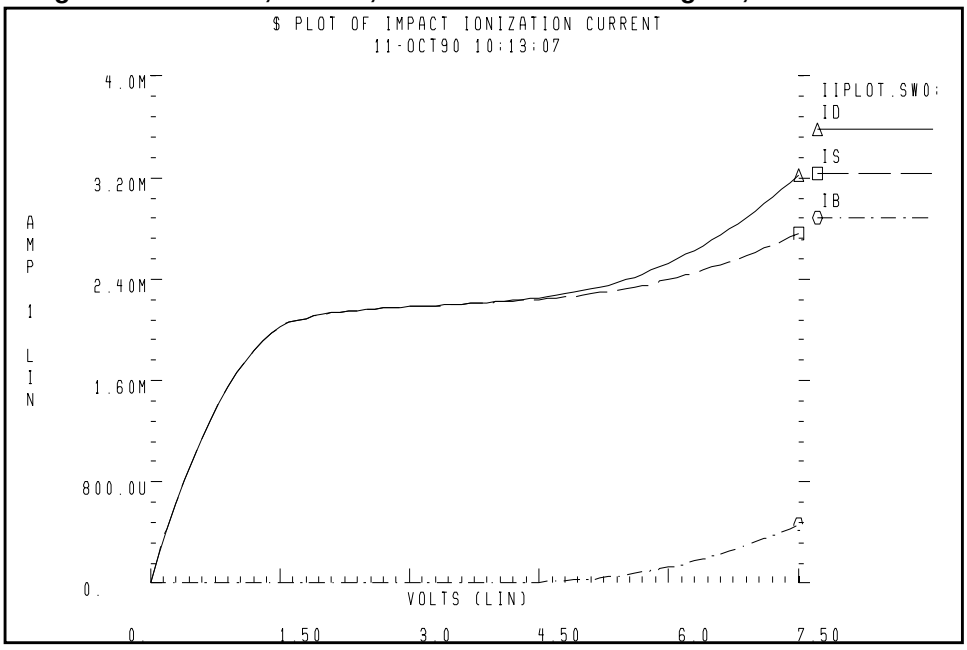
$$g_{dd} = \frac{\partial I_d}{\partial V_d} = \frac{\partial I_{ds}}{\partial V_{ds}} + \frac{\partial I_{db}}{\partial V_{db}} = \frac{\partial I_{ds}}{\partial V_{ds}} + \frac{\partial I_{bd}}{\partial V_{bd}} = g_{ds} + g_{bd}$$

$$G_{dd} = LX8 + LX10$$

For example, to print the drain output resistance of device M1:

```
.PRINT rout=PAR('1.0/(LX8(M1)+LX10(M1))')
```

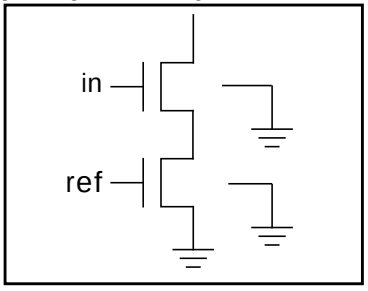
Figure 8-15: Drain, Source, and Bulk Currents for vgs=3, with IIRAT=0.5



Cascoding Example

Drain-to-bulk impact ionization current limits the use of cascoding to increase output impedance. The following cascode example shows the effect of changing IIRAT. When IIRAT is less than 1.0, the drain-to-bulk current lowers the output impedance of the cascode stage.

Figure 8-16: Low-frequency AC Analysis Measuring Output Impedance



Cascode Circuit

Example

```
iirat      gout_ac       rout
0.0       8.86E-6       113 K
0.5       4.30E-6       233 K
1.0       5.31E-8       18.8 Meg
```

Input File

```
$ cascode test
.param pvds=5.0 pvref=1.4 pvin=3.0

vdd dd 0 pvds ac 1
$ current monitor vd
vd dd d 0
vin in 0 pvin
vref ref 0 pvref
x1 d in ref cascode
.macro cascode out in ref
m1 out in 1 0   n L=1u W=10u
mref 1 ref 0 0   n L=1u W=10u
.eom

.param xiirat=0
.ac dec 2 100k 1x sweep xiirat poi 3   0, 0.5, 1.0
.print ir(vd)
.measure gout_ac avg ir(vd)

.model n nmos level=3
+ tox=200 vto=0.8 gamma=0.7 uo=600 kappa=0.05
+ alpha=1 vcr=15 iirat=xiirat
.end
```

MOS Gate Capacitance Models

You can use capacitance model parameters with all MOSFET model statements.

Model charge storage using fixed and nonlinear gate capacitances and junction capacitances. Gate-to-drain, gate-to-source, and gate-to-bulk overlap capacitances are represented by three fixed-capacitance parameters: CGDO, CGSO, and CGBO. The algorithm used for calculating nonlinear, voltage-dependent MOS gate capacitance depends on the value of model parameter CAPOP.

Model MOS gate capacitances, as a nonlinear function of terminal voltages, using Meyer's piecewise linear model for all MOS levels. The charge conservation model is also available for MOSFET model LEVELs 2 through 7, 13, and 27. For LEVEL 1, the model parameter TOX must be specified to invoke the Meyer model. The Meyer, Modified Meyer, and Charge Conservation MOS Gate Capacitance models are described in detail in the following subsections.

Some of the charge conserving models (Ward-Dutton or BSIM) can cause "*timestep too small*" errors when no other nodal capacitances are present.

Selecting Capacitor Models

Gate capacitance model selection has been expanded to allow various combinations of capacitor models and DC models. Older DC models can now be incrementally updated with the new capacitance equations without having to move to a new DC model. You can select the gate capacitance with the CAPOP model parameter to validate the effects of different capacitance models.

The capacitance model selection parameter CAPOP is associated with the MOS models. Depending on the value of CAPOP, different capacitor models are used to model the MOS gate capacitance: the gate-to-drain capacitance, the gate-to-source capacitance, or the gate-to-bulk capacitance. CAPOP allows for the selection of several versions of the Meyer and charge conservation model.

Some of the capacitor models are tied to specific DC models (DC model level in parentheses below). Other models are designated as general and can be used by any DC model.

CAPOP=0	SPICE original Meyer model (general)
CAPOP=1	Modified Meyer model (general)
CAPOP=2	Parameterized Modified Meyer model (general default)
CAPOP=3	Parameterized Modified Meyer model with Simpson integration (general)
CAPOP=4	Charge conservation model (analytic), LEVELs 2, 3, 6, 7, 13, 28, and 39 only
CAPOP=5	No capacitor model
CAPOP=6	AMI capacitor model (LEVEL 5)
CAPOP=9	Charge conservation model (LEVEL 3)
CAPOP=13	Generic BSIM model (default for LEVELs 13, 28, 39)
CAPOP=11	Ward-Dutton model (specialized, LEVEL 2)
CAPOP=12	Ward-Dutton model (specialized, LEVEL 3)
CAPOP=39	BSIM2 Capacitance model (LEVEL 39)

CAPOP=4 selects the recommended charge-conserving model from among CAPOP=11, 12, or 13 for the given DC model.

Table 8-4: CAPOP = 4 Selections

MOS Level	Default CAPOP	CAPOP=4 selects
2	2	11
3	2	12
13, 28, 39	13	13
Other levels	2	11

The proprietary models, LEVEL 5, 17, 21, 22, 25, 31, 33, and the SOS model LEVEL 27 have their own built-in capacitance routines.

Introducing Transcapacitance

If you have a capacitor with two terminals, 1 and 2 with charges Q1 and Q2 on the two terminals that sum to zero, for example, Q1=-Q2, the charge is a function of the voltage difference between the terminals, V12=V1-V2. The small-signal characteristics of the device are completely described by one quantity, C=dQ1/dV12.

If you have a four-terminal capacitor, the charges on the four terminals must sum to zero (Q1+Q2+Q3+Q4=0), and they can only depend on voltage differences, but they are otherwise arbitrary functions. So there are three independent charges, Q1, Q2, Q3, that are functions of three independent voltages V14, V24, V34. Hence there are nine derivatives needed to describe the small-signal characteristics.

It is convenient to consider the four charges separately as functions of the four terminal voltages, Q1(V1,V2,V3,V4), ... Q4(V1,V2,V3,V4). The derivatives form a four by four matrix, dQi/dVj, i=1,.4, j=1,.4. This matrix has a direct interpretation in terms of AC measurements. If an AC voltage signal is applied to terminal j with the other terminals AC grounded, and AC current into terminal i is measured, the current is the imaginary constant times 2*pi*frequency times dQi/dVj.

The fact that the charges sum to zero requires each column of this matrix to sum to zero, while the fact that the charges can only depend on voltage differences requires each row to sum to zero.

In general, the matrix is not symmetrical:

```
dQi/dVj need not equal dQj/dVi
```

This is not an expected event because it does not occur for the two terminal case. For two terminals, the constraint that rows and columns sum to zero.

$$\frac{dQ1}{dV1} + \frac{dQ2}{dV1} = 0 \qquad \frac{dQ1}{dV1} + \frac{dQ1}{dV2} = 0$$

forces dQ1/dV2 = dQ2/dV1. For three or more terminals, this relation does not hold in general.

The terminal input capacitances are the diagonal matrix entries

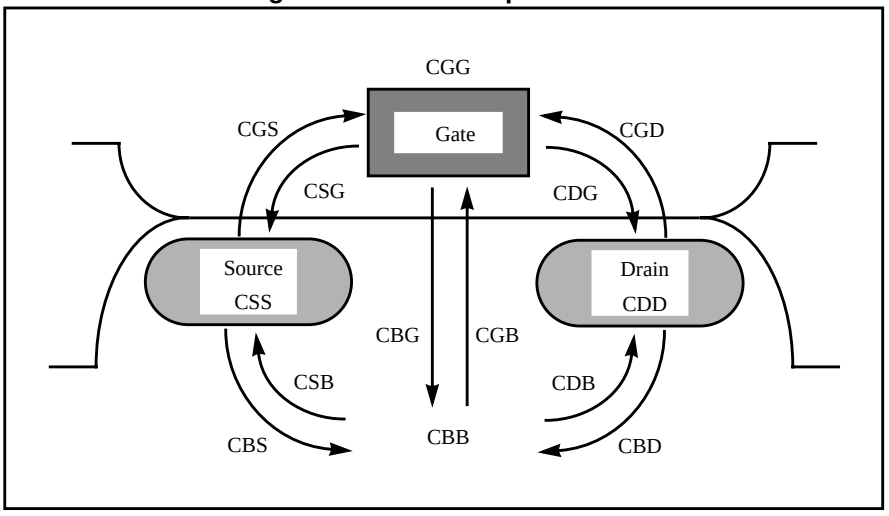
```
Cii = dQi/dVi     i=1,.4
```

and the transcapacitances are the negative of off-diagonal entries

```
Cij = -dQi/dVj     i not equal to j
```

All of the Cs are normally positive.

Figure 8-17: MOS Capacitances



In Figure 8-17, Cij determines the current transferred out of node i from a voltage change on node j. The arrows, representing direction of influence, point from node j to node i.

A MOS device with terminals D G S B provides:

$$CGG = \frac{dQg}{dVG}$$

$$CGD = -\frac{dQg}{dVD}$$

$$CDG = -\frac{dQD}{dVG}$$

CGG represents input capacitance: a change in gate voltage requires a current equal to CGGxdVG/dt into the gate terminal.

CGD represents Miller feedback: a change in drain voltage gives a current equal to CGGxdVG/dt out of the gate terminal.

CDG represents Miller feedthrough, capacitive current out of the drain due to a change in gate voltage.

To see how CGD might not be equal to CDG, the following example presents a simplified model with no bulk charge, with gate charge a function of VGS only, and 50/50 partition of channel charge into QS and QD:

$$QG = Q(vgs)$$

$$QS = -0.5 \cdot Q(vgs)$$

$$QD = -0.5 \cdot Q(vgs)$$

$$QB = 0$$

Consequently:

$$CGD = -\frac{dQG}{dVD} = 0$$

$$CDG = -\frac{dQD}{dVG} = 0.5 \cdot \frac{dQ}{dvgs}$$

Therefore, in this model there is Miller feedthrough, but no feedback.

Operating Point Capacitance Printout

Six capacitances are reported in the operating point printout:

cdtot	dQD/dVD
cgtot	dQG/dVG
cstot	dQS/dVS
cbtot	dQB/dVB
cgs	-dQG/dVS
cgd	-dQG/dVD

These capacitances include gate-drain, gate-source, and gate-bulk overlap capacitance, and drain-bulk and source-bulk diode capacitance. Drain and source refer to node 1 and 3 of the MOS element, that is, physical instead of electrical.

For the Meyer models, where the charges like QD are not well defined, the printout quantities are:

cdtot	cgd+cdb
cgtot	cgs+cgd+cgb
cstot	cgs+csb
cbtot	cgb+csb+cdb
cgs	cgs
cgd	cgd

Using the Element Template Printout

The MOS element template printouts for gate capacitance are LX18 – LX23 and LX32 – LX34. From these nine capacitances the complete four-by-four matrix of transcapacitances can be constructed. The nine LX printouts are:

```
LX18(m) = dQG/dVGB = CGGBO
LX19(m) = dQG/dVDB = CGDBO
LX20(m) = dQG/dVSB = CGSBO
LX21(m) = dQB/dVGB = CBGBO
LX22(m) = dQB/dVDB = CBDBO
LX23(m) = dQB/dVSB = CBSBO
LX32(m) = dQD/dVG = CDGBO
LX33(m) = dQD/dVD = CDDBO
LX34(m) = dQD/dVS = CDSBO
```

These capacitances include gate-drain, gate-source, and gate-bulk overlap capacitance, and drain-bulk and source-bulk diode capacitance. Drain and source refer to node 1 and 3 of the MOS element, that is, physical instead of electrical.

For an NMOS device with source and bulk grounded, LX18 represents the input capacitance, LX33 the output capacitance, -LX19 the Miller feedback capacitance (gate current induced by voltage signal on the drain), and -LX32 represents the Miller feedthrough capacitance (drain current induced by voltage signal on the gate).

A device operating with node 3 as electrical drain, for example an NMOS device with node 3 at higher voltage than node 1, is said to be in reverse mode. The LXs are physical, but you can translate them into electrical definitions by interchanging D and S:

```
CGG(reverse) = CGG = LX18
CDD(reverse) = CSS = dQS/dVS = d(-QG-QB-QD)/dVS =
   -LX20-LX23-LX34
CGD(reverse) = CGS = -LX20
CDG(reverse) = CSG = -dQS/dVG = d(QG+QB+QD)/dVG =
   LX18+LX21+LX32
```

For the Meyer models, the charges QD, and so forth, are not well defined. The formulas such as LX18= CGG, LX19= -CGD are still true, but the transcapacitances are symmetrical; for example, CGD=CDG. In terms of the six independent Meyer capacitances, cgd, cgs, cgb, cdb, csb, cds, the LX printouts are:

```
LX18(m) = CGS+CGD+CGB
LX19(m) = LX32(m) = -CGD
LX20(m) = -CGS
LX21(m) = -CGB
LX22(m) = -CDB
LX23(m) = -CSB
LX33(m) = CGD+CDB+CDS
LX34(m) = -CDS
```

Calculating Gate Capacitance

The following example shows a gate capacitance calculation in detail for a BSIM model. TOX is chosen so that:

$$\frac{eox}{tox} = 1e-3F/m^2$$

Vfb0, phi, k1 are chosen so that vth=1v. The AC sweep is chosen so that the last point is:

$$2 \cdot \pi \cdot freq = 1e6s^{-1}$$

Input File

```
$
m d g 0 b nch l=0.8u w=100u ad=200e-12 as=200e-12
vd d 0 5
vg g 0 5 ac 1
vb b 0 0
.ac dec 1 1.59155e4 1.59155e5
.print   CGG=lx18(m) CDD=lx33(m) CGD=par('-lx19(m)')
+ CDG=par('-lx32(m)')
.print   ig_imag=ii2(m) id_imag=ii1(m)
.model nch nmos level=13 update=2
+ xqc=0.6 toxm=345.315 vfb0=-1 phi0=1 k1=1.0 muz=600
+ mus=650 acm=2
+ xl=0 ld=0.1u meto=0.1u cj=0.5e-4 mj=0 cjsw=0
.alter
vd d 0 5 ac 1
vg g 0 5
.end
```

Calculations

$$\mathrm{Leff} = 0.6\mathrm{u}$$

$$\frac{\mathrm{eox}}{\mathrm{tox}} = 1\mathrm{e}-3\mathrm{F}/\mathrm{m}^2$$

$$\mathrm{Cap} = \frac{\mathrm{Leff}\cdot\mathrm{Weff}\cdot\mathrm{eox}}{\mathrm{tox}} = 60\mathrm{e}-15\mathrm{F}$$

BSIM equations for internal capacitance in saturation with xqc=0.4:

$$\mathrm{body} = 1 + 0.5\cdot\left(1 - \frac{1}{(1.744 + 0.8364\cdot(\mathrm{PHI0} + \mathrm{vsb}))}\right)\cdot\frac{\mathrm{K1}}{\sqrt{(\mathrm{PHI0} + \mathrm{vsb})}}$$

$$1 + 0.5\cdot\left(1 - \frac{1}{(1.744 + 0.8364)}\right) = 1.3062$$

$$\mathrm{cgg} = \mathrm{Cap}\cdot\left(1 - \frac{1}{(3\cdot\mathrm{body})}\right) = \mathrm{Cap}\cdot 0.7448 = 44.69\mathrm{F}$$

$$cgd = 0$$

$$cdg = \left(\frac{4}{15}\right) \cdot Cap = 16F$$

$$cdd = 0$$

$$\text{Gate-drain overlap} = (ld + meto) \cdot Weff \cdot \frac{eox}{tox} = 20e-15F$$

Adding the overlaps,

$$cgg = 44.69F + 2 \cdot 20F = 84.69F$$

$$cgd = 20F$$

$$cdg = 36F$$

$$cdd = 20F$$

$$\text{Drain-bulk diode cap } cj \cdot ad = (0.5e-4) \cdot (200e-12) = 1$$

Adding the diodes,

$$cgg = 84.69F$$

$$cgd = 20F$$

$$cdg = 36F$$

$$cdd = 30F$$

Results

```
subckt
element 0:m
model    0:nch
cdtot     30.0000f
cgtot     84.6886f
cstot     74.4684f
cbtot     51.8898f
cgs       61.2673f
cgd       20.0000f
freq       cgg         cdd        cgd        cdg
15.91550k 84.6886f    30.0000f 20.0000f   35.9999f
159.15500k 84.6886f    30.0000f   20.0000f 35.9999f
freq        ig_imag      id_imag
15.91550k   8.4689n     -3.6000n
159.15500k 84.6887n    -35.9999n
Alter results
freq      ig_imag        id_imag
15.91550k     -2.0000n    3.0000n
159.15500k   -20.0000n 30.0000n
```

The calculation and the simulation results match.

Plotting Gate Capacitances

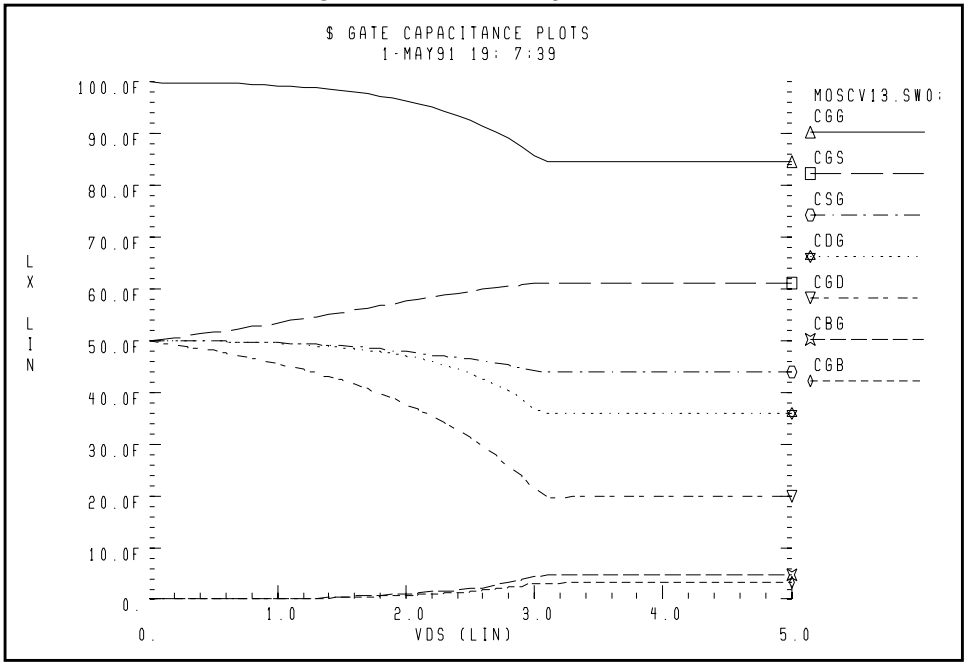
The following input file shows how to plot gate capacitances as a function of bias. Set the .OPTION DCCAP to turn on capacitance calculations for a DC sweep. The model used is the same as for the previous calculations.

Example

```
$ gate capacitance plots
.option dccap=1 post
m d g 0 b nch l=0.8u w=100u ad=200e-12 as=200e-12
vd d 0 0
vg g 0 5
vb b 0 0
.dc vd 0 5 .1
.print   vds=v(d) CGG=lx18(m)
+ CGD=par('-lx19(m)') CDG=par('-lx32(m)')
+ CGS=par('-lx20(m)') CSG=par('lx18(m)+lx21(m)+lx32(m)')
+ CGB=par('lx18(m)+lx19(m)+lx20(m)') CBG=par('-lx21(m)')

.model nch nmos
+ level=13 update=2 xqc=0.6 toxm=345.315
+ vfb0=-1 phi0=1 k1=1.0 muz=600 mus=650
+ acm=2 xl=0 ld=0.1u meto=0.1u
+ cj=0.5e-4 mj=0 cjsw=0
.end
```

Figure 8-18: Gate Capacitance



Using Capacitance Control Options

The control options affecting the CAPOP models are SCALM, CVTOL, DCSTEP, and DCCAP. SCALM scales the model parameters, CVTOL controls the error tolerance for convergence for the CAPOP=3 model (see ‘CAPOP=3 — Gate Capacitances (Simpson Integration)” on page 8-90). DCSTEP models capacitances with a conductance during DC analysis. DCCAP invokes calculation of capacitances in DC analysis.

Scaling

The parameters scaled by the option SCALM are CGBO, CGDO, CGSO, COX, LD, and WD. SCALM scales these parameters according to fixed rules that are a function of the parameter’s units. When the model parameter’s units are in meters, the parameter is multiplied by SCALM. For example, the parameter LD has units in meters, its scaled value is obtained by multiplying the value of LD by SCALM. When the units are in meters squared, the parameter is multiplied by $SCALM^2$. If the units are in reciprocal meters, the parameter’s value is divided by SCALM. For example, since CGBO is in farads/meter the value of CGBO is divided by SCALM. When the units are in reciprocal meters squared, then the parameter is divided by $SCALM^2$. The scaling equations specific to each CAPOP level are given in the individual CAPOP subsections.

MOS Gate Capacitance Model Parameters

Using Basic Gate Capacitance Parameters

Name (Alias)	Units	Default	Description
CAPOP		2.0	Capacitance model selector
COX (CO)	F/m2	3.453e-4	Oxide capacitance. If COX is not input, it is calculated from TOX. The default value corresponds to the TOX default of 1e-7: COXscaled = COX/SCALM^2
TOX	m	1e-7	Represents the oxide thickness, calculated from COX when COX is input. The program uses default if COX is not specified. For TOX>1, unit is assumed to be Angstroms. But a level-dependent default can override it. See specific level in Chapter 9, “Selecting MOSFET Models: Level 1-40”.

Using Gate Overlap Capacitance Model Parameters

Name (Alias)	Units	Default	Description
CGBO (CGB)	F/m	0.0	Gate-bulk overlap capacitance per meter channel length. If CGBO is not set but WD and TOX are set, then CGBO is calculated. CGBOscaled = CGBO/SCALM

Name (Alias)	Units	Default	Description
CGDO (CGD, C2)	F/m	0.0	Gate-drain overlap capacitance per meter channel width. If CGDO is not set but LD or METO and TOX are set, then CGDO is calculated. CGDOscaled = CGDO/SCALM
CGSO *(CGS, C1)*	F/m	0.0	Gate-source overlap capacitance per meter channel width. If CGSO is not set but LD or METO and TOX are set, then CGSO is calculated. CGSOscaled = CGSO/SCALM
LD (LATD, DLAT)	m		Lateral diffusion into channel from source and drain diffusion. When both LD and XJ are unspecified: LD default=0.0. If LD is not set but XJ is specified, then LD is calculated from XJ. LD default=0.75 · XJ for all levels except LEVEL 4, for which LD default=0.75. LDscaled = LD · SCALM LEVEL 4: LDscaled = LD · XJ · SCALM
METO	m	0.0	Fringing field factor for gate-to-source and gate-to-drain overlap capacitance calculation METOscaled = METO · SCALM
WD	m	0.0	Lateral diffusion into channel from bulk along width WDscaled = WD · SCALM

Using Meyer Capacitance Parameters CAPOP=0, 1, 2

Name (Alias)	Units	Default	Description
CF1	V	0.0	Modified MEYER control for transition of cgs from depletion to weak inversion for CGSO (only for CAPOP=2)
CF2	V	0.1	Modified MEYER control for transition of cgs from weak to strong inversion region (only for CAPOP=2)
CF3		1.0	Modified MEYER control for transition of cgs and cgd from saturation to linear region as a function of vds (only for CAPOP=2)
CF4		50.0	Modified MEYER control for contour of cgb and cgs smoothing factors
CF5		0.667	Modified MEYER control for capacitance multiplier for cgs in saturation region
CF6		500.0	Modified MEYER control for contour of cgd smoothing factor
CGBEX		0.5	cgb exponent (only for CAPOP=1)

Using Charge Conservation Parameters (CAPOP=4)

Name (Alias)	Units	Default	Description
XQC		0.5	Coefficient of channel charge share attributed to drain; its range is 0.0 to 0.5. This parameter applies only to CAPOP=4 and some of its level-dependent aliases.

Specifying XQC and XPART for CAPOP=4, 9, 11, 12 and 13

Parameter rules for gate capacitance charge sharing coefficient, XQC & XPART, in the saturation region:

- If neither XPART or XQC is specified, the 0/100 model is used.
- If both XPART and XQC are specified, XPART overrides XQC.
- If XPART is specified:
  - XPART=0 → 40/60
  - XPART=0.4 → 40/60
  - XPART=0.5 → 50/50
  - XPART=1 → 0/100
  - XPART = any other value less than 1 → 40/60
  - XPART >1 → 0/100If XQC is specified:
- XQC=0 → 0/100
  - XQC=0.4 → 40/60
  - XQC=0.5 → 50/50
  - XQC=1 → 0/100
  - XQC = any other value less than 1 → 40/60
  - XQC>1 → 0/100

The only difference is the treatment of the parameter value 0.

After XPART/XQC is specified, the gate capacitance is ramped from 50/50 at Vds=0 volt (linear region) to the value (with Vds sweep) in the saturation region specified by XPART/XQC. This charge sharing coefficient ramping ensures the smoothness of the gate capacitance characteristic.

Using Overlap Capacitance Equations

The overlap capacitors are common to all models. You can input them explicitly, or the program calculates them. These overlap capacitors are added into the respective voltage-variable capacitors before integration and the DC operating point reports the combined parallel capacitance.

Gate-to-Bulk Overlap Capacitance

If CGBO is specified, then

$$CGBOeff = M \cdot Leff \cdot CGBOscaled$$

Otherwise,

$$CGBOeff = 2 \cdot WDscaled \cdot Leff \cdot COXscaled \cdot M$$

Gate-to-Source Overlap Capacitance

If CGSO is specified, then

$$CGSOeff = Weff \cdot CGSOscaled$$

Otherwise,

$$CGSOeff = Weff \cdot (LDscaled + METOscaled) \cdot COXscaled$$

Gate-to-Drain Overlap Capacitance

If CGDO is specified, then

$$CGDOeff = Weff \cdot CGDOscaled$$

Otherwise,

$$CGDOeff = Weff \cdot (LDscaled + METOscaled) \cdot COXscaled$$

The Leff is calculated for each model differently, and it is given in the corresponding model section. The Weff calculation is not quite the same as weff given in the model LEVEL 1, 2, 3, 6, 7 and 13 sections.

$$Weff = M \cdot (Wscaled \cdot WMLT + XWscaled)$$

The 2·WDscaled factor is not subtracted.

CAPOP=0 — SPICE Meyer Gate Capacitances

Definition:

$$cap = COXscaled \cdot Weff \cdot Leff$$

Gate-Bulk Capacitance (cgb)

Accumulation, vgs ≤ vth-PH1

$$cgb = cap$$

Depletion, vgs < vth

$$cgb = cap \cdot \frac{vth - vgs}{PH1}$$

Strong Inversion, vgs ≥ vth

$$cgb = 0$$

Gate-Source Capacitance (cgs)

$$\text{Accumulation, } \mathbf{vgs} \leq \mathbf{vth} - \frac{\text{PHI}}{2}$$

$$\text{cgs} = 0$$

Depletion, vgs ≤ vth

$$\text{cgs} = \text{CF5} \cdot \text{cap} + \frac{\text{cap} \cdot (\text{vgs} - \text{cth})}{0.75 \cdot \text{PHI}}$$

Strong Inversion Saturation Region, vgs > vth and vds ≥ vdsat

$$\text{cgs} = \text{CF5} \cdot \text{cap}$$

Strong Inversion Linear Region, vgs > vth and vds < vdsat

$$\text{cgs} = \text{CF5} \cdot \text{cap} \cdot \left\{ 1 - \left[\frac{\text{vdsat} - \text{vds}}{2 \cdot (\text{vdsat} + \text{vsb}) - \text{vds} - \text{vsb}} \right]^2 \right\}$$

Gate-Drain Capacitance (cgd)

The gate-drain capacitance has value only in the linear region.

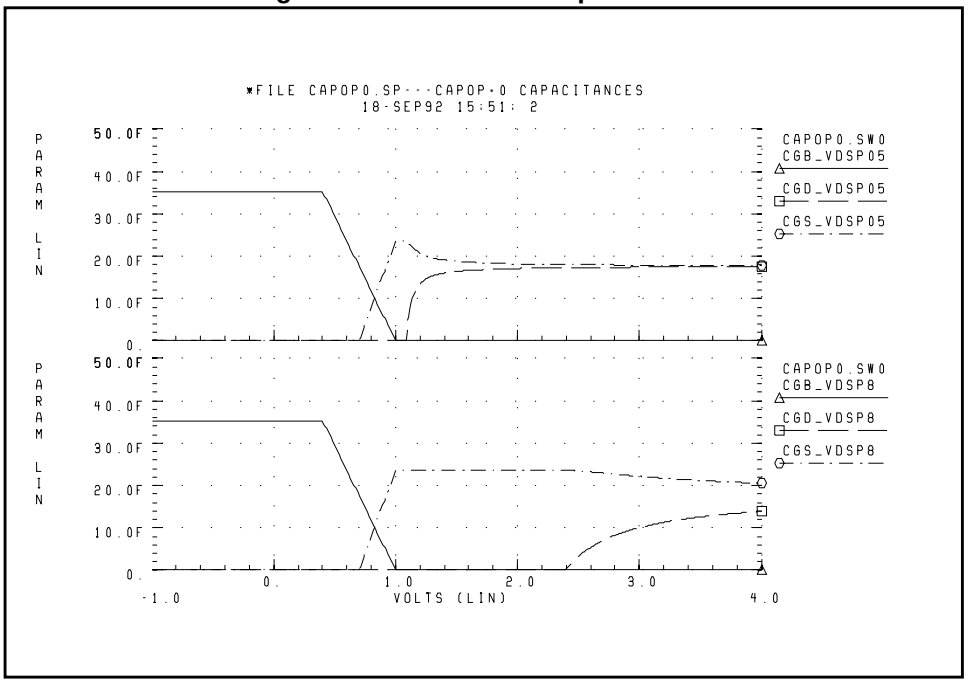
Strong Inversion Linear Region, vgs > vth and vds < vdsat.

$$\text{cgd} = \text{CF5} \cdot \text{cap} \cdot \left\{ 1 - \left[\frac{\text{vdsat} + \text{vsb}}{2 \cdot (\text{vdsat} + \text{vsb}) - \text{vds} - \text{vsb}} \right]^2 \right\}$$

Example

```
*file capop0.sp---capop=0 capacitances
*
*this file is used to create spice meyer gate c-v plots
**
*(capop=0) for low vds and high vds
*
.options acct=2 post=2 dccap=1 nomod
.dc vg1 -1 4 .01
.print dc cgb_vdsp05=par('-lx21(m1)')
+ cgd_vdsp05=par('-lx19(m1)') cgs_vdsp05=par('-lx20(m1)')
.print dc cgb_vdsp8=par('-lx21(m2)') cgd_vdsp8=par('-lx19(m2)')
+ cgs_vdsp8=par('-lx20(m2)')
****************************************
m1 d1 g1 0 0 mn l=5e-6 w=20e-6 $ create capacitances for
+ vds=0.05
m2 d2 g1 0 0 mn l=5e-6 w=20e-6 $ create capacitances for
+ vds=0.80
****************************************
vd1 d1 0 dc 0.05
vd2 d2 0 dc 0.80
vg1 g1 0 dc 0.0
*
****************************************
*
.model mn nmos ( level = 2
+ vto = 1.0 gamma = 1.40 nsub = 7.20e15
+ uo = 817 ucrit = 3.04e4 phi=.6
+ uexp = 0.102 neff = 1.74 vmax = 4.59e5
+ tox = 9.77e-8 cj = 0 cjsw = 0 js = 0
+ capop=0 )
.end
```

Figure 8-19: CAPOP=0 Capacitances



CAPOP=1 — Modified Meyer Gate Capacitances

Define

$$cap = COXscaled \cdot Weff \cdot Leff$$

In the following equations, G^-, G^+, D^-, and D^+ are smooth factors. They are not user-defined parameters.

Gate-Bulk Capacitance (cgb)

Accumulation, vgs ≤ vfb – vsb

$$cgb = cap$$

Depletion, vgs ≤vth

$$cgb = \frac{cap}{\left[1 + 4 \cdot \frac{vgs + vsb - vfb}{GAMMA^2}\right]^{CGBEX}}$$

Strong Inversion, vgs > vth

$$cgb = \frac{G^+ \cdot cap}{\left[1 + 4 \cdot \frac{GAMMA \cdot (vsb + PHI)^2 + vsb + PHI}{GAMMA^2}\right]^{CGBEX}}$$

Note: In the above equations, GAMMA is replaced by effective γ for model level higher than 4.

Gate-Source Capacitance (cgs)

Low vds (vds < 0.1)

Accumulation, vgs ≤ vth

$$cgs = CF5 \cdot cap \cdot G^{-} \cdot D^{-}$$

Weak Inversion, vgs < vth + 0.1

$$cgs = CF5 \cdot cap \cdot \left\{ \frac{vgs - vth}{0.1} \cdot \left[1 - \left(\frac{0.1 - vds}{0.2 - vds} \right)^2 - D^{-} \right] + D^{-} \right\}$$

Strong Inversion, vgs ≥ vth + 0.1

$$cgs = CF5 \cdot cap \cdot \left\{ 1 - \left[\frac{vgs - vth - vds}{2 \cdot (vgs - vth) - vds} \right]^2 \right\}$$

High vds (vds 0.1)

Accumulation, vgs ≤vth

$$cgs = CF5 \cdot cap \cdot G^{-}$$

Saturation Region, vgs < vth + vds

$$cgs = CF5 \cdot cap$$

Linear Region, vgs ≥ vth + vds

$$cgs = CF5 \cdot cap \cdot \left\{ 1 - \left[\frac{vgs - vth - vds}{2 \cdot (vgs - vth) - vds} \right]^2 \right\}$$

Gate-Drain Capacitance (cgd)

Low vds (vds < 0.1)

Accumulation, vgs ≤ vth

$$cgd = CF5 \cdot cap \cdot G^{-} \cdot D^{+}$$

Weak Inversion, vgs < vth + 0.1

$$cgd = CF5 \cdot cap \cdot \left\{ D^{+} + \frac{vgs - vgh}{0.1} \cdot \max\left[0, 1 - \left(\frac{0.1}{0.2 - vds} \right)^{2} - D^{+} \right] \right\}$$

Strong Inversion, vgs ≥ vth + 0.1

$$cgd = CF5 \cdot cap \cdot \max\left\{ D^{+}, 1 - \left[\frac{vgs - vth}{2 \cdot (vgs - vth) - vds} \right]^{2} \right\}$$

High vds(vds 0.1)

Accumulation, vgs ≤ vth

$$cgd = CF5 \cdot cap \cdot G^{-} \cdot D^{+}$$

Saturation Region, vgs < vth + vds

$$cgd = CF5 \cdot cap \cdot D^{+}$$

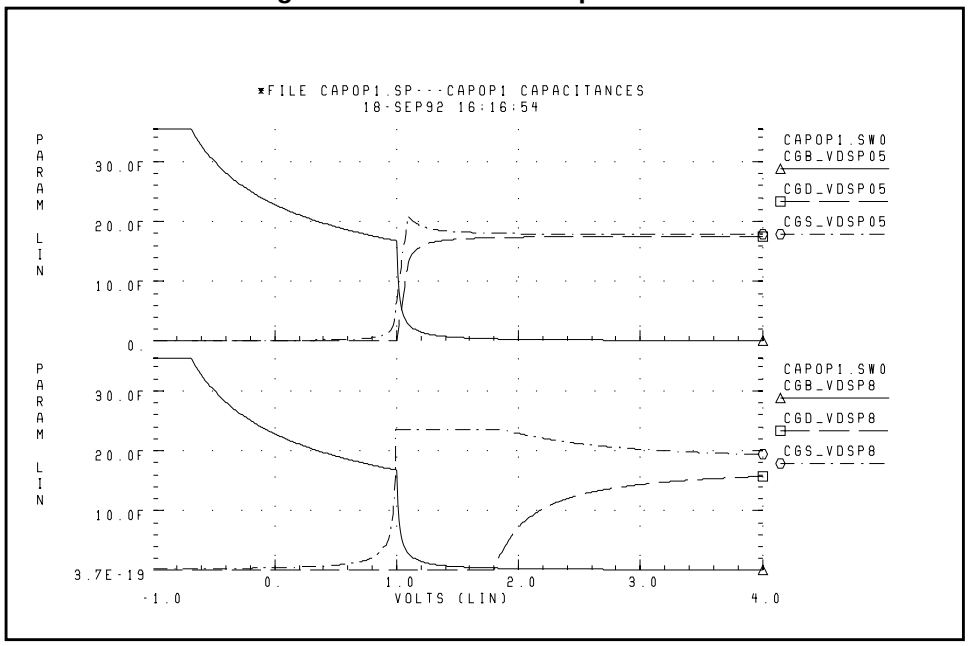
Strong Inversion, vgs ≥ vth + vds

$$cgd = CF5 \cdot cap \cdot \max\left\{ D^{+}, 1 - \left[\frac{vgs - vth}{2 \cdot (vgs - vth) - vds} \right]^{2} \right\}$$

Example

```
*file capop1.sp---capop1 capacitances
*
*this file creates the modified meyer gate c-v plots
*(capop=1) for low vds and high vds.
*
.options acct=2 post=2 dccap=1 nomod
.dc vg1 -1 4 .01
.print dc cgb_vdsp05=par('lx21(m1)')
+ cgd_vdsp05=par('-lx19(m1)')
+ cgs_vdsp05=par('-lx20(m1)')
.print dc cgb_vdsp8=par('-lx21(m2)')
+ cgd_vdsp8=par('-lx19(m2)')
+ cgs_vdsp8=par('-lx20(m2)')
****************************************
m1 d1 g1 0 0 mn l=5e-6 w=20e-6 $creates capacitances
+ for vds=0.05
m2 d2 g1 0 0 mn l=5e-6 w=20e-6 $creates capacitances
+ for vds=0.80
****************************************
vd1 d1 0 dc 0.05
vd2 d2 0 dc 0.80
vg1 g1 0 dc 0.0
*
****************************************
*
.model mn nmos ( level = 2
+ vto = 1.0 gamma = 1.40 nsub = 7.20e15
+ tox = 9.77e-8 uo = 817 ucrit = 3.04e4
+ uexp = 0.102 neff = 1.74 vmax = 4.59e5
+ phi = 0.6 cj = 0 cjsw = 0 js = 0
+ capop=1 )
.end
```

Figure 8-20: CAPOP=1 Capacitances



CAPOP=2—Parameterized Modified Meyer Capacitances

The CAPOP=2 Meyer capacitance model is the more general form of Meyer capacitance. The CAPOP=1 Meyer capacitance model is the special case of CAPOP=2 when CF1=0, CF2=0.1, and CF3=1.

In the following equations, G^-, G^+, D^-, and DD^+ are smooth factors. They are not user-defined parameters.

Definition

$$cap = COXscaled \cdot Weff \cdot Leff$$

Gate-Bulk Capacitance (cgb)

Accumulation, vgs ≤ vfb - vsb

$$cgb = cap$$

Depletion, vgs ≤ vth

$$cgs = \frac{cap}{\left(1 + 4 \cdot \frac{vgs + vsb - vfb}{GAMMA^2}\right)^{1/2}}$$

Inversion, vgs > vth

$$cgb = \frac{G^+ \cdot cap}{\left[1 + 4 \cdot \frac{GAMMA \cdot (PHI + vsb)^{1/2} + PHI + vsb}{GAMMA^2}\right]^{1/2}}$$

Note: In the above equations, GAMMA is replaced by effective γ for model level higher than 4.

Gate-Source Capacitance (cgs)

Low vds (vds < 0.1)

Accumulation, vgs < vth – CF1

$$cgs = CF5 \cdot cap \cdot G^- \cdot D^-$$

Depletion, vgs ≤ vth + CF2 – CF1

$$cgs = CF5 \cdot cap \cdot \left\{\frac{vgs - vth + CF1}{CF2} \cdot \left[1 - \left(CF2 - \frac{vds}{2 \cdot CF2 - vds}\right)^2 - D^-\right] + D^-\right\}$$

Strong Inversion, vgs > vth + max (CF2 – CF1, CF3 · vds)
UPDATE=0

Strong Inversion, vgs > vth + CF2 – CF1, UPDATE=1

$$cgs = CF5 \cdot cap \cdot \left\{1 - \left[\frac{vgs - vth + CF1 - vds}{2 \cdot (vgs - vth + CF1) - vds}\right]^2\right\}$$

High vds (vds 0.1)

Accumulation, vgs < vth – CF1

$$cgs = CF5 \cdot cap \cdot G^{-} \cdot D^{+}, \quad CF1 \neq 0$$
$$cgs = CF5 \cdot cap \cdot G^{-}, \quad CF1 = 0$$

Weak Inversion, vgs < vth + CF2 – CF1, CF1 ≠ 0

$$cgs = CF5 \cdot cap \cdot \max\left(\frac{vgs - vth + CF1}{CF2}, D^{+}\right)$$

Saturation Region, vgs < vth + CF3 · vds

$$cgs = CF5 \cdot cap$$

Linear Region, vgs > vth + CF3 · vds

$$cgs = CF5 \cdot cap \cdot \left\{1 - \left[\frac{vgs - vth - vds}{2 \cdot (vgs - vth) - vds}\right]^2\right\}, \quad \text{UPDATE=0}, \quad CF1=0$$

$$cgs = CG5 \cdot cap \cdot \left\{1 - \left[\frac{vgs - vth - CF3 \cdot vds}{2 \cdot (vgs - vth) - CF3 \cdot vds}\right]^2\right\}, \quad \text{UPDATE=1}$$

Gate-Drain Capacitance (cgd)

Low vds, (vds < 0.1)

Accumulation, vgs ≤ vth – CF1

$$cgd = CF5 \cdot cap \cdot G^{-} \cdot D^{-}$$

Weak Inversion, vgs < vth + CF2 – CF1

$$cgd = CF5 \cdot cap \cdot \left\{D^{-} + \frac{vgs - vth + CF1}{CF2} \cdot \max\left[0, 1 - \left(\frac{CF2}{2 \cdot CF2 - vds}\right)^2 - D^{-}\right]\right\}$$

Strong Inversion, vgs ≥ vth + CF2 – CF1

$$cgd = CF5 \cdot cap \cdot \max\left\{D^{-}, 1 - \left[\frac{vgs - vth + CF1}{2 \cdot (vgs - vth + CF1) - vds}\right]^2\right\}$$

High vds (vds > 0.1)

Accumulation, vgs ≤ vth – CF1

$$cgd = CF5 \cdot cap \cdot G^{-} \cdot DD^{+}$$

Saturation Region, vgs ≤ vth + CF3 · vds

$$cgd = CF5 \cdot cap \cdot DD^{+}$$

Note: In the above equation, DD^{+} is a function of CF3, if UPDATE=1.

Linear Region, vgs > vth + CF3 · vds

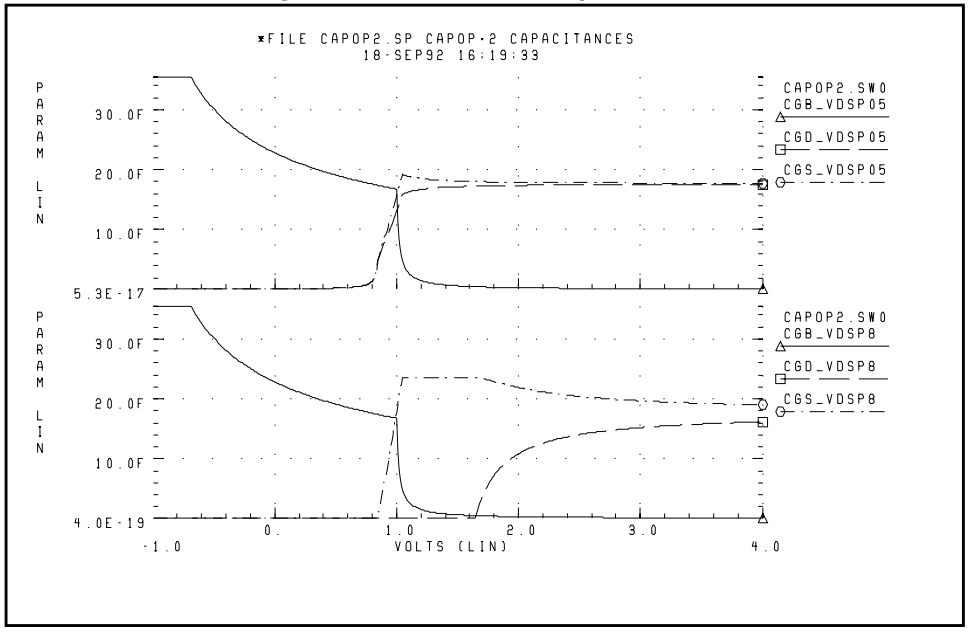
$$cgd = CF5 \cdot cap \cdot \max\left\{DD^{+}, 1 - \left[\frac{vgs - vth}{2 \cdot (vgs - vth) - CF3 \cdot vds}\right]^2\right\}$$

Example

```
*file capop2.sp capop=2 capacitances
*
*this file creates parameterized modified gate capacitances
*(capop=2) for low and high vds.
*
.options acct=2 post=2 dccap=1 nomod
.dc vg1 -1 4 .01
.print dc cgb_vdsp05=par('-lx21(m1)')
+ cgd_vdsp05=par('-lx19(m1)') cgs_vdsp05=par('-lx20(m1)')
.print dc cgb_vdsp8=par('-lx21(m2)') cgd_vdsp8=par('-
lx19(m2)')
+ cgs_vdsp8=par('-lx20(m2)')
```

```
*****************************************
m1 d1 g1 0 0 mn l=5e-6 w=20e-6 $creates capacitances for
+ vds=0.05
m2 d2 g1 0 0 mn l=5e-6 w=20e-6 $creates capacitances for
+ vds=0.80
*****************************************
vd1 d1 0 dc 0.05
vd2 d2 0 dc 0.80
vg1 g1 0 dc 0.0
*
*****************************************
*
.model mn nmos ( level = 2
+ vto = 1.0 gamma = 1.40 nsub = 7.20e15
+ tox = 9.77e-8 uo = 817 ucrit = 3.04e4
+ uexp = 0.102 neff = 1.74 phi = 0.6
+ vmax = 4.59e5 cj = 0 cjsw = 0 js = 0
+ capop=2 cf1=0.15 cf2=.2 cf3=.8 cf5=.666)
.end
```

Figure 8-21: CAPOP=2 Capacitances



CAPOP=3 — Gate Capacitances (Simpson Integration)

The CAPOP 3 model is the same set of equations and parameters as the CAPOP 2 model. The charges are obtained by Simpson numeric integration instead of the box integration found in CAPOP models 1, 2, and 6.

Gate capacitances are not constant values with respect to voltages. The capacitance values can best be described by the incremental capacitance:

$$C(v) = \frac{dq(v)}{dv}$$

where q(v) is the charge on the capacitor and v is the voltage across the capacitor.

The formula for calculating the differential is difficult to derive. Furthermore, the voltage is required as the accumulated capacitance over time. The timewise formula is:

$$i(t) = \frac{dq(v)}{dt} = C(v) \cdot \frac{dv(t)}{dt}$$

The charge is:

$$q(v) = \int_0^v C(v)dv$$

For the calculation of current:

$$i(t) = \frac{dq(v)}{dt} = \left(\frac{d}{dt}\right)\int_0^v C(v)dv$$

For small intervals:

$$I(n+1) = \frac{dq(v)}{dt} = \frac{1}{t(n+1) - t(n)} \int_{V(n)}^{V(n+1)} C(v)dv$$

The integral has been approximated in SPICE by:

$$I(n+1) = \left(\frac{V(n+1) - V(n)}{t(n+1) - t(n)}\right) \cdot \left(\frac{C[V(n+1)] + C[V(n)]}{2}\right)$$

This last formula is the trapezoidal rule for integration over two points. The charge is approximated as the average capacitance times the change in voltage. If the capacitance is nonlinear, this approximation can be in error. To estimate the charge accurately, use Simpson's numerical integration rule. This method provides charge conservation control.

To use this model, set the model parameter CAPOP to 3 and use the existing CAPOP=2 model parameters. Modify the OPTIONS settings RELV (relative voltage tolerance), RELMOS (relative current tolerance for MOSFETs), and CVTOL (capacitor voltage tolerance). The default of 0.5 is a good nominal value for CVTOL. The option CVTOL sets the number of integration steps with the formula:

$$n = \frac{|V(n+1) - V(n)|}{CVTOL}$$

Using a large value for CVTOL decreases the number of integration steps for the time interval n to n+1; this yields slightly less accurate integration results. Using a small CVTOL value increases the computational load, and in some instances, severely.

CAPOP=4 — Charge Conservation Capacitance Model

The charge conservation method (See *Ward, Donald E. and Robert W. Dutton "A Charge-Oriented Model for MOS Transistor"*) is not implemented correctly into the SPICE2G.6 program. There are errors in the derivative of charges, especially in LEVEL 3 models. Also, channel charge partition is not continuous going from linear to saturation regions.

In the Avant! True-Hspice models, these problems are corrected. By specifying model parameter CAPOP=4, the level-dependent recommended charge conservation model is selected. The ratio of channel charge partitioning between drain and source is selected by the model parameter XQC.

For example, if XQC=.4 is set, then the saturation region 40% of the channel charge is associated to drain and the remaining 60% is associated to the source. In the linear region, the ratio is 50/50. An empirical equation is used to make a smooth transition from 50/50 (linear region) to 40/60 (saturation region).

Also, the capacitance coefficients, which are the derivative of gate, bulk, drain, and source charges, are continuous. Model LEVELs 2, 3, 4, 6, 7, and 13 have a charge conservation capacitance model that is invoked by setting CAPOP=4.

In the following example, only the charge conservation capacitance CAPOP=4 and the improved charge conservation capacitance CAPOP=9 for the model LEVEL 3 are compared. The capacitances CGS and CGD for CAPOP=4 model (SPICE2G.6) show discontinuity at the saturation and linear region boundary while the CAPOP=9 model does not have discontinuity. For the purpose of comparison, the modified Meyer capacitances (CAPOP=2) also is provided. The shape of CGS and CGD capacitances resulting from CAPOP=9 are much closer to those of CAPOP=2.

Example

```
FILE MCAP3.SP CHARGE CONSERVATION MOSFET CAPS., CAPOP=4,9 LEVEL=3
*
* CGGB = LX18(M) DERIVATIVE OF QG WITH RESPECT TO VGB.
* CGDB = LX19(M) DERIVATIVE OF QG WITH RESPECT TO VDB.
* CGSB = LX20(M) DERIVATIVE OF QG WITH RESPECT TO VSB.
* CBGB = LX21(M) DERIVATIVE OF QB WITH RESPECT TO VGB.
* CBDB = LX22(M) DERIVATIVE OF QB WITH RESPECT TO VDB.
* CBSB = LX23(M) DERIVATIVE OF QB WITH RESPECT TO VSB.
* CDGB = LX32(M) DERIVATIVE OF QD WITH RESPECT TO VGB.
* CDDB = LX33(M) DERIVATIVE OF QD WITH RESPECT TO VDB.
* CDSB = LX34(M) DERIVATIVE OF QD WITH RESPECT TO VSB.
* THE SIX NONRECIPROCAL CAPACITANCES CGB,CBG,CGS,CSG,CGD,AND CDG
* ARE DERIVED FROM THE ABOVE CAPACITANCE FACTORS.
*
.OPTIONS DCCAP=1 POST NOMOD
.PARAM XQC=0.4 CAPOP=4
.DC VGG -2 5 .02
.print CGB=PAR('LX18(M)+LX19(M)+LX20(M)')
+ CBG=PAR('-LX21(M)')
+ CGS=PAR('-LX20(M)')
+ CSG=PAR('LX18(M)+LX21(M)+LX32(M)')
+ CGD=PAR('-LX19(M)')
```

```
+ CDG=PAR('-LX32(M)')
.print
+ CG =par('LX14(M)')
VDD D 0 2.5
VGG G 0 0
VBB B 0 -1
M D G 0 B MOS W=10U L=5U
.MODEL MOS NMOS LEVEL=3 COX=1E-4 VTO=.3 CAPOP=CAPOP
+ UO=1000 GAMMA=.5 PHI=.5 XQC=XQC
+ THETA=0.06 VMAX=1.9E5 ETA=0.3 DELTA=0.05 KAPPA=0.5 XJ=.3U
+ CGSO=0 CGDO=0 CGBO=0 CJ=0 JS=0 IS=0
*
.ALTER
.PARAM CAPOP=9
.END
```

Figure 8-22: CAPOP=4, 9 Capacitances for LEVEL 3 Model

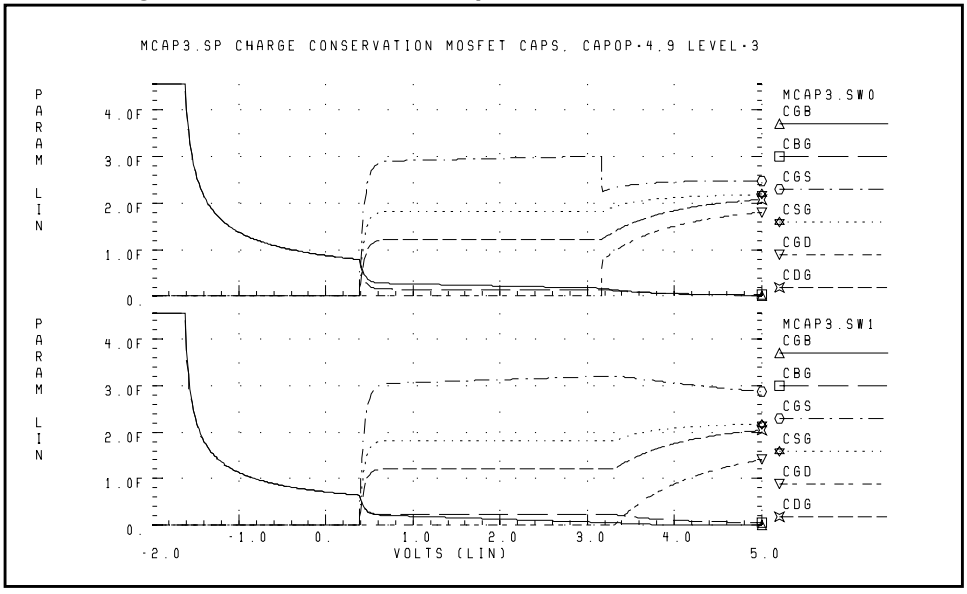
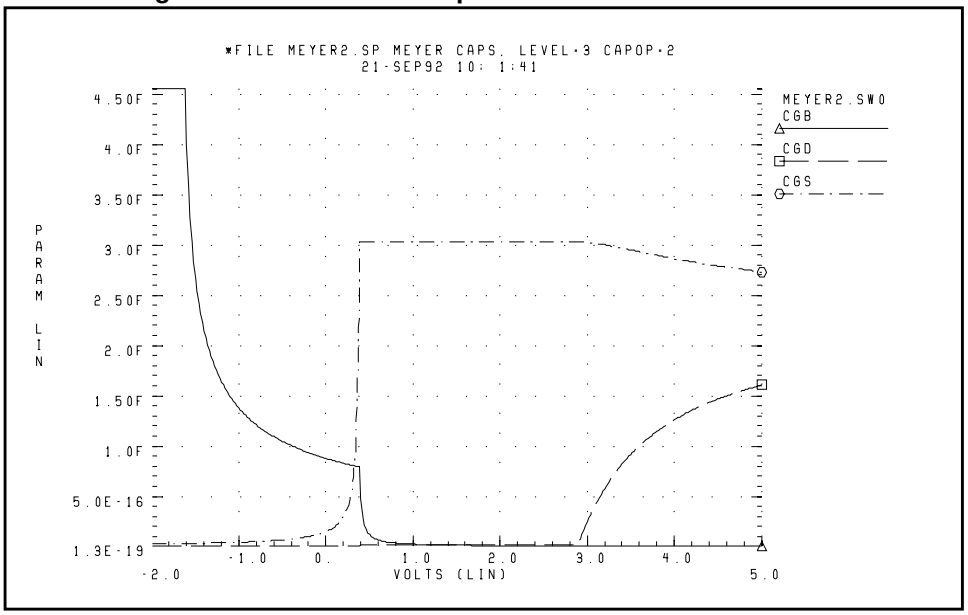


Figure 8-23: CAPOP=2 Capacitances for LEVEL 3 Model



The following example tests the charge conservation capacitance model (Yang, P., B.D. Epler, and P.K. Chaterjee ‘An Investigation of the Charge Conservation Problem) and compares the Meyer model and charge conservation model. As the following graph illustrates, the charge conservation model gives more accurate results.

Example

```
*FILE:CHRGPUMP.SP CHARGE CONSERVATION TEST FOR CHARGE
      PUMP CIRCUIT
*TEST CIRCUIT OF A MOSFET CAPACITOR AND A LINEAR CAPACITOR
.OPTIONS ACCT LIST NOMOD POST
+ RELTOL=1E-3 ABSTOL=1E-6 CHGTOL=1E-14
.PARAM CAPOP=2
.OP
.TRAN 2NS 470NS SWEEP CAPOP POI 2 2,9
.IC V(S)=1
*
VIN G 0 PULSE 0 5 15NS 5NS 5NS 50NS 100NS
VBB 0 B PULSE 0 5 0NS 5NS 5NS 50NS 100NS
VDD D D- PULSE 0 5 25NS 5NS 5NS 50NS 100NS
```

```
*
RC D- S 10K
C2 S 0 10P
M1 D G S B MM W=3.5U L=5.5U
+AD=100P AS=100P PD=50U PS=50U NRD=1 NRS=1
*
.MODEL MM NMOS LEVEL=3 VTO=0.7 KP=50E-6 GAMMA=0.96
+PHI=0.5763 TOX=50E-9 NSUB=1.0E16 LD=0.5E-6
+VMAX=268139 THETA=0.05 ETA=1 KAPPA=0.5 CJ=1E-4
+CJSW=0.05E-9 RSH=20 JS=1E-8 PB=0.7
+CGD=0 CGS=0 IS=0 JS=0
+CAPOP=CAPOP
*
.PRINT TRAN VOUT=V(S) VIN=V(D) VBB=V(B)
+ VDD=V(D,D-)
.END
```

Figure 8-24: Charge Pump Circuit

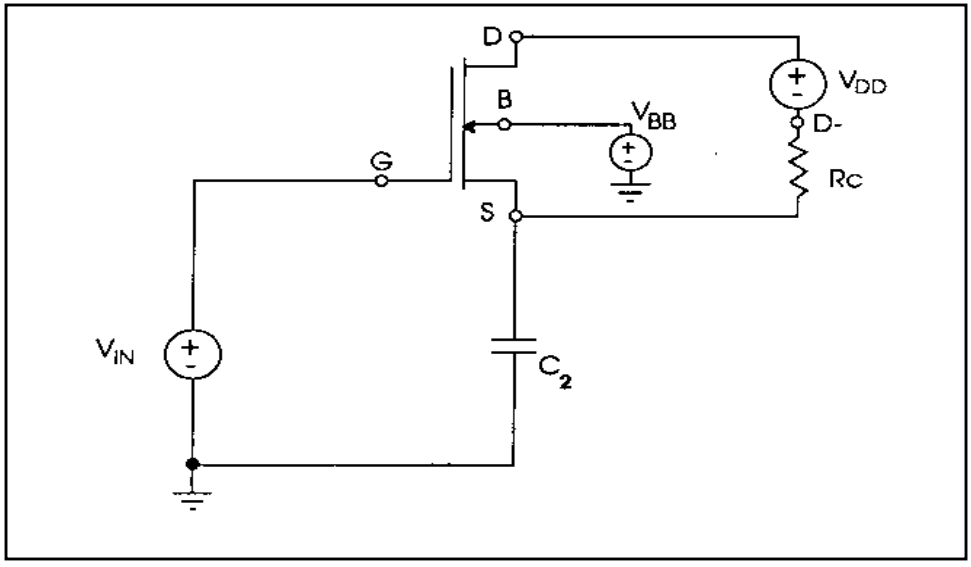
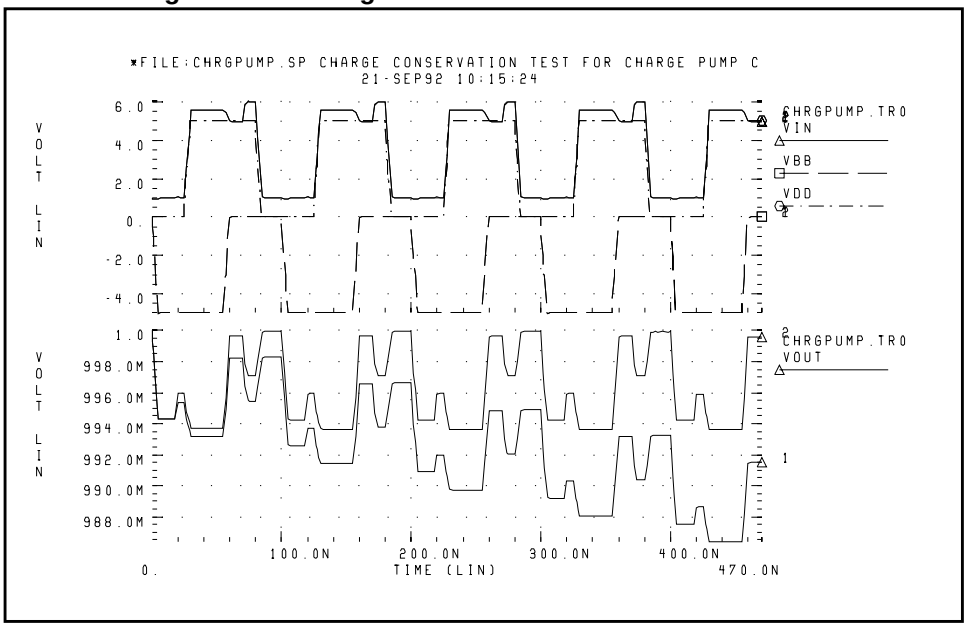


Figure 8-25: Charge Conservation Test: CAPOP=2 or 9



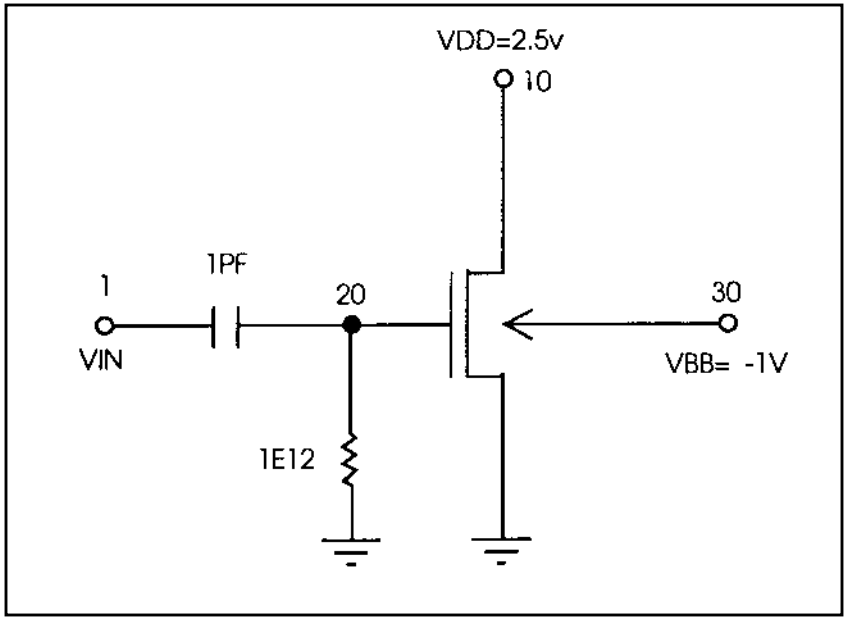
The following example applies a pulse through a constant capacitance to the gate of MOS transistor. Ideally, if the model conserves charge, the voltage at node 20 should become zero when the input pulse goes to zero. Consequently, the model that provides voltage closer to zero for node 20 conserves the charge better. As results indicate, the CAPOP=4 model is better than the CAPOP=2 model.

This example also compares the charge conservation models in SPICE2G.6 and Avant! True-Hspice models. The results indicate that the True-Hspice models are more accurate.

Example

```
FILE MCAP2_A.SP
.OPTIONS SPICE NOMOD DELMAX=.25N
.PARAM CAPOP=4
.TRAN 1NS 40NS SWEEP CAPOP POI 2 4 2
.PRINT TRAN V(1) V(20)
VIN 1 0 PULSE (0V, 5V, 0NS, 5NS, 5NS, 5NS, 20NS)
CIN 1 20 1PF
RLEAK 20 0 1E+12
VDD 10 0 1.3
VBB 30 0 -1
M 10 20 0 30 MOS W=10U L=5U
.MODEL MOS NMOS LEVEL=2 TOX=250E-10 VTO=.3
+ UO=1000 LAMBDA=1E-3 GAMMA=.5 PHI=.5 XQC=.5
+ THETA=0.067 VMAX=1.956E5 XJ=.3U
+ CGSO=0 CGDO=0 CGBO=0
+ CJ=0 JS=0 IS=0
+ CAPOP=CAPOP
.END
```

Figure 8-26: Charge Conservation Test Circuit



CAPOP=5 — Gate Capacitance

If you use CAPOP=5 for no capacitors, then simulation does not calculate gate capacitance.

CAPOP=6 — AMI Gate Capacitance Model

Define:

$$vgst = vgs - \frac{(vth + vfb)}{2}$$

$$cox = \frac{\varepsilon ox}{TOX \cdot 1e\text{-}10} \cdot Weff \cdot Leff$$

The gate capacitance *cgs* is calculated according to the equations below in the different regions.

0.5 · (vth + vfb) > vgs

$$cgs = 0$$

0.5 · (vth + vfb) <vgs <vth

For vgst < vds,

$$cgs = \frac{4}{3} \cdot \frac{cox \cdot vgst}{vth - vfb}$$

For vgst > vds,

$$cgs = arg \cdot \frac{4}{3} \cdot \frac{cox \cdot vgst}{vth - vfb}$$

vgs > vth

For vgst < vds,

$$cgs = \frac{2}{3} \cdot cox$$

For vgst > vds,

$$cgs = arg \cdot \frac{2}{3} \cdot cox$$

$$arg = vgst \cdot \frac{(3 \cdot vgst - 2 \cdot vds)}{(2 \cdot vgst - vds)^2}$$

The gate capacitance *cgd* is calculated according to the equations below in the different regions.

vgs < vth

$$cgd = 0$$

vgs > vth and vgst < vds

$$cgd = 0$$

vgs > vth and vgst > vds

$$cgd = arg \cdot \frac{2}{3} \cdot cox$$

$$arg = (3 \cdot vgst - vds) \cdot \frac{(vgst - vds)}{(2 \cdot vgst - vds)^2}$$

The gate capacitance cgb is combined with the calculation of both oxide capacitance and depletion capacitance as shown below.

$$cgb = \frac{cgbx \cdot cd}{cgbx + cd}$$

Oxide capacitance cgbx, is calculated as:

$$cgbx = cox - cgs - cgd$$

Depletion capacitance cd is voltage-dependent.

$$cd = \frac{\varepsilon si}{wd} \cdot Weff \cdot Leff$$

$$wd = \left(\frac{2 \cdot \varepsilon si \cdot vc}{q \cdot NSUB}\right)^{1/2}$$

vc = *The effective voltage from channel to substrate (bulk)*

The following shows the equations for vc under various conditions:

vgs + vsb < vfb

$$vc = 0$$

vgs + vsb > vfb

$$vc = vgs + vsb - vfb$$

vgst > 0, vgs < vth, vgst < vds

$$vc = \frac{1}{2} \cdot (vth - vfb) + \frac{3}{2} \cdot vgst + vsb$$

vgst > 0, vgs < vth, vgst > vds

$$vc = \frac{1}{2} \cdot (vth - vfb) + vgst + \frac{1}{2} \cdot vds + vsb$$

vgs > vth, vgst < vds

$$vc = vth - vfb + \frac{1}{2} \cdot vgst + vsb$$

vgs > vth, vgst > vds

$$vc = vth - vfb + \frac{1}{2} \cdot vds + vsb$$

CAPOP=13 — BSIM1-based Charge-Conserving Gate Capacitance Model

See ‘LEVEL 13 BSIM Model” on page 9-102.

CAPOP=39 — BSIM2 Charge-Conserving Gate Capacitance Model

See ‘LEVEL 39 BSIM2 Model” on page 9-177.

Calculating Effective Length and Width for AC Gate Capacitance

For some MOS processes and parameter extraction methods, it is helpful to allow different Leff and Weff values for AC analysis than for DC analysis. For AC gate capacitance calculations, substitute model parameters LDAC and WDAC for LD and WD in Leff and Weff calculations. You can use LD and WD in Leff and Weff calculations for DC current.

To use LDAC and WDAC, enter XL, LD, LDAC, XW, WD, WDAC in the .MODEL statement. The model uses the following equations for DC current calculations.

$$Leff = L + XL - 2 \cdot LD$$

$$Weff = W + XW - 2 \cdot WD$$

and uses the following equations for AC gate capacitance calculations

$$Leff = L + XL - 2 \cdot LDAC$$

$$Weff = W + XW - 2 \cdot WDAC$$

The noise calculations use the DC Weff and Leff values.

Use LDAC and WDAC with the standard XL, LD, XW, and WD parameters. Do not use LDAC and WDAC with other parameters, such as DL0 and DW0.

Noise Models

This section describes how to use noise models.

Using Noise Parameters

Name (Alias)	Units	Default	Description
AF		1.0	Flicker noise exponent
KF		0.0	Flicker noise coefficient. Reasonable values for KF are in the range 1e-19 to 1e-25 V^2F.
NLEV		2.0	Noise equation selector
GDSNOI		1.0	Channel thermal noise coefficient (use with NLEV=3)

Using Noise Equations

The MOSFET model noise equations have a selector parameter, NLEV, that selects either the original SPICE flicker noise or an equation proposed by Gray and Meyer.

Thermal noise generation in the drain and source resistors is modeled by the two sources inrd and inrs (units amp/$(Hz)^{1/2}$), as shown in Figure 8-10. The values of these sources can be determined by:

$$\text{inrs} = \left(\frac{4kt}{rs}\right)^{1/2}$$

$$\text{inrd} = \left(\frac{4kt}{rd}\right)^{1/2}$$

Channel thermal noise and flicker noise are modeled by the current source ind and defined by the equation:

$$\text{ind}^2 = (\text{channel } \textit{thermal noise})^2 + (\textit{flicker noise})^2$$

If the model parameter NLEV is less than 3, then

$$\textit{channel thermal noise} = \left(\frac{8\text{kT} \cdot \text{gm}}{3}\right)^{1/2}$$

The above formula is used in both saturation and linear regions, which can lead to wrong results in the linear region. For example, at VDS=0, channel thermal noise becomes zero because gm=0. This calculation is physically impossible. If you set the NLEV model parameter to 3, simulation uses a different equation, which is valid in both linear and saturation regions. See *Tsividis, Yanis P., Operation and Modeling of the MOS Transistor, McGraw-Hill, 1987, p. 340.*

For NLEV=3,

$$\textit{channel thermal noise} = \left(\frac{8\text{kt}}{3} \cdot \beta \cdot (\text{vgs} - \text{vth}) \cdot \frac{1 + \text{a} + \text{a}^2}{1 + \text{a}} \cdot \text{GDSNOI}\right)^{1/2}$$

where

$$\text{a} = 1 - \frac{\text{vds}}{\text{vdsat}} \qquad \textit{Linear region}$$

$$\text{a} = 0 \qquad \textit{Saturation region}$$

The two parameters AF and KF are used in the small-signal AC noise analysis to determine the equivalent flicker noise current generator connected between drain and source.

NLEV=0 (SPICE):

$$\textit{flicker noise} = \left(\frac{\text{KF} \cdot \text{Ids}^{\text{AF}}}{\text{COX} \cdot \text{Leff}^2 \cdot \text{f}}\right)^{1/2}$$

For NLEV=1 the Leff^2 in the above equation is replaced by Weff · Leff.

NLEV=2, 3:

$$flicker\ noise = \left(\frac{KF \cdot gm^2}{COX \cdot Weff \cdot Leff \cdot f^{AF}}\right)^{1/2}$$

Noise Summary Printout Definitions

RD, V^2/Hz	Output thermal noise due to drain resistor
RS, V^2/Hz	Output thermal noise due to source resistor
RX	Transfer function of channel thermal or flicker noise to the output. This is not a noise, it is a transfer coefficient, reflecting the contribution of channel thermal or flicker noise to the output.
ID, V^2/Hz	Output channel thermal noise: $ID = RX^2 \cdot (channel\ thermal\ noise)^2$
FN, V^2/Hz	Output flicker noise: $FN = RX^2 \cdot (flicker\ noise)^2$
TOT, V^2/Hz	Total output noise: $TOT = RD + RS + ID + FN$

Temperature Parameters and Equations

Temperature Parameters

The following temperature parameters apply to all MOSFET model levels and the associated bulk-to-drain and bulk-to-source MOSFET diode within the MOSFET model. The temperature equations used for the calculation of temperature effects on the model parameters are selected by the TLEV and TLEVC parameters.

Temperature Effects Parameters

Name (Alias)	Units	Default	Description
BEX		-1.5	Low field mobility, UO, temperature exponent
CTA	1/°K	0.0	Junction capacitance CJ temperature coefficient. Set TLEVC to 1 to enable CTA to override default temperature compensation.
CTP	1/°K	0.0	Junction sidewall capacitance CJSW temperature coefficient. Set TLEVC to 1 to enable CTP to override default temperature compensation.

Name (Alias)	Units	Default	Description
EG	eV		Energy gap for pn junction diode. Set default=1.11, for TLEV=0 or 1 and default=1.16, for TLEV=2. 1.17 – silicon 0.69 – Schottky barrier diode 0.67 – germanium 1.52 – gallium arsenide
F1EX		0	Bulk junction bottom grading coefficient
GAP1	eV/°K	7.02e-4	First bandgap correction factor (from Sze, alpha term) 7.02e-4 – silicon 4.73e-4 – silicon 4.56e-4 – germanium 5.41e-4 – gallium arsenide
GAP2	°K	1108	Second bandgap correction factor (from Sze, beta term) 1108 – silicon 636 – silicon 210 – germanium 204 – gallium arsenide
LAMEX	1/°K	0	LAMBDA temperature coefficient
N		1.0	Emission coefficient
MJ		0.5	Bulk junction bottom grading coefficient
MJSW		0.33	Bulk junction sidewall grading coefficient

Name (Alias)	Units	Default	Description
PTA	V/°K	0.0	Junction potential PB temperature coefficient. Set TLEVC to 1 or 2 to enable PTA to override default temperature compensation.
PTC	V/°K	0.0	Fermi potential PHI temperature coefficient. Set TLEVC to 1 or 2 to enable PTC to override default temperature compensation.
PTP	V/°K	0.0	Junction potential PHP temperature coefficient. Set TLEVC to 1 or 2 to enable PTP to override default temperature compensation.
TCV	V/°K	0.0	Threshold voltage temperature coefficient. Typical values are +1mV for n-channel and -1mV for p-channel.
TLEV		0.0	Temperature equation level selector. Set TLEV=1 for ASPEC style – default is SPICE style. When you invoke the ASPEC option, the program sets TLEV for ASPEC.
TLEVC		0.0	Temperature equation level selector for junction capacitances and potentials, interacts with TLEV. Set TLEVC=1 for ASPEC style. Default is SPICE style. When you invoke the ASPEC option, the program sets TLEVC for ASPEC.
TRD	1/°K	0.0	Temperature coefficient for drain resistor
TRS	1/°K	0.0	Temperature coefficient for source resistor

Name (Alias)	Units	Default	Description
XTI		0.0	Saturation current temperature exponent. Use XTI=3 for silicon diffused junction. Set XTI=2 for Schottky barrier diode.

Using MOS Temperature Coefficient Sensitivity Parameters

Model levels 13 (BSIM1), 39 (BSIM2), and 28 (METAMOS) have length and width sensitivity parameters associated with them as shown in the following table. These parameters are used in conjunction with the Automatic Model Selector capability and enable more accurate modeling for various device sizes. The default value of each sensitivity parameter is zero to ensure backward compatibility.

Parameter	Description	Sensitivity Parameters		
		Length	Width	Product
BEX	Low field mobility, UO, temperature exponent	LBEX	WBEX	PBEX
FEX	Velocity saturation temperature exponent	LFEX	WFEX	PFEX
TCV	Threshold voltage temperature coefficient	LTCV	WTCV	PTCV
TRS	Temperature coefficient for source resistor	LTRS	WTRS	PTRS
TRD	Temperature coefficient for drain resistor	LTRD	WTRD	PTRD

Using Temperature Equations

This section describes how to use temperature equations.

Calculating Energy Gap Temperature Equations

To determine energy gap for temperature compensation use the equations:

TLEV = 0 or 1:

$$\text{egnom} = 1.16 - 7.02\text{e}{-4} \cdot \frac{\text{tnom}^2}{\text{tnom} + 1108.0}$$

$$\text{eg(t)} = 1.16 - 7.02\text{e}{-4} \cdot \frac{\text{t}^2}{\text{t} + 1108.0}$$

TLEV = 2:

$$\text{egnom} = \text{EG} - \text{GAP1} \cdot \frac{\text{tnom}^2}{\text{tnom} + \text{GAP2}}$$

$$\text{eg(t)} = \text{EG} - \text{GAP1} \cdot \frac{\text{t}^2}{\text{t} + \text{GAP2}}$$

Calculating Saturation Current Temperature Equations

$$\text{isbd(t)} = \text{isbd(tnom)} \cdot \text{e}^{facln/\text{N}}$$

$$\text{isbs(t)} = \text{isbs(tnom)} \cdot \text{e}^{facln/\text{N}}$$

where

$$\text{facln} = \frac{\text{egnom}}{\text{vt(tnom)}} - \frac{\text{eg(t)}}{\text{vt(t)}} + \text{XTI} \cdot \ln\left(\frac{\text{t}}{\text{tnom}}\right)$$

These *isbd* and *isbs* are defined in ‘MOSFET Diode Models” on page 8-27.

Calculating MOS Diode Capacitance Temperature Equations

TLEVC selects the temperature equation level for MOS diode capacitance.

TLEVC=0:

$$PB(t) = PB \cdot \left(\frac{t}{tnom}\right) - vt(t) \cdot \left[3 \cdot \ln\left(\frac{t}{tnom}\right) + \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)}\right]$$

$$PHP(t) = PHP \cdot \left(\frac{t}{tnom}\right) - vt(t) \cdot \left[3 \cdot \ln\left(\frac{t}{tnom}\right) + \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)}\right]$$

$$CBD(t) = CBD \cdot \left[1 + MJ \cdot \left(400u \cdot \Delta t - \frac{PB(t)}{PB} + 1\right)\right]$$

$$CBS(t) = CBS \cdot \left[1 + MJ \cdot \left(400u \cdot \Delta t - \frac{PB(t)}{PB} + 1\right)\right]$$

$$CJ(t) = CJ \cdot \left[1 + MJ \cdot \left(400u \cdot \Delta t - \frac{PB(t)}{PB} + 1\right)\right]$$

$$CJSW(t) = CJSW \cdot \left[1 + MJSW \cdot \left(400u \cdot \Delta t - \frac{PHP(t)}{PHP} + 1\right)\right]$$

TLEVC=1:

$$PB(t) = PB - PTA \cdot \Delta t$$

$$PHP(t) = PHP - PTP \cdot \Delta t$$

$$CBD(t) = CBD \cdot (1 + CTA \cdot \Delta t)$$

$$CBS(t) = CBS \cdot (1 + CTA \cdot \Delta t)$$

$$CJ = CJ \cdot (1 + CTA \cdot \Delta t)$$

$$CJSW = CJSW \cdot (1 + CTP \cdot \Delta t)$$

TLEVC=2:

$$PB(t) = PB - PTA \cdot \Delta t$$

$$PHP(t) = PHP - PTP \cdot \Delta t$$

$$CBD(t) = CBD \cdot \left(\frac{PB}{PB(t)}\right)^{MJ}$$

$$CBS(t) = CBS \cdot \left(\frac{PB}{PB(t)}\right)^{MJ}$$

$$CJ(t) = CJ \cdot \left(\frac{PB}{PB(t)}\right)^{MJ}$$

$$CJSW(t) = CJSW \cdot \left(\frac{PHP}{PHP(t)}\right)^{MJSW}$$

TLEVC=3:

$$PB(t) = PB + dpbdt \cdot \Delta t$$

$$PHP(t) = PHP + dphpdt \cdot \Delta t$$

$$CBD(t) = CBD \cdot \left(1 - 0.5 \cdot dpbdt \cdot \frac{\Delta t}{PB}\right)$$

$$CBS(t) = CBS \cdot \left(1 - 0.5 \cdot dpbdt \cdot \frac{\Delta t}{PB}\right)$$

$$CJ(t) = CJ \cdot \left(1 - 0.5 \cdot dpbdt \cdot \frac{\Delta t}{PB}\right)$$

$$CJSW(t) = CJSW \cdot \left(1 - 0.5 \cdot dphpdt \cdot \frac{\Delta t}{PHP}\right)$$

where for TLEV=0 or 1:

$$dpbdt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (1.16 - egnom) \cdot \left(2 - \frac{tnom}{tnom + 1108}\right) - PB\right]}{tnom}$$

$$dphpdt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (1.16 - egnom) \cdot \left(2 - \frac{tnom}{tnom + 1108}\right) - PHP\right]}{tnom}$$

TLEV=2:

$$dpbdt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (EG - egnom) \cdot \left(2 - \frac{tnom}{tnom + GAP2}\right) - PB\right]}{tnom}$$

$$dphpdt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (EG - egnom) \cdot \left(2 - \frac{tnom}{tnom + GAP2}\right) - PHP\right]}{tnom}$$

Calculating Surface Potential Temperature Equations

TLEVC=0:

$$PHI(t) = PHI \cdot \left(\frac{t}{tnom}\right) - vt(t) \cdot \left[3 \cdot \ln\left(\frac{t}{tnom}\right) + \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)}\right]$$

TLEVC=1:

$$PHI(t) = PHI - PTC \cdot \Delta t$$

If the PHI parameter is not specified, it is calculated as:

$$PHI(t) = 2 \cdot vt(t) \cdot \ln\left(\frac{NSUB}{ni}\right)$$

The intrinsic carrier concentration, ni, must be temperature updated, and it is calculated from the silicon bandgap at room temperature.

$$ni = 145e16 \cdot \left(\frac{t}{tnom}\right)^{3/2} \cdot \exp\left[EG \cdot \left(\frac{t}{tnom} - 1\right) \cdot \left(\frac{1}{2 \cdot vt(t)}\right)\right]$$

TLEVC=2:

$$PHI(t) = PHI - PTC \cdot \Delta t$$

TLEVC=3:

$$PHI(t) = PHI + dphidt \cdot \Delta t$$

where TLEV=0 or 1:

$$dphidt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (1.16 - egnom) \cdot \left(2 - \frac{tnom}{tnom + 1108}\right) - PHI\right]}{tnom}$$

TLEV=2:

$$dphidt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (EG - egnom) \cdot \left(2 - \frac{tnom}{tnom + GAP2}\right) - PHI\right]}{tnom}$$

Calculating Threshold Voltage Temperature Equations

The threshold temperature equations are:

TLEV=0:

$$vbi(t) = vbi(tnom) + \frac{PHI(t) - PHI}{2} + \frac{egnom - eg(t)}{2}$$

$$VTO(t) = vbi(t) + GAMMA \cdot (PHI(t))^{1/2}$$

TLEV=1:

$$VTO(t) = VTO - TCV \cdot \Delta t$$

$$vbi(t) = VTO(t) - GAMMA \cdot (PHI(t))^{1/2}$$

TLEV=2:

$$VTO(t) = VTO + \left(1 + \frac{GAMMA}{2 \cdot PHI^{1/2}}\right) \cdot dphidt \cdot \Delta t$$

$$vbi(t) = VTO(t) - GAMMA \cdot (PHI(t))^{1/2}$$

Calculating Mobility Temperature Equations

The MOS mobility temperature equations are:

$$UO(t) = UO \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$KP(t) = KP \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$F1(t) = F1 \cdot \left(\frac{t}{tnom}\right)^{F1EX}$$

Calculating Channel Length Modulation Temperature Equation

The LAMBDA is modified with temperature if model parameter LAMEX is specified.

$$LAMBDA(t) = LAMBDA \cdot (1 + LAMEX \cdot \Delta t$$

Calculating Diode Resistance Temperature Equations

The following equation is an example of effective drain and source resistance:

$$RD(t) = RS \cdot (1 + TRD \cdot \Delta t)$$
$$RS(t) = RS \cdot (1 + TRS \cdot \Delta t)$$

Avant!

Chapter 9

Selecting MOSFET Models: Level 1-40

Now that you know more about MOSFET models from Chapter 8, “Introducing MOSFETs.”, you can more easily choose which type of models you require for your needs.

This chapter lists various MOSFET models, and provides the specifications for each model. This chapter includes the following topics:

The remaining True-Hspice MOSFET models are described in Chapter 10, “Selecting MOSFET Models: Level 47-63.”

LEVEL 1 IDS: Schichman-Hodges Model

This section describes the parameters and equations for the LEVEL 1 IDS: Schichman-Hodges model.

LEVEL 1 Model Parameters

The LEVEL 1 model parameters follow.

Basic Model Parameters

Name (Alias)	Units	Default	Description
LEVEL		1.0	DC model selector. LEVEL 1 is the Schichman-Hodges model.
COX	F/m^2	3.453e-4	Oxide capacitance per unit gate area. If COX is not specified, it is calculated from TOX.
KP (BET, BETA)	A/V^2		Intrinsic transconductance parameter. If KP is not specified and UO and TOX are entered, the parameter is computed from: $KP = UO \cdot COX$ The default=2.0718e-5 (NMOS), 8.632e-6 (PMOS).
LAMBDA (LAM, LA)	V^{-1}	0.0	Channel-length modulation
TOX	m	1e-7	Gate oxide thickness
UO	$cm^2/(V \cdot s)$		Carrier mobility

Effective Width and Length Parameters

Name (Alias)	Units	Default	Description
DEL	m	0.0	Channel length reduction on each side. $DEL_{scaled} = DEL \cdot SCALM$
LD (DLAT, LATD)	m		Lateral diffusion into channel from source and drain diffusion. ■ If LD and XJ are unspecified: LD Default=0.0 ■ If LD is unspecified but XJ is specified, LD is calculated as: LD Default=0.75 · XJ $LD_{scaled} = LD \cdot SCALM$
LDAC	m		This parameter is the same as LD, but if LDAC is in the .MODEL statement, it replaces LD in the Leff calculation for AC gate capacitance.
LMLT		1.0	Length shrink factor
WD	m	0.0	Lateral diffusion into channel from bulk along width $WD_{scaled} = WD \cdot SCALM$
WDAC	m		This parameter is the same as WD, but if WDAC is in the .MODEL statement, it replaces WD in the Weff calculation for AC gate capacitance.
WMLT		1.0	Diffusion layer and width shrink factor

Name (Alias)	Units	Default	Description
XJ	m	0.0	Metallurgical junction depth: $XJ_{scaled} = XJ \cdot SCALM$
XL (DL, (LDEL)	m	0.0	Accounts for masking and etching effects: $XL_{scaled} = XL \cdot SCALM$
XW (DW, WDEL)	m	0.0	Accounts for masking and etching effects: $XW_{scaled} = XW \cdot SCALM$

Threshold Voltage Parameters

Name (Alias)	Units	Default	Description
GAMMA	$V^{1/2}$	0.5276	Body effect factor. If GAMMA is not specified, it is calculated from NSUB (See ‘Common Threshold Voltage Equations” on page 8-52).
NFS (DFS, NF, DNF)	$cm^{-2}.V^{-1}$	0.0	Fast surface state density
NSUB (DNB, NB)	cm^{-3}	1e15	Bulk surface doping. NSUB is calculated from GAMMA if not specified.
PHI	V	0.576	Surface inversion potential –PH is calculated from NSUB if not specified (See ‘Common Threshold Voltage Equations” on page 8-52).
VTO (VT)	V		Zero-bias threshold voltage. If not specified, it is calculated. (See ‘Common Threshold Voltage Equations” on page 8-52).

The LEVEL 1 MOSFET model should be used when accuracy is less important than simulation turn-around time. For digital switching circuits, especially when only a “qualitative” simulation of timing and function is needed, LEVEL 1 run-time can be about half that of a simulation using the LEVEL 2 model. The agreement in timing is approximately 10%. The LEVEL 1 model, however, results in severe inaccuracies in DC transfer functions of TTL-compatible input buffers, if these buffers are present in the circuit.

The channel-length modulation parameter LAMBDA is equivalent to the inverse of the Early voltage for the bipolar transistor. LAMBDA is a measure of the output conductance in saturation. When this parameter is specified, the MOSFET has a finite but constant output conductance in saturation. If LAMBDA is not input, the LEVEL 1 model assumes zero output conductance.

LEVEL 1 Model Equations

The LEVEL 1 model equations follow.

IDS Equations

In the LEVEL 1 model the carrier mobility degradation and the carrier saturation effect and weak inversion model are not included. This model determines the DC current as follows:

Cutoff Region, $v_{gs} \leq v_{th}$

$$I_{ds} = 0.0$$

Linear Region, $v_{ds} < v_{gs} - v_{th}$

$$I_{ds} = KP \cdot \frac{W_{eff}}{L_{eff}} \cdot (1 + LAMBDA \cdot v_{ds}) \cdot \left(v_{gs} - v_{th} - \frac{v_{ds}}{2}\right) \cdot v_{ds}$$

Saturation Region, $v_{ds} \geq v_{gs} - v_{th}$

$$I_{ds} = \frac{KP}{2} \cdot \frac{W_{eff}}{L_{eff}} \cdot (1 + LAMBDA \cdot v_{ds}) \cdot (v_{gs} - v_{th})^2$$

Effective Channel Length and Width

The model calculates the effective channel length and width from the drawn length and width as follows:

$$L_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2 \cdot (LD_{scaled} + DEL_{scaled})$$
$$W_{eff} = M \cdot (W_{scaled} WMLT + XW_{scaled} - 2 \cdot WD_{scaled})$$

Threshold Voltage, v_{th}

$v_{sb} \geq 0$

$$v_{th} = v_{bi} + GAMMA \cdot (PHI + v_{sb})^{1/2}$$

$v_{sb} < 0$

$$v_{th} = v_{bi} + GAMMA \cdot \left(PHI^{1/2} + 0.5 \frac{v_{sb}}{PHI^{1/2}} \right)$$

Where the built-in voltage v_{bi} is defined as:

$$v_{bi} = v_{fb} + PHI$$

or

$$v_{bi} = VTO - GAMMA \cdot PHI^{1/2}$$

Note: See 'Common Threshold Voltage Equations" on page 8-52, for calculation of VTO, GAMMA, and PHI if they are not specified.

Saturation Voltage, v_{sat}

The saturation voltage for the LEVEL 1 model is due to channel pinch off at the drain side and is computed by:

$$v_{sat} = v_{gs} - v_{th}$$

In the LEVEL 1 model, the carrier velocity saturation effect is not included.

LEVEL 2 IDS: Grove-Frohman Model

This section describes the parameters and equations for the LEVEL 2 IDS: Grove-Frohman model.

LEVEL 2 Model Parameters

The LEVEL 2 model parameters follow.

Basic Model Parameters

Name (Alias)	Units	Default	Description
LEVEL		1.0	DC model selector. LEVEL 2 is the Grove-Frohman model.
COX	F/m^2	3.453e-4	Oxide capacitance per unit gate area. This parameter is calculated from TOX if not specified.
ECRIT (ESAT)	V/cm	0.0	Critical electric field for carrier velocity saturation. From Grove:electrons 6e4 holes 2.4e4 Use zero to indicate an infinite value. ECRIT is preferred over VMAX because the equation is more stable. ECRIT is estimated as: $ECRIT = 100 \cdot (VMAX / UO)$
KP (BET, BETA)	A/V^2	2.0e-5	Intrinsic transconductance. If KP is not specified and UO and TOX are entered, KP is calculated from $KP = UO \cdot COX$

Name (Alias)	Units	Default	Description
LAMBDA (LAM, LA)	V^{-1}	0.0	Channel length modulation
NEFF		1.0	Total channel charge (fixed and mobile) coefficient
TOX	m	1e-7	Gate oxide thickness
VMAX (VMX, VSAT)	m/s	0.0	Maximum drift velocity of carriers. Use zero to indicate an infinite value.

Effective Width and Length Parameters

Name (Alias)	Units	Default	Description
DEL	m	0.0	Channel-length reduction on each side: $DEL_{scaled} = DEL \cdot SCALM$
LD (DLAT, *LADT)*	m		Lateral diffusion into channel from source and drain diffusion. ■ If LD and XJ are unspecified, LD default=0.0 ■ If LD is unspecified but XJ is specified, LD is calculated from: XJ. Default=0.75 · XJ $LD_{scaled} = LD \cdot SCALM$
LDAC	m		This parameter is the same as LD, but if LDAC is included in the .MODEL statement, it replaces LD in the Leff calculation for AC gate capacitance.

Name (Alias)	Units	Default	Description
LMLT		1.0	Length shrink factor
LREF	m	0.0	Channel length reference $LREF_{scaled} = LREF \cdot SCALM$
WD	m	0.0	Lateral diffusion into channel from bulk along width $WD_{scaled} = WD \cdot SCALM$
WDAC	m		This parameter is the same as WD, but if WDAC is included in the .MODEL statement, it replaces WD in the Weff calculation for AC gate capacitance.
WMLT		1.0	Diffusion layer and width shrink factor
WREF	m	0.0	Channel width reference $WREF_{scaled} = WREF \cdot SCALM$
XJ	m	0.0	Metallurgical junction depth $XJ_{scaled} = XJ \cdot SCALM$
XL (DL, LDEL)	m	0.0	Length bias accounts for masking and etching effects $XL_{scaled} = XL \cdot SCALM$
XW (DW, WDEL)	m	0.0	Width bias accounts for masking and etching effects $XW_{scaled} = XW \cdot SCALM$

Threshold Voltage Parameters

Name (Alias)	Units	Default	Description
DELTA		0.0	Narrow width factor for adjusting threshold
GAMMA	$V^{1/2}$	0.5276	Body effect factor. This parameter is calculated from NSUB if not specified (see ‘Common Threshold Voltage Equations” on page 8-52).
LND	µm/V	0.0	ND length sensitivity
LN0	µm	0.0	N0 length sensitivity
ND	V^{-1}	0.0	Drain subthreshold factor
N0		0.0	Gate subthreshold factor. Typical value=1.
NFS (DFS, NF, DNF)	$cm^{-2}.V^{-1}$	0.0	Fast surface state density
NSUB (DNB, NB)	cm^{-3}	1e15	Bulk surface doping. If NSUB is not specified, it is calculated from GAMMA.
PHI	V	0.576	Surface inversion potential. If PHI is not specified, it is calculated from NSUB (see ‘Common Threshold Voltage Equations” on page 8-52).
VTO(VT)	V		Zero-bias threshold voltage. If it is not specified, it is calculated (see ‘Common Threshold Voltage Equations” on page 8-52).
WIC		0.0	Subthreshold model selector
WND	µm/V	0.0	ND width sensitivity.
WN0	µm	0.0	N0 width sensitivity

Mobility Parameters

Name (Alias)	Units	Default	Description
MOB		0.0	Mobility equation selector. This parameter can be set to MOB=0 or MOB=7. If MOB=7, the model is changed, which also affects the channel length calculation. **Note:** MOB=7 operates as a flag. It invokes the channel length modulation and mobility equations of MOSFET LEVEL 3.
THETA	V^{-1}	0.0	Mobility modulation. THETA is used only when MOB=7. A typical value in this application is THETA=5e-2.
UCRIT	V/cm	1.0e4	Critical field for mobility degradation, UCRIT. The parameter is the limit at which the surface mobility UO begins to decrease in accordance with the empirical relation given later.
UEXP (F2)		0.0	Critical field exponent in the empirical formula which characterizes surface mobility degradation
UO (UB, UBO)	$cm^2/(V \cdot s)$	600 (N) 250 (P)	Low-field bulk mobility. This parameter is calculated from KP if KP is input.

Name (Alias)	Units	Default	Description
UTRA		0.0	Transverse field coefficient **Note:** Standard SPICE does not use UTRA. Avant! in-circuit simulators, such as Star-Hspice and Star-Sim (and their XT versions), can use it if supplied, but simulation issues a warning, because UTRA can hinder convergence.

The mobility parameters are best determined by curve fitting. In most cases UTRA should be specified between 0.0 and 0.5. Nonzero values for UTRA can result in negative resistance regions at the onset of saturation.

LEVEL 2 Model Equations

The LEVEL 2 model equations follow.

IDS Equations

The following section describes the way the LEVEL 2 MOSFET model calculates the drain current of n-channel and p-channel MOSFETs.

Cutoff Region, $v_{gs} \leq v_{th}$

$$I_{ds} = 0 \quad \textit{(see subthreshold current)}$$

On Region, $v_{gs}>v_{th}$

$$I_{ds} = \beta \cdot \left\{ \left(v_{gs} - v_{bi} - \frac{\eta \cdot v_{de}}{2} \right) \cdot v_{de} - \frac{2}{3} \cdot \gamma \cdot [(PHI + v_{de} + v_{sb})^{3/2} - (PHI + v_{sb})^{3/2}] \right\}$$

where:

$$v_{de} = \min(v_{ds}, v_{dsat})$$

$$\eta = 1 + DELTA \cdot \frac{\pi \cdot \varepsilon si}{4 \cdot COX \cdot W_{eff}}$$

$$\beta = KP \cdot \frac{W_{eff}}{L_{eff}}$$

Effective Channel Length and Width

The model calculates effective channel length and width from the drawn length and width as follows:

$$L_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2 \cdot (LD_{scaled} + DEL_{scaled})$$

$$W_{eff} = M \cdot (W_{scaled} \cdot WMLT + XW_{scaled} - 2 \cdot WD_{scaled})$$

$$LREF_{eff} = LREF_{scaled} \cdot LMLT + XL_{scaled} - 2 \cdot (LD_{scaled} + DEL_{scaled})$$

$$WREF_{eff} = M \cdot (WREF_{scaled} \cdot WMLT + XW_{scaled} - 2 \cdot WD_{scaled})$$

Threshold Voltage, *v_{th}*

The model parameter VTO is an extrapolated zero-bias threshold voltage of a large device. The effective threshold voltage, including the device size effects and the terminal voltages, is calculated by:

$$v_{th} = v_{bi} + \gamma \cdot (PHI + v_{sb})^{1/2}$$

where:

$$v_{bi} = VTO - GAMMA \cdot (PHI)^{1/2} + (\eta - 1) \cdot (PHI + v_{sb})$$

The narrow width effect is included through v_{bi} and η . To include the narrow width effect, specify the model parameter DELTA. The short-channel effect is included through the effective γ . To include short-channel effects, the model parameter XJ must be greater than zero. Then:

$$\gamma = GAMMA \cdot \left\{ 1 - \frac{XJ_{scaled}}{2 \cdot L_{eff}} \cdot \left[\left(1 + \frac{2 \cdot W_s}{XJ_{scaled}} \right)^{1/2} + \left(1 + \frac{2 \cdot W_d}{XJ_{scaled}} \right)^{1/2} - 2 \right] \right\}$$

The depletion widths, W_s and W_d, are determined by:

$$W_s = \left[\frac{2 \cdot E_{si}}{q \cdot NSUB} \cdot (PHI + v_{sb}) \right]^{1/2}$$

$$W_d = \left[\frac{2 \cdot E_{si}}{q \cdot NSUB} \cdot (PHI + v_{ds} + v_{sb}) \right]^{1/2}$$

Simulation calculates parameters such as VTO, GAMMA, and PHI unless you specify them. The model uses these parameters to calculate threshold voltage. (See ‘Common Threshold Voltage Equations” on page 8-52).

Saturation Voltage, v_{dsat}

If you do not specify the model parameter VMAX, the program computes the saturation voltage due to channel pinch off at the drain side. By including the corrections for small-size effects, v_{sat} is:

$$v_{sat} = \frac{v_{gs} - v_{bi}}{\eta} + \frac{1}{2}\left(\frac{\gamma}{\eta}\right)^2 \cdot \left\{1 - \left[1 + 4 \cdot \left(\frac{\eta}{\gamma}\right)^2 \cdot \left(\frac{v_{gs} - v_{bi}}{\eta} + PHI + v_{sb}\right)\right]^{1/2}\right\}$$

$$v_{dsat} = v_{sat}$$

If you specify ECRIT, the program modifies v_{sat} to include carrier velocity saturation effect.

$$v_{dsat} = v_{sat} + v_c - (v_{sat}^2 + v_c^2)^{1/2}$$

where:

$$v_c = ECRIT \cdot L_{eff}$$

Note: If VMAX is specified, a different v_{dsat} calculation is performed. Refer to the Vladimirescu document[1.] for details.

Mobility Reduction, u_{eff}

The mobility of carriers in the channel decreases as the carriers' speeds approach their scattering limited velocity. The mobility degradation for the LEVEL 2 MOS model uses two different equations, depending on the mobility equation selector value of MOB.

If MOB=0, (default):

$$\mu_{eff} = UO \cdot \left[\frac{UCRIT \cdot E_{si}}{COX \cdot (v_{gs} - v_{th} - UTRA \cdot v_{ds})}\right]^{UEXP}$$

Because u_{eff} is less than UO, the program uses the above equation if the bracket term is less than one; otherwise the program uses u_{eff}=UO.

If MOB=7, THETA≠0

$$u_{eff} = \frac{UO}{1 + THETA \cdot (v_{gs} - v_{th})}$$

$v_{gs}<v_{th}$, u_{eff} = UO

If MOB=7, THETA=0

$$u_{eff} = UO \cdot \left[\frac{UCRIT \cdot E_{si}}{COX \cdot (v_{gs} - v_{th})}\right]^{UEXP}$$

If MOB=7, VMAX>0

$$u_{eff} = \frac{u_{eff}}{1 + u_{eff} \cdot \frac{vde}{VMAX \cdot L_{eff}}}$$

Channel Length Modulation

The LEVEL 2 MOS model includes the channel length modulation effect by modifying the I_{ds} current as follows:

$$I_{ds} = \frac{I_{ds}}{1 - \lambda \cdot v_{ds}}$$

The model calculates the value of λ if you do not specify the LAMBDA model parameter.

LAMBDA>0

$$\lambda = LAMBDA$$

VMAX>0, NSUB >0, and LAMBDA ≤0

$$\lambda = \frac{X_d}{NEFF^{1/2} \cdot L_{eff} \cdot v_{ds}} \cdot \left\{\left[\left(\frac{VMAX \cdot X_d}{2 \cdot NEFF^{1/2} \cdot u_{eff}}\right)^2 + v_{ds} - v_{dsat}\right]^{1/2} - \frac{VMAX \cdot X_d}{2 \cdot NEFF^{1/2} \cdot u_{eff}}\right\}$$

VMAX=0, NSUB>0, and LAMBDA ≤0

If MOB=0

$$\lambda = \frac{X_d}{L_{eff} \cdot v_{ds}} \cdot \left\{ \frac{v_{ds} - v_{dsat}}{4} + \left[1 + \left(\frac{v_{ds} - v_{dsat}}{4} \right)^2 \right]^{1/2} \right\}^{1/2}$$

If MOB=7

$$\lambda = \frac{X_d}{L_{eff} \cdot v_{ds}} \cdot \left\{ \left[\frac{v_{ds} - v_{dsat}}{4} + \left(1 + \left(\frac{v_{ds} - v_{dsat}}{4} \right)^2 \right)^{1/2} \right]^{1/2} - 1 \right\}$$

where X_d is defined by:

$$X_d = \left(\frac{2 \cdot E_{si}}{q \cdot NSUB} \right)^{1/2}$$

The above equations do not include the effect of the field between gate and drain and gate and pinch-off point, respectively. They tend to overestimate the output conductance in the saturation region.

The modification of I_{ds} by factor $(1 - \lambda \cdot v_{ds})$ is equivalent to replacing Leff with:

$$Le = L_{eff} - \lambda \cdot v_{ds} \cdot L_{eff}$$

To prevent the channel length (Le) from becoming negative, the value of Le is limited.

If Le < xwb, then Le is replaced by:

$$\frac{xwb}{1 + \frac{xwb - Le}{xwb}}$$

where:

$$xwb = X_d \cdot PB^{1/2}$$

Subthreshold Current, I_{ds}

This region of operation is characterized by the fast surface states model parameter, NFS. For NFS>0 the model determines the modified threshold voltage (von) as follows:

$$von = v_{th} + fast$$

where:

$$fast = vt \cdot \left[\eta + (PHI + v_{sb})^{1/2} \cdot \frac{\partial \gamma}{\partial v_{sb}} + \frac{\gamma}{2 \cdot (PHI + v_{sb})^{1/2}} + \frac{q \cdot NFS}{COX} \right]$$

and vt is the thermal voltage.

The I_{ds} current for v_{gs}<von is given by:

$$I_{ds} = I_{ds}(von, vde, v_{sb}) \cdot e^{\frac{v_{gs} - von}{fast}}$$

$v_{gs} \geq von$

$$I_{ds} = I_{ds}(v_{gs}, vde, v_{sb})$$

where:

$$vde = \min(v_{ds}, v_{dsat})$$

Note: The modified threshold voltage (von), due to NFS specification, is also used in strong inversion instead of v_{th}, mainly in the mobility equations.

If WIC=3, the model calculates the subthreshold current differently. In this case the I_{ds} current is:

$$I_{ds} = I_{ds}(v_{gs}, vde, v_{sb}) + isub(N0_{eff}, ND_{eff}, v_{gs}, v_{ds})$$

The $N0_{eff}$ and ND_{eff} are functions of effective device width and length.

LEVEL 3 IDS: Empirical Model

This sections provides the LEVEL 3 IDS: Empirical model parameters and equations.

LEVEL 3 Model Parameters

The LEVEL 3 model parameters follow.

Basic Model Parameters

Name (Alias)	Units	Default	Description
LEVEL		1.0	DC model selector. LEVEL=3 is an empirical model.
COX	F/m^2	3.453e-4	Oxide capacitance per unit gate area. If this parameter is not specified, it is calculated from TOX.
DERIV		1	Derivative method selector: ■ DERIV=0: analytic ■ DERIV=1: finite difference
KAPPA	V^{-1}	0.2	Saturation field factor. The channel length modulation equation uses this parameter.
KP (BET, BETA)	A/V^2	2.0e-5	Intrinsic transconductance parameter. If this parameter is not specified and UO and TOX are entered, KP is calculated from $KP = UO \cdot COX$
TOX	m	1e-7	Gate oxide thickness
VMAX (VMX)	m/s	0.0	Maximum drift velocity of carriers. Use zero to indicate an infinite value.

Effective Width and Length Parameters

Name (Alias)	Units	Default	Description
DEL	m	0.0	Channel length reduction on each side $DEL_{scaled} = DEL \cdot SCALM$
LD (DLAT, (LATD)	m		Lateral diffusion into channel from source and drain diffusion, ■ If LD and XJ are unspecified, LD Default= 0.0 ■ If LD is unspecified but XJ is specified, LD is calculated from XJ as $LD = 0.75 \cdot XJ$
LDAC	m		This parameter is the same as LD, but if LDAC is included in the .MODEL statement, it replaces LD in the Leff calculation for AC gate capacitance.
LREF	m	0.0	Channel length reference $LREF_{scaled} = LREF \cdot SCALM$
LMLT		1.0	Length shrink factor
WD	m	0.0	Lateral diffusion into channel width from bulk $WD_{scaled} = WD \cdot SCALM$
WDAC	m		This parameter is the same as WD, but if WDAC is included in the .MODEL statement, it replaces WD in the Weff calculation for AC gate capacitance.
WMLT		1.0	Diffusion layer and width shrink factor

Name (Alias)	Units	Default	Description
WREF	m	0.0	Channel width reference $WREF_{scaled} = WREF \cdot SCALM$
XJ	m	0.0	Metallurgical junction depth $XJ_{scaled} = XJ \cdot SCALM$
XL (DL, LDEL)	m	0.0	Length bias accounts for masking and etching effects $XL_{scaled} = XL \cdot SCALM$
XW (DW, WDEL)	m	0.0	Width bias accounts for masking and etching effects $XW_{scaled} = XW \cdot SCALM$

Threshold Voltage Parameters

Name (Alias)	Units	Default	Description
DELTA		0.0	Narrow width factor for adjusting threshold
ETA		0.0	Static feedback factor for adjusting threshold
GAMMA	$V^{1/2}$	0.5276	Body effect factor. This parameter is calculated from NSUB if not specified (See ‘Common Threshold Voltage Equations” on page 8-52).
LND	µm/V	0.0	ND length sensitivity
LN0	µm	0.0	N0 length sensitivity
ND	V^{-1}	0.0	Drain subthreshold factor

Name (Alias)	Units	Default	Description
N0		0.0	Gate subthreshold factor (typical value=1)
NFS (DFS,NF, DNF)	$cm^{-2}{\cdot}V^{-1}$	0.0	Fast surface state density
NSUB (DNB, NB)	cm^{-3}	1e15	Bulk surface doping. This parameter is calculated from GAMMA if not specified.
PHI	V	0.576	Surface inversion potential. This parameter is calculated from NSUB if not specified (see ‘Common Threshold Voltage Equations” on page 8-52).
VTO (VT)	V		Zero-bias threshold voltage. This parameter is calculated if not specified (see ‘Common Threshold Voltage Equations” on page 8-52).
WIC		0.0	Sub-threshold model selector
WND	µm/V	0.0	ND width sensitivity
WN0	µm	0.0	N0 width sensitivity

Mobility Parameters

Name (Alias)	Units	Default	Description
THETA	V^{-1}	0.0	Mobility degradation factor
UO (UB,UBO)	$cm^2/(V{\cdot}s)$	600(N) 250(P)	Low field bulk mobility. This parameter is calculated from KP if KP is specified.

LEVEL 3 Model Equations

The LEVEL 3 model equations follow.

IDS Equations

The following describes the way the LEVEL 3 MOSFET model calculates the drain current, I_{ds}.

Cutoff Region, $v_{gs} \leq v_{th}$

$$I_{ds} = 0 \quad \textit{(See subthreshold current)}$$

On Region, $v_{gs} > v_{th}$

$$I_{ds} = \beta \cdot \left(v_{gs} - v_{th} - \frac{1 + fb}{2} \cdot vde \right) \cdot vde$$

where:

$$\beta = KP \cdot \frac{W_{eff}}{L_{eff}}$$

$$= u_{eff} \cdot COX \cdot \frac{W_{eff}}{L_{eff}}$$

$$vde = \min(v_{ds}, v_{dsat})$$

and:

$$fb = f_n + \frac{GAMMA \cdot f_s}{4 \cdot (PHI + v_{sb})^{1/2}}$$

Note: In the above equation the factor 4 should be 2, but because SPICE uses a factor of 4, this model uses a factor of 4 as well.

The narrow width effect is included through the f_n parameter:

$$f_n = \frac{DELTA}{W_{eff}} \cdot \frac{1}{4} \cdot \frac{2\pi \cdot E_{si}}{COX}$$

The term f_s expresses the effect of the short channel and is determined as:

$$f_s = 1 - \frac{XJ_{scaled}}{L_{eff}} \cdot \left\{ \frac{LD_{scaled} + W_c}{XJ_{scaled}} \cdot \left[1 - \left(\frac{W_p}{XJ_{scaled} + W_p} \right)^2 \right]^{1/2} - \frac{LD_{scaled}}{XJ_{scaled}} \right\}$$

$$W_p = X_d \cdot (PHI + v_{sb})^{1/2}$$

$$X_d = \left(\frac{2 \cdot E_{si}}{q \cdot NSUB} \right)^{1/2}$$

$$W_c = XJ_{scaled} \cdot \left[0.0631353 + 0.8013292 \cdot \left(\frac{W_p}{XJ_{scaled}} \right) - 0.01110777 \cdot \left(\frac{W_p}{XJ_{scaled}} \right)^2 \right]$$

Effective Channel Length and Width

The model determines effective channel length and width in the LEVEL 3 model as follows:

$$L_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2 \cdot (LD_{scaled} + DEL_{scaled})$$

$$W_{eff} = M \cdot (W_{scaled} \cdot WMLT + XW_{scaled} - 2 \cdot WD_{scaled})$$

$$LREFF = LREF_{scaled} \cdot LMLT + XL_{scaled} - 2 \cdot (LD_{scaled} + DEL_{scaled})$$

$$WREF_{eff} = M \cdot (WREF_{scaled} \cdot WMLT + XW_{scaled} - 2 \cdot WD_{scaled})$$

Threshold Voltage, v_{th}

The effective threshold voltage, including the device size and terminal voltage effects, is calculated by:

$$v_{th} = v_{bi} - \frac{8.14e\text{-}22 \cdot ETA}{COX \cdot L_{eff}^3} \cdot v_{ds} + GAMMA \cdot f_s \cdot (PHI + v_{sb})^{1/2} + f_n \cdot (PHI + v_{sb})$$

where:

$$v_{bi} = v_{fb} + PHI$$

or

$$v_{bi} = VTO - GAMMA \cdot PHI^{1/2}$$

The VTO is the extrapolated zero-bias threshold voltage of a large device. If VTO, GAMMA, and PHI are not specified, simulation computes them (see ‘Common Threshold Voltage Equations” on page 8-52).

Saturation Voltage, v_{dsat}

The LEVEL 3 model determines saturation voltage due to channel pinch-off at the drain side. The model uses the VMAX parameter to include the reduction of the saturation voltage due to carrier velocity saturation effect.

$$v_{sat} = \frac{v_{gs} - v_{th}}{1 + f_b}$$

$$v_{dsat} = v_{sat} + v_c - (v_{sat}^2 + v_c^2)^{1/2}$$

where:

$$v_c = \frac{VMAX \cdot L_{eff}}{us}$$

The surface mobility parameter “us” is defined in the next section. If the model parameter VMAX is not specified, then:

$$v_{dsat} = v_{sat}$$

Effective Mobility, u_{eff}

The model defines the carrier mobility reduction due to the normal field as the effective surface mobility (us).

$v_{gs}>v_{th}$

$$us = \frac{UO}{1 + THETA \cdot (v_{gs} - v_{th})}$$

The model determines the degradation of mobility due to the lateral field and the carrier velocity saturation if you specify the VMAX model parameter.

VMAX>0

$$u_{eff} = \frac{us}{1 + \frac{vde}{v_c}}$$

otherwise,

$$u_{eff} = us$$

Channel Length Modulation

For $v_{ds}>v_{dsat}$, the channel length modulation factor is computed. The model determines the channel length reduction (ΔL) differently, depending on the VMAX model parameter value.

VMAX = 0

$$\Delta L = X_d \cdot [KAPPA \cdot (v_{ds} - v_{dsat})]^{1/2}$$

VMAX>0

$$\Delta L = -\frac{E_p \cdot X_d^2}{2} + \left[\left(\frac{E_p \cdot X_d^2}{2}\right)^2 + KAPPA \cdot X_d^2 \cdot (v_{ds} - v_{dsat})\right]^{1/2}$$

where E_p is the lateral electric field at the pinch off point. Its value is approximated by:

$$E_p = \frac{v_c \cdot (v_c + v_{dsat})}{L_{eff} \cdot v_{dsat}}$$

The current I_{ds} in the saturation region is computed as:

$$I_{ds} = \frac{I_{ds}}{1 - \frac{\Delta L}{L_{eff}}}$$

In order to prevent the denominator from going to zero, the ΔL value is limited, as follows:

If

$$\Delta L > \frac{L_{eff}}{2}$$

then

$$\Delta L = L_{eff} - \frac{\left(\frac{L_{eff}}{2}\right)^2}{\Delta L}$$

Subthreshold Current, I_{ds}

This region of operation is characterized by the model parameter for fast surface state (NFS). The modified threshold voltage (von) is determined as follows:

NFS>0

$$von = v_{th} + fast$$

where:

$$fast = v_{tm} \cdot \left[1 + \frac{q \cdot NFS}{COX} + \frac{GAMMA \cdot f_s \cdot (PHI + v_{sb})^{1/2} + f_n \cdot (PHI + v_{sb})}{2 \cdot (PHI + v_{sb})}\right]$$

The current I_{ds} is given by:

v_{gs}<von

$$I_{ds} = I_{ds}(von, vde, v_{sb}) \cdot e^{\frac{v_{gs} - von}{fast}}$$

v_{gs} von

$$I_{ds} = I_{ds}(v_{gs}, vde, v_{sb})$$

Note: The model does not use the modified threshold voltage in strong inversion.

If WIC=3, the model calculates subthreshold current differently. In this case, the I_{ds} current is:

$$I_{ds} = I_{ds}(v_{gs}, vde, v_{sb}) + isub(N0_{eff}, ND_{eff}, v_{gs}, v_{ds})$$

Subthreshold current isub for LEVEL=3 is the same as for LEVEL=13 (see Subthreshold Current ids on page 9-116).

$N0_{eff}$ and ND_{eff} are functions of effective device width and length.

Compatibility Notes

This section describes compatibility issues.

Avant! True-Hspice Model versus SPICE3

Differences between the Avant! Level 3 model and Berkeley SPICE3 can arise in the following situations:

Small XJ

LEVEL 3 and SPICE3 differ for small values of XJ, typically less than 0.05 microns. Such small values for XJ are physically unreasonable and should be avoided. XJ is used to calculate the short-channel reduction of the GAMMA effect,

$$\mathrm{GAMMA} \rightarrow f_s \cdot \mathrm{GAMMA}$$

f_s is normally less than or equal to 1. For very small values of XJ, f_s can be greater than one. The Avant! Level 3 model imposes the limit $f_s \leq 1.0$, while SPICE3 allows $f_s > 1.0$.

ETA

This model uses 8.14 as the constant in the ETA equation, which provides the variation in threshold with v_{ds}. Berkeley SPICE3 uses 8.15.

Solution: To convert a SPICE3 model to Avant! True-Hspice Level 3, multiply ETA by 815/814.

NSUB Missing

When NSUB is missing in SPICE3, the KAPPA equation becomes inactive. In this model, a default NSUB is generated from GAMMA, and the KAPPA equation is active.

Solution: If NSUB is missing in the SPICE3 model, set KAPPA=0 in the Avant! Level 3 model.

LD Missing

If LD is missing, simulation uses the default 0.75·XJ. SPICE3 defaults LD to zero.

Solution: If LD is missing in the SPICE3 model, set LD=0 in the Level 3 model.

Constants

Boltzmann constant	k	= 1.3806226e-23J· K^{-1}
Electron charge	e	= 1.6021918e-19C
Permittivity of silicon dioxide	ε_{ox}	= 3.45314379969e-11F/m
Permittivity of silicon	ε_{si}	= 1.035943139907e-10F/m

Temperature Compensation

The example below verifies temperature dependence for LEVEL 3.

Input File

```
$ test of temp dependence for LEVEL=3 Tlevc=0 Tlev=1
.option ingold=2 numdgt=6
.temp 25 100
vd d 0 5
vg g 0 2
m1 d g 0 0 nch w=10u L=1u
.op
.print id=lx4(m1) vdsat=lv10(m1)
.model nch nmos LEVEL=3 tlev=1 tlevc=0 acm=3
+ uo=600 tox=172.6572
+ vto=0.8 gamma=0.8 phi=0.64
+ kappa=0 xj=0
+ nsub=1e16 rsh=0
+ tcv=1.5e-3 bex=-1.5
.end
```

This simple model, with XJ=0 and KAPPA=0, has a saturation current:

$$I_{ds} = \frac{beta \cdot 0.5 \cdot (v_{gs} - v_{tm})^2}{1 + fb}$$

$$beta = COX \cdot \left(\frac{W}{L}\right) \cdot UO(t) \quad fb = \frac{GAMMA}{(4 \cdot \sqrt{phi(t)})}$$

Using the model parameters in the input file and the equations from the previous page:

$$beta = (1.2e-3) \cdot \left(\frac{t}{tref}\right)^{BEX}$$

$$v_{tm} = 0.8 - TCV \cdot (t - tref)$$

$$phi(t) = 0.64 \cdot \left(\frac{t}{tref}\right) - vtherm \cdot \left(egarg + 3 \cdot \log\left(\frac{t}{tref}\right)\right)$$

At room temperature:

$$beta = (1.2e-3)$$

$$v_{tm} = 0.8$$

$$phi(t) = 0.64$$

$$I_{ds} = (1.2e-3) \cdot 0.5 \cdot \frac{(2 - 0.8)^2}{1 + \frac{0.2}{\sqrt{0.64}}} = 6.912e-4$$

At T=100:

$$\text{beta} = 1.2\text{e}-3 \cdot (1.251551)^{-1.5} = 0.570545\text{e}-4$$

$$v_{tm} = 0.8 - (1.5\text{e}-3) \cdot 75 = 0.6875$$

$$\text{egarg} = 9.399920 \quad \text{vtherm} = 3.215466\text{e}-2$$

$$\text{phi(t)} = 0.64 \cdot 1.251551 - 0.3238962 = 0.4770964$$

$$I_{ds} = \text{beta} \cdot 0.5 \cdot \frac{(2-\text{vt})^2}{1 + \frac{0.2}{\sqrt{\text{phi(t)}}}} = 5.724507\text{e}-4$$

Simulation results:

```
T=25, id=6.91200e-04
T=100, id=5.72451e-04
```

These results agree with the hand calculations.

LEVEL 4 IDS: MOS Model

The LEVEL 4 MOS model is the same as the LEVEL 2 model, with the following exceptions:

- No narrow width effects: $\eta = 1$
- No short-channel effects: $\gamma =$ *GAMMA*
- For lateral diffusion, $LD_{scaled} = LD \cdot XJ \cdot SCALM$. The LD default = 0.75 if XJ is specified and 0 if XJ is not specified.
- TPG, the model parameter for type of gate materials, defaults to zero (AL gate). The default is 1 for other levels. This parameter computes VTO if that model parameter is not specified (see ‘Common Threshold Voltage Equations” on page 8-52).

LEVEL 5 IDS Model

This section describes the LEVEL 5 IDS model parameters and equations.

Note: This model uses micrometer units rather than the typical meter units. Units and defaults are often unique in LEVEL 5. The option SCALM is ineffective for this level.

LEVEL 5 Model Parameters

The LEVEL 5 model parameters follow.

Basic Model Parameters

Name (Alias)	Units	Default	Description
LEVEL		1.0	Model level selector
DNB (NSUB)	cm^{-3}	0.0	Surface doping
DP	μm	1.0	Implant depth (depletion model only)
ECV	V/μm	1000	Critical field
NI	cm^{-2}	2e11	Implant doping (depletion model only)
PHI	V	0.8	Built-in potential
TOX	Å	0.0	Oxide thickness
TUH		1.5	Implant channel mobility temperature exponent (depletion model only)
ZENH		1.0	Mode flag (enhancement). Set ZENH=0.0 for depletion mode.

Effective Width and Length Parameters

Name (Alias)	Units	Default	Description
DEL (WDEL)	μm	0.0	Channel length reduction on each side
LATD (LD)	μm	1.7 · XJ	Lateral diffusion on each side
LMLT		1.0	Length shrink factor
OXETCH	μm	0.0	Oxide etch
WMLT		1.0	Diffusion layer and width shrink factor

Threshold Voltage Parameters

Name (Alias)	Units	Default	Description
FSS (NFS)	$cm^{-2}.V^{-1}$	0.0	Number of fast surface states
NWM		0.0	Narrow width modifier
SCM		0.0	Short-channel drain source voltage multiplier
VT (VTO)	V	0.0	Extrapolated threshold voltage
XJ	μm	1.5	Junction depth

Mobility Parameters

Name (Alias)	Units	Default	Description
FRC	$Å \cdot s/cm^2$	0.0	Field reduction coefficient

Name (Alias)	Units	Default	Description
FSB	$V^{1/2}·s/cm^2$	0.0	Lateral mobility coefficient
UB (UO)	$cm^2/(V·s)$	0.0	Low field bulk mobility
UH	$cm^2/(V·s)$	900 (N) 300 (P)*	Implant - channel mobility * (For depletion model only)
VST	cm/s	0.0	Saturation velocity

Capacitance Parameters

Name (Alias)	Units	Default	Description
AFC		1.0	Area factor for MOSFET capacitance
CAPOP		6	Gate capacitance selector
METO	μm	0.0	Metal overlap on gate

The LEVEL 5 MOSFET model has been expanded to include two modes: enhancement and depletion. These two modes are accessed by the flag mode parameter, ZENH.

ZENH=1 This enhancement model (default mode) is a portion of the Avant! True-Hspice MOS5, and is identical to AMI SPICE MOS LEVEL 4.

ZENH=0 This depletion model is revised in the Avant! True-Hspice (from previous depletion mode) and is identical to AMI SPICE MOS LEVEL 5.

The Avant! True-Hspice enhancement and depletion models are basically identical to the AMI models. However, certain aspects have been revised to enhance performance. Using the True-Hspice enhancement and depletion models provides access to Star-Hspice features as described below.

The Avant! True-Hspice version of the enhancement and depletion models allows the choice of either SPICE-style or ASPEC-style temperature compensation. For LEVEL 5, the default is TLEV=1, invoking ASPEC style temperature compensation. Setting TLEV=0 invokes SPICE-style temperature compensation.

CAPOP=6 represents AMI Gate Capacitance in True-Hspice. CAPOP=6 is the default setting for LEVEL 5 only. The LEVEL 5 models can also use CAPOP =1, 2, 3.

The parameter ACM defaults to 0 in LEVEL 5, invoking SPICE-style parasitics. ACM also can be set to 1 (ASPEC) or to 2 (Avant! True-Hspice). All MOSFET models follow this convention.

The True-Hspice SCALE option can be used with the LEVEL 5 model; however, option SCALM cannot be used due to the difference in units.

You *must* specify the following parameters for MOS LEVEL 5: VTO (VT), TOX, UO (UB), FRC, and NSUB (DNB).

IDS Equations

The LEVEL 5 IDS equations follow.

Cutoff Region, $v_{gs} \leq v_{th}$

$$I_{ds} = 0$$ *(See "Subthreshold Current, Ids" on page 9-43)*

On Region, v_{gs} v_{th}

$$I_{ds} = \beta \cdot \left\{ \left(v_{gs} - v_{bi} - \frac{vde}{2} \right) \cdot vde - \frac{2}{3} \cdot \gamma \cdot [(\Phi_f + vde + v_{sb})^{3/2} - (\Phi_f + v_{sb})^{3/2}] \right\}$$

where:

$$vde = \min(v_{ds}, v_{dsat})$$

$$\beta = UB_{eff} \cdot cox \cdot \frac{W_{eff}}{L_{eff}}$$

$$\Phi_f = 2 \cdot v_{tm} \cdot \ln\left(\frac{DNB}{ni}\right)$$

and gate oxide capacitances per unit area are calculated by:

$$cox = \frac{E_{ox}}{TOX \cdot 1E\text{-}10} \quad F/m$$

Effective Channel Length and Width

The effective channel length and width in the LEVEL 5 model is determined as follows.

$$W_{eff} = W_{scaled} \cdot WMLT + OXETCH$$

$$L_{eff} = L_{scaled} \cdot LMLT - 2 \cdot (LATD + DEL)$$

Threshold Voltage, v_{th}

The model parameter VTO is an extrapolated zero-bias threshold voltage of a large device. The effective threshold voltage, including the device size effects and the terminal voltages, is given by:

$$v_{th} = v_{bi} + \gamma \cdot (\Phi_f + v_{sb})^{1/2}$$

where:

$$v_{bi} = v_{fb} + \Phi_f = VTO - \gamma_0 \cdot \Phi_f^{1/2}$$

$$\gamma_0 = \frac{(2 \cdot E_{si} \cdot q \cdot DNB)^{1/2}}{cox}$$

Note: For LEVEL 5 model, you must specify DNB and VTO parameters. The Avant! True-Hspice program computes γ_0 using DNB and ignores the GAMMA model parameter.

The effective body effect (γ), including the device size effects, is computed as follows.

$$\gamma = \gamma_0 \cdot (1 - scf) \cdot (1 + ncf)$$

If SCM ≤ 0,

$$scf = 0$$

otherwise,

$$scf = \frac{XJ}{L_{eff}} \cdot \left\{ \left[1 + \frac{2xd}{XJ} \cdot (SCM \cdot v_{ds} + v_{sb} + \Phi_f)^{1/2} \right]^{1/2} - 1 \right\}$$

If $NWM \leq 0$,

$$ncf = 0$$

otherwise,

$$ncf = \frac{NWM \cdot X_d \cdot (\Phi_f)^{1/2}}{W_{eff}}$$

where:

$$X_d = \left(\frac{2 \cdot E_{si}}{q \cdot DNB} \right)^{1/2}$$

Saturation Voltage, v_{dsat}

The saturation voltage due to channel pinch-off at the drain side is computed by:

$$v_{sat} = v_{gs} - v_{bi} + \frac{\gamma^2}{2} \cdot \left\{ 1 - \left[1 + \frac{4}{\gamma^2} \cdot (v_{gs} - v_{bi} + \Phi_f + v_{sb}) \right]^{1/2} \right\}$$

$$v_{dsat} = v_{sat}$$

If ECV is not equal to 1000, then the program modifies v_{sat} to include carrier velocity saturation effect:

$$v_{dsat} = v_{sat} + v_c - (v_{sat}^2 + v_c^2)^{1/2}$$

where:

$$v_c = ECV \cdot L_{eff}$$

Mobility Reduction, UB_{eff}

The mobility degradation effect in the LEVEL 5 model is computed by:

$$UB_{eff} = \frac{1}{\frac{1}{UB} + \frac{FRC \cdot (v_{gs} - v_{th})}{TOX} + \frac{vde}{VST \cdot L_e} + FSB \cdot v_{sb}^{1/2}}$$

where:

$$L_e = L_{eff} \quad \textit{linear region}$$

$$L_e = L_{eff} - \Delta L \quad \textit{saturation region}$$

The channel length modulation effect (ΔL) is defined in the following section.

Channel Length Modulation

The LEVEL 5 model includes the channel length modulation effect by modifying the I_{ds} current as follows:

$$I_{ds} = \frac{I_{ds}}{1 - \frac{\Delta L}{L_{eff}}}$$

where:

$$\Delta L = 1e4 \cdot \left[\frac{2.73e3 \cdot XJ}{DNB \cdot \ln\left(\frac{1e20}{DNB}\right)}\right]^{1/3} \cdot [(v_{ds} - v_{dsat} + PHI)^{1/3} - PHI^{1/3}]$$

The ΔL is in microns, assuming XJ is in microns and DNB is in cm^{-3}.

Subthreshold Current, I_{ds}

This region of operation is characterized by the Fast Surface State (FSS) if it is greater than 1e10. Then the effective threshold voltage, separating the strong inversion region from the weak inversion region, is determined as follows:

$$von = v_{th} + fast$$

where:

$$fast = v_{tm} \cdot \left[1 + \frac{q \cdot FSS}{cox} + \frac{\gamma}{2 \cdot (\Phi_f + v_{sb})^{1/2}} \right]$$

and vt is the thermal voltage.

The I_{ds} is given by:

Weak Inversion Region, $v_{gs} < v_{th}$

$$I_{ds} = (von, vde, v_{sb}) \cdot e^{\frac{v_{gs} - von}{fast}}$$

Strong Inversion Region, $v_{gs} \geq v_{th}$

$$I_{ds} = I_{ds}(v_{gs}, vde, v_{sb})$$

Note: The modified threshold voltage (von) produced by FSS is also used in strong inversion; that is, in the mobility equations, von is used instead of v_{th}.

Depletion Mode DC Model ZENH=0

The LEVEL 5 MOS model uses depletion mode devices as the load element in contemporary standard n-channel technologies[2.] . This model was formulated assuming a silicon gate construction with an ion implant used to obtain the depletion characteristics. A special model is required for depletion devices, because the implant used to create the negative threshold also results in a complicated impurity concentration profile in the substrate. The implant profile changes the basis for the traditional calculation of the bulk charge, QB. The additional charge from the implant, QBI, must be calculated.

This implanted layer also causes the formation of an additional channel, offering a conductive pathway through the bulk silicon, as well as through the surface channel. This second pathway can cause difficulties when trying to model a depletion device with existing MOS models. The bulk channel is partially shielded from the oxide interface by the surface channel, and the mobility of the bulk silicon can be substantially higher. Yet with all the differences, a depletion model still can share the same theoretical basis as the Ihantola and Moll gradual channel model.

The depletion model differs from the Ihantola and Moll model as follows:

- Implant charge accounted for
- Finite implant thickness (DP)
- Two channels are assumed: a surface channel and a bulk channel
- Bulk channel has a bulk mobility (UH)
- Bulk gain is assumed to be different from surface gain

In the depletion model, the gain is lower at low gate voltages and higher at high gate voltages. This variation in gain is the reason the enhancement models cannot generate an accurate representation for a depletion device. The physical model for a depletion device is basically the same as an enhancement model, except that the depletion implant is approximated by a one-step profile with a depth DP.

Due to the implant profile, the drain current equation must be calculated by region. MOSFET device model LEVEL 5 has three regions: depletion, enhancement, and partial enhancement.

Depletion Region, $v_{gs} - v_{fb} < 0$

The low gate voltage region is dominated by the bulk channel.

Enhancement Region, $v_{gs} - v_{fb} > 0$, $v_{ds} < v_{gs} - v_{fb}$

The region is defined by high gate voltage and low drain voltage. In the enhancement region, both channels are fully turned on.

Partial enhancement region, $v_{gs} - v_{fb} > 0$, $v_{ds} > v_{gs} - v_{fb}$

The region has high gate and drain voltages, resulting in the surface region being partially turned on and the bulk region being fully turned on.

IDS Equations, Depletion Model LEVEL 5

The IDS equations for a LEVEL 5 depletion model follow.

Depletion, v_{gs}-v_{fb} <0

$$I_{ds} = \beta 1 \cdot \left\{ q \cdot NI \cdot vde + cav \cdot \left[(v_{gs} - v_{fb}) \cdot vde - \frac{vde^2}{2} \right] \right.$$

$$\left. \frac{2}{3} \cdot cav \cdot \gamma \cdot [(vde + v_{sb} + \Phi_d)^{3/2} - (v_{sb} + \Phi_d)^{3/2}] \right\}$$

Enhancement, v_{gs}-v_{fb} vde>0

$$I_{ds} = \beta 1 \cdot \left\{ q \cdot NI \cdot vde - \frac{2}{3} \cdot cav \cdot \gamma \cdot [(vde + v_{sb} + \Phi_d)^{3/2} - (v_{sb} + \Phi_d)^{3/2}] \right\}$$

$$+ \beta \cdot \left[(v_{gs} - v_{fb}) \cdot vde - \frac{vde^2}{2} \right]$$

Partial Enhancement, v_{gs}-v_{fb}<vde

$$I_{ds} = \beta 1 \cdot \left\{ q \cdot NI \cdot vde + cav \cdot \left[(v_{gs} - v_{fb}) \cdot vde - \frac{vde^2}{2} \right] \right.$$

$$-\frac{2}{3}\cdot cav\cdot\gamma\cdot[(vde+v_{sb}+\Phi_d)^{3/2}-(v_{sb}+\Phi_d)^{3/2}]\Bigg\}$$

$$+\left(\frac{1}{2}\beta-\beta 1\cdot cav\right)\cdot(v_{gs}-v_{fb})^2$$

where:

$$\beta 1 = UH\cdot\frac{W_{eff}}{L_{eff}}$$

$$\beta = UBeff\cdot cox\cdot\frac{W_{eff}}{L_{eff}}$$

$$cav = \frac{cox\cdot cs}{cox+cs}$$

$$cs = \frac{2.77E_{si}}{DP\cdot 1e\text{-}4}$$

$$\Phi_d = v_{tm}\cdot\ln\left(\frac{DNB\cdot nd}{ni^2}\right)$$

$$nd = \frac{NI\cdot 1e4}{DP}$$

and:

$$vde = \min(v_{ds}, v_{dsat})$$

The saturation voltage, threshold voltage, and effective γ are described in the following sections.

Threshold Voltage, v_{th}

The model parameter VTO is an extrapolated zero-bias threshold voltage for a large device. The effective threshold voltage, including the device size effects and the terminal voltages, is calculated as follows:

$$v_{th} = v_{fb} - \beta d \cdot [vch - \gamma \cdot (\Phi_d + v_{sb})^{1/2}]$$

where:

$$v_{fb} = VTO + \beta d \cdot (vch - \gamma_0 \cdot \Phi_d^{1/2})$$

$$\beta d = \frac{UH \cdot cav}{UB \cdot cox}$$

$$vch = \frac{q \cdot NI}{cav}$$

$$\gamma_0 = \frac{(2 \cdot E_{si} \cdot q \cdot na1)^{1/2}}{cav}$$

$$na1 = \frac{nd \cdot DNB}{nd + DNB}$$

$$nd = \frac{NI}{DP \cdot 1e\text{-}4}$$

The effective γ, including small device size effects, is computed as follows:

$$\gamma = \gamma_0 \cdot (1 - scf) \cdot (1 + ncf)$$

where:

If SCM ≤0,

$$scf = 0$$

otherwise,

$$scf = \frac{XJ}{L_{eff}} \cdot \left\{ \left[1 + \frac{2xd}{XJ} \cdot (SCM \cdot v_{ds} + v_b + \Phi_d)^{1/2} \right]^{1/2} - 1 \right\}$$

If NWM ≤0,

$$ncf = 0$$

otherwise,

$$ncf = \frac{NWM \cdot X_d \cdot \Phi_d^{1/2}}{W_{eff}}$$

where:

$$X_d = \left(\frac{2 \cdot E_{si}}{q \cdot DNB} \right)^{1/2}$$

Note: When $v_{gs} \le v_{th}$, the surface is inverted and a residual DC current exists.When v_{sb} is large enough to make $v_{th} > vin_{th}$, then v_{th} is used as the inversion threshold voltage. In order to determine the residual current, vin_{th} is inserted into the I_{ds}, v_{sat}, and mobility equation in place of v_{gs} (except for v_{gs} in the exponential term of the subthreshold current). The inversion threshold voltage at a given v_{sb} is vin_{th}, which is computed as:

$$vinth = v_{fb} - \frac{q \cdot NI}{cox} - v_{sb}$$

Saturation Voltage, v_{dsat}

The saturation voltage (v_{sat}) is determined as:

$$v_{sat} = v_{gs} - v_{fb} + vch + \frac{\gamma^2}{2} \cdot \left\{ 1 - \left[1 + \frac{4}{\gamma^2} \cdot (v_{gs} - v_{fb} + vch + v_{sb} + \Phi_d) \right]^{1/2} \right\}$$

$$v_{dsat} = v_{sat}$$

IF ECV is not equal to 1000 (V/µm), Avant! True-Hspice modifies v_{sat} to include the carrier velocity saturation effect.

$$v_{dsat} = v_{sat} + v_c - (v_{sat} + v_c^2)^{1/2}$$

where:

$$v_c = ECV \cdot L_{eff}$$

Mobility Reduction, UB_{eff}

The surface mobility (UB) is dependent upon terminal voltages as follows:

$$UB_{eff} = \frac{1}{\frac{1}{UB} + \frac{FRC \cdot (v_{gs} - v_{th})}{TOX} + \frac{vde}{VST \cdot le} + FSB \cdot v_{sb}^{1/2}}$$

where:

$$L_e = L_{eff} \quad \textit{Linear region}$$

$$L_e = L_{eff} - \Delta L \quad \textit{Saturation region}$$

The channel length modulation effect (ΔL) is defined next.

Channel Length Modulation

The channel length modulation effect is included by modifying the I_{ds} current as:

$$I_{ds} = \frac{I_{ds}}{1 - \frac{\Delta L}{L_{eff}}}$$

where:

$$\Delta L = 1e4 \cdot \left[\frac{2.73e3 \cdot XJ}{na1 \cdot \ln\left(\frac{1e20}{na1}\right)}\right]^{1/3} \cdot [(v_{ds} - v_{dsat} + PHI)^{1/3} - PHI^{1/3}]$$

The ΔL parameter is in microns, assuming XJ is in microns and na1 is in cm^{-3}.

Subthreshold Current, I_{ds}

When device leakage currents become important for operation near or below the normal threshold voltage, the subthreshold characteristics are considered. The Avant! True-Hspice LEVEL 5 model uses the subthreshold model only if the number of fast surface states (that is, the FSS) is greater than 1e10. An effective threshold voltage (von) is then determined:

$$von = v_{th} + fast$$

where:

$$fast = v_{tm} \cdot \left[1 + \frac{q \cdot FSS}{cox} + \frac{\gamma}{2 \cdot (\Phi_d + v_{sb})^{1/2}}\right]$$

If von < vin_{th}, then vin_{th} is substituted for von.

Note: The Avant! True-Hspice LEVEL 5 model uses the following subthreshold model only if v_{gs} < von and the device is either in partial or full enhancement mode. Otherwise, it use the model in enhancement mode (ZENH=1). The subthreshold current calculated below includes the residual DC current.

If v_{gs} <von then,

Partial Enhancement, v_{gs}-v_{fb} < vde

$$I_{ds} = \beta 1 \cdot \left\{ q \cdot NI \cdot vde + cav \cdot \left[(von - v_{fb}) \cdot vde - \frac{vde^2}{2} \right] \right.$$

$$\left. - \frac{2}{3} \cdot cav \cdot \gamma \cdot [(vde + v_{sb} + \Phi_d)^{3/2} - (v_{sb} + \Phi_d)^{3/2}] \right\}$$

$$+ \frac{1}{2} \cdot \left(\beta \cdot e^{\frac{v_{gs} - von}{fast}} - \beta 1 \cdot cav \right) \cdot (von - v_{fb})^2$$

Full Enhancement, v_{gs}-v_{fb} vde > 0

$$I_{ds} = \beta 1 \cdot \left\{ q \cdot NI \cdot vde - \frac{2}{3} \cdot cav \cdot \gamma [(vde + v_{sb} + \Phi_d)^{3/2} - (v_{sb} + \Phi_d)^{3/2}] \right\}$$

$$+ \beta \cdot \left[(von - v_{fb}) \cdot vde - \frac{vde^2}{2} \right] \cdot e^{\frac{v_{gs} - von}{fast}}$$

Example

```
FILE ML5IV.SP HSPICE LEVEL 5 MODEL EXAMPLES
*OUTPUT CHARACTERISTICS FOR ENHANCEMENT & DEPLETION MODE
.OPT ACCT LIST CO=132
.OP
VDS 3 0 .1
VGS 2 0
M1 1 2 0 0 MODEN L=20U W=20U
```

Enhancement Mode

```
.MODEL MODEN NMOS LEVEL=5
+ VT=.7 TOX=292 FRC=2.739E-2 DNB=2.423E16 UB=642.8
+ OXETCH=-.98 XJ=.29 LATD=.34 ECV=4 VST=5.595E7
+ FSB=7.095E-5 SCM=.4 FSS=2.2E11 NWM=.93 PHI=.61
+ TCV=1.45E-3 PTC=9E-5 BEX=1.8
*
VIDS 3 1
.DC VGS 0 5 0.2
.PRINT DC I(VIDS) V(2)
.PLOT DC I(VIDS)
$$$$$$
.ALTER
$$$$$$
M1 1 2 0 0 MODDP L=20U W=20U
```

Depletion Mode

```
.MODEL MODDP NMOS LEVEL=5 ZENH=0.
+ VT=-4.0 FRC=.03 TOX=800 DNB=6E14 XJ=0.8 LATD=0.7
+ DEL=0.4 CJ=0.1E-3 PHI=0.6 EXA=0.5 EXP=0.5 FSB=3E-5
+ ECV=5 VST=4E7 UB=850 SCM=0.5 NI=5.5E11 DP=0.7 UH=1200
*
.END
```

LEVEL 6 and LEVEL 7 IDS: MOSFET Model

These models represent ASPEC, MSINC, and ISPICE MOSFET model equations. The only difference between LEVEL 6 and LEVEL 7 equations is the handling of the parasitic elements and the method of temperature compensation. See ‘Mobility Parameters” on page 9-12 and ‘Channel Length Modulation” on page 9-17 for those model parameters.

LEVEL 6 and LEVEL 7 Model Parameters

The LEVEL 6 and LEVEL 7 model parameters are listed in this section.

Basic Model Parameters

Name (Alias)	Units	Default	Description

LEVEL		1.0	IDS equation selector
			`LEVEL=6`
			Lattin-Jenkins-Grove model, using ASPEC-style parasitics
			Note: ASPEC automatically selects Level 6. However, specifying Level 6 does not automatically invoke ASPEC. (For complete information, see the end of the Level 6 section.)
			`LEVEL=7`
			Lattin-Jenkins-Grove model, using SPICE-style parasitics

Name (Alias)	Units	Default	Description
CLM (GDS)		0.0	Channel length modulation equation selector
DNB (NSUB)	$1/cm^3$	1.0e15	Substrate doping
DNS (NI)	$1/cm^3$	0.0	Surface substrate doping
ECRIT (ESAT)	V/cm	0.0	Drain-source critical field. Use zero to indicate an infinite value, typically 40,000 V/cm.
GAMMA	$V^{1/2}$		Body effect factor. ■ If this parameter is not input, GAMMA is calculated from DNB. ■ GAMMA is the body effect when vsb < VB0. ■ If vsb > VB0, LGAMMA is used. Using GAMMA, LGAMMA, and VB0 allows a two-step approximation of a non-homogeneous substrate.
LGAMMA	$V^{1/2}$	0.0	This parameter is the body effect factor when vsb > VB0. When the Poon-Yau GAMMA expression is used, LGAMMA is junction depth, in microns. In this case LGAMMA is multiplied by SCALM.
MOB		0.0	Mobility equation selector
NWM		0.0	Narrow width modulation of GAMMA
SCM		0.0	Short-channel modulation of GAMMA

Name (Alias)	Units	Default	Description
UO (UB, UBO)	$cm^2/(V \cdot s)$	600 (N) 250 (P)	This parameter is the low field bulk mobility. It is calculated from KP if KP is supplied.
UPDATE		0.0	Selector for different version of LEVEL 6 model. For UPDATE=1 and 2 alternate saturation voltage, mobility equation (MOB=3) and series resistances RS and RD are modified to be compatible with ASPEC. UPDATE=1 provides continuous Multi-Level GAMMA model.
VB0 (VB)	V	0.0	Reference voltage for GAMMA switch. ■ If vsb < VB0, GAMMA is used. ■ If vsb > VB0, LGAMMA is used in the ids equation.

VMAX (VMX)	cm/s	0.0	Maximum drift velocity of carriers. Whether or not VMAX is set determines which calculation scheme is used for vdsat. Use zero to indicate an infinite value. Typical values:
			`electrons 8.4e6 cm/s`
			`holes 4.3e6 cm/s`

Effective Length and Width Parameters

Name (Alias)	Units	Default	Description
DEL	m	0.0	Channel length reduction on each side. DEL is applicable in most MOSFET models. An exception is the BSIM (LEVEL 13) model, where DEL is not present. $DELscaled = DEL \cdot SCALM$
LD (DLAT, LATD)	m		Lateral diffusion into channel from source and drain diffusion. ■ If LD and XJ are unspecified, LD Default=0.0 ■ When LD is unspecified but XJ is specified, LD is calculated from XJ $LD\ Default = 0.75 \cdot XJ$ $LDscaled = LD \cdot SCALM$
LDAC	m		This parameter is the same as LD, but if LDAC is included in the .MODEL statement, it replaces LD in the Leff calculation for AC gate capacitance.
LREF	m	0.0	Channel length reference $LREFscaled = LREF \cdot SCALM$
LMLT		1.0	Length shrink factor
WD	m	0.0	Lateral diffusion into channel from bulk along width $WDscaled = WD \cdot SCALM$

Name (Alias)	Units	Default	Description
WDAC	m		This parameter is the same as WD, but if WDAC is included in the .MODEL statement, it replaces WD in the Weff calculation for AC gate capacitance.
WMLT		1.0	Diffusion layer and width shrink factor
WREF	m	0.0	Channel width reference $WREFscaled = WREF \cdot SCALM$
XJ	m	0.0	Metallurgical junction depth $XJscaled = XJ \cdot SCALM$
XL (DL, LDEL)	m	0.0	Accounts for masking and etching effects $XLscaled = XL \cdot SCALM$
XW (DW, WDEL)	m	0.0	Accounts for masking and etching effects $XWscaled = XW \cdot SCALM$

Threshold Voltage Parameters

Name (Alias)	Units	Default	Description
FDS		0.0	Field, drain to source, controls reduction of threshold due to source-drain electric field
LND	µm/V	0.0	ND length sensitivity
LN0	µm	0.0	N0 length sensitivity
ND	1/V	0.0	Drain subthreshold factor. Typical value=1.
N0		0.0	Gate subthreshold factor. Typical value=1.

Name (Alias)	Units	Default	Description
NFS (DFS, NF)	$cm^{-2}.V^{-1}$	0.0	Fast surface state density
NWE	m	0.0	Narrow width effect, direct compensation of VTO NWEscaled = NWE · SCALM
UFDS		0.0	High field FDS
VFDS	V	0.0	Reference voltage for selection of FDS OR UFDS: ■ FDS used if vds ≤ VFDS ■ UFDS used if vds > VFDS
VSH	V	0.0	Threshold voltage shifter for zero-bias threshold voltage (VTO) reduction as a function of the ratio of LD to Leff
VTO (VT)	V		Zero-bias threshold voltage. This parameter is calculated if not specified (see ‘Common Threshold Voltage Equations” on page 8-52).
WEX			Weak inversion exponent
WIC		0.0	Subthreshold model selector
WND	µm/V	0.0	ND width sensitivity
WN0	µm	0.0	N0 width sensitivity

Alternate Saturation Model Parameters

Name (Alias)	Units	Default	Description
KA		1.0	Alternate saturation model: short-channel vds scaling factor coefficient
KU		0.0	Lateral field mobility parameter
MAL		0.5	Alternate saturation model: short-channel vds scaling factor exponent
MBL		1.0	Exponent for mobility reduction due to source-drain electric field
NU		1.0	Mobility reduction due to source-drain electric field

UPDATE Parameter for LEVEL 6 and LEVEL 7

The general form of the I_{ds} equation for LEVEL 6 is the same as the LEVEL 2 MOS model, but the small size effects, mobility reduction, and channel length modulation are included differently. Also, you can use LEVEL 6 models to model the MOS transistors with ion-implanted channels through the multi-level GAMMA capability.

The LEVEL 6 model represents the ASPEC, MSINC, and ISPICE programs MOSFET model. Use the enhanced model parameter UPDATE to invoke different versions of the LEVEL 6 model, as described next.

UPDATE=0

This is the original LEVEL 6 model in Avant! True-Hspice which is not quite compatible with the ASPEC model. It has some discontinuities in weak inversion, mobility equations (MOB=3), and multi-level GAMMA equations.

UPDATE=1

This enhanced version of the LEVEL 6 model contains improved multi-level GAMMA equations. The saturation voltage, drain-source current, and conductances are continuous.

UPDATE=2

This version of the LEVEL 6 model is compatible with the ASPEC model. The multi-level GAMMA model is not continuous, which is the case in the ASPEC program. See 'ASPEC Compatibility" on page 9-86.

Set UPDATE to 1.0 to implement changes to the device equations. Set UPDATE to 1.0 or 2 to implement the default handling of RS and RD are implemented. These values and changes provide a more accurate ASPEC model.

UPDATE=1 or 2 then,

TOX	= 690
UO (UB)	= 750 $cm^2/(V \cdot s)$ (N-ch)
UTRA (F3)	= 0.0

UPDATE=0 then,

TOX	= 1000
UO (UB)	= 750 $cm^2/(V \cdot s)$ (N-ch)
UTRA (F3)	= 0.0

Calculation of RD and RS in the MOSFET changes as follows when LDIF is not specified:

UPDATE=1 or 2 and LDIF=0,

$$RD = \frac{(RD + NRD \cdot RL)}{M}$$

$$RS = \frac{(RS + NRS \cdot RL)}{M}$$

Note: The ASPEC program does not use the multiplier M.

LDIF≠ 0,

$$RD = \frac{LATDscaled + LDIFscaled}{Weff} \cdot RD + NRD \cdot \frac{RL}{M}$$

$$RS = \frac{LATDscaled + LDIFscaled}{Weff} \cdot RS + NRS \cdot \frac{RL}{M}$$

The vde in the mobility equations for alternate saturation model changes as follows:

$$vde = \min\left(\frac{vds}{vfa}, vsat\right), \quad UPDATE = 1 \text{ or } 2$$

$$vde = \min(vds, vfa \cdot vsat), \quad UPDATE = 0$$

The saturation voltage in the impact ionization equation is as follows:

$$vdsat = vfa \cdot vsat, \quad UPDATE = 1 \text{ or } 2$$

$$vdsat = vsat, \quad UPDATE = 0$$

Mobility equation MOB=3 changes as follows:

UPDATE= 1 or 2 and $(vgs - vth)^{F2} > VF1$***,***

$$ueff = \frac{UB}{F4 + (F1 - F3) \cdot VF1 + F3 \cdot (vgs - vth)^{F2}}$$

UPDATE= 0 and $(vgs - vth)^{F2} > VF1$***,***

$$ueff = \frac{UB}{F4 + F3 \cdot (vgs - vth)^{F2}}$$

LEVEL 6 Model Equations, UPDATE=0,2

IDS Equations

$$ids = \beta \cdot \left\{ \left(vgs - vbi - \frac{\eta \cdot vde}{2} \right) \cdot vde - \frac{2}{3} \cdot \gamma \cdot [(PHI + vde + vsb)^{3/2} - (PHI + vsb)^{3/2}] \right\}$$

where:

$$vde = \min(vds, vdsat)$$

$$\eta = 1 + \frac{NWEscaled}{weff}$$

$$\beta = ueff \cdot COX \cdot \frac{weff}{Leff}$$

Include the narrow-width effect through η, vbi, and γ values. For the narrow-width effect, specify model parameters NWE and/or NWM. Include the short-channel effect through parameters vbi and γ .

Effective Channel Length and Width

The model calculates effective channel length and width from the drawn length and width as follows:

$$leff = Lscaled \cdot LMLT + XLscaled - 2 \cdot (LDscaled + DELscaled)$$

$$weff = M \cdot (Wscaled \cdot WMLT + XWscaled - 2 \cdot WDscaled)$$

$$LREFeff = LREFscaled \cdot LMLT + XLscaled - 2 \cdot (LDscaled + DELscaled)$$

$$WREFeff = M \cdot (WREFscaled \cdot WMLT + XWscaled - 2 \cdot WDscaled)$$

Threshold Voltage, vth

The model determines effective threshold voltage as follows:

$$vth = vbi + \gamma \cdot (PHI + vsb)^{1/2}$$

The built-in voltage vbi and γ is computed differently depending on the specified model parameters.

Single-Gamma, VBO=0

When model parameter VBO is zero, the single-gamma model is used. In this case the model treats the parameter LGAMMA as a junction depth. It then modifies the GAMMA parameter for short-channel effect by the scf factor, which is computed using the Poon and Yau formulation. In this case LGAMMA is multiplied by the SCALM option.

$$scf = 1 - \frac{LGAMMA}{leff} \cdot \left\{ \left[1 + \frac{2 \cdot LAMBDA}{LGAMMA} \cdot (PHI + vsb)^{1/2} \right]^{1/2} - 1 \right\}$$

Specify the model parameter XJ to modify the model parameter GAMMA by the short-channel factor (gl).

$$gl = 1 - \frac{XJscaled}{leff} \cdot \left\{ \left[1 + \frac{2 \cdot LAMBDA}{XJscaled} \cdot (PHI + vsb + SCM \cdot vds)^{1/2} \right]^{1/2} - 1 \right\}$$

The gl factor generally replaces the scf factor for the multilevel GAMMA model.

The model also includes the narrow-width effect by modifying GAMMA with the gw factor, which is computed as:

$$gw = \frac{1 + NWM \cdot xd}{weff}$$

where:

$$xd = \left(\frac{2 \cdot \varepsilon si}{q \cdot DNB} \right)^{1/2}$$

Finally, the effective γ, including short-channel and narrow width effects, is:

$$\gamma = GAMMA \cdot gw \cdot gl \cdot scf$$

Effective Built-in Voltage, vbi

The model includes the narrow-width effect, which is the increase in threshold voltage due to extra bulk charge at the edge of the channel, by modifying vbi if you specify the model parameter NWE.

The short-channel effect, which is the decrease in threshold voltage due to the induced potential barrier- lowering effect, is included through vbi modification. To include this effect, you must specify the model parameter FDS and/or UFDS and VFDS.

The expressions for vbi, which sum up the above features, are:

vds≤VFDS , or VFDS=0

$$vbi = VTO - \gamma \cdot PHI^{1/2} + (\eta - 1) \cdot (PHI + vsb) - \frac{LDscaled}{Leff} \cdot VSH - \frac{\varepsilon si}{COX \cdot Leff} \cdot FDS \cdot vds$$

vds>VFDS

$$vbi = VTO - \gamma \cdot PHI^{1/2} + (\eta - 1) \cdot (PHI + vsb) - \frac{LDscaled}{leff} \cdot VSH - \frac{esi}{COX \cdot Leff}$$

$$\cdot [(FDS - UFDS) \cdot VFDS + UFDS \cdot vds]$$

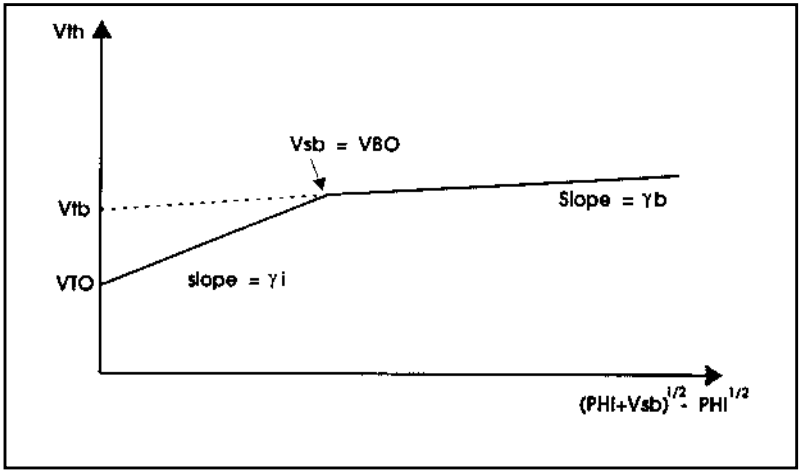
The above equations describe piecewise linear variations of vbi as a function of vds. If you do not specify VFDS, the first equation for vbi is used.

Note: The True-Hspice model calculates model parameters such as VTO, PHI, and GAMMA, if they are not user-specified (see ‘Common Threshold Voltage Equations” on page 8-52).

Multi-Level Gamma, VBO>0

Use Multi-Level Gamma to model MOS transistors with Ion-Implanted channels. The doping concentration under the gate is approximated as step functions. GAMMA and LGAMMA, respectively, represent the corresponding body effects coefficients for the implant layer and the substrate. Figure 9-1 shows the variation of vth as a function of vsb for Multi-Level Gamma.

Figure 9-1: Threshold Voltage Variation



The threshold voltage equations for different regions are as follows:

Channel Depletion Region is in the Implant Layer, vsb ≤ VBO

$$\gamma = \gamma i$$

$$vth = vbi + \gamma i \cdot (vsb + PHI)^{1/2}$$

$$vbi = VTO - \gamma i \cdot (PHI)^{1/2}$$

Channel Depletion Region is Expanded into the Bulk, vsb> VBO

$$\gamma = \gamma b$$

$$vth = vbi + \gamma b \cdot (vsb + PHI)^{1/2}$$

$$vbi = vtb - \gamma b \cdot (PHI)^{1/2}$$

In order for the threshold voltage to be continuous at vsb=VBO, vtb must be:

$$vtb = VTO + (\gamma i - \gamma b) \cdot [(VBO + PHI)^{1/2} - (PHI)^{1/2}]$$

The γi and γb are effective values of GAMMA and LGAMMA, respectively. The model computes them as γ in single-gamma models, except the scf factor is 1.0.

$$\gamma i = GAMMA \cdot gw \cdot gl$$

$$\gamma b = LGAMMA \cdot gw \cdot gl$$

Effective Built-in Voltage, vbi for VBO>0

For vds ≤VFDS,

if vsb≤VBO,

$$vbi = VTO - \gamma i \cdot (PHI)^{1/2} + (\eta - 1) \cdot (PHI + vsb) - \frac{LDscaled}{Leff} \cdot VSH - \frac{\varepsilon si}{COX \cdot Leff} \cdot FDS \cdot vds$$

if vsb>VBO,

$$vbi = VTO - \gamma b \cdot (PHI)^{1/2} + (\gamma i - \gamma b) \cdot [(VBO + PHI)^{1/2} - (PHI)^{1/2}] + (\eta - 1)$$

$$+ (PHI + vsb) - \frac{LDscaled}{Leff} \cdot VSH - \frac{\varepsilon si}{COX \cdot Leff} \cdot FDS \cdot vds$$

For vds>VFDS,

if vsb≤VBO,

$$vbi = VTO - \gamma i \cdot (PHI)^{1/2} + (\eta - 1) \cdot (PHI + vsb) - \frac{LDscaled}{Leff} \cdot VSH - \frac{\varepsilon si}{COX \cdot Leff}$$

$$\cdot [(FDS - UFDS) \cdot VFDS + UFDS \cdot vds]$$

if vsb>VBO,

$$vbi = VTO - \gamma b \cdot (PHI)^{1/2} + (\gamma i - \gamma b) \cdot [(VBO + PHI)^{1/2} - (PHI)^{1/2}] + (\eta - 1)$$

$$\cdot PHI + vsb - \frac{LDscaled}{Leff} \cdot VSH - \frac{\varepsilon si}{COX \cdot Leff} \cdot [(FDS - UFDS) \cdot VFDS + UFDS \cdot vds]$$

Saturation Voltage, vdsat (UPDATE=0,2)

The saturation voltage due to channel pinch-off at the drain side is determined by:

$$\text{vsat} = \frac{\text{vgs} - \text{vbi}}{\eta} + \frac{1}{2}\left(\frac{\gamma}{\eta}\right)^2 \cdot \left\{1 - \left[1 + \left(\frac{2 \cdot \eta}{\gamma}\right)^2 \cdot \left(\frac{\text{vgs} - \text{vbi}}{\eta} + \text{PHI} + \text{vsb}\right)\right]^{1/2}\right\}$$

The reduction of saturation voltage due to the carrier velocity saturation effect is included as follows:

$$\text{vdsat} = \text{vsat} + \text{vc} - (\text{vsat}^2 + \text{vc}^2)^{1/2}$$

where vc is determined if model parameter ECRIT >0, or VMAX >0, and KU≤1. If both ECRIT and VMAX are specified, then only the VMAX equation is used. However, the VMAX equation is not used if MOB=4 or MOB=5, since these mobility equations already contain a velocity saturation term.

$$\text{vc} = \text{ECRIT} \cdot \text{Leff}$$

or

$$\text{vc} = \frac{\text{VMAX} \cdot \text{Leff}}{\text{ueff}}$$

Because vsb>VBO, γ is switched from γi to γb, the ids, vsat, and conductances are not continuous. This problem is demonstrated in the following example. To correct the discontinuity problem, specify model parameter UPDATE=1. The next section discusses this improvement.

Example

This is an example of a multi-level gamma model, UPDATE=0.

```
$ TGAM2.SP---MULTI-LEVEL GAMMA MODEL, UPDATE=0
* THIS DATA IS FOR THE COMPARISON OF MULTI-LEVEL GAMMA
* UPDATE=0 OR 2 AND THE IMPROVED MULTI-LEVEL GAMMA UPDATE=1.
*
.OPTIONS ASPEC NOMOD POST VNTOL=.1U RELI=.001 RELV=.0001
*
.MODEL NCH NMOS BULK=99 UPDATE=0
+ FDS=0.9 KU=1.6 MAL=0.5 MOB=1 CLM=1
+ LATD=0.2 PHI=0.3 VT=0.9 GAMMA=0.72 LGAMMA=0.14
```

```
+ VB0=1.2 F1=0.08 ESAT=8.6E+4 KL=0.05
+ LAMBDA=3.2U UB=638 F3=0.22
+ KA=0.97 MBL=0.76 NFS=1.0E+12 WIC=0
+ LDEL=0.084 WDEL=0.037 TOX=365 VSH=0.7
*
VB 0 99 0
VG 2 0 1
MA 1 2 0 99 NCH 26.0 1.4
.DC VB 1.0 1.3 .01
.PRINT IDS=PAR('I(MA)') VTH=PAR('LV9(MA)')
VDSAT=PAR('LV10(MA)')
.PRINT GM=PAR('LX7(MA)') GDS=PAR('LX8(MA)')
GMBS=PAR('LX9(MA)')
.END
```

Figure 9-2: Variation of IDS, VTH and VDSAT for UPDATE=0

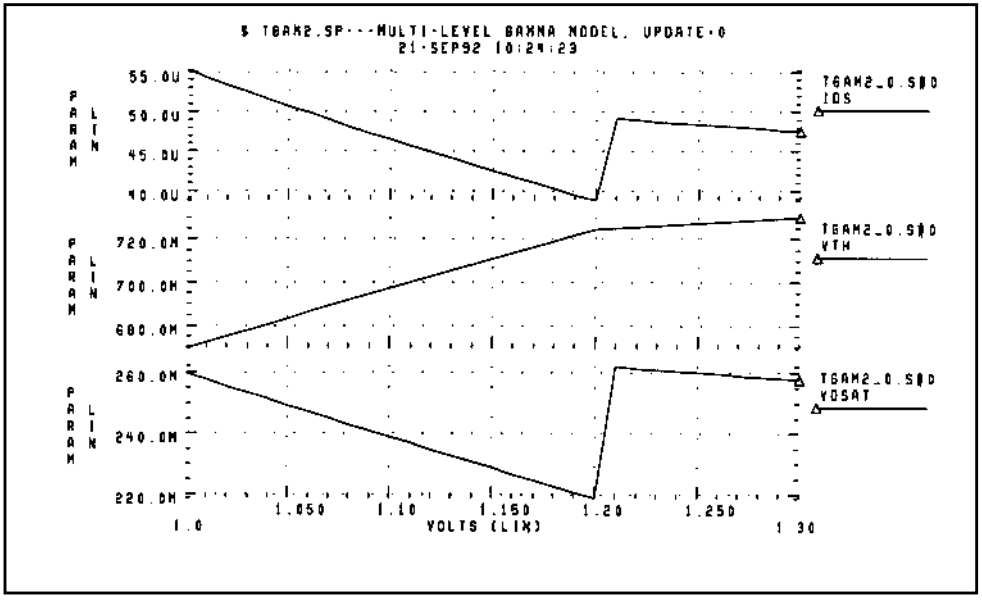
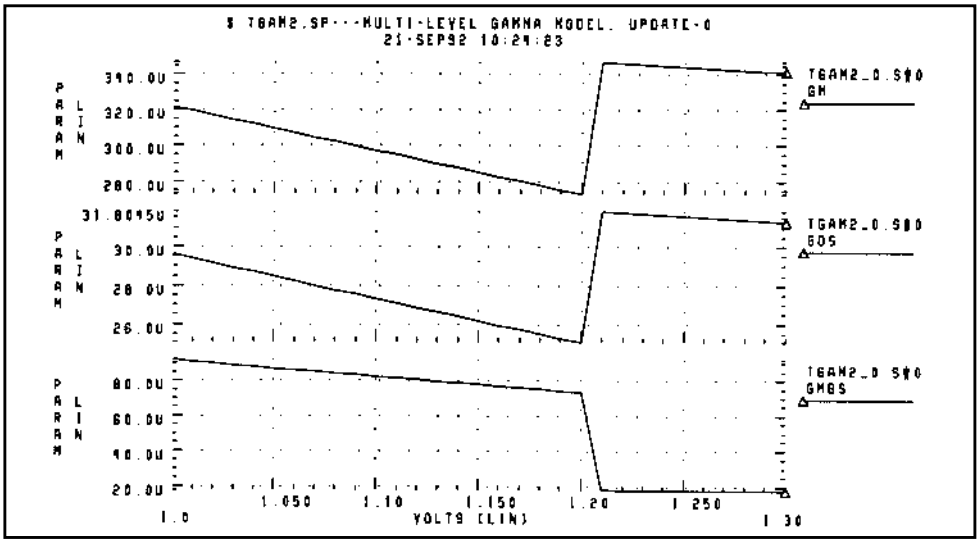


Figure 9-3: Variation of GM, GDS and GMBS for UPDATE=0



Each plot compares IDS, VTH, VDSAT, GM, GDS and GMBS as a function of vsb for UPDATE=0.

Improved Multi-Level Gamma, UPDATE=1

As demonstrated in previous sections, the regular Multi-Level Gamma displays some discontinuities in saturation voltage and drain current. This is because when v_{sb} is less than VBO, γ is set to γi and used in i_{ds} and vsat calculation. This is not correct; if (vds + vsb) exceeds VBO, the depletion regions at drain side expands into the substrate region, which means γb must be used instead of γi in v_{sat} computation. Since $v_{sat} = v_{gs} - v_{th}$ (drain), the threshold voltage at drain is computed using γi for vsb<VBO. As a result, the existing model overestimates the threshold voltage, ($\gamma i > \gamma b$), and, in turn, underestimates the saturation voltage and the drain current in the saturation region.

This causes a discontinuous increase in the saturation drain current crossing from the region vsb<VBO to the region vsb>VBO.

There are two major differences between the improved Multi-Level model and the regular Multi-Level model: the saturation voltage equation and the drain current equations. To use the improved model, set the model parameter to UPDATE=1.

Example

This is an example of a multi-level gamma model, UPDATE=2.

```
$ TGAM2.SP---MULTI-LEVEL GAMMA MODEL, UPDATE=2
* THIS DATA IS FOR THE COMPARISON OF MULTI-LEVEL GAMMA
* UPDATE=0 OR 2 AND THE IMPROVED MULTI-LEVEL GAMMA UPDATE=1.
*
.OPTIONS ASPEC NOMOD POST VNTOL=.1U RELI=.001 RELV=.0001
*
.MODEL NCH NMOS BULK=99 UPDATE=1
+ FDS=0.9 KU=1.6 MAL=0.5 MOB=1 CLM=1
+ LATD=0.2 PHI=0.3 VT=0.9 GAMMA=0.72 LGAMMA=0.14
+ VB0=1.2 F1=0.08 ESAT=8.6E+4 KL=0.05
+ LAMBDA=3.2U UB=638 F3=0.22
+ KA=0.97 MBL=0.76 NFS=1.0E+12 WIC=0
+ LDEL=0.084 WDEL=0.037 TOX=365 VSH=0.7
*

VD 1 0 5
VB 0 99 0
VG 2 0 1
MA 1 2 0 99 NCH 26.0 1.4
.DC VB 1.0 1.3 .01
.PRINT IDS=PAR('I(MA)') VTH=PAR('LV9(MA)')
   VDSAT=PAR('LV10(MA)')
.PRINT GM=PAR('LX7(MA)') GDS=PAR('LX8(MA)')
   GMBS=PAR('LX9(MA)')
.END
```

Figure 9-4: Variation of IDS, VTH and VDSAT for UPDATE=2

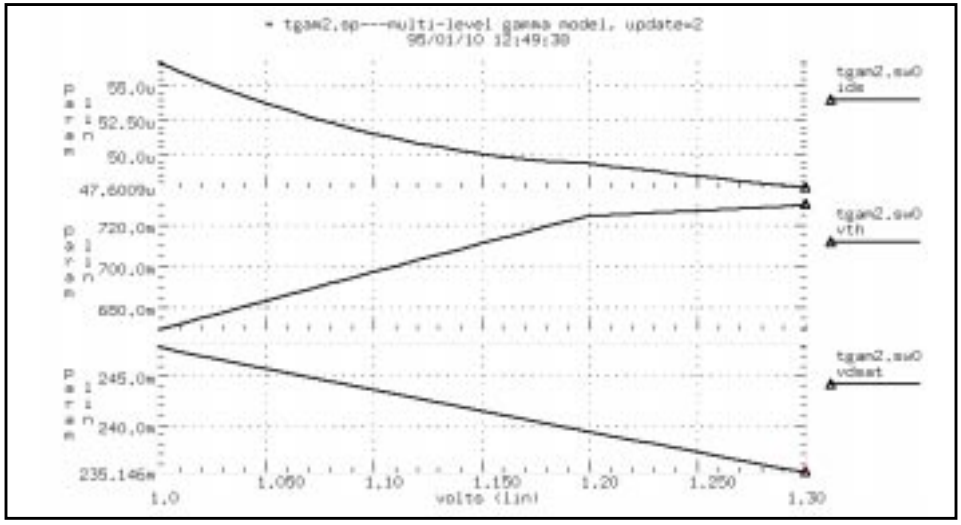
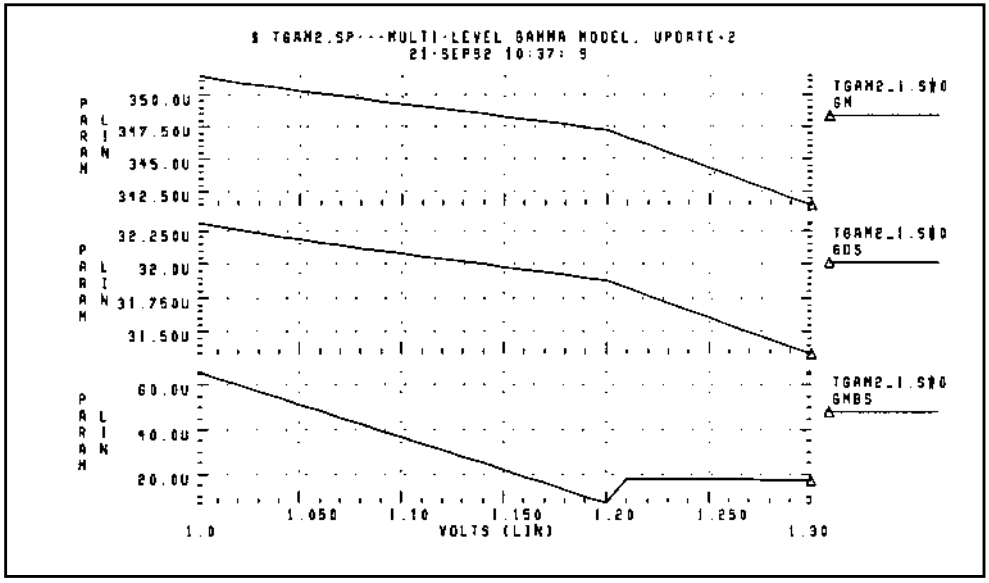


Figure 9-5: Variation of GM, GDS and GMBS for UPDATE=2



Each plot compares IDS, VTH, VDSAT, GM, GDS and GMBS as a function of vsb for UPDATE=1.

Saturation Voltage, vsat

To get the right value for vsat, two trial values of vsat corresponding to γi and γb are calculated:

$$vsat1 = \frac{vgs - vbi1}{\eta} + \frac{1}{2}\left(\frac{\gamma i}{\eta}\right)^2 \cdot \left\{1 - \left[1 + \left(\frac{2 \cdot \eta}{\gamma i}\right)^2 \cdot \left(\frac{vgs - vbi1}{\eta} + PHI + vsb\right)\right]^{1/2}\right\}$$

$$vsat2 = \frac{vgs - vbi2}{\eta} + \frac{1}{2}\left(\frac{\gamma b}{\eta}\right)^2 \cdot \left\{1 - \left[1 + \left(\frac{2 \cdot \eta}{\gamma b}\right)^2 \cdot \left(\frac{vgs - vbi2}{\eta} + PHI + vsb\right)\right]^{1/2}\right\}$$

vbi1 and vbi2 are built in potentials corresponding to γi and γb, respectively.

- If (vdsat1 + vsb) ≤ VBO, then vdsat = vdsat1
- If (vdsat2 + vsb) > VBO, then vdsat = vdsat2

Note: The vsat is modified by vc for carrier velocity saturation effects to obtain vdsat.

LEVEL 6 IDS Equations, UPDATE=1

There are three equations for ids depending upon the region of operation. The model derives these equations by integrating the bulk charge (vgs - vth (v) - v) from the source to the drain.

For vsb<VBO-vde, the model forms an entire gate depletion region in the implant layer.

$$ids = \beta \cdot \left\{\left(vgs - vbi1 - \frac{\eta \cdot vde}{2}\right) \cdot vde - \frac{2}{3} \cdot \gamma i \cdot \left[(PHI + vde + vsb)^{3/2} - (PHI + vsb)^{3/2}\right]\right\}$$

where vbi1 is the same as vbi for vsb≤VBO.

For vsb ≥ VBO, the entire gate depletion region expands into the bulk area.

$$ids = \beta \cdot \left\{ \left(vgs - vbi2 - \frac{\eta \cdot vde}{2} \right) \cdot vde - \frac{2}{3} \cdot \gamma b \cdot [(PHI + vde + vsb)^{3/2} - (PHI + vsb)^{3/2}] \right\}$$

where vbi2 is the same as vbi for vsb>VBO.

$$ids = \beta \cdot \left\{ (vgs - vbi2 - \frac{\eta \cdot vde}{2}) \cdot vde - \frac{2}{3} \cdot yi \cdot [(VBO + PHI)^{3/2} - (vsb + PHI)^{3/2}] \right.$$
$$\left. + (\gamma i - \gamma b) \cdot (VBO + PHI)^{1/2} \cdot \left(VBO - vsb \right) \right\}$$

For VBO-vde<vsb<VBO, the source side gate depletion region is in the implant layer, but the drain side gate depletion region is expanded into the bulk area.

Alternate DC Model, (ISPICE model)

If model parameter KU>1, this model is invoked. Then, the model computes vfu and vfa scale factors to scale both the vds voltage and the ids current. These scale factors are functions of ECRIT and vgs voltage. The vfa and vfu factors are defined as follows:

$$vfu = 1 - \frac{KU}{(\alpha^2 + KU^2)^{1/2} + \alpha(KU - 1)}$$

$$vfa = KA \cdot vfu^{(2 \cdot MAL)}$$

where:

$$\alpha = \frac{ECRIT \cdot Leff}{vgs - vth}$$

Note: vfu factor is always less than one.

The current ids is modified as follows:

NU=1

$$ids = vfu^{(2 \cdot MBL)} \cdot ids$$

For NU=0, the factor $vfu^{(2 \cdot MBL)}$ is set to one.

The current ids is a function of effective drain to source voltage, vde, which is determined as:

$$vde = \min(vds/vfa, vsat)$$

and:

$$vdsat = vfa \cdot vsat$$

This alternate model is generally coupled with the mobility normal field equations (MOB=3) and the channel length modulation drain field equation (CLM=3).

The vde value used in the mobility equations is:

$$vde = \min(vds, vfa \cdot vsat) \quad , \quad UPDATE=0$$

$$vds = \min(vds/vfa, vsat) \quad , \quad UPDATE=1,2$$

Subthreshold Current, ids

This region of operation is characterized by the choice of two different equations, selected through the model parameter WIC (Weak Inversion Choice). WIC can be designated as follows:

WIC=0	No weak inversion (default)
WIC=1	ASPEC-style weak inversion
WIC=2	Enhanced HSPICE-style weak inversion

In addition to WIC, set the parameter NFS. NFS represents the number of fast states per centimeter squared. Reasonable values for NFS range from 1e10 to 1e12.

WIC=0, no weak inversion

WIC=1, the threshold voltage vth is increased by the term fast

$$von = vth + fast$$

where:

$$fast = vt \cdot \left[1 + \frac{q \cdot NFS}{COX} + \frac{\gamma}{2 \cdot (vsb + PHI)^{1/2}}\right]$$

and vt is the thermal voltage.

The current ids for vgs<von is given by:

$$ids = ids(von, vde, vsb) \cdot e^{\frac{vgs - von}{fast}}$$

if vgs von, then

$$ids = ids(vge, vde, vsb)$$

Note: The modified threshold voltage (von) is not used for strong inversion conditions.

WIC=2

The subthreshold region is limited between cutoff and strong inversion regions. Although it appears that, if the gate voltage is less than vth-PHI, there can be no weak inversion conduction, there still can be diffusion conduction from the drain-to-bulk rather than drain-to-source.

$$von = vth + fast$$

where:

$$fast = vt \cdot \left[1 + \frac{q \cdot NFS}{COX} + \frac{\gamma}{2 \cdot (vsb + PHI)^{1/2}}\right]$$

Cutoff Region, vgs ≤ vth - PHI

$$ids = 0$$

Weak Inversion, vth - PHI < vgs ≤ von

$$ids = ids(von, vde, vsb) \cdot \left(1 - \frac{von - vgs}{fast + PHI}\right)^{WEX}$$

Strong Inversion, vgs > von

$$ids = ids(vgs, vde, vsb)$$

Note: The modified threshold voltage (von) is not used in strong inversion conditions.

If WIC=3, the subthreshold current is calculated differently. In this case, the ids current is:

$$ids = ids(vgs, vde, vsb) + isub(N0eff, NDeff, vgs, vds)$$

The N0eff and NDeff are functions of effective device width and length.

Effective Mobility, ueff

All mobility equations have the general form:

$$ueff = UO \cdot factor$$

ueff	Effective mobility at analysis temperature.
factor	Mobility degradation factor, see the following sections. Default=1.0

Use the MOB model parameter to select the mobility modulation equation used by Avant! True-Hspice models as follows:

MOB 0	No mobility reduction (default)
MOB 1	Gm equation
MOB 2	Frohman-Bentchkowski equation
MOB 3	Normal field equation
MOB 4	Universal field mobility reduction
MOB 5	Universal field mobility reduction with independent drain field
MOB 6	Modified MOB 3 equations (lateral field effect included)
MOB 7	Modified MOB 3 equations (lateral field effect not included)

These equations are described in the following sections.

MOB=0 Default, No Mobility

factor = 1.0 No mobility reduction

MOB=1 Gm Equation

Name (Alias)	Units	Default	Description
F1	1/V	0.0	Gate field mobility reduction
UTRA (F3)	factor	0.0	Source-drain mobility reduction factor

The MOB=1 equation is useful for transistors with constant source-to-bulk voltage, since the factor does not contain a vsb term. Use of this equation can result in over-estimation of mobility for small gate voltages and large back-bias such as depletion pull-ups.

$$\text{factor} = \frac{1}{1 + F1 \cdot (vgs - vb1 - F3 \cdot vde)}$$

$$vde = \min(vds, vdsat)$$

Note: If the alternate saturation model is used, vde is different for UPDATE=0 and UPDATE=1. See 'Alternate DC Model, (ISPICE model)" on page 9-73. Also, if VMAX>0, then vde=min (vds, vsat), and if VMAX is not specified, then vde=min (vds, vdsat).

MOB=2 Frohman-Bentchkowski Equation

Name (Alias)	Units	Default	Description
F1	V/cm	0.0	Critical gate-bulk electric field at which mobility reduction becomes significant
UEXP (F2)		0.0	Mobility exponent. Use 0.36 factor for n-channel and 0.15 for p -channel.
UTRA (F3)	factor	0.0	Source-drain mobility reduction factor
VMAX (VMX)	cm/s	0.0	Maximum drift velocity of carriers. Whether or not VMAX is set determines which calculation scheme is used for vdsat. Use zero to indicate an infinite value.

Mobility reduction equation (MOB=2$^{3.}$ produces good results for high gate voltages and drain fields with constant back-bias. This equation is typically used for p-channel pull-ups and n-channel pull-downs. Specify a value for VMAX to cause the proper calculation scheme to be used for vdsat. MOB=2 corresponds to MSINC UN=2 and is the SPICE default.

$$\text{factor} = \left[\frac{F1 \cdot \varepsilon si}{COX \cdot (vgs - vbi - F3 \cdot vde)}\right]^{F2}$$

where vde is defined the same as for MOB=1 equation.

MOB=3 Normal Field Equation

Name (Alias)	Units	Default	Description
F1	1/V	0.0	Low-field mobility multiplier
F4		1.0	Mobility summing constant
UEXP (F2)		0.0	Mobility exponent
UTRA (F3)	1/V	0.0	High-field mobility multiplier
VF1	V	0.0	Low to high field mobility (voltage switch)

This equation is the same as MSINC UN=1.

$$(vgs - vth)^{F2} \leq VF1,$$

$$factor = \frac{1}{F4 + F1 \cdot (vgs - vth)^{F2}}$$

If UPDATE=0, and $(vgs\text{-}vth)^{F2} > VF1$,

$$factor = \frac{1}{F4 + F3 \cdot (vgs - vth)^{F2}}$$

If UPDATE=1, 2 and $(vgs\text{-}vth)^{F2} > VF1$,

$$factor = \frac{1}{F4 + (F1 - F3) \cdot VF1 + F3 \cdot (vgs - vth)^{F2}}$$

MOB=4 and MOB=5 Universal Field Mobility Reduction

Name (Alias)	Units	Default	Description
ECRIT	V/cm	0.0	Critical electric drain field for mobility reduction. Use zero to indicate an infinite value.
F1	V/cm	0.0	Source-drain mobility reduction field (typical value 1e4 to 5e8)
MOB		0.0	Mobility equation selector. Set MOB=4 for critical field equation, or set MOB=5 for critical field equation with independent drain field.
UEXP (F2)	$1/V^{1/2}$	0.0	Bulk mobility reduction factor (typical value 0 to 0.5)
UTRA (F3)	V/cm	0.0	Critical electric drain field for mobility reduction

The MOB=4 equation is the same as the MSINC UN=3 equation. The MOB=5 equation is the same as MOB=4 except that F3 substitutes for ECRIT in the expression for vc.

The MOB=5 equation provides a better fit for CMOS devices in the saturation region. Do not specify a value for VMAX since velocity saturation is handled in the mobility equation.

$$\text{factor} = \frac{1}{1 + \frac{COX}{F1 \cdot \varepsilon ox} \cdot (vgs - cth) + \frac{vde}{vc} + F2 \cdot (vsb + PHI)^{1/2}}$$

If MOB=4,

$$vc = ECRIT \cdot Leff$$

If MOB=5,

$$vc = F3 \cdot Leff$$

Note: If you use the alternate saturation model, vde is different for UPDATE=0 and UPDATE=1, 2.

MOB=6, 7 Modified MOB=3

This mobility equation is the same as MOB=3, except the equation uses VTO instead of vth. When MOB=6 is used, the current ids also is modified as follows:

$$ids = \frac{ids}{1 + F1 \cdot \left(vgs - vth - \frac{vde}{2}\right) + \frac{UTRA}{Leff} \cdot vde}$$

Channel Length Modulation

The basic MOSFET current equation for ids describes a parabola, where the peak corresponds to the drain-to-source saturation voltage (vdsat). Long-channel MOSFETs generally demonstrate ideal behavior. For vds voltages greater than vdsat, there is no increase in the ids current. As the channel length decreases, the current in the saturation region continues to increase. This increase in current is modeled as a decrease in the effective channel length. Except for CLM=5 and 6, the channel length modulation equations are only calculated when the device is in the saturation region. The Avant! True-Hspice provides several channel length modulation equations; all (except for CLM=5) modify the ids equation as follows:

$$ids = \frac{ids}{1 - \frac{\Delta L}{Leff}}$$

ΔL is the change in channel length due to MOSFET electric fields.

Use the CLM model parameter to designate the channel length modulation equation that the True-Hspice model uses, as follows:

CLM = 0	No channel length modulation (default)
CLM = 1	one-sided step depletion layer drain field equation
CLM = 2	Frohman's electrostatic fringing field equation
CLM = 3	One-sided step depletion layer drain field equation, with carrier velocity saturation
CLM = 4	Wang's equation: linearly graded depletion layer
CLM = 5	Avant! channel length modulation
CLM = 6	Avant! ΔL equations

These equations and the associated model parameters are discussed in the following sections.

CLM=0 No Channel Modulation—Default

$$\Delta L = 0$$

This is the default channel length equation, representing no channel length modulation; it corresponds to MSINC GDS=0.0

CLM=1 Step Depletion Equation

Name (Alias)	Units	Default	Description
KL		0.0	Empirical constant (saturation voltage)
LAMBDA (LAM, LA)	$cm/V^{1/2}$	1.137e-4	Channel length modulation (–s calculated from NSUB unless specified) Default LAMBDA corresponds to default NSUB value

$$\Delta L = LAMBDA \cdot (vds - vdsat)^{1/2} \cdot \left(\frac{vdsat}{vsat}\right)^{KL}$$

If not user-specified, LAMBDA is calculated as:

$$LAMBDA = \left(\frac{2 \cdot \varepsilon si}{q \cdot DNB}\right)^{1/2}$$

This is a one-sided step depletion region formulation by Grove: ΔL varies with the depletion layer width, which is a function of the difference between the effective saturation voltage (vdsat) and the drain-to-source channel voltage (vds). This equation is typically used for long channels and high dopant concentrations. This corresponds to GDS=1 in MSINC.

CLM=2 Electrostatic Fringing Field

Name (Alias)	Units	Default	Description
A1		0.2	First fringing field factor gate-drain
A2		0.6	Second fringing field factor gate-vdsat

$$\Delta L = \frac{\varepsilon si}{COX} \cdot \frac{vds - vdsat}{A1 \cdot (vds - vgs + vbi) + A2 \cdot (vgs - vbi - vdsat)}$$

The fringing field equation, or electrostatic channel length reduction, developed by Frohman-Bentchkowski, is most often used for modeling short-channel enhancement transistors. In MSINC, the equivalent equation is GDS=2.

CLM=3 Carrier Velocity Saturation

Name (Alias)	Units	Default	Description
KA		1.0	vds scaling factor for velocity saturation
KCL		1.0	Exponent for vsb scaling factor

Name (Alias)	Units	Default	Description
KU		0.0	Velocity saturation switch. If KU ≤ 1, the standard velocity saturation equation is used.
LAMBDA (LAM, LA)	cm/ $V^{1/2}$	1.137e-4	Channel length modulation. This parameter is calculated from NSUB if not specified. The default LAMBDA corresponds to the default NSUB value.
MAL		0.5	vds exponent for velocity saturation
MCL		1.0	Short channel exponent

$$\Delta L = vfu^{(2 \cdot MCL)} \cdot LAMBDA \cdot$$
$$[(vds - vfa \cdot vsat + KCL \cdot vsb + PHI)^{1/2} - (KCL \cdot vsb + PHI)^{1/2}]$$

This equation is an extension of the first depletion layer equation, CLM=1, and includes the effects of carrier velocity saturation and the source-to-bulk voltage (vsb) depletion layer width. It represents the basic ISPICE equation. See ‘Alternate DC Model, (ISPICE model)” on page 9-73 for definitions of *vfa* and *vfu*.

CLM=4, Wang’s Equation

Name (Alias)	Units	Default	Description
A1	m	0.2	Junction depth A1scaled = A1 SCALM
DND	cm^{-3}	1e20	Drain diffusion concentration

Linearly Graded Depletion Layer

$$\Delta L = \left[\frac{2.73e5 \cdot A1scaled}{DNB \cdot \ln\left(\frac{DND}{DNB}\right)}\right]^{1/3} \cdot [(vds - vdsat + PHI)^{1/3} - PHI^{1/3}]$$

Wang's equation allows the inclusion of junction characteristics in the calculation of channel length modulation. The equation assumes that the junction approximated a linearly-graded junction and provides a value of 0.33 for the exponent. This equation is similar to MSINC GDS=3.

CLM=5, True-Hspice Model Channel Length Modulation

Name (Alias)	Units	Default	Description
LAMBDA	amp/V^2	0	Constant coefficient
VGLAM	1/V	0	Constant coefficient

When CLM=5, the current ids is increased by idssat, given as:

$$idssat = \frac{weff}{Leff} \cdot LAMBDA \cdot vds \cdot (vgs - vth) \cdot [1 + VGLAM \cdot (vgs - vth)$$

$$ids = ids + idssat$$

Note: The equation adds the idssat term to ids in all regions of operation. Also, LAMBDA is a function of temperature.

CLM=6, Star-Hspice ΔL Equation

Name (Alias)	Units	Default	Description
LAMBDA	$1/V^{KL}$	0	vds coefficient
LAM1	1/m	0	Channel length coefficient
KL		0	vds exponent
VGLAM	1/V	0	Gate drive coefficient

Unlike the other CLMs, this equation calculates the channel length modulation (ΔL) in all regions of operations and uses it to modify current ids.

$$\Delta L = \frac{Leff \cdot LAMBDA \cdot vds^{KL} \cdot [1 + VGLAM \cdot (vgs - vth)}{1 + LAM1 \cdot Leff}$$

and:

$$ids = \frac{ids}{1 - \frac{\Delta L}{Leff}}$$

Note: LAMBDA is a function of temperature.

ASPEC Compatibility

Make MOSFET models compatible with ASPEC by specifying ASPEC=1 in the .OPTION statement and LEVEL=6 in the associated MOSFET model statement.

If you assign the element parameters without keynames, you must use the parameter sequence given in the general format. The Avant! True-Hspice model assigns parameters in the order they are listed in the element statement. Errors occur if parameter names are also element keynames.

When Option ASPEC is in effect, a number of program variations occur. The MOSFET model parameter LEVEL is set to 6.

Note: Setting LEVEL=6 in the model does not invoke ASPEC.

ASPEC sets the following options:

MOSFET Option	WL = 1
General Options	SCALE = 1e-6
	SCALM = 1e-6

Since the ASPEC option sets the SCALE and SCALM options, it effectively changes the default units of any parameters affected by these options; use parameter values consistent with these scaling factors.

ASPEC sets the following model parameter defaults:

LEVEL	=	6
ACM	=	1
CJ	=	0.0
IS	=	0.0
NSUB	=	1e15

Note: NSUB is not be calculated from GAMMA, if UPDATE=1 or 2.

PHI	=	$1 \cdot \Phi_f$ (the Fermi potential)
TLEV	=	1
TLEVC	=	1

TLEV (TLEVC in turn, selects the ASPEC method of temperature update for the parameters CJ, CJSW, PB, PHP, VTO, and PHI.

Note: If PHI is entered explicitly, however, it is not updated for temperature. SCALM does not effect the scaling of parameters for the ASPEC mode. If SCALM is specified when using ASPEC, the Avant! True-Hspice model generates an error stating that SCALM is ignored.

LEVEL 7 IDS Model

The LEVEL 7 model is the same as the LEVEL 6 model except for the value of PHI.

If PHI is specified, then

For LEVEL=6,

$\Phi_s = \frac{PHI}{2}$, where Φ_s is the surface potential.

For LEVEL=7,

$$\Phi_s = PHI$$

To transform a LEVEL 7 equation to LEVEL 6, make the following substitution:

$$PHI \rightarrow 2 \cdot PHI$$

To transform a LEVEL 6 model into a LEVEL 7 model, make the following substitution:

$$PHI(Level\ 7) = PHI(Level\ 6)/2$$

LEVEL 8 IDS Model

The LEVEL 8 model, derived from research at Intersil and General Electric, is an enhanced version of the LEVEL 2 ids equation. LEVEL 2 differs from LEVEL 8 in the following areas: the effective substrate doping, threshold voltage, effective mobility, channel length modulation, and subthreshold current.

LEVEL 8 Model Parameters

This section lists the LEVEL 8 model parameters.

Basic DC Model Parameters

Name (Alias)	Units	Default	Description
LEVEL		1.0	IDS equation selector. Use LEVEL 8 for the advanced model using finite differences.
COX	F/m^2	3.45314 e-4	Oxide capacitance per unit gate area. This parameter is calculated from TOX if not specified.

ECRIT (ESAT)	V/cm	0.0	Critical electric field for carrier velocity saturation, from Grove:
			`electrons 6e4`
			`holes 2.4e4`
			Use zero to indicate an infinite value.

SNVB	$1/(V\ cm^3)$	0.0	Slope of doping concentration versus vsb (element parameter). (Multiplied by 1e6)
TOX	m	1e-7	Oxide thickness

Name (Alias)	Units	Default	Description
VMAX (VMX, VSAT)	m/s	0.0	Maximum drift velocity of carriers. Use zero to indicate an infinite value.

Effective Channel Width and Length Parameters

Name (Alias)	Units	Default	Description
DEL	m	0.0	Channel length reduction on each side. DEL is applicable in most MOSFET models. An exception is the BSIM (LEVEL 13) model, where DEL is not present. $DELscaled = DEL \cdot SCALM$
LD (DLAT, LATD)	m		Lateral diffusion into channel from source and drain diffusion. ■ If LD and XJ are unspecified, $LD\ default=0.0$ ■ If LD is unspecified, but XJ is specified, $LD\ default=0.75 \cdot XJ$ $LDscaled = LD \cdot SCALM.$
LDAC	m		This parameter is the same as LD, but if LDAC is included in the .MODEL statement, it replaces LD in the Leff calculation for AC gate capacitance.
WD	m	0.0	Lateral diffusion into channel from bulk along width $WDscaled = WD \cdot SCALM$

Name (Alias)	Units	Default	Description
WDAC	m		This parameter is the same as WD, but if WDAC is included in the .MODEL statement, it replaces WD in the Weff calculation for AC gate capacitance.
LMLT		1.0	Length shrink factor
LREF	m	0.0	Channel length reference $LREFscaled = LREF \cdot SCALM$
WMLT		1.0	Diffusion layer and width shrink factor
WREF	m	0.0	Channel width reference $WREFscaled = WREF \cdot SCALM$
XJ	m	0.0	Metallurgical junction depth $XJscaled = XJ \cdot SCALM$
XL (DL, LDEL)	m	0.0	Accounts for masking and etching effects $XLscaled = XL \cdot SCALM$
XW (WDEL, DW)	m	0.0	Accounts for masking and etching effects $XWscaled = XW \cdot SCALM$

Threshold Voltage Parameters

Name (Alias)	Units	Default	Description
CAV		0.0	Thermal voltage multiplier for the weak inversion equation
DELTA		0.0	Narrow width factor for adjusting threshold

Name (Alias)	Units	Default	Description
ETA		0.0	Drain-induced barrier lowering (DIBL) effect coefficient for threshold voltage
GAMMA	$V^{1/2}$		Body effect factor. This parameter is calculated from NSUB if not specified (see ‘Common Threshold Voltage Equations” on page 8-52).
LND	µm/V	0.0	ND length sensitivity
LN0	µm	0.0	N0 length sensitivity
ND	1/V	0.0	Drain subthreshold factor (typical value=1)
N0		0.0	Gate subthreshold factor (typical value=1)
WIC		0.0	Sub-threshold model selector
WND	µm/V	0.0	ND width sensitivity
WN0	µm	0.0	N0 width sensitivity
NFS (DFS, NF, DNF)	cm^{-2} V 1	0.0	Fast surface state density
NSUB (DNB, NB)	cm^{-3}	1e15	Bulk surface doping. This parameter is calculated from GAMMA if not specified.
PHI	V	0.576	Surface inversion potential. This parameter is calculated from NSUB if not specified (see ‘Common Threshold Voltage Equations” on page 8-52).
VTO(VT)	V		Zero-bias threshold voltage. This parameter is calculated if not specified (see ‘Common Threshold Voltage Equations” on page 8-52).

Mobility Parameters

Name (Alias)	Units	Default	Description
MOB		6.0	Mobility equation selector (can be set to 2, 3, 6, or 7 in LEVEL 8)
UCRIT	V/cm	1e4	MOB=6, UEXP>0 Critical field for mobility degradation, UEXP operates as a switch. MOB=6, UEXP≤0 Critical field for mobility degradation. Typical value is 0.01 V^{-1}.
UEXP (F2)		0.0	Critical field exponent in mobility degradation
UTRA	m/V	0.0	Transverse field coefficient (mobility)
UO (UB, UBO)	cm^2/ (V s)	600 (N) 250 (P)	Low field bulk mobility. This parameter is calculated from KP (BETA) if KP (BETA) is input.

Channel Length Modulation Parameters

Name (Alias)	Units	Default	Description
A1		0.2	Channel length modulation exponent (CLM=8)
CLM		7	Channel length modulation equation selector
LAM1	1/m	0.0	Channel length modulation length correction
LAMBDA (LAM, LA)		0.0	Channel length modulation coefficient

LEVEL 8 Model Equations

This section lists the LEVEL 8 model equations.

IDS Equations

LEVEL 8 ids equations are the same as the LEVEL 2 model. These equations are repeated here for convenience.

Cutoff Region, vgs≤vth

$$\mathrm{ids} = 0 \quad \textit{(See subthreshold current)}$$

On Region, vgs>vth

$$\mathrm{ids} = \beta \cdot \left\{ \left(\mathrm{vgs} - \mathrm{vb1} - \frac{\eta \cdot \mathrm{vde}}{2} \right) \cdot \mathrm{vde} - \frac{2}{3} \cdot \gamma \cdot [(\Phi + \mathrm{vde} + \mathrm{vsb})^{3/2} - (\Phi + \mathrm{vsb})^{3/2}] \right\}$$

where:

$$\mathrm{vde} = \min(\mathrm{vds}, \mathrm{vdsat})$$

$$\eta = 1 + \mathrm{DELTA} \cdot \frac{\pi \cdot \varepsilon_{si}}{4 \cdot \mathrm{COX} \cdot W_{eff}}$$

$$\beta = \mathrm{KP} \cdot \frac{W_{eff}}{L_{eff}}$$

Effective Channel Length and Width

The model calculates effective channel length and width from the drawn length and width as follows:

$$L_{eff} = \mathrm{Lscaled} \cdot \mathrm{LMLT} + \mathrm{XLscaled} - 2 \cdot (\mathrm{LDscaled} + \mathrm{DELscaled})$$

$$W_{eff} = M \cdot (\mathrm{Wscaled} \cdot \mathrm{WMLT} + \mathrm{XWscaled} - 2 \cdot \mathrm{WDscaled})$$

$$\mathrm{LREF}_{eff} = \mathrm{LREFscaled} \cdot \mathrm{LMLT} + \mathrm{XLscaled} - 2 \cdot (\mathrm{LDscaled} + \mathrm{DELscaled})$$

$$\mathrm{WREF}_{eff} = M \cdot (\mathrm{WREFscaled} \cdot \mathrm{WMLT} + \mathrm{XWscaled} - 2 \cdot \mathrm{WDscaled})$$

Effective Substrate Doping, nsub

Specify the model parameter SNVB to vary substrate doping concentration linearly as a function of vsb.

$$nsub = NSUB + SNVB \cdot vsb$$

The γ, Φ, and xd parameters are computed using the above equation for nsub.

$$\gamma = \frac{\sqrt{2 \cdot \varepsilon_{si} \cdot q \cdot nsub}}{COX}$$

$$\Phi = 2 \cdot vt \cdot \ln\left(\frac{nsub}{ni}\right)$$

$$xd = \sqrt{\frac{2 \cdot \varepsilon_{si}}{q \cdot nsub}}$$

If SNVB is zero, then γ = GAMMA. The γ value is adjusted for short-channel effect the same way as the LEVEL 2 model. Also, Φ is calculated using NSUB.

Threshold Voltage, vth

Specify ETA to include the threshold voltage reduction due to potential barrier lowering effect.

$$vbi = VTO - \gamma \cdot \sqrt{\Phi} - \frac{8.14e\text{-}22 \cdot ETA}{COX \cdot L_{eff}^3} \cdot vds + (\eta - 1) \cdot (vsb + \Phi)$$

$$vth = vbi + \gamma \cdot \sqrt{vsb + \Phi}$$

The γ is modified for short-channel effect, the same as in the LEVEL 2 model, to get effective γ .

Saturation Voltage vdsat

The saturation voltage vsat is computed the same as in the LEVEL 2 model. The carrier velocity effect is included only when ECRIT is greater than zero.

ECRIT > 0,

$$vdsat = vsat + vc - \sqrt{vsat^2 + vc^2}$$

where:

$$vc = ECRIT \cdot L_{eff}$$

ECRIT ≤ 0 or MOB=7,

$$vdsat = vsat$$

vsat is computed as in the LEVEL=2 model (see Saturation Voltage, vdsat on page 9-16).

Effective Mobility, ueff

The mobility equation selector MOB controls the mobility reduction equations. In the LEVEL 8 model, set MOB to 2, 3, 6, or 7. Default=6.

MOB=2 Mobility Reduction

$$u_{eff} = UO \cdot \left[\frac{\varepsilon_{se} \cdot UCRIT}{COX \cdot (vgs - vth - UTRA \cdot vde)}\right]^{UEXP}$$

MOB=3 Mobility Reduction

$$u_{eff} = \frac{UO}{1 + \frac{2.1e\text{-}8 \cdot (vgs + vth + egfet - \Phi)}{6 \cdot TOX}}$$

where *egfet* is the silicon energy gap at the analysis temperature.

$$egfet = 1.16 - \frac{7.02e\text{-}4 \cdot t^2}{t + 1108}$$

where t is the temperature in degrees Kelvin.

If VMAX>1,

$$u_{eff} = \frac{u_{eff}}{1 + \frac{u_{eff}}{VMAX \cdot L_{eff}} \cdot vde}$$

MOB=6 Mobility Reduction

For UEXP>0,

$$\text{If} \quad (vgs - vth) > \frac{\varepsilon_{si} \cdot UCRIT}{COX}$$

$$\text{then} \quad u_{eff} = \frac{UO \cdot \left[\frac{\varepsilon_{si} \cdot UCRIT}{COX \cdot (vgs - vth)}\right]^{UEXP}}{1 + \frac{UTRA}{L_{eff}} \cdot vde}$$

$$\text{otherwise,} \quad u_{eff} = \frac{UO}{1 + \frac{UTRA}{L_{eff}} \cdot vde}$$

For UEXP=0

$$u_{eff} = \frac{UO}{[1 + UCRIT \cdot (vgs - vth)] \cdot \left(1 + \frac{UTRA}{L_{eff}} \cdot vde\right)}$$

UCRIT for UEXP=0 has a dimension of (1/V).

MOB=7 Mobility Reduction

$$u_{eff} = \frac{UO}{1 + UTRA \cdot \left(vgs - vbi - \eta \cdot \frac{vde}{2} + \frac{body}{vde}\right)}$$

where:

$$body = \frac{2}{3} \cdot \gamma \cdot [(vde + vsb + \Phi)^{3/2} - (vsb + \Phi)^{3/2}]$$

Channel Length Modulation

The equation selector CLM controls the channel length modulation equations. In the LEVEL 8 model, set CLM to 6, 7, and 8. Default=7.

CLM=6 SPICE Channel Length Modulation

If LAMBDA=0,

$$\lambda = \frac{xd}{leff \cdot vds} \cdot \sqrt{\frac{vds - vdsat}{4} + \sqrt{1 + \left(\frac{vds - vdsat}{4}\right)^2}}$$

otherwise,

$$\lambda = LAMBDA$$

then,

$$\Delta L = \frac{\lambda \cdot L_{eff} \cdot vds}{1 + LAM1 \cdot L_{eff}}$$

Note: The LEVEL 2 model has no LAM1 term.

The current is modified for channel length modulation effect in entire regions as:

$$ids = \frac{ids}{1 - \frac{\Delta L}{L_{eff}}}$$

CLM=7 Intersil Channel Length Modulation

The ΔL is only computed for the saturation region.

vds > vdsat

$$\Delta L = \frac{LAMBDA \cdot L_{eff}}{1 + LAM1 \cdot L_{eff}} \cdot (vds - vdsat)$$

and:

$$ids = \frac{ids}{L - \frac{\Delta L}{L_{eff}}}$$

CLM=8

The ΔL is only computed for the saturation region.

vds > vdsat

$$\Delta L = \frac{L_{eff}}{1 + \frac{(1 + LAM1 \cdot L_{eff}) \cdot (1 + vde)^{A1}}{LAMBDA \cdot (vds - vde)}}$$

and:

$$ids = \frac{ids}{1 - \frac{\Delta L}{L_{eff}}}$$

Subthreshold Current Ids

The LEVEL 8 model has different subthreshold current equations, depending on the value of model parameter CAV.

Define:

$$fast = vt \cdot \left[\eta + \frac{q \cdot NFS}{COX} + \frac{\gamma}{2 \cdot (vsb + \Phi)^{1/2}} + \frac{\varepsilon_{si} \cdot q \cdot SNVB \cdot \sqrt{vsb + \Phi}}{\gamma \cdot COX^2}\right]$$

CAV≠0

$$von = vth + CAV \cdot fast$$

Subthreshold Region, vgs < von

If vgs>vth

$$ids = ids(von, vde, vsb) \cdot e^{\left(-1-\frac{CAV}{2}\right)} \cdot e^{\left\{\left[\frac{1}{fast}-\frac{(CAV-2)\cdot(vgs-vth)}{2\cdot CAV^2\cdot fast^2}\right](vgs-vth)\right\}}$$

If vgs≤vth

$$ids = ids(von, vde, vsb) \cdot e^{\left(-1-\frac{CAV}{2}\right)} \cdot e^{\left(\frac{vgs-vth}{fast}\right)}$$

CAV=0

If CLM=8,

$$von = vth + 3 \cdot fast$$

otherwise,

$$von = vth + 2 \cdot fast$$

Subthreshold Region, vgs<von

$$ids = ids(von, vde, vsb) \cdot e^{\left(\frac{vgs-von}{fast}\right)}$$

If WIC=3, the subthreshold current is calculated differently. In this case the ids current is:

$$ids = ids(vgs, vde, vsb) + isub(N0eff, NDeff, vgs, vds)$$

N0eff and NDeff are functions of effective device width and length.

LEVEL 13 BSIM Model

The LEVEL 13 MOSFET model is an adaptation of BSIM (Berkeley Short Channel IGFET) from SPICE 2G.6 (SPICE). The model is formulated on the device physics of small-geometry MOS transistors. To invoke the subthreshold region, set the model parameter N0 (low field weak inversion gate drive coefficient) to less than 200. The Level 13 wire model (from resistor element), which is compatible with SPICE BSIM interconnect model for polysilicon and metal layers, simulates resistors and capacitors generated with interconnect. The capacitor model (from capacitor element) simulates capacitors generated with interconnect. The MOSFET diffusion model is compatible with the SPICE BSIM diffusion model.

Two different types of formats are available for specifying the BSIM model parameters. Enter the model parameters as a sequence of numbers similar to SPICE, or set them using model parameter assignments. When converting from SPICE to the Avant! models, the keyletter for the MOSFET device is S for SPICE BSIM and M for the Avant! model. (Refer to the example of the BSIM model circuit file at the end of this section.) Some model parameter names have been modified, due to the SPICE BSIM model installation.

BSIM Model Features

- Vertical field dependence of carrier mobility
- Carrier velocity saturation
- Drain-induced barrier lowering
- Depletion charge sharing by source and drain
- Non-uniform doping profile for ion-implanted devices
- Channel length modulation
- Subthreshold conduction
- Geometric dependence of electrical parameters

LEVEL 13 Model Parameters

Note: When reading parameter names, be aware of the difference in appearance between the upper case letter O, the lower case letter o, and the number zero (0).

For reference purposes only, the default values below are obtained from a medium size n-channel MOSFET device.

All LEVEL 13 parameters should be specified using NMOS conventions, even for PMOS (for example, ETA0=0.02, not ETA0=-0.02).

Transistor Process Parameters

Name (Alias)	Units	Default	Description
LEVEL		1	MOSFET model level selector, set to 13 for the BSIM model
CGBOM, (CGBO)	F/m	2.0e-10	Gate-to-bulk parasitic capacitance (F/m of length)
CGDOM, (CGDO)	F/m	1.5e-9	Gate-to-drain parasitic capacitance (F/m of width)
CGSOM, (CGSO)	F/m	1.5e-9	Gate-to-source parasitic capacitance (F/m of width)
DL0	µm	0.0	Difference between drawn poly and electrical
DW0	µm	0.0	Difference between drawn diffusion and electrical
DUM1		0.0	Dummy (not used)
DUM2		0.0	Dummy (not used)

Name (Alias)	Units	Default	Description
ETA0		0.0	Linear vds threshold coefficient
LETA	mm	0.0	Length sensitivity
WETA	µm	0.0	Width sensitivity
K1	$V^{1/2}$	0.5	Root-vsb threshold coefficient
LK1	$V^{1/2}$·µm	0.0	Length sensitivity
WK1	$V^{1/2}$·µm	0.0	Width sensitivity
K2		0.0	Linear vsb threshold coefficient
LK2	µm	0.0	Length sensitivity
WK2	µm	0.0	Width sensitivity
MUS	cm^2/(V·s)	600	High drain field mobility
LMS (LMUS)	µm cm^2/(V s)	0.0	Length sensitivity
WMS (WMUS)	µm cm^2/(V s)	0.0	Width sensitivity
MUZ	cm^2/(V·s)	600	Low drain field first order mobility
LMUZ	µm cm^2/(V s)	0.0	Length sensitivity
WMUZ	µm cm^2/(V s)	0.0	Width sensitivity

Name (Alias)	Units	Default	Description
N0		0.5	Low field weak inversion gate drive coefficient (a value of 200 for N0 disables weak inversion calculation)
LN0		0.0	Length sensitivity
WN0		0.0	Width sensitivity
NB0		0.0	Vsb reduction to low field weak inversion gate drive coefficient
LNB		0.0	Length sensitivity
WNB		0.0	Width sensitivity
ND0		0.0	Vds reduction to low field weak inversion gate drive coefficient
LND		0.0	Length sensitivity
WND		0.0	Width sensitivity
PHI0	V	0.7	Two times the Fermi potential
LPHI	V·µm	0.0	Length sensitivity
WPHI	V·µm	0.0	Width sensitivity
TREF	°C	25.0	Reference temperature of model (local override of TNOM)
TOXM, (TOX)	µm, (m)	0.02	Gate oxide thickness (TOXM or TOX >1 is interpreted as Angstroms)
U00	1/V	0.0	Gate field mobility reduction factor
LU0	µm/V	0.0	Length sensitivity
WU0	µm/V	0.0	Width sensitivity
U1	µm/V	0.0	Drain field mobility reduction factor

Name (Alias)	Units	Default	Description
LU1	$\mu m^2/V$	0.0	Length sensitivity
WU1	$\mu m^2/V$	0.0	Width sensitivity
VDDM	V	50	Critical voltage for high drain field mobility reduction
VFB0 (VFB)	V	-0.3	Flatband voltage
LVFB	V·µm	0.0	Length sensitivity
WVFB	V·µm	0.0	Width sensitivity
X2E	1/V	0.0	Vsb correction to linear vds threshold coefficient
LX2E	µm/V	0.0	Length sensitivity
WX2E	µm/V	0.0	Width sensitivity
X2M (X2MZ)	$cm^2/(V^2 \cdot s)$	0.0	Vsb correction to low field first order mobility
LX2M (LX2MZ)	$\mu m \cdot cm^2/(V^2 \cdot s)$	0.0	Length sensitivity
WX2M (WX2MZ)	$\mu m \cdot cm^2/(V^2 \cdot s)$	0.0	Width sensitivity
X2MS	$cm^2/(V^2\ s)$	0.0	Vbs reduction to high drain field mobility
LX2MS	$\mu m\ cm^2/(V^2\ s)$	0.0	Length sensitivity
WX2MS	$\mu m\ cm^2/(V^2\ s)$	0.0	Width sensitivity

Name (Alias)	Units	Default	Description
X2U0	$1/V^2$	0.0	Vsb reduction to GATE field mobility reduction factor
LX2U0	$\mu m/V^2$	0.0	Length sensitivity
WX2U0	$\mu m/V^2$	0.0	Width sensitivity
X2U1	$\mu m/V^2$	0.0	Vsb reduction to DRAIN field mobility reduction factor
LX2U1	$\mu m^2/V^2$	0.0	Length sensitivity
WX2U1	$\mu m^2/V^2$	0.0	Width sensitivity
X3E	1/V	0.0	Vds correction to linear vds threshold coefficient
LX3E	µm/V	0.0	Length sensitivity
WX3E	µm/V	0.0	Width sensitivity
X3MS	$cm^2/(V^2\ s)$	5.0	Vds reduction to high drain field mobility
LX3MS	$\mu m\ cm^2/(V^2\ s)$	0.0	Length sensitivity
WX3MS	$\mu m\ cm^2/(V^2\ s)$	0.0	Width sensitivity
X3U1	$\mu m/V^2$	0.0	Vds reduction to drain field mobility reduction factor
LX3U1	$\mu m^2/V^2$	0.0	Length sensitivity

Name (Alias)	Units	Default	Description
WX3U1	$\mu m^2/V_2$	0.0	Width sensitivity
XPART		1.0	Selector for gate capacitance charge-sharing coefficient

Diffusion Layer Process Parameters

Name (Alias)	Units	Default	Description
CJW, (CJSW)	F/m	0.0	Zero-bias bulk junction sidewall capacitance
CJM, (CJ)	F/m^2	4.5e-5	Zero-bias bulk junction bottom capacitance
DS	m	0.0	Average variation of size due to side etching or mask compensation (not used)
IJS, (JS)	A/m^2	0	Bulk junction saturation current
JSW	A/m	0.0	Sidewall bulk junction saturation current
MJ0, (MJ)		0.5	Bulk junction bottom grading coefficient
MJW, (MJSW)		0.33	Bulk junction sidewall grading coefficient
PJ, (PB)	V	0.8	Bulk junction bottom potential
PJW, (PHP)	V	0.8	Bulk junction sidewall potential
RSHM, (RSH)	ohm/sq	0.0	Sheet resistance/square
WDF	m	0.0	Default width of the layer (not used)

Note: The wire model includes poly and metal layer process parameters.

Basic Model Parameters

Name (Alias)	Units	Default	Description
LD (DLAT, LATD)	m		Lateral diffusion into channel from source and drain diffusion. ■ If LD and XJ are unspecified, then LD default=0.0 ■ If LD is unspecified but XJ is specified, LD is calculated from XJ. LD Default=0.75 · XJ LDscaled = LD · SCALM
LDAC	m		This parameter is the same as LD, but if LDAC is included in the .MODEL statement, it replaces LD in the Leff calculation for AC gate capacitance.
LMLT		1.0	Length shrink factor
LREF	m	0.0 *	Channel length reference LREFscaled = LREF · SCALM
WD	m	0.0	Lateral diffusion into channel from bulk along width WDscaled = WD · SCALM
WDAC	m		This parameter is the same as WD, but if WDAC is included in the .MODEL statement, it replaces WD in the Weff calculation for AC gate capacitance.
WMLT		1.0	Diffusion layer and width shrink factor

Name (Alias)	Units	Default	Description
XL (DL, LDEL)	m	0.0	Accounts for masking and etching effects XLscaled = XL · SCALM
XW (DW, WDEL)	m	0.0	Accounts for masking and etching effects XWscaled = XW · SCALM
WREF	m	0.0 *	Reference channel width WREFscaled = WREF · SCALM

Note: *If LREF and WREF are not defined in the model, they take a value of infinity. The default of 0.0 is for both Star-Hspice and Star-Sim simulators.

Temperature Parameters

Name (Alias)	Units	Default	Description
BEX		-1.5	Temperature exponent for MUZ and MUS mobility parameters
FEX		0.0	Temperature exponent for mobility reduction factor U1
TCV	V/°K	0.0	Flat-band voltage temperature coefficient
TREF	°C	25	Temperature at which parameters are extracted. This parameter defaults to the option *TNOM*, which defaults to 25 °C.

Sensitivity Factors of Model Parameters

For transistors, denote the L (channel length) and W (channel width) sensitivity factors of a basic electrical parameter are denoted by adding the characters ‘L’ and ‘W’ at the start of the name. For example, VFB0 sensitivity factors are LVFB and WVFB. If A0 is a basic parameter, then LA and WA are the corresponding L and W sensitivity factors of this parameter. LA and WA cannot be scaled using the SCALM option. The model uses the general formula below to obtain this parameter value.

$$A = A0 + LA \cdot \left(\frac{1}{Leff} - \frac{1}{LREFeff}\right) + WA \cdot \left(\frac{1}{Weff} - \frac{1}{WREFeff}\right)$$

LA and WA are specified in units of microns times the units of A0.

The left side of the equation represents the effective model parameter value after device size adjustment. All the effective model parameters are in lower case and start with the character “z”, followed by the parameter name.

Example

$$VFB0 = -0.350v$$

$$LVFB = -0.1v\mu$$

$$WVFB = 0.08v \cdot \mu$$

$$Leff = 1 \cdot 10^{-6}m = 1\mu$$

$$Weff = 2 \cdot 10^{-6}m = 2\mu$$

$$LREFeff = 2 \cdot 10^{-6}m = 2\mu$$

$$WREFeff = 1 \cdot 10^{-5}m = 10\mu$$

$$zvfb = VFB0 + LVFB \cdot \left(\frac{1}{Leff} - \frac{1}{LREFeff}\right) + WVFB \cdot \left(\frac{1}{Weff} - \frac{1}{WREFeff}\right)$$

$$zvfb = -0.35v + -0.1v \cdot \mu \cdot \left(\frac{1}{1\mu} - \frac{1}{2\mu}\right) + 0.08v \cdot \mu \cdot \left(\frac{1}{2\mu} - \frac{1}{10\mu}\right)$$

$$zvfb = -0.35v - 0.05v + 0.032v$$

$$zvfb = -0.368v$$

.MODEL VERSION Changes to BSIM Models

The VERSION parameter to the .MODEL statement allows portability of LEVEL 13 BSIM and LEVEL 39 BSIM2 models between versions. Using the VERSION parameter in a LEVEL 13 .MODEL statement results in the following changes to the BSIM model:

Model Version	**Effect of VERSION on BSIM model**
9007B	LEVEL 13 BSIM model introduced: no changes
9007D	Removes the K2 limit
92A	Changes the TOX parameter default from 1000 A to 200 A
92B	Adds the K2LIM parameter, which specifies the K2 limit
93A	Introduces gds constraints
93A.02	VERSION parameter introduced
95.1	Fixes nonprinting TREF and incorrect GMBS problems
96.1	Flatband voltage temperature adjustment has been changed

LEVEL 13 Equations

This section lists the LEVEL 13 model equations.

Effective Channel Length and Width

The effective channel length and width for LEVEL 13 is determined differently, depending on the specified model parameters.

If DL0 is specified then,

$$Leff = Lscaled \cdot LMLT - DL0 \cdot 1e\text{-}6$$

$$LREFeff = LREFscaled \cdot LMLT - DL0 \cdot 1e\text{-}6$$

Otherwise, if XL or LD is specified,

$$Leff = Lscaled \cdot LMLT + XLscaled - 2 \cdot LDscaled$$

$$LREFeff = LREFscaled \cdot LMLT + XLscaled - 2 \cdot LDscaled$$

If DW0 is specified, then

$$Weff = Wscaled \cdot WMLT - DW0 \cdot 1e\text{-}6$$

$$WREFeff = WREFscaled \cdot WMLT - DW0 \cdot 1e\text{-}6$$

Otherwise, if XW or WD is specified, then

$$Weff = Wscaled \cdot WMLT + XWscaled - 2 \cdot WDscaled$$

$$WREFeff = WREFscaled \cdot WMLT + XWscaled - 2 \cdot WDscaled$$

IDS Equations

The device characteristics are modeled by process-oriented model parameters, which are mapped into model parameters at a specific bias voltage. The ids equations are as follows:

Cutoff Region, vgs ≤ vth

$$ids = 0 \quad \textit{(see subthreshold current)}$$

On Region, vgs >vth

For vds < vdsat, triode region:

$$ids = \frac{\beta}{1 + xu1 \cdot vds} \cdot \left[(vgs - vth) \cdot vds - \frac{body}{2} \cdot vds^2 \right]$$

For vds ≥ vdsat, saturation region:

$$ids = \frac{\beta}{2 \cdot body \cdot arg} \cdot (vgs - vth)^2$$

where:

$$\beta = ueff \cdot COX \cdot \frac{Weff}{Leff}$$

$$ueff = \frac{uo}{1 + xu0 \cdot (vgs - vth)}$$

$$xu0 = zu0 - zx2u0 \cdot vsb$$

The carrier mobility, uo, is calculated by quadratic interpolation through three data points.

$$uo|_{vds = 0} = MUZ - zx2mz \cdot vsb$$

$$uo|_{vds = VDDM} = zmus - zx2ms \cdot vsb$$

and the sensitivity of uo to vds at vds=VDDM, which is zx3ms.

The “body” factor is calculated by:

$$body = 1 + \frac{g \cdot zk1}{2 \cdot (zphi + vsb)^{1/2}}$$

where:

$$g = 1 - \frac{1}{1.744 + 0.8364 \cdot (zphi + vsb)}$$

The “arg” term in saturation region current is calculated by:

$$\text{arg} = \frac{1}{2} \cdot [1 + \text{vc} + (1 + 2 \cdot \text{vc})^{1/2}]$$

where:

$$\text{vc} = \frac{\text{xu1} \cdot (\text{vgs} - \text{vth})}{\text{body}}$$

and:

$$\text{xu1} = \text{zu1} - \text{zx2u1} \cdot \text{vsb} + \text{zx3u1} \cdot (\text{vds} - \text{VDDM}), \quad \textit{UPDATE=2}$$

$$\text{xu1} = \frac{\text{zu1} - \text{zx2u1} \cdot \text{vsb} + \text{zx3u1} \cdot (\text{vds} - \text{VDDM})}{\text{Leff}}, \quad \textit{UPDATE=0, 1}$$

Threshold Voltage

The threshold voltage can be expressed as:

$$\text{vth} = \text{zvfb} + \text{zphi} + \text{gamma} \cdot (\text{zphi} + \text{vsb})^{1/2} - \text{xeta} \cdot \text{vds}$$

where

$$\text{gamma} = \text{zk1} - \text{zk2} \cdot (\text{zphi} + \text{vsb})^{1/2}$$

and:

$$\text{xeta} = \text{zeta} - \text{zx2e} \cdot \text{vsb} + \text{zx3e} \cdot (\text{vds} - \text{VDDM}), \quad \textit{UPDATE=0, 2}$$

$$\text{xeta} = \text{zeta} + \text{zx2e} \cdot (\text{zphi} + \text{vsb}) + \text{zx3e} \cdot (\text{vds} - \text{VDDM}), \quad \text{UPDATE=1}$$

Saturation Voltage (vdsat)

The saturation voltage in the BSIM model is calculated as follows:

$$\text{vdsat} = \frac{\text{vgs} - \text{vth}}{\text{body} \cdot \text{arg}^{1/2}}$$

Subthreshold Current ids

The subthreshold current isub is calculated when zn0 is less than 200 as follows:

$$isub = \frac{Ilim \cdot Iexp}{Ilim + Iexp}$$

where:

$$Iexp = \beta_o \cdot vt^2 \cdot e^{1.8} \cdot e^{\frac{vgs - vth}{xn \cdot vt}} \cdot \left(1 - e^{-\frac{vds}{vt}}\right)$$

$$Ilim = 4.5 \cdot \beta_o \cdot vt^2$$

$$\beta_o = uo \cdot COX \cdot \frac{Weff}{Leff}$$

and:

$$xn = zn0 - znb \cdot vsb + znd \cdot vds$$

Note: The current isub also is added to the ids current in the strong inversion.

Resistors and Capacitors Generated with Interconnects

See the wire model table (resistor element) for the model parameters used.

Resistances:

$$r = RSH \cdot \frac{Leff}{Weff}$$

Capacitances:

$$c = COX \cdot Leff \cdot Weff + 2 \cdot CAPSW \cdot (Leff + Weff)$$

Temperature Effect

$$MUZ(t) = MUZ \cdot \left(\frac{t}{tnom}\right)^{BEX} \quad UPDATE=0, 1$$

$$zmus(t) = zmus \cdot \left(\frac{t}{tnom}\right)^{BEX} \quad UPDATE=0, 1$$

$$uo(t) = uo\left(\frac{t}{tnom}\right)^{BEX} \quad UPDATE=2$$

$$xu1(t) = xu1 \cdot \left(\frac{t}{tnom}\right)^{FEX}$$

$$zvfb(t) = zvfb - \Delta t \cdot TCV$$

where:

$$\Delta t = t - tnom$$

Charge-Based Capacitance Model

The LEVEL 13 capacitance model conserves charge and has nonreciprocal attributes. Using charge as the state variable guarantees charge conservation. You can get total stored charge in each of the gate, bulk, and channel regions by integrating the distributed charge densities/area of the active region.

The channel charge is partitioned into drain and source components in two physically significant methods by using the model parameter XPART: 40/60, or 0/100 in the saturation region, which smoothly changes to 50/50 in the triode region. XPART=0 selects 40/60 drain/source charge-partitioning in the saturation region, while XPART=1 and XPART=0.5 select 0/100 and 50/50 for drain/source charge-partitioning in the saturation region, respectively.

Define:

$$vtho = zvfb + zphi + zk1 \cdot (zphi + vsb)^{1/2}$$

$$cap = COX \cdot Leff \cdot Weff$$

$$vpof = \frac{vgs - vtho}{body}$$

$$argx = \frac{body \cdot vds}{12 \cdot (vgs - vtho - 0.5 \cdot body \cdot vds)}$$

If $(vgs - vtho - 0.5 \cdot body \cdot vds) \leq 1e\text{-}8$ then,

$$argx = \frac{1}{6}$$

$$argy = \frac{(vgs - vtho)^2 - 0.75 \cdot body \cdot (vgs - vtho) \cdot vds + 0.15 \cdot body^2 \cdot vds^2}{6 \cdot (vgs - vtho - 0.5 \cdot body \cdot vds)^3}$$

If $(vgs - vtho - 0.5 \cdot body \cdot vds) \leq 1e\text{-}8$ then,

$$argy = \frac{4}{15}$$

Regions Charge Expressions

Accumulation Region, vgs ≤ vtho, vgs ≤ zvfb - vsb

$$Qg = cap \cdot (vgs - zvfb + vsb)$$

$$Qb = -qg$$

$$Qs = 0$$

$$Qd = 0$$

Subthreshold Region, vgs ≤ vtho, vgs >zvfb - vsb

$$Qg = \frac{cap \cdot zk1}{2} \cdot \left\{ [(zk1)^2 + 4(vgs - zvfb + vsb)]^{1/2} - zk1 \right\}$$

$$Qb = -qg$$

$$Qs = 0$$

50/50 Channel-Charge Partitioning for Drain and Source, XPART=.5

Triode Region, vgs >vtho, vds ≤ vpof

$$Qg = cap \cdot (vgs - zvfb - zphi - 0.5 \cdot vds + vds \cdot argx)$$

$$Qb = cap \cdot [-vtho + zvfb + zphi + (1 - body) \cdot (0.5 - argx) \cdot vds]$$

$$Qd = -0.5 \cdot (qg + qb)$$

$$Qs = Qd$$

Saturation Region, vgs >vtho, vds >vpof

$$Qg = cap \cdot \left(vgs - zvfb - zphi - \frac{vgs - vtho}{3 \cdot body} \right)$$

$$Qb = cap \cdot \left[zvfb + zphi - vtho + (1 - body) \cdot \frac{(vgs - vtho)}{3 \cdot body} \right]$$

$$Qd = -\frac{cap}{3} \cdot (vgs - vtho)$$

$$Qs = Qd$$

40/60 Channel-Charge Partitioning for Drain and Source, XPART=0

Triode Region, vgs >vtho, vds ≤ vpof

$$Qg = cap \cdot (vgs - xvfb - zphi - 0.5 \cdot vds + argx \cdot vds)$$

$$Qb = cap \cdot [-vtho + zvfb + zphi + (1 - body) \cdot (0.5 - argx) \cdot vds]$$

$$Qd = -(cap \cdot [0.5 \cdot (vgs - vtho - body \cdot vds) + body \cdot argy \cdot vds])$$

$$Qs = -(Qg + Qb + Qd)$$

Saturation Region, vgs> vtho, vds >vpof

$$Qg = cap \cdot \left(vgs - zvfb - zphi - \frac{vgs - vtho}{3 \cdot body}\right)$$

$$Qb = cap \cdot \left[zvfb + zphi - vtho + (1 - body) \cdot \frac{(vgs - vtho)}{3 \cdot body}\right]$$

$$Qd = -\frac{4 \cdot cap}{15} \cdot (vgs - vtho)$$

$$Qs = \frac{3}{2} \cdot Qd$$

0/100 Channel-Charge Partitioning for Drain and Source, XPART=1

Triode Region, vgs >vtho, vds ≤ vpof

$$Qg = cap \cdot (vgs - zvfb - zphi - 0.5 \cdot vds + vds \cdot argx)$$

$$Qb = cap \cdot [-vtho + zvfb + zphi + (1 - body) \cdot (0.5 - argx) \cdot vds]$$

$$Qd = -(cap \cdot [0.5 \cdot (vgs - vtho) - body \cdot vds \cdot (0.75 - 1.5 \cdot argx)])$$

$$Qs = -(Qg + Qb + Qd)$$

Saturation Region, vgs >vtho, vds >vpof

$$Qg = cap \cdot \left(vgs - zvfb - zphi - \frac{vgs - vtho}{3 \cdot body} \right)$$

$$Qb = cap \cdot \left[zvfb + zphi - vtho + (1 - body) \cdot \frac{(vgs - vtho)}{3 \cdot body} \right]$$

$$Qd = 0$$

$$Qs = -Qg - Qb$$

Prevention of Negative Output Conductance

The LEVEL 13 model internally protects against conditions that might cause convergence problems, due to negative output conductance. The constraints imposed are:

$$ND \geq 0$$

$$MUS \geq MUZ + X3MS + VDD(M/2)$$

These constraints are imposed after length and width adjustment and *VBS* dependence. This feature is gained at the expense of some accuracy in the saturation region, particularly at high Vgs.

Consequently, you might need to qualify BSIM1 models again, if the following occur:

1. Devices exhibit self-heating during characterization, which causes declining I_{ds} at high V_{ds}. This would not occur if the device characterization measurement sweeps V_{ds}.
2. Extraction produces parameters that result in negative conductance.
3. Voltage simulation is attempted outside the characterized range of the device.

Calculations Using LEVEL 13 Equations

To verify the equations, it is helpful to do very simple simulation and analysis tests, and check the results with a hand calculator. Check threshold, vdsat, and ids for a very simple model, with many parameters set to zero. There is no series resistance, RSH=0. Diode current has been turned off, JS=JSW=IS=0. The LEVEL 13 subthreshold current has been turned off by n0=200. The geometry parameters are set to zero, so Leff=L=1u, Weff=W=1u.

A value of TOX has been chosen to give:

$$cox = \frac{2.00000e-3F}{m^2}$$

The test is at vbs=-0.35, so that phi-vbs=1.0:

```
$ t1
.option ingold=2 numdgt=6
vd d 0 5
vg g 0 5
vb b 0 -0.35
m1 d g 0 b nch w=10u L=1u
.dc vd 4 5 1
.print ids=lx4(m1) vth=lv9(m1) vdsat=lv10(m1)
.model nch nmos LEVEL=13
+ vfb0=-0.4 lvfb=0 wvfb=0
+ phi0=0.65 lphi=0 wphi=0
+ k1=0.5 lk1=0 wk1=0
+ k2=0 lk2=0 wk2=0
+ eta0=1e-3 leta=0 weta=0
+ muz=600 mus=700 x3ms=10
+ xl=0 ld=0 xw=0 wd=0
+ u00=0 lu0=0 wu0=0
+ u1=0 lu1=0 wu1=0
+ tox=172.657
+ acm=2 rsh=0 js=0 jsw=0 is=0 n0=200
.end
```

Simulation Results

```
ids         vth         vdsat
1.09907e-02 7.45000e-01 3.69000e+00
```

Calculations at vgs=vds=5, vbs=-0.35

$$\text{phi} - \text{vbs} = 1$$

$$\text{vth} = -0.4 + 0.65 + (0.5 \cdot 1) - (\text{ETA} \cdot \text{vds}) = 0.75 - (0.001 \cdot \text{vds}) = 0.745$$

$$g = 1 - \frac{1}{(1.744 + 0.8364 \cdot 1)} = 0.612463$$

$$\text{body} = 1 + \frac{g \cdot 0.5}{(2 \cdot 1)} = 1 + 0.25 \cdot g = 1.153116$$

$$\text{vc} = \textit{0 arg = 1}$$

$$\text{vdsat} = \frac{(\text{vgs} - \text{vth})}{\text{body} \cdot \sqrt{(\text{arg})}} = \frac{(5 - 0.745)}{\text{body}} = 3.69000$$

At vds=VDDM (default VDDM=5), mobility=mus=700

$$\text{ids} = \text{cox} \cdot \left(\frac{\text{Weff}}{\text{Leff}}\right) \cdot 700 \cdot \frac{(\text{vgs} - \text{vth})^2}{(2 \cdot \text{body} \cdot \text{arg})}$$

$$\text{ids} = \left(\frac{10 \cdot 700 \cdot 4.255^2}{2 \cdot 1.15311 \cdot 1}\right) \cdot \text{cox} = 54953.36 \cdot \text{cox}$$

$$\text{ids} = 1.09907\text{e} - 2$$

These calculations agree with the simulation results above.

Compatibility Notes

Model Parameter Naming

The following names are HSPICE-specific: U00, DL0, DW0, PHI0, ETA0, NB0, ND0. A zero was added to the SPICE names to avoid conflicts with other standard parameter names. For example, U0 cannot be used because it is an alias for UB, the mobility parameter in many other levels. DL cannot be used because it is an alias for XL, a geometry parameter available in all levels.

This model supports the use of DL0 and DW0, but the use of XL, LD, XW, WD is recommended instead (noting the difference in units).

Watch the units of TOX. It is safest to enter a number greater than one, which is always interpreted as Angstroms.

To avoid negative gds:

1. Set X3U1, LX3U1 and WX3U1 to zero.
2. Check that

   zx3ms>=0, where zx3ms=X3MS, with L, W adjustment
3. Check that

   zmuz+VDDM · zx3ms<zmus

SPICE/True-Hspice Model Parameter Differences

A cross-reference table for UCB's BSIM1 and the Avant! LEVEL 13 model parameters is provided for comparison. Units are given in brackets. The model parameter name is used only if it differs from the SPICE name. The model specifies parameter units only if they differ from SPICE units. These aliases are in parentheses. Note that some parameter aliases match the SPICE names.

An asterisk (*) in front of a UCB SPICE name denotes an incompatibility between the parameter name in the Avant! True-Hspice model and the UCB SPICE name (that is, the parameter alias does not match, or units are different).

Even when there is a difference in parameter name between this model and SPICE, the corresponding L and W sensitivity parameter names might not differ. L and W sensitivity parameters are only listed for the few cases for which there is a difference.

Table 9-1: Comparing Avant! Model Parameters and UCB SPICE 2/3 (Sheet 1 of 3)

UC Berkeley SPICE 2, 3	Avant! True-Hspice Model
VFB [V]	VFB0 (VFB)
PHI [V]	PHI0
K1 [$V^{1/2}$]	same

Table 9-1: Comparing Avant! Model Parameters and UCB SPICE 2/3 (Sheet 2 of 3)

UC Berkeley SPICE 2, 3	Avant! True-Hspice Model
K2	same
* ETA	ETA0
MUZ [$cm^2/V{\cdot}s$]	same
* DL [µm]	DL0
* DW [µm]	DW0
* U0 [1/V]	U00
* U1 [µ/V]	same
X2MZ [$cm^2/V^2{\cdot}s$]	X2M (X2MZ)
LX2MZ [$\mu m{\cdot}cm^2/V^2{\cdot}s$]	X2M (LX2MZ)
WX2MZ [$\mu m{\cdot}cm^2/V^2{\cdot}s$]	WX2M (WX2MZ)
X2E [1/V]	same
X3E [1/V]	same
X2U0 [$1/V^2$]	same
X2U1 [$\mu m/V^2$]	same
MUS [$cm^2/V{\cdot}s$]	same
LMUS [$\mu m{\cdot}cm^2/V{\cdot}s$]	LMS (LMUS)
WMUS [$\mu m{\cdot}cm^2/V{\cdot}s$]	WMS (WMUS)
X2MS [$cm^2/V^2{\cdot}s$]	same
X3MS [$cm^2/V^2{\cdot}s$]	same

Table 9-1: Comparing Avant! Model Parameters and UCB SPICE 2/3 (Sheet 3 of 3)

UC Berkeley SPICE 2, 3	Avant! True-Hspice Model
X3U1 [μm/V^2]	same
* TOX [μm]	TOXM[μ] (TOX[m])
* TEMP [°C]	TREF
* VDD [V]	VDDM
CGDO [F/m]	CGDOM (CGDO)
CGSO [F/m]	CGSOM (CGSO)
CGBO [F/m]	CGBOM (CGBO)
XPART	same
N0	same
* NB	NB0
* ND	ND0
RSH [ohm/sq]	RSHM (RSH)
JS [A/m^2]	IJS (JS)
PB [V]	PJ (PB)
MJ	MJ0 (MJ)
* PBSW [V]	PJW (PHP)
MJSW	MJW (MJSW)
CJ [F/m^2]	CJM (CJ)
CJSW [F/m]	CCJW (CJSW)
* WDF [m]	–
* DELL [m]	–

In UCB SPICE, you must specify all BSIM model parameters. The Avant! model provides defaults for the parameters.

Parasitics

ACM >0 invokes parasitic diode models. ACM=0 (default) is SPICE style.

Temperature Compensation

The model reference temperature TNOM's default is 25˚C, unless you set .OPTION SPICE, causing TNOM to default to 27˚C. This option also sets some other SPICE compatibility parameters. You set TNOM in an .OPTION line in the netlist, and you can always override it locally (that is, for a model) with model parameter TREF. (The model "reference temperature" means that the model parameters were extracted at and are valid at that temperature).

In UCB SPICE, TNOM (default 27˚C) is not effective for BSIM, and the model parameter TEMP is used instead (and must be specified) as both the model reference temperature and analysis temperature. The analysis at TEMP only applies to thermally activated exponentials in the model equations. There is no adjustment of model parameter values with TEMP. It is assumed that the model parameters were extracted at TEMP, TEMP being both the reference and the analysis temperature.

In contrast to UCB SPICE's BSIM, the Avant! LEVEL 13 model does provide for temperature analysis. The default analysis temperature is 25˚C (and 27˚C in UCB SPICE for all model levels except for BSIM, as explained in the previous paragraph). Use a .TEMP statement in the netlist to change the analysis temperature.

The LEVEL 13 model provides two temperature coefficients: TCV and BEX. Threshold voltage is adjusted by

$$vth(t) = vth - TCV \cdot (t - tnom)$$

There are two implementations of the BEX factor, selected by the UPDATE parameter, which is described in the next section. The mobility in BSIM is a combination of five quantities: MUZ, zmus, z3ms, zx2mz, and zx2ms.

BEX Usage

$$MUZ(t) = MUZ \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$zmus(t) = zmus \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$zx3ms(t) = zx3ms \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$zx2mz(t) = zx2mz \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$zx2ms(t) = zx2ms \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

This is equivalent to multiplying the final mobility by the factor:

$$\left(\frac{t}{tnom}\right)^{BEX}$$

UPDATE Parameter

The UPDATE parameter selects between variations of the BSIM equations. UPDATE=0 is the default, which is consistent with UCB SPICE3. UPDATE=3 also is consistent with UCB SPICE3 and BEX usage.

Here is the sequence of UPDATE choices, which were responses to specific customer requests.

UPDATE=0	UCB compatible, previous BEX usage
UPDATE=1	Special X2E equation, previous BEX usage
UPDATE=2	Remove 1/Leff in U1 equation, present BEX usage
UPDATE=3	UCB compatible, present BEX usage

Explanations

The normal X2E equation is

$$xeta = zeta - (zx2e \cdot vsb) + zx3e \cdot (vds - VDDM)$$

The special X2E equation, for UPDATE=1 only, is

$$xeta = zera + zx2e \cdot (zphi + vsb) + zx3e \cdot (vds - VDDM)$$

The special X2E equation was requested to match a parameter extraction program. Whenever you use a parameter extraction program, the equations should be checked carefully.

The original U1 equation divides by Leff in microns,

$$xu1 = \frac{(zu1 - (zx2u1 \cdot vsb) + zx3u1 \cdot (vds - VDDM))}{Leff}$$

This is one of the few places where Leff enters explicitly into the BSIM equations; usually the Leff variation is handled by the L-adjustment model parameters, such as LU1. Physically xu1 should decrease as 1/Leff at long channels, but when dealing with short-channel devices, you can turn off this variation. Set UPDATE=2 to remove the 1/Leff factor in the xu1 equation.

UPDATE=2 introduces the present BEX usage as the 1/Leff removal ability. UPDATE=3 provides the present BEX usage with the previous xu1 equation.

IDS and VGS Curves for PMOS and NMOS

```
FILE:ML13IV.SP IDS AND VGS CURVES FOR PMOS AND NMOS
```

Two Different Types Of Model Parameter Formats Used

```
.OPTIONS ACCT LIST NOPAGE
.OP
.DC VDDN 0 5.0 .1 VBBN 0 -3 -3

*N-CHANNEL I D S CURVES (VD=0 to 5, VG=1,2,3,4,5, VB=0,-3)
.PRINT DC I(VN1) I(VN2) I(VN3) I(VN4) I(VN5) V(90)
.PLOT DC I(VN1) I(VN2) I(VN3) I(VN4) I(VN5)

*P-CHANNEL I D S CURVES (VD=0 to -5,VG=-1,-2,-3,-4,-5,VB=0,3)
.PRINT DC I(VP1) I(VP2) I(VP3) I(VP4) I(VP5) V(90)
.PLOT DC I(VP1) I(VP2) I(VP3) I(VP4) I(VP5)
```

VGS Curves

```
.PRINT DC I(VN6) I(VP6)
.PLOT DC I(VN6) I(VP6)
* N-CHANNEL LX7=GM (VD=5,     VG=0 to ->5, VS=0, VB=0,-3)
* N-CHANNEL LX8=GD (VD=0 to 5,VG=5,        VS=0, VB=0,-3)
* N-CHANNEL LX9=GB (VD=5,     VG=5,        VS=0, VB=0 to -5)
.PLOT DC LX7(M21) LX8(M5) LX9(M31)

* P-CHANNEL LX7=GM (VD=0,      VG=0->-5,   VS=-5VB=0,3)
* P-CHANNEL LX8=GD (VD=0 to -5,VG=-5,      VS=-5,VB=0,3)
* P-CHANNEL LX9=GB (VD=0,      VG=0,       VS=-5,VB=0- >5)
.PLOT DC LX7(M22) LX8(M15) LX9(M32)
*
VDDN 99 0 5.0
VBBN 90 0 0
EPD 98 0 99 0 -1
EPB 91 0 90 0 -1

V1 1 0 1
V2 2 0 2
V3 3 0 3
V4 4 0 4
V5 5 0 5
V11 11 0 -1
V12 12 0 -2
V13 13 0 -3
V14 14 0 -4
V15 15 0 -5
*

VN1 99 31 0
VN2 99 32 0
VN3 99 33 0
VN4 99 34 0
VN5 99 35 0

M1 31 1 0 90 PC_NM1 8U 8U
M2 32 2 0 90 PC_NM1 8U 8U
M3 33 3 0 90 PC_NM1 8U 8U
M4 34 4 0 90 PC_NM1 8U 8U
M5 35 5 0 90 PC_NM1 8U 8U
*
VP1 98 41 0
```

```
VP2 98 42 0
VP3 98 43 0
VP4 98 44 0
VP5 98 45 0

M11 41 11 0 91 PC_PM1 8U 8U
M12 42 12 0 91 PC_PM1 8U 8U
M13 43 13 0 91 PC_PM1 8U 8U
M14 44 14 0 91 PC_PM1 8U 8U
M15 45 15 0 91 PC_PM1 8U 8U
```

GM Test

```
VN6 5 36 0
VP6 0 46 0
M21 36 99 0 90 PC_NM1 8U 8U
M22 46 98 15 91 PC_PM1 8U 8U
```

GM B CVN7 5 37 0

```
VP7 0 47 0
M31 37 5 0 98 PC_NM1 8U 8U
M32 47 0 15 99 PC_PM1 8U 8U
```

.PROCESS PC Filename=M57R

```
* Preliminary MOSIS BSIM parameters for SPICE3:
* The following parameters were extracted from a MOSIS
* experimental 1.2 um fabrication run.
```

For N-channel Devices

```
* NM1 PM1 PY1 ML1 ML2 DU1 DU2
*PROCESS=PC1
*RUN=m57r
*WAFER=11
*OPERATOR=david & ming
*DATE=6/12/87
```

First Model Parameter Format

```
*nmos model
.MODEL PC_NM1 NMOS LEVEL=13 VFB0=
+-8.27348E-01, 1.42207E-01, 3.48523E-02
+ 7.87811E-01, 0.00000E+00, 0.00000E+00
```

```
+ 9.01356E-01,-1.96192E-01, 1.89222E-02
+ 4.83095E-02,-4.10812E-02,-2.21153E-02
+ 2.11768E-03, 3.04656E-04,-1.14155E-03
+ 4.93528E+02, 5.39503E-02, 4.54432E-01
+ 5.81155E-02, 4.95498E-02,-1.96838E-02
+-5.88405E-02, 6.06713E-01, 4.88790E-03
+ 9.22649E+00,-8.66150E+00, 9.55036E+00
+-7.95688E-04, 2.67366E-03, 3.88974E-03
+ 2.14262E-03,-7.19261E-04,-3.56119E-03
+ 2.05529E-03,-3.66841E-03, 1.86866E-03
+-1.64733E-02,-3.63561E-03, 3.59209E-02
+ 4.84793E+02, 3.14763E+02,-3.91874E+01
+-4.21265E+00,-7.97847E+00, 3.50692E+01
+-5.83990E+00, 6.64867E+01,-1.99620E+00
+-1.44106E-02, 8.14508E-02, 7.56591E-04
+ 2.30000E-02, 2.30000E+01, 5.00000E+00
+ 5.04000E-10, 5.04000E-10, 1.91000E-09
+ 1.00000E+00, 0.00000E+00, 0.00000E+00
+ 2.00000E+02, 0.00000E+00, 0.00000E+00
+ 0.00000E+00, 0.00000E+00, 0.00000E+00
+ 0.00000E+00, 0.00000E+00, 0.00000E+00
*n+ diffusion layer
+80.0,7.000E-004,4.20E-010,1.00E-008,0.700E000
+0.8000e000,0.5,0.33,0,0
```

PMOS Model

```
.MODEL PC_PM1 PMOS LEVEL=13 VFB0=
+-5.63441E-01,-1.06809E-01, 1.32967E-01
+ 7.46390E-01, 0.00000E+00, 0.00000E+00
+ 6.57533E-01, 1.94464E-01,-1.60925E-01
+-2.55036E-03, 1.14752E-01,-8.78447E-02
+-5.59772E-03, 2.50199E-02,-5.66587E-04
+ 1.73854E+02, 2.72457E-01, 6.57818E-01
+ 1.26943E-01, 4.25293E-02,-4.31672E-02
+-1.00718E-02, 1.50900E-01,-1.00228E-02
+ 1.03128E+01,-3.94500E+00, 1.87986E+00
+ 1.55874E-03, 4.80364E-03,-1.45355E-03
+ 4.20214E-04,-2.05447E-03,-7.44369E-04
+ 1.00044E-02,-4.43607E-03, 1.05796E-03
+-5.64102E-04, 1.97407E-03, 6.65336E-04
+ 1.77550E+02, 1.02937E+02,-2.94207E+01
```

```
+ 8.73183E+00, 1.51499E+00, 9.06178E-01
+ 1.11851E+00, 9.75265E+00,-1.88238E+00
+-4.70098E-05, 9.43069E-04,-9.19946E-05
+ 2.30000E-02, 2.30000E+01, 5.00000E+00
+ 1.00000E-09, 1.00000E-09, 1.91000E-09
+ 1.00000E+00, 0.00000E+00, 0.00000E+00
+ 2.00000E+02, 0.00000E+00, 0.00000E+00
+ 0.00000E+00, 0.00000E+00, 0.00000E+00
+ 0.00000E+00, 0.00000E+00, 0.00000E+00
*p+ diffusion layer
+140.0,4.0E-004,2.4E-010,1.00E-008,0.700E000
+0.8000e000,0.5,0.33,0,0
```

Wire Model for Poly and Metal Layers

```
*NOT REFERENCED BY ANY ELEMENTS IN THIS CIRCUIT,
*JUST FOR MODEL EXAMPLES.
.MODEL PC_PY1 R
*poly layer
+ 65.0
.MODEL PC_ML1 R
*metal layer 1
+ 0.200
$$$$$$$
.ALTER
$$$$$$$
```

Second Model Parameter Format

```
*nmos model
.MODEL PC_NM1 NMOS LEVEL=13
+ VFB0=-8.27348E-01 LVFB=1.42207E-01   WVFB=3.48523E-02
+ PHI0=7.87811E-01 LPHI=0.00000E+00   WPHI=0.00000E+00
+ K1=9.01356E-01    LK1=-1.96192E-01   WK1=1.89222E-02
+ K2=4.83095E-02    LK2=-4.10812E-02   WK2=-2.21153E-02
+ ETA0=2.11768E-03 LETA=3.04656E-04   WETA=-1.14155E-03
+ MUZ=4.93528E+02   DL0=5.39503E-02    DW0=4.54432E-01
+ U00=5.81155E-02   LU0=4.95498E-02    WU0=-1.96838E-02
+ U1=-5.88405E-02   LU1=6.06713E-01    WU1=4.88790E-03
+ X2M=9.22649E+00   LX2M=-8.66150E+00 WX2M=9.55036E+00
+ X2E=-7.95688E-04 LX2E=2.67366E-03   WX2E=3.88974E-03
+ X3E=2.14262E-03   LX3E=-7.19261E-04 WX3E=-3.56119E-03
+ X2U0=2.05529E-03 LX2U0=-3.66841E-03 WX2U0=1.86866E-03
```

```
+ X2U1=-1.64733E-02 LX2U1=-3.63561E-03 WX2U1=3.59209E-02
+ MUS=4.84793E+02   LMS=3.14763E+02    WMS=-3.91874E+01
+ X2MS=-4.21265E+00 LX2MS=-7.97847E+00 WX2MS=3.50692E+01
+ X3MS=-5.83990E+00 LX3MS=6.64867E+01 WX3MS=-1.99620E+00
+ X3U1=-1.44106E-02 LX3U1=8.14508E-02 WX3U1=7.56591E-04
+ TOXM=2.30000E-02 TEMPM=2.30000E+01 VDDM=5.00000E+00
+ CGDOM=5.04000E-10 CGSOM=5.04000E-10 CGBOM=1.91000E-09
+ XPART=1.00000E+00 DUM1=0.00000E+00   DUM2=0.00000E+00
+ N0=2.00000E+02    LN0=0.00000E+00    WN0=0.00000E+00
+ NB0=0.00000E+00   LNB=0.00000E+00    WNB=0.00000E+00
+ ND0=0.00000E+00   LND=0.00000E+00    WND=0.00000E+00
```

N+ Diffusion Layer

```
+ RSHM=80.0         CJM=7.000E-004     CJW=4.20E-010
+ IJS=1.00E-008     PJ=0.700E000
+ PJW=0.8000E000    MJ0=0.5            MJW=0.33
+ WDF=0             DS=0
```

PMOS Model

```
.MODEL PC_PM1 PMOS LEVEL=13
+ VFB0=-5.63441E-01 LVFB=-1.06809E-01   WVFB=1.32967E-01
+ PHI0=7.46390E-01 LPHI=0.00000E+00    WPHI=0.00000E+00
+ K1=6.57533E-01    LK1=1.94464E-01     WK1=-1.60925E-01
+ K2=-2.55036E-03   LK2=1.14752E-01     WK2=-8.78447E-02
+ ETA0=-5.59772E-03 LETA=2.50199E-02    WETA=-5.66587E-04
+ MUZ=1.73854E+02   DL0=2.72457E-01     DW0=6.57818E-01
+ U00=1.26943E-01   LU0=4.25293E-02     WU0=-4.31672E-02
+ U1=-1.00718E-02   LU1=1.50900E-01     WU1=-1.00228E-02
+ X2M=1.03128E+01   LX2M=-3.94500E+00   WX2M=1.87986E+00
+ X2E=1.55874E-03   LX2E=4.80364E-03    WX2E=-1.45355E-03
+ X3E=4.20214E-04   LX3E=-2.05447E-03   WX3E=-7.44369E-04
+ X2U0=1.00044E-02 LX2U0=-4.43607E-03 WX2U0=1.05796E-03
+ X2U1=-5.64102E-04 LX2U1=1.97407E-03   WX2U1=6.65336E-04
+ MUS=1.77550E+02   LMS=1.02937E+02     WMS=-2.94207E+01
+ X2MS=8.73183E+00 LX2MS=1.51499E+00   WX2MS=9.06178E-01
+ X3MS=1.11851E+00 LX3MS=9.75265E+00   WX3MS=-1.88238E+00
+ X3U1=-4.70098E-05 LX3U1=9.43069E-04   WX3U1=-9.19946E-05
+ TOXM=2.30000E-02 TEMPM=2.30000E+01   VDDM=5.00000E+00
+ CGDOM=1.00000E-09 CGSOM=1.00000E-09   CGBOM=1.91000E-09
+ XPART=1.00000E+00 DUM1=0.00000E+00    DUM2=0.00000E+00
+ N0=2.00000E+02    LN0=0.00000E+00     WN0=0.00000E+00
```

```
+ NB0=0.00000E+00   LNB=0.00000E+00     WNB=0.00000E+00
+ ND0=0.00000E+00   LND=0.00000E+00     WND=0.00000E+00
*p+ diffusion layer
+ RSHM=140.0        CJM=4.0E-004        CJW=2.4E-010
+ IJS=1.00E-008     PJ=0.700E000
+ PJW=0.8000E000    MJ0=0.5             MJW=0.33
+ WDF=0             DS=0
```

Wire Model for Poly and Metal Layers

```
*NOT REFERENCED BY ANY ELEMENTS IN THIS CIRCUIT,
*JUST FOR MODEL EXAMPLES.
*
.MODEL PC_PY1 R
*poly layer
+ RSH=65.0
.MODEL PC_ML1 R
*metal layer 1
+ RSH=0.200
*
.END
```

LEVEL 27 SOSFET Model

A three-terminal silicon-on-sapphire (SOS) FET transistor model is available in the Avant! True-Hspice model.[4.] This SOSFET model is based on a sapphire insulator that isolates the substrate and models the behavior of SOS devices more accurately than standard MOSFET models with physically unreal parameter values. The SOSFET model also includes a charge conservation model (Ward and Dutton model based).

Because the defaults of the SOSFET model parameters are channel-length dependent, you must specify the model parameter SOSLEV to select either the 5 μm or 3 μm processing model.

Setting SOSLEV=1 selects the 5 μm model; otherwise the 3 μm model is automatically set, including the second-order effects (default=3 μm).

Note: There is no bulk node specification for this model. If you specify bulk nodes, simulation ignores them.

This model does not use the model parameter ACM because the model includes no junction diodes. Also, the model parameter CAPOP only accepts a value of 7. Seven is its own charge conservation model, which cannot be used by the other level MOSFET models.

Temperature compensation equations for SOSFET model parameters VTO and UO are the same as those used for the MOSFET model.

Note: The model provides a special option for bulk nodes for silicon on sapphire. In the model definition, when you specify -1 for the bulk node, the model generates a special node for each element. This bulk node is named in the form, B#<element name>, where the element name is that of the defined element. Use this name in any statement, such as a .PRINT statement, to refer to the element's bulk node.

Syntax

```
.MODEL mname PMOS <LEVEL=27> <SOSLEV=val> <pname1=val1>…
```

or

```
.MODEL mname NMOS <LEVEL=27> <SOSLEV=val> <pname=val1>…
```

mname	The model name
PMOS	Identifies a p-channel MOSFET model
NMOS	Identifies an n-channel MOSFET model
LEVEL	Model level selector
SOSLEV	Selects the processing model. If you set SOSLEV=1, the default=5μm. The automatic default=3μm.
pname	Parameter model

LEVEL 27 Model Parameters

5-μm Model Parameters

Name (Alias)	Units	Default	Description
CGDO	F/m		Gate-drain overlap capacitance per unit channel width. The default=3.1e-10 (n-type), 2.2e-10 (p-type).
CGSO	F/m		Gate-source overlap capacitance per unit channel width. The default=3.1e-10 (n-type), 2.2e-10 (p-type).
LD	m		Lateral diffusion. The default=0.6μ (n-type), 0.3μ (p-type).

Name (Alias)	Units	Default	Description
RSH	ohm/ sq		Drain and source diffusion sheet resistance. The default=25 (n ŧype), 100 (p-type).
SOSLEV		1	Model index
TOX	m	7.0e-8	Oxide thickness
UO	cm^2/ (V s)		Surface mobility. The default=350 (n-type), 220 (p-type).
VTO	V		Threshold voltage. The default=1.25 (n-type), -1.25 (p-type).

3-μm Model Parameters

Name (Alias)	Units	Default	Description
A	m/V	0.1μm	Channel length shortening coefficient (2nd effect)
ALPHA	V/m		Threshold voltage length dependence. The default=0.15μ (n-type), 0.18μ (p-type).
CAPOP		7	Capacitance model selector
CGDO	F/m		Gate-drain overlap capacitance per unit channel width. The default=4.6e-10 (n-type), 3.6e-10 (p-type).
CGSO	F/m		Gate-source overlap capacitance per unit channel width. The default=4.6e-10 (n-type), 3.6e-10 (p-type).
EC	V/m		Critical electric field for velocity saturation (2nd effect). The default=3.0e6 (n-type), 7.5e6 (p-type).

Name (Alias)	Units	Default	Description
FB			Body effect coefficient (2nd effect). The default=0.15 (n-type), 0 (p-type).
LD	m		Lateral diffusion. The default=0.3µ (n-type), 0.2µ (p-type).
LEVEL		27	Model level selector
RSH	ohm/sq		Drain and source diffusion sheet resistance. The default=25 (n-type), 80 (p-type).
SOSLEV		2	Model index
THETA	1/V		Mobility degradation coefficient (2nd effect). The default=0.055 (n-type), 0.075 (p-type).
TOX	m	3.4e-8	Oxide thickness
UO	cm^2/(V s)		Surface mobility. The default=370 (n-type), 215 (p-type).
VTO	V		Threshold voltage. The default=0.83 (n-type), -0.74 (p-type).

Example

```
*FILE ML27IV.SP: IDS AND VGS CURVES FOR NMOS AND PMOS SOSFETS
.OPTIONS ACCT LIST NOPAGE NOMOD
.OP
.DC VDDN 0 5.0 .1

* N-CHANNEL IDS CURVES (VD=0->5, VG=1,2,3,4,5)
.PRINT DC I(VN1) I(VN2) I(VN3) I(VN4) I(VN5)
.PLOT DC I(VN1) I(VN2) I(VN3) I(VN4) I(VN5)

* P-CHANNEL IDS CURVES (VD=0->-5,VG=-1,-2,-3,-4,-5)
.PRINT DC I(VP1) I(VP2) I(VP3) I(VP4) I(VP5)
.PLOT DC I(VP1) I(VP2) I(VP3) I(VP4) I(VP5)
```

```
* V G S CURVES
.PRINT DC I(VN6) I(VP6)
.PLOT DC I(VN6) I(VP6)

* N-CHANNEL LX7=GM (VD=5,      VG=0->5,   VS=0)
* N-CHANNEL LX8=GD (VD=0->5,   VG=5,      VS=0)
* N-CHANNEL LX9=GB (VD=5,      VG=5,      VS=0)
.PLOT DC   LX7 (M21)   LX8(M5) LX9(M31)

* P-CHANNEL LX7=GM (VD=0,      VG=0->-5, VS=-5)
* P-CHANNEL LX8=GD (VD=0->-5, VG=-5,    VS=-5)
* P-CHANNEL LX9=GB (VD=0,      VG=0,     VS=-5)
.PLOT DC   LX7(M22) LX8(M15) LX9(M32)
*
VDDN 99 0 5.0
EPD 98 0 99 0 -1

V1 1 0 1
V2 2 0 2
V3 3 0 3
V4 4 0 4
V5 5 0 5
V11 11 0 -1
V12 12 0 -2
V13 13 0 -3
V14 14 0 -4
V15 15 0 -5
*
VN1 99 31 0
VN2 99 32 0
VN3 99 33 0
VN4 99 34 0
VN5 99 35 0

M1 31 1 0 N1 8U 8U
M2 32 2 0 N1 8U 8U
M3 33 3 0 N1 8U 8U
M4 34 4 0 N1 8U 8U
M5 35 5 0 N1 8U 8U
*
VP1 98 41 0
VP2 98 42 0
VP3 98 43 0
VP4 98 44 0
VP5 98 45 0
```

```
M11 41 11 0 P1 8U 8U
M12 42 12 0 P1 8U 8U
M13 43 13 0 P1 8U 8U
M14 44 14 0 P1 8U 8U
M15 45 15 0 P1 8U 8U
*
G M Test
VN6 5 36 0
VP6 0 46 0
M21 36 99 0 N1 8U 8U
M22 46 98 15 P1 8U 8U
*
G M B   Test
VN7 5 37 0
VP7 0 47 0
M31 37 5 0 98 N1 8U 8U
M32 47 0 15 99 P1 8U 8U
*
.MODEL N1 NMOS LEVEL=27 SOSLEV=2
+ VTO=0.814 TOX=0.34E-7 THETA=0.55E-1
+ FB=0.15 EC=0.3E7 A=0.1E-6
+ UO=370 CGSO=0.46E-9 CGDO=0.46E-9
+ RSH=25 LD=0.3E-6
*
.MODEL P1 PMOS LEVEL=27 SOSLEV=2
+ VTO=-0.7212 TOX=0.34E-7 THETA=0.75E-1
+ FB=0.0 EC=0.75E7 A=0.1E-6
+ UO=215 CGSO=0.36E-9 CGDO=0.36E-9
+ RSH=80 LD=0.2E-6
*
.END
```

Non-Fully Depleted SOI Model

When you use Avant! True-Hspice models for SOS/SOI applications, several approaches are currently available. True-Hspice has a 3-terminal SOS model (LEVEL=27) that is stable for circuit design usage, but has some limitations. The model does not have provisions for depleted bulk. Use it only with non-fully depleted applications and where kink effects are not considered.

The following circuit example is a 4-terminal SOI model for incompletely depleted bulk with kink effect. The example uses a sub-circuit to allow a parasitic capacitance to the substrate. In this example, the bulk is considered to be the region under the channel. The substrate is assumed to be the conductive layer under the insulator.

For SOI, the insulator is usually silicon dioxide and the substrate is silicon. For SOS, the insulator is sapphire and the substrate is the metal that contacts the back of the integrated circuit die.

Model Components

The model consists of the following subcomponents:

- Core IDS model: any level works since the impact ionization and weak inversion models are common to all DC levels. The example uses a LEVEL=3 DC MOS model.
- Subthreshold model: the model parameter WIC=3 allows the older models to use the more advanced models found in the BSIM (LEVEL=13, LEVEL=28) models. Model parameter N0 should have a typical value around 1.0.
- Impact ionization model: set the parameters ALPHA and VCR to enable the impact ionization model. Impact ionization is available to all MOS DC equations. Typical values are ALPHA=0.1 and VCR=18.
- Charge conservation gate cap model (CAPOP=9 XQC=.4) keeps the floating bulk node from obtaining extreme values.
- The automatic periphery diode area calculation method (ACM) is set to 3 to allow automatic calculation of the source and drain resistances and diode junction leakage and capacitance. (ACM=3 CJ=0 CJSW=0 CJGATE=4e-10 JS=0 JSW=1e-9 LD=.1u HDIF=1.5u RS=40 RD=40 N=1).

Note: These models assume that the source/drain diffusions extend to the buried oxide; thus, the area part of the diode has no capacitance to bulk. Linear capacitors to the substrate, however, are included in the sub-circuit.

Obtaining Model Parameters

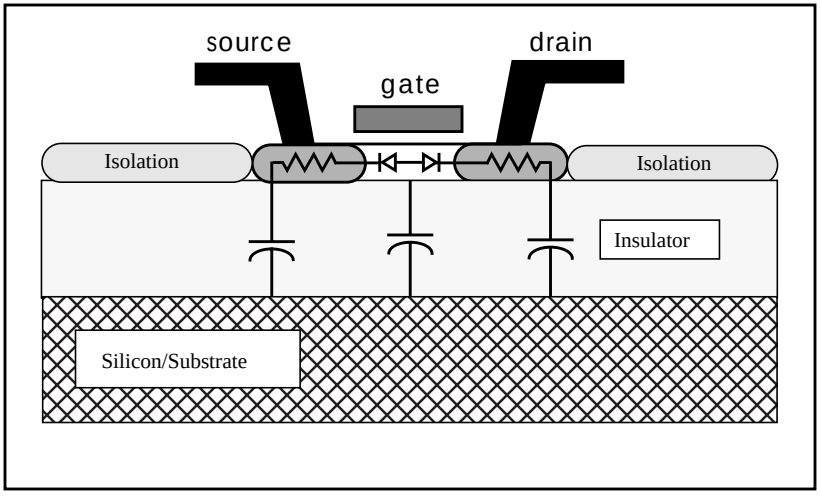
Use the optimizing capabilities in the Avant! True-Hspice models to obtain the core IDS model parameters.

Use the optimizer to get the core model, subthreshold, and impact ionization parameters. The subthreshold model selected is an improved BSIM type of model that was altered for the older models. The impact ionization model is similar to the Intel model.

The charge conservation model is more charge conserving than the original Ward-Dutton model in SPICE 2G6.

The automatic diode area and resistance calculation estimates the junction capacitance, saturation current, and resistance as a function of the transistor width. The parameters VNDS and NDS allow for a piecewise linear approximation to the reverse junction current characteristics.

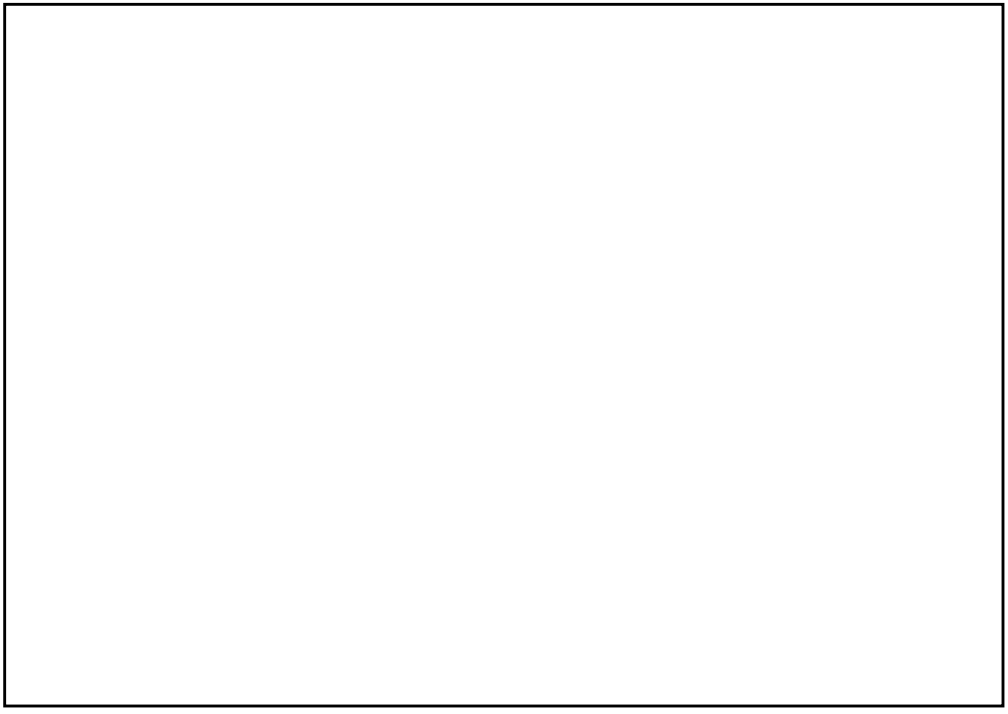
Figure 9-6: Non-fully Depleted SOI Model



Example

```
ssoi.sp LEVEL=3 floating bulk model
** non-fully depleted
* test 1st order soi model with floating substrate
.option nomod post
* substrate capacitance 3.45e-11 is for SiO2
.param t_sub_ox=.5u   subcap='3.45e-11/t_sub_ox' hdif=1.5u
.global substrate
.dc vd 0 5 0.1 sweep vg 1.5 3.5 0.5
.print id=i(xm1.m) vds=v(d) vgs=v(g)
.param vds=0 vgs=0 vbs=0
vd d gnd vds
vg g gnd vgs
vs s gnd 0
vsub substrate gnd vbs
xm1 d g s nch w=50u L=5u
.macro nch d g s w=10u l=2u
* macro definition for fet+ parasitic cap to substrate
* assumes existence of undepleted bulk
   m d g s b nch w=w L=L
   cx d substrate c='w*2*hdif*subcap'
   cx s substrate c='w*2*hdif*subcap'
   cx b substrate c='w*L*subcap'
.eom
.model nch nmos LEVEL=3
+ lmin=.5u lmax=100u wmin=.5u wmax=500u $model selector
+ ld=0.1u wd=.15u xl=0 xw=0        $diffusion+photobias
+ acm=3   hdif=hdif rsh=30 rs=10k rd=10k $resistors
+ ldif=0.1u
$junction cap (ACM=3 (h9007 only) allows diode on gate edge
+ cj=0 cjsw=0 cgate=0.4e-9 mjsw=0.33 php=0.6
+ js=0 jsw=1e-9   n=1 vnds=.5 nds=1        $junction leakage
+    bex=-1.5 tcv=2m                        $temperature
+    tox=200 capop=9 xqc=.4 meto=0.08u   $gate cap
+    alpha=0.1     vcr=18                  $impact ionization
   vto=0.7   phi=1 gamma=1        $threshold
+    eta=10      xj=0.1u            $threshold
+    wic=3 n0=0.9   nd=0            $subthreshold
+    uo=400         theta=1m        $dc mobility
+    vmax=100k   kappa=0            $dc saturation
.end
```

Figure 9-7: LEVEL 3 Floating Bulk Model



Fully Depleted SOI Model Considerations

Fully-depleted transistors require additional modeling equations. The first-order effects are:

- Threshold sensitivity to the substrate
- No kink current
- Depletion capacitance hits a minimum determined by the silicon thickness

Lack of these effects is not a serious problem for an inverter circuit because the source-to-substrate voltage does not move. Digital circuits with good gate drive are not seriously affected because a large gate voltage renders the small Vth shift to a small change in IDS current.

Analog amplifiers with transistors at back-bias and low gate voltages and similar circuits can be affected by the substrate threshold sensitivity.

LEVEL 28 Modified BSIM Model

This section lists the LEVEL 28 parameters and equations for the modified BSIM model.

LEVEL 28 Features

The following are the significant features of the LEVEL 28 model.

- Vertical field dependence of carrier mobility
- Carrier velocity saturation
- Drain-induced barrier lowering
- Depletion charge sharing by source and drain
- Nonuniform doping profile for ion-implanted devices
- Channel length modulation
- Subthreshold conduction
- Geometric dependence of electrical parameters

LEVEL 28 Model Parameters

The LEVEL 28 model parameters follow.

Transistor Process Parameters

Name (Alias)	Units	Default	Description
LEVEL		1	MOSFET model level selector. Set this parameter to 28 for this model.
B1		0.0	Lower vdsat transition point
LB1	μm	0.0	Length sensitivity
WB1	μm	0.0	Width sensitivity
B2		1	Upper vdsat transition point

Name (Alias)	Units	Default	Description
LB2	μm	0.0	Length sensitivity
WB2	μm	0.0	Width sensitivity
CGBO	F/m	2.0e-10	Gate-to-bulk parasitic capacitance (F/m of length)
CGDO	F/m	1.5e-9	Gate-to-drain parasitic capacitance (F/m of width)
CGSO	F/m	1.5e-9	Gate-to-source parasitic capacitance (F/m of width)
ETA0		0.0	Linear vds threshold coefficient
LETA	μm	0.0	Length sensitivity
WETA	μm	0.0	Width sensitivity
ETAMN		0.0	Minimum linear vds threshold coefficient
LETAMN	μm	0.0	Length sensitivity
WETAMN	μm	0.0	Width sensitivity
GAMMN	$V^{1/2}$	0.0	Minimum root-vsb threshold coefficient
LGAMN	$V^{1/2}$·μm	0.0	Length sensitivity
WGAMN	$V^{1/2}$·μm	0.0	Width sensitivity
K1	$V^{1/2}$	0.5	Root-vsb threshold coefficient
LK1	$V^{1/2}$·μm	0.0	Length sensitivity
WK1	$V^{1/2}$·μm	0.0	Width sensitivity
K2		0.0	Linear vsb threshold coefficient
LK2	μm	0.0	Length sensitivity

Name (Alias)	Units	Default	Description
WK2	µm	0.0	Width sensitivity
MUZ	$cm^2/V \cdot s$	600	Low drain field first order mobility
LMUZ	$\mu m \cdot cm^2/V \cdot s$	0.0	Length sensitivity
WMUZ	$\mu m \cdot cm^2/V \cdot s$	0.0	Width sensitivity
N0		200	Low field weak inversion gate drive coefficient (value of 200 for N0 disables weak inversion calculation)
LN0	µm	0.0	Length sensitivity
WN0	µm	0.0	Width sensitivity
NB0		0.0	Vsb reduction to low field weak inversion gate drive coefficient
LNB	µm	0.0	Length sensitivity
WNB	µm	0.0	Width sensitivity
ND0		0.0	Vds reduction to low field weak inversion gate drive coefficient
LND	µm	0.0	Length sensitivity
WND	µm	0.0	Width sensitivity
PHI0	V	0.7	Two times the Fermi potential
LPHI	V·µm	0.0	Length sensitivity
WPHI	V·µm	0.0	Width sensitivity
TOXM (TOX)	µm (m)	0.02	Gate oxide thickness (if TOXM or TOX >1, Angstroms is assumed)

Name (Alias)	Units	Default	Description
U00	1/V	0.0	Gate field mobility reduction factor
LU0	µm/V	0.0	Length sensitivity
WU0	µm/V	0.0	Width sensitivity
U1	1/V	0.0	Drain field mobility reduction factor
LU1	µm/V	0.0	Length sensitivity
WU1	µm/V	0.0	Width sensitivity
VDDM	V	5.0	Critical voltage for high drain field mobility reduction
VFB0 (VFB)	V	-0.3	Flatband voltage
LVFB	V·µm	0.0	Length sensitivity
WVFB	V·µm	0.0	Width sensitivity
WFAC		4	Weak inversion factor
LWFAC	µm	0.0	Length sensitivity
WWFAC	µm	0.0	Width sensitivity
WFACU		0.0	Second weak inversion factor
LWFACU	µm	0.0	Length sensitivity
WWFACU	µm	0.0	Width sensitivity
X2E	1/V	0.0	Vsb correction to linear vds threshold coefficient
LX2E	µm/V	0.0	Length sensitivity
WX2E	µm/V	0.0	Width sensitivity

Name (Alias)	Units	Default	Description
X2M (X2MZ)	$cm^2/V^2 \cdot s$	0.0	Vsb correction to low field first order mobility
LX2M (LX2MZ)	$\mu m \cdot cm^2/V^2 \cdot s$	0.0	Length sensitivity
WX2M (WX2MZ)	$\mu m \cdot cm^2/V^2 \cdot s$	0.0	Width sensitivity
X2U0	$1/V^2$	0.0	Vsb reduction to GATE field mobility reduction factor
LX2U0	$\mu m/V^2$	0.0	Length sensitivity
WX2U0	$\mu m/V^2$	0.0	Width sensitivity
X2U1	$\mu m/V^2$	0.0	Vsb reduction to DRAIN field mobility reduction factor
LX2U1	$\mu m^2/V^2$	0.0	Length sensitivity
WX2U1	$\mu m^2/V^2$	0.0	Width sensitivity
X33M	$cm^2/V^2 \cdot s$	0.0	Gate field reduction of X3MS
LX33M	$\mu m \cdot cm^2/V^2 \cdot s$	0.0	Length sensitivity
WX33M	$\mu m \cdot cm^2/V^2 \cdot s$	0.0	Width sensitivity
X3E	1/V	0.0	Vds correction to linear vds threshold coefficient
LX3E	µm/V	0.0	Length sensitivity
WX3E	µm/V	0.0	Width sensitivity

Name (Alias)	Units	Default	Description
X3MS	$cm^2/V^2 \cdot s$	5.0	Vds correction for high drain field mobility
LX3MS	$\mu m \cdot cm^2/V^2 \cdot s$	0.0	Length sensitivity
WX3MS	$\mu m \cdot cm^2/V^2 \cdot s$	0.0	Width sensitivity
X3U1	$1/V^2$	0.0	Vds reduction to drain field mobility reduction factor
LX3U1	$\mu m/V^2$	0.0	Length sensitivity
WX3U1	$\mu m/V^2$	0.0	Width sensitivity
XPART		1.0	Selector for gate capacitance charge sharing coefficient

Notes:

1. When reading parameter names, be aware of the difference in appearance between the capital letter O, and the number zero 0.
2. All LEVEL 28 parameters should be specified using NMOS conventions, even for PMOS—for example, ETA0 = 0.02, not ETA0 = -0.02.
3. The WL-product sensitivity parameter is available for any parameter with an L and W sensitivity. Replace the leading “L” of the L sensitivity parameter name with a “P”.

Basic Model Parameters

Name (Alias)	Units	Default	Description
LD (DLAT, LATD)	m		Lateral diffusion into channel from source and drain diffusion. ■ If LD and XJ are unspecified LD default=0.0 ■ If LD is unspecified but XJ is specified, LD is calculated from XJ. LD default=0.75 XJ LDscaled = LD · SCALM
LDAC	m		This parameter is the same as LD, but if LDAC is included in the .MODEL statement, it replaces LD in the Leff calculation for AC gate capacitance.
LMLT		1.0	Length shrink factor
LREF	m	0.0	Reference channel length LREFscaled = LREF · SCALM
XLREF	m	0.0	Difference between physical (on wafer) and drawn reference channel length XLREFscaled = XLREF · SCALM
WD	m	0.0	Lateral diffusion into channel from bulk along width WDscaled = WD · SCALM

Name (Alias)	Units	Default	Description
WDAC	m		This parameter is the same as WD, but if WDAC is in the .MODEL statement, it replaces WD in the Weff calculation for AC gate capacitance.
WMLT		1.0	Diffusion layer and width shrink factor
XL (DL, LDEL)	m	0.0	Accounts for masking and etching effects XLscaled = XL · SCALM
XW (DW, WDEL)	m	0.0	Accounts for masking and etching effects XWscaled = XW · SCALM
WREF	m	0.0	Reference channel width WREFscaled = WREF · SCALM
XWREF	m	0.0	Difference between physical (on wafer) and drawn reference channel width XWREFscaled = XWREF · SCALM

Temperature Parameters

Name (Alias)	Units	Default	Description
BEX		-1.5	Temperature exponent for MUZ, X2M, X3MS, X33M mobility parameters
FEX		0.0	Temperature exponent for mobility reduction factor U1
TCV	V/°K	0.0	Flat-band voltage temperature coefficient

Sensitivity Factors of Model Parameters

For transistors, the L (channel length), W (channel width), and WL-product sensitivity factors of a basic electrical parameter are denoted by adding the characters L, W, and P, respectively, at the start of the name, and often dropping any ending “0”. For example, VFB0 sensitivity factors are LVFB, WVFB, and PVFB. If A0 is a basic parameter, LA, WA and PA are the corresponding sensitivity factors of this parameter (note that LA, WA and PA cannot be scaled using the SCALM option). Then the model uses the following general formula to obtain the parameter value.

The left side of the equation represents the effective model parameter value after device size adjustment. All the effective model parameters are in lower case and start with the character z, followed by the parameter name.

$$za = A0 + LA \cdot \left[\frac{1}{Leff} - \frac{1}{LREFeff}\right] + WA \cdot \left[\frac{1}{Weff} - \frac{1}{WREFeff}\right]$$

$$+ PA \cdot \left[\frac{1}{Leff} - \frac{1}{LREFeff}\right] \cdot \left[\frac{1}{Weff} - \frac{1}{WREFeff}\right]$$

LA and WA are specified in units of microns times the units of A0. PA is specified in units of square microns times the units of A0.

If you set LREF or WREF=0, you effectively set the parameter to infinity. This is the default.

Example

$$VFB0 = -0.350v$$

$$LVFB = -0.1v\mu$$

$$WVFB = 0.08v \cdot \mu$$

$$Leff = 1 \cdot 10^{-6}m = 1\mu$$

$$Weff = 2 \cdot 10^{-6}m = 2\mu$$

$$LREFeff = 2 \cdot 10^{-6}m = 2\mu$$

$$WREFeff = 1 \cdot 10^{-5}m = 10\mu$$

$$vfb = VFB0 + LVFB \cdot \left(\frac{1}{Leff} - \frac{1}{LREFeff}\right) + WVFB \cdot \left(\frac{1}{Weff} - \frac{1}{WREFeff}\right)$$

$$zvfb = -0.35v + -0.1v \cdot \mu \cdot \left(\frac{1}{1\mu} - \frac{1}{2\mu}\right) + 0.08v \cdot \mu \cdot \left(\frac{1}{2\mu} - \frac{1}{10\mu}\right)$$

$$zvfb = -0.35v - 0.05v + 0.032v$$

$$zvfb = -0.368v$$

LEVEL 28 Model Equations

The LEVEL 28 model equations follow.

Effective Channel Length and Width

The effective channel length and width for LEVEL 28 is determined to be consistent with the LEVEL 3 model. L, W and the multiplier M are from the .MODEL statement in the netlist. SCALE and SCALM are options. When no scaling options or multipliers are used,

$$Leff = L+XL-2 \cdot LD \quad Weff = W+XW-2 \cdot WD$$

Note: If LDAC and WDAC are included in the .MODEL statement, Leff=L+XL-2·LDAC Weff=W+XW-2·WDAC

Syntax

```
Lscaled = L  SCALE
Wscaled = W  SCALE
XLscaled = XL  SCALM
LDscaled = LD  SCALM
XWscaled = XW  SCALM
WDscaled = WD  SCALM
Leff = Lscaled  LMLT+XLscaled-2  LDscaled
LREFeff = LREFscaled  LMLT+XLREFscaled-2  LDscaled
Weff = M  (Wscaled  WMLT+XWREFscaled-2  WDscaled)
WREFeff = M  (WREFscaled  WMLT+XWscaled-2  WDscaled)
```

Threshold Voltage

Effective model parameter values for threshold voltage after device size adjustment are zphi, zvfb, zk1, zk2, zeta, zx2e, zx3e, zgammn, and zetamn. They are calculated from the model parameters PHI0, VFB0, K1, K2, ETA0, X2E, X3E, GAMMN, ETAMN, and their respective length and width sensitivity parameters.

$$xbs=(zphi-vbs)^{1/2}$$

$$xeta=zeta+zx2e\cdot vbs+zx3e\cdot vds$$

$$vth=zvfb + zphi + zk1\cdot xbs - zk2\cdot xbs^{2}-xeta\cdot vds$$

This equation is quadratic in xbs and vds. It is joined to linear equations at d(vth)/d(xbs) = zgammn and at d(vth)/d(vds) = -zetamn, which prevents the quadratics from going in the wrong direction.

Both gammn and etamn default to zero and typically do not affect behavior in the normal operating region.

Effective Mobility

The effective model parameter values for mobility after device size adjustment are zmuz, zx2m, zx3m, zx33m, zu0, and zx2u0. They are calculated from the model parameters MUZ, X2M, X3m, X33M, U00, X2U0, and their respective length and width sensitivity parameters.

$$v_{gst} = v_{gs} - v_{th}$$

$$cx3ms = \frac{zx3ms}{(muz + zx33m \cdot v_{gst})}$$

$$m_{eff} = (zmuz + zx2m \cdot v_{bs})$$

$$\cdot (1 + cx3ms \cdot (VDDM + v_{ds} - (VDDM \cdot VDDM + v_{ds} \cdot v_{ds})^{1/2}))$$

$$xu0 = zu0 + zx2u0 \cdot v_{bs}$$

$$u_{eff} = \frac{m_{eff}}{(1 + xu0 \cdot v_{gst})}$$

$$beta = u_{eff} \cdot COX \cdot \frac{W_{eff}}{L_{eff}}$$

Saturation Voltage (vdsat)

The effective model parameter values for saturation voltage, after device size adjustment, are zu1, zx2u1, and zx3u1. They are calculated from the U1, X2U1, X3U1 model parameters, and their length and width sensitivity parameters.

$$xbs = (zphi - v_{bs})^{1/2}$$

$$g = 1 - \frac{1}{(1.744 + 0.8364 \cdot xbs^2)}$$

$$body = \frac{1 + g \cdot zk1}{(2 \cdot xbs)}$$

$$xu1 = zu1 + vbs \cdot zx2u1$$

$$rx = (body^2 + zu1 \cdot 2 \cdot body \cdot v_{gst} + zx3u1 \cdot 4 \cdot v_{gst}^2)^{1/2}$$

$$v_{dsat} = \frac{2 \cdot v_{gst}}{(body + rx)}$$

This is the value of vds that makes the partial derivative of

$$f(v_{ds}, v_{gst}, v_{bs}) = (v_{gst} - body/2 \cdot v_{ds}) \cdot \frac{v_{ds}}{(1 + (xu1 + zx3u1 \cdot v_{ds}) \cdot v_{ds})}$$

with respect to vds equal to zero.

Transition Points

The effective model parameter values for transition points after device size adjustment are zb1 and zb2. They are calculated from the model parameters B1, B2, and their respective length and width sensitivity parameters.

$$v1 = v_{dsat} - zb1 \cdot \frac{v_{dsat}}{1 + v_{dsat}}$$

$$v2 = v_{dsat} + zb2 \cdot v_{gst}$$

Strong Inversion Current

For vds < v1,

$$I_{ds} = beta \cdot (v_{gst} - body/2 \cdot v_{ds}) \cdot \frac{v_{ds}}{(1 + (zu1 + zx3u1 \cdot v_{ds}) \cdot v_{ds})}$$

The vds derivative varies approximately linearly between v1 and v2.

For vds>v2, ids is a function of beta and vgst only. If zb1 and zb2 are both positive, their main effect is to increase the current in saturation.

Weak Inversion Current

The effective model parameter values for weak inversion current after device size adjustment are zn0, znb, znd, zwfac and zwfacu. They are calculated from the model parameters N0, ND0, NB0, WFAC, WFACU, and their respective length and width sensitivity parameters.

The weak inversion current is calculated when zn0 is less than 200. It is added to the strong inversion current,

$$Itotal = Istrong + Iweak \cdot \left(1 - \exp\left(\frac{-v_{ds}}{vtherm}\right)\right)$$

In deep subthreshold,

$$xn = zn0 + znb \cdot v_{bs} + znd \cdot v_{ds}$$

$$vtherm = \frac{KT}{Q}$$

$$xweak = \frac{(v_{gs} - vt)}{(xn \cdot vtherm)}$$

$$Iweak = const \cdot \exp(xweak)$$

The modification of this formula near threshold is controlled by zwfac and zwfacu. Just above threshold, the device is in saturation:

$$\text{Istrong} = \text{const} \cdot \text{xweak}^2$$

so Iweak needs an xweak^2 term to cancel the kink in gm at threshold. Then Iweak goes to zero for xweak>A0, which is at a small voltage above threshold. Iweak has four regions:

(1) xweak < -zwfac+A0

$$\text{Iweak} = \text{const} \cdot \exp(\text{xweak})$$

(2) -zwfac+A0 < xweak < 0

$$\text{Iweak} = \text{const} \cdot \exp(\text{xweak} - \text{const} \cdot \text{wf})$$

where wf is the integral with respect to xweak of

$$\text{dwf} = \frac{(\text{xweak} + \text{zwfac} - \text{A0})^2}{[(1 + \text{xweak} + \text{zwfac} - \text{A0})(1 + \text{zwfacu} \cdot (\text{xweak} + \text{zwfac} - \text{A0}))]}$$

(3) 0 < xweak < A0

$$\text{Iweak} = (\textit{same formula as in region 2}) - \text{const} \cdot \text{xweak}^2$$

(4) A0 < xweak

$$\text{Iweak} = 0$$

A0 and the constants in the formulas above are not model parameters, but are uniquely determined by continuity conditions at the boundaries between regions.

LEVEL 38 IDS: Cypress Depletion Model

The LEVEL 38 Cypress Depletion MOSFET model (Cypress Semiconductor Corporation) is a further development of the Avant! True-Hspice LEVEL 5 model and features:

- BSIM-style length and width sensitivities
- Degraded body effect at high substrate bias (second GAMMA)
- Empirical fitting parameters for Ids current calculations in the depletion mode of operations
- A comprehensive surface mobility equation
- Drain-induced barrier lowering

At the default parameter settings, the LEVEL 38 model is basically backwards-compatible with LEVEL 5 /ZENH=0.0, with the exception of the surface mobility degradation equation (see the discussion below). Refer to the documentation for LEVEL 5 for the underlying physics that forms the foundation for the Huang-Taylor construct.

In LEVEL 38, the temperature compensation for threshold is ASPEC-style, concurring with the default in LEVEL 5. This section introduces and documents model parameters unique to this depletion model and additional temperature compensation parameters.

LEVEL 38 allows the use of all Avant! True-Hspice model capacitance options (CAPOP). CAPOP=2 is the default setting for LEVEL 38. By setting CAPOP=6 (AMI capacitance model), LEVEL 38 capacitance calculations become identical to those of LEVEL 5.

The parameter ACM default (ACM=0 in LEVEL 38) invokes SPICE-style parasitics. ACM also can be set to 1 (ASPEC), or to 2 (Avant! True-Hspice). All MOSFET models follow this convention.

You can use the SCALE option with the True-Hspice LEVEL 5 model. However, you cannot use the SCALM option, due to the difference in units. You also cannot use the DERIV option.

The following parameters *must* be specified for MOS LEVEL 38: VTO (VT), TOX, UO (UB), FRC, ECV, and NSUB (DNB).

As with LEVEL 5, the Ids current is calculated according to three gate voltage regions:

Depletion Region, vgs - vfb < 0

The low gate voltage region dominated by the bulk channel.

Enhancement Region, vgs - vfb > 0, vds < vgs - vfb

The region defined by high gate voltage and low drain voltage. In the enhancement region, both channels are fully turned on.

Partial enhancement region, vgs - vfb > 0, vds > vgs - vfb

The region with high gate and drain voltages, resulting in the surface region being partially turned on and the bulk region being fully turned on.

To better model depletion region operations, empirical fitting constants have been added to the original Huang-Taylor mechanism to account for the effects caused by nonuniform channel implants and also to make up for an oversight in the average capacitance construct[5]. For the enhancement region, a significantly more elaborate surface mobility model is used.

Body effect in LEVEL 38 is calculated in two regions[6]:

Bulk body effect, vsb-vsbc > 0

With sufficiently high (and negative) substrate bias (exceeding vsbc), the depletion region at the implanted channel-substrate junction reaches the Si-oxide interface. Under such circumstances, the free carriers can only accumulate at the interface (like in an enhancement device) and the body effect is determined by the bulk doping level.

Implant-dominated body effect, vsb-vsbc < 0

Before reaching vsbc, and as long as the implant dose overwhelms the substrate doping level, the body effect of the depletion mode device is dominated by the deeply “buried” transistor due to the implant. The body effect coefficient $\bar{\gamma}$ is proportional to both the substrate doping and, to first order, the implant depth.

In this model level, the “amplification” of the body effect due to deep implant is accounted for by an empirical parameter, BetaGam.

Model parameters that start with L or W represent geometric sensitivities. In the model equations, a quantity denoted by zX (X being the variable name) is determined by three model parameters: the large-and-wide channel case value X and length and width sensitivities LX and WX, according to zX=X+LX/Leff+WX/Weff. For example, the zero field surface mobility is given by

$$zUO = UO + \frac{LUO}{leff} + \frac{WUO}{weff}$$

Note: This model uses mostly micrometer units rather than the typical meter units. Units and defaults are often unique in LEVEL 38. The I_{ds} derivatives that give small signal gains gm, gds, and gmbs are calculated using the finite difference method. The options SCALM and DERIV are ineffective for this model.

LEVEL 38 Model Parameters

The LEVEL 38 model parameters follow.

Basic Model Parameters

Name (Alias)	Units	Default	Description
LEVEL		1.0	Model level selector. This parameter is set to 38 for this model.
DNB (NSUB)	cm^{-3}	0.0	Surface doping density.
DP	μm	1.0	Implant depth
ECV	V/μm	1000	Critical field

Name (Alias)	Units	Default	Description
KCS		2.77	Implant capacitance integration constant
NI	cm^{-2}	2e11	Implant doping
PHI	V	0.8	Built-in potential
TOX	Å	0.0	Oxide thickness

Effective Width and Length Parameters

Name (Alias)	Units	Default	Description
DEL (WDEL)	m	0.0	Channel length reduction on each side
LATD (LD)	m	1.7 · XJ	Lateral diffusion on each side
LDAC	m		This parameter is the same as LD, but if LDAC is included in the .MODEL statement, it replaces LD in the Leff calculation for AC gate capacitance.
LMLT		1.0	Length shrink factor
OXETCH	µm	0.0	Oxide etch
WMLT		1.0	Diffusion layer and width shrink factor

Threshold Voltage Parameters

Name (Alias)	Units	Default	Description
FSS (NFS)	$cm^{-2}.V^{-1}$	0.0	Number of fast surface states
NWM		0.0	Narrow width modifier

Name (Alias)	Units	Default	Description
SCM		0.0	Short-channel drain source voltage multiplier
BetaGam		1.0	Body effect transition ratio
LBetaGam	µm	0.0	BetaGam dependence on channel length
WBetaGam	µm	0.0	BetaGam dependence on channel width
DVSBC	V	0.0	Empirical body effect transition voltage adjustment
LDVSBC	V·µm	0.0	L-dependent body effect transition voltage adjustment
WDVSBC	V·µm	0.0	W-dependent body effect transition voltage adjustment
TDVSBC	V/K	0.0	Body effect transition voltage shift due to temperature
VT (VTO)	V	0.0	Extrapolated threshold voltage
LVT (LVTO)	V·µm	0.0	VT dependence on channel length
WVT (WVTO)	V·µm	0.0	VT dependence on channel width
ETA		0.0	Channel-length independent drain-induced barrier lowering
LETA(DIBL)	µm	0.0	Channel-length dependent drain-induced barrier lowering
WETA	µm	0.0	Channel-width dependent drain-induced barrier lowering
DVIN	V	0.0	Empirical surface inversion voltage adjustment
XJ	µm	1.5	Junction depth

Mobility Parameters

Name (Alias)	Units	Default	Description
FRC	Å·s/ cm^2	0.0	Field reduction coefficient
LFRC	10^{-4}Å·s/ cm	0.0	FRC sensitivity to effective channel length
WFRC	10^{-4}Å·s/ cm	0.0	FRC sensitivity to effective channel width
VFRC	Å·s/ (cm^2·V)	0.0	Field reduction coefficient variation due to drain bias
LVFRC	10^{-4}Å·s/ (cm·V)	0.0	VFRC sensitivity to effective channel length
WVFRC	10^{-4}Å·s/ (cm·V)	0.0	VFRC sensitivity to effective channel width
BFRC	Å·s/ (cm^2·V)	0.0	Field reduction coefficient variation due to substrate bias.
LBFRC	10^{-4}Å·s/ (cm·V)	0.0	BFRC sensitivity to effective channel length
WBFRC	10^{-4}Å·s/ (cm·V)	0.0	BFRC sensitivity to effective channel width

Name (Alias)	Units	Default	Description
FSB	$V^{1/2}\cdot s/cm^2$	0.0	Substrate bias-induced mobility degradation coefficient
LFSB	$10^{-4}V^{1/2}\cdot s/cm$	0.0	FSB sensitivity to effective channel length
WFSB	$10^{-4}V^{1/2}\cdot s/cm$	0.0	FSB sensitivity to effective channel width
UO (UB)	$cm^2/(V\cdot s)$	600	Low field bulk mobility
LUO(LUB)	$cm^2\cdot \mu m/(V\cdot s)$	0.0	UO sensitivity to effective channel length
WUO(WUB)	$cm^2\cdot \mu m/(V\cdot s)$	0.0	UO sensitivity to effective channel width
FRCEX(F1EX)		0.0	Temperature coefficient for *FRC*
UH	$cm^2/(V\cdot s)$	900	Implant-channel mobility
KBeta1		1.0	Effective implant-channel mobility modifier
LKBeta1	µm	0.0	Length-dependent implant-channel mobility modifier
WKBeta1	µm	0.0	Width-dependent implant-channel mobility modifier
KI0(KIO)		1.0	Residue current coefficient
LKI0(LKIO)	µm	0.0	Length-dependent residue current coefficient

Name (Alias)	Units	Default	Description
WKI0(WKIO)	μm	0.0	Width-dependent residue current coefficient
HEX(TUH)		-1.5	Implant channel mobility temperature exponent
BEX		-1.5	Surface channel mobility temperature exponent
VST	cm/s	0.0	Saturation velocity
UHSAT	μm/V	0.0	Implant-channel mobility saturation factor

Capacitance Parameters

Name (Alias)	Units	Default	Description
AFC		1.0	Area factor for MOSFET capacitance
CAPOP		6	Gate capacitance selector
METO	μm	0.0	Metal overlap on gate

LEVEL 38 Model Equations

The LEVEL 38 model equations follow.

IDS Equations

Depletion, vgs-vfb <0

$$ids = \beta 1 \cdot \left\{ q \,.\, zKI0 \cdot NI \cdot vde + cav \cdot \left[(vgs - vfb) \cdot vde - \frac{vde^2}{2} \right] \right.$$

$$\left. -\frac{2}{3} \cdot cav \cdot \bar{\gamma} \cdot [(vde + vsb + Phid)^{3/2} - (vsb + Phid)^{3/2}] + Icrit \right\}$$

Enhancement, vgs-vfb vde >0

$$ids = \beta 1 \cdot \left\{ q \cdot zKI0 \cdot NI \cdot vde - \frac{2}{3} \cdot cav \cdot \bar{\gamma} \cdot [(vde + vsb + Phid)^{3/2} - (vsb + Phid)^{3/2}] + Icrit \right\}$$

$$+ \beta \cdot \left[(vgs - vfb) \cdot vde - \frac{vde^2}{2} \right]$$

Partial Enhancement, vgs-vfb<vde

$$ids = \beta 1 \cdot \left\{ q \cdot zKI0 \cdot NI \cdot vde + cav \cdot \left[(vgs - vfb) \cdot vde - \frac{vde^2}{2} \right] \right.$$

$$\left. - \frac{2}{3} \cdot cav \cdot \bar{\gamma} \cdot [(vde + vsb + Phid)^{3/2} - (vsb + Phid)^{3/2}] + Icrit \right\}$$

$$+ \left(\frac{1}{2}\beta - \frac{1}{2}\beta 1 \cdot cav \right) \cdot (vgs - vfb)^2$$

where:

$$\beta 1 = \frac{zKBeta1}{1 + UHSAT \cdot \frac{vde}{Leff}} \cdot UH \cdot \frac{Weff}{Leff}$$

$$\beta = UBeff \cdot cox \cdot \frac{Weff}{Leff}$$

$$cav = \frac{cox \cdot cs}{cox + cs}$$

$$cs = \frac{KCS \cdot \varepsilon_{Si}}{DP \cdot 1e\text{-}4}$$

$$Phid = vt \cdot \ln\left(\frac{DNB \cdot nd}{ni^2} \right)$$

$$nd = \frac{NI \cdot 1e4}{DP}$$

and:

$$vde = \min(vds, vdsat)$$

The temperature dependence of the mobility terms assume the ordinary exponential form:

$$UH(t) = UH(tnom) \cdot \left(\frac{t}{tnom}\right)^{TUH}$$

$$zUO(t) = zUO(tnom) \cdot \left(\frac{t}{tnom}\right)^{TUH}$$

The continuity term at the body effect transition point is given by

$$Icrit = -\frac{2}{3} \cdot cav \cdot [(vde + vsbc + Phid)^{3/2} - (vsbc + Phid)^{3/2}] \cdot \gamma \cdot \left(\frac{1}{zBetaGam} - 1\right)$$

for vsb>vsbc; $Icrit = 0$ otherwise.

The saturation voltage, threshold voltage, body effect transition voltage, and body effect coefficient $\bar{\gamma}$ are described in the following sections.

Threshold Voltage, vth

The model parameter VTO, often called the “pinch-off,” is a zero-bias threshold voltage extrapolated from a large device operating in the depletion mode. The effective pinch-off threshold voltage, including the device size effects and the terminal voltages, is given by:

$$vth = vfb - \beta d \cdot [vch - \bar{\gamma} \cdot (Phid + vsb)^{1/2} + vcrit]$$

where:

$$vfb = zVTO - zETA \cdot vds + \beta d \cdot (vch - \gamma_0 \cdot Phid^{1/2})$$

$$vcrit = \left(\gamma - \frac{\gamma}{zBetaGam}\right) \cdot (Phid + vsbc)^{1/2} \text{ for vsb > vsbc; 0 otherwise.}$$

$$\beta d = \frac{UH \cdot cav}{zUO \cdot cox}$$

$$vch = \frac{q \cdot NI}{cav}$$

$$\gamma_0 = \frac{(2 \cdot \varepsilon si \cdot q \cdot na1)^{1/2}}{cav}$$

$$na1 = \frac{nd \cdot DNB}{nd + DNB}$$

$$nd = \frac{NI}{DP \cdot 1e\text{-}4}$$

The effective $\bar{\gamma}$, including small device size effects, is computed as follows:

$$\bar{\gamma} = \frac{\gamma}{zBetaGam} \text{ for vsb>vsbc, and } =g \text{ otherwise.}$$

$$\gamma = \gamma_0 \cdot (1 - scf) \cdot (1 + ncf)$$

where:

If SCM ≤0,

$$scf = 0$$

otherwise,

$$scf = \frac{XJ}{Leff} \cdot \left\{ \left[1 + \frac{2xd}{XJ} \cdot (SCM \cdot vds + vsb + Phid)^{1/2} \right]^{1/2} - 1 \right\}$$

If NWM ≤0,

$$ncf = 0$$

otherwise,

$$ncf = \frac{NWM \cdot xd \cdot (Phid)^{1/2}}{Weff}$$

where:

$$xd = \left(\frac{2 \cdot \varepsilon si}{q \cdot DNB}\right)^{1/2}$$

The body effect transition point is calculated as follows:

$$Vsbc = \frac{qDP^2}{2\varepsilon si}\left(\frac{NI}{DP \cdot 1e-4} - DNB\right) + zDVSBC + TDVSBC \cdot (t - tnom) - Phid$$

When vgs ≤ vth, the surface is inverted and a residual DC current exists. When vsb is large enough to make vth > vinth, then vth is used as the inversion threshold voltage.

In order to determine the residual current, vinth is inserted into the ids, vsat, and mobility equation in place of vgs (except for vgs in the exponential term of the subthreshold current). The inversion threshold voltage at a given vsb is vinth, which is computed as:

$$vinth = vfb - \frac{q \cdot NI}{cox} - vsb + DVIN - zETA \cdot vds$$

Saturation Voltage, vdsat

The saturation voltage vsat is determined by:

$$vsat = vgs - vfb + vch + \frac{\gamma^2}{2} \cdot \left\{1 - \left[1 + \frac{4}{\gamma^2} \cdot (vgs - vfb + vch + vsb + Phid)\right]^{1/2}\right\}$$

$$vdsat = vsat$$

Simulation modifies vsat to include the carrier velocity saturation effect:

$$vdsat = vsat + vc - (vsat^2 + vc^2)^{1/2}$$

where:

$$vc = ECV \cdot Leff$$

Mobility Reduction, UBeff

The surface mobility UB is dependent upon terminal voltages as follows:

$$JBeff = \frac{1}{\frac{1}{zUO} + \frac{(zFRC + zVFRC \cdot vde + zBFRC \cdot vsb) \cdot (vgs - vfb)}{TOX} + \frac{vde}{VST \cdot Le} + zFSB \cdot vsb^{1/2}}$$

where:

$$Le = Leff \quad \textit{Linear region}$$

$$Le = Leff - \Delta L \quad \textit{Saturation region}$$

and at elevated temperatures

$$zFRC(t) = zFRC(tnom) \cdot \left(\frac{t}{tnom}\right)^{FRCEX}$$

The ΔL is the channel length modulation effect, defined in the next section. Note that v_{fb} assumes the role of v_{th} in the LEVEL 5 mobility equation. The degradation parameters are semi-empirical and grouped together according to their (linearized) mathematical dependencies instead of physical origin to better provide parameter extraction.[7.]

Channel Length Modulation

The channel length modulation effect is included by modifying the ids current as follows:

$$ids = \frac{ids}{1 - \frac{\Delta L}{Leff}}$$

where:

$$\Delta L = 1e4 \cdot \left[\frac{2.73e3 \cdot XJ}{na1 \cdot \ln\left(\frac{1e20}{na1}\right)}\right]^{1/3} \cdot [(vds - vdsat + PHI)^{1/3} - PHI^{1/3}]$$

The ΔL is in microns, assuming XJ is in microns and na1 is in cm^{-3}.

Subthreshold Current, ids

When device leakage currents become important for operation near or below the normal threshold voltage, the model considers the subthreshold characteristics. In the presence of surface states, the effective threshold voltage von is determined by:

$$von = \max(vth,vinth) + fast$$

where:

$$fast = vt \cdot \left[1 + \frac{q \cdot FSS}{cox} + \frac{\gamma}{2 \cdot (Phid + vsb)^{1/2}}\right]$$

If vgs <von, then

Partial Enhancement, 0< vgs-vfb < vde

$$ids = \beta 1 \cdot \left\{q \cdot zKI0 \cdot NI \cdot vde + cav \cdot \left[(von - vfb) \cdot vde - \frac{vde^2}{2}\right]\right.$$

$$\left. -\frac{2}{3} \cdot cav \cdot \bar{\gamma} \cdot [(vde + vsb + Phid)^{3/2} - (vsb + Phid)^{3/2}] + Icrit\right\}$$

$$+ \frac{1}{2} \cdot \left(\beta \cdot e^{\frac{vgs - von}{fast}} - \beta 1 \cdot cav\right) \cdot (von - vfb)^2$$

Full Enhancement, vgs-vfb -vde > 0

$$ids = \beta 1 \cdot \left\{ q \cdot zKI0 \cdot NI \cdot vde - \frac{2}{3} \cdot cav \cdot \bar{\gamma} \cdot [(vde + vsb + Phid)^{3/2} - (vsb + Phid)^{3/2}] + Icrit \right\}$$

$$+ \beta \cdot \left[(von - vfb) \cdot vde - \frac{vde^2}{2} \right] \cdot e^{\frac{vgs - von}{fast}}$$

Depletion, vgs-vfb < 0

$$ids = \beta 1 \cdot \left\{ q \cdot zKI0 \cdot NI \cdot vde + cav \cdot \left[(vgs - vfb) \cdot vde - \frac{vde^2}{2} \right] \right.$$

$$\left. - \frac{2}{3} \cdot cav \cdot \bar{\gamma} \cdot [(vde + vsb + Phid)^{3/2} - (vsb + Phid)^{3/2}] + Icrit \right\} \cdot e^{\frac{vgs - von}{fast}}$$

Example Model File

```
$ file Depstor.mod
.MODEL DEPSTOR NMOS LEVEL=38
* PARASITIC ELEMENTS
+ ACM=1
+ LD=0.15u WD=0.2u $ for LEFF AND WEFF
+ CJ=0.3E-16 MJ=0.4 PB=0.8 JS=2.0E-17 $ INTRINSIC DIODE
+ CJSW=0 MJSW=0.3
+ BULK=98 $ DEFAULT NODE FOR SUBSTRATE
* THRESHOLD
+ VTO=-2.5 LVT=-0.25 WVT=0
+ leta=0.02 eta=0.0 weta=0.0
+ TCV=0.003    $ TEMPERATURE COEFFICIENT
*           MISC
+ DVIN=0.5 PHI=0.75
+ NFS=2e10     DNB=3.0E16
```

Mobility Model

```
+ UH= 1300
+ UO=495   FRC= 0.020 FSB=5e-5    VFRC=-1e-4    BFRC=-0
+ LUO=-100 LFRC=.03   LFSB=-1e-5  LVFRC=-.002   LBFRC=-1e-3
+ WUO=-30 WFRC=-0.01 WFSB=5e-5  WVFRC=-0.00  + WBFRC=-0.4e-3
+ KI0=.9    KBETA1=.5   LKI0=0.16         LKBETA1=-0.15
+ WKI0=0.0     WKBETA1=-0.0
+ BEX=-1.3 TUH=-1.0 Frcex=1.0
```

Body Effect

```
+ NWM=0.5      SCM=.1
+ DVSBC=0.1    LDVSBC=0 WDVSBC=0
+ TDVSBC=.002
+ BetaGam=0.9  LBetaGam=-.2 WBetaGam=.1
```

Saturation

```
+ ECV=      2.9 VST=8000      UHSAT=0
* CHANNEL LENGTH MODULATION
+ XJ= 0.1
* OXIDE THICKNESS AND CAPACITANCE
+ TOX=165 CGSO=0 CAPOP=2
*  CHANNEL IMPLANT
+ NI=1.5e12       KCS=3 DP=0.25
*.END
```

LEVEL 39 BSIM2 Model

The BSIM2 (Berkeley Short-Channel IGFET Model 2)[8.] [9.] is available in the Avant! True-Hspice model as LEVEL 39. The Avant! implementation of this model is based on Berkeley SPICE 3E2.

Provide input to the model by assigning model parameters, as for other True-Hspice models. Tabular model entry without model parameter names (as used for BSIM1) is *not* allowed for BSIM2.

LEVEL 39 Model Parameters

The following is a list of the BSIM2 parameters, their units, their defaults (if any) in the Avant! True-Hspice model, and their descriptions. The table lists 47 BSIM2-specific parameters. Considering that three of the parameters (TEMP, DELL, DFW) are not used in the Avant! True-Hspice model and, considering the width and length sensitivity parameters associated with all the remaining parameters except the first six (TOX, VDD, VGG, VBB, DL, DW), the total parameter count is 120. (Unlike Berkeley SPICE, True-Hspice has L and W sensitivity for MU0). This count does not include the “generic” MOS parameters listed in a later table or the WL-product sensitivity parameters, which are Avant! enhancements.

BSIM2 Model Parameters

Name (Alias)	Units	Default	Description
TOX	m	0.02	Gate oxide thickness. (TOX > 1 is assumed to be in Angstroms)
TEMP	C	-	NOT USED IN the Avant! True-Hspice model (see the compatibility notes)
VDD	V	5	Drain supply voltage (NMOS convention)
VGG	V	5	Gate supply voltage (NMOS convention)

Name (Alias)	Units	Default	Description
VBB	V	-5	Body supply voltage (NMOS convention)
DL	m	0	Channel length reduction
DW	m	0	Channel width reduction
VGHIGH	V	0	Upper bound of the weak-strong inversion transition region
VGLOW	V	0	Lower bound of same
VFB	V	-0.3	Flat band voltage
PHI	V	0.8	Surface potential
K1	V^{-1}	0.5	Body effect coefficient
K2	-	0	Second order body effect coefficient (for nonuniform channel doping)
ETA0	-	0	Drain-induced barrier lowering coefficient.
ETAB	V^{-1}	0	Sensitivity of drain-induced barrier lowering coefficient to V_{bs}
MU0	$cm^2/V{\cdot}s$	400	Low-field mobility
MU0B	$cm^2/V^2{\cdot}s$	0	Sensitivity of low-field mobility to V_{bs}
MUS0	$cm^2/V{\cdot}s$	600	High drain field mobility
MUSB	$cm^2/V^2{\cdot}s$	0	Sensitivity of high drain field mobility to V_{bs}
MU20	-	0	Empirical parameter for output resistance

Name (Alias)	Units	Default	Description
MU2B	V^{-1}	0	Sensitivity of empirical parameter to V_{bs}
MU2G	V^{-1}	0	Sensitivity of empirical parameter to V_{gs}
MU30	$cm^2/V^2 \cdot s$	0	Empirical parameter for output resistance
MU3B	$cm^2/V^3 \cdot s$	0	Sensitivity of empirical parameter to V_{bs}
MU3G	$cm^2/V^3 \cdot s$	0	Sensitivity of empirical parameter to V_{gs}
MU40	$cm^2/V^3 \cdot s$	0	Empirical parameter for output resistance
MU4B	$cm^2/V^4 \cdot s$	0	Sensitivity of empirical parameter to V_{bs}
MU4G	$cm^2/V^4 \cdot s$	0	Sensitivity of empirical parameter to V_{gs}
UA0	V^{-1}	0	First-order vertical-field mobility reduction factor
UAB	V^{-2}	0	Sensitivity of first-order factor to V_{bs}
UB0	V^{-2}	0	Second-order vertical-field mobility reduction factor
UBB	V^{-3}	0	Sensitivity of second-order factor to V_{bs}
U10	V^{-1}	0	High drain field (velocity saturation) mobility reduction factor
U1B	V^{-2}	0	Sensitivity of mobility reduction factor to V_{bs}

Name (Alias)	Units	Default	Description
U1D	V^{-2}	0	Sensitivity of mobility reduction factor to V_{ds}
N0	-	0.5	Subthreshold swing coefficient
NB	$V^{1/2}$	0	Sensitivity of subthreshold swing to V_{bs}
ND	V^{-1}	0	Sensitivity of subthreshold swing to V_{ds}
VOF0	-	0	Threshold offset (normalized to NKT/q) for subthreshold.
VOFB	V^{-1}	0	Sensitivity of offset to V_{bs}.
VOFD	V^{-1}	0	Sensitivity of offset to V_{ds}.
AI0	-	0	Impact ionization coefficient.
AIB	V^{-1}	0	Sensitivity of impact ionization coefficient to V_{bs}.
BI0	V	0	Impact ionization exponent.
BIB	-	0	Sensitivity of impact ionization exponent to V_{bs}.
DELL	m	-	Length reduction of source drain diffusion. NOT USED IN the Avant! True-Hspice model.
WDF	m	-	Default width. NOT USED IN the Avant! True-Hspice model. Use ".OPTION DEFW=#" in the netlist instead.

All BSIM2 parameters should be specified according to NMOS convention, even for a PMOS model. Examples: VDD=5, not -5, and VBB=-5, not 5, and ETA0=0.02, not -0.02.

Also see the notes following the last table in this section.

Other SPICE Parameters

The following generic SPICE MOS parameters are used with BSIM2 in Berkeley SPICE 3. All are also Avant! True-Hspice model parameters that you can use with the True-Hspice BSIM2 model. See ‘Gate Capacitance Modeling” on page 9-222 and ‘Selecting MOSFET Model LEVELs” on page 8-4 for more information.

Generic SPICE MOS Parameters

Name (Alias)	Units	Default	Description
CGDO	F/m	-	Gate-drain overlap capacitance. Calculated if not specified and if LD or METO, and TOX are.
CGSO	F/m	-	Gate-source overlap capacitance. This parameter is calculated if not specified and if LD or METO, and TOX are.
CGBO	F/m	-	Gate-bulk overlap capacitance. This parameter is calculated if not specified and if WD and TOX are.
RSH	ohm/sq	0	Source/drain sheet resistance.
JS	A/m^2	0	Source/drain bulk diode reverse saturation current density.
PB	V	0.8	Source/drain bulk junction potential.
PBSW	V	PB	Sidewall junction potential
CJ	F/m^2	0	Source/drain bulk zero-bias junction capacitance
CJSW	F/m	0	Sidewall junction capacitance
MJ	-	0.5	Source/drain bulk junction grading coefficient
MJSW		0.33	Sidewall junction grading coefficient

Additionally, source/drain bulk diode sidewall reverse saturation current density, JSW[A/m], is available in the Avant! True-Hspice model.

Other True-Hspice Model Parameters Affecting BSIM2

The following Avant! True-Hspice MOS model parameters are needed to use some True-Hspice enhancements, such as LDD-compatible parasitics, model parameter geometry adjustment relative to a reference device, impact ionization modeling with bulk-source current partitioning, and element temperature adjustment of key model parameters.

This is a partial list. For complete information, see the following:

- Calculating Effective Length and Width for AC Gate Capacitance on page 8-101
- Using Drain and Source Resistance Model Parameters on page 8-30
- Using Impact Ionization Model Parameters on page 8-55
- Temperature Parameters on page 8-105

See .MODEL VERSION Changes to BSIM2 Models on page 9-192 for information about how the .MODEL statement VERSION parameter changes the BSIM2 model depending on the model version number.

True-Hspice Model Parameters

Name (Alias)	Units	Default	Description
ACM	-	0	MOS S/D parasitics selector. ACM=0 is SPICE style. Use ACM=2 or 3 for LDD.
SPICE3	-	0	SPICE3 model compatibility selector. For accurate SPICE3 BSIM2, set SPICE3=1.
DERIV	-	0	Derivative selector: DERIV=0 ⇒ analytic. DERIV=1 ⇒ finite difference
CAPOP	-	*	MOS gate cap model selector: CAPOP=39 for BSIM2, CAPOP=13 for BSIM1, CAPOP=4 is a synonym for CAPOP=13. ■ If SPICE3=0, default CAPOP=13. ■ If SPICE3=1, default CAPOP=39.

Name (Alias)	Units	Default	Description
LMLT	-	1.0	Gate length shrink factor
XL	m	0	Difference between physical (on wafer) and drawn channel length. This parameter is used for L_{eff} calculation only if DL=0. $XL_{scaled} = XL \cdot SCALM$
LD	m	0	Lateral diffusion under gate (per side) of S/D junction. This parameter is used for L_{eff} calculation only if DL=0. $LD_{scaled} = LD \cdot SCALM$
LDAC	m		This parameter is the same as LD, but if LDAC is included in the .MODEL statement, it replaces LD in the Leff calculation for AC gate capacitance.
XW	m	0	Difference between physical (on wafer) and drawn S/D active width. This parameter is used for W_{eff} calculation only if DW=0. $XW_{scaled} = XW \cdot SCALM$
WMLT	-	1.0	Diffusion and gate width shrink factor
WD	m	0	Channel stop lateral diffusion under gate (per side). This parameter is used for W_{eff} calculation only if DW=0. $WD\ scaled = WD \cdot SCALM$
WDAC	m		This parameter is the same as WD, but if WDAC is included in the .MODEL statement, it replaces WD in the Weff calculation for AC gate capacitance.

Name (Alias)	Units	Default	Description
LREF	m	0 (∞)	Reference channel length for length adjustment of BSIM model parameters. For Berkeley compatibility (LREF-> ∞), use LREF=0. $LREF_{scaled} = LREF \cdot SCALM$
XLREF	m	0.0	Difference between physical and drawn reference channel length
WREF	m	0 (∞)	Reference device width for width adjustment of BSIM model parameters. For Berkeley compatibility (WREF-> ∞), use WREF=0. $WREF_{scaled} = WREF \cdot SCALM$
XWREF	m	0.0	Difference between physical and drawn reference channel width
DELVTO	V	0	Threshold voltage shift. This parameter is “type” sensitive. For example, DELVTO>0 increases the magnitude of n-channel threshold and decreases the magnitude of p-channel threshold. It adds to the element-line DELVTO parameter.
ALPHA	V^{-1}	0	Impact ionization coefficient. This parameter has associated geometry sensitivity parameters. Choose between BSIM2 (A10>0 and HSPICE (ALPHA>0) impact ionization modeling. D*o not use both.*
VCR	V	0	Impact ionization critical voltage. This parameter has associated geometry sensitivity parameters.

Name (Alias)	Units	Default	Description
IIRAT	-	0	Impact ionization source bulk current partitioning factor. One corresponds to 100% source. Zero corresponds to 100% bulk.
TCV	V/C	0	Zero-bias threshold voltage temperature coefficient. The sign of TCV is adjusted automatically for NMOS and PMOS to make threshold decrease in magnitude with rising temperature.
BEX	-	-1.5	Temperature exponent for mobility
FEX	-	0	Temperature exponent for velocity saturation
Px	*[x]*·μ μ^2	0	P*x* is Avant!'s proprietary WL-product sensitivity parameter for *x*, where *x* is a model parameter with length and width sensitivity.

LEVEL 39 Model Equations

In the following expressions, model parameters are in all upper case Roman. It is assumed that all model parameters have already been adjusted for geometry, and that those without a trailing "0" have already been adjusted for bias, as appropriate. The exceptions are U1 and N, whose bias dependences are given explicitly below.

Threshold voltage, V_{th}:

$$V_{th} = V_{bi} + K1\sqrt{PHI - V_{bs}} - K2(PHI - V_{bs}) - ETA \cdot V_{ds}$$

where:

$$V_{bi} = VFB + PHI$$

Strong inversion ($V_{gs} > V_{th} + VGHIGH$):

Linear region ($V_{ds}<V_{dsat}$) drain-source current I_{DS}:

$$I_{DS} = \frac{\beta'\left(V_{gs}-V_{th}-\frac{a}{2}V_{ds}\right)V_{ds}}{1 + UA(V_{gs}-V_{th}) + UB(V_{gs}-V_{th})^2 + U1 \cdot V_{ds}}$$

where:

$$V_{dsat} = \frac{V_{gs} - V_{th}}{a\sqrt{K}},$$

$$K = \frac{1 + V_c + \sqrt{1 + 2V_c}}{2},$$

$$V_c = \frac{U_{1S}(V_{gs} - V_{th})}{a[1 + UA(V_{gs}-V_{th}) + UB(V_{gs}-V_{th})^2]},$$

$$U_{1S} = U10 + U1B \cdot V_{bs},$$

$$U1 = U_{1S}\left[1 - \Theta(V_{dsat} - V_{ds})\frac{U1D(V_{ds} - V_{dsat})^2}{V_{dsat}^2}\right]$$

where $\Theta(x)$ is the usual unit step function,

$$\beta' = \beta_0 + \beta_1 \tanh\left(MU2\frac{V_{ds}}{V_{dsat}}\right) + \beta_3 V_{ds} - \beta_4 V_{ds}^2$$

$$\beta_0 = \frac{W_{eff}}{L_{eff}}MU \cdot C_{ox},$$

$$\beta_1 = \beta_S - (\beta_0 + \beta_3 VDD - \beta_4 VDD^2),$$

$$\beta_i = \frac{W_{eff}}{L_{eff}}MUi \cdot C_{ox}, \quad i = S, 3, 4,$$

$$a = 1 + \frac{gK1}{2\sqrt{PHI - V_{bs}}},$$

and:

$$g = 1 - \frac{1}{1.744 + 0.8364(PHI - V_{bs})}$$

Saturation ($V_{ds} > V_{dsat}$) drain-source current, I_{DS}:

$$I_{DS} = \frac{\beta'(V_{gs} - V_{th})^2}{2aK[1 + UA(V_{gs} - V_{th}) + UB(V_{gs} - V_{th})^2]} \cdot (1 + f)$$

where the impact ionization term, *f* is

$$f = AI \cdot e^{\frac{-BI}{V_{ds} - V_{dsat}}}.$$

Weak Inversion ($V_{gs} < V_{th}$+VGLOW; [VGLOW<0]):

Subthreshold drain-source current, I_{ds}:

$$I_{DS} = \beta' \cdot V_{tm}^2 \cdot \exp\left(\frac{V_{gs} - V_{th}}{N \cdot V_{tm}} + VOFF\right) \cdot \left[1 - \exp\left(-\frac{V_{ds}}{V_{tm}}\right)\right] \cdot (1 + f)$$

$$\text{where } V_{tm} = \frac{kT}{q} \text{ and } N = N0 + \frac{NB}{\sqrt{PHI - V_{bs}}} + ND \cdot V_{ds}$$

Strong inversion-to-weak inversion transition region (V_{th} +VGLOW≤ $V_{gs} \leq \varsigma_{th}$ +VGHIGH):

$$V_{geff}(V_{gst}) = \sum_{j=0}^{3} C_j V_{gst}^j$$

replaces $V_{gst} = V_{gs} - V_{th}$ in the linear or saturation drain currents, based on V_{dsat} (V_{geff}). At the lower boundary V_{gs}-V_{th}=VGLOW, the saturation equation is assumed to be valid for all V_{ds} (that is, V_{dsat} (V_{geff}(VGLOW)) ≈ 0), to allow a

match to the subthreshold equation given above. The coefficients Cj of the cubic spline V_{geff} are internally determined by the conditions that I_{DS} and dI_{ds}/dV_{gs} both be continuous at the boundaries $V_{gs} = V_{th}$ + VGLOW and $V_{gs} = V_{th}$ + VGHIGH.

Effective Length and Width

If DL is nonzero:

$$L_{eff} = L_{scaled} \cdot LMLT - DL$$

$$LREF_{eff} = LREF_{scaled} \cdot LMLT - DL$$

Otherwise,

$$L_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2 \cdot LD_{scaled}$$

$$LREF_{eff} = LREF_{scaled} \cdot LMLT + XLREF_{scaled} - 2 \cdot LD_{scaled}$$

If DW is nonzero:

$$W_{eff} = (W_{scaled} \cdot WMLT - DW) \cdot M$$

$$WREF_{eff} = (WREF_{scaled} \cdot WMLT - DW) \cdot M$$

Otherwise,

$$W_{eff} = (W_{scaled} \cdot WMLT + XW - 2 \cdot WD_{scaled}) \cdot M$$

$$WREF_{eff} = (WREF_{scaled} \cdot WMLT + XWREF_{scaled} - 2 \cdot WD_{scaled}) \cdot M$$

Geometry and Bias of Model Parameters

Most of the BSIM2 parameters have associated width and length sensitivity parameters. You can also specify Avant!-proprietary WL-product sensitivity parameters. If P is a parameter, then its associated width, length, and WL-product sensitivity parameters are WP, LP, and PP.

The value of the P' parameter, adjusted for width, length, and WL-product, is:

$$P' = P + WP \cdot \left(\frac{1}{W_{eff}} - \frac{1}{WREF_{eff}}\right) + LP \cdot \left(\frac{1}{L_{eff}} - \frac{1}{LREF_{eff}}\right)$$
$$+ PP \cdot \left(\frac{1}{W_{eff}} - \frac{1}{WREF_{eff}}\right) \cdot \left(\frac{1}{L_{eff}} - \frac{1}{LREF_{eff}}\right)$$

The WREF and LREF terms do not appear in Berkeley SPICE. They are effectively infinite, which is the default in the Avant! True-Hspice model.

The following BSIM2 parameters have no associated geometry sensitivity parameters:

- TOX
- TEMP (not used)
- VDD
- VGG
- VBB
- DL
- DW

The BSIM2 parameters ending in "0" are assumed to be valid at zero bias, and they have associated bias sensitivities, as given in the BSIM2 parameter table.

If PB, PD, and PG are the geometry-adjusted v_{bs}-, v_{ds}-, and v_{gs}- sensitivity parameters, respectively, associated with the geometry-adjusted zero-bias parameter P0, then in general the bias-dependent parameter P is given by

$$P = P0 + PB \cdot V_{bs} + PD \cdot V_{ds} + PG \cdot V_{gs}$$

The exceptions are the velocity saturation factor U1 and the subthreshold swing coefficient N. Expressions for their bias dependences is given later.

Compatibility Notes

SPICE3 Flag

If model parameter SPICE3=0 (default), certain Avant! corrections to the BSIM2 equations are effective. If SPICE3 is set to 1, the equations used are as faithful as possible to the BSIM2 equations for SPICE3E2. Even in this mode, certain numerical problems have been addressed and should not be noticeable under normal circumstances.

Temperature

The model reference temperature TNOM's default is 25˚C in the Avant! True-Hspice model, unless you set .OPTION SPICE. In this case TNOM defaults to 27˚ C. This option also sets some other SPICE compatibility parameters. In the True-Hspice model, you set TNOM in an .OPTION line in the netlist; to override this locally (that is, for a model), use the TREF model parameter. ("Reference temperature" means that the model parameters were extracted at, and are therefore valid at, that temperature.)

In UCB SPICE 3, TNOM (default 27˚ C) is not effective for the BSIM models, and model parameter TEMP is used (and must be specified) as both the model reference temperature and analysis temperature. The analysis at TEMP only applies to thermally activated exponentials in the model equations. There is no adjustment of model parameter values with TEMP. It is assumed that the model parameters were extracted at TEMP, TEMP being both the reference and analysis temperature.

For model levels *other than* 4 (BSIM1) and 5 (BSIM2) in UCB SPICE3, key model parameters are adjusted for the difference between TEMP (default 27˚C) and TNOM, and TEMP is specified in the netlist with .TEMP #, just as in the Avant! True-Hspice model.

In contrast to UCB SPICE's BSIM models, the Avant! True-Hspice LEVEL 39 model does provide for temperature analysis. The default analysis temperature is 25˚C in the True-Hspice model. Set .TEMP # in your netlist to change the True-Hspice analysis temperature (TEMP as a model parameter is NOT USED). The True-Hspice model provides temperature adjustment of key model parameters, as explained later.

Parasitics

ACM > 0 invokes the MOS source-drain parasitics in the Avant! True-Hspice model. ACM=0 (default) is SPICE style. See ‘True-Hspice Model Enhancements” on page 9-195.

Gate Capacitance Selection

CAPOP=39 selects the BSIM2 charge-conserving capacitance model as shipped with Berkeley SPICE 3E2. This is the default selection if SPICE3=1 is set. Please note that XPART (charge-sharing flag) is currently not a BSIM2 model parameter, despite its specification in the sample BSIM2 input decks shipped with Berkeley SPICE 3E. It appears that its use in SPICE 3E was as a printback debug aid. Saturation charge sharing appears to be fixed at 60/40 (S/D) in the BSIM2 capacitance model. Charge equations are given later under ‘Charge-based Gate Capacitance Model (CAPOP=39)” on page 9-193. See also ‘Modeling Guidelines and Removal of Mathematical Anomalies” on page 9-197.

Other CAPOPs can be chosen. CAPOP=13 (recommended) selects the Avant! BSIM1-based charge-conserving capacitance model that is in common usage with the Avant! True-Hspice MOS LEVELs 13 (BSIM1) and LEVEL 28 (modified BSIM1) models. This option is the default selection if SPICE3=0. With this capacitance model, charge sharing can be adjusted using model parameters XPART or XQC. See LEVEL 13 BSIM Model on page 9-102 for more information.

Unused Parameters

The DELL (S/D diode length reduction) and WDF (default device width) SPICE model parameters are not used in the Avant! True-Hspice model. The function of DELL in SPICE 3E cannot be determined. You can specify a default width in the Avant! True-Hspice model, on t .OPTION line, as DEFW (which defaults to 100μ).

.MODEL VERSION Changes to BSIM2 Models

The True-Hspice model provides a VERSION parameter to the .MODEL statement, which allows portability of LEVEL 13 BSIM and LEVEL 39 BSIM2 models between True-Hspice model versions. Use the VERSION parameter in a LEVEL 13 .MODEL statement; the following changes in the BSIM model:

Model Version	Effect of VERSION on BSIM2 Model
92A	LEVEL 39 BSIM2 model introduced: no changes
92B	No changes
93A	Introduces gds constraints, fixes WMU3B parameter defect, and introduces MU4 parameter defect
93A.02	VERSION parameter introduced, fixes MU4 parameter defect
95.1	Fixes defects that cause PMUSB, LDAC, WDAC parameter problems, fixes GMBS defect when gds constraints are used
96.1	Limited ETA + ETAB · vb5≥0

Preventing Negative Output Conductance

The Avant! True-Hspice model internally protects against conditions in the LEVEL 13 model that cause convergence problems due to negative output conductance. The constraints imposed are:

$$MU2 \geq 0 \quad ND \geq 0 \quad AI \geq 0$$

These constraints are imposed after length and width adjustment and *VBS* dependence. This feature is gained at the expense of some accuracy in the saturation region, particularly at high Vgs.

Consequently, BSIM2 models might need to be requalified in the following situations:

1. Devices exhibit self-heating during characterization, which causes declining I_{ds} at high V_{ds}. This would not occur if the device characterization measurement sweeps V_{ds}.
2. The extraction technique produces parameters that result in negative conductance.
3. Voltage simulation is attempted outside the characterized range of the device.

Charge-based Gate Capacitance Model (CAPOP=39)

The BSIM2 gate capacitance model conserves charge and has non-reciprocal attributes. The use of charges as state variables guarantees charge conservation. Charge partitioning is fixed at 60/40 (S/D) in saturation and is 50/50 in the linear region. $Q_s = -(Q_g+Q_d+Q_b)$ in all regions.

Accumulation region ($V_{gs}<V_{bs}$+VFB):

$$Q_g = C_{ox}W_{eff} \cdot L_{eff}(V_{gs} - V_{bs} - VFB)$$

$$Q_b = -Q_g$$

$$Q_d = 0$$

Subthreshold region (V_{bs} + VFB$<V_{gs}<V_{th}$ + VGLOW):

$$Q_g = C_{ox}W_{eff} \cdot L_{eff}(V_{gs} - V_{bs} - VFB)$$

$$\cdot \left[1 - \frac{V_{gs} - V_{bs} - VFB}{V_{gs} - V_{bs} - VFB - V_{gst}} + \frac{1}{3}\left\{ \frac{V_{gs} - V_{bs} - VFB}{V_{gs} - V_{bs} - VFB - V_{gst}} \right\}^2 \right]$$

$$Q_b = -Q_g$$

$$Q_d = 0$$

Saturation region ($V_{ds} > V_{dsat}$):

$$Q_g = \frac{2}{3}C_{ox}W_{eff} \cdot L_{eff} \cdot V_{gst} + Q_{bulk}$$

where:

$$Q_{bulk} = \frac{1}{3}C_{ox}W_{eff} \cdot L_{eff}[V_{th} - V_{bs} - VFB]$$

$$Q_b = -Q_{bulk}$$

$$Q_d = -\frac{4}{10} \cdot \frac{2}{3}C_{ox}W_{eff} \cdot L_{eff} \cdot V_{gst} = \left(-\frac{4}{15}\right)C_{ox}W_{eff} \cdot L_{eff} \cdot V_{gst}$$

Linear region ($\mathbf{V_{ds} < V_{dsat}}$):

$$Q_g = \frac{2}{3}C_{ox}W_{eff} \cdot L_{eff} \cdot V_{gst} \cdot \left[\frac{3\left(1 - \frac{V_{ds}}{V_{dsat}}\right) + \left(\frac{V_{ds}}{V_{dsat}}\right)^2}{2 - \frac{V_{ds}}{V_{dsat}}}\right] + Q_{bulk}$$

$$Q_b = -Q_{bulk}$$

$$Q_d = -\frac{1}{3}C_{ox}W_{eff} \cdot L_{eff} \cdot V_{gst}$$

$$\cdot \left[\frac{3\left(1 - \frac{V_{ds}}{V_{dsat}}\right) + \left(\frac{V_{ds}}{V_{dsat}}\right)^2}{2 - \frac{V_{ds}}{V_{dsat}}} + \frac{\frac{V_{ds}}{V_{dsat}}\left(1 - \frac{V_{ds}}{V_{dsat}}\right) + 0.2\left(\frac{V_{ds}}{V_{dsat}}\right)^2}{\left(2 - \frac{V_{ds}}{V_{dsat}}\right)^2}\right] + Q_{bulk}$$

True-Hspice Model Enhancements

In the following expressions, model parameters are in all upper case Roman. It is assumed that all model parameters without a trailing “0” have already been adjusted for both geometry and bias, as appropriate.

Temperature Effects

TLEV=1 is enforced for LEVEL=39. No other TLEV value is currently allowed.

Threshold voltage for LEVEL 39 TLEV=1 is adjusted according to:

$$V_{th}(T) = V_{bi}(T) + K1 \cdot \sqrt{\phi(T) - V_{bs}} - K2 \cdot (\phi(T) - V_{bs}) - ETA \cdot V_{ds}$$

where:

$$V_{bi}(T) = V_{to}(T) - K1 \cdot \sqrt{\phi(T)} + K2 \cdot \phi(T),$$

$$V_{to}(T) = V_{to} - TCV \cdot (T - T_{nom}),$$

and the nominal-temperature, zero-bias threshold voltage is given by

$$V_{to} = V_{bi} + K1 \cdot \sqrt{PHI} - K2 \cdot PHI$$

$$= VFB + PHI + K1 \cdot \sqrt{PHI} - K2 \cdot PHI,$$

and $\phi(T)$ is calculated according to the value of TLEVC as specified.

Mobility is adjusted according to

$$\mu(T) = \mu(T_{nom}) \cdot \left(\frac{T}{T_{nom}}\right)^{BEX} \text{ where } \mu = \frac{\beta'}{C_{ox}(W_{eff}/L_{eff})}.$$

Velocity saturation is adjusted through UIS according to

$$U1S(T) = U1S \cdot \left(\frac{T}{T_{nom}}\right)^{FEX}$$

In addition, all of the usual Avant! True-Hspice model adjustments to capacitances and parasitic, diodes and resistors are also effective.

Alternate Gate Capacitance Model

Select CAPOP=13 for the Avant! True-Hspice charge-conserving capacitance model, widely used with LEVEL=13 (BSIM1) and LEVEL=28 (improved BSIM1). See LEVEL 13 BSIM Model on page 9-102 for more details.

Impact Ionization

To select Avant! True-Hspice impact ionization modeling (instead of BSIM2), keep AI0=0, and specify model parameters ALPHA [ALPHA · (V_{ds} - V_{dsat}) replaces AI in equation for *f* in the BSIM2 equations section above], VCR (replaces BI), and IIRAT (multiplies *f*).

Avant! True-Hspice impact ionization modeling differs from BSIM2 modeling in two ways:

1. There is a bias term, V_{ds} - V_{dsat}, multiplying the exponential, as well as ALPHA.
2. The impact ionization component of the drain current can be partitioned between the source and the bulk with model parameter IIRAT. IIRAT multiplies *f* in the saturation I_{ds} equation. Thus, the fraction IIRAT of the impact ionization current goes to the source, and the fraction 1-IIRAT goes to the bulk, adding to I_{DB}. IIRAT defaults to zero (that is, 100% of impact ionization current goes to the bulk).

BSIM2's impact ionization assumes that all of the impact ionization current is part of I_{ds}. In other words, it flows to the source. This assumption can lead to inaccuracies in, for example, cascode circuits. See Calculating the Impact Ionization Equations on page 8-55 for more details.

Parasitic Diode for Proper LDD Modeling

The Avant! True-Hspice model has alternative MOS parasitic diodes to replace SPICE-style MOS parasitic diodes. These alternatives allow for geometric scaling of the parasitics with MOS device dimension, proper modeling of LDD parasitic resistances, allowance for shared sources and drains, and allowance for different diode sidewall capacitances along the gate edge and field edge.

The MOS parasitic diode is selected with model parameter ACM. ACM=0 (default) chooses SPICE style. The alternatives likely to be of most interest to the BSIM2 user are ACM=2 and 3.

ACM=2 allows for diode area calculation based on W, XW, and HDIF (contact to gate spacing). The calculation can be overridden from the element line. It further allows specification of LDIF (spacer dimension) and RS, RD (source and drain sheet resistance under the spacer) for LDD devices, as well as RSH (sheet resistance of heavily doped diffusion). Thus, total parasitic resistance of LDD devices is properly calculated.

ACM=3 uses all the features of ACM=2 and, in addition, its calculations of diode parasitics takes into account the sharing of source/drains, and different junction sidewall capacitances along the gate and field edges. Specify source/drain sharing from the element line with parameter GEO.

See Selecting MOSFET Diode Models on page 8-27 for more details.

Skewing of Model Parameters

The BSIM2 model file, like any other Avant! True-Hspice model, can be set up for skewing to reflect process variation. Worst-case or Monte-Carlo analysis can be performed, based on fab statistics. For more information, see Chapter 13, “Statistical Analysis and Optimization”, in the *Star-Hspice Manual*.

Star-Hspice Optimizer

The BSIM2 model, like any other Star-Hspice model, can be tied into the optimizer in an Avant! in-circuit simulator, for fitting to actual device data.

For more information, see Chapter 13, “Statistical Analysis and Optimization”, in the *Star-Hspice Manual*. An example fit appears at the end of this section.

Modeling Guidelines and Removal of Mathematical Anomalies

Because of the somewhat arbitrary geometric and bias adjustments given to BSIM2 parameters, they can take on non-physical or mathematically unallowed values in Berkeley SPICE 3. This can lead to illegal function arguments, program crashes, and unexpected model behavior (for example, negative conductance). The following guidelines and corrections must be satisfied at all geometries of interest and at biases, up to double the supply voltages (that is, to $V_{ds} = 2 \cdot VDD$, $V_{gs} = 2 \cdot VGG$, and $V_{bs} = 2 \cdot VBB$).

To avoid drain current discontinuity at $V_{ds} = V_{dsat}$, be sure that BI ≠ if AI0 ≠ 0.

To prevent negative g_{ds}, be sure that ETA > 0 and that MU3 > 0 and MU4 < MU3 / (4 * VDD). This should ensure positive g_{ds} at biases up to double the supply voltages. To simplify matters, set all MU4 parameters to zero. You can obtain reasonably good fits to submicron devices without using MU4[10.] .

In the Avant! True-Hspice model, U1S is prevented from becoming negative. A negative U1S is physically meaningless and causes negative arguments in a square root function in one of the BSIM2 equations. It is also recommended that U1D be kept less than unity (between 0 and 1).

For reasonable V_{th} behavior, make sure that $K1 - 2K2 \cdot \sqrt{PHI - V_{bs}} \geq 0$.

For the equations to make sense, the following must hold: N > 0, VGLOW ≤ 0, and VGHIGH ≥ 0.

The BSIM2 gate capacitance model of SPICE 3E tends to display negative C_{gs} in subthreshold. This appears to be due to $C_{gg} \rightarrow 0$ as $V_{gs} \rightarrow V_{th}$ by construction of the gate charge equation, so that $C_{gs} = C_{gg} - C_{gd} - C_{gb} \rightarrow - C_{gd} - C_{gb} \approx - C_{gb}$. Therefore the use of CAPOP=13 (default) is recommend until an improved BSIM2 gate capacitance model is released by Berkeley.

Modeling Example

The following is the result of fitting data from a submicron channel-length NMOS device to BSIM2. The fitting was performed with the Avant! ATEM characterization software and the Avant! simulation optimizer.

Figure 9-8: I_{DS} vs.V_{ds} for V_{gs} = 1, 2, 3, 4, 5V; BSIM2 Model vs. Data

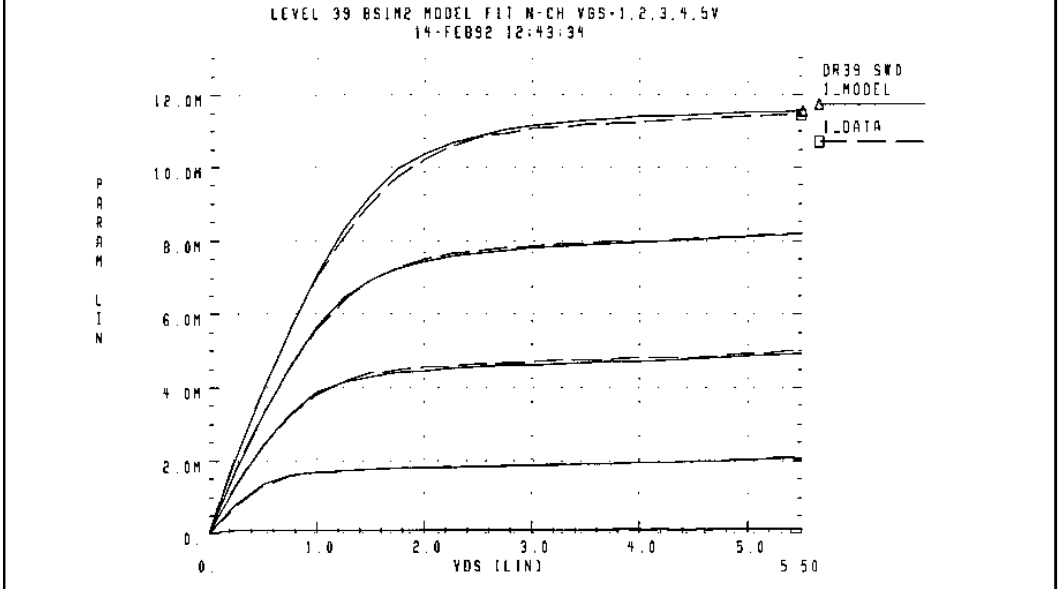


Figure 9-9: g_{ds} vs. V_{ds} for V_{gs} = 2, 3, 4, 5V; BSIM2 Model vs. Data, LOG scale

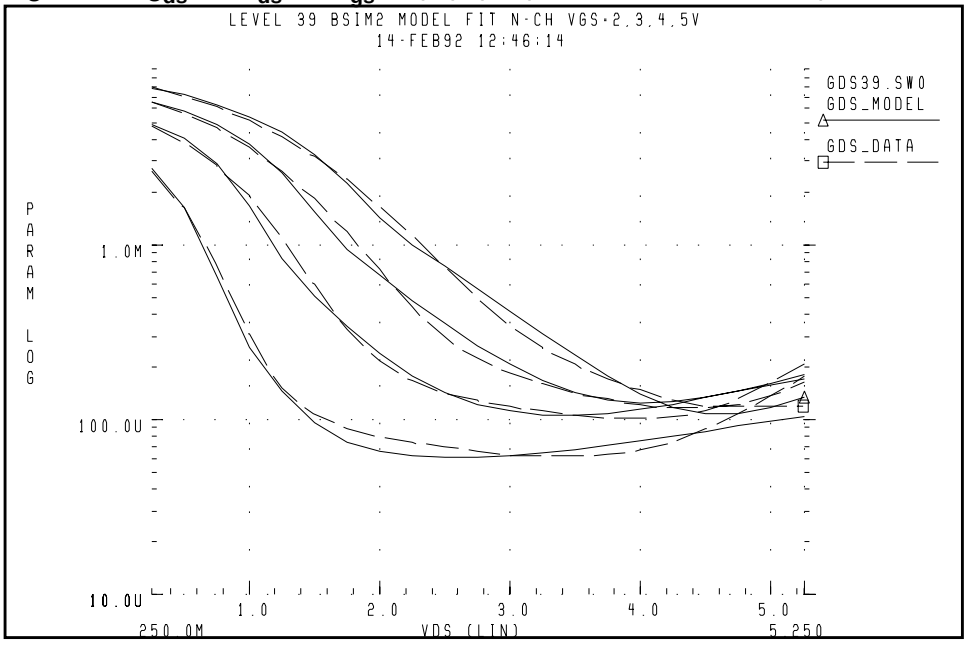


Figure 9-10: I_{DS} vs. V_{gs} for V_{ds} = 0.1V, V_{bs} = 0, -1, -2, -3, -4V, Showing Subthreshold Region; Model vs. Data

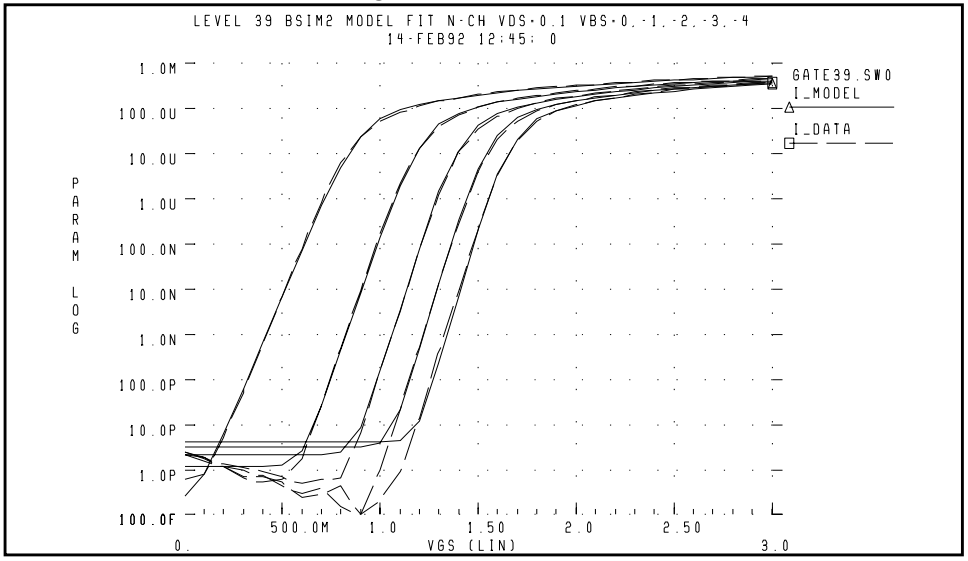
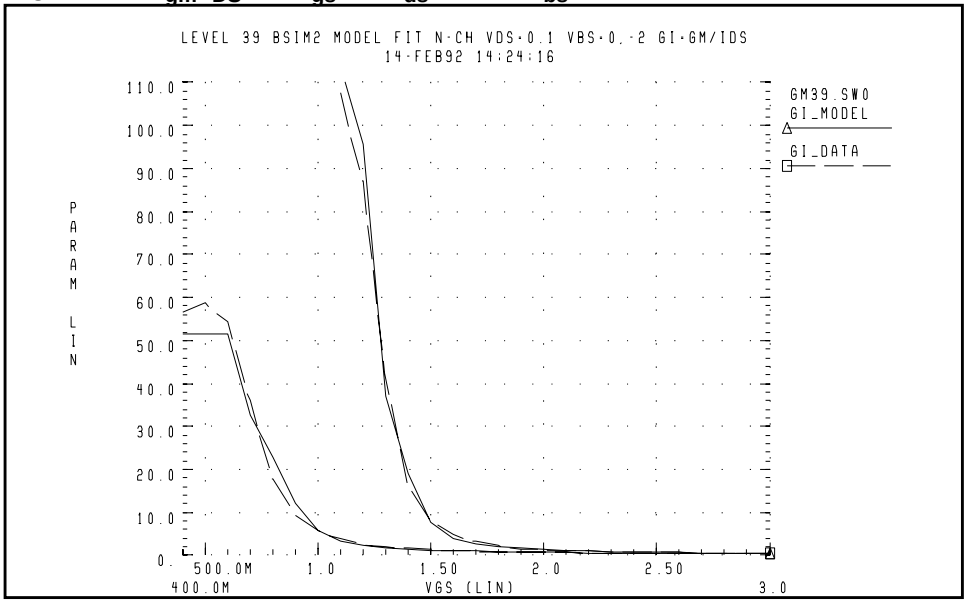


Figure 9-11: $_{gm}/I_{DS}$ vs. V_{gs} for V_{ds} = 0.1V, V_{bs} = 0, -2V; BSIM2 Model vs. Data



Typical BSIM2 Model Listing

In this example, geometry sensitivities are set to zero because a fit at only one geometry has been performed. Note the extra HSPICE parameters for LDD, temperature, and geometry.

```
.MODEL NCH NMOS LEVEL = 39
+ TOX = 2.000000E-02    TEMP = 2.500000E+01
+ VDD = 5.000000E+00    VGG = 5.000000E+00    VBB =-5.000000E+00
+ DL = 0.000000E+00     DW = 0.000000E+00
+ VGHIGH = 1.270000E-01 LVGHIGH= 0.000000E+00
+ WVGHIGH= 0.000000E+00
+ VGLOW =-7.820000E-02  LVGLOW = 0.000000E+00
+ WVGLOW = 0.000000E+00
+ VFB =-5.760000E-01    LVFB = 0.000000E+00
+ WVFB = 0.000000E+00
+ PHI = 6.500000E-01    LPHI = 0.000000E+00
+ WPHI = 0.000000E+00
+ K1 = 9.900000E-01     LK1 = 0.000000E+00    WK1 = 0.000000E+00
+ K2 = 1.290000E-01     LK2 = 0.000000E+00    WK2 = 0.000000E+00
+ ETA0 = 4.840000E-03   LETA0 = 0.000000E+00
+ WETA0 = 0.000000E+00
+ ETAB =-5.560000E-03   LETAB = 0.000000E+00
+ WETAB = 0.000000E+00
+ MU0 = 3.000000E+02
+ MU0B = 0.000000E+00   LMU0B = 0.000000E+00
+ WMU0B = 0.000000E+00
+ MUS0 = 7.050000E+02   LMUS0 = 0.000000E+00
+ WMUS0 = 0.000000E+00
+ MUSB = 0.000000E+00   LMUSB = 0.000000E+00
+ WMUSB = 0.000000E+00
+ MU20 = 1.170000E+00   LMU20 = 0.000000E+00
+ WMU20 = 0.000000E+00
+ MU2B = 0.000000E+00   LMU2B = 0.000000E+00
+ WMU2B = 0.000000E+00
+ MU2G = 0.000000E+00   LMU2G = 0.000000E+00
+ WMU2G = 0.000000E+00
+ MU30 = 3.000000E+01   LMU30 = 0.000000E+00
+ WMU30 = 0.000000E+00
+ MU3B = 0.000000E+00   LMU3B = 0.000000E+00
+ WMU3B = 0.000000E+00
+ MU3G =-2.970000E+00   LMU3G = 0.000000E+00
```

```
+ WMU3G = 0.000000E+00
+ MU40 = 0.000000E+00   LMU40 = 0.000000E+00
+ WMU40 = 0.000000E+00
+ MU4B = 0.000000E+00   LMU4B = 0.000000E+00
+ WMU4B = 0.000000E+00
+ MU4G = 0.000000E+00   LMU4G = 0.000000E+00
+ WMU4G = 0.000000E+00
+ UA0 = 0.000000E+00    LUA0 = 0.000000E+00
+ WUA0 = 0.000000E+00
+ UAB = 0.000000E+00    LUAB = 0.000000E+00
+ WUAB = 0.000000E+00
+ UB0 = 7.450000E-03    LUB0 = 0.000000E+00
+ WUB0 = 0.000000E+00
+ UBB = 0.000000E+00    LUBB = 0.000000E+00
+ WUBB = 0.000000E+00
+ U10 = 0.000000E+00    LU10 = 7.900000E-01
+ WU10 = 0.000000E+00
+ U1B = 0.000000E+00    LU1B = 0.000000E+00
+ WU1B = 0.000000E+00
+ U1D = 0.000000E+00    LU1D = 0.000000E+00
+ WU1D = 0.000000E+00
+ N0 = 8.370000E-01     LN0 = 0.000000E+00    WN0 = 0.000000E+00
+ NB = 6.660000E-01     LNB = 0.000000E+00    WNB = 0.000000E+00
+ ND = 0.000000E+00     LND = 0.000000E+00    WND = 0.000000E+00
+ VOF0 = 4.770000E-01   LVOF0 = 0.000000E+00
+ WVOF0 = 0.000000E+00
+ VOFB =-3.400000E-02   LVOFB = 0.000000E+00
+ WVOFB = 0.000000E+00
+ VOFD =-6.900000E-02   LVOFD = 0.000000E+00
+ WVOFD = 0.000000E+00
+ AI0 = 1.840000E+00    LAI0 = 0.000000E+00
+ WAI0 = 0.000000E+00
+ AIB = 0.000000E+00    LAIB = 0.000000E+00
+ WAIB = 0.000000E+00
+ BI0 = 2.000000E+01    LBI0 = 0.000000E+00
+ WBI0 = 0.000000E+00
+ BIB = 0.000000E+00    LBIB = 0.000000E+00
+ WBIB = 0.000000E+00
+ DELL = 0.000000E+00   WDF = 0.000000E+00
```

Common SPICE Parameters

```
+ CGDO = 1.000000E-09   CGSO = 1.000000E-09
+ CGBO = 2.500000E-11
+ RSH = 3.640000E+01    JS = 1.380000E-06
+ PB = 8.000000E-01     PBSW = 8.000000E-01
+ CJ = 4.310000E-04     CJSW = 3.960000E-10
+ MJ = 4.560000E-01     MJSW = 3.020000E-01
```

Avant! Parameters

```
+ ACM = 3               LMLT = 8.500000E-01
+ WMLT = 8.500000E-01
+ XL =-5.000000E-08     LD = 5.000000E-08
+ XW = 3.000000E-07     WD = 5.000000E-07
+ CJGATE = 2.000000E-10 HDIF = 2.000000E-06
+ LDIF = 2.000000E-07
+ RS = 2.000000E+03     TRS = 2.420000E-03
+ RD = 2.000000E+03     TRD = 2.420000E-03
+ TCV = 1.420000E-03  BEX =-1.720000E+00  FEX =-2.820000E+00
+ LMU0 = 0.000000E+00  WMU0 = 0.000000E+00 JSW=2.400000E-12
```

LEVEL 40 HP a-Si TFT Model

The Avant! True-Hspice LEVEL 40 model is a Hewlett-Packard amorphous silicon thin-film transistor model.

Model Parameters

Name	Units	Default	Description
UO	$cm^2/V/s$	1.0	Mobility
VTO	V	0.0	Zero voltage threshold voltage
PHI	V	0.0	Surface potential
NFS	cm^2	0.0	Fast surface state density
NSS	cm^2	0.0	Surface state density
T1	m	280n	First thin film thickness
T2	m	0.0	Second thin film thickness
E1		3.9	Dielectric constant of 1st film
E2		0.0	Dielectric constant of 2nd film
THETA	V^{-1}	0.0	Mobility modulation
ETA	V^{-1}	0.0	Static feedback on threshold voltage (difficulty of band bending)
VMAX	m/s	1e6	Maximum drift velocity of carriers
GO	ohm^{-1}	10e-15	Conductance of TFT leakage current
DEFF		2.0	Drain voltage effect for TFT leakage current

Name	Units	Default	Description
NU		0.0	First order temperature gradient
CHI		0.5	Temperature exponential part
PSI		1e-20	Temperature exponential part
K2		2.0	Temperature exponential part
VTIME	s	10m	Voltage stress
TREF		1.5	Temperature gradient of UO
RD	ohm	1.0K	(External) drain resistance
RS	ohm	1.0K	(External) source resistance
CGSO	F	1.0p	TFT gate-to-source overlap capacitance
CGDO	F	1.0p	TFT gate-to-drain overlap capacitance
CSC	F/m^2	10µ	Space charge capacitance
FREQ	Hz	400	Frequency of device
FEFF		0.5	Frequency effect constant
TAU	s	10n	Relaxation time constant

Using the HP a-Si TFT Model

1. Set LEVEL=40 to identify the model as the HP a-Si TFT model.
2. The default value for L is 10µm, and the default value for W is 40 µm.
3. Use the “M” designation for MOSFET rather than the “A” designation for a-Si TFT in the netlist.
4. Use the “NMOS” or “PMOS” designation for device type rather than the “NAT” or “PAT” designation.

   Note: Because of the unavailability of p-channel TFTs, PMOS model testing has been very limited.

5. The LEVEL 40 model is a three-terminal model. No bulk node exists; therefore, no parasitic drain-bulk or source-bulk diodes are appended to the model. A fourth node can be specified, but does not affect simulation results (except for GMIN terms).

6. Parasitic resistances and overlap capacitances are constant. They are not scaled with width, length, and temperature.

7. The capacitance expressions in this model do not conserve charge.

8. The HP a-Si TFT model has a TREF parameter that is an exponent in an expression for mobility temperature dependence.

   Other models use the BEX parameter for similar mobility temperature dependence expressions. The HP a-Si TFT TREF model parameter is *not the same as the reference temperature TREF* used in other models. The reference temperature for the HP a-Si TFT model is 312 K (or 38.85 ^{o}C), and cannot be modified. Experimental results from TFT manufacturers indicate that amorphous silicon materials are most stable at this temperature.

9. The default room temperature is 25^{o} C in the Avant! True-Hspice model, but is 27^{o} C in some other simulators. It is a matter of choice whether or not to set the nominal simulation temperature to 27^{o} C, by adding .OPTION TNOM=27 to the netlist. Although the *reference* temperature of the HP a-Si TFT model is fixed at 312^{o} K (or 38.85 ^{o}C), the behavior of the model adjusts to other *simulation* temperatures that are user specified or provided by Avant! in-circuit simulators as defaults.

10. HP's SPICE3E2 implementation of this model, on which this implementation is based, is not temperature-dependent. The LEVEL 40 has temperature dependency enabled.

11. The default value of CAPOP is 40, which is the HP a-Si TFT non-charge-conserving capacitance model. CAPOP values of 0, 1, 2, 3, 4, 5, 9, 12, or 13 are allowed, but have not been thoroughly tested.

12. The default of DERIV is zero, the analytical method. DERIV can be set to 1 to select the finite difference method.

Effect of SCALE and SCALM

The SCALE option has the same effect for LEVEL 40 as for other Avant! True-Hspice models, such as LEVEL 3 or LEVEL 28. If the values of L and W are in microns rather than meters (for example, L=1 rather than L=1µ or 1e-6), set .OPTION SCALE=1e-6.

The SCALM option is disabled in the LEVEL 40 model. For standard True-Hspice models (such as LEVEL 3), SCALM affects the scale of model parameters such as XL, XW, LD, WD, CJ, and CJSW.

Because the SCALM option is ignored by the LEVEL 40 model, LEVEL 40 models can be mixed in a simulation with other models in which the SCALM is set.

In general, netlists for Avant! simulators should be made as standard as possible. Also, it is best to convert L and W to meters scale instead of microns scale, so that the netlist can be used without the OPTION SCALE=1E-6. If these recommendations are followed, then a system-level Avant! simulation user can use I/O sub-circuits from different vendors in one simulation.

Noise Model

The LEVEL 40 model uses the standard NLEV=0 noise model inherited from the Avant! True-Hspice models.

DELVTO Element

DELVTO and DTEMP on the element line can be used with LEVEL 40.

True-Hspice Model and Element Statement Example

```
.MODEL nch nmos LEVEL=40 UO=0.4229 VTO=1.645 PHI=1.25 NSS=0
+ NFS=2.248E+21 VMAX=1231
+ THETA=-0.01771 ETA=0.0002703 T1=2.6E-07 T2=0 E1=3.9 E2=0
+ GO=9.206E-15 NU=0 K2=2 CHI=0.5
+ PSI=1E-20 VTIME=0.01 TREF=1.5 CGSO=5.203E-14 CGDO=4.43E-14
+ CSC=0.0001447 RD=5097
+ RS=5097 FREQ=1E+06 DEFF=2.15 TAU=1.64E-07 FEFF=0.5
MCKT 1 2 3 nch L=1e-05 W=4e-05
```

LEVEL 40 Model Equations

In the following equations, model parameters are shown in all capital letters; working variables are in lower case. Model parameters and bias voltages vgs and vds are inputs. Ids, gm, and gds are the DC outputs, and the gate-to-source capacitance Cgs and the gate-to-drain capacitance Cgd are the AC outputs. Electron charge is q, Boltzmann's constant is k, and the permittivity of a vacuum is $\varepsilon 0$.

Scaling by SCALE has been done prior to evaluation of the equations. Scaling by M is done after evaluation.

The variables gm_{tft} and gds_{tft} are intermediate, not final, quantities.

A complete description of TFT technology and the device physics underlying these equations can be found in the Hewlett-Packard HP IC-CAP manual.

Initially, $Cgdi = 0$, $Cgsi = 0$, $phi = PHI$, $vto = VTO$, $uo = UO$

If $uo = 0$ then $uo = 1$

Cfm, the dielectric capacitance per unit area, is computed as follows:

$$\text{If } T1 \neq 0 \text{ and } T2 \neq 0, \text{ then } Cfm = \frac{(\varepsilon 0 \cdot E1 \cdot E2)}{((T2 \cdot E1) + (T1 \cdot E2))}$$

$$\text{If } T1 = 0 \text{ and } T2 \neq 0, \text{ then } Cfm = \frac{(\varepsilon 0 \cdot E2)}{T2}$$

$$\text{If } T2 = 0 \text{ and } T1 \neq 0, \text{ then } Cfm = \frac{(\varepsilon 0 \cdot E1)}{T1}$$

$$kp = uo \cdot Cfm \cdot 10^{-4}$$

TEMP is the Avant! device simulation temperature, specified in ^{o}C, but converted to ^{o}K internally to evaluate these equations.

$$vt = \frac{(k \cdot TEMP)}{q}$$

$$eg = (2 \cdot 10^{4} \cdot (TEMP - 312)) + 1.4$$

$$vto = vto + (DELVTOmodel \cdot type) + (DELVTOelement \cdot type)$$

$$vbi = vto$$

$$\text{ratio} = \frac{\text{TEMP}}{312}$$

If $\text{VTIME} \le 1$, then $\text{uo} = \text{uo} \cdot (\text{ratio}^{\text{TREF}})$ and $\text{kp} = \text{kp} \cdot (\text{ratio}^{\text{TREF}})$.

Note: TREF is the LEVEL 40 model parameter TREF, which is an exponent in temperature adjustment equations. It is not the reference temperature of this device model.

$$\text{vfb} = \text{vto} - (0.5 \cdot \text{PHI}) + (0.5 \cdot (1.4 - \text{eg}))$$

$$\text{vbi} = \text{vfb} + (0.5 + \text{PHI} \cdot \text{ratio})$$

$$\text{vto} = \text{vbi} \quad \text{(printback definition)}$$

$$\text{phi} = \text{phi} \cdot \text{ratio} \quad \text{(printback definition)}$$

$$\text{vfb} = \text{vbi} - \text{phi} \quad \text{(printback definition)}$$

$$\text{vdsat} = 0$$

$$\text{beta} = \text{kp} \cdot \text{W} \cdot \text{L}$$

$$\text{vth} = \text{vbi} + (\text{ETA} \cdot \text{vds})$$

If $\text{NU} \neq 0$ and $\text{K2} \neq 0$ and $\text{PSI} \neq 0$ and $\text{VTIME} > 1$, then:

$$\text{vth} = \text{vth} + \text{f}(\text{vgs}, \text{vds}, \text{NU}, \text{K2}, \text{PSI}, \text{CHI}, \text{VTIME}, \text{TEMP})$$

$$\text{von} = \text{vth}$$

If $\text{NFS} \neq 0$, then:

$$\text{xn} = 1 + \left(\frac{(\text{q} \cdot \text{NFS} \cdot 10^4 \cdot \text{W} \cdot \text{L})}{\text{Cfm}}\right)$$

$$\text{von} = \text{f}(\text{vth}, (\text{vt} \cdot \text{xn}))$$

Cutoff Region (NFS = 0, vgs ≤ von)

If $NFS = 0$ and $vgs \le von$, then:

$$Cgdi = 0$$

$$Cgsi = 0$$

$$Ids = GO \cdot f(vgs, (DEFF \cdot vds))$$

$$gm = GO$$

$$gds = GO \cdot DEFF$$

Noncutoff Region (NFS ≠ 0)

If $vgs > von$, then:

$$vgsx = vgs$$

If $vgs \le von$, then:

$$vgsx = von$$

Mobility modulation by vgs:

$$ueff = f(uo, \eta, vgs, THETA)$$

If $VMAX > 0$, then:

$$vdsc = \frac{L \cdot VMAX}{ueff}$$

$$vdsat = (vgsx - vth) + vdsc - \sqrt{((vgsx - vth)^2 + vdsc^2)}$$

$$Cfmlw = \frac{(Cfm \cdot CSC)}{(Cfm + CSC)} \cdot L \cdot W$$

$Cfmlw$ is the series combination of the dielectric and space charge capacitance of the MIS structure.

If vds < vdsat, then:

$$vdsx = vds$$

$$epsfm = Cfm \cdot \frac{(T2 + T1)}{\varepsilon 0}$$

epsfm is the effective equivalent dielectric constant of the insulator layers.

$$fval = 0.8 + \left(\frac{epsfm - 0.8}{1 + (2 \cdot \pi \cdot FREQ \cdot TAU)^2} \right)$$

$$Cgdi = f(Cfmlw \cdot f(efm, 0.8) \cdot (exp(fval, FEFF, vgs - vth - vds)))$$

$$Cgsi = f(Cfmlw \cdot f(efm, 0.8) \cdot (exp(fval, FEFF, (vgs - vth), vds)))$$

Otherwise, vds ≥ vdsat :

$$vdsx = vdsat$$

$$Cgdi = Cfmlw$$

$$Cgsi = \frac{Cfmlw}{2}$$

If $vdsx \neq 0$, then:

$$cdnorm = vdsx \cdot \left(vgsx - vth - \frac{vdsx}{2} \right)$$

Normalized drain current:

$$gm_{tft} = vdsx$$

$$gds_{tft} = vgsx - vth - vdsx$$

$$cd1 = beta \cdot cdnorm$$

Drain current without velocity saturation effect:

$$beta = beta \cdot fgate$$

$$idrain = beta \cdot cdnorm$$

$$gm_{tft} = (beta \cdot gm_{tft}) + (dfgdvg \cdot cd1)$$

Velocity saturation factor—if $VMAX \neq 0$, then:

$$fdrain = \frac{1}{\left(1 + \left(\frac{vdsx}{vdsc}\right)\right)}$$

$$dfddvg = -dfgdvg \cdot \frac{((fdrain^2) \cdot vdsx)}{(vdsc \cdot fgate)}$$

$$dfddvd = \frac{-(fdrain^2)}{vdsc}$$

Strong inversion current:

$$gm_{tft} = (fdrain \cdot gm_{tft}) + (dfddvg \cdot idrain)$$

$$gds_{tft} = (fdrain \cdot gds_{tft}) + (dfddvd \cdot idrain)$$

$$idrain = fdrain \cdot idrain$$

$$beta = beta \cdot fdrain$$

$$Ids = idrain \cdot f(GO, vgs, DEFF, vds)$$

$$gm = f(gm_{tft}, GO)$$

$$gds = f(gds_{tft}, GO, DEFF)$$

Weak inversion current—if $vgs < von$, then:

$$idrain = idrain \cdot \exp\left(\frac{(vgs - von)}{(vt \cdot xn)}\right)$$

$$Ids = idrain + f(GO, vgs, DEFF, vds)$$

$$gm_{tft} = \frac{idrain}{(vt \cdot xn)}$$

$$gm = f(gm_{tft}, GO)$$

$$gds_{tft} = gds_{tft} \cdot \exp\left(\frac{(vgs - von)}{(vt \cdot xn)}\right)$$

$$gds = gds_{tft} + f(GO, DEFF)$$

vdsx = 0

$$Ids = f(GO \cdot vgs, DEFF, vds)$$

$$gm = GO$$

$$gds_{tft} = beta \cdot (vgsx - vth)$$

If $NFS \neq 0$ and $vgs < von$, then

$$gds_{tft} = gds_{tft} \cdot \exp\left(\frac{(vgs - von)}{(vt \cdot xn)}\right)$$

$$gds = f(gds_{tft}, GO, DEFF)$$

Cgd, Cgs

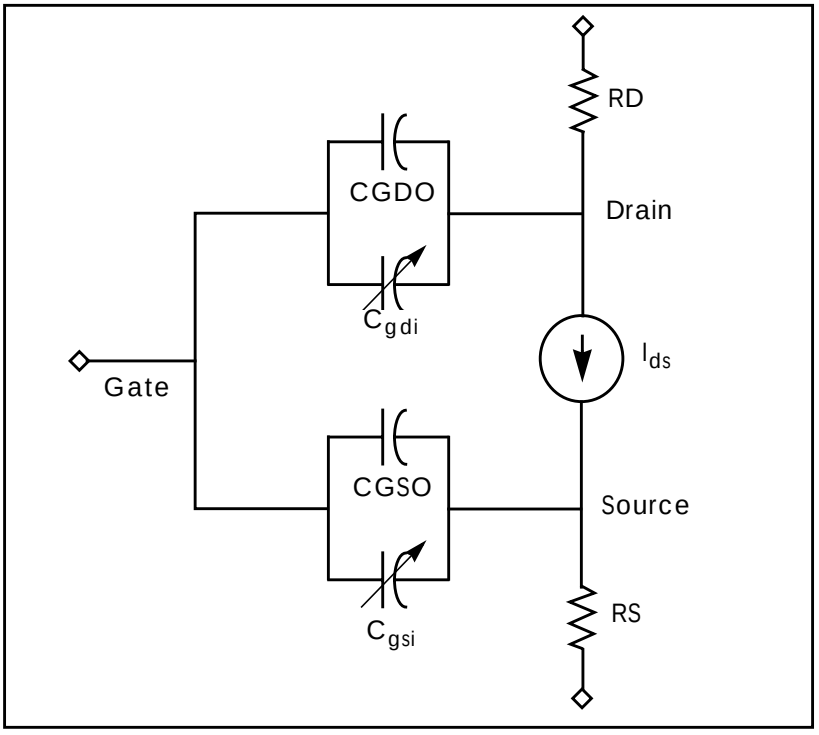
$$Cgd = Cgdi + CGDO$$

$$Cgs = Cgsi + CGSO$$

LEVEL 40 Model Topology

Figure 9-12 shows the topology of the LEVEL 40 model.

Figure 9-12: LEVEL 40 HP a-Si TFT Topology



Comparing MOS Models

This section reviews the history, motivation, strengths and weaknesses of the most commonly used Avant! True-Hspice MOS models:

LEVEL 2	SPICE LEVEL 2
LEVEL 3	SPICE LEVEL 3
LEVEL 13	BSIM1
LEVEL 28	Avant! proprietary model, based on BSIM1
LEVEL 39	SIM2

History and Motivation

This section describes the history of and motivation for using the Avant! True-Hspice MOS.

True-Hspice Model Enhancements

Avant! modified the standard SPICE models to satisfy the needs of customers. The modifications are in the areas of:

- Drawn dimensions with corrections for photolithography and diffusion
- Corrections for optical shrink
- Model-independent process variation parameters
- Uniform subthreshold equations
- Charge-conserving capacitance equations
- Impact ionization with selectable source/bulk partitioning of the excess drain current
- Enhanced temperature relationships

LEVEL 2

The LEVEL 2 model is an enhanced Grove equation. It is the most common of MOS equations in all simulators.

The basic current equation with the 3/2-power terms was developed by Ihantola and Moll in 1964. Channel length modulation was added by Reddi and Sah in 1965. The vertical field reduction was added by Crawford in 1967. The ECRIT parameter was added by Klassen in 1978.

LEVEL 3

The LEVEL 3 model was developed by Liu in 1981. It is computationally more efficient, replacing the 3/2-power terms with a first-order Taylor expansion. The drain-induced barrier lowering effect (ETA parameter) was added.

The LEVEL 3 models is impressively physical, modeling two-dimensional effects based on junction depth and depletion depths.

LEVEL 13 - BSIM

The BSIM1 model was developed by Sheu, Scharfetter, Poon and Hu at Berkeley in 1984, for higher accuracy modeling of short-channel devices. The approach is empirical rather than physical. It uses polynomials frequently. This makes it easier to write a parameter extraction program, but the polynomials often behave badly. For example, a quadratic function of VDS is used for mobility. Parameters specify the values at VDS=0 and 5 and the slope at VDS=5; unfortunately, values that look reasonable can produce a quadratic that is non-monotonic, giving a GDS<0 problem.

The Avant! True-Hspice implementation of BSIM1 as the LEVEL 13 model removed discontinuities in the current function, added temperature parameters, and added diode and capacitance models consistent with other models. The Berkeley version did not include temperature parameters.

LEVEL 28

LEVEL 28 is a proprietary Avant! True-Hspice model for submicron devices, designed to fix the following problems in BSIM1:

- Negative GDS
- Bad behavior of some polynomial expressions
- A kink in GM at threshold

LEVEL 28 is based on BSIM1, but some of the parameters are quite different. A BSIM1 parameter set cannot be used as a LEVEL 28 model. The LEVEL 28 model is designed for optimization; there is no simple extraction program. It has proven stable for automated model parameter generation.

Optimization of LEVEL 28 models to IDS, GDS, GM data is accomplished routinely by Avant!.

LEVEL 39

The BSIM2 model was developed by Duster, Jeng, Ko, and Hu, and released in SPICE3 in 1991. It is designed for deep submicron devices. It uses a cubic spline to give smooth weak inversion transition and has many additional parameters for improved accuracy. The GDS transition at VDSAT is markedly smoother than in BSIM1.

Future for Model Developments

This sequence of models shows a trend towards empirical rather than physical models, and an ever- increasing number of parameters. It is unfortunate to lose contact with the physics, but it can be unavoidable, because the physics has become less universal. Short-channel devices are much more sensitive to the detail of the process. I-V curves from different manufacturers show qualitative differences in the shape of the curves. Therefore, the models need to be very flexible, requiring a large number of empirical parameters.

Model Equation Evaluation Criteria

This section describes the following aspects of the model equations:

- Potential for good fit to data
- Ease of fitting to data
- Robustness and convergence properties
- Behavior follows actual devices in all circuit conditions
- Ability to simulate process variation
- Gate capacitance modeling

Some of these aspects depend on general features of the Avant! True-Hspice models that are the same for all levels. Others result in simple objective measures for comparing the levels. These measures are summarized in the ‘Comparing Avant! Model Parameters and UCB SPICE 2/3” on page 9-124.

Potential for Good Fit to Data

Generally, the model with the largest number of parameters has the potential to give the best fit. For the purpose of comparing the models, the number of parameters are counted in two ways.

Measure: Number of Parameters

Only the drain current parameters are counted, not the diode or series resistance, nor gate capacitance and impact ionization parameters, since these are almost the same for all levels.

```
LEVEL 2: VTO, PHI, GAMMA, XJ, DELTA, UO, ECRIT, UCRIT, UTRA,
UEXP, NSUB, LAMBDA, NFS (total=13).

LEVEL 3: VTO, PHI, GAMMA, XJ, DELTA, ETA, UO, THETA, VMAX,
NSUB, KAPPA, NFS (total=12).

LEVEL 13: VFB0, PHI0, K1, K2, ETA0, X2E, X3E, MUZ, X2M, X3MS,
MUS, X2MS, U00, X2U0, U1, X2U1, X3U1, N0, ND0, NB0, plus L-
and W- variation parameters (total = 20*3 = 60).

LEVEL 28: similar to LEVEL 13, minus MUS, X2MS, plus X33M,
WFAC, WFACU (total = 21*3 = 63).

LEVEL 39: VGHIGH, VGLOW, VFB, K1, K2, ETA0, ETAB, MU0, MU0B,
MUS0, MUSB, MU20, MU2B, MU2G, MU30, MU3B, MU40, MU4B, MU4G,
UA0, UAB, UB0, UBB, U10, U1B, U1D, N0, NB, ND, plus L- and
W- parameters (total = 33*3=99).
```

Measure: Minimal Number of Parameters

The minimal number of parameters is a subset of the above parameters, that you use to fit a specific W/L device. LEVEL 2 and 3 drop DELTA, which is a W-effect parameter. LEVEL 13 and 28 drop the L- and W- terms and the X2E, X3E, and ND0 second-order effects. LEVEL 39 drops ETAB, MU40, MU4B, MU4G, and ND.

The resulting minimal parameter counts for the five models are:

- LEVEL 2=12
- LEVEL 3=11
- LEVEL 13=17
- LEVEL 28=18
- LEVEL 39=28

Ease of Fit to Data

Generally, the larger the “minimal number of parameters”, the more time needs to be spent fitting the data. The systematic L and W effect parameters of LEVEL 13, 28, and 39 makes fitting easier because optimization can be done to individual W/L devices. Then the final model parameters, with L and W terms, can be calculated from the individual models. On the other hand, the more physical parameters of LEVEL 2 and 3 are helpful because it is easier to predict the value from a knowledge of the process, before fitting to I-V data. Examples of physical parameters are junction depths and doping concentrations.

Measure: Physical Percentage of Parameters

Starting with the minimal set of parameters, the percentage that are physical are calculated. For LEVEL 2— PHI, XJ, UO, ECRIT, NSUB, and NFS are physical, while VTO, GAMMA, UCRIT, UTRA, UEXP, LAMBDA are empirical, which gives 50% physical parameters. For LEVEL 3— PHI, XJ, UO, VMAX, NSUB, NFS are physical, which gives 55%. For LEVELs 13, 28, and 39—only PHI0 and MUZ are physical, giving 12%, 11%, and 7% physical parameters, respectively.

Robustness and Convergence Properties

A discontinuity in the derivatives GM, GDS, GMBS can cause convergence problems. Also, since real devices have continuous derivatives, a discontinuity leads to a large inaccuracy in the derivatives near that region. This can be annoying to an analog designer looking at a plot of gain versus bias, for example. The most common important discontinuities are GDS at vds=vdsat, and GM at vgs=vth. The LEVEL 2 and 3 models have these discontinuities, while the LEVEL 13, 28, and 39 models do not.

However, the LEVEL 13 model (BSIM1) often produces a negative GDS, which is obviously inaccurate, and causes oscillation, which can lead to convergence failure or a “timestep too small” error. It is possible for a LEVEL 13 model to avoid negative GDS, but it depends on complex relationships between the parameters MUZ, X2M, MUS, X2MS, X3MS, U1, X2U1, X3U1. Usually, a negative GDS can be removed by setting X3MS=0, but this lowers the accuracy of the model in the linear region. The LEVEL 39 (BSIM2) model also can produce negative GDS, unless you select parameters carefully. The LEVEL 28 model does not give negative GDS.

The BSIM1 model has a continuous GM at vgs=vth, but a plot of GM/IDS versus VGS shows a kink, while data from real devices is monotonic. This kink is annoying to analog designers working with devices in the weak and medium inversion region. LEVEL 28 and 39 have solved this problem, at the cost of additional parameters.

There are three more important measures, as follows:

Measure: Continuous Derivatives

```
LEVELs 2 and 3 fail. LEVELs 13, 28, and 39 pass.
```

Measure: Positive GDS

```
LEVELs 13 and 39 fail. LEVELs 2, 3, and 28 pass.
```

Measure: Monotonic GM/IDS in weak inversion

```
LEVELs 2, 3, and 13 fail. LEVELs 28 and 39 pass.
```

Behavior Follows Actual Devices In All Circuit Conditions

A model can be a very good fit to IDS data in the normal operating region, and still fail to be useful for simulating some circuits.

The first criterion is that the model should have good temperature dependence. The True-Hspice models provide temperature-dependence parameters for threshold voltage and mobility for all levels. The LEVEL 13, 28 and 39 models also have an FEX parameter that controls VDSAT variation with temperature.

The next most important criterion is that the model should have subthreshold current to provide accurate analog simulation. Even for digital circuits it aids in convergence. Fortunately, all of these models have subthreshold current.

Impact ionization causes a drain-to-bulk current that has a strong effect on cascode circuits. The Avant! True-Hspice models provide ALPHA and VCR parameters for this current, which can be used for all levels.

The BSIM2 model has a more complex impact ionization model, with parameters AI0, AIB, BI0, BIB, but in the Berkeley SPICE3 release this current was all assigned to drain-to-source current, IDS. Using the True-Hspice ALPHA and VCR parameters, the impact ionization current is assigned to IDB, which is essential for cascode simulation. The True-Hspice IIRAT parameter allows the model to divide the current between IDS and IDB, if needed.

Ability to Simulate Process Variation

Usually, full model parameter extraction or optimization is only done on a small number of test wafers. Statistical data on process variation is gathered by in-fabrication measurements (for example, TOX) and simple electrical measurements (for example, VT), made on a large number of wafers. This statistical data gives variances that are used to simulate process variation, using a worst-case, Monte-Carlo, or Taguchi methodology.

In order to do this simulation, models must be modified to take into account variations in TOX, thresholds, line widths, and sheet resistance. In the Avant! True-Hspice models, the different levels use these parameters in similar ways. All of the models discussed here accept the following parameters: TOX, DELVTO, XL, XW, RSH. The DELVTO model parameter shifts the threshold.

For the LEVEL 2 and 3 models, setting DELVTO=0.1 is equivalent to adding 0.1 to VTO; for the LEVEL 13, 28, 39 models, it is equivalent to adding 0.1 to VFB0. The parameters XL and XW represent line width variation. The equation for effective channel length is:

$$Leff = L + XL - 2 \cdot LD$$

The Berkeley BSIM1 and BSIM2 models use Leff = L - DL. The DL and DW parameters (DL0, DW0 for BSIM1) are supported in the Avant! True-Hspice models for compatibility; using XL, LD, XW, WD is recommended instead. In the True-Hspice models, the geometry parameters (XL, LD, XW, WD) and the parasitic parameters (CJ, MJ, CJSW, MJSW, RSH) are kept simple and level-independent to use process variation information consistently.

Gate Capacitance Modeling

LEVEL 2 and 3 were released in Berkeley SPICE with the Meyer model for gate capacitance. This model is non-charge-conserving and sets dQG/dVD = dQD/dVG, which is not valid in a real device, although provides an adequate response for most digital simulations. The BSIM1 and BSIM2 models were released from Berkeley with charge-conserving, non-symmetric capacitance models.

In the Avant! True-Hspice models, several choices of capacitance models are available; the range of choices and the default varies with the model chosen. The default for LEVELs 2 and 3 is still the Meyer model, but you can also select a charge-conserving Ward-Dutton model.

LEVEL Comparisons

LEVEL	**2**	**3**	**13**	**28**	**39**
Number of parameters	13	12	60	63	99
Minimal number of parameters	12	11	17	18	28
Physical parameters	50%	55%	12%	11%	7%
Continuous derivatives	no	no	yes	yes	yes
Positive GDS	yes	yes	no	yes	no
Monotonic GM/IDS	no	no	no	yes	yes

Outline of Optimization Procedure

1. Extract XL, LD, XW, WD, TOX, RSH, CGSO, CGDO, CGBO, CJ, MJ, CJSW, MJSW from resistor and capacitor data, and plots of Beta vs. W, L.
2. For each W/L device,
   a) Extract VT versus VBS from IDS vs. VGS data.
   b) Calculate ETA from log(IDS) vs. VGS plots at VDS=0.1, 5.0.
   c) Fit VT parameters to the VT vs. VBS data.
   d) Optimize the rest of the parameters, except L and W sensitivity parameters, to IDS, GDS, GM vs. VGS, VDS, VBS data.
3. For each W/L device, calculate L and W sensitivity parameters from the optimized parameters of nearby devices.
4. Fit the models together into one model using the Avant! True-Hspice Lmin, Lmax, Wmin, Wmax feature.

Examples of Data Fitting

The following plots show fits of LEVELs 2, 3, 13, 28, 39 to data from a submicron device, fabricated by a modern CMOS process. All of the models were optimized to the same data. Similar optimization files were used, optimizing different parameters. The Avant! True-Hspice impact ionization model, with ALPHA and VCR parameters, was used in all models except LEVEL 39, which has its own impact ionization parameters.

The problem of negative GDS in LEVEL 13 was avoided by improved optimization of parameter values, but the GDS discontinuity in LEVEL 3 and the GM discontinuity in LEVEL 2 could not be avoided.

Model versus data plots are presented for drain and gate sweeps. These are followed by close-up plots of the models with small step size to show GM and GDS problems with the individual levels.

LEVEL 28, 2, 3—Ids Model vs. Data

- Ids vs. Vds at Vgs=1, 2, 3, 4, 5, Vbs=0
- Fits to IDS only (not GDS and GM) would have looked better for these plots, but would not have been acceptable for analog design.

Figure 9-13: LEVEL 2 Ids Model vs. Data Curves

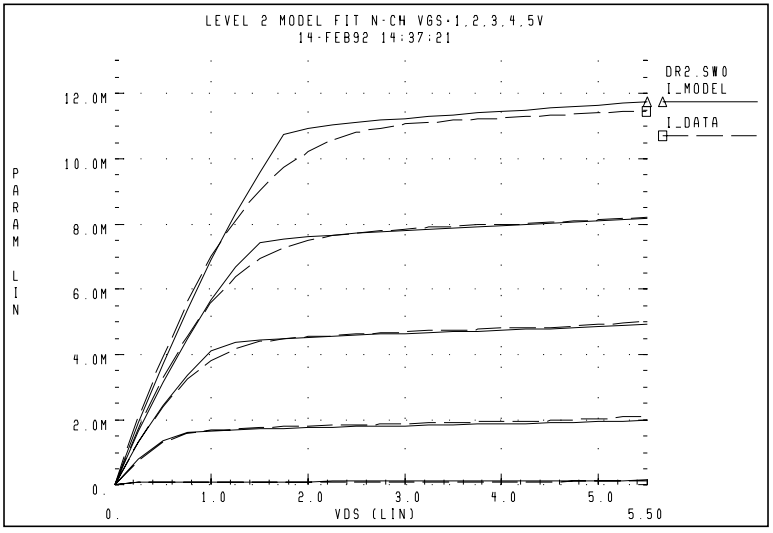


Figure 9-14: LEVEL 28 Ids Model vs. Data Curves

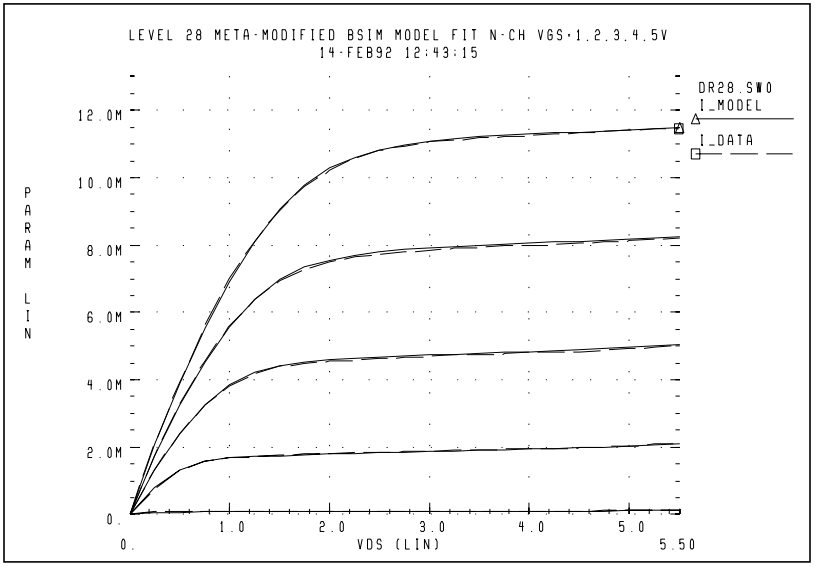
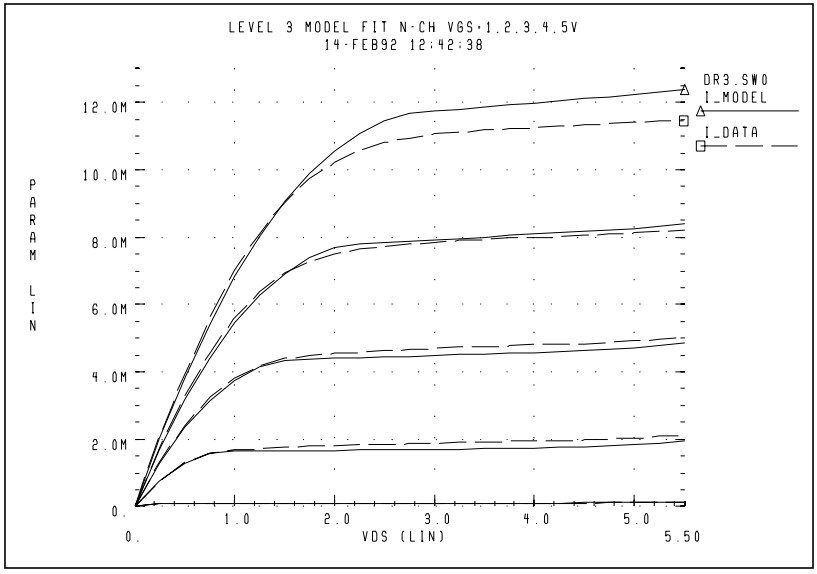


Figure 9-15: LEVEL 3 Ids Model vs. Data Curves



LEVEL 13, 28, 39 - Ids Model vs. Data

Ids vs. Vds at Vgs= 1, 2, 3, 4, 5, Vbs=0

Figure 9-16: LEVEL 13 Ids vs. Vds Curves

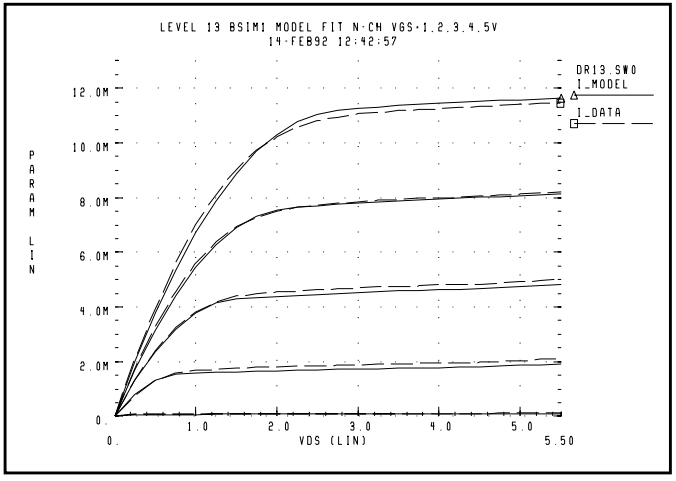


Figure 9-17: LEVEL 28 Ids vs. Vds Curves

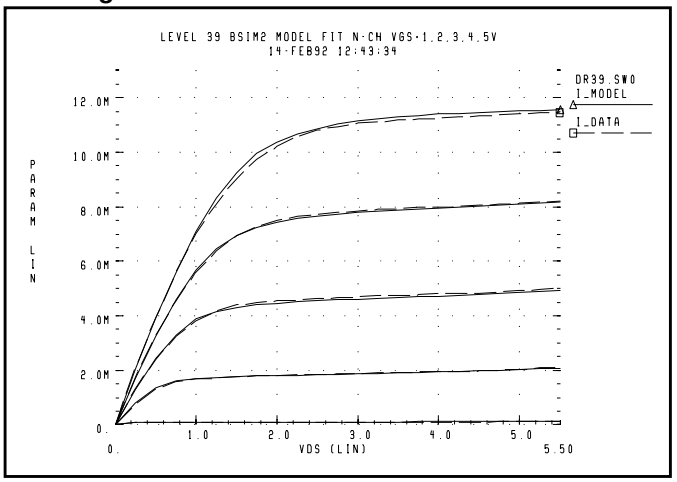
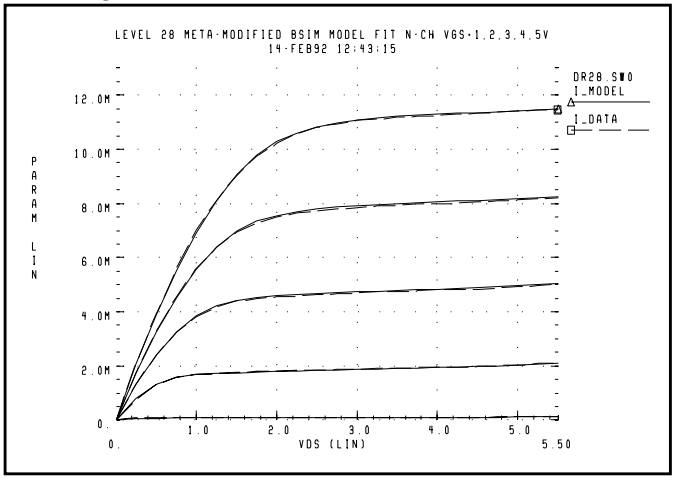


Figure 9-18: LEVEL 39 Ids vs. Vds Curves



LEVEL 28, 2, 3—Gds Model vs. Data

- gds -vs.- Vds at Vgs=2, 3, 4, 5, Vbs=0
- This plot shows the inability of LEVEL 2 and 3 to model GDS accurately.

Figure 9-19: LEVEL 2 gds vs. Vds Curves

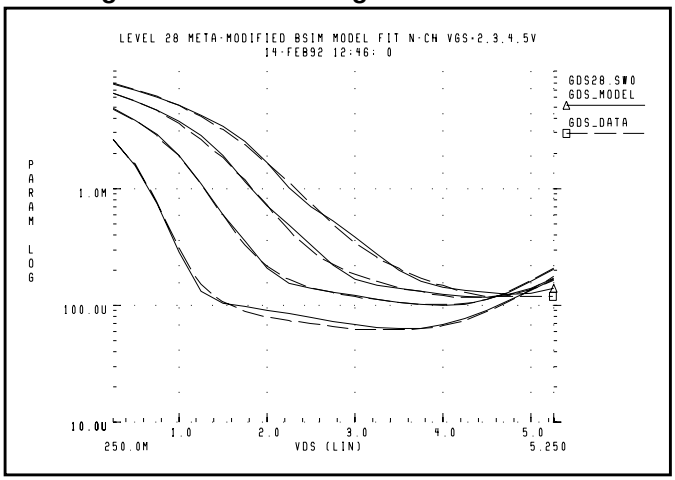


Figure 9-20: LEVEL 28 gds vs. Vds Curves

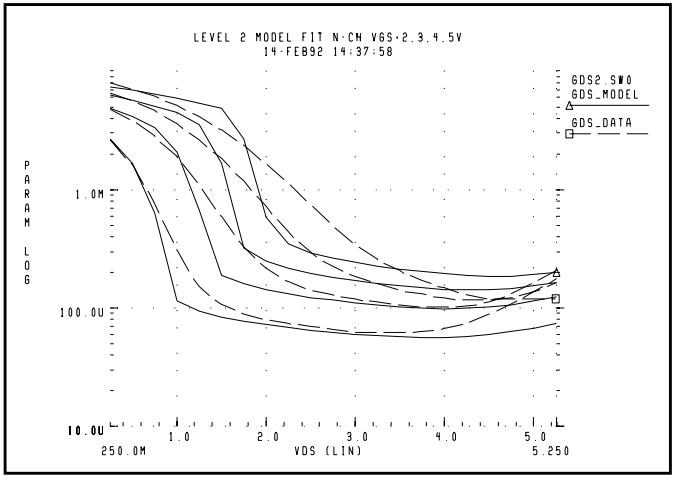
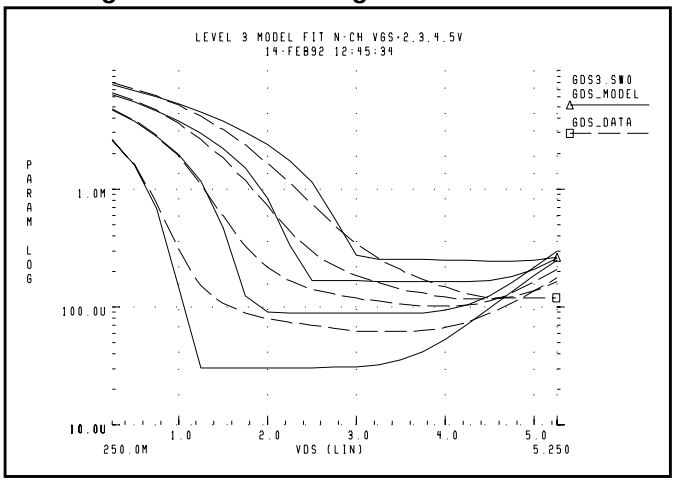


Figure 9-21: LEVEL 3 gds vs. Vds Curves



LEVEL 13, 28, 39—Gds Model vs. Data

- gds = vs. Vds at Vgs=2, 3, 4, 5, Vbs=0
- These models still have a small change in slope of Gds at Vdsat, more visible for the LEVEL 13 model than for LEVEL 28 or 39.

Figure 9-22: LEVEL 13 gds vs. Vds Curves

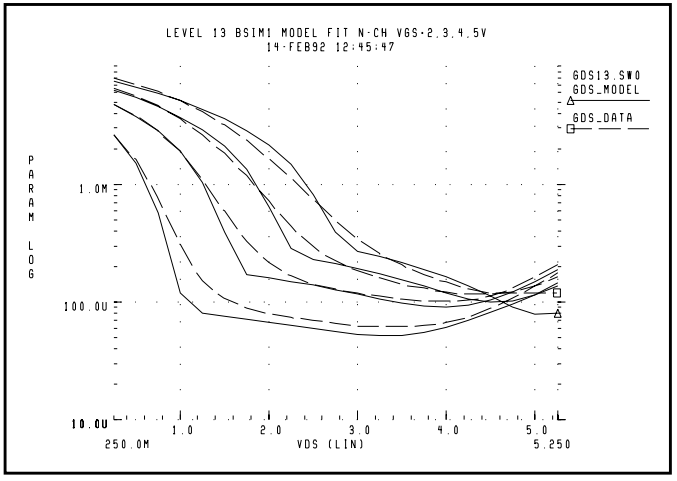


Figure 9-23: LEVEL 28 gds vs. Vds Curves

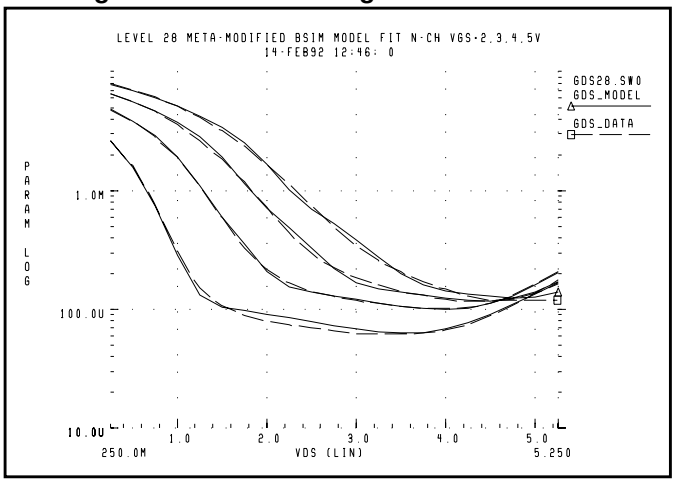
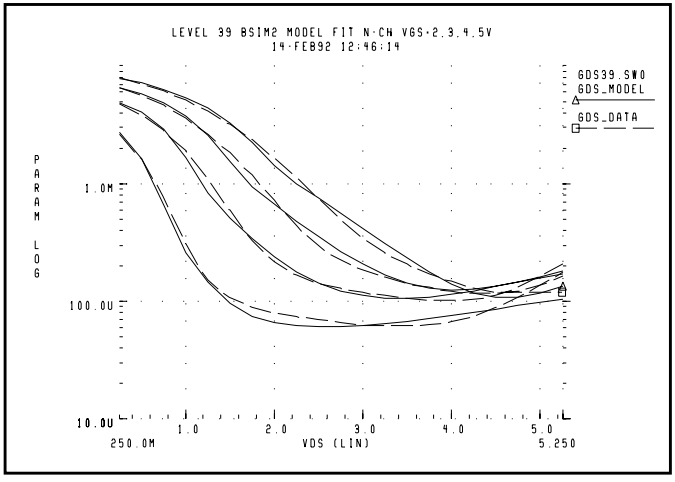


Figure 9-24: LEVEL 39 gds vs. Vds Curves



LEVEL 2, 3, 28— Ids Model vs. Data

Ids -vs.- Vgs at Vds=0.1, Vgs =0, -1, -2, -3, -4

Figure 9-25: LEVEL 2 Ids vs. Vgs Curves

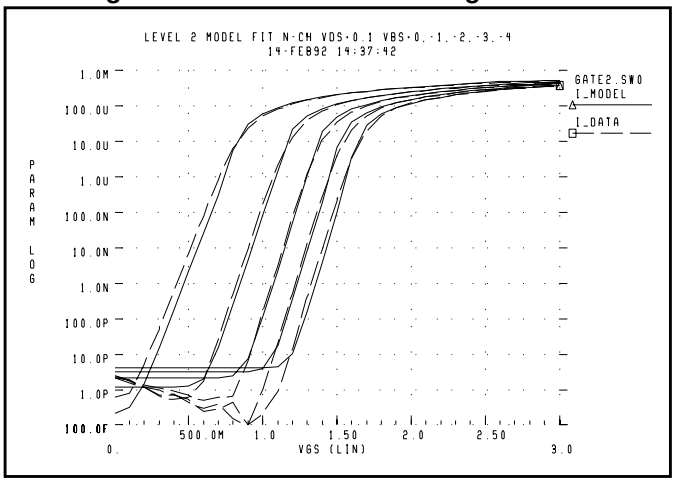


Figure 9-26: LEVEL 28 Ids vs. Vgs Curves

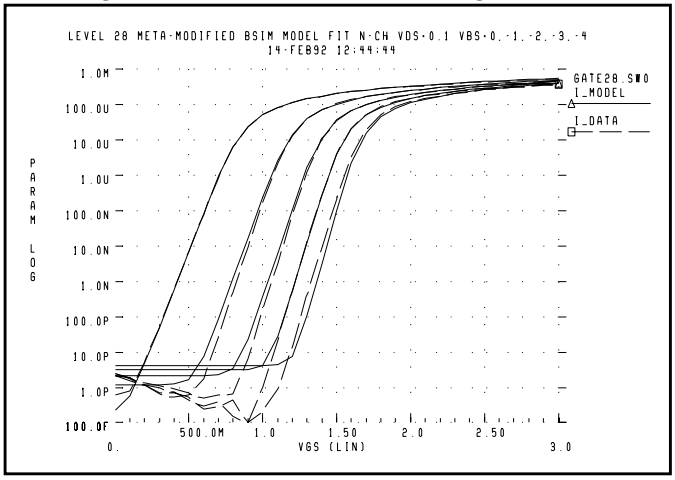
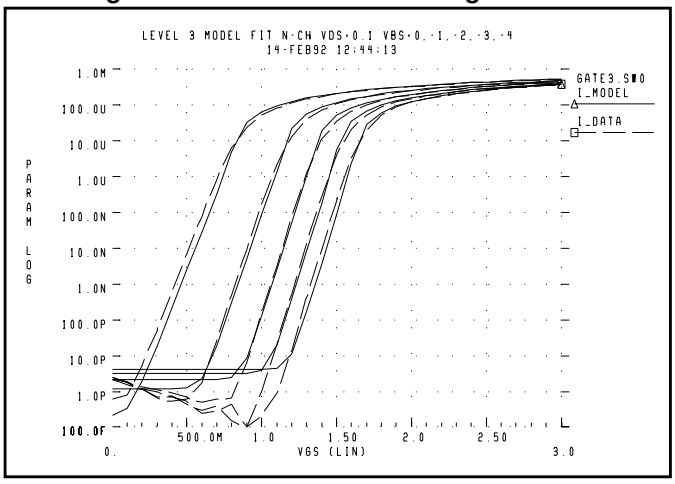


Figure 9-27: LEVEL 3 Ids vs. Vgs Curves



LEVEL 13, 28, 39—Ids Model vs. Data

Ids -vs.- Vgs at Vds=0.1, Vbs =0, -1, -2, -3, -4

Figure 9-28: LEVEL 13 Ids vs. Vgs Curves

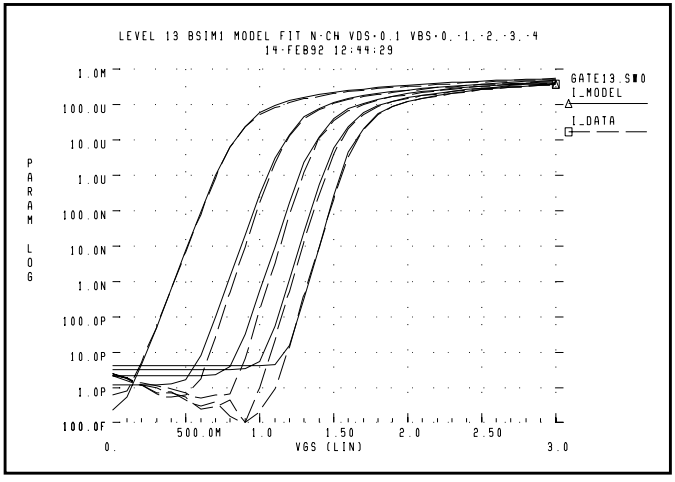


Figure 9-29: LEVEL 28 Ids vs. Vgs Curves

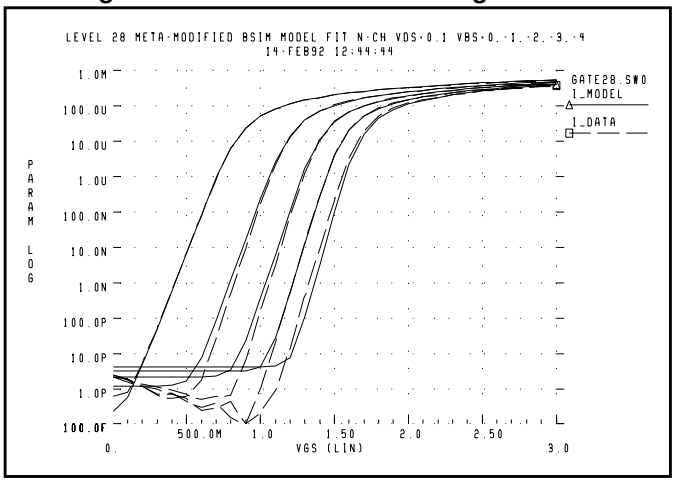
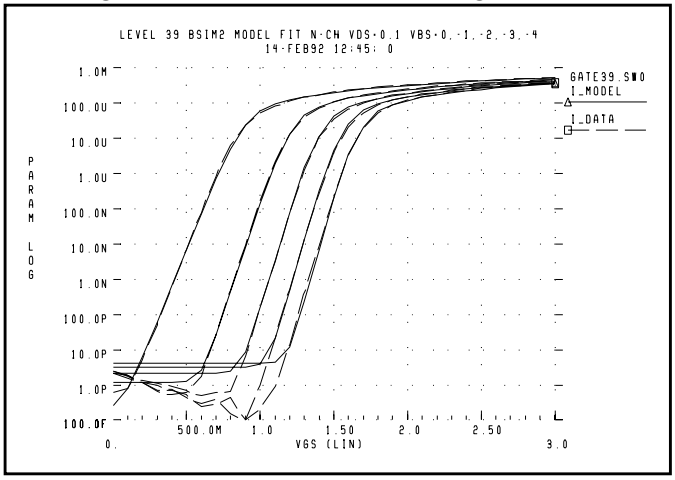


Figure 9-30: LEVEL 39 Ids vs. Vgs Curves



LEVEL 2, 3, 28—Gm/Ids Model vs. Data

- gm/Ids -vs.- Vgs at Vds=0.1, Vbs =0, -2
- The LEVEL 2 and 3 models have spikes at Vgs=Vth. The data, and the LEVEL 28 model, is monotonic decreasing.

Figure 9-31: LEVEL 2 gm/Ids vs. Vgs Curves

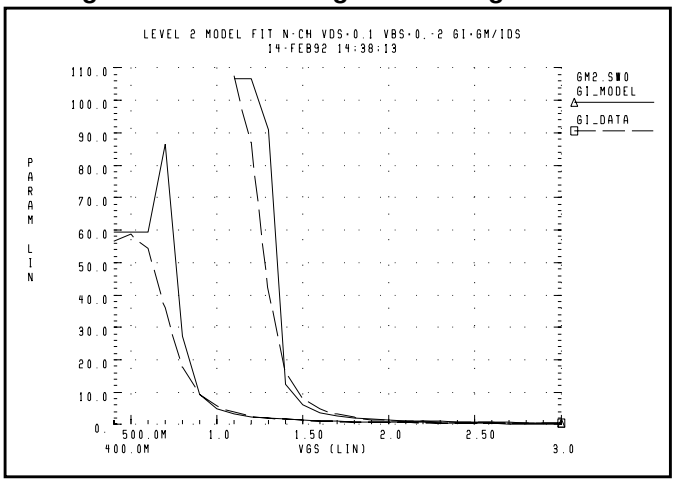


Figure 9-32: LEVEL 28 gm/Ids vs. Vgs Curves

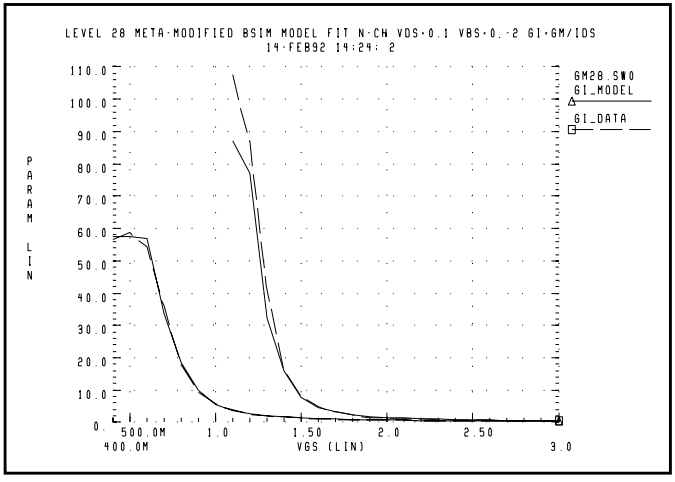
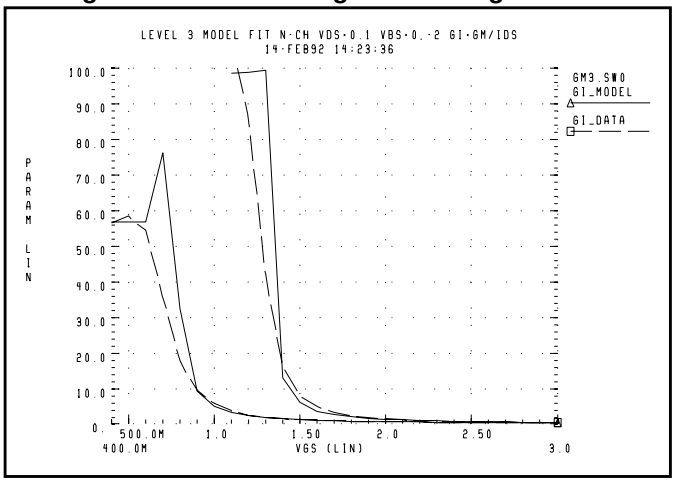


Figure 9-33: LEVEL 3 gm/Ids vs. Vgs Curves



LEVEL 13, 28, 39—Gm/Ids Model vs. Data

- gm/Ids -vs.- Vgs at Vds=0.1, Vbs =0, -2
- LEVEL 13 has a kink at Vth, which is not visible at this resolution. LEVEL 28 and 39 are monotonic.

Figure 9-34: LEVEL 13 gm/Ids vs. Vgs Curves

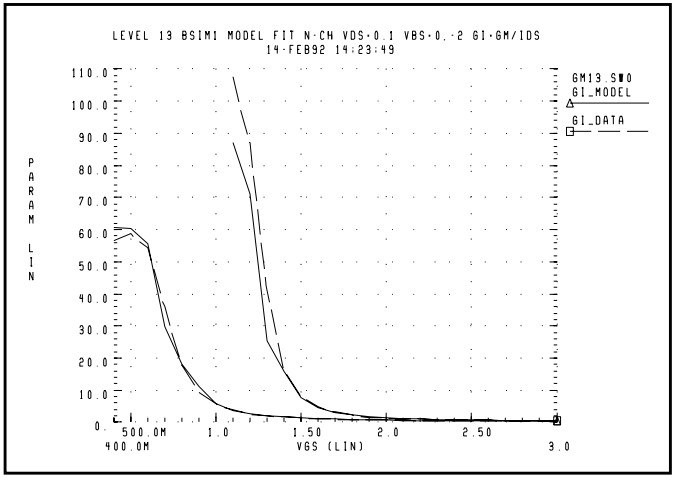


Figure 9-35: LEVEL 28 gm/Ids vs. Vgs Curves

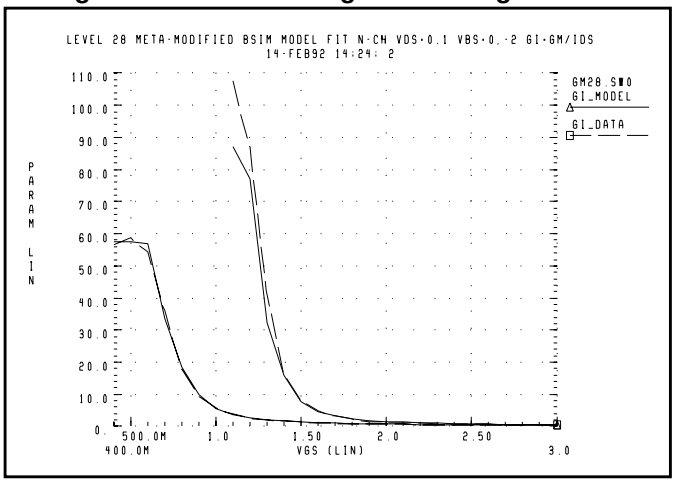
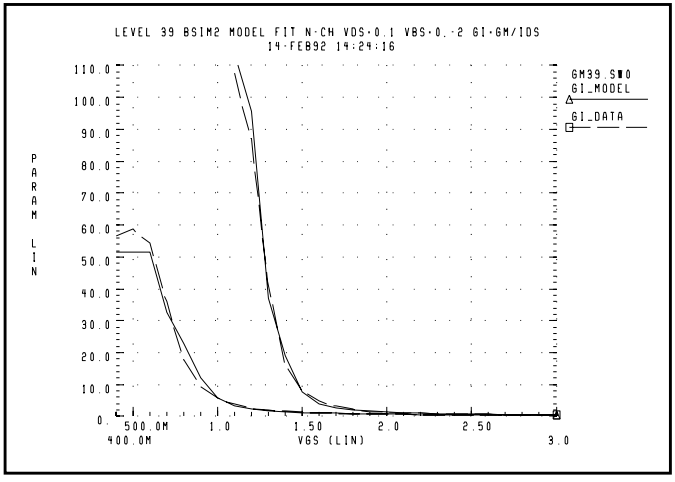


Figure 9-36: LEVEL 39 gm/Ids vs. Vgs Curves



Gds vs. Vds at Vgs=4, Vbs=0

This plot shows the behavior of gds at the linear to saturation transition. The LEVEL 3 model has a gds discontinuity.

Figure 9-37: LEVELs 2, 3, 28 gds vs. Vds Curves

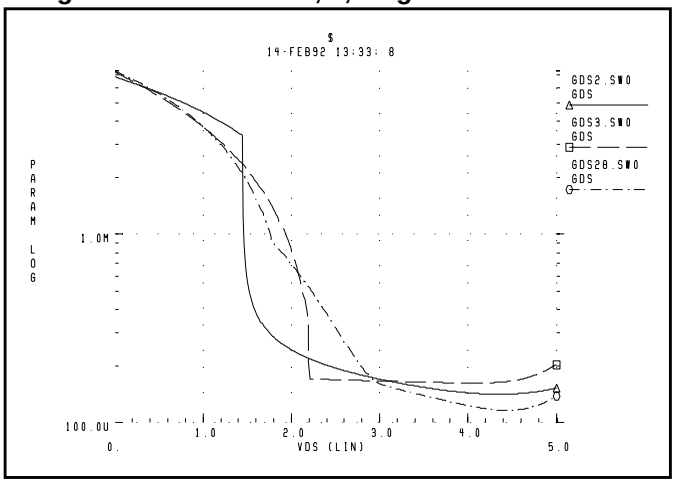
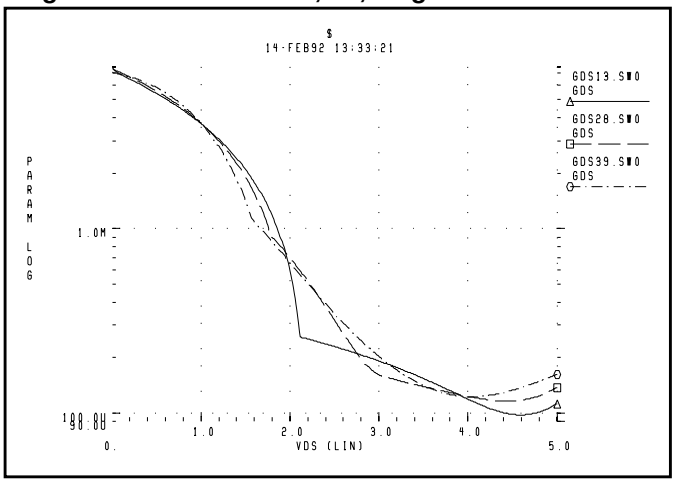


Figure 9-38: LEVELs 13, 28, 39 gds vs. Vds Curves



Gm/Ids vs. Vgs at Vds=0.1, Vbs=0, 2

This plot shows a gm discontinuity in the LEVEL 2 model, related to parameters UCRIT and UEXP.

Figure 9-39: LEVEL 2 gm/Ids vs. Vgs Curves

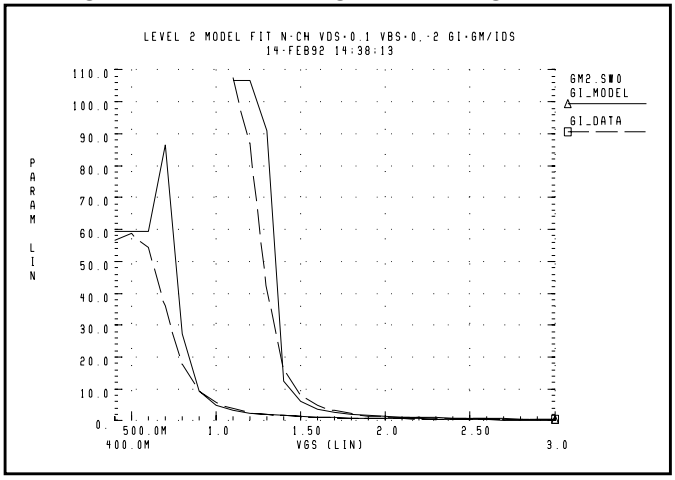
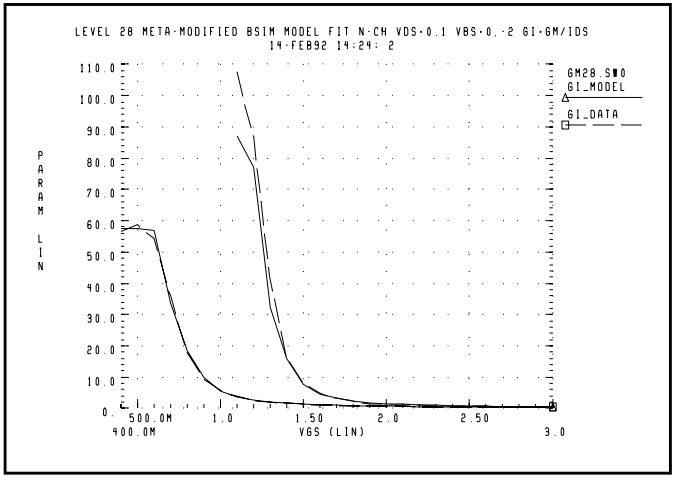


Figure 9-40: LEVEL 28 gm/Ids vs. Vgs Curves



Gm/Ids vs. Vgs at Vds=0.1, Vbs=0

This plot shows the ratio gm/Ids in the weak inversion transition region. The LEVEL 2, 3, and 13 models have kinks near threshold, while LEVELs 28 and 39 are monotonic.

Figure 9-41: LEVELs 2, 3, 28 gm/Ids vs. Vgs Curves

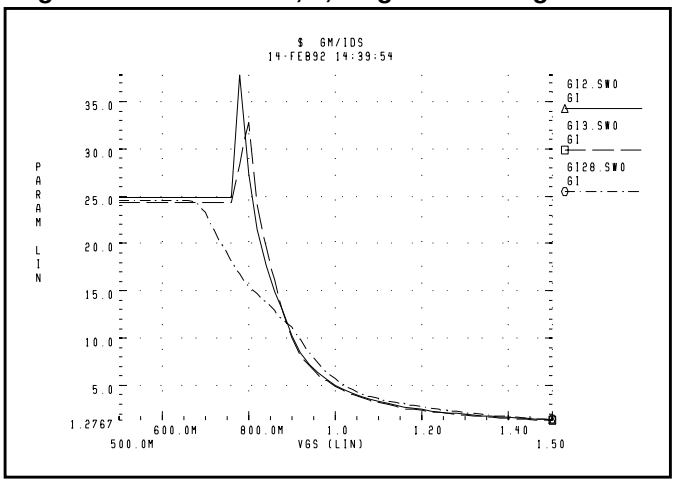
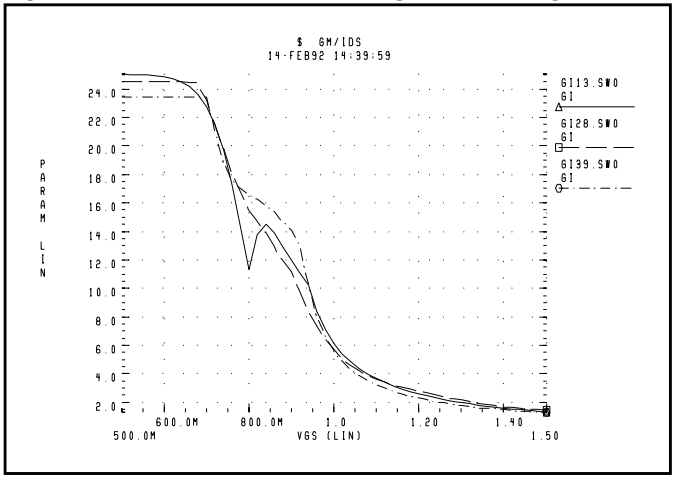


Figure 9-42: LEVELs 13, 28, 39 gm/Ids vs. Vgs Curves



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10. Duster, J.S., Jeng, M.C., Ko, P. K., and Hu, C. *User’s Guide for the BSIM2 Parameter Extraction Program and the SPICE3 with BSIM Implementation*. Industrial Liaison Program, Software Distribution Office, University of California, Berkeley, May 1990.

Avant!

Chapter 10

Selecting MOSFET Models: Level 47-63

The MOSFET models described in this chapter are the most currently developed and widely used models. Avant! True-Hspice models have introduced Levels that are compatible with models developed by Berkeley, The University of Florida, Rensselaer Polytechnic Institute, and others.

This chapter lists the various MOSFET models (Level 47 to 62), and provides the specifications for each model. The following topics are covered in this chapter:

For information about MOSFET Models Levels 1 to 40, see Chapter 9, “Selecting MOSFET Models: Level 1-40”.

Level 47 BSIM3 Version 2 MOS Model

The BSIM3 version 2.0 MOS model from UC Berkeley is available as the Avant! Level 47 model.

Level 47 Model Parameters

Name	Unit	Default	Description
VTH0	V	0.7	Threshold voltage of long channel at V_{bs} = 0 and small V_{ds} ■ 0.7 for n-channel. ■ - 0.7 for p-channel)
K1	$V^{1/2}$	0.53	First-order body effect coefficient
K2		-0.0186	Second-order body effect coefficient
K3		80.0	Narrow width effect coefficient
K3B	1/V	0	Body width coefficient of narrow width effect
KT1	V	-0.11	Temperature coefficient for threshold voltage
KT2		0.022	Body bias coefficient of threshold temperature effect
GAMMA1	$V^{1/2}$	See Level 47 Model Equations on page 10-11.	Body effect coefficient, near interface

Name	Unit	Default	Description
GAMMA2	$V^{1/2}$	See Level 47 Model Equations on page 10-11.	Body effect coefficient in the bulk
W0	m	2.5e-6	Narrow width effect coefficient
NLX	m	1.74e-7	Lateral nonuniform doping along channel
TOX	m	150e-10	Gate oxide thickness
XJ	m	0.15e-6	Junction depth
DL	m	0.0	Channel length reduction on one side (multiplied by SCALM)
DW	m	0.0	Channel width reduction on one side (multiplied by SCALM)
NPEAK	cm^{-3} (see Note 8)	1.7e17	Peak doping concentration near interface
NSUB	cm^{-3}	6.0e16	Substrate doping concentration
PHI	V	See Level 47 Model Equations on page 10-11.	Surface potential under strong inversion
XT	m	1.55e-7	Doping depth
VBM	V	-5.0	Maximum substrate bias

Name	Unit	Default	Description
VBX	V	See Level 47 Model Equations on page 10-11.	V_{bs} at which the depletion width equals *XT*
DVT0		2.2	Short-channel effect coefficient 0
DVT1		0.53	Short-channel effect coefficient 1
DVT2	1/V	-0.032	Short-channel effect coefficient 2
U0	m^2/ Vsec (Note 8)	0.067	Low field mobility at T = *TREF* ■ 0.067 for n-channel. ■ 0.025 for p-channel.
UA	m/V	2.25e-9	First-order mobility degradation coefficient
UA1	m/V	4.31e-9	Temperature coefficient of *UA*
UB	m^2/V^2	5.87e-19	Second-order mobility degradation coefficient
UB1	m^2/V^2	-7.61e-18	Temperature coefficient of *UB*
UC	1/V	0.0465	Body bias sensitivity coefficient of mobility
UC1	1/V	-0.056	Temperature coefficient of *UC*
VSAT	cm/ sec	8e6	Saturation velocity of carrier at T = *TREF*
AT	m/sec	3.3e4	Temperature coefficient of *VSAT*
RDSW	ohm · µm	0.0	Source drain resistance per unit width

Name	Unit	Default	Description
RDS0	ohm	0.0	Source drain contact resistance
LDD	m	0.0	Total length of LDD region
ETA		0.3	Coefficient of drain voltage reduction
ETA0		0.08	Subthreshold region DIBL (Drain Induced Barrier Lowering) coefficient
ETAB	1/V	-0.07	Subthreshold region DIBL coefficient
EM	V/m	4.1e7	Electrical field in channel above which hot carrier effect dominates
NFACTOR		1.0	Subthreshold region swing
VOFF	V	-0.11	Offset voltage in subthreshold region
LITL	m		Characteristic length. The default is: $$\mathrm{LITL} = \left(\frac{\varepsilon_{si} T_{ox} X_j}{\varepsilon_{ox}}\right)^{1/2}$$
VGLOW	V	-0.12	Lower bound of the weak-strong inversion transition region
VGHIGH	V	0.12	Upper bound of the weak-strong inversion transition region
CDSC	F/m^2	2.4e-4	Drain/source and channel coupling capacitance
CDSCB	F/Vm^2	0	Body coefficient for CDSC
CIT	F/m^2	0.0	Interface state capacitance
PCLM		1.3	Coefficient of channel length modulation

Name	Unit	Default	Description
PDIBL1		0.39	DIBL (Drain Induced Barrier Lowering) effect coefficient 1
PDIBL2		0.0086	DIBL effect coefficient 2
DROUT		0.56	DIBL effect coefficient 3
DSUB		DROUT	DIBL coefficient in subthreshold region
PSCBE1	V/m	4.24e8	Substrate current induced body effect exponent 1
PSCBE2	m/V	1.0e-5	Substrate current induced body effect coefficient 2
A0		1	Bulk charge effect. The default is 4.4 for PMOS.
TNOM (TREF)	°C	25	Temperature at which parameters are extracted. This parameter defaults to the option *TNOM*, which defaults to 25 °C. See 4 and 5 in “Reminders for this Installation,” below.
SUBTHMOD		2	Subthreshold model selector
SATMOD		2	Saturation model selector
KETA	1/V	-0.047	Body bias coefficient of the bulk charge effect
A1	1/V	0	First nonsaturation factor (0 for NMOS, 0.23 for PMOS)
A2		1.0	Second nonsaturation factor (1.0 for NMOS, 0.08 for PMOS)

Name	Unit	Default	Description
UTE		-1.5	Mobility temperature exponent
KT1L	Vm	0	Channel length sensitivity of temperature coefficient for threshold voltage
UC0*	$(V/m)^2$		Temperature coefficient
BULKMOD		1	Bulk charge model selector
XPART		1	Charge partitioning flag
VFB	V		Flat-band voltage
PVAG		0	Gate dependence of output resistance
* UC0 has no effect on the model			

Using the BSIM3 Version 2 MOS Model

The Level 47 model uses the same model parameters for source/drain diode current, capacitance, and resistance as do the other supported MOS levels. The model parameter ACM controls the choice of source/drain equations.

The Level 47 model also uses the same noise equations as the other levels. The parameter NLEV controls the choice of noise equations.

This model, like all Avant! simulation device models, can include parameters. This is useful for modeling process skew, either by worst-case corners or by Monte Carlo. For information on worst-case and Monte Carlo analysis, see “Performing Worst Case Analysis” and “Performing Monte Carlo Analysis” in Chapter 13 of the *Star-Hspice Manual*.

Notes:

1. Set Level=47 to identify the model as a BSIM3 model.
2. This model is based on BSIM3 version 2.0 from UC Berkeley. Code was received from UC Berkeley in July 1994, in the form of SPICE3e2. Changes announced in a letter from UCB September 13, 1994, have been included. DC sweeps have been checked against SPICE3e2.
3. The default setting for *CAPOP* is CAPOP=13, which is the BSIM1 charge-conserving capacitance model. The BSIM3 capacitance model has not been installed.
4. The Level 47 model supports the model parameter name *TNOM* as an alias for *TREF*. The conventional terminology is *TREF*, which is supported as a model parameter in all Avant! MOS levels. The alternative name *TNOM* is supported for Level 47, for compatibility with SPICE3.
5. The default room temperature is 25°C in this model, but is 27°C in SPICE3. If the BSIM3 model parameters are specified at 27°C, TREF=27 should be added to the model, so that the model parameters is interpreted correctly. It is a matter of choice whether or not to set the nominal simulation temperature to 27, by adding .OPTION TNOM=27 to the netlist. This should be done when testing the Avant! model versus SPICE3.
6. The default of *DERIV* is zero, the analytical method. You can set *DERIV* to 1 for the finite difference method. Analytic derivatives in the SPICE3e2 code are not exact in some regions. Setting DERIV=1 gives more accurate derivatives (*GM*, *GDS*, *GMBS*), but consumes more CPU time.
7. There are three ways for the BSIM3 model to calculate V_{th}:
   - Using *K1* and *K2* values that are user specified
   - Using *GAMMA1*, *GAMMA2*, *VBM*, and *VBX* values entered in the .MODEL statement
   - Using *NPEAK*, *NSUB*, *XT*, and *VBM* values that are user specified
8. You can enter the *NPEAK* and *U0* model parameters in meters or centimeters. *NPEAK* is converted to cm^{-3} as follows: if *NPEAK* is greater than 1e20, it is multiplied by 1e-6. *U0* is converted to $m^2/Vsec$ as follows: if *U0* is greater than 1, it is multiplied by 1e-4. You must enter the parameter *NSUB* in cm^{-3} units.

9. The specified value of *VTH0* for p-channel in the .MODEL statement should be negative.
10. The default value of *KT1* is -0.11. The negative sign ensures that the absolute value of threshold decreases with increasing temperature for NMOS and PMOS.
11. Model parameter *LITL* is not allowed to go below a minimum value of 1.0e-9 m, to avoid a possible divide by zero error.
12. *VSAT*, after temperature adjustment, is not allowed to go below a minimum value of 1.0e4 m/sec, to assure that it is positive after temperature compensation.
13. There are seven model parameters for accommodating the temperature dependencies of six temperature dependent model variables. They are *KT1* and *KT2* for *VTH*, *UTE* for *U0*, *AT* for *VSAT*, *UA1* for *UA*, *UB1* for *UB*, and *UC1* for *UC*.
14. Set up the conversion of temperature between this model and SPICE3 as follows:

```
SPICE3:.OPTIONS TEMP=125
            .MODEL NCH NMOS Level=8
            + TNOM =27 ...
HSPICE:.TEMP 125
            .MODEL NCH NMOS Level=47
            + TREF =27 ...
```

15. The option SCALM does not affect the parameters unique to this model, but it does affect the common MOS parameters, such as *XL*, *LD*, *XW*, *WD*, *CJ*, *CJSW*, *JS*, and *JSW*.
16. Level 47 uses the common Avant! MOS parasitic models, specified by ACM.
17. Level 47 uses the common Avant! MOS noise models, specified by NLEV.
18. *DELVTO* and *DTEMP* on the element line can be used with Level 47.
19. The impact ionization current determined by the model parameters PSCBE1 and PSCBE2 contributes to the drain-source current; it does not contribute to bulk current.

Leff and Weff Equations for BSIM3 Version 2.0

The standard equations for Leff and Weff in the Avant! model are:

$$L_{eff} = L + XL - (2 \cdot LD)$$

$$W_{eff} = W + XW - (2 \cdot WD)$$

The UCB SPICE3 equations used for BSIM3 are:

$$L_{eff} = L - (2 \cdot DL)$$

$$W_{eff} = W - (2 \cdot DW)$$

The units for these parameters are meters, with defaults of zero.

Simulation uses the standard Avant! model equation for both cases, and accepting DL(DW) as the value for LD(WD). If both LD(WD) and DL(DW) are specified in a .MODEL statement, simulation uses the LD(WD) value.

If LDAC and WDAC are included in the .MODEL statement,

$$Leff = L+XL-2 \cdot LDAC, \quad Weff = W+XW-2 \cdot WDAC$$

The model uses the values of LD(DL) and WD(DW) to generate defaults for CGSO, CGDO, and CGBO. The values are also used with parameters RS and RD for ACM>0.

Example

The following two models give the same simulation results:

```
* HSPICE style:
.MODEL n1 nmos Level=47 XL=0.1e6 LD=0.15e-6
+ SatMod=2 SubthMod=2 BulkMod=1
+ CGSO=0.3e-9 CGDO=0.3e-9 CGBO=0
* SPICE3 style:
.MODEL n2 nmos Level=47 LD=0.1e-6
+ SatMod=2 SubthMod=2 BulkMod=1
+ CGSO=0.3e-9 CGDO=0.3e-9 CGBO=0
```

Level 47 Model Equations

The following model equations are based on the source code of BSIM3.

Threshold Voltage

Model Parameters

V_{th0}, K1, K2, ϕ_s, N_{lx}, K3, W_0, T_{ox}, V_{bi}, D_{vt0}, D_{vt1}, D_{vt2}, N_{peak}, N_{sub}, Υ_1, Υ_2, V_{bx}, V_{bm}, V_{bi}, X_t, TREF

$$V_{th} = V_{th0} + K1(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s}) - K2V_{bs} + K1\left(\sqrt{1 + \frac{N_{lx}}{L_{eff}}\sqrt{\frac{\phi_s}{\phi_s - V_{bs}}}} - 1\right)\sqrt{\phi_s}$$

$$+ \quad (K3 + K3B \cdot V_{bs}) \cdot \left(\frac{T_{ox}}{W_{eff} + W_0}\right)\phi_s - \Delta V_{th}$$

$$T_{ratio} = \frac{(TEMP + DTEMP + 273.15)}{(TREF + 273.15)}$$

$$\Delta V_{th} = \theta_{th}(L_{eff}) \cdot (V_{bi} - \phi_s)$$

$$\theta_{th}(L_{eff}) = D_{vt0} \cdot \left[exp\left(\frac{-D_{vt1} \cdot L_{eff}}{2l_t}\right) + 2\,exp\left(\frac{-D_{vt1} \cdot L_{eff}}{l_t}\right)\right]$$

$$l_t = \sqrt{3 \cdot T_{ox} \cdot X_{dep}} \cdot (1 + D_{vt2} \cdot V_{bs})$$

$$X_{dep} = \sqrt{\frac{2 \cdot \varepsilon_{si} \cdot (\phi_s - V_{bs})}{q \cdot N_{peak}}}$$

If Phi_s is not specified as a model parameter, then

$$\phi_s = 2 \cdot V_{tm} \cdot \ln\left(\frac{N_{peak}}{n_i}\right) \qquad (N_{peak} \text{ and } n_i \text{ in } cm^{-3})$$

$$V_{tm} = K \cdot T/q$$

$$n_i = 1.45e10 \cdot \left(\frac{T}{300.15}\right)^{1.5} \cdot exp(21.5565981 - Eg/(2 \cdot V_{tm}))$$

$$Eg = 1.16 - (7.02e-4) \cdot T^2/(T + 1108.0)$$

If you do not specify *K1*, *K2* as model parameters, they are calculated as follows:

$$K_1 = \Upsilon_2 - 2 \cdot K_2 \cdot \sqrt{\phi_s - V_{bm}}$$

$$K_2 = (\Upsilon_1 - \Upsilon_2) \cdot \frac{\sqrt{\phi_s - V_{bx}} - \sqrt{\phi_s}}{2 \cdot \sqrt{\phi_s} \cdot (\sqrt{\phi_s - V_{bm}} - \sqrt{\phi_s}) + V_{bm}}$$

$$\Upsilon_1 = \frac{\sqrt{2 \cdot q \cdot \varepsilon_{si} \cdot N_{peak}}}{C_{ox}}$$

$$\Upsilon_2 = \frac{\sqrt{2 \cdot q \cdot \varepsilon_{si} \cdot N_{sub}}}{C_{ox}}$$

$$V_{bx} = \phi_s - \left(\frac{q \cdot N_{peak} \cdot X_t^2}{2 \cdot \varepsilon_{si}}\right)$$

If V_{bi} is not specified as a model parameter, then

$$V_{bi} = \frac{k \cdot T}{q} \cdot \ln\left(\frac{1.0e22 \cdot N_{peak}}{n_i^2}\right)$$

Mobility of Carrier

Model Parameters

$$\mu_0,\ U_a,\ U_b,\ U_c$$

$$\mu_{eff} = \frac{\mu_0}{1 + U_a \cdot \left(\frac{V_{gs} + V_{th}}{T_{ox}}\right) + U_b \cdot \left(\frac{V_{gs} + V_{th}}{T_{ox}}\right)^2 + U_c \cdot V_{bs}}$$

Drain Saturation Voltage

Model Parameters

$$A_0,\ v_{sat},\ X_j,\ A_1,\ A_2,\ R_{ds0},\ R_{dsw}$$

Rds and Pfactor:

$$R_{ds} = R_{ds0} + R_{dsw} / (1e6 \cdot W_{eff})$$

$$Pfactor = A_1 \cdot V_{gst} + A_2 \qquad \text{(if Pfactor >1, it is set to Pfactor = 1)}$$

$$V_{gst} = V_{gs} - V_{th}$$

Vdsat for the case Rds = 0 and Pfactor = 1:

$$V_{dsat} = \frac{E_{sat} \cdot L_{eff} \cdot V_{gst}}{A_{bulk} \cdot E_{sat} \cdot L_{eff} + V_{gst}}$$

For BULKMOD = 1,

$$A_{bulk} = \left(1 + \frac{K1 \cdot A_0 \cdot L_{eff}}{(L_{eff} + T1) \cdot T1s \cdot 2}\right) / (1 + KETA \cdot V_{bs})$$

For BULKMOD = 2,

$$A_{bulk} = \left(\frac{K1 \cdot A_0 \cdot L_{eff}}{(L_{eff} + T1) \cdot \sqrt{\phi_s} \cdot 2}\right) / (1 + KETA \cdot V_{bs})$$

$$T1 = 2 \cdot \sqrt{X_j \cdot X_{dep}}$$

For $V_{bs} \le 0$,

$$T1s = \sqrt{\phi_s - V_{bs}}$$

For $V_{bs} \ge 0$,

$$T1s = \frac{\phi_s \cdot \sqrt{\phi_s}}{\phi_s + \frac{V_{bs}}{2}}$$

$$E_{sat} = 2 \cdot \frac{v_{sat}}{\mu_{eff}}$$

Vdsat for the general case:

V_{dsat} is the solution of Tmpa * V_{dsat} * V_{dsat} - Tmpb * V_{dsat} + Tmpc = 0

$$V_{dsat} = \left(Tmpb - \sqrt{Tmpb^2 - 4 \cdot Tmpa \cdot Tmpc}\right) / (2 \cdot Tmpa)$$

$$Tmpa = A_{bulk} \cdot (A_{bulk} \cdot W_{eff} \cdot v_{sat} \cdot C_{ox} \cdot R_{ds} - 1 + 1/Pfactor)$$

$$Tmpb = V_{gst} \cdot (2/Pfactor - 1) + (A_{bulk} \cdot E_{sat} \cdot L_{eff}) + (3 \cdot A_{bulk} \cdot V_{gst} \cdot W_{eff} \cdot v_{sat} \cdot C_{ox} \cdot R_{ds})$$

$$Tmpc = (V_{gst} \cdot E_{sat} \cdot L_{eff}) + (V_{gst}^2 \cdot 2 \cdot W_{eff} \cdot v_{sat} \cdot C_{ox} \cdot R_{ds})$$

Linear Region

$$I_{dslin0} = \mu_{eff} \cdot C_{ox} \cdot \frac{W_{eff}}{L_{eff}} \cdot \frac{1}{1 + V_{ds}/(E_{sat} \cdot L)} \cdot \left(V_{gs} - V_{th} - A_{bulk} \cdot \frac{V_{ds}}{2}\right) \cdot V_{ds}$$

$$I_{ds} = \frac{I_{dslin0}}{1 + \frac{R_{ds} \cdot I_{dslin0}}{V_{ds}}}$$

Saturation Region

Model Parameters

litl, eta, L_{dd}, E_m, D_{rout}, P_{clm}, P_{dibl1}, P_{dibl2}, P_{scbe1}, P_{scbe2}

Vasat and Fvag:

$$V_{asat} = \frac{E_{sat} \cdot L_{eff} + V_{dsat} + 2R_{ds} \cdot v_{sat} \cdot C_{ox} \cdot W_{eff} \cdot \left(V_{gst} - \frac{A_{bulk} \cdot V_{dsat}}{2}\right)}{2/Pfactor - 1 + R_{ds} \cdot v_{sat} \cdot C_{ox} \cdot W_{eff} \cdot A_{bulk}}$$

$$F_{vag} = 1 + \frac{P_{vag} \cdot V_{gst}}{E_{sat} \cdot L_{eff}}$$

Early Voltage, satMod = 1:

$$V_A = V_{asat} + F_{vag} \cdot \left(\frac{1 + eta \cdot \frac{L_{dd}}{litl}}{P_{clm} \cdot A_{bulk}} \right) \cdot \left(\frac{(A_{bulk} \cdot E_{sat} \cdot L_{eff} + V_{gst} - \lambda \cdot (V_{ds} - V_{dsat})) \cdot (V_{ds} - V_{dsat})}{E_{sat} \cdot litl} \right)$$

$$\lambda = \frac{A_{bulk} \cdot E_{sat} \cdot L_{eff} + (V_{gst})}{2 \cdot litl \cdot E_m}$$

Early Voltage, satMod = 2:

$$V_A = V_{asat} + F_{vag} \cdot U_{vds} \cdot \left(\frac{1}{V_{aclm}} + \frac{1}{V_{adibl}} \right)^{-1}$$

$$U_{vds} = 1 + eta \cdot \frac{L_{dd}}{litl}$$

$$V_{aclm} = \frac{1}{P_{clm}} \cdot \frac{A_{bulk} \cdot E_{sat} \cdot L_{eff} + V_{gst}}{A_{bulk} \cdot E_{sat} \cdot litl} \cdot (V_{ds} - V_{dsat})$$

$$V_{adibl} = \frac{1}{\theta_{rout}} \cdot \left[(V_{gs} - V_{th}) - \left(\frac{1}{A_{bulk} \cdot V_{dsat}} + \frac{1}{V_{gst}} \right)^{-1} \right]$$

$$\theta_{rout} = P_{dibl1} \cdot \left[exp\left(\frac{-D_{rout} \cdot L_{eff}}{2 \cdot l_t} \right) + 2\, exp\left(\frac{-D_{rout} \cdot L_{eff}}{l_t} \right) \right] + P_{dibl2}$$

$$V_{ahce} = \left[\frac{P_{scbe2}}{L_{eff}} \cdot exp\left(\frac{-P_{scbe1} \cdot litl}{V_{ds} - V_{dsat}} \right) \right]^{-1}$$

Drain Current

$$I_{dsat} = W_{eff} \cdot v_{sat} \cdot C_{ox} \cdot (V_{gs} - V_{th} - A_{bulk} \cdot V_{dsat}) \cdot Pfactor$$

$$Pfactor = A_1 \cdot V_{gst} + A_2$$

$$I_{ds} = I_{dsat} \cdot \left(1 + \frac{V_{ds} - V_{dsat}}{V_A}\right) \cdot \left(1 + \frac{V_{ds} - V_{dsat}}{V_{ahce}}\right)$$

Subthreshold Region

Model Parameters

$$Nfactor,\ C_{dsc},\ C_{dscb},\ V_{off},\ C_{it},\ D_{sub},\ eta_0,\ eta_b$$

n and DIBL:

$$n = 1 + \frac{Nfactor \cdot 1.034e{-}10}{X_{dep} \cdot C_{ox}} + \frac{(C_{dsc} + C_{dscb} \cdot V_{bs}) \cdot \left[exp\left(\frac{-L_{eff}}{2 \cdot l_t}\right) + 2\,exp\left(\frac{-L_{eff}}{l_t}\right)\right] + C_{it}}{C_{ox}}$$

$$DIBL = (eta_0 + eta_b \cdot V_{bs}) \cdot \left[exp\left(\frac{-D_{sub} \cdot L_{eff}}{2 \cdot l_{t0}}\right) + 2\,exp\left(\frac{-D_{sub} \cdot L_{eff}}{l_{t0}}\right)\right]$$

$$l_{t0} = \sqrt{3 \cdot T_{ox} \cdot X_{dep0}}$$

$$X_{dep0} = \sqrt{\frac{2 \cdot \varepsilon_{si} \cdot \phi_s}{q \cdot N_{peak}}}$$

If subthMod = 0,

$$I_{ds} = g_m = g_{ds} = g_{mb} = 0$$

If subthMod = 1,

$$I_{ds} = \frac{I_{limit} \cdot I_{exp}}{I_{limit} + I_{exp}} \cdot \left[1 - exp\left(\frac{-V_{ds}}{V_{tm}}\right)\right]$$

$$I_{limit} = \frac{9}{2} \cdot u0 \cdot \sqrt{\frac{q\varepsilon_{si} \cdot N_{peak}}{2 \cdot \phi_s}} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_{tm}^2$$

$$I_{exp} = u0 \cdot \sqrt{\frac{q \cdot \varepsilon_{si} \cdot N_{peak}}{2 \cdot \phi_s}} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_{tm}^2 \cdot exp\left(\frac{V_{gs} - V_{th} - V_{off} + DIBL \cdot V_{ds}}{n \cdot V_{tm}}\right)$$

If subthMod = 2,

$$I_{ds} = u0 \cdot \sqrt{\frac{q \cdot \varepsilon_{si} \cdot N_{peak}}{2 \cdot \phi_s}} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_{tm}^2 \cdot \left[1 - exp\left(\frac{-V_{ds}}{V_{tm}}\right)\right] \cdot exp\left(\frac{V_{gs} - V_{th} - V_{off} + DIBL \cdot V_{ds}}{n \cdot V_{tm}}\right)$$

Transition Region (for subthMod = 2 only)

Model Parameters

$$V_{gshigh},\ V_{gslow}$$

$$I_{ds} = (1-t)^2 \cdot I_{dslow} + 2 \cdot (1-t) \cdot t \cdot I_p + t^2 \cdot I_{dshigh}$$

$$t = \left(\frac{V_p - V_{gslow}}{V_{gslow} - 2 \cdot V_p + V_{gshigh}}\right) \cdot \left(\sqrt{1 + \frac{(V_{gslow} - 2 \cdot V_p + V_{gshigh})(V_{gs} - V_{th} - V_{gslow})}{(V_p - V_{gslow})^2}} - 1\right)$$

$$V_p = \frac{(g_{mhigh} \cdot V_{gshigh} - g_{mlow} \cdot V_{gslow}) - (I_{dshigh} - I_{dslow})}{g_{mhigh} - g_{mlow}}$$

$$I_p = I_{dslow} + g_{mlow} \cdot (V_p - V_{gslow})$$

Temperature Compensation

Model Parameters

$$A_t,\ U_{a1},\ U_{b1},\ U_{c1},\ KT1,\ KT2,\ UTE$$

$$V_{th}(temp) = V_{th}(tref) + (KT1 + KT2 \cdot V_{bs}) \cdot (T_{ratio} - 1)$$

$$u0(temp) = u0(tref) \cdot (T_{ratio})^{UTE}$$

$$V_{sat}(temp) = V_{sat}(tref) - A_t \cdot (T_{ratio} - 1)$$

$$U_a(temp) = U_a(tref) + U_{a1} \cdot (T_{ratio} - 1)$$

$$U_b(temp) = U_b(tref) + U_{b1} \cdot (T_{ratio} - 1)$$

$$U_c(temp) = U_c(tref) + U_{c1} \cdot (T_{ratio} - 1)$$

PMOS Model

The following is an example of a PMOS model. Note that VTH0 is negative.

```
.model pch PMOS Level=47
+ Tnom=27.0
+ Npeak= 1.5E+23 Tox=7.0E-09 Xj=1.0E-07
+ dl= 0.2E-06 dw=-0.1E-06
+ SatMod= 2 SubthMod= 2 BulkMod= 1
+ Vth0= -.8 Phi= .7 K1= .5 K2=0.03 K3= 0
+ Dvt0= 48 Dvt1= .6 Dvt2=-5e-4
+ Nlx=0 W0= 0
+ Vsat= 9E6 Ua= 1E-09 Ub= 0 Uc= -3E-02
+ Rds0= 180 Rdsw= 0 U0= 7E-03
+ A0= .87
+ Voff=-.07 NFactor= 1.5 Cit=-3E-05
+ Cdsc= 6E-02 Vglow=-.12 Vghigh= .12
+ Pclm= 77 Pdibl1= 0 Pdibl2= 2E-011
+ Drout= 0 Pscbe1= 0 Pscbe2= 1E-28
+ Eta= 0 Litl= 4.5E-08
+ Em= 0 Ldd= 0
+ kt1=-.3 kt2=-.03
+ At= 33000
+ Ua1= 4E-09 Ub1= 7E-18 Uc1= 0
```

Levels 49 and 53 BSIM3v3 MOS Models

The BSIM3v3 MOS model from UC Berkeley is available as Avant! Level 49 and Level 53 models. Level 49 is an Hspice-enhanced version of BSIM3v3 while Level 53 maintains full compliance with the Berkeley release. This compliance includes numerically identical model equations, identical parameter default values, and identical parameter range limits. Level 49 maintains compliance with the UC Berkeley release of BSIM3v3 with the following three exceptions:

1. *Default parameter values.* Eliminate differences in default parameter values by explicit assignment of the parameters CAPMOD, XPART and by setting ACM=10.
2. *Parameter range limits.* Provides parameter range limits that are identical to that of the Berkeley release. Differences occur only in the severity of warning for five parameters. Level 49 issues a warning that the parameter range has been exceeded but continues with simulation, whereas, in the Berkeley release, a fatal error is issued and simulation is aborted. These five parameters include NGATE, DVT1W, DVT1, DSUB, DROUT. (See Parameter Range Limits on page 10-50 for more details.)
3. *Improvements in numerical stability.* Provides improvements in numerical stability. In most practical situations, these improvements will not affect compliance with the Berkeley release, but will improve convergence and simulation time.

Both Levels 49 and 53 support a superset of model parameters that include Hspice-specific parameters. For Level 53, in all cases, Hspice-specific parameters default to OFF. The single exception in Level 49 is that ACM defaults to 0. Level 49 compliance with Berkeley BSIM3v3 can be achieved by setting ACM=10.

Selecting Model Versions

Recommended BSIM3v3 Version

As of the 2001.4 release (November 2001), the recommended BSIM3v3 model specification is Level=49, VERSION=3.23. This version provides the most stable and up-to-date representation of the UCB BSIM3v3.2.2 model. However, do not change the VERSION specification in existing model cards without consulting the foundry or model extraction group that created the model cards.

There are, as of the 99.2 release, five official BSIM3v3 releases from Berkeley and several Level 49 releases. (See the BSIM3 home page at http://www-device.EECS.Berkeley.EDU/~bsim3/ for additional release information from the UCB group.) To minimize confusion and maintain back compatibility, you can select the model parameters VERSION and HSPVER. VERSION selects the Berkeley release version and HSPVER selects the release version. For example, HSPVER=97.2 and VERSION=3.1 reproduce results from Hspice 97.2 using the BSIM3 Version 3.1 model.

HSPVER defaults to the current release being executed. The model parameter, VERSION, selects among the various Berkeley releases of BSIM3v3 as follows:

- ***Version 3.0 Berkeley release (October 30, 1995) default for HSPICE96.1,96.2,96.3***. This version is invoked when VERSION=3.0 and HSPVER= 98.0 are specified. To invoke the Avant! model version that most accurately represents the Berkeley release of October 1995, specify the parameters VERSION=3.0 and HSPVER=98.0
- ***Version 3.1 Berkeley (December 9, 1997) default for HSPICE97.1,97.2. 97.4***. This version is invoked when VERSION=3.1 or 3.11 and HSPVER= 98.0 are specified. To invoke the Avant! model version that most accurately represents the Berkeley release of December, 1996 specify the parameters VERSION=3.1 or 3.11 and HSPVER = 98.0.
- ***Berkeley Version 3.0, 3.1 bug fixes.*** Berkeley corrected several Version 3.0 and 3.1 bugs in the June, 1998 release. These bug fixes are incorporated into Hspice98.2 and are represented when VERSION=3.0 and VERSION=3.1 are specified respectively with HSPVER=98.2. As a result of bug fixes, some differences between Version 3.0/3.1 in Hspice98.2 and previous Version 3.0/3.1 releases are expected. Notably, differences occur when perimeter factors PD,PS less than Weff are specified (PD,PS < Weff are no longer clamped to Weff in Version 3.1) and when DLC and LINT are not identical (LeffCV calculation bug in Versions3.0, 3.1).

You can find a complete list of bug fixes at the BSIM3 web site:

http://www-device.eecs.berkeley.edu/~bsim3

Note: Version 3.11 was introduced in Hspice97.4. This version represented Berkeley Version 3.1 (Dec., 1996) with Hspice bug fixes. Back compatibility will be maintained for this model. Starting with Hspice98.2, Version 3.1 and 3.11 will be identical and represent Version 3.1 with Berkeley June, 1998 bug fixes.

- ***Version 3.2 Berkeley release (June 16, 1998)***. This version is invoked when VERSION=3.2 and HSPVER=98.2 are specified.
- ***Version 3.2.1 Berkeley release (April 20, 1999)***. This version is invoked when VERSION=3.21 and HSPVER=99.2 are specified.
- ***Version 3.2.2 Berkeley release (April 20, 1999)***. This version is invoked when VERSION=3.22 and HSPVER=99.2 are specified.
- For the latest HSPICE improvements, use VERSION=3.23 and HSPVER=01.4.

Note: Versions 3.2.1 and 3.2.2 are identical except BSIM3v3.2.1 uses a bias-dependent Vfb and BSIM3v3.2.2 uses a bias-independent Vfb for the capacitance models capMod = 1 and 2. Version 3.23 provides various model fixes compared to Version 3.22.

The table below summarizes the parameter settings required to match Berkeley releases:

Berkeley Release	VERSION	HSPVER
Version 3.0 (October 1995)	3.0	98.0
Version 3.0 with June 1998 bug fixes	3.0	98.2
Version 3.1 (December 1996)	3.1	98.0
Version 3.1 with June 1998 bug fixes	3.1	98.2
Version 3.2 (June 16,1998)	3.2	98.2

Berkeley Release	VERSION	HSPVER
Version 3.2.1 (April 20, 1999)	3.21	99.2
Version 3.2.2 (April 20, 1999)	3.22 3.23	99.2 01.4

Version 3.2 Features

In June, 1998 Berkeley released BSIM3 Version 3.2, which contains many new features. These features are summarized below.

- A new intrinsic capacitance model, CAPMOD=3, includes finite charge layer thickness effects; CAPMOD now defaults to 3 (new parameters: CAPMOD=3, ACDE, MOIN)
- Improved modeling of C-V characteristics at the weak-to-strong inversion transition (new parameters: NOFF, VOFFCV)
- Vth dependence on Tox (new parameter: TOXM)
- Flatband voltage parameter more accurately models different gate materials (new parameter: VFB)
- Improved substrate current scaleability with channel length, (new parameter: APLHA1)
- Restructured nonquasi-static (NQS) model includes pole-zero analysis and bug fixes. Note that NQSMOD is now a BSIM3 element parameter. Hspice supports only the model parameter, not the element parameter.
- Junction diode model temperature dependence, (new parameters: TCJ, TCJSW, TCJSWG, TPB, TPBSW, TPBSWG)
- Adjustable current limiting in the junction diode current model (new parameter: IJTH)
- Option of using C-V inversion charge equations of CAPMOD=0,1,2,3 to calculate the thermal noise when NOIMOD=2 or 4
- Elimination of small negative capacitance values (Cgs, Cgd) in the accumulation-depletion regions
- A separate set of length/width dependence parameters for the CV model (New parameters: LLC, LWC, LWLC, WLC, WWC, WWLC)
- Additional parameter checking
- Bug fixes

Note: If all new Version 3.2 parameters are defaulted, Version 3.2 and Version 3.1 (with June, 1998 bug fixes) will give identical DC results. However, transient and AC results will differ, in general. This discrepancy arises only from differences in flatband voltage calculations used in the intrinsic charge/capacitance models. These differences occur in all CAPMOD models 1-3.

- HSPVER < 98.0 is reset to 98.0 for Level 53.
- HSPVER < 98.2 will be reset to 98.2 when VERSION >=3.2 for Levels 49 and 53.
- Version 3.0, 3.1, and 3.11 in Hspice do not support NQSMOD and CAPMOD=3. These are supported only by Version 3.2.

You can obtain additional information about the Berkeley releases from the BSIM3 web site:

http://www-device.eecs.berkeley.edu/~bsim3

Nonquasi-Static (NQS) Model

The Berkeley NonQuasi-Static (NQS) model is also available (as of the 98.2 release) for Levels 49 and 53. This model provides a first-order correction to the quasi-static charge models. See *M.Chan, K.- Y. Hui, C. Hu, and P.-K. Ko, IEEE Trans. Electron Devices, vol. ED-45, pp.834-841, 1998*. The Avant! True--Hspice model supports only the model parameter implementation.

To invoke the NQS model, specify the parameter NQSMOD=1 in the model card. NQSMOD can be used with any of the CAPMOD Levels (0-3) but is restricted to use with Version 3.2. NQS is not supported in Version 3.0 and 3.1. In future releases, the NQS will be supported in Versions 3.0, 3.1.

Enhancements

Hspice Junction Diode Model and Area Calculation Method (ACM)

There are two junction diode models that can be used with both Levels 49 and 53: the Hspice junction model and the Berkeley junction model. The Hspice

junction model is invoked by specifying the model parameter value ACM=0,1,2, or 3. The Berkeley junction model is invoked by specifying ACM=10,11,12, or 13. The default ACM value is 0 and 10 for Levels 49 and 53 respectively. The junction current, junction capacitance, and parasitic resistance equations corresponding to ACM=0,1,2,3 can be found in ‘Selecting MOSFET Diode Models” on page 8-27.

The effect of setting ACM=10,11,12, or 13 is to enable the Berkeley junction diodes and to add parasitic resistors to the MOSFET. The parasitic resistor equations for ACM=10-13 correspond to the ACM=0-3 parasitic resistor equations respectively. ACM=10-13 all use the Berkeley junction capacitance model equations:

```
   (Bulk-source capacitance)
if (Ps >Weff)
   Cbs = AS * Cjbs + (PS - Weff) * Cjbssw + Weff *
   Cjbsswg
else
   Cbs = AS * Cjbs + PS * Cjbsswg
```

Area and perimeter factors AS, PS default to 0 if not specified on the element line.

```
if (Vbs < 0)
   Cjbs = Cj * (1 - (Vbs/Pb))^-Mj
   Cjbssw = Cjsw * (1 - (Vbs/Pbsw))^-Mjsw
   Cjbsswg = Cjswg * (1 - (Vbs/Pbswg))^-Mjswg
else
   Cjbs = Cj * (1 + Mj * (Vbs/Pb))
   Cjbssw = Cjsw * (1 + Mjsw * (Vbs/Pbsw))
   Cjbsswg = Cjswg * (1 + Mjswg * (Vbs/Pbswg))
```

Bulk-drain equations are analogous. The Hspice equations for AS,PS,AD,PD are not used with ACM=10,11,12,13 and, in accordance with the BSIM3v3 model, the default values for these area and perimeter factors are zero. However, you can invoke the Hspice calculations for AS,PS,AD,PD by specifying the model parameter CALCACM=1.

Note: CALCACM is invoked only when used with ACM=12.The calculations used in ACM=10, 11, 13 are not consistent with the Berkeley diode calculations.

With CALCACM = 1 and ACM = 12 the following area and perimeter calculations are invoked:

if AD is not specified on the element line:

```
AD = 2 * HDIFeff * Weff
```

else:

```
AD = AD * WMLT^2
```

if AS is not specified on the element line:

```
AS = 2 * HDIFeff * Weff
```

else:

```
AS = AS * WMLT^2
```

if PS is not specified on the element line:

```
PS = 4 * HDIFeff + 2 * Weff
```

else:

```
PS = PS * WMLT
```

if PD is not specified on the element line:

```
PD = 4 * HDIFeff + 2 * Weff
```

else:

```
PD = PD * WMLT
```

Note: Weff is not the same Weff used in the BSIM3v3, and Levels 49 and 53 I-V, C-V model equations!

In the preceding equations the following simple form is used.

```
Weff = W * WMLT + XW
```

where:

```
HDIFeff = HDIF * WMLT
```

W	is the width specified on the element line
HDIF	is a heavy diffusion length specified in the model card
WMLT	is a shrink factor specified in the model card
XW	is an etch/mask effect factor specified in the model card

Note: SCALM, SCALE, and M factor effects have been ignored in these equations. See MOSFET Diode Models on page 8-27 (ACM=2) for further details.

Parameter Differences

There are some differences in parameter names between the Avant! model and the Berkeley junction models. The Avant! models (ACM=0-3) do not recognize the following BSIM3v3 parameters:

- NJ (ignored, instead use N)
- CJSWG (ignored, instead use CJGATE)
- MJSWG (ignored, there is no equivalent HSPICE parameter, the gate sidewall grading coefficient will be set = MJSW)
- PBSW (ignored, instead use PHP)
- PBSWG (ignored, there is no equivalent HSPICE parameter, the gate sidewall contact potential will be set = PHP)

The Berkeley model (ACM=10,11,12,13) will not recognize the following parameters:

- CJGATE (ignored, instead use CJSWG)
- PHP (ignored, instead use PBSW)

Noise Model

The Hspice-specific parameter NLEV overrides the BSIM3v3 parameter NOIMOD. Specifying NLEV will invoke the Hspice noise model. See Noise Models on page 8-102 for further information. If NLEV is not specified, the Berkeley noise equations are invoked.

Performance Improvements

The performance of Levels 49 and 53 has been improved by reducing model equation complexity, replacing some calculations with spline functions, and compiler optimization. For Level 49, the result is a reduction in simulation time of up to 40% compared to releases prior to 97.4 while maintaining accuracy to 5 digits or better. The use of spline functions can be enabled by setting the model parameter to SFVTFLAG=1 in the model card. SFVTFLAG=0, the default value, disables the spline functions. For Level 53, all BSIM3v3 non-compliant features default to off. There is a significant reduction in simulation time compared to pre-97.4 releases remains.

Reduced Parameter Set BSIM3v3 Model (BSIM3-lite)

Setting the Level 49 model parameter LITE=1 invokes the BSIM3v3-lite model. This is a BSIM3v3 reduced parameter set model Use it with model binning. Without binning, to account for geometry effects, the full BSIM3v3 model specifies many model parameters. However, it is often difficult to extract a “global” BSIM3v3 model that is accurate over the entire geometry range. To improve accuracy over a range of geometries, you can bin the model parameters. That is, the entire length-width geometry range is divided into rectangular regions or bins. A different set of parameters is extracted for each bin. The Hspice built-in bilinear parameter interpolation scheme maintains continuity (over length-width) at the boundaries between bins. Since many BSIM3 model parameters account for MOSFET geometry effects, these geometry-effect parameters are redundant and can be eliminated when binning is used.

The BSIM3-lite model parameter set was created in response to the question: What BSIM3 parameters should be excluded when using a binned model? The BSIM3-lite model is invoked by specifying the model parameter LITE=1 in the model card. Simulation checks the model card to determine if it conforms to the BSIM3-lite parameter set. BSIM3-lite takes advantage of the smaller number of calculations and will reduce simulation times by up to 10% compared to the full parameter set BSIM3 model. LITE=1 is supported only by Level 49.

The following table lists model parameters (total 49) that are excluded from the BSIM3-lite model. All parameters in this list should either be excluded from the model card or explicitly set to the default value specified in the list. In some cases, as noted, the BSIM3-lite default value differs from the standard BSIM3v3 default value. Also, exclusion of WR,ALPHA0, CIT is only recommended but not required in the BSIM3-lite model card.

Table 10-1: Parameters Excluded from BSIM3-Lite Model *(Sheet 1 of 3)*

Parameter	Comments
mobmod	Recommended default or set = 1
nqsmod	Recommended default or set = 0
toxm	default = tox
ll	default = 0
lln	default = 1
lw	default = 0
lwn	default = 1
lwl	default = 0
wl	default = 0
wln	default = 1
ww	default = 0
wwn	default = 1
wwl	default = 0
dwg	default = 0
dwb	default = 0
llc	default = 0
lwc	default = 0

Table 10-1: Parameters Excluded from BSIM3-Lite Model *(Sheet 2 of 3)*

Parameter	Comments
lwlc	default = 0
wlc	default = 0
wwc	default = 0
wwlc	default = 0
b0	default = 0
b1	default = 0
vbx	do not define
vbm	do not define
xt	do not define
nsub	do not define
nlx	default = 0, std default=1.74e-7
gamma1	do not define
gamma2	do not define
ngate	Recommended default or set = 0
k3	default = 0, std default=80
k3b	default = 0
w0	no effect
dvt0	default = 0, std default=2.2
dvt1	default = 0, std default=0.53
dvt2	default = 0, std default=-0.032
dvt0w	default = 0

Table 10-1: Parameters Excluded from BSIM3-Lite Model *(Sheet 3 of 3)*

Parameter	Comments
dvt1w	default = 0, std default=5.3e6
dvt2w	default = 0, std default=-0.032
dsub	default = 0
prwg	default = 0
prwb	default = 0
wr	Recommended default or set = 1
drout	default = 0, std default=0.56
pdiblc1	default = 0, std default=0.39
cit	Recommended default or set = 0
alpha0	Recommended default or set = 0 for Version 3.2
kt1l	default = 0

Parameter Binning

Parameter binning is supported in the Berkeley BSIM3v3 release through the specification of LWP parameters. That is, a subset of model parameters can be bilinearly interpolated over `1/Leff` and `1/Weff` by specifying four terms: the parameter Xo, a length term Xl, a width term Xw, and a product term Xp. The parameter value at a given L,W is then interpolated as:

```
X = Xo + Xl/Leff + Xw/Weff + Xp/Leff/Weff
```

See ‘Model Parameter Range Limit” on page 10-51 to determine whether a parameter can be binned. Simulation adds the LMIN, LMAX, WMIN, WMAX and LREF, WREF parameters to allow multiple cell binning. LMIN, LMAX, WMIN, WMAX define the cell boundary. LREF, WREF are offset values that provide a convenient interpolation scheme. LREF,WREF offsets are used when both values are defined and the model parameter BINFLAG >0.9 is specified.

The parameter value at a given L,W is then interpolated as:

```
X = Xo + Xl*(1/Leff - 1/LREF) + Xw*(1/Weff - 1/WREF) +
   Xp/(1/Leff - 1/LREF)/(1/Weff - 1/WREF)
```

The units for the lwp geometry parameters can be selected to be in microns by setting the model parameter BINUNIT = 1. For other choices of BINUNIT, the lengths are in units of meters. The Hspice XL, XLREF, XW, and XWREF parameters are handled in a manner consistent with other Hspice models, and they produce shifts in parameter values without disrupting the continuity across bin boundaries.

Charge Models

In the December, 1996 release of BSIM3v3, Berkeley offers the BSIM1 capacitance model as CAPMOD=0. This is replaced with a modified BSIM1 capacitance model based on the Hspice CAPOP=13 model in Level 49. Level 53 uses the Berkeley BSIM1 capacitance model for CAPMOD=0. The following table lists CAPMOD defaults for the Berkeley BSIM3v3 model and for Levels 49 and 53.

Version	BSIM3v3	Level 49	Level 53
3.0	1	1	1
3.1	2	0	2
3.2	3	3	3

Hspice VFBFLAG

The capacitance model CAPMOD=0 normally calculates the threshold voltage as Vth = vfbc + phi + k1 * sqrt(phi - vbs), where vfbc is the model parameter VFBCV. This has the effect of eliminating any dependence on the parameter VTH0. To allow capacitance dependence on VTH0, set the model parameter VFBFLAG=1. The capacitance model CAPMOD=0 will calculate the threshold voltage as Vth = vth0 + k1 * sqrt(phi - vbs) - k1 * sqrt(phi). The VFBFLAG default value is 0.

Printback

Printback of all model parameters with units is now enabled. The printback also indicates whether Berkeley or Avant! model junction diodes and noise models are invoked and which parameters are not used (for example, CJGATE is not used when ACM=0-3).

Using BSIM3v3

The following are points to note when using BSIM3v3 with one of the Avant! in-circuit simulators:

1. Use either the Level 49 or Level 53 model. Level 53 fully complies with the Berkeley BSIM3v3 release. However, in most cases Level 49, in comparison to Level 53, gives identical results, run as fast or faster, shows better convergence, and allows a wider range of parameter specifications.
2. Explicitly set all Berkeley-specific BSIM3 model parameters in the model card. This will minimize problems resulting from version changes and compatibility with other simulators. Explicitly setting all lwp binning parameters is not necessary.
3. To obtain matching results with simulations from previous Hspice versions use the model parameter HSPVER=YY.N, e.g., HSPVER=97.4. Do not use the full year specification (e.g., do not use 1997.4). Patch version numbers are implemented as HSPVER=YY.NN (for example, HSPVER=98.21 for Hspice release 98.2.1).
4. Levels 49 and 53 support the model parameter name TNOM as an alias for TREF. The conventional terminology in Hspice is TREF, which is supported as a model parameter in all Avant! model MOS levels. The alternative name TNOM is supported in both Levels 49 and 53, for compatibility with SPICE3.

   The default room temperature is 25^{o}C in this model, but is 27^{o}C in SPICE3. If the BSIM3 model parameters are specified at 27^{o}C, TNOM=27 should be added to the model, so that the model parameters are interpreted correctly. It is a matter of choice whether or not to set the nominal simulation temperature to 27, by adding .OPTION TNOM=27 to the netlist. Add this option when testing the Avant! model versus SPICE3.

DELVTO and DTEMP on the element line can be used with Levels 49 and 53. The conversion of temperature setup between the Avant! model and SPICE3 is as follows:

```
SPICE3:      .OPTIONS TEMP=125
             .MODEL NCH NMOS Level=8
             + TNOM =27 ...

Avant! True-Hspice:.TEMP 125
             .MODEL NCH NMOS Level=49
             + TNOM =27 ...
```

5. To automatically calculate drain, source area, and perimeter factors with the Berkeley junction diode models, use ACM=12 with CALCACM=1. Normally, ACM=10-13 defaults area and perimeter factors to 0. To override this for ACM=12, specify CALCACM=1. Define the Hspice-specific parameter (HDIF) in the model card. If you do not want to have parasitic Rs and Rd in addition to the BSIM3v3 internal Rsd, then make sure that the Hspice-specific parameters (RSH, RSC, RDC,RS, RD) are either not specified (default is 0) or explicitly set to 0.
6. Simulation and analysis will either warn or abort with a fatal error when certain model parameter values are out of a normal range. To view all the warnings, the .OPTION WARNLIMIT value may have to be increased (default=1). To turn full parameter range checking, set the model parameter PARAMCHK=1 (default is 0). With PARAMCHK=0 a smaller set of parameters is checked. (See ‘Model Parameter Range Limit” on page 10-51 for more details regarding parameter limits.) Use the model parameter APWARN=1 (default=0) to turn off PS,PD < Weff warnings.
7. NQSMOD can only be used with Version 3.2 and can only be specified in the model card.

Level 49, 53 Model Parameters

The following tables describe all Level 49 and Level 53 model parameters including:

- parameter name
- units
- default value
- whether the parameter can be binned
- a description

These tables are a superset of the BSIM3v3 model parameter set, and include Hspice-specific parameters. These Hspice-specific parameters are noted in the description column, and always default (for Level 53) to maintain compliance with the BSIM3v3 standard. These parameters also apply to Level 49 with the following exceptions: ACM default value = 0, XPART default value = 1, CAPMOD default value = 0.

Model Flags

Name	Unit	Default	Bin	Description
VERSION	-	3.2	No	Selects from BSIM3 Versions 3.0, 3.1, 3.2. Warning is issued if not explicitly set.
HSPVER	-	98.2	No	Selects from Hspice Versions: 98.2, 97.4, 97.2, 96.4, 96.3, 96.1
PARAMCHK	-	0	No	PARAMCHK=1 will check model parameters for range compliance
APWARN	-	0	No	When >0 turns off warning message for PS,PD < Weff (Hspice specific)
BINFLAG	-	0	No	Uses wref, lref when set >0.9 (Hspice specific)
MOBMOD	-	1	No	Mobility model selector
CAPMOD	-	3	No	Selects from charge models 0,1,2,3 Level 49 CAPMOD defaults to 0.
CAPOP	-	-	No	Obsolete for Levels 49, 53. Ignored by Hspice (Hspice specific) in all versions.
NOIMOD	-	1	No	Berkeley noise model flag

Name	Unit	Default	Bin	Description
NLEV	-	-(off)	No	The noise model flag (non-zero overrides NOIMOD) (Hspice specific). See Noise Models on page 8-102 for more information.
NQSMOD	-	0 (off)	No	NQS Model flag
SFVTFLAG	-	0 (off)	No	Spline function for Vth (Hspice specific)
VFBFLAG	-	0 (off)	No	VFB selector for CAPMOD=0 (Hspice specific)

Basic Model Parameters

Name	Unit	Default	Bin	Description
VGSLIM	V	0	No	Asymptotic Vgs value, Min value is 5V. 0-value indicates an asymptote of infinity. (Hspice and Level 49 specific)
TOX	m	150e-10	No	Gate oxide thickness
XJ	m	0.15e-6	Yes	Junction depth
NGATE	cm^{-3}	0	Yes	Poly gate doping concentration
VTH0 (VTHO)	V	0.7 NMOS -0.7 PMOS	Yes	Threshold voltage of long channel device at $V_{bs} = 0$ and small V_{ds}
NSUB	cm^{-3}	6.0e16	Yes	Substrate doping concentration

Name	Unit	Default	Bin	Description
NCH	cm^{-3} See Note6	1.7e17	Yes	Peak doping concentration near interface
NLX	m	1.74e-7	Yes	Lateral nonuniform doping along channel
K1	$V^{1/2}$	0.50	Yes	First-order body effect coefficient
K2	-	-0.0186	Yes	Second-order body effect coefficient
K3	-	80.0	Yes	Narrow width effect coefficient
K3B	1/V	0	Yes	Body width coefficient of narrow width effect
W0	m	2.5e-6	Yes	Narrow width effect coefficient
DVT0W	1/m	0	Yes	Narrow width coefficient 0, for Vth, at small L
DVT1W	1/m	5.3e6	Yes	Narrow width coefficient 1, for Vth, at small L
DVT2W	1/V	-0.032	Yes	Narrow width coefficient 2, for Vth, at small L
DVT0	-	2.2	Yes	Short channel effect coefficient 0, for V_{th}
DVT1	-	0.53	Yes	Short channel effect coefficient 1, for V_{th}
DVT2	1/V	-0.032	Yes	Short channel effect coefficient 2, for V_{th}
ETA0	-	0.08	Yes	Subthreshold region DIBL (drain induced barrier lowering) coefficient

Name	Unit	Default	Bin	Description
ETAB	1/V	-0.07	Yes	Subthreshold region DIBL coefficient
DSUB	-	DROUT	Yes	DIBL coefficient exponent in subthreshold region
VBM	V	-3.0	Yes	Maximum substrate bias, for V_{th} calculation
U0	cm^2/V/sec	670 nmos 250 pmos	Yes	Low field mobility at T = *TREF* = *TNOM*
UA	m/V	2.25e-9	Yes	First-order mobility degradation coefficient
UB	m^2/V^2	5.87e-19	Yes	Second-order mobility degradation coefficient
UC	1/V	-4.65e-11 or -0.0465	Yes	Body bias sensitivity coefficient of mobility -4.65e-11 for MOBMOD=1,2 or, -0.0465 for MOBMOD = 3
A0	-	1.0	Yes	Bulk charge effect coefficient for channel length
AGS	1/V	0.0	Yes	Gate bias coefficient of Abulk
B0	m	0.0	Yes	Bulk charge effect coefficient for channel width
B1	m	0.0	Yes	Bulk charge effect width offset
KETA	1/V	-0.047	Yes	Body-bias coefficient of bulk charge effect

Name	Unit	Default	Bin	Description
VOFF	V	-0.08	Yes	Offset voltage in subthreshold region
VSAT	m/sec	8e4	Yes	Saturation velocity of carrier at T = *TREF = TNOM*
A1	1/V	0	Yes	First nonsaturation factor
A2	-	1.0	Yes	Second nonsaturation factor
RDSW	ohm · μm	0.0	Yes	Parasitic source drain resistance per unit width
PRWG	1/V	0	Yes	Gate bias effect coefficient of RDSW
PRWB	$1/V^{1/2}$	0	Yes	Body effect coefficient of RDSW
WR	-	1.0	Yes	Width offset from Weff for Rds calculation
NFACTOR	-	1.0	Yes	Subthreshold region swing
CIT	F/m^2	0.0	Yes	Interface state capacitance
CDSC	F/m^2	2.4e-4	Yes	Drain/source and channel coupling capacitance
CDSCD	F/Vm^2	0	Yes	Drain bias sensitivity of CDSC
CDSCB	F/Vm^2	0	Yes	Body coefficient for CDSC
PCLM	-	1.3	Yes	Coefficient of channel length modulation values ≤ 0 will result in an error message and program exit.

Name	Unit	Default	Bin	Description
PDIBLC1	-	0.39	Yes	DIBL (drain induced barrier lowering) effect coefficient 1
PDIBLC2	-	0.0086	Yes	DIBL effect coefficient 2
PDIBLCB	1/V	0	Yes	Body effect coefficient of DIBL effect coefficients
DROUT	-	0.56	Yes	Length dependence coefficient of the DIBL correction parameter in R_{out}
PSCBE1	V/m	4.24e8	Yes	substrate current induced body effect exponent 1
PSCBE2	V/m	1.0e-5	Yes	Substrate current induced body effect coefficient 2
PVAG	-	0	Yes	Gate dependence of Early voltage
DELTA	V	0.01	Yes	Effective Vds parameter
ALPHA0	m/V	0	Yes	First parameter of impact ionization current
BETA0	V	30	Yes	Second parameter of impact ionization current
RSH	0.0	ohm/ square	No	Source/drain sheet resistance in ohm per square

AC and Capacitance Parameters

Name	Unit	Default	Bin	Description
XPART	-	0	No	Charge partitioning rate flag (default deviates from BSIM3V3=0) Level 49 XPART defaults to 1
CGSO	F/m	p1 (see Note1)	No	Non-LDD region source-gate overlap capacitance per unit channel length
CGDO	F/m	p2 (see Note2)	No	Non-LDD region source-gate overlap capacitance per unit channel length
CGBO	F/m	0	No	Gate-bulk overlap capacitance per unit channel length
CGS1	F/m	0.0	Yes	Lightly doped source-gate overlap region capacitance
CGD1	F/m	0.0	Yes	Lightly doped drain-gate overlap region capacitance
CKAPPA	F/m	0.6	Yes	Coefficient for lightly doped region overlap capacitance fringing field capacitance
CF	F/m	(see Note3)	Yes	Fringing field capacitance
CLC	m	0.1e-6	Yes	Constant term for the short channel model
CLE	-	0.6	Yes	Exponential term for the short channel model
VFBCV	V	-1.0	Yes	Flat band voltage used only in CAPMOD=0 C-V calculations

Length and Width Parameters

Name	Unit	Default	Bin	Description
WINT	m	0.0	No	Width offset fitting parameter from I-V without bias
WLN	-	1.0	No	Power of length dependence of width offset
WW	m^{WWN}	0.0	No	Coefficient of width dependence for width offset
WWN	-	1.0	No	Power of width depends on width offset.
WWL	m^{WWN} *m^{WLN}	0.0	No	Coefficient of length and width cross term for width offset
DWG	m/V	0.0	Yes	Coefficient of Weff's gate dependence
DWB	$m/V^{1/2}$	0.0	Yes	Coefficient of Weff's substrate body bias dependence
LINT	m	0.0	No	Length offset fitting parameter from I-V without bias
LL	m^{LLN}	0.0	No	Coefficient of length dependence for length offset
LLN	-	1.0	No	Power of length dependence of length offset
LW	m^{LWN}	0.0	No	Coefficient of width dependence for length offset
LWN	-	1.0	No	Power of width dependence of length offset

Name	Unit	Default	Bin	Description
LWL	m^{LWN} *m^{LLN}	0.0	No	Coefficient of length and width cross term for length offset
DLC	m	LINT	No	Length offset fitting parameter from CV
DWC	m	WINT	No	Width offset fitting parameter from CV

Temperature Parameters

Name	Unit	Default	Bin	Description
KT1	V	-0.11	Yes	Temperature coefficient for Vth
KT1L	m-V	0.0	Yes	Temperature coefficient for channel length dependence of Vth
KT2	-	0.022	Yes	Body bias coefficient of Vth temperature effect
UTE	-	-1.5	Yes	Mobility temperature exponent
UA1	m/V	4.31e-9	Yes	Temperature coefficient for UA
UB1	$(m/V)^2$	-7.61e-18	Yes	Temperature coefficient for UB
UC1	m/V^2	-5.69e-11	Yes	Temperature coefficient for UC
AT	m/sec	3.3e4	Yes	Temperature coefficient for saturation velocity
PRT	ohm-um	0	Yes	Temperature coefficient for RDSW
XTI	-	3.0	No	Junction current temperature exponent

Bin Description Parameters

Name	Unit	Default	Bin	Description
LMIN	m	0.0	No	Maximum channel length
LMAX	m	1.0	No	Maximum channel length
WMIN	m	0.0	No	Minimum channel width
WMAX	m	1.0	No	Maximum channel width
BINUNIT				Assumes weff, leff, wref, lref units are in microns when BINUNIT=1 or meters otherwise

Process Parameters

Name	Unit	Default	Bin	Description
GAMMA1	$V^{1/2}$	see Note 8	Yes	Body effect coefficient near the surface
GAMMA2	$V^{1/2}$	see Note 9	Yes	Body effect coefficient in the bulk
VBX	V	see Note 10	Yes	VBX at which the depletion region width equals XT
XT	m	1.55e-7	Yes	Doping depth

Noise Parameters

Name	Unit	Default	Bin	Description
NIOA	-	1.0e20 nmos 9.9e18 pmos	No	Body effect coefficient near the surface

Name	Unit	Default	Bin	Description
NOIB	-	5.0e4 nmos 2.4e3 pmos	No	Body effect coefficient in the bulk
NOIC	-	-1.4e-12 nmos 1.4e-12 pmos	No	VBX at which the depletion region width equals XT
EM	V/m	$4.1e^{7}$	No	Flicker noise parameter
AF	-	1.0	No	Flicker noise exponent
KF	-	0.0	No	Flicker noise coefficient
EF	-	1.0	No	Flicker noise frequency exponent

Note: See also Noise Models on page 8-102, for Hspice noise model usage (Hspice parameter NLEV overrides Berkeley NOIMOD).

Junction Parameters

Name	Unit	Default	Bin	Description
ACM	-	10	No	Area calculation method selector (Hspice specific) ■ ACM=0-3 uses Hspice junction models ■ ACM=10-13 uses Berkeley junction models ■ Level 49 ACM defaults to 0
JS	A/m^2	0.0	No	Bulk junction saturation current. (Default deviates from BSIM3v3 = $1.0e^{-4}$)

Name	Unit	Default	Bin	Description
JSW	A/m	0.0	No	Sidewall bulk junction saturation current
NJ	-	1	No	Emission coefficient (used only with Berkeley junction model: ACM=10-13)
N	-	1	No	Emission coefficient (Hspice-specific), (used only with the Hspice junction model, i.e., ACM=0-3)
CJ	F/m^2	$5.79e^{-4}$	No	Zero-bias bulk junction capacitance (Default deviates from BSIM3v3 = $5.0e^{-4}$)
CJSW	F/m	0.0	No	Zero-bias sidewall bulk junction capacitance (Default deviates from BSIM3v3 = $5.0e^{-10}$)
CJSWG	F/m	CJSW	No	Zero-bias gate-edge sidewall bulk junction capacitance (only used with Berkeley junction model, i.e., ACM=10-13)
CJGATE	F/m	CJSW	No	Zero-bias gate-edge sidewall bulk junction capacitance (Hspice-specific) (used only with ACM=3)
PB, PHIB	V	1.0	No	Bulk junction contact potential
PBSW	V	1.0	No	Sidewall bulk junction contact potential
PHP	V	1.0	No	Sidewall bulk junction contact potential (Hspice-specific) (used only with Hspice junction model: ACM=0-3)

Name	Unit	Default	Bin	Description
PBSWG	V	PBSW	No	Gate-edge sidewall bulk junction contact potential (only used with Berkeley junction model, i.e., ACM=10-13). **Note:** There is no equivalent Hspice parameter. Gate-edge contact potential is always set to PHP for Hspice junction model.
MJ	-	0.5	No	Bulk junction grading coefficient
MJSW	-	0.33	No	Sidewall bulk junction grading coefficient
MJSWG	-	MJSW	No	Gate-edge sidewall bulk junction grading coefficient (only used with Berkeley junction model: ACM=10-13) **Note:** There is no equivalent Hspice parameter. Gate-edge grading coefficient is always set to MJSW for Hspice junction model.

Note: See MOSFET Diode Models on page 8-27 for Hspice junction diode model usage.

NonQuasi-Static (NQS) Parameters

Name	Unit	Default	Bin	Description
ELM	-	5.0	Yes	Elmore constant

Version 3.2 Parameters

Name	Unit	Default	Bin	Description
TOXM	m	TOX	No	Reference gate oxide thickness
VFB	V	See Note 11	Yes	DC flatband voltage
NOFF	-	1.0	Yes	I-V parameter for weak to strong inversion transition
VOFFCV	-	0.0	Yes	C-V parameter for weak to strong inversion transition
JTH	A	0.1	No	Diode limiting current
ALPHA1	V^{-1}	0.0	Yes	Substrate current parameter
ACDE	m/V	1.0	Yes	Exponential coefficient for charge thickness in the accumulation and depletion regions
MOIN	m/V	15.0	Yes	Coefficient for gate-bias dependent surface potential
TPB	V/K	0.0	No	Temperature coefficient of PB
TPBSW	V/K	0.0	No	Temperature coefficient of PBSW
TPBSWG	V/K	0.0	No	Temperature coefficient of PBSWG
TCJ	V/K	0.0	No	Temperature coefficient of CJ

Name	Unit	Default	Bin	Description
TCJSW	V/K	0.0	No	Temperature coefficient of CJSW
TCJSWG	V/K	0.0	No	Temperature coefficient of CJSWG
LLC	m^{lln}	LL	No	Coefficient of length dependence for C-V channel length offset
LWC	m^{lwn}	LW	No	Coefficient of width dependence for C-V channel length offset
LWLC	$m^{lln+lwn}$	LWL	No	Coefficient of length and width for C-V channel length offset
WLC	m^{wln}	WL	No	Coefficient of length dependence for C-V channel width offset
WWC	m^{wwn}	WW	No	Coefficient of width dependence for C-V channel width offset
WWLC	$m^{wln+wwn}$	WWL	No	Coefficient of length and width cross terms for C-V channel width offset

Notes:

1. If C_{gso} is not given, it is calculated as follows:
   If (*dlc* is given and is greater than *0.0)*, then,

   cgso = p1 = max(0,dlc*cox - cgs1)

   Otherwise, *cgso = 0.6*xj*cox*

2. If C_{gdo} is not given, it is calculated as follows:

   if (*dlc* is given and is greater than *0.0)*, then,

   cgdo = p2 = max(0,dlc*cox - cgd1)

   Otherwise *cgdo = 0.6*xj*cox*

3. If C_f is not given, it is calculated using:

$$C_f = \frac{2\varepsilon_{ox}}{\pi}\log\left(1 + \frac{4\times10^{-7}}{T_{ox}}\right)$$

4. If V_{th0} is not specified in the .MODEL statement, it is calculated with V_{fb} = -1, using:

$$V_{th0} = V_{fb} + \phi_s + K_1\sqrt{\phi_s}$$

5. If K_1 and K_2 are not given, they are calculated using:

$$K_1 = GAMMA_2 + 2K_2\sqrt{\phi_s - V_{bs}}$$

$$K_2 = \frac{(GAMMA_2 - GAMMA_1)(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s})}{2\sqrt{\phi_s}(\sqrt{\phi_s - V_{bm}} - \sqrt{\phi_s}) + V_{bm}}$$

6. If n_{ch} is not given, and $GAMMA_1$ is given, n_{ch} is calculated from:

$$n_{ch} = \frac{GAMMA_1^2 C_{OX}^2}{2q\varepsilon_{si}}$$

If you do not specify either n_{ch} and $GAMMA_1$, then n_{ch} defaults to 1.7e17 per cubic meter and $GAMMA_1$ is calculated from n_{ch}.

7. If *PHI* is not given, it is calculated using:

$$\phi_s = 2\frac{k_B T}{q}\log\left(\frac{n_{ch}}{n_i}\right)$$

$$n_i = 1.45\times10^{10}\left(\frac{T}{300.15}\right)^{1.5}\exp\left(21.5565981 - \frac{qE_g(T)}{2k_B T}\right)$$

$$E_g(T) = 1.16 - \frac{7.02\times10^{-4}T^2}{T + 1108}$$

8. If you do not specify $GAMMA_1$, it is calculated using:

$$\mathrm{GAMMA}_1 = \frac{\sqrt{2q\varepsilon_{si}n_{ch}}}{C_{ox}}$$

9. If $GAMMA_2$ is not given, it is calculated using:

$$\mathrm{GAMMA}_2 = \frac{\sqrt{2q\varepsilon_{si}n_{sub}}}{C_{ox}}$$

10. If V_{bx} is not given, it is calculated using:

$$V_{bx} = \phi_s - \frac{qn_{ch}X_t^2}{2\varepsilon_{si}}$$

11. The BSIM3 model can calculate V_{th} in any of three ways:
    - Using *K1* and *K2* values that are user specified
    - Using *GAMMA1*, *GAMMA2*, *VBM*, and *VBX* values entered in the .MODEL statement
    - Using *NPEAK*, *NSUB*, *XT*, and *VBM* values that are user specified

You can enter the U0 model parameter in meters or centimeters. U0 is converted to m^2/Vsec as follows: if U0 is greater than 1, it is multiplied by 1e-4. The parameter NSUB must be entered in cm^{-3} units.

Specify a negative value of VTH0 for p-channel in the .MODEL statement.

The impact ionization current determined by the model parameters PSCBE1 and PSCBE2 contributes to the bulk current.

Parameter Range Limits

Simulation reports either warning or fatal error when BSIM3v3 parameters fall outside predefined ranges. These range limitations prevent or at least warn of potential numerical problems. Level 53 follows exactly the BSIM3v3 range limit reporting scheme. Level 49 deviates from the BSIM3v3 scheme as noted in the comments column of Model Parameter Range Limit.

To control the maximum number of simulation warning messages printing to the output file use:

```
.OPTION WARNLIMIT=#
```

where # is the maximum number of warning messages that simulation reports. The default WARNLIMIT value is 1. In some cases (as noted in the following table) parameters are checked only when the model parameter PARMAMCHK=1 is set.

Model Parameter Range Limit

Name	Limits	Comments
TOX	<= 0 Fatal < 10-9 Warn if parmchk=1	
TOXM	<= 0 Fatal < 10-9 Warn if parmchk=1	
XJ	<= 0 Fatal	
NGATE	< 0 Fatal > 10^{25} Fatal <= 10^{18} Fatal if parmchk=1	if >10^{23} NGATE is multiplied by 10-6. This is done prior to the other limit checks. Level 49 gives: ■ < 0 Fatal ■ > 10^{25} Warn ■ <= 10^{18} Warn if paramchk==1
NSUB	<= 0 Fatal <= 10^{14} Warn if parmchk=1 >= 10^{21} Warn if parmchk=1	NSUB is ignored if k1,k2 are defined
NCH	<= 0 Fatal <= 10^{15} Warn if parmchk=1 >= 10^{21} Warn if parmchk=1	if >10^{20} NCH is multiplied by 10-6. This is done prior to the other limit checks.

Name	Limits	Comments
NLX	< -Leff Fatal < 0 Warn if parmchk=1	
W0	= -Weff Fatal w0 + Weff < 10^{-7} Warn if paramchk==1	
DVT1W	< 0 Fatal	< 0 Level 49 gives Warn
DVT0	< 0 Warn if paramchk=1	
DVT1	< 0 Fatal	< 0 Level 49 gives Warn
ETA0	<= 0 Warn if paramchk=1	
DSUB	< 0 Fatal	< 0 Level 49 gives Warn
VBM		Ignored if K1,K2 are defined
U0	<= 0 Fatal	
B1	= -Weff Fatal B1 + Weff < 10^{-7} Warn if paramchk=1	
VSAT	<= 0 Fatal < 10^{3} Warn if paramchk==1	
A1	-	See a2 conditions
A2	■ < 0.01 Warn and reset a2=0.01 if paramchk=1 ■ > 1 Warn and reset a2=1,a1=0 if paramchk=1	
DELTA	< 0 Fatal	
RDSW	< 0.001 Warn if paramchk=1 and reset rdsw=0	

Name	Limits	Comments
NFACTOR	< 0 Warn if paramchk=1	
CDSC	< 0 Warn if paramchk=1	
CDSCD	< 0 Warn if paramchk=1	
PCLM	<= 0 Fatal	
PDIBLC1	< 0 Warn if paramchk=1	
PDIBLC2	< 0 Warn if paramchk=1	
PS	< Weff Warn	
DROUT	< 0 Fatal if paramchk=1	Level 49 gives Warn
PSCBE2	<= 0 warn if paramchk=1	
CGS0	< 0 Warn and reset to 0 if paramchk=1	
CGD0	< 0 Warn and reset to 0 if paramchk=1	
CGB0	< 0 Warn and reset to 0 if paramchk=1	
ACDE	< 0.4, >1.6 Warn	
MOIN	< 5.0, >25 Warn	
IJTH	< 0 Fatal	
NOFF	< 0.1, >4.0 Warn	

Element Parameters Range Limits

Name	Limits	Comments
PD	< Weff, Warn	
PS	< Weff, Warn	
Leff	< 5.0 x 10^{-8} Fatal	
Weff	< 1.0 x 10^{-7} Fatal	
LeffCV	< 5.0 x 10^{-8} Fatal	
WeffCV	< 1.0 x 10^{-7} Fatal	

Level 49, 53 Equations

The effective channel length and width used in all model equations are:

$$L_{eff} = L_{drawn} - 2dL$$

$$W_{eff} = W_{drawn} - 2dW$$

$$W'_{eff} = W_{drawn} - 2dW'$$

Wdrawn = W * WMULT + XW
Ldrawn = L * LMULT + XL

The unprimed W_{eff} is bias-dependent. The primed quantity is bias-independent.

$$dW = dW' + dW_g V_{gsteff} + dW_b(\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s})$$

$$dW' = W_{int} + \frac{W_L}{L^{WLN}} + \frac{W_W}{W^{WWN}} + \frac{W_{WL}}{L^{WLN} W^{WWN}}$$

$$dL = L_{int} + \frac{L_L}{L^{LLN}} + \frac{L_W}{W^{LWN}} + \frac{L_{WL}}{L^{LLN} W^{LWN}}$$

For C-V calculations dW’ is replaced with

$$dW' = DWC + \frac{W_{LC}}{L^{WLN}} + \frac{W_{WC}}{W^{WWN}} + \frac{W_{WLC}}{L^{WLN} W^{WWN}}$$

and dL’ is replaced with

$$dL = DLC + \frac{L_{LC}}{L^{LLN}} + \frac{L_{WC}}{W^{LWN}} + \frac{L_{WLC}}{L^{LLN} W^{LWN}}$$

Note: A detailed discussion of the BSIM3 Version 3 equations is available from the BSIM3 site:
http://www-device.eecs.berkeley.edu/~bsim3/get.html

.MODEL CARDS NMOS Model

```
.model nch nmos Level=49
+ Tnom=27.0
+ nch=1.024685E+17 tox=1.00000E-08 xj=1.00000E-07
+ lint=3.75860E-08 wint=-2.02101528644562E-07
+ vth0=.6094574 k1=.5341038 k2=1.703463E-03 k3=-17.24589
+ dvt0=.1767506 dvt1=.5109418 dvt2=-0.05
+ nlx=9.979638E-08 w0=1e-6
+ k3b=4.139039
+ vsat=97662.05 ua=-1.748481E-09 ub=3.178541E-18 uc=1.3623e-
10
+ rdsw=298.873 u0=307.2991 prwb=-2.24e-4
+ a0=.4976366
+ keta=-2.195445E-02 a1=.0332883 a2=.9
+ voff=-9.623903E-02 nFactor=.8408191 cit=3.994609E-04
+ cdsc=1.130797E-04
+ cdscb=2.4e-5
+ eta0=.0145072 etab=-3.870303E-03
+ dsub=.4116711
```

```
+ pclm=1.813153 pdiblc1=2.003703E-02 pdiblc2=.00129051
+ pdiblcb=-1.034e-3
+ drout=.4380235 pscbe1=5.752058E+08 pscbe2=7.510319E-05
+ pvag=.6370527 prt=68.7 ngate=1.e20 alpha0=1.e-7 beta0=28.4
+ prwg=-0.001 ags=1.2
+ dvt0w=0.58 dvt1w=5.3e6 dvt2w=-0.0032
+ kt1=-.3 kt2=-.03
+ at=33000
+ ute=-1.5
+ ua1=4.31E-09 ub1=7.61E-18 uc1=-2.378e-10
+ kt1l=1e-8
+ wr=1 b0=1e-7 b1=1e-7 dwg=5e-8 dwb=2e-8 delta=0.015
+ cgdl=1e-10 cgsl=1e-10 cgbo=1e-10 xpart=0.0
+ cgdo=0.4e-9 cgso=0.4e-9
+ clc=0.1e-6
+ cle=0.6
+ ckappa=0.6
```

PMOS Model

This is an example of a PMOS model. VTH0 is negative.

```
.model pch PMOS Level=49
+ Tnom=27.0
+ nch=5.73068E+16 tox=1.00000E-08 xj=1.00000E-07
+ lint=8.195860E-08 wint=-1.821562E-07
+ vth0=-.86094574 k1=.341038 k2=2.703463E-02 k3=12.24589
+ dvt0=.767506 dvt1=.65109418 dvt2=-0.145
+ nlx=1.979638E-07 w0=1.1e-6
+ k3b=-2.4139039
+ vsat=60362.05 ua=1.348481E-09 ub=3.178541E-19 uc=1.1623e-
10
+ rdsw=498.873 u0=137.2991 prwb=-1.2e-5
+ a0=.3276366
+ keta=-1.8195445E-02 a1=.0232883 a2=.9
+ voff=-6.623903E-02 nFactor=1.0408191 cit=4.994609E-04
+ cdsc=1.030797E-3
+ cdscb=2.84e-4
+ eta0=.0245072 etab=-1.570303E-03
+ dsub=.24116711
+ pclm=2.6813153 pdiblc1=4.003703E-02 pdiblc2=.00329051
```

```
+ pdiblcb=-2.e-4
+ drout=.1380235 pscbe1=0 pscbe2=1.e-28
+ pvag=-.16370527
+ prwg=-0.001 ags=1.2
+ dvt0w=0.58 dvt1w=5.3e6 dvt2w=-0.0032
+ kt1=-.3 kt2=-.03 prt=76.4
+ at=33000
+ ute=-1.5
+ ua1=4.31E-09 ub1=7.61E-18 uc1=-2.378e-10
+ kt1l=0
+ wr=1 b0=1e-7 b1=1e-7 dwg=5e-8 dwb=2e-8 delta=0.015
+ cgdl=1e-10 cgsl=1e-10 cgbo=1e-10 xpart=0.0
+ cgdo=0.4e-9 cgso=0.4e-9
+ clc=0.1e-6
+ cle=0.6
+ ckappa=0.6
```

Level 50 Philips MOS9 Model

The Philips MOS Model 9, Level 902, is available as Level 50 in the Avant! models (based on the “Unclassified Report NL-UR 003/94” by R.M.D.A. Velghe, D.B.M. Klaassen, and F.M. Klaassen).

The model has been installed in its entirety, except for the gate noise current.

The ACM Parasitic Diode Model, using parameters JS, JSW, N, CJ, CJSW, CJGATE, MJ, MJSW, PB, PHP, ACM, and HDIF, has been added. The older parameter IS is not used. The Philips JUNCAP Parasitic Diode Model is available in the Avant! True--Hspice models. The model parameter JUNCAP=1 selects the JUNCAP Model, JUNCAP=0 (default) selects the Hspice ACM Model. For additional information regarding the MOS Model-9,e see:

http://www-us.semiconductors.com/Philips_Models

Level 50 Model Parameters

Name	Unit	Default (N)	Default (P)	Description
LER	m	1.1e-6	1.25e-6	Reference Leff
WER	m	20.0e-6	20.0e-6	Reference Weff
LVAR	m	-220.0e-9	-460.0e-9	Variation in gate length
LAP	m	100.0e-9	25.0e-9	Lateral diffusion per side
WVAR	m	-25.0e-9	-130.0e-9	Variation in active width
WOT	m	0.0	0.0	Channel-stop diffusion per side
TR	°C	21.0	21.0	Reference temperature for model
VTOR	V	730.0e-3	1.1	Threshold voltage at zero bias
STVTO	V/K	-1.2e-3	-1.7e-3	Temperature dependence of VTO
SLVTO	Vm	-135.0e-9	35.0e-9	Length dependence of VTO

Name	Unit	Default (N)	Default (P)	Description
SL2VTO	Vm^2	0.0	0.0	Second length dependence of VTO
SWVTO	Vm	130.0e-9	50.0e-9	Width dependence of VTO
KOR	$V^{-1/2}$	650.0e-3	470.0e-3	Low-back-bias body factor
SLKO	$V^{-1/2}m$	-130.0e-9	-200.0e-9	Length dependence of KO
SWKO	$V^{-1/2}m$	2.0e-9	115.0e-9	Width dependence of KO
KR	$V^{-1/2}$	110.0e-3	470.0e-3	High-back-bias body factor
SLK	$V^{-1/2}m$	-280.0e-9	-200.0e-9	Length dependence of K
SWK	$V^{-1/2}m$	275.0e-9	115.0e-9	Width dependence of K
PHIBR	V	650.0e-3	650.0e-3	Strong inversion surface potential
VSBXR	V	660.0e-3	0.0	Transition voltage for dual-k-factor model
SLVSBX	Vm	0.0	0.0	Length dependence of *VSBX*
SWVSBX	Vm	-675.0e-9	0.0	Width dependence of *VSBX*
BETSQ	AV^{-2}	83.0e-6	26.1e-6	Gain factor of infinite square transistor
ETABET	-	1.6	1.6	Exponent of temperature dependence of gain factor
THE1R	V^{-1}	190.0e-3	190.0e-3	Gate-induced mobility reduction coefficient
STTHE1R	V^{-1}/K	0.0	0.0	Temperature dependence coefficient of *THE1R*
SLTHE1R	$V^{-1}m$	140.0e-9	70.0e-9	Length dependence coefficient of *THE1R*
STLTHE1	$V^{-1}m/K$	0.0	0.0	Temperature dependence of, length dependence of *THE1R*

Name	Unit	Default (N)	Default (P)	Description
SWTHE1	$V^{-1}m$	-58.0e-9	-80.0e-9	Width dependence coefficient of *THE1R*
THE2R	$V^{-1/2}$	12.0e-3	165.0e-3	Back-bias induced mobility reduction coefficient
STTHE2R	$V^{-1/2}$/ K	0.0	0.0	Temperature dependence coefficient of *THE2R*
SLTHE2R	$V^{-1/2}m$	-33.0e-9	-75.0e-9	Length dependence coefficient of *THE2R*
STLTHE2	$V^{-1/2}$ m/K	0.0	0.0	Temperature dependence of, length dependence of *THE2R*
SWTHE2	$V^{-1/2}m$	30.0e-9	20.0e-9	Width dependence coefficient of *THE2R*
THE3R	V^{-1}	145.0e-3	27.0e-3	Lateral field induced mobility reduction coefficient
STTHE3R	V^{-1}/K	-660.0e-6	0.0	Temperature dependence coefficient of *THE3R*
SLTHE3R	$V^{-1}m$	185.0e-9	27.0e-9	Length dependence coefficient of *THE3R*
STLTHE3	$V^{-1}m$/ K	-620.0e-12	0.0	Temperature dependence of, length dependence of *THE3R*
SWTHE3	$V^{-1}m$	20.0e-9	11.0e-9	Width dependence coefficient of *THE3R*
GAM1R	-	145.0e-3	77.0e-3	Drain-induced threshold shift coefficient, for high gate drive
SLGAM1	-	160.0e-9	105.0e-9	Length dependence of *GAM1R*
SWGAM1	-	-10.0e-9	-11.0e-9	Width dependence of *GAM1R*

Name	Unit	Default (N)	Default (P)	Description
ETADSR	-	600.0e-3	600.0e-3	Exponent of drain dependence of *GAM1R*
ALPR	-	3.0e-3	44.0e-3	Channel length modulation factor
ETAALP	-	150.0e-3	170.0e-3	Exponent of length dependence of *ALPR*
SLALP	-	-5.65e-3	9.0e-3	Coefficient of length dependence of *ALPR*
SWALP	m	1.67e-9	180.0e-12	Coefficient of width dependence of *ALPR*
VPR	V	340.0e-3	235.0e-3	Characteristic voltage for channel length modulation
GAMOOR	-	18.0e-3	7.0e-3	Drain-induced threshold shift coefficient, at zero gate drive, and zero back-bias
SLGAMOO	m^2	20.0e-15	11.0e-15	Length dependence of *GAMOOR*
ETAGAMR	-	2.0	1.0	Exponent of back-bias dependence of zero gate-drive, drain-induced threshold shift
MOR	-	500.0e-3	375.0e-3	Subthreshold slope factor
STMO	K^{-1}	0.0	0.0	Temperature dependence coefficient of *MOR*
SLMO	$m^{1/2}$	280.0e-6	47.0e-6	Length dependence coefficient of *MOR*
ETAMR	-	2.0	1.0	Exponent of back-bias dependence of subthreshold slope
ZET1R	-	420.0e-3	1.3	Weak-inversion correction factor

Name	Unit	Default (N)	Default (P)	Description
ETAZET	-	170.0e-3	30.0e-3	Exponent of length dependence of *ZET1R*
SLZET1	-	-390.0e-3	-2.8	Length dependence coefficient of *ZET1R*
VSBTR	V	2.1	100.0	Limiting voltage for back-bias dependence
SLVSBT	Vm	-4.4e-6	0.0	Length dependence of *VSBTR*
A1R	-	6.0	10.0	Weak-avalanche current factor
STA1	K^{-1}	0.0	0.0	Temperature coefficient of *A1R*
SLA1	m	1.3e-6	-15.0e-6	Length dependence of *A1R*
SWA1	m	3.0e-6	30.0e-6	Width dependence of *A1R*
A2R	V	38.0	59.0	Exponent of weak-avalanche current
SLA2	Vm	1.0e-6	-8.0e-6	Length dependence of *A2R*
SWA2	Vm	2.0e-6	15.0e-6	Width dependence of *A2R*
A3R	-	650.0e-3	520.0e-3	Factor of minimum drain bias above which avalanche sets in
SLA3	m	-550.0e-9	-450.0e-9	Length dependence of *A3R*
SWA3	m	0.0	-140.0e-9	Width dependence of *A3R*
TOX	m	25.0e-9	25.0e-9	Oxide thickness
COL	F/m	320.0e-12	320.0e-12	Gate overlap capacitance per unit width
WDOG	m	0	0	Characteristic drawn gate width below which dogboning appears

Name	Unit	Default (N)	Default (P)	Description
FTHE1	-	0	0	Coefficient describing the width dependence of THE1 for W < WDOG
NFMOD		0		Flicker noise selector 0 selects old flicker noise model added in release 98.4
NTR	J	24.4e-21	21.1e-21	Thermal noise coefficient
NFR	V^2	70.0e-12	21.4e-12	Flicker noise coefficient
NFAR	$V^{-1}m^{-2}$	7.15e+22	1.53xe+22	1st flicker noise coefficient added in release 98.4
NFBR	$V^{-1}m^{-2}$	2.16e+06	4.06e+06	2nd flicker noise coefficient added in release 98.4
NFCR	V^{-1}	0.0	2.92e-10	3rd flicker noise coefficient added in release 98.4
SL3VTO	V	0	0	Third coefficient of the length dependence of V_{TO}
SL2KO	$V^{1/2}m^2$	0	0	Second coefficient of the length dependence of K_0
SL2K	$V^{1/2}m^2$	0	0	Second coefficient of the length dependence of K
LP1	M	1E-6	1E-6	Characteristic length of first profile
FBET1	-	0	0	Relative mobility decrease due to first profile
LP2	M	1E-8	1E-8	Characteristic length of second profile
FBET2	-	0	0	Relative mobility decrease due to second profile

Name	Unit	Default (N)	Default (P)	Description
GTHE1	-	0	0	Parameter that selects either the old (=0) or the new(=1) scaling rule of θ_1
SL2GAMOO	-	0	0	Second coefficient of the length dependence Υ_{00}

JUNCAP Model Parameters

Name	Unit	Default	Description
JUNCAP	-	0	JUNCAP flag: 0-off, 1-on
DTA	^{o}c	0.0	Temperature offset of the JUNCAP element with respect to T_A
VR	V	0.0	Voltage at which the parameters have been determined
JSGBR	$A*m^{-2}$	1.00e-3	Bottom saturation-current density due to electron-hole generation at $V=V_R$
JSDBR	$A*m^{-2}$	1.00e-3	Bottom saturation-current density due to diffusion from back contact
JSGSR	$A*m^{-1}$	1.00e-3	Sidewall saturation-current density due to electron-hole generation at $V=V_R$
JSDSR	$A*m^{-1}$	1.00e-3	Sidewall saturation-current density due to diffusion from back contact
JSGGR	$A*m^{-1}$	1.00e-3	Gate edge saturation-current density due to electron-hole generation at $V=V_R$
JSDGR	$A*m^{-1}$	1.00e-3	Gate edge saturation-current density due to diffusion from back contact

Name	Unit	Default	Description
NB	-	1.00	Emission coefficient of the bottom forward current
NS	-	1.00	Emission coefficient of the sidewall forward current
NG	-	1.00	Emission coefficient of the gate edge forward current
CJBR	$F*m^{-2}$	1.00e-12	Bottom junction capacitance at $V=V_R$
CJSR	$F*m^{-1}$	1.00e-12	Sidewall junction capacitance at $V=V_R$
CJGR	$F*m^{-1}$	1.00e-12	Gate edge junction capacitance at $V=V_R$
VDBR	v	1.00	Diffusion voltage of the bottom junction at $T=T_R$
VDSR	v	1.00	Diffusion voltage of the sidewall junction at $T=T_R$
VDGR	v	1.00	Diffusion voltage of the gate edge junction at $T=T_R$
PB	-	0.40	Bottom-junction grading coefficient
PS	-	0.40	Sidewall-junction grading coefficient
PG	-	0.40	Gate edge-junction grading coefficient

Using the Philips MOS9 Model

1. Set Level=50 to identify the model as the Philips MOS Model 9.
2. The default room temperature is 25 ^oC in the Avant! model, but is 27 ^oC in most other simulators. When comparing to other simulators, set the simulation temperature to 27 with .TEMP 27 or with .OPTION TNOM=27.

3. The model parameter set should always include the model reference temperature, TR, which corresponds to TREF in other model levels. The default for TR is 21.0 ^{o}C, to match the Philips simulator.
4. The model has its own charge-based capacitance model. The CAPOP parameter, which selects different capacitance models, is ignored for this model.
5. The model uses analytical derivatives for the conductances. The DERIV parameter, which selects the finite difference method, is ignored for this model.
6. DTEMP can be used with this model. It is set on the element line and increases the temperature of individual elements relative to the circuit temperature.
7. Since defaults are nonzero, it is strongly recommended that every model parameter listed in Level 50 Model Parameters table be set in the .MODEL statement.
8. Use the model parameter JUNCAP to select one of two available parasitic junction diode models, ACM and JUNCAP. JUNCAP=1 selects the Philips JUNCAP model, JUNCAP=0 (default) selects the ACM model.

Model Statement

Example

This is an example of the model statement.

```
.model nch nmos Level=50
+ ler =      1e-6 wer =       10e-6
+ lvar =      0.0 lap =       0.05e-6
+ wvar =      0.0 wot =       0.0
+ tr   =      27.00
+ vtor =      0.8 stvto = 0 slvto = 0 sl2vto= 0
+ swvto =     0
+ kor =      0.7 slko = 0 swko = 0
+ kr   =    0.3 slk = 0 swk = 0
+ phibr   = 0.65
+ vsbxr   = 0.5 slvsbx = 0 swvsbx= 0
+ betsq   = 120e-6
+ etabet =   1.5
+ the1r    =   0.3
```

```
+ stthe1r = 0 slthe1r = 0 stlthe1= 0 swthe1 = 0
+ the2r    =   0.06
+ stthe2r = 0 slthe2r = 0 stlthe2 = 0 swthe2   = 0
+ the3r    = 0.1
+ stthe3r = 0 slthe3r = 0 stlthe3 = 0 swthe3 = 0
+ gam1r    = 0.02   slgam1 = 0 swgam1 = 0
+ etadsr=   0.60
+ alpr =    0.01
+ etaalp = 0 slalp = 0 swalp = 0
+ vpr =     0.4
+ gamoor =   0.006
+ slgamoo = 0
+ etagamr = 2.0
+ mor =   0.5 stmo = 0 slmo = 0
+ etamr = 2.0
+ zet1r = 1.0
+ etazet = 0.5
+ slzet1 = 0
+ vsbtr = 2.5
+ slvsbt = 0
+ a1r = 10   sta1 = 0   sla1 = 0   swa1 = 0
+ a2r = 30   sla2 = 0   swa2 = 0
+ a3r = 0.8 sla3 = 0   swa3 = 0
+ tox = 15.00e-9
+ col = 0.3e-9
+ ntr = 2.0e-20
+ nfr = 5.0e-11
+ acm=2 hdif=1u js=1e-3
+ cj=1e-3 mj=0.5 pb=0.8
+ cjsw=1e-9 cjgate=1e-9 mjsw=0.3 php=0.8
```

Level 54 BSIM4.0 Model

UC Berkeley BSIM4.0 model is developed to explicitly address many issues in modeling sub-0.13 micron CMOS technology and RF high-speed CMOS circuit simulation. The BSIM4.0.0 MOS model for UC Berkeley is available as the Level 54 model.

BSIM4.0 has the following major improvements and additions over BSIM3v3:

- An accurate new model of the intrinsic input resistance (Rii) for both RF, high-frequency analog, and high-speed digital applications
- A flexible substrate resistance network for RF modeling
- A new accurate channel thermal noise model and a noise partition model for the induced gate noise
- A non-quasi-static (NQS) model consistent with the Rii-based RF model and a consistent AC model that accounts for the NQS effect in both transconductances and capacitances
- An accurate gate direct tunneling model
- A comprehensive and versatile geometry-dependent parasitics model for various source/drain connections and multi-finger devices
- An improved model for steep vertical retrograde doping profiles
- A better model for pocket-implanted devices in Vth, bulk charge effect model, and Rout
- An asymmetrical and bias-dependent source/drain resistance, either internal or external to the intrinsic MOSFET, at the user's discretion
- An acceptance of either the electrical or physical gate oxide thickness as the model input (at the user's choice) in a physically accurate manner
- The quantum mechanical charge-layer-thickness model for both IV and CV
- A more accurate mobility model for predictive modeling
- A gate-induced drain leakage (GIDL) current model, available in BSIM for the first time
- An improved unified flicker (1/f) noise model, which is smooth over all bias regions and considers the bulk charge effect
- Different diode IV and CV characteristics for source and drain junctions
- A junction diode breakdown with or without current limiting
- A dielectric constant of the gate dielectric as a model parameter

- Can correctly pass parameters from the .option statements into model cards and instance lines, including parameter passing in the .subckt blocks.
- Instance parameters can correctly override the model parameters, including parameter overriding in the .subckt blocks.

Level 54 Model Parameters

Model Selectors/Controllers

Parameter	Default	Binnable	Description
VERSION	4.0.0	NA	Model version number
BINUNIT	1	NA	Binning unit selector
PARAMCHK	1	NA	Switch for parameter value check
MOBMOD	1	NA	Mobility model selector
RDSMOD	0	NA	Bias-dependent source/drain resistance model selector
IGCMOD	0	NA	Gate-to-channel tunneling current model selector
IGBMOD	0	NA	Gate-to-substrate tunneling current model selector
CAPMOD	2	NA	Capacitance model selector
RGATEMOD	0 (no gate resistance)		Gate resistance model selector
RBODYMOD	0 (network off)	NA	Substrate resistance network model selector
TRNQSMOD	0	NA	Transient NQS model selector
ACNQSMOD	0	NA	AC small-signal NQS model selector

Parameter	Default	Binnable	Description
FNOIMOD	1	NA	Flicker noise model selector
TNOIMOD	0	NA	Thermal noise model selector
DIOMOD	1	NA	Source/drain junction diode IV model selector
PERMOD	1	NA	Whether PS/PD includes the gate-edge perimeter
GEOMOD	0 (isolated)	NA	Geometry-dependent parasitics model selector
RGEOMOD	0	NA	Source/drain diffusion resistance and contact model selector

Process Parameters

Parameter	Default	Binnable	Description
EPSROX	3.9 (SiO_2)	No	Gate dielectric constant relative to vacuum
TOXE	3.0e-9m	No	Electrical gate equivalent oxide thickness
TOXP	TOXE	No	Physical gate equivalent oxide thickness
TOXM	TOXE	No	Tox at which parameters are extracted
DTOX	0.0m	No	Defined as (TOXE-TOXP)
XJ	1.5e-7m	Yes	S/D junction depth
GAMMA1 ($\gamma 1$ in equation)	calculated ($V^{1/2}$)	Yes	Body-effect coefficient near the surface

Parameter	Default	Binnable	Description
GAMMA2 ($\gamma 2$ in equation)	calculated ($V^{1/2}$)	Yes	Body-effect coefficient in the bulk
NDEP	1.7e17cm^{-3}	Yes	Channel doping concentration at depletion edge for zero body bias
NSUB	6.0e16cm^{-3}	Yes	Substrate doping concentration
NGATE	0.0cm^{-3}	Yes	Poly Si gate doping concentration
NSD	1.0e20cm^{-3}	Yes	Source/drain doping concentration
VBX	calculated (v)	No	V_{bs} at which the depletion region width equals XT
XT	1.55e-7m	Yes	Doping depth
RSH	0.0ohm/ square	No	Source/drain sheet resistance
RSHG	0.1ohm/ square	No	Gate electrode sheet resistance

Basic Model Parameters

Parameter	Default	Binnable	Description
VTH0 or VTHO	0.7V (NMOS) -0.7V (PMOS)	Yes	Long-channel threshold voltage at V_{bs}=0
VFB	-1.0V	Yes	Flat-band voltage PHIN
PHIN	0.0V	Yes	Non-uniform vertical doping effect on surface potential
K1	0.5$V^{1/2}$	Yes	First-order body bias coefficient
K2	0.0	Yes	Second-order body bias coefficient

Parameter	Default	Binnable	Description
K3	80.0	Yes	Narrow width coefficient
K3B	$0.0V^{-1}$	Yes	Body effect coefficient of K3
W0	2.5e-6m	Yes	Narrow width parameter
LPE0	1.74e-7m	Yes	Lateral non-uniform doping parameter
LPEB	0.0m	Yes	Lateral non-uniform doping effect on K1
VBM	-3.0V	Yes	Maximum applied body bias in VTH0 calculation
DVT0	2.2	Yes	First coefficient of short-channel effect on V_{th}
DVT1	0.53	Yes	Second coefficient of short-channel effect on V_{th}
DVT2	$-0.032V^{-1}$	Yes	Body-bias coefficient of short-channel effect on V_{th}
DVTP0	0.0m	Yes	First coefficient of drain-induced V_{th} shift due to for long-channel pocket devices
DVTP1	$0.0V^{-1}$	Yes	First coefficient of drain-induced V_{th} shift due to for long-channel pocket devices
DVT0W	0.0	Yes	First coefficient of narrow width effect on V_{th} for small channel length

Parameter	Default	Binnable	Description
DVT1W	$5.3e6m^{-1}$	Yes	Second coefficient of narrow width effect on V_{th} for small channel length
DVT2W	$-0.032V^{-1}$	Yes	Body-bias coefficient of narrow width effect for small channel length
U0	$0.067m^2/(Vs)$ (NMOS); $0.025 m^2/(Vs)$ (PMOS)	Yes	Low-field mobility
UA	1.0e-9m/V for MOBMOD=0 and 1; 1.0e-15m/V for MOBMOD=2	Yes	Coefficient of first-order mobility degradation due to vertical field
UB	$1.0e-19m^2/V^2$	Yes	Coefficient of second-order mobility degradation due to vertical field
UC	$-0.0465V^{-1}$ for MOB-MOD=1; $-0.0465e-9 m/V^2$ for MOBMOD=0 and 2	Yes	Coefficient of mobility degradation due to body-bias effect
EU	1.67 (NMOS); 1.0 (PMOS)	No	Exponent for mobility degradation of MOBMOD=2
VSAT	8.0e4m/s	Yes	Saturation velocity
A0	1.0	Yes	Coefficient of channel-length dependence of bulk charge effect

Parameter	Default	Binnable	Description
AGS	$0.0V^{-1}$	Yes	Coefficient of V_{gs} dependence of bulk charge effect
B0	0.0m	Yes	Bulk charge effect coefficient for channel width
B1	0.0m	Yes	Bulk charge effect width offset
KETA	$-0.047V^{-1}$	Yes	Body-bias coefficient of bulk charge effect
A1	$0.0V^{-1}$	Yes	First non-saturation effect parameter
A2	1.0	Yes	Second non-saturation factor
WINT	0.0m	No	Channel-width offset parameter
LINT	0.0m	No	Channel-length offset parameter
DWG	0.0m/V	Yes	Coefficient of gate bias dependence of W_{eff}
DWB	$0.0m/V^{1/2}$	Yes	Coefficient of body bias dependence of W_{eff} bias dependence
VOFF	-0.08V	Yes	Offset voltage in subthreshold region for large W and L
VOFFL	0.0mV	No	Channel-length dependence of VOFF
MINV	0.0	Yes	V_{gsteff} fitting parameter for moderate inversion condition
NFACTOR	1.0	Yes	Subthreshold swing factor

Parameter	Default	Binnable	Description
ETA0	0.08	Yes	DIBL coefficient in subthreshold region
ETAB	$-0.07V^{-1}$	Yes	Body-bias coefficient for the subthreshold DIBL effect
DSUB	DROUT	Yes	DIBL coefficient exponent in subthreshold region
CIT	$0.0F/m^2$	Yes	Interface trap capacitance
CDSC	$2.4e\text{-}4F/m^2$	Yes	Coupling capacitance between source/drain and channel
CDSCB	$0.0F/(Vm^2)$	Yes	Body-bias sensitivity of CDSC
CDSCD	$0.0(F/Vm^2)$	Yes	Drain-bias sensitivity of DCSC
PCLM	1.3	Yes	Channel-length modulation parameter
PDIBLC1	0.39	Yes	Parameter for DIBL effect on Rout
PDIBLC2	0.0086	Yes	Parameter for DIBL effect on Rout
PDIBLCB	$0.0V^{-1}$	Yes	Body bias coefficient of DIBL effect on Rout
DROUT	0.56	Yes	Channel-length dependence of DIBL effect on Rout
PSCBE1	4.24e8V/m	Yes	First substrate current induced body-effect parameter
PSCBE2	1.0e-5m/V	Yes	Second substrate current induced body-effect parameter

Parameter	Default	Binnable	Description
PVAG	0.0	Yes	Gate-bias dependence of Early voltage
DELTA δ (in equation)	0.01V	Yes	Parameter for DC V_{dseff}
FPROUT	$0.0V/m^{0.5}$	Yes	Effect of pocket implant on Rout degradation
PDITS	$0.0V^{-1}$	Yes	Impact of drain-induced V_{th} shift on Rout.
PDITSL	$0.0m^{-1}$	No	Channel-length dependence of drain-induced V_{th} shift for Rout.
PDITSD	$0.0V^{-1}$	Yes	Vds dependence of drain-induced V_{th} shift for Rout

Parameters for Asymmetric and Bias-Dependent R_{ds} Model

Parameter	Default	Binnable	Description
RDSW	$200.0\ ohm(\mu m)^{WR}$	Yes	Zero bias LLD resistance per unit width for RDSMOD=0
RDSWMIN	$0.0\ ohm(\mu m)^{WR}$	No	LDD resistance per unit width at high V_{gs} and zero V_{bs} for RDSMOD=0
RDW	$100.0\ ohm(\mu m)^{WR}$	Yes	Zero bias lightly-doped drain resistance $R_d(v)$ per unit width for RDSMOD=1
RDWMIN	$0.0\ ohm(\mu m)^{WR}$	No	Lightly-doped drain resistance per unit width at high V_{gs} and zero V_{bs} for RDSMOD=1

Parameter	Default	Binnable	Description
RSW	100.0 ohm(μm)^{WR}	Yes	Zero bias lightly-doped source resistance $R_s(V)$ per unit width for RDSMOD=1
RSWMIN	0.0 ohm(μm)^{WR}	No	Lightly-doped source resistance per unit width at high V_{gs} and zero V_{bs} for RDSMOD=1
PRWG	1.0V^{-1}	Yes	Gate-bias dependence of LDD resistance
PRWB	0.0V$^{-0.5}$	Yes	Body-bias dependence of LDD resistance
WR	1.0	Yes	Channel-width dependence parameter of LDD resistance
NRS	1.0	No	Number of source diffusion squares
NRD	1.0	No	Number of drain diffusion squares

Impact Ionization Current Model Parameters

Parameter	Default	Binnable	Description
ALPHA0	0.0Am/V	Yes	First parameter of impact ionization current
ALPHA1	0.0A/V	Yes	Isub parameter for length scaling
BETA0	30.0V	Yes	The second parameter for impact ionization current

Gate-Induced Drain Leakage Model Parameters

Parameter	Default	Binnable	Description
AGIDL	0.0ohm	Yes	Pre-exponential coefficient for GIDL
BGIDL	2.3e9V/m	Yes	Exponential coefficient for GIDL
CGIDL	$0.5V^3$	Yes	Parameter for body-bias effect on GIDL
DGIDL	0.8V	Yes	Fitting parameter for band bending for GIDL

Gate Dielectric Tunneling Current Model Parameters

Parameter	Default	Binnable	Description
AIGBACC	$0.43\ (F_s^2/_g)^{0.5}m^{-1}$	Yes	Parameter for I_{gb} in accumulation
BIGBACC	$0.054\ (F_s^2/_g)^{0.5}\ m^{-1}V^{-1}$	Yes	Parameter for I_{gb} in accumulation
CIGBACC	$0.075V^{-1}$	Yes	Parameter for I_{gb} in accumulation
NIGBACC	1.0	Yes	Parameter for I_{gb} in accumulation
AIGBINV	$0.35\ (F_s^2/_g)^{0.5}m^{-1}$	Yes	Parameter for I_{gb} in inversion
BIGBINV	$0.03\ (F_s^2/_g)^{0.5}m^{-1}V^{-1}$	Yes	Parameter for I_{gb} in inversion
CIGBINV	$0.0006V^{-1}$	Yes	Parameter for I_{gb} in inversion
EIGBINV	1.1V	Yes	Parameter for I_{gb} in inversion
NIGBINV	3.0	Yes	Parameter for I_{gb} in inversion
AIGC	0.054 (NMOS) and 0.31 (PMOS) $(F_s^2/_g)^{0.5}m^{-1}$	Yes	Parameter for I_{gcs} and I_{gcd}

Parameter	Default	Binnable	Description
BIGC	0.054 (NMOS) and 0.024 (PMOS) $(F_s^2/_g)^{0.5}$ $m^{-1}V^{-1}$	Yes	Parameter for I_{gcs} and I_{gcd}
CIGC	0.075 (NMOS) and 0.03(PMOS) V^{-1}	Yes	Parameter for I_{gcs} and I_{gcd}
AIGSD	0.43 (NMOS) and 0.31 (PMOS) $(F_s^2/_g)^{0.5}$ m^{-1}	Yes	Parameter for I_{gs} and I_{gd}
BIGSD	0.054 (NMOS) 0.024 (PMOS) $(F_s^2/_g)^{0.5}$ $m^{-1}V^{-1}$	Yes	Parameter for I_{gs} and I_{gd}
CIGSD	0.075 (NMOS) and 0.03 (PMOS) V^{-1}	Yes	Parameter for I_{gs} and I_{gd}
DLCIG	LINT	Yes	Source/drain overlap length for Igs and Igd
NIGC	1.0	Yes	Parameter for I_{gcs}, I_{gcd}, I_{gs} and I_{gd}
POXEDGE	1.0	Yes	Factor for the gate oxide thickness in source/drain overlap regions
PIGCD	1.0	Yes	V_{ds} dependence of I_{gcs} and I_{gcd}
NTOX	1.0	Yes	Exponent for the gate oxide ratio
TOXREF	3.0e-9m	No	Nominal gate oxide thickness for gate dielectric tunneling current model only

Charge and Capacitance Model Parameters

Parameter	Default	Binnable	Description
XPART	0.0	No	Charge partition parameter
CGSO	calculated (F/m)	No	Non LDD region source-gate overlap capacitance per unit channel width
CGDO	calculated (F/m)	No	Non LDD region drain-gate overlap capacitance per unit channel width
CGBO	0.0 (F/m)	No	Gate-bulk overlap capacitance per unit channel length
CGSL	0.0F/m	Yes	Overlap capacitance between gate and lightly-doped source region
CGDL	0.0F/m	Yes	Overlap capacitance between gate and lightly-doped source region
CKAPPAS	0.6V	Yes	Coefficient of bias-dependent overlap capacitance for the source side
CKAPPAD	CKAPPAS	Yes	Coefficient of bias-dependent overlap capacitance for the drain side
CF	calculated (F/m)	Yes	Fringing field capacitance
CLC	1.0e-7m	Yes	Constant term for short channel model
CLE	0.6	Yes	Exponential term for short channel model
DLC	LINT (m)	No	Channel-length offset parameter for CV model
DWC	WINT (m)	No	Channel-width offset parameter for CV model

Parameter	Default	Binnable	Description
VFBCV	-1.0V	Yes	Flat-band voltage parameter (for CAPMOD=0 only)
NOFF	1.0	Yes	CV parameter in $V_{gsteff,CV}$ for week to strong inversion
VOFFCV	0.0V	Yes	CV parameter in $V_{gsteff,CV}$ for week to strong inversion
ACDE	1.0m/V	Yes	Exponential coefficient for charge thickness in CAPMOD=2 for accumulation and depletion regions
MOIN	15.0	Yes	Coefficient for the gate-bias dependent surface potential

High-Speed/RF Model Parameters

Parameter	Default	Binnable	Description
XRCRG1	12.0	Yes	Parameter for distributed channel-resistance effect for both intrinsic-input resistance and charge-deficit NQS models
XRCRG2	1.0	Yes	Parameter to account for the excess channel diffusion resistance for both intrinsic input resistance and charge-deficit NQS models
RBPB	50.0ohm	No	Resistance connected between bNodePrime and bNode
RBPD	50.0ohm	No	Resistance connected between bNodePrime and dbNode

Parameter	Default	Binnable	Description
RBPS	50.0ohm	No	Resistance connected between bNodePrime and sbNode
RBDB	50.0ohm	No	Resistance connected between dbNode and dbNode
RBSB	50.0ohm	No	Resistance connected between sbNode and bNode
GBMIN	1.0e-12mho	No	Conductance in parallel with each of the five substrate resistances to avoid potential numerical instability due to unreasonably too large a substrate resistance

Flicker and Thermal Noise Model Parameters

Parameter	Default	Binnable	Description
NOIA	6.25e41 $(eV)^{-1}s^{1-EF}m^{-3}$ for NMOS; 6.188e40 $(eV)^{-1}s^{1-EF}m^{-3}$ for PMOS	No	Flicker noise parameter A
NOIB	3.125e26 $(eV)^{-1}s^{1-EF}m^{-1}$ for NMOS; 1.5e25 $(eV)^{-1}s^{1-EF}m^{-1}$ for PMOS	No	Flicker noise parameter B
NOIC	8.75 $(eV)^{-1}S^{1-EF}m$	No	Flicker noise parameter C
EM	4.1e7V/m	No	Saturation field
AF	1.0	No	Flicker noise exponent
EF	1.0	No	Flicker noise frequency exponent

Parameter	Default	Binnable	Description
KF	0.0 $A^{2-EF}s^{1-EF}F$	No	Flicker noise coefficient
NTNOI	1.0	No	Noise factor for short-channel devices for TNOIMOD=0 only
TNOIA	1.5	No	Coefficient of channel-length dependence of total channel thermal noise
TNOIB	3.5	No	Channel-length dependence parameter for channel thermal noise partitioning

Layout-Dependent Parasitics Model Parameters

Parameter	Default	Binnable	Description
DMCG	0.0m	No	Distance from S/D contact center to the gate edge
DMCI	DMCG	No	Distance from S/D contact center to the isolation edge in the channel-length direction
DMDG	0.0m	No	Same as DMCG, but merged device only
DMCGT	0.0m	No	DMCG of test structures
NF	1	No	Number of device figures
DWJ	DWC (in CVmodel)	No	Offset of the S/D junction width
MIN	0	No	Whether to minimize the number of drain or source diffusions for even-number fingered device

Parameter	Default	Binnable	Description
XGW	0.0m	No	Distance from the gate contact to the channel edge
XGL	0.0m	No	Offset of the gate length due to variations in patterning
NGCON	1	No	Number of gate contacts

Asymmetric Source/Drain Junction Diode Model Parameters

Parameter	Default	Binnable	Description
IJTHSREV	IJTHSREV=0.1A	No	Limiting current in reverse bias region
IJTHDREV	IJTHDREV= IJTHSREV	No	Limiting current in reverse bias region
IJTHSFWD	IJTHSFWD=0.1A	No	Limiting current in forward bias region
IJTHDFWD	IJTHDFWD= IJTHSFWD	No	Limiting current in forward bias region
XJBVS	XJBVS=1.0	No	Fitting parameter for diode breakdown
XJBVD	XJBVD=XJBVS	No	Fitting parameter for diode breakdown
BVS	BVS=10.0V	No	Breakdown voltage
BVD	BVD=BVS	No	Breakdown voltage
JSS	JSS=1.0e-4A/m^2	No	Bottom junction reverse saturation current density
JSD	JSD=JSS	No	Bottom junction reverse saturation current density
JSWS	JSWS=0.0A/m	No	Isolation-edge sidewall reverse saturation current density

Parameter	Default	Binnable	Description
JSWD	JSWD=JSWS	No	Isolation-edge sidewall reverse saturation current density
JSWGS	JSWGS=0.0A/m	No	Gate-edge sidewall reverse saturation current density
JSWGD	JSWGD=JSWGS	No	Gate-edge sidewall reverse saturation current density
CJS	CJS=5.0e-4 F/m^2	No	Bottom junction capacitance per unit area at zero bias
CJD	CJD=CJS	No	Bottom junction capacitance per unit area at zero bias
MJS	MJS=0.5	No	Bottom junction capacitance grading coefficient
MJD	MJD=MJS	No	Bottom junction capacitance grading coefficient
MJSWS	MJSWS=0.33	No	Isolation-edge sidewall junction capacitance grading coefficient
MJSWD	MJSWD=MJSWS	No	Isolation-edge sidewall junction capacitance grading coefficient
CJSWS	CJSWS=5.0e-10 F/m	No	Isolation-edge sidewall junction capacitance per unit area
CJSWD	CJSWD=CJSWS	No	Isolation-edge sidewall junction capacitance per unit area
CJSWGS	CJSWGS=CJSWS	No	Gate-edge sidewall junction capacitance per unit length
CJSWGD	CJSWGD=CJSWS	No	Gate-edge sidewall junction capacitance per unit length
MJSWGS	MJSWGS=MJSWS	No	Gate-edge sidewall junction capacitance grading coefficient

Parameter	Default	Binnable	Description
MJSWGD	MJSWGD=MJSWS	No	Gate-edge sidewall junction capacitance grading coefficient
PBS	PBS=1.0V	No	Bottom junction built-in potential
PBD	PBD=PBS	No	Bottom junction built-in potential
PBSWS	PBSWS=1.0V	No	Isolation-edge sidewall junction built-in potential
PBSWD	PBSWD=PBSWS	No	Isolation-edge sidewall junction built-in potential
PBSWGS	PBSWGS=PBSWS	No	Gate-edge sidewall junction built-in potential
PBSWGD	PBSWGD=PBSWS	No	Gate-edge sidewall junction built-in potential

Temperature Dependence Parameters

Parameter	Default	Binnable	Description
TNOM	27°C	No	Temperature at which parameters are extracted
UTE	-1.5	Yes	Mobility temperature exponent
KT1	-0.11V	Yes	Temperature coefficient for threshold voltage
KT1L	0.0Vm	Yes	Channel length dependence of the temperature coefficient for threshold voltage
KT2	0.022	Yes	Body-bias coefficient of *Vth* temperature effect
UA1	1.0e-9m/V	Yes	Temperature coefficient for UA

Parameter	Default	Binnable	Description
UB1	-1.0e-18 (m/V^2)	Yes	Temperature coefficient for UB
UC1	$0.067V^{-1}$ for MOBMOD=1; $0.025m/V^2$ for MOBMOD=0 and 2	Yes	Temperature coefficient for UC
AT	3.3e4m/s	Yes	Temperature coefficient for saturation velocity
PRT	0.0ohm-m	Yes	Temperature coefficient for Rdsw
NJS, NJD	NJS=1.0; NJD=NJS	No	Emission coefficients of junction for source and drain junctions, respectively
XTIS, XTID	XTIS=3.0; XTID=XTIS	No	Junction current temperature exponents for source and drain junction, respectively
TPB	0.0V/K	No	Temperature coefficient of PB
TPBSW	0.0V/K	No	Temperature coefficient of PBSW
TPBSWG	0.0V/K	No	Temperature coefficient of PBSWG
TCJ	$0.0K^{-1}$	No	Temperature coefficient of CJ
TCJSW	$0.0K^{-1}$	No	Temperature coefficient of CJSW
TCJSWG	$0.0K^{-1}$	No	Temperature coefficient of CJSWG

dW and *dL* Parameters

Parameter	Default	Binnable	Description
WL	$0.0m^{WLN}$	No	Coefficient of length dependence for width offset
WLN	1.0	No	Power of length dependence of width offset
WW	$0.0m^{WWN}$	No	Coefficient of width dependence for width offset
WWN	1.0	No	Power of width dependence of width offset
WWL	$0.0\ m^{WWN+WLN}$	No	Coefficient of length and width cross term dependence for width offset
LL	$0.0m^{LLN}$	No	Coefficient of length dependence for length offset
LLN	1.0	No	Power of length dependence for length offset
LW	$0.0m^{LWN}$	No	Coefficient of width dependence for length offset
LWN	1.0	No	Power of width dependence for length offset
LWL	$0.0\ m^{LWN+LLN}$	No	Coefficient of length and width cross term dependence for length offset
LLC	LL	No	Coefficient of length dependence for CV channel length offset
LWC	LW	No	Coefficient of width dependence for CV channel length offset

Parameter	Default	Binnable	Description
LWLC	LWL	No	Coefficient of length and width cross-term dependence for CV channel length offset
WLC	WL	No	Coefficient of length dependence for CV channel width offset
WWC	WW	No	Coefficient of width dependence for CV channel width offset
WWLC	WWL	No	Coefficient of length and width cross-term dependence for CV channel width offset

Range Parameters for Model Application

Parameter	Default	Binnable	Description
LMIN	0.0m	No	Minimum channel length
LMAX	1.0m	No	Maximum channel length
WMIN	0.0m	No	Minimum channel width
WMAX	1.0m	No	Maximum channel width

Level 55 EPFL-EKV MOSFET Model

The EPFL-EKV MOSFET model is a scalable and compact simulation model built on fundamental physical properties of the MOS structure. This model is dedicated to the design and simulation of low-voltage, low-current analog, and mixed analog-digital circuits using submicron CMOS technologies.

This section provides a description of the equations and parameters used for the computer simulation version of the EPFL-EKV MOSFET model. The description concentrates on the intrinsic part of the MOSFET, and is intended to give the model user information on parameter handling and the actual equations used in the computer simulation.

The extrinsic part of the MOSFET is handled as it is often made for other MOSFET models. The extrinsic model includes the series resistances of the source and drain diffusions, which are handled as external elements, as well as junction currents and capacitances.

Single Equation Model

The EPFL-EKV MOSFET model is in principle formulated as a ‘single expression’, which preserves continuity of first- and higher-order derivatives with respect to any terminal voltage, in the entire range of validity of the model. The analytical expressions of first-order derivatives as transconductances and transcapacitances are not presented in this section but are also available for computer simulation.

Effects Modeled

The EPFL-EKV MOSFET model version 2.6 includes modeling of the following physical effects:

- Basic geometrical and process related aspects as oxide thickness, junction depth, effective channel length and width
- Effects of doping profile, substrate effect
- Modeling of weak, moderate, and strong inversion behavior

- Modeling of mobility effects due to vertical and lateral fields, velocity saturation
- Short-channel effects as channel-length modulation (CLM), source and drain charge-sharing (including for narrow channel widths), reverse short channel effect (RSCE)
- Modeling of substrate current due to impact ionization
- Quasi-static charge-based dynamic model
- Thermal and flicker noise modeling
- First-order non-quasi-static model for the transadmittances
- Short-distance geometry- and bias-dependent device matching.

Coherence of Static and Dynamic Models

All aspects regarding the static, the quasi-static and non-quasi-static dynamic and noise models are all derived in a coherent way from a single characteristic, the normalized transconductance-to-current ratio. Symmetric normalized forward and reverse currents are used throughout these expressions. For quasi-static dynamic operation, both a charge-based model for the node charges and trans-capacitances, and a simpler capacitances model are available. The dynamic model, including the time constant for the nonquasi-static model, is described in symmetrical terms of the forward and reverse normalized currents. The charge formulation is further used to express effective mobility dependence of local field.

Bulk Reference and Symmetry

Voltages are all referred to the local substrate:

$V_G = V_{GB}$ Intrinsic gate-to-bulk voltage

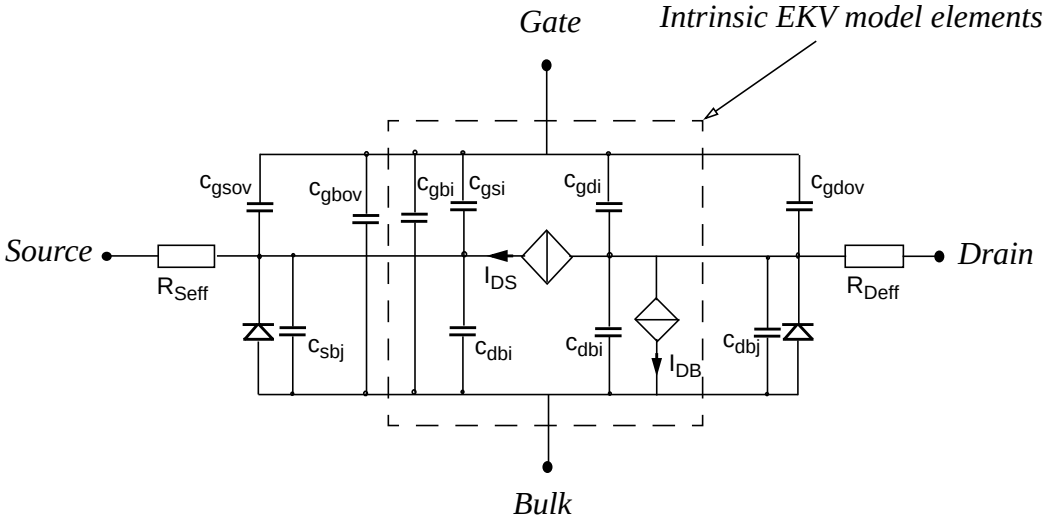
$V_S = V_{SB}$ Intrinsic source-to-bulk voltage

$V_D = V_{DB}$ Intrinsic drain-to-bulk voltage

V_S and V_D are the intrinsic source and drain voltages, which means that the voltage drop over extrinsic resistive elements is supposed to have already been accounted for externally. V_D is the electrical drain voltage, and is chosen such that $V_D \geq V_S$. Bulk reference allows the model to be handled symmetrically with respect to source and drain, a symmetry that is inherent in common MOS technologies (excluding non-symmetric source-drain layouts).

Note: Intrinsic model equations are presented for an N-channel MOSFET. P-channel MOSFETs are dealt with as pseudo-N-channel, i.e. the polarity of the voltages (V_G, V_S, V_D, as well as *VFB*, *VTO* and *TCV*) is reversed prior to computing the current for P-channel, which is given a negative sign. No other distinctions are made between N-channel and P-channel, with the exception of the η factor for effective mobility calculation.

Equivalent Circuit



This figure represents the intrinsic and extrinsic elements of the MOS transistor. For quasi-static dynamic operation, only the intrinsic capacitances from the simpler capacitances model are shown here. However, a charge-based transcapacitances model is also available for computer simulation.

Device Input Variables

Name	Unit	Default	Description
L	m	-	Channel length
W	m	-	Channel width
M or NP	-	1.0	Parallel multiple device number
N or NS	-	1.0	Series multiple device number

EKV Intrinsic Model Parameters

Process Related Parameters

Name	Unit	Default	Range	Description
COX[a]	F/m^2	0.7E-3	-	Gate oxide capacitance per unit area
XJ	m	0.1E-6	$\geq$ 1.0E-9	Junction depth
DW[b]	m	0	-	Channel width correction
DL	m	0	-	Channel length correction

a. The default value of COX can be calculated as a function of TOX.

b. DL and DW parameters usually have a negative value; see effective length and width calculation.

Basic Intrinsic Model Parameters

Name	Unit	Default[a]	Range	Description
VTO[b]	V	0.5	-	Long-channel threshold voltage
GAMMA	$\sqrt{V}$	1.0	≥ 0	Body effect parameter
PHI	V	0.7	≥ 0.1	Bulk Fermi potential (*2)
KP	A/V^2	50.0E-6	-	Transconductance parameter
E0 (EO)	V/m	1.0E12	≥ 1E5	Mobility reduction coefficient
UCRIT	V/m	2.0E6	≥ 1E5	Longitudinal critical field

a. The default values of VTO, GAMMA, PHI, KP can be calculated as function of TOX, NSUB, UO,VFB for the purpose of statistical circuit simulation.

b. As V_G, VTO is also referred to the bulk.

Optional Parameters

The following parameters accommodate scaling behavior of the process and basic intrinsic model parameters, as well as statistical circuit simulation. Note that the parameters `TOX`, `NSUB`, `VFB`, `UO`, and `VMAX` are only used if `COX`, `GAMMA` and/or `PHI`, `VTO`, `KP` and `UCRIT` are *not* specified, respectively. Further, a simpler mobility reduction model due to vertical field is accessible. The mobility reduction coefficient `THETA` is only used if E0 is *not* specified.

Name	Unit[a]	Default	Range	Description
TOX[b]	m	-	≥ 0	Oxide thickness
NSUB[c]	cm^{-3}	-	≥ 0	Channel doping
VFB[d]	V	-	-	Flat-band voltage
UO[e]	$cm^2/(Vs)$	-	≥ 0	Low-field mobility

Name	Unit[a]	Default	Range	Description
VMAX[f]	m/s	-	≥ 0	Saturation velocity
THETA[g]	1/V	0	≥ 0	Mobility reduction coefficient

a. In this example, cm is the basic unit for NSUB and UO, while TOX and VMAX are in m

b. Optional parameter used to calculate COX.

c. Optional parameter accounting for the dependence of GAMMA on COX, as well as for calculation of PHI.

d. Optional parameter used to calculate VTO as a function of COX, GAMMA, PHI.

e. Optional parameter accounting for the dependence of KP on COX.

f. Optional parameter used to calculate UCRIT.

g. Optional parameter for mobility reduction due to vertical field.

Channel Length Modulation and Charge Sharing Parameters

Name	Unit	Default	Range	Description
LAMBDA	-	0.5	≥ 0	Depletion length coefficient (channel length modulation)
WETA	-	0.25	-	Narrow-channel effect coefficient
LETA	-	0.1	-	Short-channel effect coefficient

Reverse Short-channel Effect Parameters

Name	Unit	Default	Range	Description
Q0 (QO)	$A \cdot s/m^2$	0	-	Reverse short channel effect peak charge density
LK	m	0.29E-6	≥ 1.0E-8	Reverse short channel effect characteristic length

Impact Ionization Related Parameters

Name	Unit	Default	Range	Description
IBA	1/m	0	-	First impact ionization coefficient
IBB	V/m	3.0E8	≥ 1.0E8	Second impact ionization coefficient
IBN	-	1.0	≥ 0.1	Saturation voltage factor for impact ionization

Intrinsic Model Temperature Parameters

Name	Unit	Default	Description
TCV	V/K	1.0E-3	Threshold voltage temperature coefficient
BEX	-	-1.5	Mobility temperature exponent
UCEX	-	0.8	Longitudinal critical field temperature exponent
IBBT	1/K	9.0E-4	Temperature coefficient for IBB

Matching Parameters

Name	Unit	Default	Description
AVTO	Vm	0[a]	Area related threshold voltage mismatch parameter
AKP	m	0	Area related gain mismatch parameter
AGAMMA	$\sqrt{}$Vm	0	Area related body effect mismatch parameter

a. Only DEV values are applicable to the statistical matching parameters (AVTO, AGAMMA, AKP) for Monte-Carlo type simulations. Default is 1E-6 for all three parameters in some implementations, to allow sensitivity analysis on the matching parameters. LOT specifications should not be used for AVTO, AGAMMA, AKP.

Flicker Noise Parameters

Name	Unit	Default	Description
KF	-[a]	0	Flicker noise coefficient
AF	-	1	Flicker noise exponent

a. Unit of KF may depend on flicker noise model chosen if options are available.

Setup Parameters

Name	Unit	Default	Description
NQS[a]	-	0	Non-Quasi-Static (NQS) operation switch
SATLIM[b]	-	exp(4)	Ratio defining the saturation limit i_f/i_r

Name	Unit	Default	Description
XQC[c]	-	0.4	Charge/capacitance model selector

a. NQS=1 switches Non-Quasi-Static operation on, default is off (NQS model option may not be available in all implementations).

b. Only used for operating point information. (SATLIM option may not be available in all implementations).

c. Selector for charges/transcapacitances (default) or capacitances only model. XQC=0.4: charges/transcapacitances model; XQC=1: capacitances only model. (XQC model option may not be available in all implementations).

Static Intrinsic Model Equations

Basic Definitions

$$\varepsilon_{si} = SCALE \cdot 104.5\times10^{-12}[F/m] \qquad \text{Permittivity of silicon}$$

$$\varepsilon_{ox} = SCALE \cdot 34.5\times10^{-12}[F/m] \qquad \text{Permittivity of silicon dioxide}$$

$q = 1.602\times10^{-19}[C]$ Magnitude of electron charge

$k = 1.3807\times10^{-23}[JK^{-1}]$ Boltzmann constant

$T_{ref} = 300.15[K]$ Reference temperature

T_{nom} [K] Nominal temperature of model parameters

T [K] Model simulation temperature

$$V_t(T) = \frac{k \cdot T}{q} \qquad \text{Thermal voltage}$$

$$E_g(T) = \left(1.16 - 0.000702 \cdot \frac{T^2}{T + 1108}\right)[eV] \qquad \text{Energy gap}$$

$$n_i(T) = 1.45\times10^{16}\cdot\left(\frac{T}{T_{ref}}\right)\cdot\exp\left(\frac{E_g(T_{ref})}{2\cdot V_t(T_{ref})}-\frac{E_g(T)}{2\cdot V_t(T)}\right)[m^{-3}]$$ Intrinsic carrier concentration

Parameter Preprocessing

Handling of Model Parameters for P-channel MOSFETs

For P-channel devices, the sign of VFB, VTO and TCV is inversed before processing. Therefore, VTO and TCV are usually positive and VFB negative for N-channel, and vice versa for P-channel MOSFETs.

Intrinsic Parameters Initialization

The basic intrinsic model parameters COX, GAMMA, PHI, VTO, KP and UCRIT are related to the fundamental process parameters TOX, NSUB, VFB, UO, VMAX, respectively, similarly as in early SPICE models. For the purpose of statistical circuit simulation, it is desirable to introduce parameter variations on the level of the latter parameters. These dependencies are also of interest if device scaling is to be analyzed, and are useful when parameter sets should be obtained from other MOSFET models. Therefore, the possibility is introduced to use the following relations:

If COX is not specified, then it is initialized as:

$$\mathrm{COX} = \begin{cases} \varepsilon_{ox}/\mathrm{TOX} & \text{for: } \mathrm{TOX} > 0 \\ \text{default} & \text{otherwise} \end{cases}$$

If GAMMA is not specified, then it is initialized as:

$$\mathrm{GAMMA} = \begin{cases} \dfrac{\sqrt{2q\varepsilon_{si}\cdot(\mathrm{NSUB}\cdot10^{6})}}{\mathrm{COX}} & \text{for: } \mathrm{NSUB} > 0 \\ \text{default} & \text{otherwise} \end{cases}$$

If PHI is not specified, then it is initialized as:

$$\mathtt{PHI} = \begin{cases} 2V_t(T_{nom}) \cdot \ln\left(\dfrac{\mathtt{NSUB} \cdot 10^6}{n_i(T_{nom})}\right) & \text{for: } \mathtt{NSUB} > 0 \\ \text{default} & \text{otherwise} \end{cases}$$

If VTO is not specified, then it is initialized as:

$$\mathtt{VTO} = \begin{cases} \mathtt{VFB} + \mathtt{PHI} + \mathtt{GAMMA} \cdot \sqrt{\mathtt{PHI}} & \text{if VFB specified} \\ \text{default} & \text{otherwise} \end{cases}$$

If DP is not specified, then it is initialized as:

$$\mathtt{KP} = \begin{cases} (\mathtt{UO} \cdot 10^{-4}) \cdot \mathtt{COX} & \text{for: } \mathtt{UO} > 0 \\ \text{default} & \text{otherwise} \end{cases}$$

If UCRIT is not specified, then it is initialized as:

$$\mathtt{UCRIT} = \begin{cases} \mathtt{VMAX}/(\mathtt{UO} \cdot 10^{-4}) & \text{for: } \mathtt{VMAX} > 0, \mathtt{UO} > 0 \\ \text{default} & \text{otherwise} \end{cases}$$

If E0 is not specified, then a simplified mobility model is used with the parameter THETA:

$$\mathtt{E0} = \begin{cases} 0 & \text{if THETA specified} \\ \text{default} & \text{otherwise} \end{cases}$$

Note: The value zero is given to *E0* here, indicating that the simplified mobility model is used in conjunction with *THETA* instead of the standard mobility model.

Optional parameters might not be available in all implementations.

Default Values and Parameter Ranges

Model parameters that are not defined in the model parameter sets are either initialized according to the above relations, or set to their default values. For certain parameters, their numerical range has to be restricted to avoid numerical problems such as divisions by zero. If a parameter given in a parameter set falls outside the specified range (see range column in the parameter tables) then its value is set to the closest acceptable value.

Intrinsic Parameters Temperature Dependence

$$\mathtt{VTO}(T) = \mathtt{VTO} - \mathtt{TCV} \cdot (T - T_{nom})$$

$$\mathtt{KP}(T) = \mathtt{KP} \cdot \left(\frac{T}{T_{nom}}\right)^{\mathtt{BEX}}$$

$$\mathtt{UCRIT}(T) = \mathtt{UCRIT} \cdot \left(\frac{T}{T_{nom}}\right)^{\mathtt{UCEX}}$$

$$\mathtt{PHI}(T) = \mathtt{PHI} \cdot \frac{T}{T_{nom}} - 3 \cdot V_t \cdot \ln\left(\frac{T}{T_{nom}}\right) - E_g(T_{nom}) \cdot \frac{T}{T_{nom}} + E_g(T)$$

$$\mathtt{IBB}(T) = \mathtt{IBB} \cdot [1.0 + \mathtt{IBBT} \cdot (T - T_{nom})]$$

Bulk Referenced Intrinsic Voltages

Voltages are all referred to the local substrate (see ‘Bulk Reference and Symmetry” on page 10-91):

$V_G = V_{GB} = V_{GS} - V_{BS}$ Intrinsic gate-to-bulk voltage

$V_S = V_{SB} = -V_{BS}$ Intrinsic source-to-bulk voltage

$V_D = V_{DB} = V_{DS} - V_{BS}$ Intrinsic drain-to-bulk voltage

For P-channel devices, all signs of the above voltages are inverted prior to processing.

Effective Channel Length and Width

$$W_{eff} = W + DW$$

$$L_{eff} = L + DL$$

Note: Contrary to the convention adopted in other MOSFET models, DL and DW usually do have a negative value due to the above definition.

Short Distance Matching

Random mismatch between two transistors with identical layout and close to each other is in most cases suitably described by a law following the inverse of the square root of the transistors' area. The following relationships have been adopted:

$$VTO_a = VTO + \frac{AVTO}{\sqrt{NP \cdot W_{eff} \cdot NS \cdot L_{eff}}}$$

$$KP_a = KP \cdot \left(1 + \frac{AKP}{\sqrt{NP \cdot W_{eff} \cdot NS \cdot L_{eff}}}\right)$$

$$GAMMA_a = GAMMA + \frac{AGAMMA}{\sqrt{NP \cdot W_{eff} \cdot NS \cdot L_{eff}}}$$

These model equations are only applicable in Monte-Carlo and sensitivity simulations.

Note that since negative values for both KP_a and $GAMMA_a$ are not physically meaningful, these are clipped at zero.

Reverse Short-channel Effect (RSCE)

$$C_\varepsilon = 4 \cdot (22 \times 10^{-3})^2 \qquad C_A = 0.028$$

$$\xi = C_A \cdot \left(10 \cdot \frac{L_{eff}}{LK} - 1\right)$$

$$\Delta V_{RSCE} = \frac{2 \cdot Q0}{COX} \cdot \frac{1}{\left[1 + \frac{1}{2} \cdot (\xi + \sqrt{\xi^2 + C_\varepsilon})\right]^2}$$

Effective Gate Voltage Including RSCE

$$V_G' = V_G - VTO_a - \Delta V_{RSCE} + PHI + GAMMA_a\sqrt{PHI}$$

Effective substrate factor including charge-sharing for short and narrow channels

Pinch-off voltage for narrow-channel effect:

$$V_{P0} = \begin{cases} V_G' - PHI - GAMMA_a\left(\sqrt{V_G' + \left(\frac{GAMMA_a}{2}\right)^2} - \frac{GAMMA_a}{2}\right) & \text{for: } V_G' > 0 \\ -PHI & \text{for: } V_G' \le 0 \end{cases}$$

Effective substrate factor accounting for charge-sharing:

$$V'_{S(D)} = \frac{1}{2} \cdot [V_{S(D)} + PHI + \sqrt{(V_{S(D)} + PHI)^2 + (4V_t)^2}]$$

Note: Equation prevents the argument of the square roots in the subsequent code from becoming negative.

$$\gamma^{\circ} = \mathrm{GAMMA}_a - \frac{\varepsilon_{si}}{\mathrm{COX}} \cdot \left[\frac{\mathrm{LETA}}{L_{eff}} \cdot \left(\sqrt{V'_S} + \sqrt{V'_D} \right) - \frac{3 \cdot \mathrm{WETA}}{W_{eff}} \cdot \sqrt{V_{P0} + \mathrm{PHI}} \right]$$

$$\gamma' = \frac{1}{2} \cdot \left(\gamma^{\circ} + \sqrt{\gamma^{\circ 2} + 0.1 \cdot V_t} \right)$$

Note: The purpose of Equation is to prevent the effective substrate factor from becoming negative.

Pinch-off Voltage Including Short- and Narrow-channel Effects

$$V_P = \begin{cases} V_G' - \mathrm{PHI} - \gamma' \cdot \left(\sqrt{V_G' + \left(\frac{\gamma'}{2} \right)^2} - \frac{\gamma'}{2} \right) & \text{for: } V_G' > 0 \\ -\mathrm{PHI} & \text{for: } V_G' \le 0 \end{cases}$$

Note that the pinch-off voltage accounts for channel doping effects such as threshold voltage and substrate effect. For long-channel devices, V_p is a function of gate voltage; for short-channel devices, it becomes also a function of source and drain voltage due to the charge-sharing effect.

Slope Factor

$$n = 1 + \frac{\mathrm{GAMMA}_a}{2 \cdot \sqrt{V_P + \mathrm{PHI} + 4V_t}}$$

Note that the slope factor (or body effect factor), which is primarily a function of the gate voltage, is linked to the weak inversion slope.

Large Signal Interpolation Function

F(v) is the large-signal interpolation function relating the normalized currents to the normalized voltages. A simple and accurate expression for the transconductance-to-current ratio allows a consistent formulation of the static large-signal interpolation function, the dynamic model for the intrinsic charges (and capacitances) as well as the intrinsic time constant and the thermal noise model for the whole range of current from weak to strong inversion:

$$\frac{g_{ms} \cdot V_t}{I_{DS}} = \frac{1}{\sqrt{0.25 + i} + 0.5}$$

Large-signal interpolation function:

$$y = \sqrt{0.25 + i} - 0.5$$

$$v = 2y + \ln(y)$$

Unfortunately, Eqn. cannot be inverted analytically. However, it can be inverted using a Newton-Raphson iterative scheme. Currently, a simplification of this algorithm that avoids iteration is used, leading to a continuous expression for the large signal interpolation function. The (inverted) large signal interpolation function has the following asymptotes in strong and weak inversion respectively:

$$F(v) = \begin{cases} (v/2)^2 & \text{for: } v >> 0 \\ \exp(v) & \text{for: } v << 0 \end{cases}$$

Forward Normalized Current

$$i_f = F\left[\frac{V_P - V_S}{V_t}\right]$$

Velocity Saturation Voltage

$$V_C = \texttt{UCRIT} \cdot \texttt{NS} \cdot L_{eff}$$

Note: Equation accounts for multiple series device number `NS`.

$$V_{DSS} = V_C \cdot \left[\sqrt{\frac{1}{4} + \frac{V_t}{V_C} \cdot \sqrt{i_f}} - \frac{1}{2} \right]$$

Note: The variable V_{DSS} in this formulation for computer simulation is half the value of the actual saturation voltage.

Drain-to-source Saturation Voltage for Reverse Normalized Current

$$V_{DSS}' = V_C \cdot \left[\sqrt{\frac{1}{4} + \frac{V_t}{V_C} \cdot \left(\sqrt{i_f} - \frac{3}{4} \cdot \ln(i_f) \right)} - \frac{1}{2} \right] + V_t \cdot \left[\ln\left(\frac{V_C}{2V_t} \right) - 0.6 \right.$$

Channel-length Modulation

$$\Delta V = 4 \cdot V_t \cdot \sqrt{\texttt{LAMBDA} \cdot \left(\sqrt{i_f} - \frac{V_{DSS}}{V_t} \right) + \frac{1}{64}}$$

$$V_{ds} = \frac{V_D - V_S}{2}$$

$$V_{ip} = \sqrt{V_{DSS}^2 + \Delta V^2} - \sqrt{(V_{ds} - V_{DSS})^2 + \Delta V^2}$$

$$L_C = \sqrt{\frac{\varepsilon_{si}}{\texttt{COX}} \cdot \texttt{XJ}}$$

$$\Delta L = \texttt{LAMBDA} \cdot L_C \cdot \ln\left(1 + \frac{V_{ds} - V_{ip}}{L_C \cdot \texttt{UCRIT}}\right)$$

Equivalent Channel Length Including Channel-length Modulation and Velocity Saturation

$$L' = \texttt{NS} \cdot L_{eff} - \Delta L + \frac{V_{ds} + V_{ip}}{\texttt{UCRIT}}$$

$$L_{min} = \texttt{NS} \cdot L_{eff} / 10$$

Note: Equation and Equation account also for multiple series device number NS.

$$L_{eq} = \frac{1}{2} \cdot (L' + \sqrt{L'^2 + L_{min}^2})$$

Note: Equation prevents the equivalent channel length to become zero or negative.

Reverse Normalized Current

Reverse normalized current:

$$i_r' = F\left[\frac{V_P - V_{ds} - V_S - \sqrt{V_{DSS}'^2 + \Delta V^2} + \sqrt{(V_{ds} - V_{DSS}')^2 + \Delta V^2}}{V_t}\right].$$

Reverse normalized current for mobility model, intrinsic charges/capacitances, thermal noise model and NQS time-constant:

$$i_r = F\left[\frac{V_P - V_D}{V_t}\right]$$

Transconductance Factor and Mobility Reduction Due to Vertical Field

$$\beta_0 = \mathrm{KP}_a \cdot \frac{\mathrm{NP} \cdot W_{eff}}{L_{eq}}$$

Note that the use of the device parameter NP (or M) gives accurate results for simulation of parallel devices, whereas the use of NS (or N) for series devices is only approximate. Note that L_{eq} accounts for multiple series device number NS.

$$\eta = \begin{cases} 1/2 & \text{for NMOS} \\ 1/3 & \text{for PMOS} \end{cases}$$

$$q_{B0} = \mathrm{GAMMA}_a \cdot \sqrt{\mathrm{PHI}}$$

$$\beta_0' = \beta_0 \cdot \left(1 + \frac{\mathrm{COX}}{\mathrm{E0} \cdot \varepsilon_{si}} \cdot q_{B0}\right)$$

$$\beta = \frac{\beta_0'}{1 + \frac{\mathrm{COX}}{\mathrm{E0} \cdot \varepsilon_{si}} \cdot V_t \cdot \left|q_B + \eta \cdot q_I\right|}$$

For the definition of the normalized depletion and inversion charges q_B and q_I refer to the section on the node charges. The use of β_0' ensures that $\beta \approx \beta_0$ when $q_I << q_B$. The formulation of β arises from the integration of the local effective field as a function of depletion and inversion charge densities along the channel. No substrate bias dependency is needed due to the inclusion of depletion charge. Note that the resulting mobility expression also depends on V_{DS} .

Simple Mobility Reduction Model

For compatibility with the former EKV model versions (prior to v2.6), you can choose the simpler mobility reduction model, which uses the THETA parameter.

If you do *not* specify the E0 model parameter (see parameter preprocessing), the simpler mobility model is taken into account according to:

$$V_P' = \frac{1}{2} \cdot (V_P + \sqrt{V_P^2 + 2V_t^2})$$

$$\beta = \frac{\beta_0}{1 + \mathrm{THETA} \cdot V_P'}$$

Specific Current

$$I_S = 2 \cdot n \cdot \beta \cdot V_t^2$$

Drain-to-source Current

$$I_{DS} = I_S \cdot (i_f - i_r')$$

For P-channel devices, I_{DS} is given a negative sign.

Note: This drain current expression is a single equation, valid in all operating regions: weak, moderate and strong inversion, non-saturation and saturation. It is therefore not only continuous among all these regions, but also continuously derivable.

Transconductances

The transconductances are obtained through derivation of the drain current:

$$g_{mg} \equiv \frac{\partial I_{DS}}{\partial V_G} \qquad g_{ms} \equiv -\frac{\partial I_{DS}}{\partial V_S} \qquad g_{md} \equiv \frac{\partial I_{DS}}{\partial V_{DS}}$$

In the following relationships, the source for the derivatives is a reference:

$$g_m \equiv \frac{\partial I_{DS}}{\partial V_{GS}} = g_{mg} \qquad g_{mbs} \equiv \frac{\partial I_{DS}}{\partial V_{BS}} = g_{ms} - g_{mg} - g_{md} \qquad g_{ds} \equiv \frac{\partial I_{DS}}{\partial V_{DS}} = g_{md}$$

The analytic derivatives are available with the model code.

Impact Ionization Current

$$V_{ib} = V_D - V_S - \mathtt{IBN} \cdot 2 \cdot V_{DSS}$$

$$I_{DB} = \begin{cases} I_{DS} \cdot \dfrac{\mathtt{IBA}}{\mathtt{IBB}} \cdot V_{ib} \cdot \exp\left(\dfrac{-\mathtt{IBB} \cdot L_C}{V_{ib}}\right) & \text{for: } V_{ib} > 0 \\ 0 & \text{for: } V_{ib} \le 0 \end{cases}$$

Note that the factor 2 in the expression for V_{ib} accounts for the fact that the numerical value of V_{DSS} is half the actual saturation voltage. Further note that the substrate current is intended to be treated as a component of the total extrinsic drain current, flowing from the drain to the bulk. The total drain current is therefore expressed as $I_D = I_{DS} + I_{DB}$.

The substrate current therefore also affects the total extrinsic conductances, in particular the drain conductance.

Quasi-static Model Equations

Both a charge-based model for transcapacitances, allowing charge-conservation during transient analysis, and a simpler capacitances-based model are available. Note that the charges model is formulated in symmetric terms of the forward and reverse normalized currents, that is, symmetrical for both drain and source sides.

Further note that short-channel effects, as charge-sharing and reverse short-channel effects, are included in the dynamic model through the pinch-off voltage.

Dynamic Model for the Intrinsic Node Charges

$$n_q = 1 + \frac{\mathtt{GAMMA}_a}{2 \cdot \sqrt{V_P + \mathtt{PHI} + 10^{-6}}}$$

Normalized Intrinsic Node Charges:

$$x_f = \sqrt{\frac{1}{4} + i_f}$$

$$x_r = \sqrt{\frac{1}{4} + i_r}$$

$$q_D = -n_q \cdot \left(\frac{4}{15} \cdot \frac{3x_r^3 + 6x_r^2 x_f + 4x_r x_f^2 + 2x_f^3}{(x_f + x_r)^2} - \frac{1}{2} \right)$$

$$q_S = -n_q \cdot \left(\frac{4}{15} \cdot \frac{3x_f^3 + 6x_f^2 x_r + 4x_f x_r^2 + 2x_r^3}{(x_f + x_r)^2} - \frac{1}{2} \right)$$

$$q_I = q_S + q_D = -n_q \cdot \left(\frac{4}{3} \cdot \frac{x_f^2 + x_f x_r + x_r^2}{x_f + x_r} - 1 \right)$$

$$q_B = \begin{cases} (-\mathtt{GAMMA}_a \cdot \sqrt{V_P + \mathtt{PHI} + 10^{-6}}) \cdot \frac{1}{V_t} - \left(\frac{n_q - 1}{n_q} \right) \cdot q_I & \text{for: } V'_G > 0 \\ -V'_G \cdot \frac{1}{V_t} & \text{for: } V'_G \le 0 \end{cases}$$

$$q_G = -q_I - q_{OX} - q_B$$

q_{OX} is a fixed oxide charge assumed to be zero. The above equation expresses the charge conservation among the four nodes of the transistor.

Total Charges:

$$C_{ox} = \mathtt{COX} \cdot \mathtt{NP} \cdot W_{eff} \cdot \mathtt{NS} \cdot L_{eff}$$

$$Q_{(I, B, D, S, G)} = C_{ox} \cdot V_t \cdot q_{(I, B, D, S, G)}$$

Intrinsic Capacitances

Transcapacitances

The intrinsic capacitances are obtained through derivation of the node charges with respect to the terminal voltages:

$$C_{xy} = \pm \frac{\partial}{\partial V_y}(Q_x) \qquad x, y = G, D, S, B$$

where the positive sign is chosen when $x = y$ and the negative sign otherwise. The result is simple, continuous analytical expressions for all transcapacitances in terms of x_f, x_r, the pinch-off voltage and the slope factor, and derivatives thereof, from weak to strong inversion and non-saturation to saturation.

Normalized Intrinsic Capacitances

A simplified capacitive dynamic model, using the five intrinsic capacitances corresponding to the 'Equivalent Circuit" on page 10-92, can be obtained when neglecting the slight bias dependence of the slope factor n, resulting in the following simple functions:

$$c_{gs} = \frac{2}{3} \cdot \left(1 - \frac{x_r^2 + x_r + \frac{1}{2}x_f}{(x_f + x_r)^2} \right)$$

$$c_{gd} = \frac{2}{3} \cdot \left(1 - \frac{x_f^2 + x_f + \frac{1}{2}x_r}{(x_f + x_r)^2} \right)$$

$$c_{gb} = \left(\frac{n_q - 1}{n_q} \right) \cdot (1 - c_{gs} - c_{gd})$$

$$c_{sb} = (n_q - 1) \cdot c_{gs}$$

$$c_{db} = (n_q - 1) \cdot c_{gd}$$

To choose this simplified capacitances model, set `XQC`=1.

Total Intrinsic Capacitances

$$C_{(gs,\ gd,\ gb,\ sb,\ db)} = C_{ox} \cdot c_{(gs,\ gd,\ gb,\ sb,\ db)}$$

Non-Quasi-Static (NQS) Model Equations

The EKV model includes a first order NQS model for small-signal (.AC) simulations. The expression of the NQS drain current is obtained from the quasi-static value of the drain current which is then 1st-order low-pass filtered. NQS is a flag (model parameter) allowing to disable the NQS model and τ is the bias dependent characteristic time constant.

τ_0 is the intrinsic time constant defined as:

$$\tau_0 = \frac{(NS \cdot L_{eff})^2}{2 \cdot \mu_{eff} \cdot V_t} = \frac{C_{ox}}{2 \cdot V_t \cdot \beta}$$

$$\tau = \tau_0 \cdot \frac{4}{15} \cdot \frac{(x_f^2 + 3x_f x_r + x_r^2)}{(x_f + x_r)^3}$$

$$I_{DS}(s) = \frac{I_{DS}}{1 + NQS \cdot s \cdot \tau}$$

The corresponding small-signal (.AC) transadmittances are then given by:

$$Y_{mg}(s) = \frac{g_{mg}}{1 + NQS \cdot s \cdot \tau}$$

$$Y_{ms}(s) = \frac{g_{ms}}{1 + NQS \cdot s \cdot \tau}$$

$$Y_{md}(s) = \frac{g_{md}}{1 + NQS \cdot s \cdot \tau}$$

$$Y_{mbs}(s) = Y_{ms}(s) - Y_{mg}(s) - Y_{md}(s)$$

The availability of the NQS model is simulator-dependent.

Intrinsic Noise Model Equations

The noise is modeled by a current source I_{NDS} between intrinsic source and drain. It is composed of a thermal noise component and a flicker noise component and has the following Power Spectral Density (PSD):

$$S_{INDS} = S_{thermal} + S_{flicker}$$

Thermal Noise

The thermal noise component PSD is given by:

$$S_{thermal} = 4kT \cdot \frac{\mu_{eff}}{(NS \cdot L_{eff})^2} \cdot |Q_I| = 4kT \cdot \beta \cdot |q_I|$$

Note that the above thermal noise expression is *valid in all regions of operation*, including for small V_{DS} .

Flicker Noise

The flicker noise component PSD is given by:

$$S_{flicker} = \frac{KF \cdot g_{mg}^2}{NP \cdot W_{eff} \cdot NS \cdot L_{eff} \cdot COX \cdot f^{AF}}$$

Note that in some implementations, different expressions are accessible.

Operating Point Information

At operating points, the following information displays to help in circuit design:

Numerical values of model internal variables:

V_G, V_S, V_D, I_{DS}, I_{DB}, g_{mg}, g_{ms}, g_{mbs}, g_{md}, V_P, n, β, I_S, i_f, i_r, i_r', τ, τ_0 intrinsic charges/capacitances.

Transconductance efficiency factor:

$$tef = g_{ms} \cdot V_t / I_{DS}$$

Early voltage:

$$VM = I_{DS} / g_{md}$$

Overdrive voltage:

$$n \cdot (V_P - V_S) \approx V_G - \mathtt{VTO}_a - n \cdot V_S$$

For P-channel devices, $n \cdot (V_P - V_S)$ is given a negative sign.

SPICE-like threshold voltage:

$$VTH = \mathtt{VTO}_a + \Delta V_{RSCE} + \gamma' \cdot \sqrt{V'_S} - \mathtt{GAMMA}_a \cdot \sqrt{\mathtt{PHI}}$$

Note: This expression is the **'**SPICE-like' threshold voltage (the source). It also accounts for charge-sharing and reverse short-channel effects on the threshold voltage.

For P-channel devices, VTH is given a negative sign.

Saturation voltage:

$$VDSAT = 2V_{DSS} + 4V_t$$

For P-channel devices, VDSAT is given a negative sign.

Saturation / non-saturation flag:

$$\text{'SAT' or '1'} \qquad \text{for} \quad \frac{i_f}{i_r} > \mathtt{SATLIM}$$

$$\text{'LIN' or '0'} \qquad \text{for} \quad \frac{i_f}{i_r} \leq \mathtt{SATLIM}$$

Note: Implementation of operating point information may differ in some simulators (some information might not be available).

Estimation and Limits of Static Intrinsic Model Parameters

The EKV intrinsic model parameters can roughly be estimated from SPICE level 2/3 parameters as indicated in the table below, if no parameter extraction facility is available. Attention has to be paid to units of the parameters. This estimation method can be helpful and generally gives reasonable results. Nevertheless, be aware that the underlying modeling in SPICE Level 2/3 and in the EKV model is not the same, even if the names and the function of several parameters are similar. Therefore, it is preferred if parameter extraction is made directly from measurements.

Lower and upper limits indicated in the table should give an idea on the order of magnitude of the parameters but do not necessarily correspond to physically meaningful limits, nor to the range specified in the parameter tables. These limits may be helpful for obtaining physically meaningful parameter sets when using nonlinear optimization techniques to extract EKV model parameters.

Name	Unit	Default	Example	Lower	Upper	Estimation[a]
COX	F/m^2	0.7E-3	3.45E-3	-	-	ε_{ox}/TOX
XJ	m	0.1E-6	0.15E-6	0.01E-6	1E-6	XJ
VTO	V	0.5	0.7	0	2	VTO
GAMMA	$\sqrt{V}$	1.0	0.7	0	2	$\sqrt{2q\varepsilon_{si} \cdot NSUB}/COX$
PHI[b]	V	0.7	0.5	0.3	2	$2V_t \cdot \ln(NSUB/n_i)$
KP	A/V^2	50E-6	150E-6	10E-6	-	$UO \cdot COX$
E0	V/m	1.0E12	200E6	$0.1/(0.4 \cdot TOX)$		$0.2/(THETA \cdot TOX)$
UCRIT	V/m	2.0E6	2.3E6	1.0E6	25E6	VMAX/UO
DL	m	0	$-0.15*L_{min}$	$-0.5*L_{min}$	$0.5*L_{min}$	$XL - 2 \cdot LD$
DW	m	0	$-0.1*W_{min}$	$-0.5*W_{mi}$	$0.5*W_{min}$	$XW - 2 \cdot WD$

Name	Unit	Default	Example	Lower	Upper	Estimation[a]
LAMBDA	-	0.5	0.8	0	3	-
LETA	-	0.1	0.3	0	2	-
WETA	-	0.25	0.2	0	2	-
Q0	As/m^2	0.0	230E-6	0	-	-
LK	m	0.29E-6	0.4E-6	0.05E-6	2E-6	-
IBA	1/m	0.0	2.0E8	0.0	5.0E8	$ALPHA \cdot VCR/L_C$
IBB	V/m	3.0E8	2.0E8	1.8E8	4.0E8	VCR/L_C
IBN	-	1.0	0.6	0.4	1.0	-

a. Also compare with optional process parameters.

b. The minimum value of PHI also determines the minimum value of the pinch-off voltage. Due to the intrinsic temperature dependence of PHI, a lower value results for higher temperature, limiting the range of simulation for small currents.

ε_{ox} = 0.0345E-9 F/m q = 1.609E-19 C k = 1.381E-23 J/K $L_c = \sqrt{\varepsilon_{si} \cdot XJ/COX}$

ε_{si}= 0.104E-9 F/m n_i = 1.45E16 m^{-3} V_t = kT/q = 0.0259 V (at room temperature)

Note: Parameters in this table suppose m (meter) has been chosen as length unit. L_{min} and W_{min} are the minimum drawn length and width of the transistors. Example values are indicated for enhancement N-channel devices.

Model Updates Description

Throughout the use of the EKV v2.6 MOSFET model by many designers, several enhancements have appeared to be necessary from the model formulation point of view, or desirable from the point of view of the application of the model. This paragraph provides a summary of the updates to the EKV v2.6 model formulation and documentation since its first release. Wherever possible, backward compatibility with former formulations is maintained.

Revision I, September 1997

Description: Narrow channel effect on the substrate factor is revised to improve the transcapacitances behavior. The narrow channel effect is not anymore a function of the source voltage V_S, but of the pinch-off voltage V_P .

Consequence: the narrow channel effect parameters WETA, DW require different numerical values to achieve the same effect.

Revision II, July 1998

Intrinsic time constant

Description: Intrinsic time constant τ_0 is calculated as a function of the effective β factor (including vertical field dependent mobility and short-channel effects) instead of maximum mobility according to the KP parameter.

Consequence: the NQS time constant has an additional gate voltage dependence, resulting in more conservative (lower) estimation of the NQS time constant at high V_G, and additional dependence on short-channel effects.

Thermal noise

Description: Thermal noise power spectral density $s_{thermal}$ is calculated as a function of the effective β factor (including vertical field dependent mobility and short-channel effects) instead of maximum mobility according to the KP parameter.

Consequence: $s_{thermal}$ has an additional gate voltage and short-channel effect dependence.

Optional process parameters for calculating electrical intrinsic parameters

Description: The option is introduced to calculate the electrical parameters COX, GAMMA and/or PHI, VTO, KP and UCRIT as a function of the optional parameters TOX, NSUB, VFB, UO, and VMAX, respectively. NSUB and UO have *cm* as length units.

Consequence: This accommodates scaling behavior and allows more meaningful statistical circuit simulation due to decorrelation of physical effects. Compatible with former revisions except for default calculation of the parameters mentioned, if the optional parameters are specified.

Optional simplified mobility model

Description: The simple mobility model of former model versions, using the parameter THETA, is reinstated as an option.

Consequence: Simplifies adaptation from earlier model versions to the current version.

Parameter synonyms

Description: The parameters E0 and Q0 can be called by their synonyms EO and QO, respectively.

Consequence: Accommodates certain simulators where only alphabetic characters are allowed.

Operating point information

Description: The analytical expression for the 'SPICE'-like threshold voltage VTH in the operating point information is modified to include charge-sharing and reverse short-channel effects. The analytical expression for the saturation voltage VDSAT in the operating point information is modified such that its value is non-zero in weak inversion.

Consequence: Improved information for the designer.

Corrections from EPFL R11, March, 1999

Equation 45, Equation 53, Equation 54, and Equation 58 have been corrected for multiple series device behavior with the NS parameter.

Corrections from EPFL R12, July 30, 1999

The following corrections were released by EPFL.

Correction 1- 99/07/30 mb (r12) corrected dGAMMAprime_dVG (narrow channel). An error has been detected in the analytical model derivatives. It is in the derivatives of GAMMAprime variable, affecting the transconductances and transcapacitances.

Correction 2- 99/07/30 mb (r12) preventing PHI from being smaller than 0.2 at init and after temperature update. For certain CMOS technologies, parameter values for the parameter PHI turn out to be as low as 400mV required to account for particular process details. When increasing the temperature from room temperature, PHI decreases due to its built-in temperature dependence, thus making PHI attain very low values, or even be negative, when reaching 100degC. To allow the model to function at these temperatures, a lower limit for PHI is introduced (200mV). Note: the usual range for this parameter is well above this value (600mV to 1V).

Correction 3- 99/06/28 mb (r12) corrected COX and KP initialization (rg).

Correction 4- 99/05/04 mb (r12) completed parameters init for XQC, DL, DW, removed IBC, ibc (cd).

Level 57 UC Berkeley BSIM3-SOI Model

The UC Berkeley SOI model (BSIM3SOI) supports Fully Depleted (FD), Partially Depleted (PD), and Dynamically Depleted (DD) SOI devices, of which BSIM3PD2.0.1 for PD SOI devices is installed as Level 57. This model is described in the “BSIM3PD2.0 MOSFET MODEL User’ Manual,” which can be found at “http://www-device.eecs.berkeley.edu/~bsim3soi”.

The general syntax for including a BSIM3/SOI MOSFET element in a netlist is:

General Form

```
Mxxx nd ng ns ne <np> <nb> <nT> mname <L=val>
+ <W=val> <M=val> <AD=val> <AS=val> <PD=val> <PS=val>
+ <NRD=val> <NRS=val> <NRB=val> <RTH0=val> <CTH0=val>
+ <NBC=val> <NSEG=val> <PDBCP=val> <PSBCP=val>
+ <AGBCP=val> <AEBCP=val> <VBSUSR=val> <TNODEOUT>
+ <off> <FRBODY> <BJToff=val> <IC=Vds, Vgs, Vbs, Ves, Vps>
```

where the angle brackets indicate optional parameters.

The arguments are as follows:

Mxxx	SOI MOSFET element name. Must begin with M, which can be followed by up to 1023 alphanumeric characters.
nd	Drain terminal node name or number
ng	Front gate node name or number
ns	Source terminal node name or number
ne	Back gate (or substrate) node name or number
np	External body contact node name or number
nb	Internal body node name or number
nT	Temperature node name or number
mname	MOSFET model name reference

L	SOI MOSFET channel length in meters. This parameter overrides DEFL in an OPTIONS statement. Default=DEFL with a maximum of 0.1m.
W	MOSFET channel width in meters. This parameter overrides DEFW in an OPTIONS statement. Default=DEFW.
M	Multiplier to simulate multiple SOI MOSFETs in parallel. All channel widths, diode leakages, capacitances and resistances are affected by the setting of M. Default=1.
AD	Drain diffusion area. Overrides DEFAD in the OPTIONS statement. Default=DEFAD.
AS	Source diffusion area. Overrides DEFAS in the OPTIONS statement. Default=DEFAS.
PD	Perimeter of the drain junction, including the channel edge. Overrides DEFPD in the OPTIONS statement.
PS	Perimeter of the source junction, including the channel edge. Overrides DEFPS in the OPTIONS statement.
NRD	Number of squares of drain diffusion for drain series resistance. Overrides DEFNRD in the OPTIONS statement.
NRS	Number of squares of source diffusion for source series resistance. Overrides DEFNRS in the OPTIONS statement.
NRB	Number of squares for body series resistance.
FRBODY	Coefficient of distributed body resistance effects default = 1.0
RTH0	Thermal resistance per unit width If not specified, RTH0 is extracted from the model card. If specified, it will override the one in the model card.

CTH0	Thermal capacitance per unit width If not specified, CTH0 is extracted from model card. If specified, it will override the one in the model card.
NBC	Number of body contact isolation edge
NSEG	Number of segments for channel width partitioning
PDBCP	Parasitic perimeter length for the body contact at drain side
PSBCP	Parasitic perimeter length for the body contact at source side
AGBCP	Parasitic gate-to-body overlap area for body contact
AEBCP	Parasitic body-to-substrate overlap area for body contact
VBSUSR	Optional initial value of Vbs specified by user for transient analysis
TNODEOUT	Temperature node flag indicating the usage of T node
OFF	Sets initial condition of element to OFF in DC analysis
BJTOFF	Turning off BJT if equal to 1
IC	Initial guess in the order (drain, front gate, internal body, back gate, external voltage). (Vps will be ignored in the case of 4-terminal device) These are used when UIC is present in the .TRAN statement and are overridden by the .IC statement.

Notes:

- If TNODEOUT is not set, specifying 4 nodes for a device floats the body, specifying 5 nodes implies the fifth node is the external body contact node with a body resistance put between the internal and the external terminals. This configuration applies to a distributed body resistance simulation.
- If TNODEOUT is set, the last node is interpreted as the temperature node. In this case, specifying 5 nodes floats the device, specifying 6 nodes implies a body-contacted case. If user specifies seven nodes, it is a body-contacted case with an accessible internal body node. The temperature node is useful for thermal coupling simulation.

Level 57 Model Parameters

Model Control Parameters

Parameter	Unit	Default	Description
Level	-	-	Level 57 for BSIM3SOI
SHMOD	-	0	Flag for self-heating: 0 - no self-heating 1 - self-heating
MOBMOD	-	1	Mobility model selector
capmod	-	2	Flag for the short channel capacitance model
noimod	-	1	Flag for noise model

Process Parameters

Parameter	Unit	Default	Description
Tsi	m	1.0e-7	Silicon film thickness
Tbox	m	3.0e-7	Buried oxide thickness
Tox	m	1.0e-8	Gate oxide thickness
Xj	m	-	S/D junction depth
Nch	$1/cm^3$	1.7e17	Channel doping concentration
Nsub	$1/cm^3$	6.0e16	Substrate doping concentration
Ngate	$1/cm^3$	0	Poly gate doping concentration

DC Parameters

Parameter	Unit	Default	Description
vth0	v	NMOS 0.7 PMOS -0.7	Threshold voltage @ Vbs=0 for long wide device
k1	$V^{1/2}$	0.6	First-order body effect coefficient
k1w1	m	0	First-order effect width dependent parameter
k1w2	m	0	Second-order effect width dependent parameter
k2	-	0	Second-order body effect coefficient
k3	-	0	Narrow coefficient
k3b	1/V	0	Body effect coefficient of k3
kb1	-	1	Backgate body charge coefficient
w0	m	0	Narrow width parameter
nlx	m	1.74e-7	Lateral non-uniform doping parameter
Dvt0	-	2.2	First coefficient of short-channel effect on Vth
dvt1	-	0.53	Second coefficient of short-channel effect on Vth
dvt2	1/V	-0.032	Body-bias coefficient of short-channel effect on Vth
dvt0w	-	0	First coefficient of narrow width effect on Vth for small channel length

Parameter	Unit	Default	Description
dvt1w	-	5.3e6	Second coefficient of narrow width effect on Vth for small channel length
dvt2w	1/V	-0.032	Body-bias coefficient of narrow width effect on Vth for small channel length
u0	cm^2/(V-sec)	NMOS-670 PMOS-250	Mobility at Temp=Tnom
ua	m/V	2.25e-9	First-order mobility degradation coefficient
ub	$(m/V)^2$	5.87e-19	Second-order mobility degradation coefficient
uc	1/V	-0.0465	Body-effect of mobility degradation coefficient
vsat	m/sec	8e4	Saturation velocity at Temp=Tnom
a0	-	1.0	Bulk charge effect coefficient for channel length
ags	1/V	0.0	Gate bias coefficient of A_{bulk}
b0	m	0.0	Bulk charge effect coefficient for channel width
b1	m	0.0	Bulk charge effect width offset
keta	1/V	-0.6	Body-bias coefficient of bulk charge effect
Ketas	V	0.0	Surface potential adjustment for bulk charge effect

Parameter	Unit	Default	Description
A1	1/V	0.0	First non-saturation effect parameter
A2	-	1.0	Second non-saturation effect parameter
rdsw	$\Omega*\mu m^{wr}$	100	Parasitic resistance per unit width
prwb	$1/V^{1}$	0	Body effect coefficient of Rdsw
prwg	$1/V^{1/2}$	0	Gate bias effect coefficient of Rdsw
wr	-	1	Width offset from Weff for Rds calculation
nfactor	-	1	Subthreshold swing factor
wint	m	0.0	Width offset fitting parameter from I-V without bias
lint	m	0.0	Length offset fitting parameter from I-V without bias
dwg	m/V	0.0	Coefficient of Weff's gate dependence
dwb	$m/V^{1/2}$	0.0	Coefficient of Weff's substrate body bias dependence
dwbc	m	0.0	Width offset for body contact isolation edge
voff	v	-0.08	Offset voltage in the subthreshold region for large W and L
eta0	-	0.08	DIBL coefficient in the subthreshold region

Parameter	Unit	Default	Description
etab	1/V	-0.07	Body-bias coefficient for the subthreshold DIBL effect
dsub	-	0.56	DIBL coefficient exponent
cit	F/m^2	0.0	Interface trap capacitance
cdsc	F/m^2	2.4e-4	Drain/source to channel coupling capacitance
cdscb	F/m^2	0	Body-bias sensitivity of cdsc
cdscd	F/m^2	0	Drain-bias sensitivity of cdsc
pclm	-	1.3	Channel length modulation parameter
PDIBLC1	-	0.39	First output resistance DIBL effect correction parameter
pdiblc2	-	0.0086	Second output resistance DIBL effect correction parameter
drout	-	0.56	L dependence coefficient of the DIBL correction parameter in Rout
pvag	-	0.0	Gate dependence of Early voltage
delta	-	0.01	Effective V_{ds} parameter
alpha0	m/V	0.0	The first parameter of impact ionization current
fbjtii	-	0.0	Fraction of bipolar current affecting the impact ionization
beta0	1/V	0.0	First V_{ds} dependence parameter of impact ionization current

Parameter	Unit	Default	Description
beta1	-	0.0	Second V_{ds} dependence parameter of impact ionization current
beta2	V	0.1	Third V_{ds} dependence parameter of impact ionization current
vdsatii0	V	0.9	Nominal drain saturation voltage at threshold for impact ionization current
tii	-	0	Temperature dependence parameter for impact ionization current
lii	-	0	Channel length dependence parameter for impact ionization current
esati	V/m	1.e7	Saturation channel electric field for impact ionization current
sii0	1/V	0.5	First V_{gs} dependence parameter for impact ionization current
sii1	1/V	0.1	Second V_{gs} dependence parameter for impact ionization current
sii2	1/V	0	Third V_{gs} dependence parameter for impact ionization current
siid	1/V	0	V_{ds} dependence parameter of drain saturation voltage for impact ionization current
Agidl	1/W	0.0	GIDL constant
Bgidl	V/m	0.0	GIDL exponential coefficient

Parameter	Unit	Default	Description
Ngidl	V	1.2	GIDL V_{ds} enhancement coefficient
Ntun	-	10.0	Reverse tunneling non-ideality factor
NdioDE	-	1.0	Diode non-ideality factor
Nrecf0	-	2.0	Recombination non-ideality factor at forward bias
Nrecr0	-	10	Recombination non-ideality factor at reversed bias
Isbjt	A/m^2	1.0e-6	BJT injection saturation current
Isdif	A/m^2	0	Body to source/drain injection saturation current
Isrec	A/m^2	1.0e-5	Recombination in depletion saturation current
Istun	A/m^2	0.0	Reverse tunneling saturation current
Ln	m	2.0e-6	Electron/hole diffusion length
Vrec0	V	0.0	Voltage dependent parameter for recombination current
Vtun0	V	0.0	Voltage dependent parameter for tunneling current
Nbjt	-	1	Power coefficient of channel length dependency for bipolar current
Lbjt0	m	0.2e-6	Reference channel length for bipolar current

Parameter	Unit	Default	Description
Vabjt	V	10	Early voltage for bipolar current
Aely	V/m	0	Channel length dependency of early voltage for bipolar current
Ahli	-	0	High-level injection parameter for bipolar current
Rbody	ohm/m^2	0.0	Intrinsic body contact sheet resistance
Rbsh	ohm/m^2	0.0	Extrinsic body contact sheet resistance
rsh	ohm/square	0.0	Source/drain sheet resistance in ohm per square
VEVB	v	0.075v	Electron tunneling from the valence band
VECB	v	0.026v	Electron tunneling from conduction band

AC and Capacitance Parameters

Parameter	Unit	Default	Description
xpart	-	0	Charge partitioning rate flag
cgso	F/m	calculated	Non LDD region source-gate overlap capacitance per channel length
cgdo	F/m	0	Non LDD region drain-gate overlap capacitance per channel length
CGEO	F/m	0	Gate substrate overlap capacitance per unit channel length
cjswg	F/m^2	1.e-10	Source/drain (gate side) sidewall junction capacitance per unit width (normalized to 100nm Tsi)
pbswg	V	0.7	Source/drain (gate side) sidewall junction capacitance built in potential
mjswg	V	0.5	Source/drain (gate side) sidewall junction capacitance grading coefficient
tt	second	1ps	Diffusion capacitance transit time coefficient
Ndif	-	-1	Power coefficient of channel length dependency for diffusion capacitance
Ldif0	-	1	Channel length dependency coefficient of diffusion cap.

Parameter	Unit	Default	Description
vsdfb	V	cal.	Source/drain bottom diffusion capacitance flatband voltage
vsdth	V	cal.	Source/drain bottom diffusion capacitance threshold voltage
csdmin	V	cal.	Source/drain bottom diffusion minimum capacitance
asd	V	0.3	Source/drain bottom diffusion smoothing parameter
csdesw	F/m	0.0	Source/drain sidewall fringing capacitance per unit length
cgsl	F/m	0.0	Lightly doped source-gate region overlap capacitance
cgdl	F/m	0.0	Lightly doped drain-gate region overlap capacitance
ckappa	F/m	0.6	Coefficient for lightly doped region overlap capacitance fringing field capacitance
cf	F/m	cal.	Gate to source/drain fringing field capacitance
clc	m	0.1e-7	Constant term for the short channel model
cle	-	0.0	Exponential term for the short channel model
dlc	m	lint	Length offset fitting parameter for gate charge

Parameter	Unit	Default	Description
dlcb	m	lint	Length offset fitting parameter for body charge
dlbg	m	0	Length offset fitting parameter for backgate charge
dwc	m	wint	Width offset fitting parameter from C-V
delvt	V	0.0	Threshold voltage adjust for C-V
fbody	-	1.0	Scaling factor for body charge
acde	m/V	1.0	Exponential coefficient for charge thickness in CapMod=3 for accumulation and depletion regions
moin	$V^{1/2}$	15.0	Coefficient for the gate-bias dependent surface potential

Temperature Parameters

Parameter	Unit	Default	Description
tnom	^{o}C	25	Temperature at which parameters are expected
ute	-	-1.5	Mobility temperature exponent
kt1	V	-0.11	Temperature coefficient for the threshold voltage
ktil	V*m	0	Channel length dependence of the temperature coefficient for the threshold voltage

Parameter	Unit	Default	Description
kt2	-	0.022	Body-bias coefficient of the threshold voltage temperature effect
ua1	m/V	4.31e-9	Temperature coefficient for U_a
ub1	$(m/V)^2$	-7.61e-18	Temperature coefficient for U_b
uc1	1/V	-0.056	Temperature coefficient for U_c
at	m/sec	3.3e4	Temperature coefficient for U_a
tcjswg	1/K	0	Temperature coefficient of C_{jswg}
tpbswg	V/K	0	Temperature coefficient of P_{bswg}
cth0	$m^oC/(W*s)$	0	Normalized thermal capacity
prt	Ω-um	0	Temperature coefficient for Rdsw
rth0	m^oC/W	0	Normalized thermal resistance
Ntrecf	-	0	Temperature coefficient for N_{recf}
Ntrecr	-	0	Temperature coefficient for N_{recr}
xbjt	-	1	Power dependence of j_{bjt} on temperature
xdif	-	XBJT	Power dependence of j_{dif} on temperature
xrec	-	1	Power dependence of j_{rec} on temperature
xtun	-	0	Power dependence of j_{tun} on temperature

Notes:

- BSIMPD2.01 supports capmod=2 and 3 only. capmod=0 and 1 are not supported.
- In modern SOI technology, source/drain extension or LDD are commonly used. As a result, the source/drain junction depth (Xj) can be different from the silicon film thickness (Tsi). By default, if Xj is not given, it is set to Tsi. Xj is not allowed to be greater than Tsi.
- BSIMPD refers substrate to the silicon below buried oxide, not the well region in BSIM3. It is used to calculated backgate flatband voltage (Vfbb) and parameters related to source/drain diffusion bottom capacitance (Vsdth, Vsdfb, Csdmin). Positive nsub means the same type of doping as the body and negative nsub means opposite type of doping.

Level 57 Template Output

Additional element templates are added to this model for output of state variables, stored charges, capacitor currents and capacitances.

SOI MOSFET (Level 57)

Name	Alias	Description
L	LV1	Channel length (L)
W	LV2	Channel width (W)
AD	LV3	Area of the drain diode (AD)
AS	LV4	Area of the source diode (AS)
ICVDS	LV5	Initial condition for drain-source voltage (VDS)
ICVGS	LV6	Initial condition for gate-source voltage (VGS)
ICVES	LV7	Initial condition for Substrate-source voltage (VES)
VTH	LV9	Threshold voltage (bias dependent)
VDSAT	LV10	Saturation voltage (VDSAT)

Name	Alias	Description
PD	LV11	Drain diode periphery (PD)
PS	LV12	Source diode periphery (PS)
RDS	LV13	Drain resistance (squares) (RDS)
RSS	LV14	Source resistance (squares) (RSS)
GDEFF	LV16	Effective drain conductance (1/RDeff)
GSEFF	LV17	Effective source conductance (1/RSeff)
COVLGS	LV36	Gate-source overlap capacitance
COVLGD	LV37	Gate-drain overlap capacitance
COVLGE	LV38	Gate-substrate overlap capacitance
VES	LX1	Substrate-source voltage (VES)
VGS	LX2	Gate-source voltage (VGS)
VDS	LX3	Drain-source voltage (VDS)
CDO	LX4	DC drain current (CDO)
CBSO	LX5	DC source-body diode current (CBSO)
CBDO	LX6	DC drain-body diode current (CBDO)
GMO	LX7	DC gate transconductance (GMO)
GDSO	LX8	DC drain-source conductance (GDSO)
GMESO	LX9	DC substrate transconductance (GMBSO)
GBDO	LX10	Conductance of the drain diode (GBDO)
GBSO	LX11	Conductance of the source diode (GBSO)

Meyer and Charge Conservation Model Parameters

Name	Alias	Description
QB	LX12	Body charge (QB)
CQB	LX13	Body charge current (CQB)
QG	LX14	Gate charge (QG)
CQG	LX15	Gate charge current (CQG)
QD	LX16	Channel charge (QD)
CQD	LX17	Channel charge current (CQD)
CGGBO	LX18	CGGBO = ∂Qg/∂Vgb = CGS + CGD + CGB
CGDBO	LX19	CGDBO = ∂Qg/∂Vdb, (for Meyer CGD=-CGDBO)
CGSBO	LX20	CGSBO = ∂Qg/∂Vsb , (for Meyer CGS=-CGSBO)
CBGBO	LX21	CBGBO = ∂Qb/∂Vgb , (for Meyer CGB=-CBGBO)
CBDBO	LX22	CBDBO = ∂Qb/∂Vdb
CBSBO	LX23	CBSBO = ∂Qb/∂Vsb
CDGBO	LX32	CDGBO = ∂Qd/∂Vgb
CDDBO	LX33	CDDBO = ∂Qd/∂Vdb
CDSBO	LX34	CDSBO = ∂Qd/∂Vsb
QE	LX35	Substrate charge (QE)
CQE	LX36	Substrate charge current (CQE)
CDEBO	LX37	CDEBO = ∂Qd/∂Veb
CBEBO	LX38	CBEBO = ∂Qb/∂Veb
CEEBO	LX39	CEEBO = ∂Qe/∂Veb

Name	Alias	Description
CEGBO	LX40	CEGBO = ∂Qe/∂Vgb
VBS	LX43	Body-source voltage (VBS)
ICH	LX44	Channel current
IBJT	LX45	Parasitic BJT collector current
III	LX46	Impact ionization current
IGIDL	LX47	GIDL current
ITUN	LX48	Tunneling current
Qbacko	LX49	Internal body charge
Ibp	LX50	Body contact current
Sft	LX51	Value of the temperature node with *shmod=1*
Vfb	LX52	Internal body node voltage, if terminal is not specified
Rbp	LX53	Combination of rbody and rhalo
Ig	LX54	Gate tunneling current
QS	LX55	Source charge
CQs	LX56	Source charge current
CGEBO	LX57	CGEBO=d_Q_g/d_V_{eb}
CSSBO	LX58	CSSBO=d_Q_s/d_V_{sb}
CSGBO	LX59	CSGBO=d_Q_s/d_V_{gb}
CSDBO	LX60	CSDBO=d_Q_s/d_V_{db}
CSEBO	LX61	CSEBO=d_Q_s/d_V_{eb}

Level 57 Updates to BSIM3-SOI PD versions 2.2, 2.21, and 2.22

- BSIM PD version 2.2 is updated to enhance the model flexibility and accuracy from PD version 2.0, and the following are its major features.
  - The gate-body tunneling (substrate current) is added to enhance the model accuracy.
  - The body contact resistance is improved for modeling accuracy.
  - The binning is added in this release to enhance the model flexibility.
- BSIM PD version 2.21 is updated from the PD version 2.2 for bug fixes and S/D swapping for the gate current components.
- BSIM PD version 2.22 is updated from the 2.21 version for bug fixes and enhancements. The major features are:
  - Added a new instance parameter FRBODY
  - Improved the temperature dependence of the gate direct tunneling model
  - Added two new model parameters, VEVB and VECB
  - UC Berkeley code no longer supports the model parameters NECB and NEVB. These parameters are still accepted in 2.22 for backwards compatibility, but they have no effect.

Using BSIM3-SOI PD

To use BSIM3-SOI PD versions 2.0, 2.2, 2.21, and 2.22 in simulation, apply the VERSION model parameter. For example:

- PD2.0 is invoked when VERSION=2.0
- PD2.2 and PD2.21 are invoked when VERSION=2.2
- PD2.22 is invoked when VERSION=2.22

For gate-body tunneling, the model parameter IGMOD should be set to 1.

Example

This is an example of the BSIM3-SOI PD model and element statement.

```
mckt drain gate source bulk nch L=10e-6 W=10e-6
.model nch       nmos Level=57    igmod=1         version=2.2
+ tnom=27         tox=4.5e-09      tsi=.0000001     tbox=8e-08
+ mobmod=0         capmod=2         shmod=0         paramchk=0
+ wint=0           lint=-2e-08        vth0=.42          k1=.49
```

```
+ k2=.1           k3=0             k3b=2.2          nlx=2e-7
+ dvt0=10         dvt1=.55         dvt2=-1.4        dvt0w=0
+ dvt1w=0        dvt2w=0         nch=4.7e+17     nsub=-1e+15
+ ngate=1e+20     agidl=1E-15      bgidl=1E9       ngidl=1.1
+ ndiode=1.13     ntun=14.0        nrecf0=2.5      nrecr0=4
+ vrec0=1.2       ntrecf=.1       ntrecr=.2       isbjt=1E-4
+ isdif=1E-5      istun=2E-5       isrec=4E-2      xbjt=.9
+ xdif=.9         xrec=.9          xtun=0.01       ahli=1e-9
+ lbjt0=0.2e-6     ln=2e-6          nbjt=.8         ndif=-1
+ aely=1e8        vabjt=0          u0=352          ua=1.3e-11
+ ub=1.7e-18      uc=-4e-10        w0=1.16e-06     ags=.25
+ A1=0             A2=1             b0=.01          b1=10
+ rdsw=0           prwg=0           prwb=-.2        wr=1
+ rbody=1E0       rbsh=0.0         a0=1.4          keta=0.1
+ ketas=0.2       vsat=135000      dwg=0           dwb=0
+ alpha0=1e-8     beta0=0         beta1=0.05      beta2=0.07
+ vdsatii0=.8     esatii=1e7       voff=-.14       nfactor=.7
+ cdsc=.00002      cdscb=0          cdscd=0         cit=0
+ pclm=2.9       pvag=12         pdiblc1=.18     pdiblc2=.004
+ pdiblcb=-.234    drout=.2         delta=.01       eta0=.05
+ etab=0         dsub=.2         rth0=.005       clc=.0000001
+ cle=.6          cf=1e-20         ckappa=.6       cgdl=1e-20
+ cgsl=1e-20       kt1=-.3          kt1l=0          kt2=.022
+ ute=-1.5      ua1=4.31e-09   ub1=-7.61e-18    uc1=-5.6e-11
+ prt=760         at=22400         cgso=1e-10      cgdo=1e-10
+ cjswg=1e-12     tt=3e-10        asd=0.3        csdesw=1e-12
+ tcjswg=1e-4      mjswg=.5         pbswg=1
```

Level 58 University of Florida SOI Model

UFSOI has non-fully depleted (NFD) and fully depleted (FD) SOI models (no dynamic mode operating between NFD and FD allowed) that separately describe two main types of SOI devices. The UFSOI version 4.5F model has been installed in the Avant! True-Hspice models as Level 58. This model is described in the "UFSOI Model User's Manual," which can be found at "http://www.soi.tec.ufl.edu/".

In some processes, there is an external contact to the body of the device. The Avant! True-Hspice model supports only a 4-terminal device, which includes drain, front gate, source and back gate (or substrate). The additional body contact is currently not supported and is floated.

The effects of parasitic diodes in SOI are different from those in bulk MOSFET. The True-Hspice junction model (ACM), developed for bulk MOSFETs, is not included in the SOI model.

The general syntax for including Level 58 in a netlist follows:

General Form

```
Mxxx nd ngf ns <ngb> mname <L=val> <W=val> <M=val>
+ <AD=val> <AS=val> <PD=val> <PS=val> <NRD=val>
+ <NRS=val> <NRB=val> <RTH=val> <CTH=val> <off>
+ <IC=Vds,Vgfs,VGbs>
```

where the angle brackets indicate optional parameters. The arguments are identical to those used for BSIM3-SOI model, except the thermal resistance and capacitance have different names:

RTH	Thermal resistance, unit in $K \cdot W^{-1}$, defaulted to 0.0
CTH	Thermal capacitance, unit in $W \cdot s \cdot K^{-1}$, defaulted to 0.0

Notes:

- The defaulted value for channel length L and width W is 1.0e-6.

- The present version supports only 4 nodes, which means only floating-body devices are supported. AB is typically zero and should be specified accordingly.
- When the self-heating option is activated (on the model line), RTH and CTH, typical values of which are 5e3 and 1e-12, respectively, but which can vary widely from one device to another, are used to define the thermal impedance of the device.
- For M > 1, W, AD, AS, NRD, NRS, NRB, PDJ, PSJ, RTH, and CTH must be specified per gate finger.
- The initial condition IC is in the order: drain voltage Vds, front gate voltage Vgfs, and back gate voltage Vbgs.

Level 58 FD/SOI MOSFET Model Parameters

The following tables describe the Level 58 model parameters for fully depleted (FD) SOI including parameter name, descriptions, units, default and typical notes.

Flag Parameters

Parameter	Unit	Default	Typical Value	Description
Level	-	-	-	Level 57 for UFSOI
NFDMOD	-	0	0	Model selector (0: FD)
BJT	-	1	1	Parasitic bipolar flag (0: off; 1: on)
SELFT	-	0	0	Self-heating flag (0: no self-heating; 1: approximate model; 2: full self-heating)
TPG	-	1	-	Type of gate polysilicon (+1: opposite to body; -1: same as body)

Parameter	Unit	Default	Typical Value	Description
TPS	-	-1	-	Type of substrate (+1: opposite to body; -1: same as body)

Structural Parameters

Parameter	Unit	Default	Typical Value	Description
TOXF	m	1.0e-8	(3-8)x10^{-9}	Front-gate oxide thickness
TOXB	m	0.5e-6	(80-400) x10^{-9}	Back-gate oxide thickness
NSUB	cm^{-3}	1.0e15	10^{15}-10^{17}	Substrate doping density
NGATE	cm^{-3}	0.0	10^{19}-10^{20}	Poly-gate doping density (0 for no poly-gate depletion)
NDS	cm^{-3}	5.0e19	10^{19}-10^{20}	Source/drain doping density
TB	m	0.1e-6	(30-100) x10^{-9}	Film (body) thickness
NBODY	cm^{-3}	5.0e16	10^{17}-10^{18}	Film (body) doping density
LLDD	m	0.0	(0.05-0.2) x10^{-6}	LDD/LDS region length (0 for no LDD)
NLDD	cm^{-3}	5.0e19	1x10^{19}	LDD/LDS doping density (>1e19: LDD/LDS treated as D/S extensions)
DL	m	0.0	(0.05-0.15)x10^{-6}	Channel-length reduction
DW	m	0.0	(0.1-0.5) x10^{-6}	Channel-width reduction

Electrical Parameters

Parameter	Unit	Default	Typical Value	Description
NQFF	cm^{-2}	0.0	~ 10^{10}	Front oxide fixed charge (normalized)
NQFB	cm^{-2}	0.0	~ 10^{11}	Back oxide fixed charge (normalized)
NQFSW	cm^{-2}	0.0	~ $\pm 10^{12}$	Effective sidewall fixed charge (0 for no narrow-width effect)
NSF	$cm^{-2} \cdot eV^{-1}$	0.0	~10^{10}	Front surface state density
NSB	$cm^{-2} \cdot eV^{-1}$	0.0	~ 10^{11}	Back surface state density
QM	-	0.0 - 0.5		Energy quantization parameter (0 for no quantization)
UO	$cm^2 \cdot V^{-1} \cdot s^{-1}$	7.0e2	200-700 (nMOS) 70-400 (pMOS)	Low-field mobility
THETA	$cm \cdot V^{-1}$	7.0e2	(0.1-3) $x10^{-6}$	Mobility degradation coefficient
VSAT	$cm \cdot s^{-1}$	1.0e-6	(0.5-1)x10	Carrier saturated drift velocity
ALPHA	cm^{-1}	0.0	$2.45x10^6$	Impact-ionization coefficient (0 for no impact ionization)
BETA	$V \cdot cm^{-1}$	0.0	$1.92x10^6$	Impact-ionization exponential factor (0 for no impact ionization)

Parameter	Unit	Default	Typical Value	Description
BGIDL	$V \cdot cm^{-1}$	0.0	$(4\text{-}8)x10^{9}$	Exponential factor for gate-induced drain leakage (0 for no GIDL)
GAMMA	-	0.3	0.3-1.0	BOX fringing field weighting factor
KAPPA	-	0.5	0.5-1.0	BOX fringing field weighting factor
JRO	$A \cdot m^{-1}$	1.0e-10	10^{-11}-10^{-9}	Body-source/drain junction recombination current coefficient
M	-	2.0	1.0-2.0	Body-source/drain junction recombination ideality factor
LDIFF	m	1.0e-7	$(0.1\text{-}0.5)$ $x10^{-6}$	Effective diffusion length in source/drain
SEFF	$cm \cdot s^{-1}$	1.0e5	$(0.5\text{-}5)$ $x10^{5}$	Effective recombination velocity in source/drain
CGFDO	$F \cdot m^{-1}$	0.0	$1x10^{-10}$	Gate-drain overlap capacitance
CGFSO	$F \cdot m^{-1}$	0.0	$1x10^{-10}$	Gate-source overlap capacitance
CGFBO	$F \cdot m^{-1}$	0.0	0.0	Gate-body overlap capacitance
RD	ohm·m	0.0	200-1000	Specific drain parasitic resistance
RS	ohm·m	0.0	200-1000	Specific source parasitic resistance

Parameter	Unit	Default	Typical Value	Description
RHOB	ohm/sq.	0.0	$30x10^{3}$	Body sheet resistance
FNK	F·A	0.0	$0\text{-}10^{-2}$	Flicker noise coefficient
FNA	-	1.0	0.5-2	Flicker noise exponent

Optional Parameters

Parameter	Unit	Default	Typical Value	Description
VFBF	V	calc.	-1 (nMOS) 1 (pMOS)	Front-gate flatband voltage
VFBB	V	calc.	-	Back-gate flatband voltage
WKF	V	calc.	~ VFBF	Front-gate work function difference
WKB	V	calc.	-	Back-gate work function difference
TAUO	s	calc.	$10^{-7}\text{-}10^{-5}$	Carrier lifetime in lightly doped regions
BFACT	-	0.3	0.1-0.5	V_{DS}-averaging factor for mobility degradation
FVBJT	-	0.0	0-1	BJT current directional partitioning factor (0 for lateral 1D flow)
RHOSD	ohm/ sq.	0.0	50	Source/drain sheet resistance

Level 58 NFD/SOI MOSFET Model Parameters

The following tables describe the Level 58 model parameters for non-fully depleted (NFD) SOI including parameter name, descriptions, units, default and typical notes.

Flag Parameters

Parameter	Unit	Default	Typical Value	Description
Level	-	-	-	Level 57 for UFSOI
NFDMOD	-	0	-	Model selector(1: NFD)
BJT	-	1	1	Parasitic bipolar flag (0: off; 1: on)
SELFT	-	0	0	Self-heating flag (0: no self-heating; 1: approximate model; 2: full self-heating)
TPG	-	1	1	Type of gate polysilicon (+1: opposite to body; -1: same as body)
TPS	-	-1	-1	Type of substrate (+1: opposite to body; -1: same as body)

Structural Parameters

Parameter	Unit	Default	Typical Value	Description
TOXF	m	1.0e-8	(3-8)x10^{-9}	Front-gate oxide thickness
TOXB	m	0.5e-6	(80-400) x10^{-9}	Back-gate oxide thickness
NSUB	cm^{-3}	1.0e15	10^{15}-10^{17}	Substrate doping density
NGATE	cm^{-3}	0.0	10^{19}-10^{20}	Poly-gate doping density (0 for no poly-gate depletion)
NDS	cm^{-3}	5.0e19	10^{19}-10^{20}	Source/drain doping density
TF	m	0.2e-6	(3-8)x10^{-9}	Silicon film thickness
TB	m	0.1e-6	(30-100) x10^{-9}	Film (body) thickness
THALO	m	0.0	-	Halo thickness (0 for no halo)
NBL	cm^{-3}	5.0e16	10^{17}-10^{18}	Low body doping density
NBH	cm^{-3}	5.0e17	10^{19}-10^{20}	Halo doping density
NHALO	cm^{-3}	-	~10^{18}	Halo doping density
LRSCE	m	0.0	~0.1x10^{-6}	Characteristic length for reverse short-channel effect (0 for no RSCE)
LLDD	m	0.0	(0.05-0.2) x10^{-6}	LDD/LDS region length (0 for no LDD)

Parameter	Unit	Default	Typical Value	Description
NLDD	cm^{-3}	5.0e19	$1x10^{19}$	LDD/LDS doping density (>1e19: LDD/LDS treated as D/S extensions)
DL	m	0.0	$(0.05\text{-}0.15)x10^{-6}$	Channel-length reduction
DW	m	0.0	$(0.1\text{-}0.5)\ x10^{-6}$	Channel-width reduction

Electrical Parameters

Parameter	Unit	Default	Typical Value	Description
NQFF	cm^{-2}	0.0	$\sim 10^{10}$	Front oxide fixed charge (normalized)
NQFB	cm^{-2}	0.0	$\sim 10^{11}$	Back oxide fixed charge (normalized)
NQFSW	cm^{-2}	0.0	$\sim \pm 10^{12}$	Effective sidewall fixed charge (0 for no narrow-width effect)
QM	-	0.0 - 0.5		Energy quantization parameter (0 for no quantization)
UO	$cm^2 \cdot V^{-1} \cdot s^{-1}$	7.0e2	200-700 (nMOS) 70-400 (pMOS)	Low-field mobility
THETA	$cm \cdot V^{-1}$	7.0e2	$(0.1\text{-}3)\ x10^{-6}$	Mobility degradation coefficient

Parameter	Unit	Default	Typical Value	Description
VSAT	$cm \cdot s^{-1}$	1.0e-6	(0.5-1) x10	Carrier saturated drift velocity
ALPHA	cm^{-1}	0.0	$2.45x10^{6}$	Impact-ionization coefficient (0 for no impact ionization)
BETA	$V \cdot cm^{-1}$	0.0	$1.92x10^{6}$	Impact-ionization exponential factor (0 for no impact ionization)
BGIDL	$V \cdot cm^{-1}$	0.0	$(4\text{-}8)x10^{9}$	Exponential factor for gate-induced drain leakage (0 for no GIDL)
NTR	cm^{-3}	0.0	10^{14}-10^{15}	Effective trap density for trap-assisted junction tunneling (0 for no tunneling)
JRO	$A \cdot m^{-1}$	1.0e-10	10^{-11}-10^{-9}	Body-source/drain junction recombination current coefficient
M	-	2.0	1.0-2.0	Body-source/drain junction recombination ideality factor
LDIFF	m	1.0e-7	$(0.1\text{-}0.5)x10^{-6}$	Effective diffusion length in source/drain
SEFF	$cm \cdot s^{-1}$	1.0e5	$(0.5\text{-}5)x10^{5}$	Effective recombination velocity in source/drain
CGFDO	$F \cdot m^{-1}$	0.0	$1x10^{-10}$	Gate-drain overlap capacitance
CGFSO	$F \cdot m^{-1}$	0.0	$1x10^{-10}$	Gate-source overlap capacitance
CGFBO	$F \cdot m^{-1}$	0.0	0.0	Gate-body overlap capacitance

Parameter	Unit	Default	Typical Value	Description
RD	ohm·m	0.0	200-1000	Specific drain parasitic resistance
RS	ohm·m	0.0	200-1000	Specific source parasitic resistance
RHOB	ohm/sq.	0.0	$30x10^{3}$	Body sheet resistance
FNK	F·A	0.0	$0\text{-}10^{-2}$	Flicker noise coefficient
FNA	-	1.0	0.5-2	Flicker noise exponent

Optional Parameters

Parameter	Unit	Default	Typical Value	Description
VFBF	V	calc.	-1 (nMOS) 1 (pMOS)	Front-gate flatband voltage
VFBB	V	calc.	-	Back-gate flatband voltage
WKF	V	calc.	~ VFBF	Front-gate work function difference
WKB	V	calc.	-	Back-gate work function difference
TAUO	s	calc.	$10^{-7}\text{-}10^{-5}$	Carrier lifetime in lightly doped regions
BFACT	-	0.3	0.1-0.5	V_{DS}-averaging factor for mobility degradation

Parameter	Unit	Default	Typical Value	Description
FVBJT	-	0.0	0-1	BJT current directional partitioning factor (0 for lateral 1D flow)
RHOSD	ohm/ sq.	0.0	50	Source/drain sheet resistance

Notes:

- The model line must include Level=58 and NFDMOD=0 for FD or NFDMOD=1 for NFD devices.
- Specifying VFBF turns off the narrow-width effect defined by NQFSW (which can be positive or negative) and the reverse short-channel effect defined by LRSCE (and NBH, or NHALO if specified); the latter effect is also turned off when WKF is specified.
- For floating-body devices, CGFBO is small and should be specified to be 0.
- JRO and SEFF influence the gain of the BJT, but LDIFF affects only bipolar charge storage in the source/drain. The BJT gain is influenced by NBH and NHALO (if THALO is specified) as well.
- The value of TAUO should be loosely correlated with JRO in accord with basic pn-junction recombination/generation properties. Its default value is calculated based on JRO, which is appropriate for short L; for long L, body generation tends to predominate over that in the junctions, and hence TAUO should be specified.
- The (non-local) impact-ionization model is physical, and its parameters should not be varied arbitrarily.
- The LDD option intensifies the model, so it is advisable to set LLDD to 0 for large-scale circuit simulation, and add the unbiased LDD resistance to RD; this simplification is foisted when NLDD > 1e19 is specified.

Level 58 Template Output

Some element templates are added to this model for output of state variables, stored charges and capacitor currents.

SOI MOSFET (Level 58)

Name	Alias	Description
L	LV1	Channel length (L)
W	LV2	Channel width (W)
AD	LV3	Area of the drain diode (AD)
AS	LV4	Area of the source diode (AS)
ICVDS	LV5	Initial condition for drain-source voltage (VDS)
ICVGS	LV6	Initial condition for gate-source voltage (VGS)
ICVES	LV7	Initial condition for Substrate-source voltage (VES)
VTH	LV9	Threshold voltage (bias dependent)
VDSAT	LV10	Saturation voltage (VDSAT)
PD	LV11	Drain diode periphery (PD)
PS	LV12	Source diode periphery (PS)
RDS	LV13	Drain resistance (squares) (RDS)
RSS	LV14	Source resistance (squares) (RSS)
GDEFF	LV16	Effective drain conductance (1/RDeff)
GSEFF	LV17	Effective source conductance (1/RSeff)
VES	LX1	Substrate-source voltage (VES)
VGS	LX2	Gate-source voltage (VGS)
VDS	LX3	Drain-source voltage (VDS)
CDO	LX4	DC drain current (CDO)
GMO	LX7	DC gate transconductance (GMO)

Name	Alias	Description
GDSO	LX8	DC drain-source conductance (GDSO)
GMESO	LX9	DC substrate transconductance (GMBSO)

Meyer and Charge Conservation Model Parameters

Name	Alias	Description
QB	LX12	Body charge (QB)
CQB	LX13	Body charge current (CQB)
QG	LX14	Gate charge (QG)
CQG	LX15	Gate charge current (CQG)
QD	LX16	Channel charge (QD)
CQD	LX17	Channel charge current (CQD)
CGGBO	LX18	CGGBO = ∂Qg/∂Vgb = CGS + CGD + CGB
CGDBO	LX19	CGDBO = ∂Qg/∂Vdb, (for Meyer CGD=-CGDBO)
CGSBO	LX20	CGSBO = ∂Qg/∂Vsb, (for Meyer CGS=-CGSBO)
CBGBO	LX21	CBGBO = ∂Qb/∂Vgb, (for Meyer CGB=-CBGBO)
CBDBO	LX22	CBDBO = ∂Qb/∂Vdb
CBSBO	LX23	CBSBO = ∂Qb/∂Vsb
CDGBO	LX32	CDGBO = ∂Qd/∂Vgb
CDDBO	LX33	CDDBO = ∂Qd/∂Vdb
CDSBO	LX34	CDSBO = ∂Qd/∂Vsb
QE	LX35	Substrate charge (QE)

Name	Alias	Description
CQE	LX36	Substrate charge current (CQE)
VBS	LX43	Body-source voltage (VBS)
ICH	LX44	Channel current
IBJT	LX45	Parasitic BJT collector current
III	LX46	Impact ionization current
IGIDL	LX47	GIDL current
ITUN	LX48	Tunneling current

Level 59 UC Berkeley BSIM3-SOI FD Model

The UC Berkeley SOI (BSIM3-SOI) Fully Depleted (FD) model is installed in the Avant! True-Hspice models as Level 59. This model is described in the "BSIM3SOI FD2.1 MOSFET MODEL User Manual," which can be found at "http://www-device.eecs.berkeley.edu/~bsim3soi".

The general syntax for including a BSIM3-SOI FD MOSFET element in a netlist is:

General Form

```
Mxxx nd ng ns ne <np> mname <L=val>
+ <W=val> <M=val> <AD=val> <AS=val> <PD=val> <PS=val>
+ <NRD=val> <NRS=val> <NRB=val> <RTH0=val> <CTH0=val>
+ <off> <BJToff=val> <IC=Vds, Vgs, Vbs, Ves, Vps>
```

where the angle brackets indicate optional parameters.

The arguments are as follows:

Mxxx	SOI MOSFET element name. Must begin with M, which can be followed by up to 1023 alphanumeric characters.
nd	Drain terminal node name or number
ng	Front gate node name or number
ns	Source terminal node name or number
ne	Back gate (or substrate) node name or number
np	Optional external body contact node name or number
mname	MOSFET model name reference
L	SOI MOSFET channel length in meters. This parameter overrides DEFL in an OPTIONS statement. Default=DEFL with a maximum of 0.1m.
W	MOSFET channel width in meters. This parameter overrides DEFW in an OPTIONS statement. Default=DEFW.

M	Multiplier to simulate multiple SOI MOSFETs in parallel. All channel widths, diode leakages, capacitances and resistances are affected by the setting of M. Default=1.
AD	Drain diffusion area. Overrides DEFAD in the OPTIONS statement. Default=DEFAD.
AS	Source diffusion area. Overrides DEFAS in the OPTIONS statement. Default=DEFAS.
PD	Perimeter of the drain junction, including the channel edge. Overrides DEFPD in the OPTIONS statement.
PS	Perimeter of the source junction, including the channel edge. Overrides DEFPS in the OPTIONS statement.
NRD	Number of squares of drain diffusion for drain series resistance. Overrides DEFNRD in the OPTIONS statement.
NRS	Number of squares of source diffusion for source series resistance. Overrides DEFNRS in the OPTIONS statement.
NRB	Number of squares for body series resistance.
RTH0	Thermal resistance per unit width ■ If not specified, RTH0 is extracted from the model card. ■ If specified, it overrides the one in the model card.
CTH0	Thermal capacitance per unit width ■ If not specified, CTH0 is extracted from model card. ■ If specified, it overrides the one in the model card.
OFF	Sets initial condition to OFF for this element in DC analysis
BJTOFF	Turning off BJT if equal to 1
IC	Initial guess in the order (drain, front gate, internal body, back gate, external voltage). (Vps is ignored in the case of 4-terminal device) These are used when UIC is present in the .TRAN statement and are overridden by the .IC statement.

Level 59 Model Parameters

Model Control Parameters

Parameter	Unit	Default	Description
CAPMOD	-	2	Flag for the short channel capacitance model
Level	-	-	Level 59 for BSIM3SOI
MOBMOD	-	1	Mobility model selector
NOIMOD	-	1	Flag for Noise model
SHMOD	-	0	Flag for self-heating: ■ 0 - no self-heating ■ 1 - self-heating

Process Parameters

Parameter	Unit	Default	Description
NCH	$1/cm^3$	1.7e17	Channel doping concentration
NGATE	$1/cm^3$	0	Poly gate doping concentration
NSUB	$1/cm^3$	6.0e16	Substrate doping concentration
TBOX	m	3.0e-7	Buried oxide thickness
TOX	m	1.0e-8	Gate oxide thickness
TSI	m	1.0e-17	Silicon film thickness

DC Parameters

Parameter	Unit	Default	Description
A0	-	1.0	Bulk charge effect coefficient for channel length
A1	1/V	0.0	First non-saturation effect parameter
A2	-	1.0	Second non-saturation effect parameter
ABP	-	1.0	Coefficient of A_{beff} dependency on V_{gst}
ADICE0	-	1	DICE bulk charge factor
AGIDL	1/W	0.0	GIDL constant
AGS	1/V	0.0	Gate bias coefficient of A_{bulk}
AII	1/V	0.0	First Leff dependence Vdsatii parameter
ALPHA0	m/V	0.0	The first parameter of impact ionization current
ALPHA1	1/V	1.0	The second parameter of impact ionization current
B0	m	0.0	Bulk charge effect coefficient for channel width
B1	m	0.0	Bulk charge effect width offset
BGIDL	V/m	0.0	GIDL exponential coefficient
BII	m/V	0.0	Second Leff dependence Vdsatii parameter

Parameter	Unit	Default	Description
CDSC	F/m^2	2.4e-4	Drain/source to channel coupling capacitance
CDSCB	F/m^2	0	Body-bias sensitivity of cdsc
CDSCD	F/m^2	0	Drain-bias sensitivity of cdsc
CII	-	0.0	First V_{ds} dependence Vdsatii parameter
CIT	F/m^2	0.0	Interface trap capacitance
DELP	V	0.02	Constant for limiting V_{bseff} to surface potential
DELTA	-	0.01	Effective V_{ds} parameter
DII	V	-1.0	Second V_{ds} dependence Vdsatii parameter
DROUT	-	0.56	L dependence coefficient of the DIBL correction parameter in R_{out}
DSUB	-	0.56	DIBL coefficient exponent
DVBD0	V	0	First coefficient of $V_{bs}0$ dependency on Leff
DVBD1	V	0	Second coefficient of $V_{bs}0$ dependency on Leff
DVT0	-	2.2	First coefficient of short-channel effect on V_{th}
DVT0W	-	0	First coefficient of narrow width effect on V_{th} for small channel length

Parameter	Unit	Default	Description
DVT1	-	0.53	Second coefficient of short-channel effect on V_{th}
DVT1W	-	5.3e6	Second coefficient of narrow width effect on V_{th} for small channel length
DVT2	1/V	-0.032	Body-bias coefficient of short-channel effect on V_{th}
DVT2W	1/V	-0.032	Body-bias coefficient of narrow width effect on V_{th} for small channel length
DWB	$m/V^{1/2}$	0.0	Coefficient of Weff's substrate body bias dependence
DWG	m/V	0.0	Coefficient of Weff's gate dependence
EDL	m	2e-6	Electron diffusion length
ETA0	-	0.08	DIBL coefficient in the subthreshold region
ETAB	1/V	-0.07	Body-bias coefficient for the subthreshold DIBL effect
ISBJT	A/m^2	1.0e-6	BJT injection saturation current
ISDIF	A/m^2	0	Body to source/drain injection saturation current
ISREC	A/m^2	1.0e-5	Recombination in depletion saturation current
ISTUN	A/m^2	0.0	Reverse tunneling saturation current

Parameter	Unit	Default	Description
K1	$V^{1/2}$	0.6	First-order body effect coefficient
K2	-	0	Second-order body effect coefficient
K3	-	0	Narrow coefficient
K3B	1/V	0	Body effect coefficient of k3
KB1	-	1	Coefficient of $V_{bs}0$ dependency on V_{gbs}
KB3	-	1	Coefficient of $V_{bs}0$ dependency on V_{gs} at subthreshold region
KBJT1	m/V	0	Parasitic bipolar early effect coefficient
KETA	m	-0.6	Body-bias coefficient of bulk charge effect
LINT	m	0.0	Length offset fitting parameter from I-V without bias
MXC	-	-0.9	Fitting parameter for A_{beff} calculation
NDIODE	-	1.0	Diode non-ideality factor
NFACTOR	-	1	Subthreshold swing factor
NGIDL	V	1.2	GIDL V_{ds} enhancement coefficient
NLX	m	1.74e-7	Lateral non-uniform doping parameter
NTUN	-	10.0	Reverse tunneling non-ideality factor

Parameter	Unit	Default	Description
PCLM	-	1.3	Channel length modulation parameter
PDIBL1	-	0.39	First output resistance DIBL effect correction parameter
PDIBL2	-	0.0086	Second output resistance DIBL effect correction parameter
PRWB	$1/V^{1}$	0	Body effect coefficient of Rdsw
PRWG	$1/V^{1/2}$	0	Gate bias effect coefficient of Rdsw
PVAG		0.0	Gate dependence of Early voltage
RBODY	ohm/m^2	0.0	Intrinsic body contact sheet resistance
RBSH	ohm/m^2	0.0	Extrinsic body contact sheet resistance
RDSW	$\Omega*\mu m^{wr}$	100	Parasitic resistance per unit width
RSH	ohm/square	0.0	Source/drain sheet resistance in ohm per square
U0	$cm^2/(V\text{-}sec)$	NMOS-670 PMOS-250	Mobility at Temp=Tnom
UA	m/V	2.25e-9	First-order mobility degradation coefficient
UB	$(m/V)^2$	5.87e-19	Second-order mobility degradation coefficient
UC	1/V	-0.0465	Body-effect of mobility degradation coefficient

Parameter	Unit	Default	Description
VBSA	V	0	Transition body voltage offset
VOFF	v	-0.08	Offset voltage in the subthreshold region for large W and L
VSAT	m/sec	8e4	Saturation velocity at Temp=Tnom
VTH0	v	NMOS 0.7 PMOS -0.7	Threshold voltage @ Vbs=0 for long wide device
W0	m	0	Narrow width parameter
WINT	m	0.0	Width offset fitting parameter from I-V without bias
WR	-	1	Width offset from Weff for R_{ds} calculation

AC and Capacitance Parameters

Parameter	Unit	Default	Description
ASD	V	0.3	Source/drain bottom diffusion smoothing parameter
CF	F/m	cal.	Gate to source/drain fringing field capacitance
CGDL	F/m	0.0	Lightly doped drain-gate region overlap capacitance
CGDO	F/m	calculated	Non LDD region drain-gate overlap capacitance per channel length
CGEO	F/m	0.0	Gate-substrate overlap capacitance per channel length

Parameter	Unit	Default	Description
CGSL	F/m	0.0	Lightly doped source-gate region overlap capacitance
CGSO	F/m	calculated	Non LDD region source-gate overlap capacitance per channel length
CJSWG	F/m^2	1.e-10	Source/drain (gate side) sidewall junction capacitance per unit width (normalized to 100nm Tsi)
CKAPPA	F/m	0.6	Coefficient for lightly doped region overlap capacitance fringing field capacitance
CLC	m	0.1e-7	Constant term for the short channel model
CLE	-	0.0	Exponential term for the short channel model
CSDESW	F/m	0.0	Source/drain sidewall fringing capacitance per unit length
CSDMIN	V	cal.	Source/drain bottom diffusion minimum capacitance
DLC	m	lint	Length offset fitting parameter for gate charge
DWC	m	wint	Width offset fitting parameter from C-V
MJSWG	V	0.5	Source/drain (gate side) sidewall junction capacitance grading coefficient

Parameter	Unit	Default	Description
PBSWG	V	0.7	Source/drain (gate side) sidewall junction capacitance built in potential
TT	second	1ps	Diffusion capacitance transit time coefficient
VSDFB	V	cal.	Source/drain bottom diffusion capacitance flatband voltage
VSDTH	V	cal.	Source/drain bottom diffusion capacitance threshold voltage
XPART	-	0	Charge partitioning rate flag

Temperature Parameters

Parameter	Unit	Default	Description
AT	m/sec	3.3e4	Temperature coefficient for U_a
CTH0	$m^oC/(W*s)$	0	Normalized thermal capacity
KT1	V	-0.11	Temperature coefficient for the threshold voltage
KT2	-	0.022	Body-bias coefficient of the threshold voltage temperature effect
KTIL	V*m	0	Channel length dependence of the temperature coefficient for the threshold voltage
PRT	Ω-um	0	Temperature coefficient for R_{dsw}
RTH0	m^oC/W	0	Normalized thermal resistance

Parameter	Unit	Default	Description
TNOM	^{o}C	25	Temperature at which parameters are expected
UA1	m/V	4.31e-9	Temperature coefficient for U_a
UB1	$(m/V)^2$	-7.61e-18	Temperature coefficient for U_b
UC1	1/V	-0.056	Temperature coefficient for U_c
UTE	-	-1.5	Mobility temperature exponent
XBJT	-	1	Power dependence of j_{bjt} on temperature
XDIF	-	XBJT	Power dependence of j_{dif} on temperature
XREC	-	1	Power dependence of j_{rec} on temperature
XTUN	-	0	Power dependence of j_{tun} on temperature

Note: BSIMFD refers substrate to the silicon below buried oxide, not the well region in BSIM3. It is used to calculated backgate flatband voltage (V_{fbb}) and parameters related to source/drain diffusion bottom capacitance (V_{sdth}, V_{sdfb}, C_{sdmin}). Positive nsub means the same type of doping as the body and negative nsub means opposite type of doping.

Level 59 Template Output

Additional element templates are added to this model for output of state variables, stored charges, capacitor currents and capacitances.

BSIM3SOI MOSFET FD (Level 59) Template Output

Name	Alias	Description
L	LV1	Channel length (L)
W	LV2	Channel width (W)
AD	LV3	Area of the drain diode (AD)
AS	LV4	Area of the source diode (AS)
ICVDS	LV5	Initial condition for drain-source voltage (VDS)
ICVGS	LV6	Initial condition for gate-source voltage (VGS)
ICVES	LV7	Initial condition for Substrate-source voltage (VES)
VTH	LV9	Threshold voltage (bias dependent)
VDSAT	LV10	Saturation voltage (VDSAT)
PD	LV11	Drain diode periphery (PD)
PS	LV12	Source diode periphery (PS)
RDS	LV13	Drain resistance (squares) (RDS)
RSS	LV14	Source resistance (squares) (RSS)
GDEFF	LV16	Effective drain conductance (1/RDeff)
GSEFF	LV17	Effective source conductance (1/RSeff)
COVLGS	LV36	Gate-source overlap capacitance
COVLGD	LV37	Gate-drain overlap capacitance
COVLGE	LV38	Gate-substrate overlap capacitance
VES	LX1	Substrate-source voltage (VES)
VGS	LX2	Gate-source voltage (VGS)

Name	Alias	Description
VDS	LX3	Drain-source voltage (VDS)
CDO	LX4	DC drain current (CDO)
CBSO	LX5	DC source-body diode current (CBSO)
CBDO	LX6	DC drain-body diode current (CBDO)
GMO	LX7	DC gate transconductance (GMO)
GDSO	LX8	DC drain-source conductance (GDSO)
GMESO	LX9	DC substrate transconductance (GMBSO)
GBDO	LX10	Conductance of the drain diode (GBDO)
GBSO	LX11	Conductance of the source diode (GBSO)

Meyer and Charge Conservation Model Parameters

Name	Alias	Description
QB	LX12	Body charge (QB)
CQB	LX13	Body charge current (CQB)
QG	LX14	Gate charge (QG)
CQG	LX15	Gate charge current (CQG)
QD	LX16	Channel charge (QD)
CQD	LX17	Channel charge current (CQD)
CGGBO	LX18	CGGBO = ∂Qg/∂Vgb = CGS + CGD + CGB
CGDBO	LX19	CGDBO = ∂Qg/∂Vdb, (for Meyer CGD=-CGDBO)
CGSBO	LX20	CGSBO = ∂Qg/∂Vsb, (for Meyer CGS=-CGSBO)

Name	Alias	Description
CBGBO	LX21	CBGBO = ∂Qb/∂Vgb, (for Meyer CGB=-CBGBO)
CBDBO	LX22	CBDBO = ∂Qb/∂Vdb
CBSBO	LX23	CBSBO = ∂Qb/∂Vsb
CDGBO	LX32	CDGBO = ∂Qd/∂Vgb
CDDBO	LX33	CDDBO = ∂Qd/∂Vdb
CDSBO	LX34	CDSBO = ∂Qd/∂Vsb
QE	LX35	Substrate charge (QE)
CQE	LX36	Substrate charge current (CQE)
CDEBO	LX37	CDEBO = ∂Qd/∂Veb
CBEBO	LX38	CBEBO = ∂Qb/∂Veb
CEEBO	LX39	CEEBO = ∂Qe/∂Veb
CEGBO	LX40	CEGBO = ∂Qe/∂Vgb
CEDBO	LX41	CEDBO = ∂Qe/∂Vdb
CESBO	LX42	CESBO = ∂Qe/∂Vsb
VBS	LX43	Body-source voltage (VBS)
ICH	LX44	Channel current
IBJT	LX45	Parasitic BJT collector current
III	LX46	Impact Ionization current
IGIDL	LX47	GIDL current
ITUN	LX48	Tunneling current

Level 60 UC Berkeley BSIM3-SOI DD Model

The UC Berkeley SOI model (BSIM3SOI) supports Fully Depleted (FD), Partially Depleted (PD), and Dynamically Depleted (DD) SOI devices.

BSIM3DD2.2 for DD SOI devices is installed in the Avant! True-Hspice models as Level 60.

This model is described in the "BSIM3DD2.1 MOSFET MODEL User's Manual," which can be found at

```
http://www-device.eecs.berkeley.edu/~bsim3soi
```

In BSIM3DD2.1, many advanced concepts are introduced to allow transition between PD and FD operation dynamically and continuously, namely the Dynamic Depletion approach.

Model Features

- Dynamic depletion approach is applied on both I-V and C-V. Charge and drain current are scalable with Tbox and Tsi continuously.
- Supports external body bias and backgate bias; a total of 6 nodes.
- Real floating body simulation in both I-V and C-V. Body potential is properly bounded by diode and C-V formulation.
- Self-heating implementation improved.
- Improved impact ionization current model.
- Various diode leakage components and parasitic bipolar current included.
- New depletion charge model (EBCI) introduced for better accuracy in capacitive coupling prediction. An improved BSIM3v3 based model is added as well.
- Dynamic depletion can suit different requirements for SOI technologies.
- Single I-V expression as in BSIM3v3.1 to assure continuities of Ids, Gds, Gm and their derivatives for all bias conditions.

Syntax

The general syntax for including a BSIM3SOI MOSFET element in a netlist is:

General Form

```
Mxxx nd ng ns ne <np> mname <L=val> <W=val> <M=val> <AD=val>
  <AS=val> <PD=val> <PS=val> <NRD=val> <NRS=val> <NRB=val>
  <RTHO=val> <CTHO=val> <off> <BJToff=val>
  <IC=Vds, Vgs, Vbs, Ves, Vps>
```

where the angle brackets indicate optional parameters.

The arguments are as follows:

Mxxx	SOI MOSFET element name. Must begin with M, which can be followed by up to 1023 alphanumeric characters
nd	Drain terminal node name or number
ng	Front gate node name or number
ns	Source terminal node name or number
ne	Back gate (or Substrate) node name or number
np	External body contact node name or number
mname	MOSFET model name reference
L	SOI MOSFET channel length in meters. This parameter overrides DEFL in an OPTIONS statement Default=DEFL with a maximum of 0.1m
W	SOI MOSFET channel width in meters. This parameter overrides DEFW in an OPTIONS statement Default=DEFW with a maximum of 0.1m
M	Multiplier to simulate multiple SOI MOSFETs in parallel. All channel widths, diode leakages, capacitances and resistances are affected by the setting of M Default=1

AD	Drain diffusion area. Overrides DEFAD in the OPTIONS statement Default=DEFAD
AS	Source diffusion area. Overrides DEFAS in the OPTIONS statement Default=DEFAS
PD	Perimeter of the drain junction, including the channel edge. Overrides DEFPD in the OPTIONS statement
PS	Perimeter of the source junction, including the channel edge. Overrides DEFPS in the OPTIONS statement
NRD	Number of squares of drain diffusion for drain series resistance. Overrides DEFNRD in the OPTIONS statement
NRS	Number of squares of source diffusion for source series resistance. Overrides DEFNRS in the OPTIONS statement
NRB	Number of squares for body series resistance
RDC	Additional drain resistance due to contact resistance with units of ohms. This value overrides the RDC setting in the model specification Default =0.0
RSC	Additional source resistance due to contact resistance with units of ohms. This value overrides the RDC setting in the model specification Default=0.0
RTHO	Thermal resistance per unit width ■ If not specified, RTHO is extracted from the model card ■ If specified, it will override the one in the model card
CTHO	Thermal capacitance per unit width ■ If not specified, CTHO is extracted from the model card ■ If specified, it will override the one in the model card

OFF	Sets initial condition to OFF for this element in DC analysis
BJTOFF	Turns off BJT if equal to 1
IC	Initial guess in the order (drain, front gate, internal body, back gate, external voltage). Vps will be ignored in the case of 4-terminal device. These are used when UIC is present in the .TRAN statement and are overridden by the .IC statement

Level 60 Model Parameters

Note: All additional BSIM3v3 parameters are shown in bold.

Table 10-2: BSIMSOI Model Control Parameters

SPICE Symbol	Description	Unit	Default	Notes (below)
level	**Level 60 for BSIMSOI**	**-**	**9**	**-**
shMod	**Flag for self-heating 0 - no self-heating 1 - self-heating**	**-**	**0**	
mobmod	Mobility model selector	-	1	-
capmod	Flag for the short channel capacitance model	-	2	**nI-1**
noimod	Flag for noise model	-	1	-

Table 10-3: Process Parameters

SPICE Symbol	Description	Unit	Default	Notes (below)
Tsi	**Silicon film thickness**	**m**	**10^{-7}**	**-**
Tbox	**Buried oxide thickness**	**m**	**$3x10^{-7}$**	**-**
Tox	Gate oxide thickness	m	$1x10^{-8}$	-
Nch	Channel doping concentration	1/ cm^3	$1.7x10^{17}$	-
Nsub	Substrate doping concentration	1/ cm^3	$6x10^{16}$	**nI-2**
ngate	Poly gate doping concentration	1/ cm^3	0	-

Table 10-4: DC Parameters *(Sheet 1 of 7)*

SPICE Symbol	Description	Unit	Default	Notes (below)
vth0	Threshold voltage @ V_{bs} =0 for long and wide device	-	0.7	**nI-3**
k1	First order body effect coefficient	$V^{1/2}$	0.6	-
k2	Second order body effect coefficient	-	0	-
k3	Narrow width coefficient	-	0	-
k3b	Body efficient coefficient of k3	1/V	0	-
Vbsa	**Transition body voltage offset**	**V**	**0**	**-**
delp	**Constant for limiting V_{bseff} to ϕ_s**	**V**	**0.02**	**-**

Table 10-4: DC Parameters *(Sheet 2 of 7)*

SPICE Symbol	Description	Unit	Default	Notes (below)
Kb1	**Coefficient of V_{bs0} dependency on V_{es}**	**-**	**1**	**-**
Kb3	**Coefficient of V_{bs0} dependency on V_{gs} at subthreshold region**	**-**	**1**	**-**
Dvbd0	**First coefficient of V_{bs0} dependency on L_{eff}**	**V**	**0**	**-**
Dvbd1	**Second coefficient of V_{bs0} dependency on L_{eff}**	**V**	**0**	**-**
w0	Narrow width parameter	m	0	-
nlx	Lateral non-uniform doping parameter	m	1.74e-7	-
dvt0	First coefficient of short-channel effect on Vth	-	2.2	-
dvt1	Second coefficient of short-channel effect on Vth	-	0.53	-
dvt2	Body-bias coefficient of short-channel effect on Vth	1/V	-0.032	-
dvt0w	First coefficient of narrow width effect on Vth for small channel length	-	0	-
dvt1w	Second coefficient of narrow width effect on Vth for small channel length	-	5.3e6	-
dvt2w	Body-bias coefficient of narrow width effect on Vth for small channel length	1/V	-0.032	-

Table 10-4: DC Parameters *(Sheet 3 of 7)*

SPICE Symbol	Description	Unit	Default	Notes (below)
u0	Mobility at Temp = Tnom NMOSFET PMOSFET	$cm^2/(V\text{-}sec)$	 670 250	-
ua	First-order mobility degradation coefficient	m/V	2.25e-9	-
ub	Second-order mobility degradation coefficient	$(m/V)^2$	5.9e-19	-
uc	Body-effect of mobility degradation coefficient	1/V	-.0465	-
vsat	Saturation velocity at Temp = Tnom	m/sec	8e4	-
a0	Bulk charge effect coefficient for channel length	-	1.0	-
ags	Gate bias coefficient of A_{bulk}	1/V	0.0	-
b0	Bulk charge effect coefficient for channel width	m	0.0	-
b1	Bulk charge effect width offset	m	0.0	-
keta	Body-bias coefficient of bulk charge effect	m	-0.6	-
Abp	**Coefficient of A_{beff} dependency on V_{gst}**	**-**	**1.0**	**-**
mxc	**Fitting parameter for A_{beff} calculation**	**-**	**-0.9**	**-**
adice0	**DICE bulk charge factor**	**-**	**1**	**-**
A1	First non-saturation effect parameter	1/V	0.0	-

Table 10-4: DC Parameters *(Sheet 4 of 7)*

SPICE Symbol	Description	Unit	Default	Notes (below)
A2	Second non-saturation effect parameter	0	1.0	-
rdsw	Parasitic resistance per unit width	W-mmWr	100	-
prwb	Body effect coefficient Rdsw	1/V	0	-
prwg	Gate bias effect coefficient of Rdsw	$1/V^{1/2}$	0	-
wr	Width offset from Weff for Rds calculation	-	1	-
wint	Width offset fitting parameter from I-V without bias	m	0.0	-
lint	Length offset fitting parameter from I-V without bias	m	0.0	-
dwg	Coefficient of W_{eff}'s gate dependence	m/V	0.0	
dwb	Coefficient of W_{eff}'s substrate body bias dependence	$m/V^{1/2}$	0.0	
voff	Offset voltage in the subthreshold region for large W and L	V	-0.08	-
nfactor	Subthreshold swing factor	-	1	-
eta0	DIBL coefficient in subthreshold region	-	0.08	-
etab	Body-bias coefficient for the subthreshold DIBL effect	1/V	-0.07	-
dsub	DIBL coefficient exponent	-	0.56	-
cit	Interface trap capacitance	F/m^2	0.0	-

Table 10-4: DC Parameters *(Sheet 5 of 7)*

SPICE Symbol	Description	Unit	Default	Notes (below)
cdsc	Drain/Source to channel coupling capacitance	F/m^2	2.4e-4	-
cdscb	Body-bias sensitivity of C_{dsc}	F/m^2	0	-
cdscd	Drain-bias sensitivity of C_{dsc}	F/m^2	0	-
pclm	Channel length modulation parameter	-	1.3	-
pdibl1	First output resistance DIBL effect correction parameter	-	.39	-
pdibl2	Second output resistance DIBL effect correction parameter	-	0.086	-
drout	L dependence coefficient of the DIBL correction parameter in Rout	-	0.56	-
pvag	Gate dependence of early voltage	-	0.0	-
delta	Effective V_{ds} parameter	-	0.01	-
aii	**1^{st} L_{eff} dependence V_{dsatii} parameter**	**1/V**	**0.0**	**-**
bii	**2^{nd} L_{eff} dependence V_{dsatii} parameter**	**m/V**	**0.0**	**-**
cii	**1^{st} V_{ds} dependence V_{dsatii} parameter**	**-**	**0.0**	**-**
dii	**2^{nd} dependence V_{dsatii} parameter**	**V**	**-1.0**	**-**
alpha0	First parameter of impact ionization current	m/V	0.0	-

Table 10-4: DC Parameters *(Sheet 6 of 7)*

SPICE Symbol	Description	Unit	Default	Notes (below)
alpha1	Second parameter of impact ionization current	1/V	1.0	-
beta0	Third parameter of impact ionization current	V	30	-
Agidl	**GIDL constant**	**Ω^{-1}**	**0.0**	-
Bgidl	**GIDL exponential coefficient**	**V/m**	**0.0**	-
Ngidl	**GIDL V_{ds} enhancement coefficient**	**V**	**1.2**	-
ntun	**Reverse tunneling non-ideality factor**	**-**	**10.0**	-
Ndiode	**Diode non-ideality factor**	**-**	**1.0**	-
Isbjt	**BJT injection saturation current**	**A/m^2**	**1e-6**	-
Isdif	**Body to source/drain injection saturation current**	**A/m^2**	**0.0**	-
Isrec	**Recombination in depletion saturation current**	**A/m^2**	**1e-5**	-
Istun	**Reverse tunneling saturation current**	**A/m^2**	**0.0**	-
Edl	**Electron diffusion length**	**m**	**2e-6**	-
Kbjt1	**Parasitic bipolar early effect coefficient**	**m/V**	**0**	-
Rbody	**Intrinsic body contact sheet resistance**	**ohm/m^2**	**0.0**	-
Rbsh	**Extrinsic body contact sheet resistance**	**ohm/m^2**	**0.0**	-

Table 10-4: DC Parameters *(Sheet 7 of 7)*

SPICE Symbol	Description	Unit	Default	Notes (below)
rsh	Source drain sheet resistance in ohm per square	Ω/square	0.0	-

Table 10-5: AC and Capacitance Parameters

SPICE Symbol	Description	Unit	Default	Notes (below)
xpart	Charge partitioning rate flag	-	0	
cgso	Non LDD region source-gate overlap capacitance per channel length	F/m	calcu-lated	**nC-1**
cgdo	Non LDD region drain-gate overlap capacitance per channel length	F/m	calcu-lated	**nC-2**
cgeo	**Gate substrate overlap capacitance per unit channel length**	**F/m**	**0.0**	**-**
cjswg	Source/Drain (gate side) sidewall junction Capacitance per unit width (normalized to 100nm T_{si})	F/m^2	1e-10	-
pbswg	Source/Drain (gate side) sidewall junction capacitance built in potential	V	.7	-
mjswg	Source/Drain (gate side) sidewall junction capacitance grading coefficient	V	0.5	-
tt	**Diffusion capacitance transit time coefficient**	**seco nd**	**1ps**	**-**

Table 10-5: AC and Capacitance Parameters *(Continued)*

SPICE Symbol	Description	Unit	Default	Notes (below)
vsdfb	**Source/drain bottom diffusion capacitance flatband voltage**	**V**	**calculated**	**nC-3**
vsdth	**Source/drain bottom diffusion capacitance threshold voltage**	**V**	**calculated**	**nC-4**
csdmin	**Source/drain bottom diffusion minimum capacitance**	**V**	**calculated**	**nC-5**
asd	**Source/drain bottom diffusion smoothing parameter**	**-**	**0.3**	**-**
csdesw	**Source/drain sidewall fringing capacitance per unit length**	**F/m**	**0.0**	**-**
cgs1	Light doped source-gate region overlap capacitance	F/m	0.0	-
cgd1	Light doped drain-gate region overlap capacitance	F/m	0.0	-
ckappa	Coefficient for lightly doped region overlap capacitance fringing field capacitance	F/m	0.6	-
cf	Gate to source/drain fringing field capacitance	F/m	calculated	**nC-6**
clc	Constant term for the short channel mode	m	0.1×10^{-7}	-
cle	Exponential term for the short channel mode	none	0.0	-
dlc	Length offset fitting parameter from C-V	m	lint	-
dwc	Width offset fitting parameter from C-V	m	wint	-

Table 10-6: Temperature Parameters

SPICE Symbol	Description	Unit	Default	Notes (below)
tnom	Temperature at which parameters are expected	^{o}C	27	-
ute	Mobility temperature exponent	none	-1.5	-
kt1	Temperature coefficient for threshold voltage	V	-0.11	-
kt11	Channel length dependence of the temperature coefficient for threshold voltage	V*m	0.0	
kt2	Body-bias coefficient of the Vth temperature effect	none	0.022	-
ua1	Temperature coefficient for U_a	m/V	4.31e-9	-
ub1	Temperature coefficient for U_b	$(m/V)^2$	-7.61e-18	-
uc1	Temperature coefficient for U_c	1/V	-.056	**nT-1**
at	Temperature coefficient for saturation velocity	m/sec	3.3e4	-
cth0	**Normalized thermal capacity**	**m^{o}C/(W*sec)**	**0**	**-**
prt	Temperature coefficient for Rdsw	Ω-μm	0	-
rth0	**Normalized thermal resistance**	**m^{o}C/W**	**0**	**-**

Table 10-6: Temperature Parameters *(Continued)*

SPICE Symbol	Description	Unit	Default	Notes (below)
xbjt	**Power dependence of j_{bjt} on temperature**	**none**	**2**	**-**
xdif	**Power dependence of j_{dif} on temperature**	**none**	**2**	**-**
xrec	**Power dependence of j_{rec} on temperature**	**none**	**20**	**-**
xtun	Power dependence of j_{tun} on temperature	none	0	-

Table 10-7: Model Parameter Notes

nI-1	*Capmod* 0 and 1 do not have the dynamic depletion calculation. Therefore, ddMod does not work with *capmod*.
nI-2	BSIMSOI refers substrate to the silicon below buried oxide, not the well region in BSIM3. It is used to calculate backgate flatband voltage (V_{fbb}) and parameters related to source/drain diffusion bottom capacitance (V_{sdth}, V_{sdfb}, C_{sdmin}). Positive n_{sub} means the same type of doping as the body and negative n_{sub} means opposite type of doping.

nC-1	If *cgso* is not given then it is calculated using:
	if (*dlc* is given and is greater than 0) then,
	*cgso=pl=(dlc*cox)-cgs1*
	■ if (the previously calculated cgso<0), then
	`cgso=0`
	■ else *cgso=0.6*Tsi*cox*

nC-2	*Cgdo* is calculated similar to *Csdo*

Table 10-7: Model Parameter Notes *(Continued)*

nC-3	If (n_{sub} is positive)
	$$V_{sdfb} = -\frac{kT}{q}\log\left(\frac{10^{20}\cdot n_{sub}}{n_i \cdot n_i}\right) - 0.3$$
	else
	$$V_{sdfb} = -\frac{kT}{q}\log\left(\frac{10^{20}}{n_{sub}}\right) + 0.3$$

nC-4	If (n_{sub} is positive)
	$$\phi_{sd} = 2\frac{kT}{q}\log\left(\frac{n_{sub}}{n_i}\right), \Upsilon_{sd} = \frac{5.753\text{x}10^{-12}\sqrt{n_{sub}}}{C_{box}}$$
	$$V_{sdth} = V_{sdfb} + \phi_{sd} + \Upsilon_{sd}\sqrt{\phi_{sd}}$$
	else
	$$\phi_{sd} = 2\frac{kT}{q}\log\left(-\frac{n_{sub}}{n_i}\right), \Upsilon_{sd} = \frac{5.753\text{x}10^{-12}\sqrt{-n_{sub}}}{C_{box}}$$
	$$V_{sdth} = V_{sdfb} - \phi_{sd} + -\Upsilon_{sd}\sqrt{\phi_{sd}}$$

nC-5	$$X_{sddep} = \sqrt{\frac{2\varepsilon_{si}\phi_{sd}}{q\left\|n_{sub}\cdot 10^{6}\right\|}}, C_{sddep} = \frac{\varepsilon_{si}}{X_{sddep}}, C_{sdmin} = \frac{C_{sddep}C_{box}}{C_{sddep}+C_{box}}$$
nC-6	If cf is not given then it is calculated using $$CF = \frac{2\varepsilon_{ox}}{\pi}1n\left(1+\frac{4\text{x}10^{-7}}{T_{ox}}\right)$$
nT-1	For mobmod=1 and 2, the unit is m/V^2. Default is -5.6E-11. For mobmod=3, unit is 1/V and default is -0.056.

Level 61 RPI a-Si TFT Model

Level 61 in the Avant! True-Hspice models is an AIM-SPICE MOS15 amorphous silicon (a-Si) thin-film transistor (TFT) model.

Model Features

AIM-SPICE MOS15 a-Si TFT model features include:

- Modified charge control model; induced charge trapped in localized states
- Above threshold includes:
  - Field effect mobility becoming a function of gate bias
  - Band mobility dominated by lattice scattering
- Below threshold
  - Fermi level located in deep localized states
  - Relate position of Fermi level, including the deep DOS back to the gate bias
- Empirical expression for current at large negative gate biases for hole-induced leakage current
- Interpolation techniques are applied to the equations to unify the model

Using Level 61

When using the AIM-SPICE MOS15 a-Si TFT model:

1. Set Level=61 to identify the model as the AIM-SPCIE MOS15 a-Si TFT model.
2. The default value for L is 100 m, and the default value for W is 100 m.
3. The Level 61 model is a 3-terminal model. No bulk node exists; therefore no parasitic drain-bulk or source-build diodes are appended to the model. A fourth node can be specified, but does not affect simulation results.
4. The default room temperature is 25C in the Avant! True-Hspice models, but is 27C in some other simulators. The user may choose whether or not to set the nominal simulation temperature to 27C, by adding .OPTION TNOM=27 to the netlist.

Example

This is an example of how the Avant! True-Hspice model and element statement modified for use with Level 61.

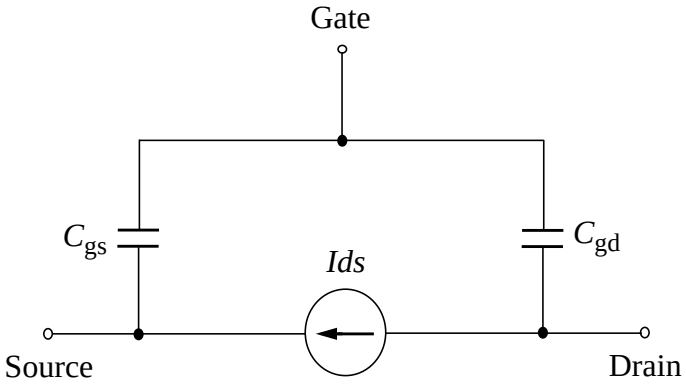
```
mckt drain gate source nch L=10e-6 W=10e-6
.MODEL nch nmos Level=61
+ alphasat = 0.6 cgdo = 0.0 cgso = 0.0 def0 = 0.6
+ delta = 5.0 el = 0.35 emu = 0.06 eps = 11
+ epsi = 7.4 gamma = 0.4 gmin = 1e23 iol = 3e-14
+ kasat = 0.006 kvt = -0.036 lambda = 0.0008 m = 2.5
+ muband = 0.001 rd = 0.0 rs = 0.0 sima0 = 1e-14
+ tnom = 27 tox = 1.0e-7 v0 = 0.12 vaa = 7.5e3
+ vdsl = 7 vfb = -3 vgsl = 7 vmin = 0.3 vto = 0.0
```

Level 61 Model Parameters

Name	Unit	Default	Description
ALPHASAT	-	0.6	Saturation modulation parameter
CGDO	F/m	0.0	Gate-drain overlap capacitance per meter channel width
CGSO	F/m	0.0	Gate-source overlap capacitance per meter channel width
DEF0	eV	0.6	Dark Fermi level position
DELTA	-	5	Transition width parameter
EL	eV	0.35	Activation energy of the hole leakage current
EMU	eV	0.06	Field effect mobility activation energy
EPS	-	11	Relative dielectric constant of substrate
EPSI	-	7.4	Relative dielectric constant of gate insulator
GAMMA	-	0.4	Power law mobility parameter
GMIN	$m^{-3}eV^{-1}$	1E23	Minimum density of deep states

Name	Unit	Default	Description
IOL	A	3E-14	Zero bias leakage current parameter
KASAT	1/°C	0.006	Temperature coefficient of ALPHASAT
KVT	V/°C	-0.036	Threshold voltage temperature coefficient
LAMBDA	1/V	0.0008	Output conductance parameter
M	-	2.5	Knee shape parameter
MUBAND	m^2/Vs	0.001	Conduction band mobility
RD	m	0.0	Drain resistance
RS	m	0.0	Source resistance
SIGMA0	A	1E-14	Minimum leakage current parameter
TNOM	^oC	25	Parameter measurement temperature
TOX	m	1E-7	Thin-oxide thickness
V0	V	0.12	Characteristic voltage for deep states
VAA	V	7.5E3	Characteristic voltage for field effect mobility
VDSL	V	7	Hole leakage current drain voltage parameter
VFB	V	-3	Flat band voltage
VGSL	V	7	Hole leakage current gate voltage parameter
VMIN	V	0.3	Convergence parameter
VTO	V	0.0	Zero-bias threshold voltage

Equivalent Circuit



Model Equations

Drain Current

$$I_{ds} = I_{leakage} + I_{ab}$$

$$I_{ab} = g_{ch} V_{dse} (1 + \mathrm{LAMBDA} \cdot V_{ds})$$

$$V_{dse} = \frac{V_{ds}}{[1 + (V_{ds}/V_{sate})^{M}]^{1/M}}$$

$$V_{sate} = \alpha_{sat} V_{gte}$$

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi}(RS + RD)}$$

$$g_{chi} = q n_s W \cdot \mathrm{MUBAND}/L$$

$$n_s = \frac{n_{sa} n_{sb}}{n_{sa} + n_{sb}}$$

$$n_{sa} = \frac{EPSI \cdot V_{gte}}{q \cdot TOX}\left(\frac{V_{gte}}{V_{aat}}\right)^{GAMMA}$$

$$n_{sb} = n_{so}\left(\frac{t_m}{TOX}\frac{V_{gfbe}}{V0}\frac{EPSI}{EPS}\right)^{\frac{2 \cdot V0}{V_e}}$$

$$n_{so} = N_c t_m \frac{V_e}{V0}\exp\left(-\frac{DEF0}{V_{th}}\right)$$

$$N_c = 3.0 \cdot 10^{25} m^{-3}$$

$$V_e = \frac{2 \cdot V0 \cdot V_{tho}}{2 \cdot V0 - V_{th}}$$

$$t_m = \sqrt{\frac{EPS}{2q \cdot GMIN}}$$

$$V_{gte} = \frac{VMIN}{2}\left[1 + \frac{V_{gt}}{VMIN} + \sqrt{DELTA^2 + \left(\frac{V_{gt}}{VMIN} - 1\right)^2}\right]$$

$$V_{gt} = V_{gs} - V_T$$

$$V_{gfbe} = \frac{VMIN}{2}\left[1 + \frac{V_{gfb}}{VMIN} + \sqrt{DELTA^2 + \left(\frac{V_{gfb}}{VMIN} - 1\right)^2}\right]$$

$$V_{gfb} = V_{gs} - VFB$$

$$I_{leakage} = I_{hl} + I_{min}$$

$$I_{hl} = IOL\left[\exp\left(\frac{V_{ds}}{VDSL}\right) - 1\right]\exp\left(-\frac{V_{gs}}{VGSL}\right)\exp\left[\frac{EL}{q}\left(\frac{1}{V_{tho}} - \frac{1}{V_{th}}\right)\right]$$

$$I_{min} = SIGMA0 \cdot V_{ds}$$

Temperature Dependence

$$V_{tho} = k_B \cdot TNOM / q$$

$$V_{th} = k_B \cdot (TEMP) / q$$

$$V_{aat} = VAA \exp\left[\frac{EMU}{q \cdot GAMMA}\left(\frac{1}{V_{th}} - \frac{1}{V_{tho}}\right)\right]$$

$$V_T = VTO + KVT(TEMP - TNOM)$$

$$\alpha_{sat} = ALPHASAT + KASAT(TEMP - TNOM)$$

Capacitance

$$C_{gs} = C_f + \frac{2}{3}C_{gc}\left[1 - \left(\frac{V_{sate} - V_{dse}}{2V_{sate} - V_{dse}}\right)^2\right]$$

$$C_{gd} = C_f + \frac{2}{3}C_{gc}\left[1 - \left(\frac{V_{sate}}{2V_{sate} - V_{dse}}\right)^2\right]$$

$$C_f = 0.5 \cdot EPS \cdot W$$

$$C_{gs} = q\frac{dn_{sc}}{dV_{gs}}$$

$$n_{sc} = \frac{n_{sac} n_{sbc}}{n_{sac} + n_{sbc}}$$

$$n_{sac} = \frac{EPSI \cdot V_{gte}}{q \cdot TOX}$$

$$n_{sbc} = n_{sb}$$

Level 62 RPI Poli-Si TFT Model

The Avant! True-Hspice Level 62 model is an AIM-SPICE MOS16 poly-silicon (Poli-Si) thin-film transistor (TFT) model.

Model Features

The AIM-SPICE MOS16 Poli-Si TFT model features include:

- A design based on the crystalline MOSFET model
- Field effect mobility that becomes a function of gate bias
- Effective mobility that accounts for trap states:
  - For low V_{gs}, it is power law
  - For high V_{gs}, it is constant
- Reverse bias drain current function of electric field near drain and temperature
- A design independent of channel length
- A unified DC model that includes all four regimes for channel lengths down to 4 m:
  - Leakage (thermionic emission)
  - Subthreshold (diffusion-like model)
  - Above threshold (c-Si-like, with mFet)
  - Kink (impact ionization with feedback)
- An AC model that accurately reproduces C_{gc} frequency dispersion
- An automatic scaling of model parameters that accurately model a wide range of device geometries

Using Level 62 with Avant! Simulators

When using the AIM-SPICE MOS16 Poli-Si TFT model:

1. Set Level=62 to identify the model as the AIM-SPICE MOS16 Poli-Si TFT model.
2. The default value for L is 100 m, and the default value for W is 100 m.

3. The Level 62 model is a 3-terminal model. No bulk node exists; therefore no parasitic drain-bulk or source-bulk diodes are appended to the model. A fourth node can be specified, but does not affect simulation results.
4. The default room temperature is 25^{o}C in the Avant! True-Hspice models, but is 27^{o}C in some other simulators. You can choose whether to set the nominal simulation temperature to 27^{o}C by adding .OPTION TNOM=27 to the netlist.

Example

This is an example of a True-Hspice model and element statement modified for use with Level 62:

```
mckt drain gate source nch L=10e-6 W=10e-6
.MODEL nch nmos Level=62
+ asat = 1 at = 3e-8 blk = 0.001 bt = 0.0 cgdo = 0.0
+ cgso = 0.0 dasat = 0.0 dd = 1.4e-7 delta = 4.0
+ dg = 2.0e-7 dmu1 = 0.0 dvt = 0.0 dvto = 0.0 eb = 0.68
+ eta = 7 etac0 = 7 etac00 = 0 i0 = 6.0 i00 = 150
+ lasat = 0lkink = 19e-6 mc = 3.0 mk = 1.3 mmu = 3.0
+ mu0 = 100 mu1 = 0.0022 mus = 1.0 rd = 0.0 rdx = 0.0
+ rs = 0.0 rsx = 0.0 tnom = 27 tox = 1.0e=7 vfb = -0.1
+ vkink = 9.1 von = 0.0 vto = 0.0
```

Level 62 Model Parameters

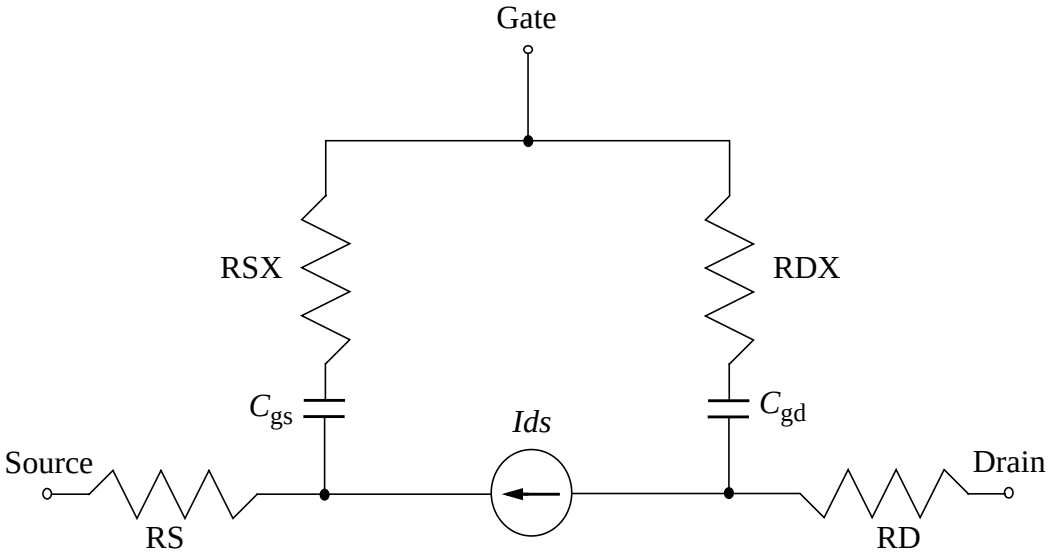
Name	Unit	Default	Description
ASAT	-	1	Proportionality constant of Vsat
AT	m/V	3E-8	DIBL parameter 1
BLK	-	0.001	Leakage barrier lowering constant
BT	m·V	1.9E-6	DIBL parameter 2
CAPMOD	-	0	Model capacitance selector (zero is recommended)

Name	Unit	Default	Description
CGDO	F/m	0	Gate-drain overlap capacitance per meter channel width
CGSO	F/m	0	Gate-source overlap capacitance per meter channel width
DASAT	1/°C	0	Temperature coefficient of ASAT
DD	m	1400 Å	Vds field constant
DELTA	-	4.0	Transition width parameter
DG	m	2000 Å	Vgs field constant
DMU1	$cm^2/Vs°C$	0	Temperature coefficient of MU1
DVT	V	0	The difference between VON and the threshold voltage
DVTO	V/°C	0	Temperature coefficient of VTO
EB	EV	0.68	Barrier height of diode
ETA	-	7	Subthreshold ideality factor
ETAC0	-	ETA	Capacitance subthreshold ideality factor at zero drain bias
ETAC00	1/V	0	Capacitance subthreshold coefficient of drain bias
I0	A/m	6.0	Leakage scaling constant
I00	A/m	150	Reverse diode saturation current
KSS	-	0	Small signal parameter (zero is recommended)
LASAT	M	0	Coefficient for length dependence of ASAT

Name	Unit	Default	Description
LKINK	M	19E-6	Kink effect constant
MC	-	3.0	Capacitance knee shape parameter
MK	-	1.3	Kink effect exponent
MMU	-	3.0	Low field mobility exponent
MU0	cm^2/Vs	100	High field mobility
MU1	cm^2/Vs	0.0022	Low field mobility parameter
MUS	cm^2/Vs	1.0	Subthreshold mobility
RD		0	Drain resistance
RDX	Ω	0	Resistance in series with C_{gd}
RS		0	Source resistance
RSX	Ω	0	Resistance in series with C_{gs}
TNOM	°C	25	Parameter measurement temperature
TOX	m	1e-7	Thin-oxide thickness
V0	V	0.12	Characteristic voltage for deep states
VFB	V	-0.1	Flat band voltage
VKINK	V	9.1	Kink effect voltage
VON	V	0	On-voltage
VSI	V	2.0	vgs dependence parameter
VST	V	2.0	vgs dependence parameter
VTO	V	0	Zero-bias threshold voltage

Name	Unit	Default	Description
ZEROC	-	0	Flag for capacitance calculations in capmod=1 (capmod=1:set the capacitance value 0, capmod=0:calculation capacitance).

Equivalent Circuit



Model Equations

Drain Current

Total Current

The total current is:

$$I_{ds} = \left(\frac{I_a \cdot I_{sub}}{I_a + I_{sub}} + I_{leak} \right) \cdot (1 + I_{kink})$$

Subthreshold Current

The expression for the subthreshold current is given by:

$$I_{sub} = MUS \cdot C_{ox} \frac{W}{L} V_{sth}^2 \exp\left(\frac{V_{GT}}{V_{sth}}\right)\left[1 - \exp\left(-\frac{V_{DS}}{V_{sth}}\right)\right]$$

$$I_{sub} = MUS \cdot C_{ox} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_{sth}^2 \cdot \exp\left(\frac{V_{GT}}{V_{sth}}\right) \cdot \left(1 - \exp\left(-\frac{V_{DS}}{V_{sth}}\right)\right)$$

$$C_{ox} = \frac{\varepsilon_i \cdot W_{eff} \cdot L_{eff}}{T_{ox}}$$

$$V_{sth} = ETA \cdot V_{th}$$

$$V_{th} = \frac{k_B \cdot TEMP}{q}$$

$$V_{GT} = V_{GS} - V_{Teff}$$

$$V_{Teff} = V_{TX} - \frac{AT \cdot {V_{DS}}^2 + BT}{L_{eff} \cdot \left(1 + \exp\left(\frac{V_{GS} - VST - VTX}{VSI}\right)\right)}$$

where $\varepsilon\iota$ is the dielectric constant of the oxide and k_B is the Boltzmanns constant.

Above threshold ($V_{GT} > 0$), the conduction current is given by:

$$I_a = \begin{cases} \dfrac{\mu_{FET} \cdot C_{ox} \cdot W_{eff}}{Leff} \left(V_{GTE} \cdot V_{DS} - \dfrac{{V_{DS}}^2}{2 \cdot \alpha_{sat}} \right) & \text{for } V_{DS} \le \alpha_{sat} V_{GTE} \\ \dfrac{\mu_{FET} \cdot C_{ox} \cdot W_{eff} \cdot {V_{GTE}}^2 \cdot \alpha_{sat}}{2 \cdot L_{eff}} & \text{for } V_{DS} > \alpha_{sat} V_{GTE} \end{cases}$$

$$\frac{1}{\mu_{FET}} = \frac{1}{MUO} + \frac{1}{\mu 1 \cdot \left(\dfrac{2 \cdot V_{GTE}}{V_{sth}} \right)^{MMU}}$$

$$V_{GTE} = V_{sth} \cdot \left[1 + \frac{V_{GT}}{2 \cdot V_{sth}} + \sqrt{DELTA^2 + \left(\frac{V_{GT}}{2 \cdot V_{sth}} - 1 \right)^2} \right]$$

Subthreshold Leakage Current

Subthreshold leakage current is the result of thermionic field emission of carriers through the grain boundary trap states and is described by:

$$I_{leak} = IO \cdot W_{eff} \cdot \left[\exp\left(\frac{q \cdot BLK \cdot V_{DS}}{k \cdot T} \right) - 1 \right] \cdot \left(X_{TFE} + X_{TE} \right) + I_{diode}$$

$$X_{TFE} = \frac{X_{TFE,lo} \cdot X_{TFE,hi}}{X_{TFE,lo} + X_{TFE,hi}}$$

where:

$$X_{TE} = \exp(-W_c)$$

$$W_c = \frac{E_c - E_t}{k \cdot T} = \frac{0.55eV}{k \cdot T}$$

$$X_{TFE,lo} = \begin{cases} \frac{4\sqrt{\pi}}{3} \cdot \mathrm{f} \cdot \exp\left(\frac{4}{27} \cdot f^2 - W_c\right) & \text{for } f \le f_{lo} \\ X_{TFE,lo}(f_{lo}) \exp\left[\left(\frac{1}{f_{lo}} + \frac{8}{27} \cdot f_{lo}\right) \cdot (f - f_{lo})\right] & \text{for } f > f_{lo} \end{cases}$$

$$f = \frac{F_{\min}}{2}\left[1 + \frac{\frac{F_f}{F_{fo}}}{F_{\min}} + \sqrt{DELTA^2 + \left(\frac{\frac{F_f}{F_{fo}}}{F_{\min}} - 1\right)^2}\right]$$

$$F_{\min} = 1e^{-4}$$

$$X_{TFE,lo}(f_{lo}) = \frac{2\sqrt{4\pi}}{3} \cdot f_{lo} \cdot \exp\left(\frac{4}{27} {f_{lo}}^2 - W_c\right)$$

$$F_f = \left(\frac{V_{DS}}{DD} - \frac{V_{GS} - VFB}{DG}\right)$$

$$F_{fo} = (k \cdot T)^{3/2} \cdot \left(\frac{4}{3} \cdot \frac{2\pi\sqrt{2m^*}}{q \cdot h}\right)$$

$$m^* = 0.27 \cdot m_0$$

$$f_{lo} = \frac{3}{2} \cdot \left(\sqrt{W_c + 1} - 1\right)$$

$$X_{TFE,hi} = \begin{cases} \frac{2W_c}{3} \cdot \exp\left(1 - \frac{2W_c}{3}\right) & \text{for } f < f_{hi} \\ \left(1 - \frac{3\sqrt{W_c}}{2 \cdot f}\right)^{-1} \exp\left[\frac{-{W_c}^{3/2}}{f}\right] & \text{for } f \geq f_{hi} \end{cases}$$

$$f_{hi} = 3 \cdot \left(\frac{{W_c}^{3/2}}{2W_c - 3}\right)$$

$$I_{diode} = IOO \cdot W_{eff} \cdot \exp\left(-\frac{EB}{k \cdot T}\right)\left[1 - \exp\left(-\frac{q \cdot V_{DS}}{k \cdot T}\right)\right]$$

Impact Inonization Effect

Finally, for very large drain biases, the kink effect is observed. It is modeled as impact ionization in a narrow region near the drain. The impact ionization current, *Ikink*, is added to the drain current.

The expression can be written as:

$$I_{kink} = A_{kinkt} \cdot (V_{DS} - V_{DSE}) \cdot \exp\left(-\frac{VKINK}{V_{DS} - V_{DSE}}\right)$$

$$A_{kinkt} = \frac{1}{VKINK}\left(\frac{LKINK}{L_{eff}}\right)^{MK}$$

$$V_{DSE} = \frac{V_{DS}}{\left(1 + \left(\frac{V_{DS}}{V_{DSAT}}\right)^3\right)^{1/3}} - V_{th}$$

$$V_{DSAT} = \alpha_{sat} \cdot V_{GTE}$$

Threshold Voltage

If VTO is not specified:

$$V_T = VON - DVT$$

else:

$$V_T = VTO$$

Temperature Dependence

$$V_{TX} = V_T - DVTO \cdot (TEMP - TNOM)$$
$$\mu_1 = MU1 + DMU1 \cdot (TEMP - TNOM)$$
$$\alpha_{sat} = ASAT - \frac{LASAT}{L_{eff}} - DASAT \cdot (TEMP - TNOM)$$

Capacitance

CAPMOD=0:

$$C_{gs} = C_f + \frac{2}{3}\cdot C_{gcs}\cdot\left[1-\left(\frac{V_{DSAT}-V_{DSEX}}{2V_{DSAT}-V_{DSEX}}\right)^2\right]$$

$$C_{gd} = C_f + \frac{2}{3}\cdot C_{\mathrm{gcd}}\cdot\left[1-\left(\frac{V_{DSAT}}{2V_{DSAT}-V_{DSEX}}\right)^2\right]$$

$$C_f = 0.5\cdot EPS\cdot W_{eff}$$

$$C_{\mathrm{gcd}} = \frac{C_{ox}}{1+\eta_{cd}\cdot\exp\left(-\frac{V_{GTX}}{\eta_{cd}\cdot V_{th}}\right)}$$

$$C_{gcs} = \frac{C_{ox}}{1+ETAC0\cdot\exp\left(-\frac{V_{GTX}}{ETAC0\cdot V_{th}}\right)}$$

$$C_{ox} = \frac{W_{eff}\cdot L_{eff}\cdot\varepsilon_i}{TOX},\quad \eta_{cd} = ETAC0 + ETAC00\cdot V_{DSEX}$$

$$V_{DSEX} = \frac{V_{DS}}{\left[1+\left(\frac{V_{DS}}{V_{DSAT}}\right)^{MC}\right]^{\frac{1}{MC}}}$$

$$V_{GTX} = V_{GS} - V_{TX}$$

CAPMOD=1:

If ZEROC is equal to 1:

$$V_{gst} = V_{GS} - V_{TX}$$
$$Phi = 0.6$$

- $V_{gst} < \frac{-phi}{2}$ $\qquad C_{gs} = C_{gd} = 0$
- $\frac{-phi}{2} \le V_{gst} < 0$ $\qquad C_{gs} = \frac{4 \cdot V_{gst} \cdot C_{ox}}{3 \cdot Phi} + \frac{2 \cdot C_{ox}}{3}, C_{gd} = 0$
- $V_{gst} \ge 0$

$$\begin{cases} V_{DS} \ge V_{DSAT} & C_{gs} = \frac{2C_{ox}}{3}, \quad C_{gd} = 0 \\ V_{DS} < V_{DSAT} & Cgd = \frac{2}{3} \cdot Cox \cdot \left[1 - \left(\frac{V_{DSAT}}{2V_{DSAT} - V_{DSEX}} \right)^2 \right] \\ & Cgs = \frac{2}{3} \cdot Cox \cdot \left[1 - \left(\frac{V_{DSAT} - V_{DSE}}{2V_{DSAT} - V_{DSEX}} \right)^2 \right] \end{cases}$$

$$C_{ox} = \frac{\varepsilon_i \cdot W_{eff} \cdot L_{eff}}{T_{ox}}$$

$$V_{DSEX} = \frac{V_{DS}}{\left[1 + \left(\frac{V_{DS}}{V_{DSAT}}\right)^{MC}\right]^{\frac{1}{MC}}}$$

Geometry Effect

$$W_{eff} = W + XW$$
$$L_{eff} = L + XL$$

Level 63 Phillips MOS11 Model

The Philips MOS Model 11, Level 1100, is available as Level 63 in the Avant! True-Hspice models (based on the “Unclassified Report NL-UR 2001/813” by R. Langevelde). Also, for the parasitic diode model, the Philips JUNCAP Parasitic Diode Model was added.

For additional information regarding the MOS Model 11 and the Philips JUNCAP Parasitic Diode Model, see:

http://www.semiconductors.philips.com/Philips_Models

Using the Phillips MOS11 Model

1. Set Level=63 to identify the model as Philips MOS Model 11.
2. The default room temperature is 25 in the Avant! True--Hspice models, but is 27 in most other simulators. When comparing to other simulators, set the simulation temperature to 27, using either .TEMP 27 or .OPTIONS TNOM=27.
3. The set of model parameters should always include the model reference temperature, TR, which corresponds to TREF in other levels in the Avant! True-Hspice models. The default for TR is 21.0, to match the Philips simulator.
4. The model has its own charge-based capacitance model. This model ignores the CAPOP parameter, which selects different capacitance models.
5. The model uses the analytical derivatives for the conductances. This model ignores the DERIV parameter, which selects the finite difference method.
6. You can use DTEMP with this model. DTEMP increases the temperature of individual elements, relative to the circuit temperature. Set DTEMP on the element line.
7. Because the defaults are non-zero, you should set *every* model parameter listed in the Level 63 Model Parameters table, in the .MODEL statement.

8. The general syntax for the MOSFET element is the same as the other standard MOSFET models, other than PS and PD. In Level=63, PS and PD are the length of the sidewall of the source/drain, which is not under the gate.
9. MOS11 has its own LMIN parameter, which has a different definition from that of Star-Hspice and Star-Sim simulators. To avoid the conflict with LMIN in simulation, the LMIN parameter in HPICE Level=63 was changed to LLMIN.

Description of Parameters

Table 10-8: Level 63 MOS11 Parameters *(Sheet 1 of 10)*

Name	Description	Units	NMOS	PMOS
LEVEL	Level of this model	-	1	1
LER	Effective channel length of the reference transistor	m	1E-6	1E-6
WER	Effective channel width of the reference transistor	m	1E-5	1E-5
LVAR	Difference between the actual and the programmed poly silicon gate length	m	0	0
LAP	Effective channel length reduction per side due to the lateral diffusion of the source/ drain dopant ions	m	4E-8	4E-8
WVAR	Difference between the actual and the programmed field oxide opening	m	0	0

Table 10-8: Level 63 MOS11 Parameters *(Sheet 2 of 10)*

Name	Description	Units	NMOS	PMOS
WOT	Effective reduction of the channel width per side due to the lateral diffusion of the channel stop dopant ions	m	0	0
TR	Temperature at which the parameters for the reference transistor have been determined	^{o}C	21	21
VFBR	Flat-band voltage for the reference transistor at the reference temperature	V	-1.05	-1.05
STVFB	Coefficient of the temperature dependence of V_{FB}	V/K	5E-4	5E-4
KOR	Body-effect factor for the reference transistor	$V^{1/2}$	0.5	0.5
SLKO	Coefficient of the length dependence of k_O	$V^{1/2}m$	0	0
SL2KO	Second coefficient of the length dependence of k_O	$V^{1/2}m^2$	0	0
SWKO	Coefficient of the width dependence of k_O	$V^{1/2}m$	0	0
KPINV	Inverse of body –effect factor of the poly-silicon gate	$V^{-1/2}$	0	0
PHIBR	Surface potential at the onset of strong inversion at the reference temperature	V	0.95	0.95

Table 10-8: Level 63 MOS11 Parameters *(Sheet 3 of 10)*

Name	Description	Units	NMOS	PMOS
SLPHIB	Coefficient of the length dependence of ϕ_B	Vm	0	0
SL2PHIB	Second coefficient of the length dependence of ϕ_B	Vm^2	0	0
SWPHIB	Coefficient of the width dependence of ϕ_B	Vm	0	0
BETSQ	Gain factor for an infinite square transistor at the reference temperature	AV^{-2}	3.709E-4	1.15E-4
ETABET	Exponent of the temperature dependence of the gain factor	-	1.3	0.5
FBET1	Relative mobility decrease due to first lateral profile	-	0	0
LP1	Characteristic length of first lateral profile	m	8E-7	8E-7
FBET2	Relative mobility decrease due to second lateral profile	-	0	0
LP2	Characteristic length of second lateral profile	m	8E-7	8E-7
THESRR	Coefficient of the mobility reduction due to surface roughness scattering for the reference transistor at the reference temperature	V^{-1}	0.4	0.73
SWTHESR	Coefficient of the width dependence of θ_{SR}	m	0	0

Table 10-8: Level 63 MOS11 Parameters *(Sheet 4 of 10)*

Name	Description	Units	NMOS	PMOS
THEPHR	Coefficient of the mobility reduction due to phonon scattering for the reference transistor at the reference temperature	V^{-1}	1.29E-2	1E-3
ETAPH	Exponent of the temperature dependence of θ_{SR} for the reference temperature	-	1.75	1.75
SWTHEPH	Coefficient of the width dependence of θ_{SR}	m	0	0
ETAMOBR	Effective field parameter for dependence on depletion/ inversion charge for the reference transistor	-	1.4	3
STETAMOB	Coefficient of the temperature dependence of η_{MOB}	K^{-1}	0	0
SWETAMOB	Coefficient of the width dependence of η_{MOB}	m	0	0
NUR	Exponent of the field dependence of the mobility model minus 1(i.e. ν-1) at the reference temperature	-	1	1
NUEXP	Exponent of the temperature dependence of parameter n	-	5.25	3.23

Table 10-8: Level 63 MOS11 Parameters *(Sheet 5 of 10)*

Name	Description	Units	NMOS	PMOS
THERR	Coefficient of the series resistance for the reference transistor at the reference temperature	V^{-1}	0.155	0.08
ETAR	Exponent of the temperature dependence of θ_R	-	0.95	0.4
SWTHER	Coefficient of the width dependence of θ_R	m	0	0
THER1	Numerator of the gate voltage dependent part of series resistance for the reference transistor	V	0	0
THER2	Denominator of the gate voltage dependent part of series resistance for the reference transistor	V	1	1
THESATR	Velocity saturation parameter due to optical/acoustic phonon scattering for the reference transistor at the reference temperature	V^{-1}	0.5	0.2
SLTHESAT	Coefficient of the length dependence of θ_{SAT}	-	1	1
THESATEXP	Exponent of the length dependence of θ_{SAT}	-	1	1
ETASAT	Exponent of the temperature dependence of θ_{SAT}	-	1.04	0.86

Table 10-8: Level 63 MOS11 Parameters *(Sheet 6 of 10)*

Name	Description	Units	NMOS	PMOS
SWTHESAT	Coefficient of the width dependence of θ_{SAT}	m	0	0
THETHR	Coefficient of self-heating for the reference transistor at the reference temperature	V^{-3}	1E-3	1E-3
THETHEXP	Exponent of the length dependence of θ_{TH}	-	1	1
SWTHETH	Coefficient of the width dependence of θ_{TH}	m	0	0
SDIBLO	Drain-induced barrier-lowering parameter for the reference transistor	$V^{-1/2}$	2E-3	1E-3
SDIBLEXP	Exponent of the length dependence of σ_{DIBL}	-	1.35	1.35
MOR	Parameter for short-channel subthreshold slope for the reference transistor	-	0	0
MOEXP	Exponent of the length dependence of m_O	-	1.34	1.34
SSFR	Static feedback parameter for the reference transistor	$V^{-1/2}$	6.25E-3	6.25E-3
SLSSF	Coefficient of the length dependence of σ_{SF}	m	1E-6	1E-6
SWSSF	Coefficient of the width dependence of σ_{SF}	m	0	0

Table 10-8: Level 63 MOS11 Parameters *(Sheet 7 of 10)*

Name	Description	Units	NMOS	PMOS
ALPR	Factor of the channel length modulation for the reference transistor	-	1E-2	1E-2
SLALP	Coefficient of the length dependence of α	-	1	1
ALPEXP	Exponent of the length dependence of α	-	1	1
SWALP	Coefficient of the width dependence of α	m	0	0
VP	Characteristic voltage of the channel length modulation	V	5E-2	5E-2
LLMIN	Minimum effective channel length in technology, used for calculation of smoothing factor m	m	1.5E-7	1.5E-7
A1R	Factor of the weak-avalanche current for the reference transistor at the reference temperature	-	6	6
STA1	Coefficient of the temperature dependence of a_1	K^{-1}	0	0
SLA1	Coefficient of the length dependence of a_1	m	0	0
SWA1	Coefficient of the width dependence of a_1	m	0	0

Table 10-8: Level 63 MOS11 Parameters *(Sheet 8 of 10)*

Name	Description	Units	NMOS	PMOS
A2R	Exponent of the weak-avalanche current for the reference transistor	V	38	38
SLA2	Coefficient of the length dependence of a_2	Vm	0	0
SWA2	Coefficient of the width dependence of a_2	Vm	0	0
A3R	Factor of the drain-source voltage above which weak-avalanche occurs, for the reference transistor	-	1	1
SLA3	Coefficient of the length dependence of a_3	m	0	0
SWA3	Coefficient of the width dependence of a_3	m	0	0
IGINVR	Gain factor for intrinsic gate tunneling current in inversion for the reference transistor	AV^{-2}	0	0
BINV	Probability factor for intrinsic gate tunneling current in inversion	V	48	48
IGACCR	Gain factor for intrinsic gate tunneling current in accumulation for the reference transistor	AV^{-2}	0	0

Table 10-8: Level 63 MOS11 Parameters *(Sheet 9 of 10)*

Name	Description	Units	NMOS	PMOS
BACC	Probability factor for intrinsic gate tunneling current in accumulation	V	48	48
VFBOV	Flat-band voltage for the Source/Drain overlap extensions	V	0	0
KOV	Body-effect factor for the Source/Drain overlap extensions	$V^{1/2}$	2.5	2.5
IGOVR	Gain factor for Source/Drain overlap tunneling current for the reference transistor	AV^{-2}	0	0
TOX	Thickness of the gate oxide layer	m	3.2E-9	3.2E-9
COL	Gate overlap capacitance per unit channel length	Fm^{-1}	3.2E-10	3.2E-10
GATENOISE	Flag for in/exclusion of induced gate thermal noise	-	0	0
NTR	Coefficient of the thermal noise at the actual temperature	J	1.656E-20	1.656E-20
NFAR	First coefficient of the flicker noise for the reference transistor	$V^{-1}m^{-4}$	1.573E22	1.573E22
NFBR	Second coefficient of the flicker noise for the reference transistor	$V^{-1}m^{-2}$	4.752E8	4.752E8

Table 10-8: Level 63 MOS11 Parameters *(Sheet 10 of 10)*

Name	Description	Units	NMOS	PMOS
NFCR	Third coefficient of the flicker noise for the reference transistor	V^{-1}	0	0

Table 10-9: Level 63 JUNCAP Parameters

Name	Description	Units	Default
DTA	Temperature offset of the JUNCAP element with respect toT_A	^oC	0
VR	Voltage at which the parameters have been determined	V	0
JSGBR	Bottom saturation-current density due to electron-hole generation at $V=V_R$	Am^{-2}	1E-03
JSDBR	Bottom saturation-current density due to diffusion from back contact	Am^{-2}	1E-03
JSGSR	Sidewall saturation-current density due to electron-hole generation at $V=V_R$	Am^{-1}	1E-03
JSDSR	Sidewall saturation-current density due to diffusion from back contact	Am^{-1}	1E-03
JSGGR	Gate edge saturation-current density due to electron-hole generation at $V=V_R$	Am^{-1}	1E-03
JSDGR	Gate edge saturation-current density due to diffusion from back contact	Am^{-1}	1E-03
NB	Emission coefficient of the bottom forward current	-	1
NS	Emission coefficient of the sidewall forward current	-	1

Table 10-9: Level 63 JUNCAP Parameters *(Continued)*

Name	Description	Units	Default
NG	Emission coefficient of the gate edge forward current	-	1
CJBR	Bottom junction capacitance at $V=V_R$	Fm^{-2}	1E-12
CJSR	Sidewall junction capacitance at $V=V_R$	Fm^{-1}	1E-12
CJGR	Gate edge junction capacitance at $V=V_R$	Fm^{-1}	1E-12
VDBR	Diffusion voltage of the bottom junction at $T=T_R$	V	1
VDSR	Diffusion voltage of the sidewall junction at $T=T_R$	V	1
VDGR	Diffusion voltage of the gate-edge junction at $T=T_R$	V	1
PB	Bottom junction grading coefficient	-	0.4
PS	Sidewall junction grading coefficient	-	0.4
PG	Gate edge junction grading coefficient	-	0.4

Note: All symbols refer to “Unclassified Report NL-UR 2001/813”.

Example

```
.model nch nmos level=63
+LER     = 1E-06       WER       = 1E-05       LAP       = -1.864E-08
+TR      = 21          VFBR      = -1.038      SLPHIB    = -1.024E-08
+SL2PHIB = 1.428E-14   KOR       = 5.763E-01   SLKO      = 2.649E-08
+SL2KO   =-1.737E-14   KPINV     = 2.2E-01     PHIBR     = 0.85
+BETSQ   = 1.201E-04   ETABET    = 1.3         FBET1     =-3.741000E-01
+LP1     = 2.806E-06   LP2       = 1E-10       THESATEXP = 2
+THESRR  = 7.109E-01   THEPHR    = 1E-03       TOX       = 3.2E-09
+ETAPH   = 1.75E+00    ETAMOBR   = 2.825       NUR       = 1
+NUEXP   = 3.228       THERR     = 1.267E-01   ETAR      = 0.4
+THER2   = 1           THESATR   = 6.931E-02   SLTHESAT  = 1
+ETASAT  = 8.753E-01   SSFR      = 2.304E-03   VP        = 5E-02
+SLSSF   = 1.002E-06   ALPR      = 1.062E-02   SLALP     = 9.957E-01
+ALPEXP  = 1.039       THETHR    = 2.413E-03   THETHEXP  = 1
+SDIBLO  = 1.06E-06    SDIBLEXP  = 6.756       LLMIN     = 2E-07
+MOR     = 1.05E-03    MOEXP     = 3.146
+A1R     = 9.938E+04   STA1      = 9.3E-02     SLA1      =-2.805E-03
+A2R     = 4.047E+01   SLA2      = 1E-15
+A3R     = 7.54E-01    SLA3      =-8.705E-08
+COL     = 3.2E-10
+NTR     = 1.6237E-20  NFAR      = 1           NFBR      = 0
+NFCR    = 0           GATENOISE =0
+CJBR    = 1.347E-3    CJSR      = 0.183E-9    CJGR      = 0.374E-9
+JSDBR   = 0.027E-6    JSDSR     = 0.040E-12   JSDGR     = 0.100E-12
+VR      = 0.000
+JSGBR   = 1.900E-6    JSGSR     =78.000E-12   JSGGR     = 54.000E-12
+VB      = 20.000
+VDBR    = 0.828       VDSR      = 0.593       VDGR      = 0.500
+PB      = 0.394       PS        = 0.171       PG        = 0.193
+NB      = 1.000       NS        = 1.000       NG        = 1.000
```

Avant!

Appendix A
Ideal and Lumped Transmission Lines

A transmission line delivers an output signal at a distance from the point of signal input. Any two conductors can make up a transmission line. The signal that is transmitted from one end of the pair to the other end is the voltage between the conductors. Power transmission lines, telephone lines, and waveguides are examples of transmission lines. Traces on printed circuit boards and multichip modules (MCMs) in integrated circuits are other electrical elements that are examples of transmission lines.

With current technologies that use high-speed active devices on both ends of most circuit traces, all of the following transmission line effects must be considered during circuit analysis:

- Time delay
- Phase shift
- Power, voltage, and current loss
- Distortion
- Reduction of frequency bandwidth
- Coupled line crosstalk

Avant! provides accurate modeling for all kinds of circuit connections, including both lossless (ideal) and lossy transmission line elements.

This chapter describes:

Selecting Wire Models

A transmission line or interconnect is one of the following:

- Wire
- Trace
- Conductor
- Line

Many applications model electrical properties of interconnections between nodes by their equivalent circuits, and integrate them into the system simulation to accurately predict system performance.

An electrical model that simulates the behavior of interconnect must consider all of the following:

- Physical nature or electrical properties of the interconnect
- Bandwidth or risetime and source impedance of signals of interest
- Interconnect's actual time delay
- Complexity and accuracy of the model, and the corresponding effects on the amount of CPU time required for simulations

You can choose from the following circuit models for interconnects:

- No model at all. Use a common node to connect two elements.
- Lumped models with R, L, and C Elements, as described in Chapter 13, "Statistical Analysis and Optimization", in the *Star-Hspice Manual*. These include a series resistor (R), a shunt capacitor (C), a series inductor and resistor (RL), and a series resistor and a shunt capacitor (RC).
- Transmission line models such as an ideal transmission line (T Element) or a lossy transmission line (U Element)

Choosing the simplest model that adequately simulates the required performance minimizes sources of confusion and error during analysis.

Generally, to simulate both low and high frequency electrical properties of interconnects, select the U Element transmission line model. For compatibility with conventional versions of SPICE, use one a discrete lumped model or the T Element.

Following are the factors that determine the best choice of a transmission line:

Source properties

t_{rise} = source risetime

R_{source} = source output impedance

Interconnect properties

Z0 = characteristic impedance

TD = time delay of the interconnection

or

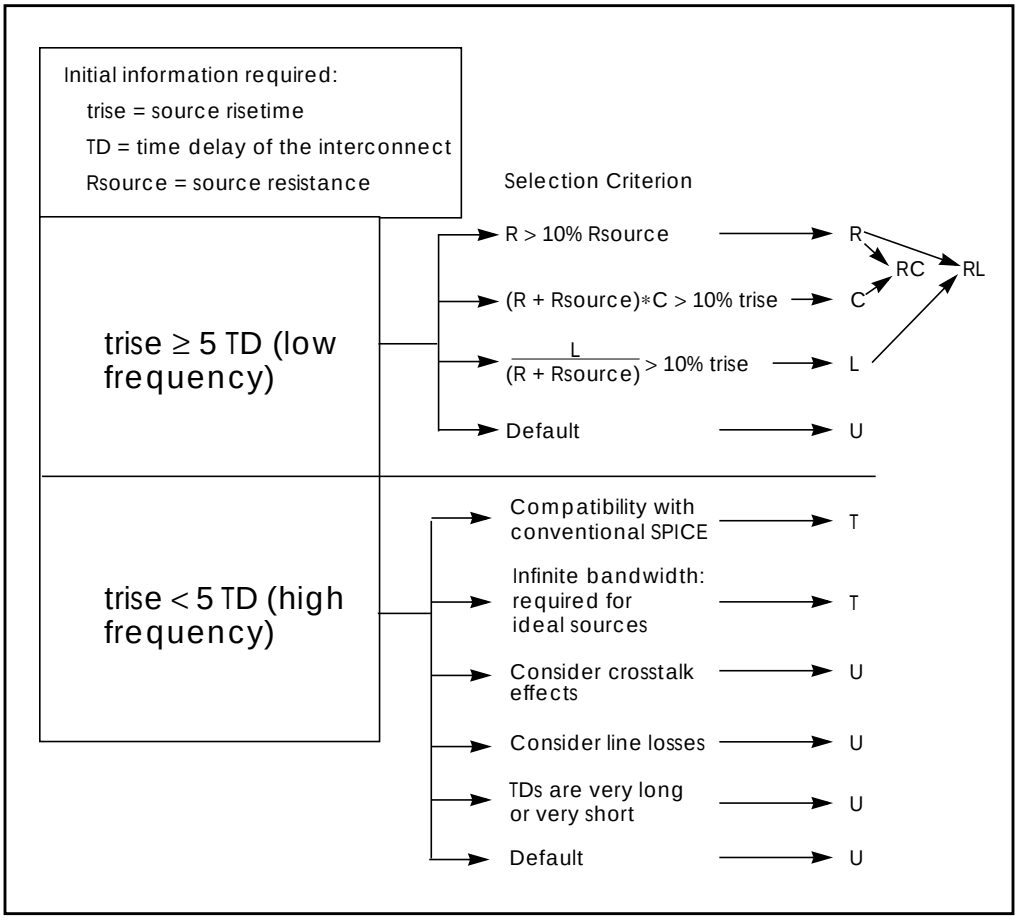
R = equivalent series resistance

C = equivalent shunt capacitor

L = equivalent series inductance

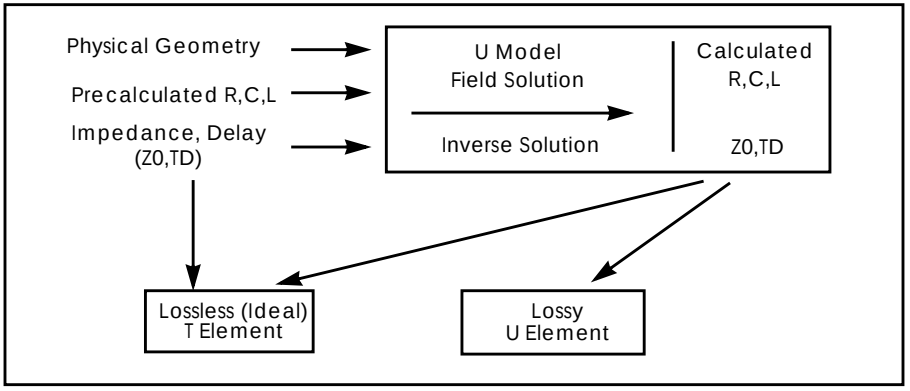
Figure A-1 shows you how to select a model based on source and interconnect properties.

Figure A-1: Wire Model Selection Chart



Use the U model with either the ideal T Element or the lossy U Element. You can also use the T Element alone, without the U model. Avant! offers both, a flexible definition of the conventional SPICE T Element and an accurate U Element lossy simulation.

Figure A-2: U Model, T Element and U Element Relationship



The T and U Elements do not support the <M=val> multiplier function. If a U or T Element is used in a subcircuit and an instance of the subcircuit has a multiplier applied, the results are inaccurate.

A warning message similar to the following is issued in both the status file (*.st0*) and the output file (*.lis*) if the smallest transmission line delay is less than TSTOP/10e6:

```
**warning**: the smallest T-line delay (TD) = 0.245E-14 is
    too small
Please check TD, L and SCALE specification
```

This feature is an aid to finding errors that cause excessively long simulations.

Using Ground and Reference Planes

All transmission lines have a ground reference for the signal conductors. In this manual, the ground reference is called the reference plane so that it is not confused with SPICE ground. The reference plane is the shield or the ground plane of the transmission line element. The reference plane nodes may or may not be connected to SPICE ground.

Selecting Ideal or Lossy Transmission Line Element

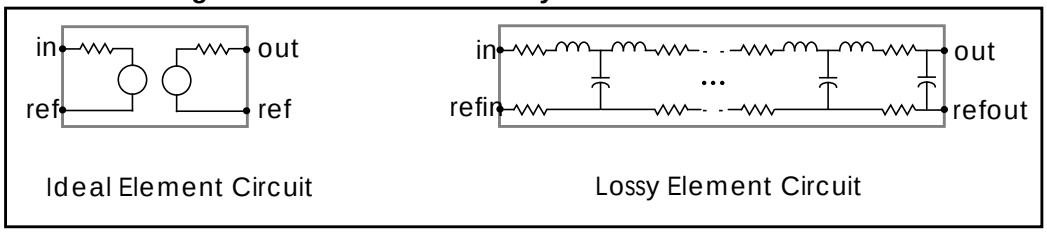
The ideal and lossy transmission line models each have particular advantages, and they may be used in a complementary manner. Both model types are fully functional in AC analysis and transient analysis. Some of the comparative advantages and uses of each type of model are listed in Table A-1.

Table A-1: Ideal versus Lossy Transmission Line

Ideal Transmission Line	Lossy Transmission Line
lossless	includes loss effects
used with voltage sources	used with buffer drivers
no limit on input risetime	prefiltering necessary for fast rise
less CPU time for long delays	less CPU time for short delays
differential mode only	supports common mode simulation
no ground bounce	includes reference plane reactance
single conductor	up to five signal conductors allowed
AC and transient analysis	AC and transient analysis

The ideal line is modeled as a voltage source and a resistor. The lossy line is modeled as a multiple lumped filter section, as shown in Figure A-3.

Figure A-3: Ideal versus Lossy Transmission Line Model



Because the ideal element represents the complex impedance as a resistor, the transmission line impedance is constant, even at DC values. On the other hand, you must prefilter the lossy element if ideal piecewise linear voltage sources are used to drive the line.

Selecting U Models

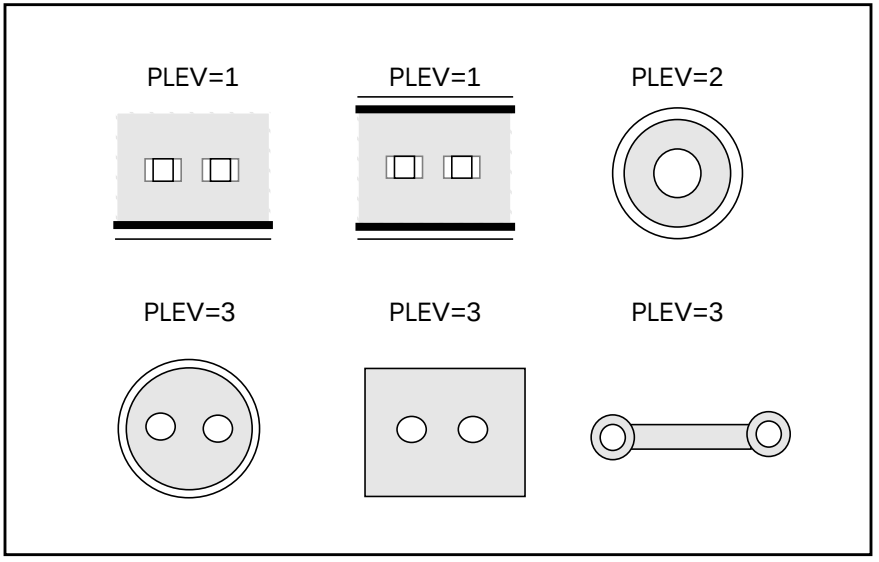
The U model allows three different description formats: geometric/physical, precomputed, and electrical. It provides equally natural description of vendor parts, physically described shapes, and parametric input from field solvers. The description format is specified by the required model parameter ELEV, as follows:

- ELEV=1 – geometric/physical description such as width, height, and resistivity of conductors. It is used by board designers dealing with physical design rules.
- ELEV=2 – precomputed parameters. These are available with some commercial packaging, or as a result of running a field solver on a physical description of commercial packaging.
- ELEV=3 – electrical parameters such as delay and impedance, available with purchased cables. It allows one conductor and ground plane for PLEV = 1.

The U model explicitly supports transmission lines with several types of geometric structures. The geometric structure type is indicated by the PLEV model parameter, as follows:

- PLEV=1 – Selects planar structures, such as microstrip and stripline, (the usual conductor shapes on integrated circuits and printed-circuit boards).
- PLEV=2 – Selects coax, which frequently is used to connect separated instruments.
- PLEV=3 – Selects twinlead, which is used to connect instruments and to suppress common mode noise coupling.

Figure A-4: U Model Geometric Structures



Using Transmission Lines - Example

The following file fragment is an example of how both T Elements and U Elements can be referred to a single U model as indicated in Figure A-2. The file specifies a 200 millimeter printed circuit wire implemented as both a U Element and a T Element. The two implementations share a U model that is a geometric description (ELEV=1) of a planar structure (PLEV=1).

```
T1 in gnd t_out gnd micro1 L=200m
U1 in gnd u_out gnd micro1 L=200m
.model micro1 U LEVEL=3 PLEV=1 ELEV=1 wd=2m ht=2m th=0.25m
   KD=5
```

The next section provides details of element and model syntax.

where:

T1, U1	are element names
micro1	is the model name
in, gnd, t_out, and u_out	are nodes
L	is the length of the signal conductor
wd, ht, th	are dimensions of the signal conductor and dielectric, and
KD	is the relative dielectric constant

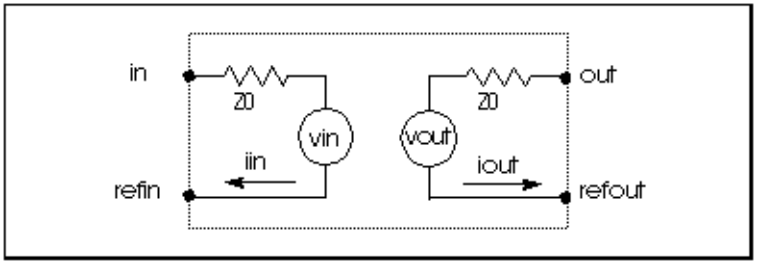
Performing Interconnect Simulation

This section provides details of the requirements for T line or U line simulation.

Using the Ideal Transmission Line

The ideal transmission line element contains the element name, connecting nodes, characteristic impedance (Z_0), and wire delay (TD), unless Z_0 and TD are obtained from a U model. In that case, it contains a reference to the U model.

Figure A-5: Ideal Element Circuit



The input and output of an ideal transmission line have these relationships:

$$\mathrm{Vin}\big|_t = \mathrm{V(out-refout)}\big|_{t-\mathrm{TD}} + (\mathrm{iout} \times Z_0)\big|_{t-\mathrm{TD}}$$

$$\mathrm{Vout}\big|_t = \mathrm{V(in-refin)}\big|_{t-\mathrm{TD}} + (\mathrm{iin} \times Z_0)\big|_{t-\mathrm{TD}}$$

The signal delays for ideal transmission lines are given by:

TDeff=TD·L

If TD is given, or

TDeff=NL/F

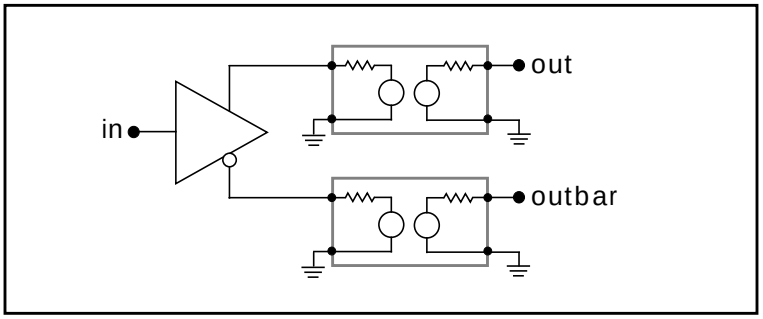
if NL and F are given, or

TDeff=TD

if a U model is used.

The ideal transmission line only delays the difference between the signal and the reference. Some applications, such as a differential output driving twisted pair cable, require both differential and common mode propagation. Use a U Element, if you need the full signal and reference. You can use approximately two T Elements (as shown in Figure A-6). In this figure, the two lines are completely uncoupled, so that only the delay and impedance values are correctly modeled.

Figure A-6: Use of Two T Elements for Full Signal and Reference



You cannot implement coupled lines with the T Element, so use U Elements for applications requiring two or three coupled conductors.

Avant! in-circuit simulation uses a transient timestep that does not exceed half the minimum line delay. Very short transmission lines (relative to the analysis time step) cause long simulation times. You can replace very short lines with a single R, L, or C Element (see Figure A-1 on page A-4).

Lossy U Element Statement

The U Element models single and coupled lossy transmission lines for various planar, coaxial, and twinlead structures. When a U Element is included in your netlist, simulation creates an internal network of R, L, C, and G Elements to represent up to five lines and their coupling capacitances and inductances. For more information, see Chapter 2, “Using Passive Device Models”.

You can specify interconnect properties in three ways:

- Specify the R, L, C, and G (conductance) parameters in a matrix form (ELEV = 2).
- Provide common electrical parameters, such as characteristic impedance and attenuation factors (ELEV = 3).
- Specify the geometry and the material properties of the interconnect (ELEV = 1).

This section initially describes how to use the third method.

The U model is optimized for typical geometries used in ICs, MCMs, and PCBs. The model's closed form expressions are optimized via measurements and comparisons with several different electromagnetic field solvers.

The U Element geometric model handles one to five uniformly spaced transmission lines, all at the same height. Also, the transmission lines can be on top of a dielectric (microstrip), buried in a sea of dielectric (buried), have reference planes above and below them (stripline), or have a single reference plane and dielectric above and below the line (overlay). Thickness, conductor resistivity, and dielectric conductivity allow for calculating loss as well.

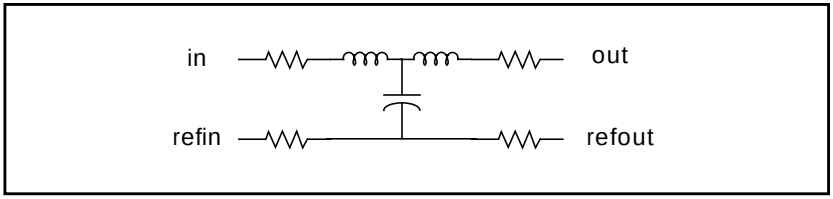
The U Element statement contains the element name, the connecting nodes, the U model reference name, the length of the transmission line, and, optionally, the number of lumps in the element. You can create two kinds of lossy lines: lines with a reference plane inductance (LRR, controlled by the model parameter LLEV) and lines without a reference plane inductance. Wires on integrated circuits and printed circuit boards require reference plane inductance.

The reference ground inductance and the reference plane capacitance to SPICE ground are set by the HGP, CMULT, and optionally, the CEXT parameters.

Lossy U Model Statement

The schematic for a single lump of the U model, with LLEV=0, is shown in Figure A-7. If LLEV is 1, the schematic includes inductance in the reference path as well as capacitance to HSPICE ground. See Reference Planes and HSPICE Ground on page A-19 for more information about LLEV=1 and reference planes.

Figure A-7: Lossy Line with Reference Plane



The following describes the netlist syntax for the U model. Table A-2 and Table A-3 list the model parameters.

U Model Syntax

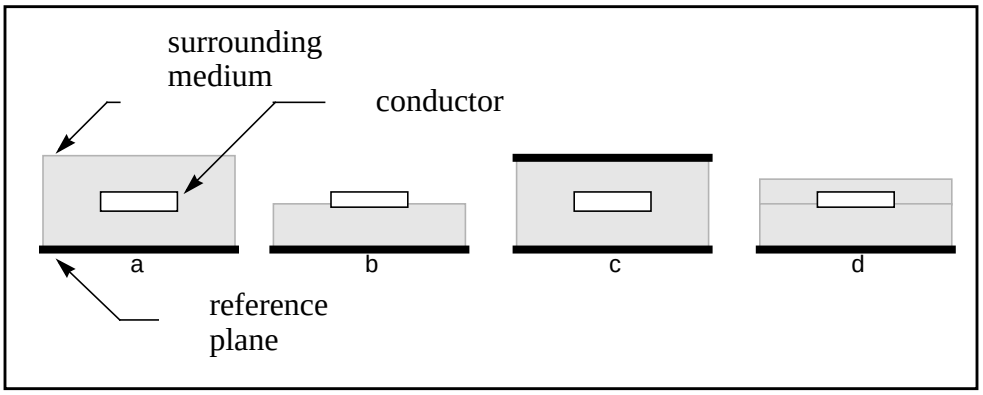
The syntax is:

```
.MODEL mname U LEVEL=3 ELEV=val PLEV=val <DLEV=val>
+ <LLEV=val> + <Pname=val> ...
```

LEVEL=3	Selects the lossy transmission line model
ELEV=val	Selects the electrical specification format including the geometric model val=1
PLEV=val	Selects the transmission line type
DLEV=val	Selects the dielectric and ground reference configuration
LLEV=val	Selects the use of reference plane inductance and capacitance to HSPICE ground.
Pname=val	Specifies a physical parameter, such as NL or WD (see Table A-2) or a loss parameter, such as RHO or NLAY (see Table A-3).

Figure A-8 shows the three dielectric configurations for the geometric U model. You use the DLEV switch to specify one of these configurations. The geometric U model uses ELEV=1.

Figure A-8: Dielectric and Reference Plane Configurations



In Figure A-8 a) sea, DLEV=0, b) microstrip, DLEV=1, c) stripline, DLEV=2 and d) overlay, DLEV=3

Planar Geometric Models Lossy U Model Parameters

Common Planar Model Parameters

The parameters for U models are shown in Table A-2.

Table A-2: U Element Physical Parameters *(Sheet 1 of 3)*

Parameter	Units	Default	Description
LEVEL		required	(=3) required for lossy transmission lines model
ELEV		required	Electrical model (=1 for geometry)
DLEV			Dielectric model (=0 for sea, =1 for microstrip, =2 stripline, =3 overlay; default is 1)

Table A-2: U Element Physical Parameters *(Sheet 2 of 3)*

Parameter	Units	Default	Description
PLEV		required	Transmission line physical model (=1 for planar)
LLEV			Omit or include the reference plane inductance (=0 to omit, =1 to include; default is 0)
NL			Number of conductors (from 1 to 5)
WD	m		Width of each conductor
HT	m		Height of all conductors
TH	m		Thickness of all conductors
THB	m		Reference plane thickness
TS	m		Distance between reference planes for stripline (default for DLEV=2 is 2 HT + TH. TS is not used when DLEV=0 or 1)
SP	m		Spacing between conductors (required if NL > 1)
KD			Dielectric constant
XW	m		Perturbation of conductor width added (default is 0)
CEXT	F/m		External capacitance between reference plane and ground. Only used when LLEV=1, this overrides the computed characteristic.
CMULT		1	Dielectric constant of material between reference plane and ground (default is 1 – only used when LLEV=1)

Table A-2: U Element Physical Parameters *(Sheet 3 of 3)*

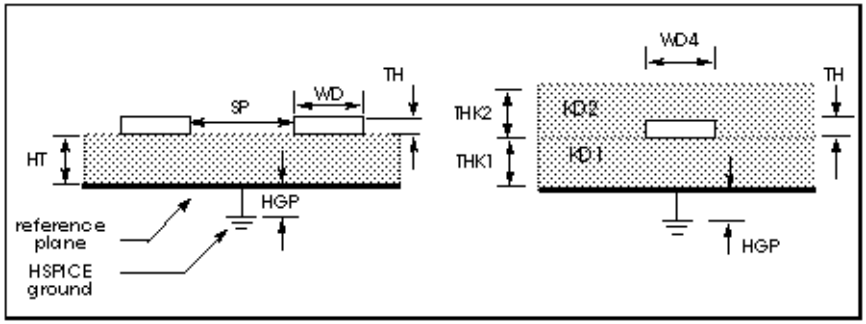
Parameter	Units	Default	Description
HGP	m		Height of the reference plane above HSPICE ground. Used for computing reference plane inductance and capacitance to ground (default is 1.5*HT – HGP is only used when LLEV=1).
CORKD			Perturbation multiplier for dielectric (default is 1)
WLUMP		20	Number of lumps per wavelength for error control
MAXL		20	Maximum number of lumps per element

There are two parametric adjustments in the U model: XW, and CORKD. XW adds to the width of each conductor, but does not change the conductor pitch (spacing plus width). XW is useful for examining the effects of conductor etching. CORKD is a multiplier for the dielectric value. Some board materials vary more than others, and CORKD provides an easy way to test tolerance to dielectric variations.

Physical Parameters

The dimensions for one and two-conductor planar transmission lines are shown in Figure A-9.

Figure A-9: U Element Conductor Dimensions



Loss Parameters

Loss parameters for the U model are shown in Table A-3.

Table A-3: U Element Loss Parameters

Parameter	Units	Description
RHO	ohm·m	Conductor resistivity (default is rho of copper, 17E-9 ohm·m)
RHOB	ohm·m	Reference plane resistivity (default value is for copper)
NLAY		Number of layers for conductor resistance computation (=1 for DC resistance or core resistance, =2 for core and skin resistance at skin effect frequency)
SIG	mho/m	Dielectric conductivity

Losses have a large impact on circuit performance, especially as clock frequencies increase. RHO, RHOB, SIG, and NLAY are parameters associated with losses. Time domain simulators, such as SPICE, cannot directly handle losses that vary with frequency. Both the resistive skin effect loss and the effects of dielectric loss create loss variations with frequency. NLAY is a switch that turns on skin effect calculations in circuit simulation and analysis. The skin effect resistance is proportional to the conductor and backplane resistivities, RHO and RHOB.

The dielectric conductivity is included through SIG. The U model computes the skin effect resistance at a single frequency and uses that resistance as a constant. The dielectric SIG computes a fixed conductance matrix, which is also constant for all frequencies. To closely approximate the losses, compute these resistances and conductances at the frequency of maximum power dissipation. In AC analysis, resistance increases as the square root of frequency above the skin-effect frequency, and resistance is constant below the skin effect frequency.

Geometric Parameter Recommended Ranges

The U Element analytic equations compute quickly, but have a limited range of validity. The U Element equations were optimized for typical IC, MCM, and PCB applications. Table A-4 lists the recommended minimum and maximum values for U Element parameter variables.

Table A-4: Recommended Ranges

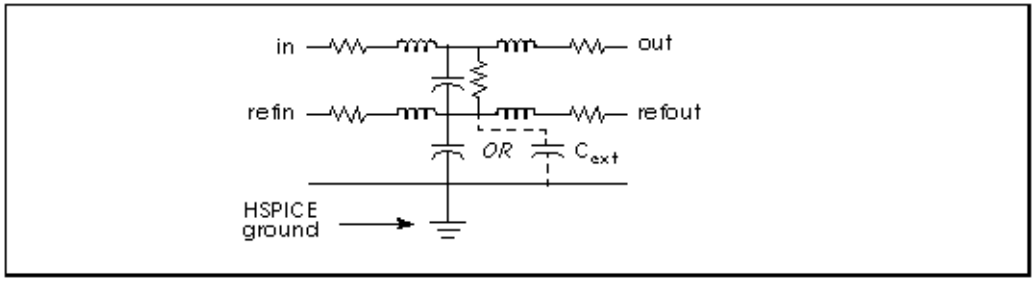
Parameter	Min	Max
NL	1	5
KD	1	24
WD/HT	0.08	5
TH/HT	0	1
TH/WD	0	1
SP/HT	0.15	7.5
SP/WD	1	5

The U Element equations lose their accuracy when you use values outside the recommended ranges. Because the single-line formula is optimized for single lines, you will notice a difference between the parameters of single lines and two coupled lines at a very wide separation. The absolute error for a single line parameter is less than 5% when used within the recommended range. The main line error for coupled lines is less than 15%. Coupling errors can be as high as 30% in cases of very small coupling. Since the largest errors occur at small coupling values, actual waveform errors are kept small.

Reference Planes and HSPICE Ground

Figure A-10 shows a single lump of a U model, for a single line with reference plane inductance. When LLEV=1, the reference plane inductance is computed, and capacitance from the reference plane to HSPICE ground is included in the model. The reference plane is the ground plane of the conductors in the U model.

Figure A-10: Schematic of a U Element Lump when LLEV=1



The model reference plane is not necessarily the same as HSPICE ground. For example, a printed circuit board with transmission lines can have a separate reference plane above a chassis. Simulation with the U model uses either HGP, the distance between the reference plane and HSPICE ground, or C_{ext} to compute the parameters for the ground-to-reference transmission line.

When HGP is used, the capacitance per meter of the ground-to-reference line is computed based on a planar line of width (NL+2)(WD+SP) and the height of HGP above the SPICE ground. CMULT is used as the dielectric constant of the ground-to-reference transmission line. If C_{ext} is given, then C_{ext} is used as the capacitance per meter for the ground-to-reference line. The inductance of the ground-to-reference line is computed from the capacitance per meter and an assumed propagation at the speed of light.

Estimating the Skin Effect Frequency

Most of the power in a transmission line is dissipated at the clock frequency. As a first choice, simulation estimates the maximum dissipation frequency, or skin effect frequency, from the risetime parameter. The risetime parameter is set with the .OPTION statement (for example, .OPTION RISETIME=0.1ns).

Some designers use 0.35/*trise* to estimate the skin effect frequency. This estimate is good for the bandwidth occupied by a transient, but not for the clock frequency, at which most of the energy is transferred. In fact, a frequency of 0.35/*trise* is far too high and results in excessive loss for almost all applications. Simulation computes the skin effect frequency from 1/(15**trise*). If you use precomputed model parameters (ELEV = 2), compute the resistance matrix at the skin effect frequency.

When the risetime parameter is not given, simulation uses other parameters to compute the skin effect frequency. The circuit simulator examines the .TRAN statement for *tstep* and *delmax* and examines the source statement for *trise*. If you set any one of the parameters *tstep*, *delmax*, and *trise*, simulation uses the maximum of these parameters as the effective risetime.

In AC analysis, the skin effect is evaluated at the frequency of each small-signal analysis. Below the computed skin effect frequency (ELEV=1) or FR1(ELEV=3), the AC resistance is constant. Above the skin effect frequency, the resistance increases as the square root of frequency.

Number of Lumped-Parameter Sections

The number of sections (lumps) in a transmission line model also affects the transmission line response. Simulation computes the default number of lumps from the line delay and the signal risetime. There should be enough lumps in the transmission line model to ensure that each lump represents a length of line that is a small fraction of a wavelength at the highest frequency used. It is easy to compute the number of lumps from the line delay and the signal risetime, using an estimate of 0.35/*trise* as the highest frequency.

For the default number of lumps, simulation uses the smaller of 20 or 1+(20*TDeff/*trise*), where TDeff is the line delay. In most transient analysis cases, using more than 20 lumps gives a negligible bandwidth improvement at the cost of increased simulation time. In AC simulations over many decades of frequency with lines over one meter long, more than 20 lumps may be needed for accurate simulation.

Ringing

Sometimes a transmission line simulation shows ringing in the waveforms, as in Figure A-27 on page A-43. If the ringing is not verifiable by measurement, it might be due to an incorrect number of lumps in the transmission line models or due to the simulator integration method. Increasing the number of lumps in the model or changing the integration method to Gear reduces the amount of ringing due to simulation errors. The default integration method is TRAP (trapezoidal), but you can change it to Gear with the statement .OPTION METHOD=GEAR.

See ‘Oscillations Due to Simulation Errors” on page A-60 for more information about the number of lumps and ringing.

The next section covers parameters for geometric lines. Coaxial and twinlead transmission lines are discussed in addition to the previously described planar type.

Geometric Parameters (ELEV=1)

Geometric parameters provide a description of a transmission line in terms of the geometry of its construction and the physical constants of each layer, or other geometric shape involved.

PLEV=1, ELEV=1 Geometric Planar Conductors

Planar conductors are used to model printed circuit boards, packages, and integrated circuits. The geometric planar transmission line is restricted to:

- One conductor height (HT or HT1)
- One conductor width (WD or WD1)
- One conductor thickness (TH or TH1)
- One conductor spacing (SP or SP12)
- One dielectric conductivity (SIG or SIG1)
- One or two relative dielectric constants (KD or KD1, and KD2 only if DLEV=3)

Common planar conductors include:

- DLEV=0 – microstrip sea of dielectric. This planar conductor has a single reference plane and a common dielectric surrounding conductor (Figure A-11 on page A-22).

- DLEV=1 – microstrip dual dielectric. This planar conductor has a single reference plane and two dielectric layers (Figure A-12 on page A-22).
- DLEV=2 – stripline. This planar conductor has an upper and lower reference plane (Figure A-13 on page A-23). Both symmetric and asymmetric spacing are available.
- DLEV=3 – overlay dielectric. This planar conductor has a single reference plane and an overlay of dielectric material covering the conductor (Figure A-14 on page A-23).

Figure A-11: Planar Transmission Line, DLEV=0, Sea of Dielectric

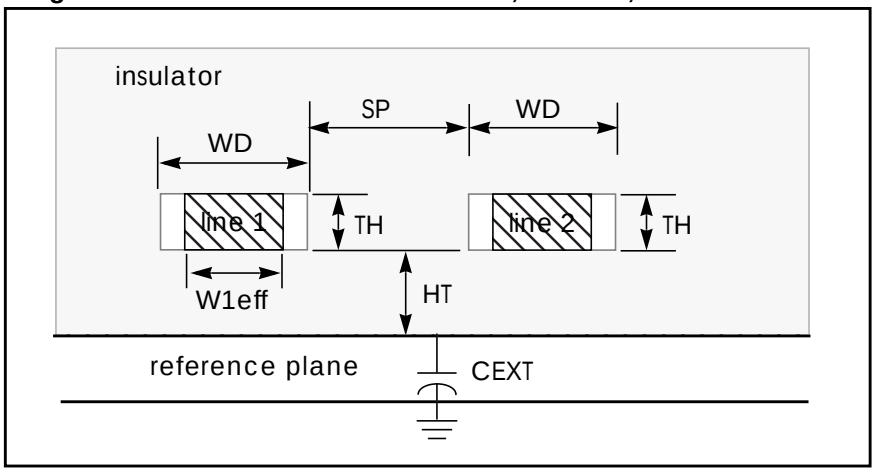


Figure A-12: Planar Transmission Line, DLEV=1, Microstrip

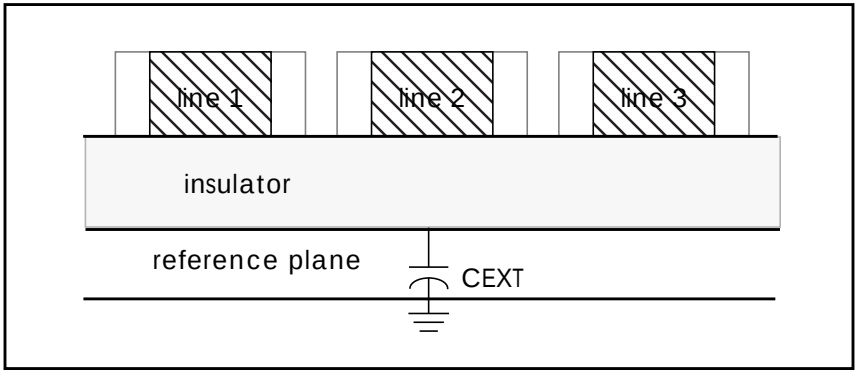


Figure A-13: Planar Transmission Line, DLEV=2, Stripline

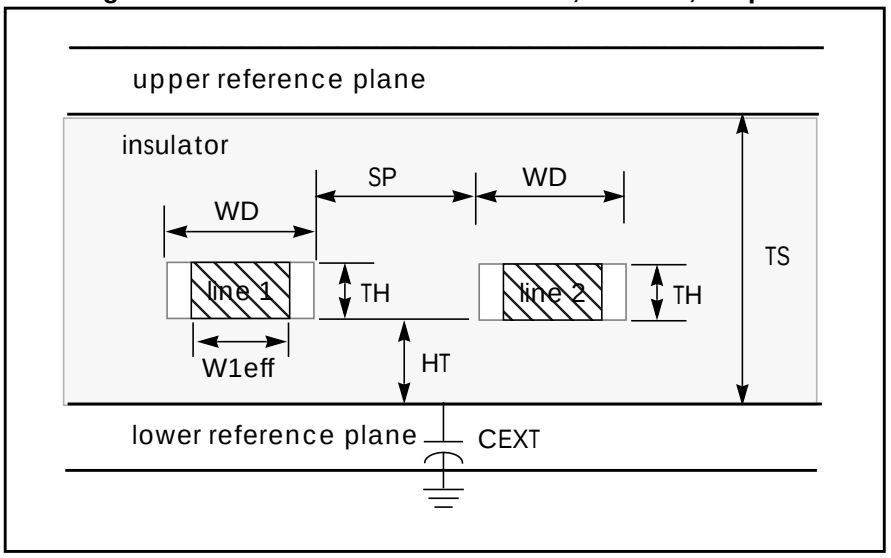
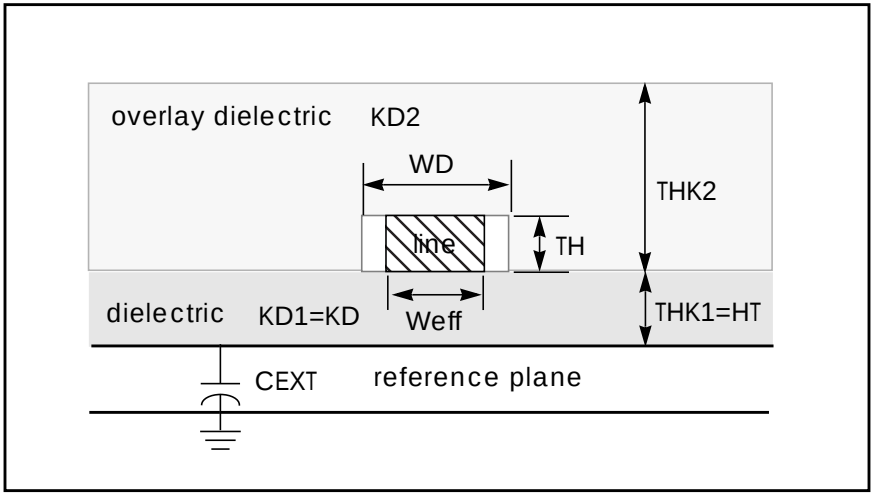


Figure A-14: Planar Transmission Line, DLEV=3, Overlay Dielectric



ELEV=1 Parameters

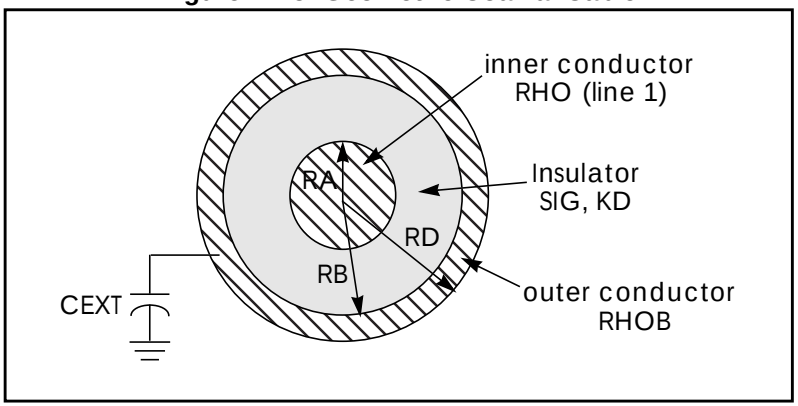
Name (Alias)	Units	Default	Description
DLEV	—	1.0	0: microstrip sea of dielectric 1: microstrip layered dielectric 2: stripline
NL	—	1	Number of conductors
NLAY	—	1.0	Layer algorithm: 1: DC cross section only 2: skindepth cross section on surface plus DC core
HT(HT1)	m	req	Conductor height
WD(WD1)	m	req	Conductor width
TH(TH1)	m	req	Conductor thickness
THK1	m	HT	Dielectric thickness for DLEV=3
THK2	m	0.0	Overlay dielectric thickness for DLEV=3 $0 \le THK2 < 3 \cdot HT$ (see Note)
THB	m	calc	Reference conductor thickness
SP(SP12)	m	req	Spacing: line 1 to line 2 required for nl > 1
XW	m	0.0	Difference between drawn and realized width
TS	m	calc	Height from bottom reference plane to top reference plane $TS=TH+2 \cdot HT$ (DLEV=2, stripline only)
HGP	m	HT	Height of reference plane above SPICE ground – LLEV=1

Name (Alias)	Units	Default	Description
CMULT	—	1.0	Multiplier (used in defining CPR) for dielectric constant of material between shield and SPICE ground when LLEV=1 and CEXT is not present
CEXT	F/m	und	External capacitance from reference plane to *circuit ground point* – used only to override HGP and CMULT computation
RHO	ohm·m	17E-9	Resistivity of conductor material – defaults to value for copper
RHOB	ohm·m	rho	Resistivity of reference plane material
SIG1(SIG)	mho/m	0.0	Conductivity of dielectric
KD1(KD)	—	4.0	Relative dielectric constant of dielectric
KD2		KD	Relative dielectric constant of overlay dielectric for DLEV=3 $1 < KD1 < 4 \cdot KD$
CORKD	—	1.0	Correction multiplier for KD

Note: If THK2 is greater than three times HT, simulation accuracy decreases. A warning message is issued to indicate this. A *reference plan*e is a ground plane, but it is not necessarily at SPICE ground potential.

Lossy U Model Parameters for Geometric Coax (PLEV=2, ELEV=1)

Figure A-15: Geometric Coaxial Cable



Geometric Coax Parameters

Name (Alias)	Units	Default	Description
RA	m	req	Outer radius of inner conductor
RB	m	req	Inner radius of outer conductor (shield)
RD	m	ra+rb	Outer radius of outer conductor (shield)
HGP	m	RD	Distance from shield to SPICE ground
RHO	ohm·m	17E-9	Resistivity of conductor material – defaults to value for copper
RHOB	ohm·m	rho	Resistivity of shield material
SIG	mho/m	0.0	Conductivity of dielectric
KD	—	4.0	Relative dielectric constant of dielectric

Name (Alias)	Units	Default	Description
CMULT	—	1.0	Multiplier (used in defining CPR) for dielectric constant of material between shield and SPICE ground when LLEV=1 and CEXT is not present
CEXT	F/m	und.	External capacitance from shield to SPICE ground – used only to override HGP and CMULT computation
SHTHK	m	2.54E-4	Coaxial shield conductor thickness

Lossy U Model Parameters Geometric Twinlead (PLEV=3, ELEV=1)

Figure A-16: Geometric Embedded Twinlead, DLEV=0, Sea of Dielectric

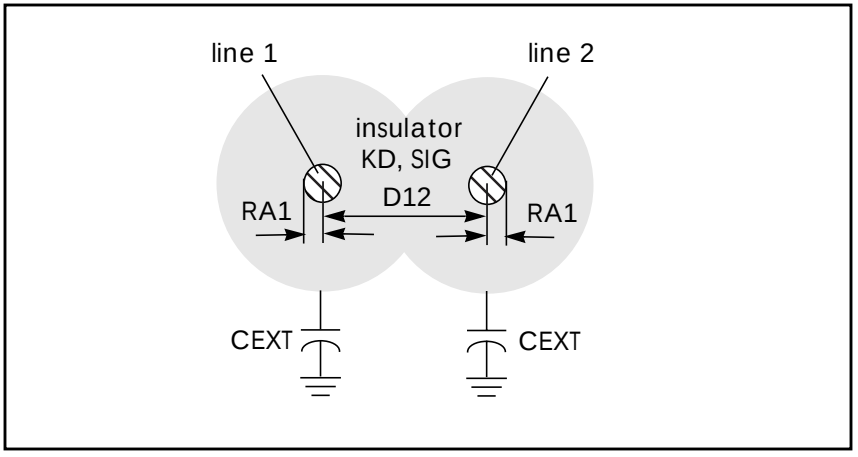


Figure A-17: Geometric Twinlead, DLEV=1, with Insulating Spacer

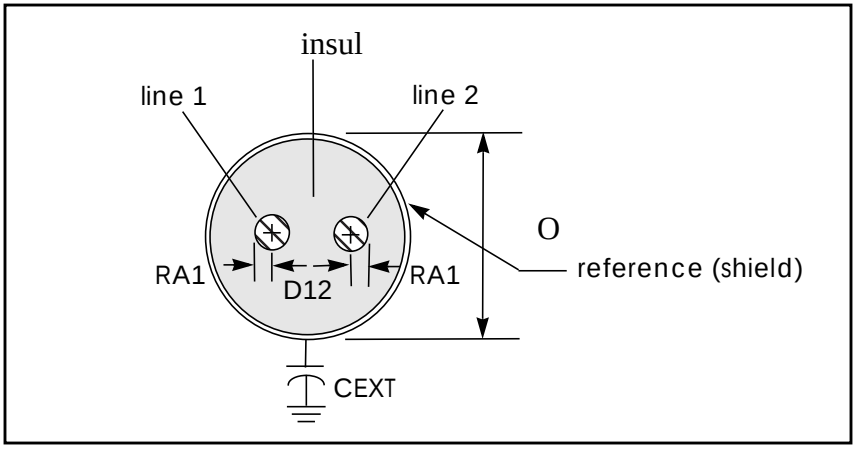
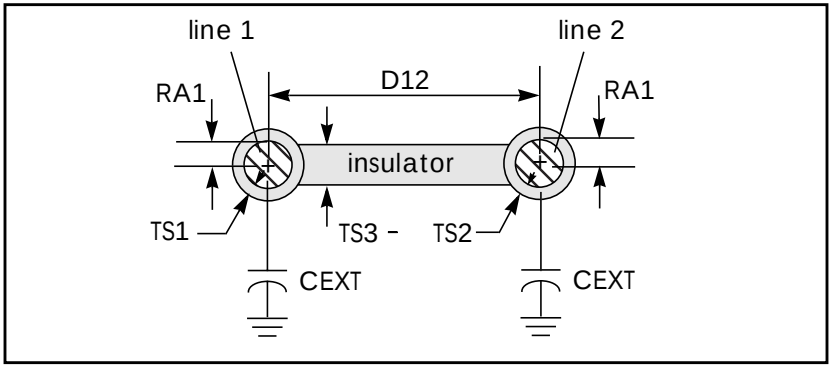


Figure A-18: Geometric Twinlead, DLEV=2, Shielded



Geometric Twinlead Parameters (ELEV=1)

Name (Alias)	Units	Default	Description
DLEV	—	0.0	0: embedded twinlead 1: spacer twinlead 2: shielded twinlead
RA1	m	req.	Outer radius of each conductor
D12	m	req.	Distance between the conductor centers
RHO	ohm·m	17E-9	Resistivity of first conductor material – defaults to value for copper
KD		4.0	Relative dielectric constant of dielectric
SIG	mho/m	0.0	Conductivity of dielectric
HGP	m	d12	Distance to reference plane
CMULT	—	1.0	Multiplier {used in defining CPR} for dielectric constant of material between reference plane and SPICE ground when LLEV=1 and CEXT is not present.
CEXT	F/m	undef.	External capacitance from reference plane to SPICE ground point (overrides LRR when present)
TS1	m	req.	Insulation thickness on first conductor
TS2	m	TS1	Insulation thickness on second conductor
TS3	m	TS1	Insulation thickness of spacer between conductor

Name (Alias)	Units	Default	Description
The following parameters apply to shielded twinlead:			
RHOB	ohm·m	rho	Resistivity of shield material (if present)
OD1	m	req.	Maximum outer dimension of shield
SHTHK	m	2.54E-4	Twinlead shield conductor thickness

Precomputed Model Parameters (ELEV=2)

Precomputed parameters allow the specification of up to five signal conductors and a reference conductor. These parameters may be extracted from a field solver, laboratory experiments, or packaging specifications supplied by vendors. The parameters supplied include:

- Capacitance/length. Each conductor has a capacitance to all other conductors.
- Conductance/length.Each conductor has a conductance to all other conductors due to dielectric leakage.
- Inductance/length. Each conductor has a self inductance and mutual inductances to all other conductors in the transmission line.
- Resistance/length. Each conductor has two resistances, high frequency resistance due to skin effect and bent wires and DC core resistance.

Figure A-19 identifies the precomputed components for a three-conductor line with a reference plane. The names for the resistance, capacitance, and conductance components for up to five lines are shown in Figure A-20.

Figure A-19: Precomputed Components for 3 Conductors and a Reference Plane

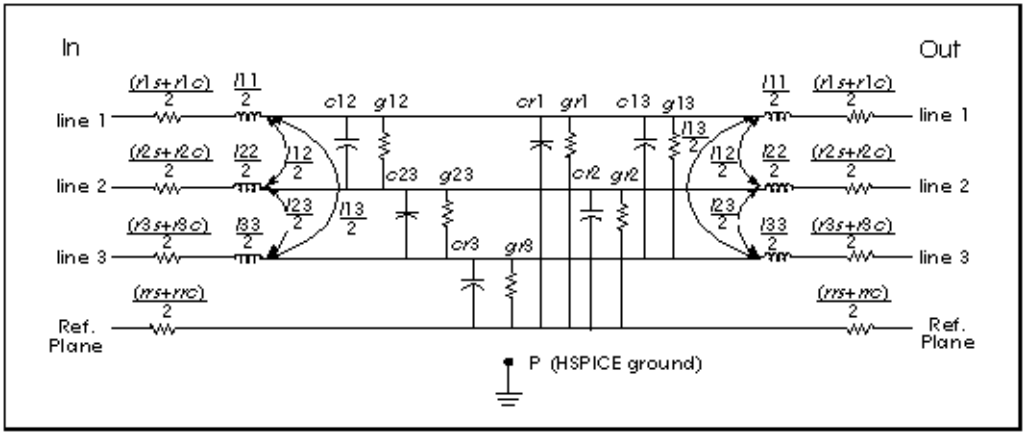


Figure A-20: ELEV=2 Model Keywords for Conductor PLEV=1

	Ref. plane	line 1	line 2	line 3	line 4	line 5
HSPICE ground	CPR GPR	CP1 GP1	CP2 GP2	CP3 GP3	CP4 GP4	CP5 GP5
Ref. plane	RRR LRR	CR1 GR1 LR1	CR2 GR2 LR2	CR3 GR3 LR3	CR4 GR4 LR4	CR5 GR5 LR5
line 1		R11 L11	C12 G12 L12	C13 G13 L13	C14 G14 L14	C15 G15 L15
line 2			R22 L22	C23 G23 L23	C24 G24 L24	C25 G25 L25
line 3				R33 L33	C34 G34 L34	C35 G35 L35
line 4					R44 L44	C45 G45 L45
line 5						R55 L55

LLEV=1 parameter only

All precomputed parameters default to zero except CEXT, which is not used unless it is defined. The units are standard MKS in every case, namely:

capacitance	F/m
inductance	H/m
conductance	mho/m
resistance	ohm/m

Three additional parameters, LLEV (which defaults to 0), CEXT, and GPR are described below.

- LLEV=0. The reference plane conductor is resistive only (the default).
- LLEV=1. Reference plane inductance is included, as well as common mode inductance and capacitance to SPICE ground for all conductors.
- CEXT. External capacitance from the reference plane to SPICE ground. When CEXT is specified, it overrides CPR.
- GPR. Conductance to circuit ground; is zero except for immersion in a conductive medium.

Conductor Width Relative to Reference Plane Width

For the precomputed lossy U model (ELEV=2), the conductor width must be smaller than the reference plane width, which makes the conductor inductance smaller than the reference plane inductance. If the reference plane inductance is greater than the conductor inductance, simulation reports an error.

Alternative Multi-conductor Capacitance/Conductance Definitions

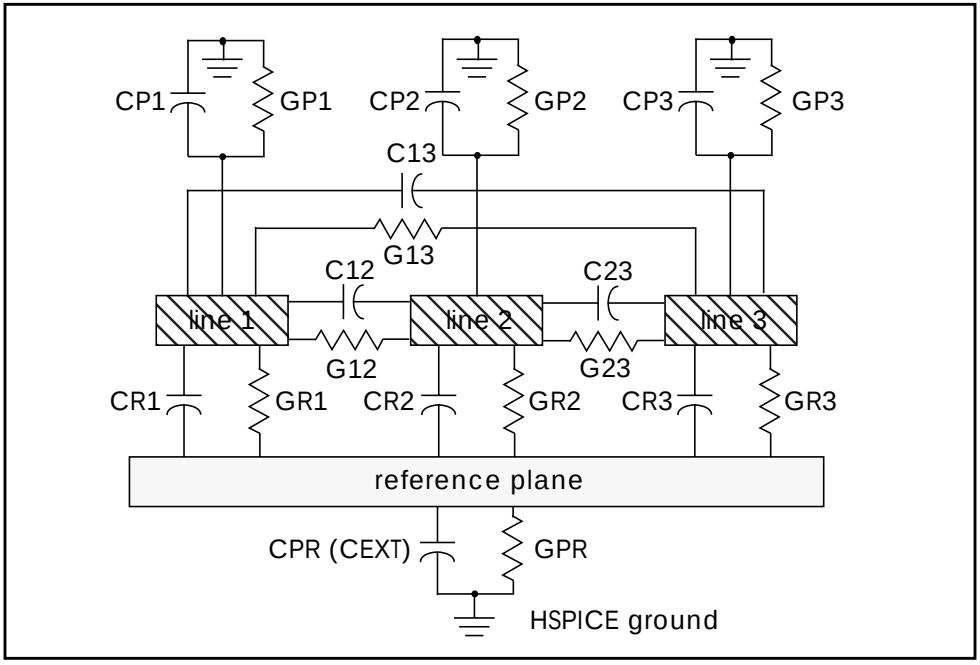
Three different definitions of capacitances and conductances between multiple conductors are currently used. In this manual, relationships are written explicitly only for various capacitance formulations, but they apply equally well to corresponding conductance quantities, which are electrically in parallel with the capacitances. The symbols used in this section, and where one is likely to encounter these usages, are:

- CXY: branch capacitances, input, and circuit models.
- Cjk: Maxwell matrices for capacitance, multiple capacitor stamp for MNA (modified nodal admittance) matrix, which is a SPICE (and Star-Hspice/ Star-Sim) internal. Also the output of some field solvers.

- CX: capacitance with all conductors except X grounded. The output of some test equipment.
- GXY, Gjk, GX: conductances corresponding to above capacitances

The following example uses a multiple conductor capacitance model, a typical U model transmission line. The U Element supports up to five signal conductors plus a reference plane, but the three conductor case, Figure A-21, demonstrates the three definitions of capacitance. The branch capacitances are specified in Hspice notation.

Figure A-21: Single-Lump Circuit Capacitance



The branch and Maxwell matrices are completely derivable from each other. The "O.C.G." ("other conductors grounded") matrix is derivable from either the Maxwell matrix or the branch matrix. Thus:

$$CX = \sum_{X \neq Y} CXY$$

Cjk = CX on diagonal
= –CXY off diagonal

The matrices for the example given above provide the following “O.C.G.” capacitances:

C1 = CR1 + C12 + C13
C2 = CR2 + C12 + C23
C3 = CR3 + C13 + C23
CR = CR1 + CR2 + CR3 + CPR

Also, the Maxwell matrix is given as:

$$Cjk = \begin{bmatrix} CR & -CR1 & -CR2 & -CR3 \\ -CR1 & C1 & -C12 & -C13 \\ -CR2 & -C12 & C2 & -C23 \\ -CR3 & -C13 & -C23 & C3 \end{bmatrix}$$

The branch capacitances also may be obtained from the Maxwell matrices. The off-diagonal terms are the negative of the corresponding Maxwell matrix component. The branch matrix terms for capacitance to circuit ground are the sum of all the terms in the full column of the maxwell matrix, with signs intact:

CPR = sum (Cjk), j=R, k=R:3

CP1 = sum (C1k), j=1, k=R:3

CP2 = sum (C2k), j=2, k=R:3

CP3 = sum (C3k), j=3, k=R:3

CP1, ... CP5 are not computed internally with the geometric (ELEV=1) option, although CPR is. This, and the internally computed inductances, are consistent with an implicit assumption that the signal conductors are completely shielded by the reference plane conductor. This is true, to a high degree of accuracy, for stripline, coaxial cable, and shielded twinlead, and to a fair degree for MICROSTRIP. If accurate values of CP1 and so forth are available from a field solver, they can be used with ELEV=2 type input.

If the currents from each of the other conductors can be measured separately, then all of the terms in the Maxwell matrix may be obtained by laboratory experiment. By setting all voltages except that on the first signal conductor equal to 0, for instance, you can obtain all of the Maxwell matrix terms in column 1.

$$\begin{bmatrix} IR \\ I1 \\ I2 \\ I3 \end{bmatrix} = \begin{bmatrix} CR & -CR1 & -CR2 & -CR3 \\ -CR1 & C1 & -C12 & -C13 \\ -CR2 & -C12 & C2 & -C23 \\ -CR3 & -C13 & -C23 & C3 \end{bmatrix} \cdot jw \cdot \begin{bmatrix} 0.0 \\ 1.0 \\ 0.0 \\ 0.0 \end{bmatrix} = jw \cdot \begin{bmatrix} -CR1 \\ C1 \\ -C12 \\ -C13 \end{bmatrix}$$

The advantage of using branch capacitances for input derives from the fact that only one side of the off-diagonal matrix terms are input. This makes the input less tedious and provides fewer opportunities for error.

Measured Parameters (ELEV=3)

When measured parameters are specified in the input, the program calculates the resistance, capacitance, and inductance parameters using TEM transmission line theory with the LLEV=0 option. If redundant measured parameters are given, the program recognizes the situation, and discards those which are usually presumed to be less accurate. For twinlead models, PLEV=3, the common mode capacitance is one thousandth of that for differential-mode, which allows a reference plane to be used.

The ELEV=3 model is limited to one conductor and reference plane for PLEV=1.

Basic ELEV=3 Parameters

Name (Alias)	Units	Default	Description
PLEV			1: planar 2: coax 3: twinlead
ZK	ohm	calc	Characteristic impedance
VREL	—	calc	Relative velocity of propagation (delen / (delay · clight))
DELAY	sec	calc	Delay for length delen
CAPL		1.0	Linear capacitance in length clen
AT1		1.0	Attenuation factor in length atlen. Use dB scale factor when specifying attenuation in dB.
DELEN	m	1.0	Unit of length for delay (for example, ft.)
CLEN	m	1.0	Unit of length for capacitance
ATLEN	m	1.0	Unit of length for attenuation
FR1	Hz	req.	Frequency at which AT1 is valid. Resistance is constant below FR1, and increases as $\sqrt{}$(frequency) above FR1.

Parameter Combinations

You can use several combinations of measured parameters to compute the L and C values used internally. The full parameter set is redundant. If you input a redundant parameter set, the program discards those that are presumed to be less accurate. Table A-5 on page A-37 shows how each of seven possible parameter combinations are reduced, if need be, to a unique set and then used to compute C and L.

Three different delays are used in discussing transmission lines:

DELAY	U model input parameter that is the delay required to propagate a distance “dlen”
TD	T Element input parameter signifying the delay required to propagate one meter
TD_{eff}	internal variable, which is the delay required to propagate the length of the transmission line T Element or U Element.

Table A-5: Lossless Parameter Combinations

Input Parameters	Basis of Computation
ZK, *DELAY, DELEN*, *CAPL*, *CLEN*	redundant. Discard CAPL and CLEN.
ZK, *VREL*, *CAPL*, *CLEN*	redundant. Discard CAPL and CLEN.
ZK, *DELAY, DELEN*	VREL=DELEN/(DELAY · CLIGHT)
ZK and *VREL*	C=1/(ZK · VREL · CLIGHT) L=ZK/(VREL · CLIGHT)
ZK, *CAPL*, *CLEN*	C=CAPL/CLEN $L=C \cdot ZK^2$
CAPL, *CLEN*, *DELAY, DELEN*	VREL=DELEN/(DELAY · CLIGHT)
CAPL, CLEN, VREL	LC=CAPL/CLEN $LL=1/(C \cdot VREL^2 \cdot CLIGHT^2)$

Loss Factor Input

The attenuation per unit length may be specified either as an attenuation factor or as a decibel attenuation. In order to allow for the fact that the data may be available either as input/output or output/input, decibels greater than 0, or factors greater than 1 are assumed to be input/output. The following example shows the four ways that one may specify that an input of 1.0 is attenuated to an output of 0.758.

Table A-6: Input Attenuation Variations

AT1 Input	Computation of attenuation factor and linear resistance
AT1 = –2.4dB	v(out)/v(in) = 0.758 = $10^{(+AT1/20)}$ (for dB < 0)
AT1 = +2.4dB	v(out)/v(in) = 0.758 = $10^{(-AT1/20)}$ (for dB > 0)
AT1 = 1.318	v(out)/v(in) = 0.758 = 1/AT1 (for ATl < 1)
AT1 = 0.758	v(out)/v(in) = 0.758 = AT1 (for ATl > 1)

The attenuation factor is used to compute the exponential loss parameter and linear resistance.

$$\alpha = \frac{\ln((v(in))/(v(out)))}{ATlin}$$

$$LR = 2 \cdot \alpha \cdot \sqrt{(LL)/(LC)}$$

U Element Examples

The following examples show the results of simulating a stripline geometry using the U model in a PCB scale application and in an IC scale application.

Three Coupled Lines, Stripline Configuration

Figure A-22 shows three coupled lines in a stripline configuration on an FR4 printed circuit board. A simple circuit using three coupled striplines is shown in Figure A-23.

Figure A-22: Three Coupled Striplines (PCB Scale)

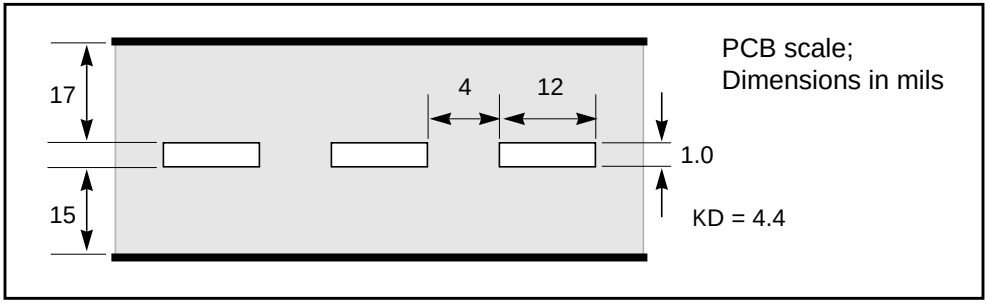
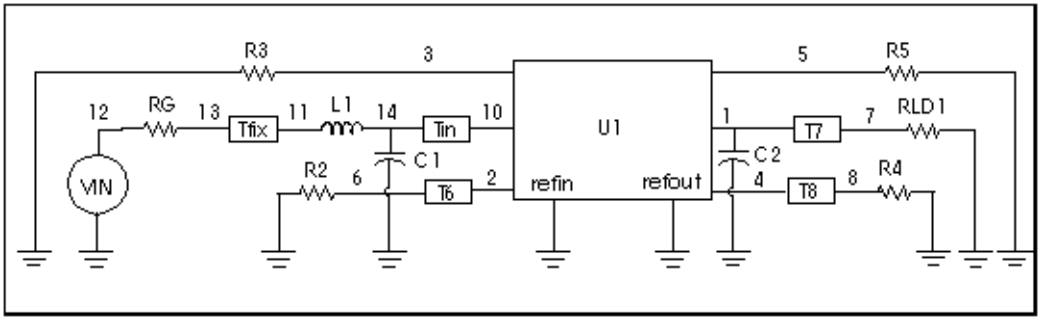


Figure A-23: Schematic Using the Three Coupled Striplines U Model



The input file for the simulation is shown below.

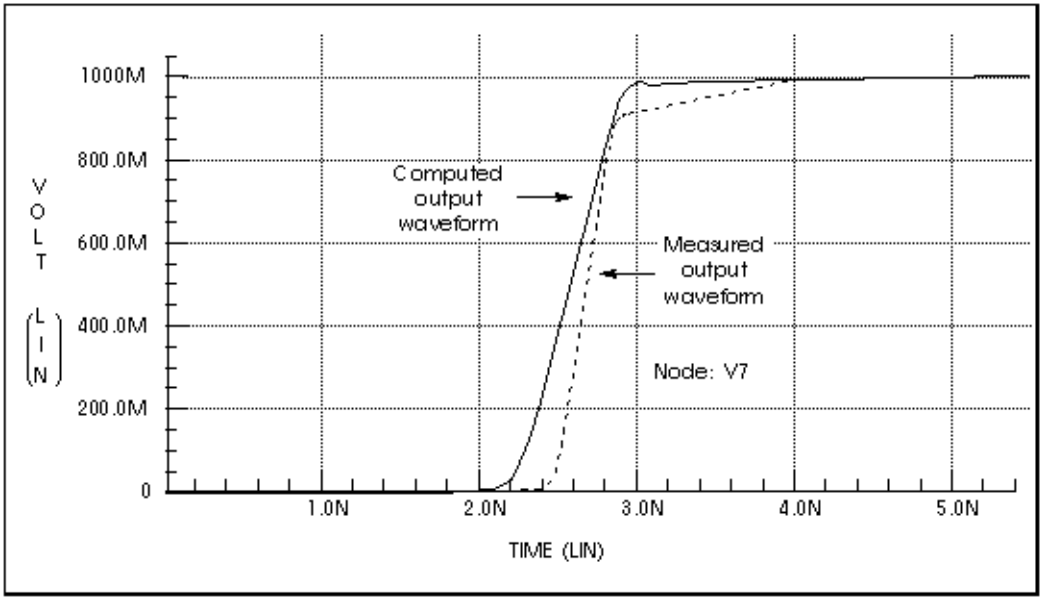
```
* Stripline circuit

.Tran 50ps 7.5ns
.Options Post NoMod Accurate Probe Method=Gear
VIN 12 0 PWL 0 0v 250ps 0v 350ps 2v
L1 14 11 2.5n
C1 14 0 2p
Tin 14 0 10 0 ZO=50 TD=0.17ns
Tfix 13 0 11 0 ZO=45 TD=500ps
RG 12 13 50
RLD1 7 0 50
C2 1 0 2p
U1 3 10 2 0 5 1 4 0 USTRIP L=0.178
T6 2 0 6 0 ZO=50 TD=0.17ns
```

```
T7 1 0 7 0 ZO=50 TD=0.17ns
T8 4 0 8 0 ZO=50 TD=0.17ns
R2 6 0 50
R3 3 0 50
R4 8 0 50
R5 5 0 50
.Model USTRIP U LEVEL=3 PLev=1 Elev=1 Dlev=2 Nl=3 Ht=381u
+ Wd=305u Th=25u Sp=102u Ts=838u Kd=4.7
.Probe v(13) v(7) v(8)
.End
```

Figure A-24, Figure A-25, and Figure A-26 show the main line and crosstalk responses. The rise time and delay of the waveform are sensitive to the skin effect frequency, since losses reduce the slope of the signal rise. The main line response shows some differences between simulation and measurement. The rise time differences are due to layout parasitics and the fixed resistance model of skin effect. The differences between measured and simulated delays are due to errors in the estimation of dielectric constant and the probe position.

Figure A-24: Measured versus Computed Through-Line Response



The gradual rise in response between 3 ns and 4 ns is due to skin effect. During this period, the electric field driving the current penetrates farther into the conductor so that the current flow increases slightly and gradually. This affects the measured response as shown for the period between 3 ns and 4 ns.

Figure A-25 shows the backward crosstalk response. The amplitude and delay of this backward crosstalk are very close to the measured values. The risetime differences are due to approximating the skin effect with a fixed resistor, while the peak level difference is due to errors in the LC matrix solution for the coupled lines.

Figure A-25: Measured Versus Computed Backward Crosstalk Response

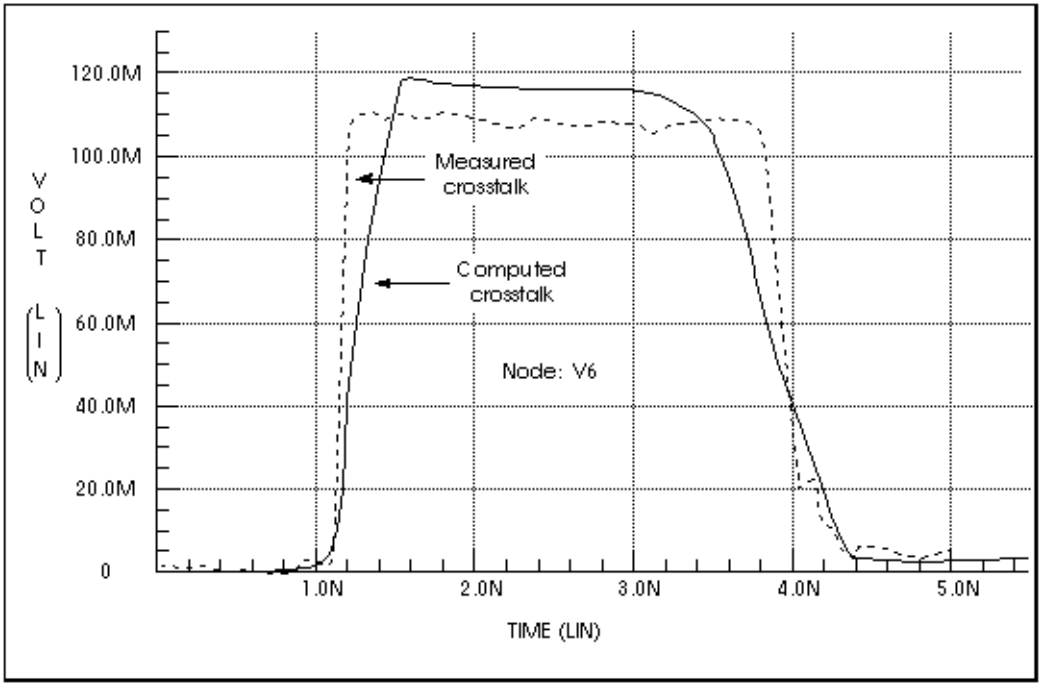


Figure A-26: Measured Versus Computed Forward Crosstalk Response

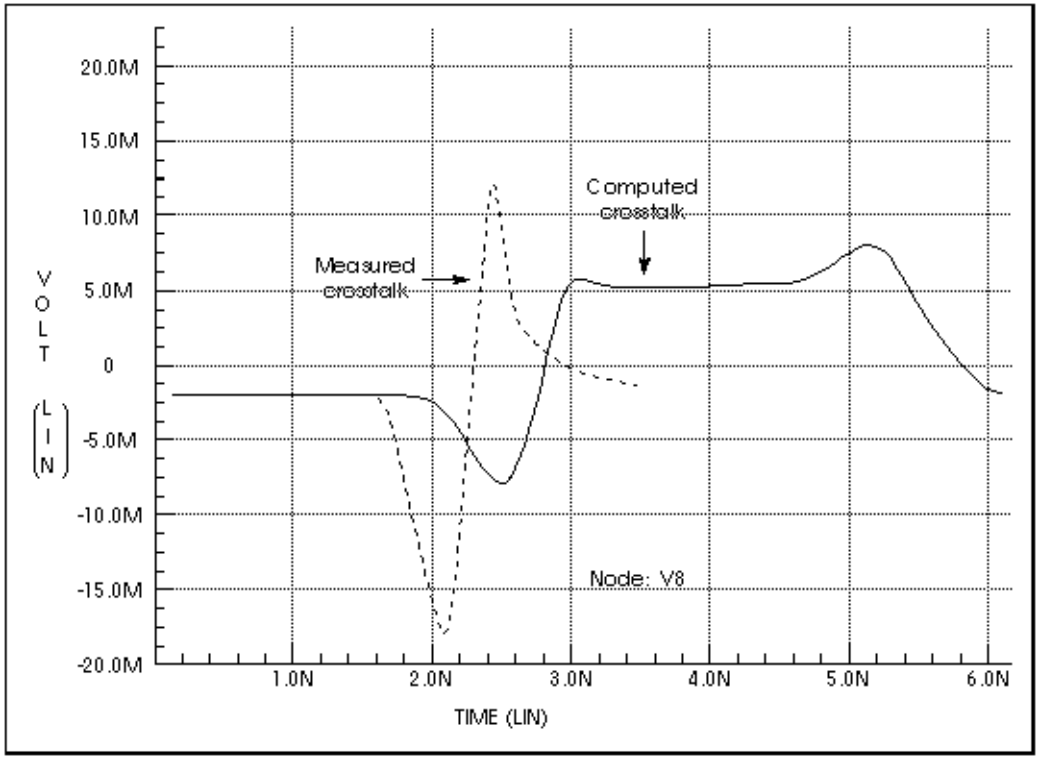
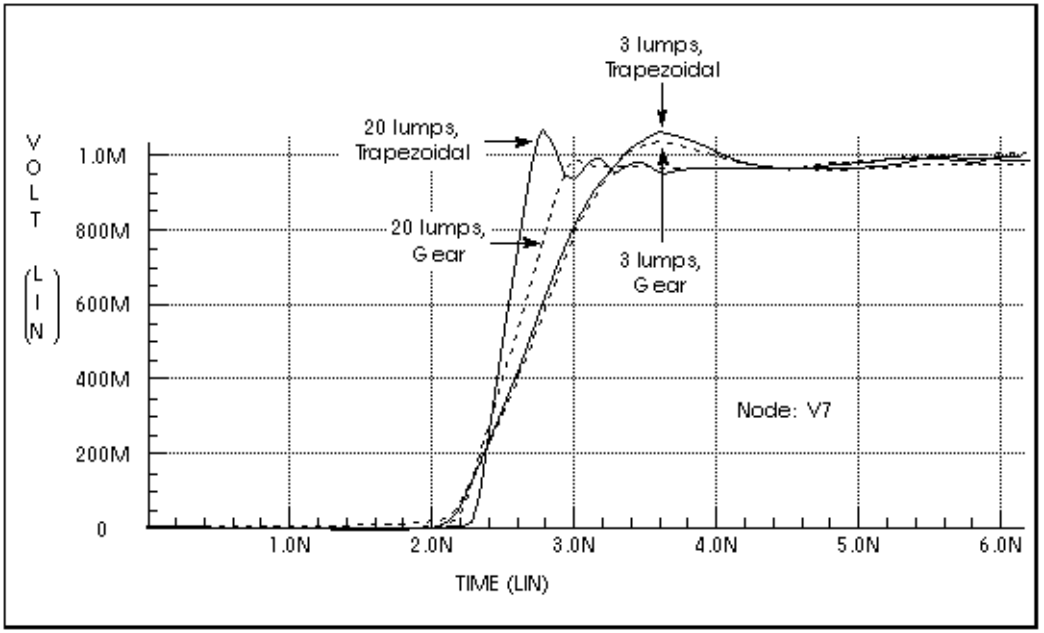


Figure A-26 shows the forward crosstalk response. This forward crosstalk shows almost complete signal cancellation in both measurement and simulation. The forward crosstalk levels are about one tenth the backward crosstalk levels. The onset of ringing of the forward crosstalk has reasonable agreement between simulation and measurement. However, the trailing edge of the measured and simulated responses differ. The measured response trails off to zero after about 3 ns, while the simulated response does not trail down to zero until 6 ns. Errors in simulation at this voltage level can easily be due to board layout parasitics that have not been included in the simulation.

Simulation methods can have a significant effect on the predicted waveforms. Figure A-27 shows the main line response at Node 7 of Figure A-23 as the integration method and the number of lumped elements change. With the recommended number of lumps, 20, the Trapezoidal integration method shows

a fast risetime with ringing, while the Gear integration method shows a fast risetime and a well damped response. When the number of lumped elements is changed to 3, both Trapezoidal and Gear methods show a slow risetime with ringing. In this situation, the Gear method with 20 lumps gives the more accurate simulation.

Figure A-27: Computed Responses for 20 Lumps and 3 Lumps, Gear and Trapezoidal Integration Methods



Three Coupled Lines, Sea of Dielectric Configuration

This example shows the U Element analytic equations for a typical integrated circuit transmission line application. Three 200µm-long aluminum wires in a silicon dioxide dielectric are simulated to examine the through-line and coupled line response.

The U model uses the transmission line geometric parameters to generate a multisection lumped-parameter transmission line model. Use a single U Element statement to create an internal network of three 20-lump circuits.

Figure A-28 shows the IC-scale coupled line geometry.

Figure A-28: Three Coupled Lines with One Reference Plane in a Sea of Dielectric (IC Scale)

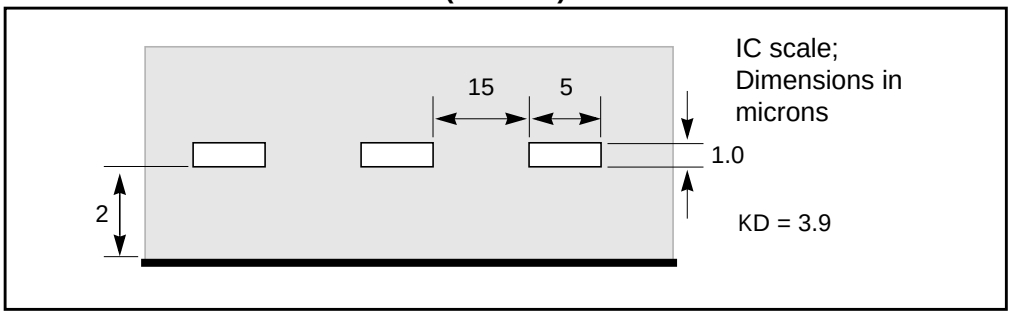


Figure A-29 shows one lump of the lumped-parameter schematic for the three-conductor stripline configuration of Figure A-28. This internal circuitry represents one U Element instantiation. The internal elements are described in ‘Simulation Output” on page A-47.

Figure A-29: Schematic for Three Coupled Lines with One Reference Plane

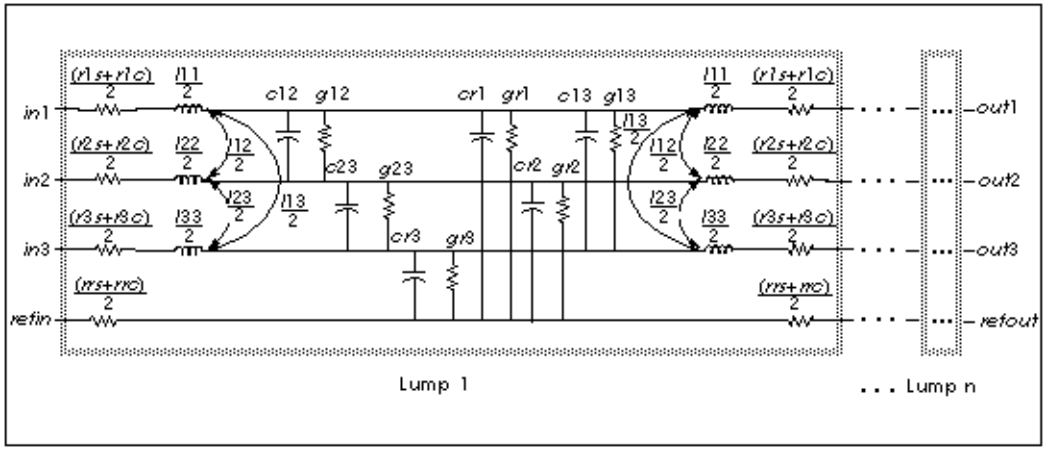
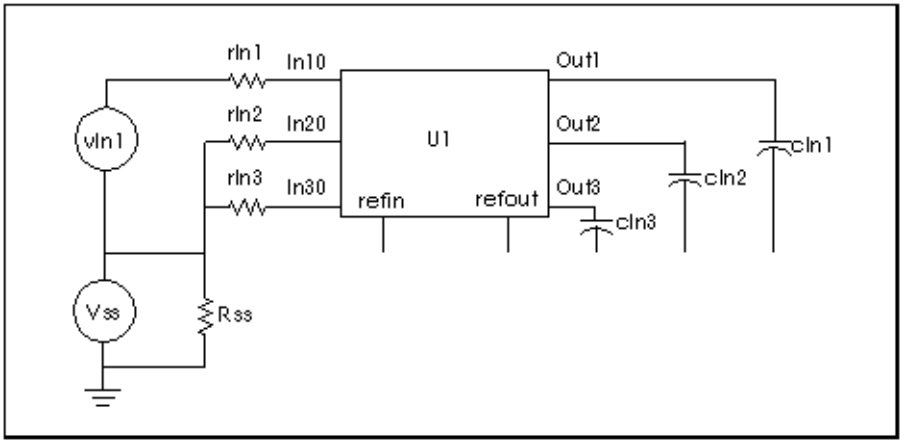


Figure A-30 shows a schematic using the U Element of Figure A-29. In this simple circuit, a pulse drives a three-conductor transmission line source terminated by 50Ω resistors and loaded by 1pF capacitors.

Figure A-30: Schematic Using the Three Coupled Lines U Model



The input file for the U Element solution is shown below.

```
.Tran 0.1ns 20ns
.Options Post Accurate NoMod Brief Probe
Vss Vss 0 0v
Rss Vss 0 1x
vIn1 In1 Vss Pwl 0ns 0v 11ns 0v 12ns 5v 15ns 5v 16ns 0v
rIn1 In1 In10 50
rIn2 Vss In20 50
rIN3 Vss In30 50
u1 In10 In20 In30 Vss Out1 Out2 Out3 Vss IcWire L=200um
cIn1 Out1 Vss 1pF
cIn2 Out2 Vss 1pF
cIn3 Out3 Vss 1pF
.Probe v(Out1) v(Out2) v(Out3)
.Model IcWire U LEVEL=3 Dlev=0 Nl=3 Nlay=2 Plev=1 Elev=1
+ Llev=0 Ht=2u Wd=5u Sp=15u Th=1u Rho=2.8e-8 Kd=3.9
.End
```

The U Element uses the conductor geometry to create length-independent RLC matrices for a set of transmission lines. You can then input any length, and simulation computes the number of circuit lumps that are required.

Figure A-31, Figure A-32, and Figure A-33 show the through and coupled responses, computed using the U Element equations.

Figure A-31: Computed Through-Line Response

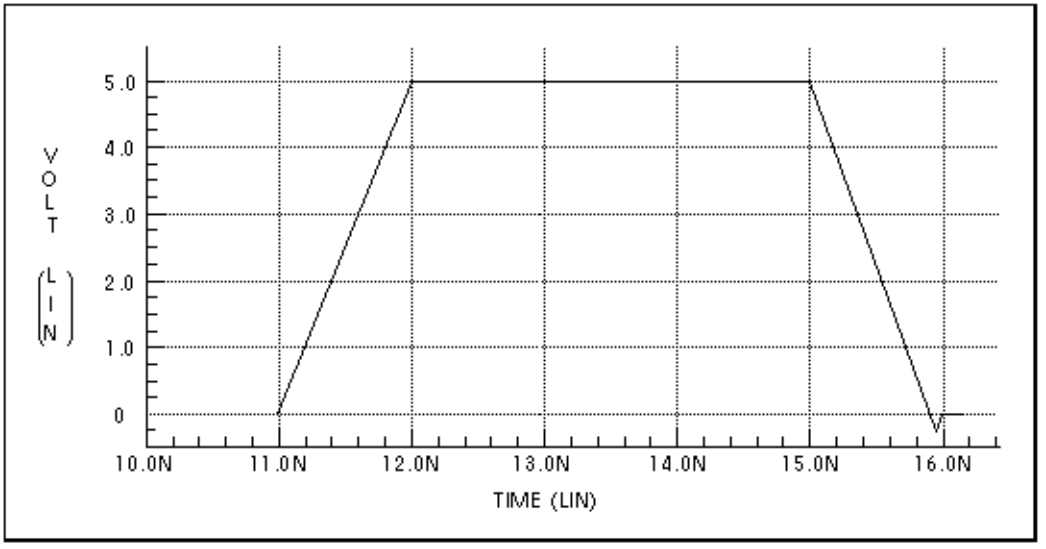


Figure A-32 shows the nearest coupled line response. This response only occurs during signal transitions.

Figure A-32: Computed Nearest Coupled-Line Response

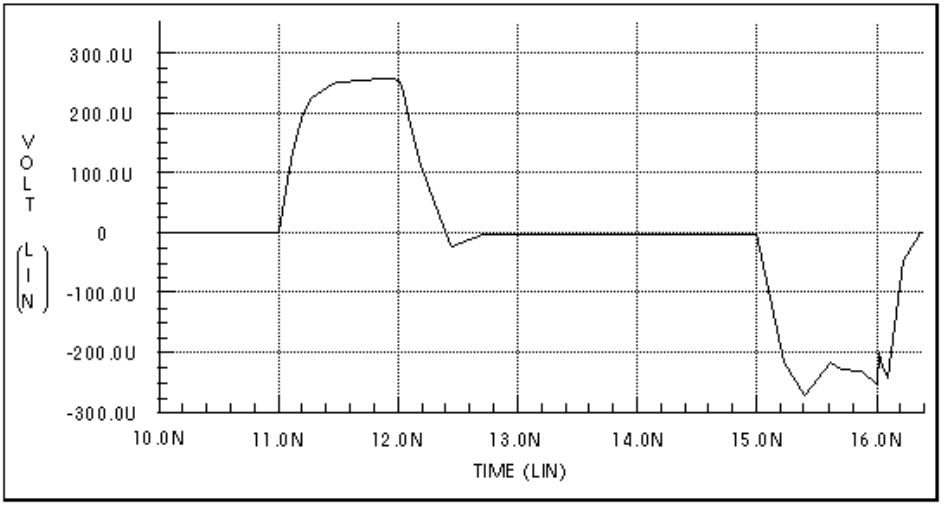
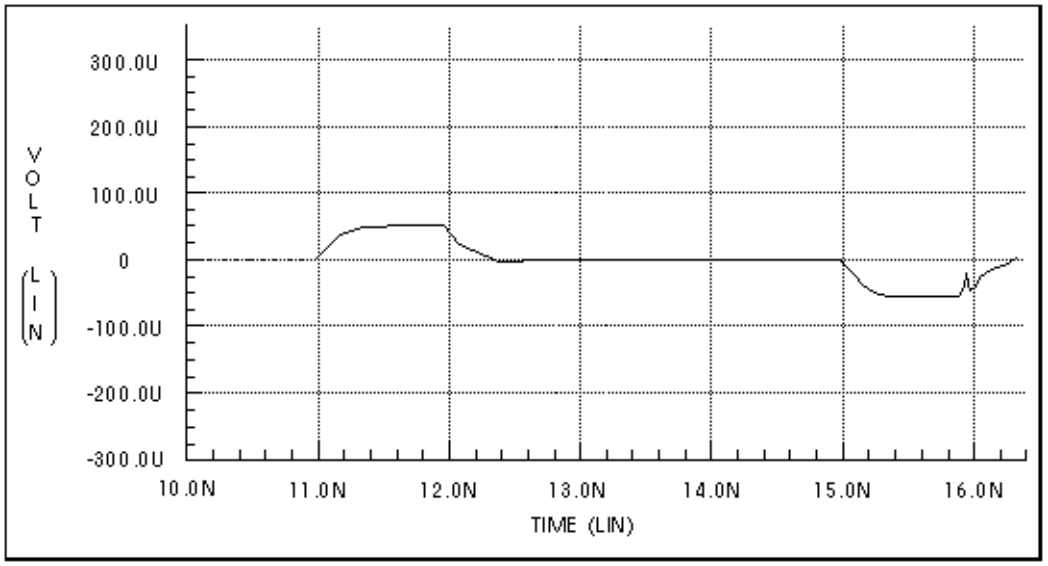


Figure A-33 shows the third coupled line response. The predicted response is about 1/100000 of the main line response.

Figure A-33: Computed Furthest Coupled-Line Response



By default, simulation prints the model values, including the LCRG matrices, for the U Element. All of the printed LCRG parameters are identified in the following section.

Simulation Output

The listing below is part of the output from a simulation using the HSPICE input deck for the *IcWire* U model. Descriptions of the parameters specific to U Elements follows the listing. (Parameters not listed in this section are described in Table A-2 on page A-14 and Table A-3 on page A-17.)

IcWire Output Section

```
*** model name:    0:icwire           ****
names values   units     names values   units    names values units
----- ------   -----     ----- ------   -----    ----- ------ -----
--- u-model control parameters ---
maxl= 20.00    #lumps    wlump= 20.00             elev= 1.00
plev=   1.00               llev= 0.               nlay= 2.00    #layrs
  nl=   3.00    #lines    nb= 1.00    #refpl
--- begin type specific parameters ---
dlev=   0.   #              kd=   3.90            corkd=   1.00
sig=   0.    mho/m        rho= 28.00n ohm*m      rhob= 28.00n ohm*m
th=   1.00u meter        thb=   1.42u meter      skin= 10.31u meter
skinb= 10.31u meter         wd2   5.00u meter        ht2   2.00u meter
th2   1.00u meter         sp1 15.00u meter        wd3   5.00u meter
ht3   2.00u meter         th3   1.00u meter         sp2 15.00u meter
cr1= 170.28p f/m          gr1=   0.    mho/m        l11= 246.48n h/m
cr2= 168.25p f/m          gr2=   0.    mho/m        c12=   5.02p f/m
g12=   0.    mho/m        l12=   6.97n h/m          l22= 243.44n h/m
cr3= 170.28p f/m          gr3=   0.    mho/m        c13= 649.53f f/m
g13=   0.    mho/m        l13=   1.11n h/m          c23=   5.02p f/m
g23=   0.    mho/m        l23=   6.97n h/m          l33= 246.48n h/m
--- two layer (skin and core) parameters ---
rrs=   1.12k ohm/m        rrc=   0.    ohm/m        r1s=   5.60k ohm/m
r1c=   0.    ohm/m        r2s=   5.60k ohm/m        r2c=   0.    ohm/m
r3s=   5.60k ohm/m        r3c=   0.    ohm/m
```

U Element Parameters

c*ij*	coupling capacitance from conductor *i* to conductor *j* (positive)
cr*j*	self capacitance/m of conductor *j* to the reference plane
cpr	capacitance of the reference plane to the HSPICE ground
g*ij*	conductance/m from conductor *i* to conductor *j* (zero if sig=0)
gr*j*	conductance/m from conductor *j* to the reference plane (0 if sig=0)
gpr	conductance from the reference plane to the HSPICE ground, always=0
ht*i*	height of conductor *i* above the reference plane (only ht is input, all heights are the same)
lr*i*	inductance/m from conductor *i* to the reference plane
lrr	inductance/m of the reference plane
l*ij*	inductance/m from conductor *i* to conductor *j*
l*jj*	self inductance/m of conductor *j*
rrc	core resistance/m of the reference plane (if NLAY = 2, zero of skin depth > 90% of thb)
rrr	resistance/m of the reference plane (if NLAY = 1)
rrs	skin resistance/m of the reference plane (if NLAY = 2)
r*i*s	skin resistance/m of conductor *i* (if NLAY = 2)
r*i*c	core resistance/m of conductor *i* (if NLAY = 2, zero if skin depth > 50% of th)
r*jj*	resistance/m of conductor *j* (if NLAY = 1)
skin	skin depth

skinb	skin depth of the reference plane
sp*i*	spacing between conductor *i* and conductor *i*+1 (only sp is input, all spacings are the same)
th*i*	thickness of conductor *i* (only th is input, all thicknesses are the same)
wd*i*	width of conductor *i* (only wd is input – all widths are the same)

The total conductor resistance is indicated by r*jj* when NLAY = 1, or by r*is* + r*ic* when NLAY = 2.

As shown in the next section, *some difference between HSPICE and field solver results is to be expected.* Within the range of validity shown in Table A-4 on page A-18 for the U model, simulation comes very close to field solver accuracy. In fact, discrepancies between results from different field solvers can be as large as their discrepancies with simulation. The next section compares some Avant! physical circuit models to models derived using field solvers.

Capacitance and Inductance Matrices

Simulation places capacitance and inductance values for U Elements in matrix form, for example:

$$\begin{bmatrix} C & .. & C \\ . & & \\ C & & C \end{bmatrix}$$

Figure A-33 on page A-51 shows the capacitance and inductance matrices for the three-line, buried microstrip IC-scale example shown in Figure A-28 on page A-44.

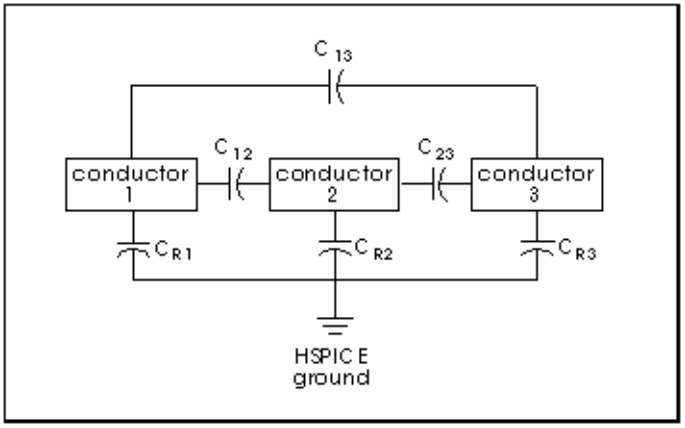
Table A-7: Capacitance and Inductance Matrices for the Three-Line, IC-Scale Interconnect System

Capacitance (pF/m)	176 -5.02 -0.65 -5.02 178 -5.02 -0.65 -5.02 176
Inductance (nH/m)	246 6.97 1.11 6.97 243 6.97 1.11 6.97 246

The capacitance matrices in Table A-7 are based on the admittance matrix of the capacitances between the conductors. The negative values in the capacitance matrix are due to the sign convention for admittance matrices. The inductance matrices are based on the impedance matrices of the self and mutual inductance of the conductors. Each matrix value is per meter of conductor length. The actual lumped values use a conductor length equal to the total line length divided by the number of lumps.

The above capacitance matrix can be related directly to the output of Example 2. Simulation uses the branch capacitance matrix for internal calculations. For the three-conductors in this example, Figure A-34 shows the equivalent capacitances, in terms of simulation device model parameters.

Figure A-34: Conductor Capacitances for Example 2



The capacitances of Figure A-34 are those shown in Figure A-29 on page A-44. The HSPICE nodal capacitance matrix of Table A-7 on page A-51 is shown below, using the capacitance terms that are listed in the HSPICE output.

$$\begin{bmatrix} C_{R1} + C_{12} & -C_{12} & -C_{13} \\ -C_{12} & C_{R2} + C_{12} & -C_{23} \\ -C_{13} & -C_{23} & C_{R3} + C_{13} \end{bmatrix}$$

The off-diagonal terms are the negative of the coupling capacitances (to conform to the sign convention). The diagonal terms require some computation, for example,

$$\begin{aligned} C_{11} &= C_{R1} + C_{12} + C_{13} \\ &= 170.28 + 5.02 + 0.65 \\ &= 175.95, \text{ or } 176 \text{ pF/m} \end{aligned}$$

Note that the matrix values on the diagonal in Table A-7 on page A-51 are large: they indicate self-capacitance and inductance. The diagonal values show close agreement among the various solution methods. As the coupling values become small compared to the diagonal values, the various solution methods give very different results. Third-line coupling capacitances of 0.65 pF/m, 1.2 pF/m, and 0.88 pF/m are shown in Table A-7 on page A-51. Although the differences between these coupling capacitances seem large, they represent a negligible difference in waveforms because they account for only a very small amount of voltage coupling. Table A-7 on page A-51 represents very small coupling because the line spacing is large (about seven substrate heights).

Table A-8 shows the parameters for the stripline shown in Figure A-35.

Figure A-35: Stripline Geometry Used in MCM Technology

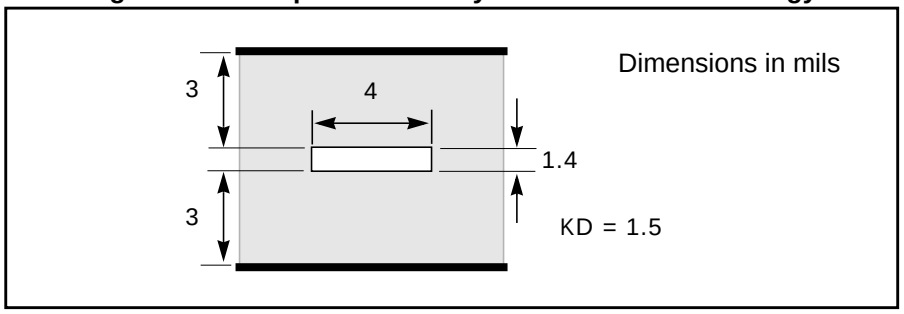


Table A-8: Capacitance and Inductance for the Single Line MCM-Scale Stripline

Capacitance (pF/m)	164.4
Inductance (nH/m)	236.5

Five Coupled Lines, Stripline Configuration

This example shows a five-line interconnect system in a PCB technology. Table A-9 shows the matrix parameters for the line configuration of Figure A-36.

Figure A-36: Five Coupled Lines on a PCB

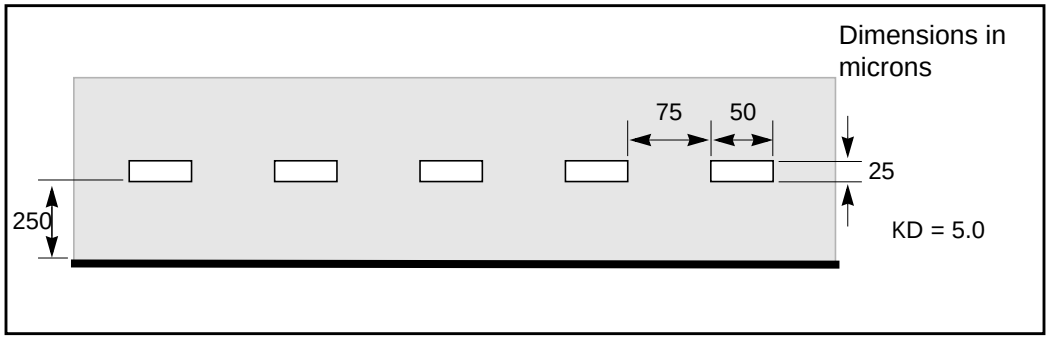


Table A-9: Capacitance and Inductance for the Five-Line PCB-Scale Interconnect System

Capacitance (pF/m)	59 -19 -2.5 -0.8 -0.4 -19 69 -18 -2.2 -0.8 -2.5 -18 69 -18 -2.5 -0.8 -2.2 -18 69 -19 -0.4 -0.8 -2.5 -19 57
Inductance (nH/m)	676 309 179 116 81 309 641 297 174 116 179 297 637 297 179 116 174 297 641 309 81 116 179 309 676

U Model Applications

This section gives examples of use, and then explains some of the aspects of ringing (impulse-initiated oscillation) in real and simulated transmission line circuits.

Data Entry Examples

Coax Geometry Entry (ELEV=1,PLEV=2) with ground reference (LLEV=1) and skin effect (NLAY=2)

```
uc in1 3 out1 4 wire2 l=1
.model wire2 u LEVEL=3 nlay=2 plev=2 elev=1 Llev=1
+ ra=1m rb=7.22m hgp=20m rho=1.7e-8 kd=2.5
```

Matrix Entry (ELEV=2)

```
u1 In1 In2 In3 Vss Out1 Out2 Out3 Vss Wire3 L=0.01
.model Wire3 U LEVEL=3 NL=3 Elev=2 Llev=0
+ rrr=1.12k r11=5.6k r22=5.6k r33=5.6k c13=0.879pF
+ cr1=176.4pF cr2=172.6pF cr3=176.4pF c12=4.7pF c23=4.7pF
+ L11=237nH L22=237nH L33=237nH L12=5.52nH L23=5.52nH
+ L13=1.34nH
```

Coax Measured Data Entry (ELEV=3, PLEV=2)

```
u10 1 0 2 0 rg58 l=12
.model rg58 u LEVEL=3 plev=2 elev=3
+ zk=50 capl=30.8p clen=1ft vrel=0.66
+ fr1=100meg at1=5.3db atlen=100ft
```

Printed Circuit Board Models

Figure A-37 on page A-56 illustrates a small cross section of a six-layer printed circuit board. The top and bottom signal layers require a microstrip U model (DLEV=1), while the middle signal layers use a stripline U model (DLEV=2).

Important aspects of such a circuit board are the following:

- Trace impedance is difficult to control because of etch variation
- 6 mil effective trace widths
- 8 mil drawn widths
- 10 mil insulator thickness
- 1 ounce copper 1.3 mil thick
- Microstrip model TOP used for top and bottom
- Stripline model MID used for middle signal layers

Example

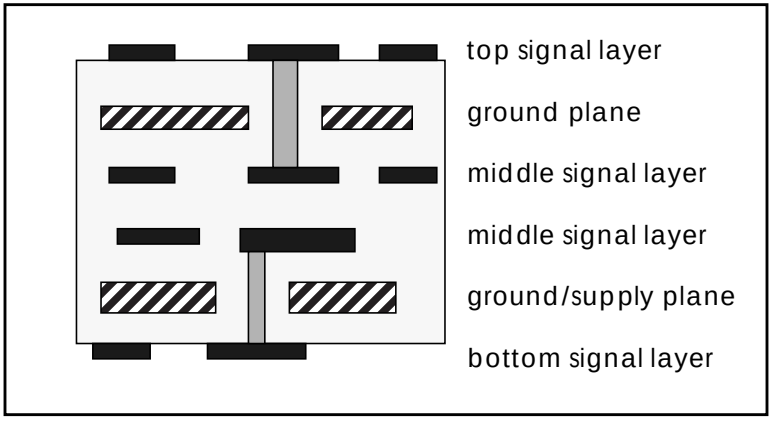
Top and bottom layer model:

```
.MODEL TOP U LEVEL=3 ELEV=1 PLEV=1 TH=1.3mil HT=10mil KD=4.5
   DLEV=1
+ WD=8mil XW=-2mil
```

Middle layer model:

```
.MODEL MID U LEVEL=3 ELEV=1 PLEV=1 TH=1.3mil HT=10mil KD=4.5
   DLEV=2
+ WD=8mil XW=-2mil TS=32mil
```

Figure A-37: Six-Layer Printed Circuit Board



Coax Models

The following examples are for standard coax. These are obtained from commonly available tables[1]. (The parameter fr1 is the frequency at which a specific amount of attenuation, at1, occurs for a specified length of coax, atlen.) Avant! simulators accept dB (decibel) and ft. (foot) units.

Example

```
.model rg9/u    u         LEVEL=3     plev=2       elev=3
+              Zk=51      vrel=.66
+             fr1=100meg at1=2.1db   atlen=100ft
*
.model rg9b/u   u         LEVEL=3     plev=2       elev=3
+              Zk=50      vrel=.66
+             fr1=100meg at1=2.1db   atlen=100ft
*
.model rg11/u   u         LEVEL=3     plev=2       elev=3
+              Zk=75      vrel=.78
+             fr1=100meg at1=1.5db   atlen=100ft
*
.model rg11a/u u         LEVEL=3     plev=2       elev=3
+              Zk=75      vrel=.66
+             fr1=100meg at1=1.9db   atlen=100ft
*
.model rg54a/u u         LEVEL=3     plev=2       elev=3
+              Zk=58      vrel=.66
+             fr1=100meg at1=3.1db   atlen=100ft
*
.model rg15/u   u         LEVEL=3     plev=2       elev=3
+              Zk=53.5    vrel=.66
+             fr1=100meg at1=4.1db   atlen=100ft
*
.model rg53/u   u         LEVEL=3     plev=2       elev=3
+              Zk=53.5    vrel=.66
+             fr1=100meg at1=4.1db   atlen=100ft
*
.model rg58a/u u         LEVEL=3     plev=2       elev=3
+              Zk=50      vrel=.66
+             fr1=100meg at1=5.3db   atlen=100ft
*
.model rg58c/u u         LEVEL=3     plev=2       elev=3
```

```
+              Zk=50      vrel=.66
+             fr1=100meg at1=5.3db   atlen=100ft
*
.model rg59b/u u         LEVEL=3     plev=2       elev=3
+              Zk=75      vrel=.66
+             fr1=100meg at1=3.75db   atlen=100ft
*
.model rg62/u   u         LEVEL=3     plev=2       elev=3
+              Zk=93      vrel=.84
+             fr1=100meg at1=3.1db   atlen=100ft
*
.model rg62b/u u         LEVEL=3     plev=2       elev=3
```

Twinlead Models

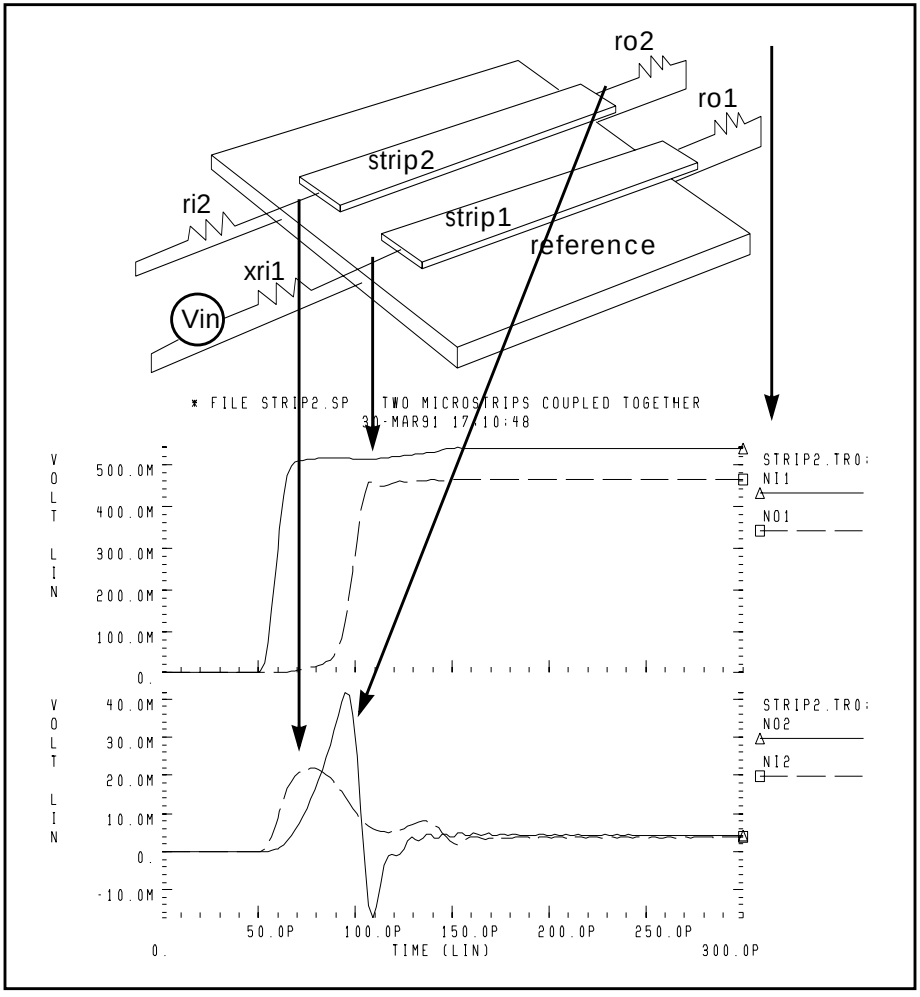
Example

```
.model tw/sh    u         LEVEL=3     plev=3       elev=3
*              Shielded TV type twinlead
+              Zk=300     vrel=.698
+             fr1=57meg   at1=1.7db   atlen=100ft
*
.model tw/un    u         LEVEL=3     plev=3       elev=3
*              Unshielded TV type twinlead
+              Zk=300     vrel=.733
+             fr1=100meg at1=1.4db   atlen=100ft
```

Two Coupled Microstrips

Figure A-38 shows two metal lines formed of the first aluminum layer of a modern CMOS process. The microstrip model assumes that the metal strips sit on top of a dielectric layer that covers the reference plane.

Figure A-38: Two Coupled Microstrips Geometrically Defined as LSI Metallization



Example of Two Microstrips Coupled Together

```
* file strip2.sp Two microstrips coupled together
*.... The tests following use geometric/physical model
.option acct post list
.print tran V(no1) V(no2) V(noref)
```

Signal Source

```
.tran 1ps 300ps
.PARAM Rx=54
* excitation voltage + prefilter
V1 np1 0 PWL 0.0s 0v 50ps 0v 60ps 1v
xrI1 NP1 NI1 rcfilt rflt=rx tdflt=1ps
```

Circuit Definition

```
Ue1 NI1 NI2 0 NO1 NO2 NORef u1 L=5.0m
RI2 NI2 0 Rx
RO1 NO1 NORef Rx
RO2 NO2 NORef Rx
rref noref 0 1
* ...MODEL DEFINITION -- metal layer1 (sea of dielectric)
.MODEL u1 U LEVEL=3 plev=1 elev=1 nl=2
+ KD=3.5 xw=0.1u rho=17e-9 rhob=20e-9
+ wd=1.5u ht=1.0u th=0.6u sp=1.5u
+ llev=1 dlev=0 maxl=50
*
.END
```

Solving Ringing Problems with U Elements

Ringing oscillations at sharp signal edges may be produced by:

- Oscillations due to the simulator
- Oscillations due to lossy approximation of a transmission line (U Element)
- Signal reflections due to impedance mismatch

The primary reason for using a circuit simulator to measure high speed transmission line effects is to calculate how much transient noise the system contains and to determine how to reduce it to acceptable values.

Oscillations Due to Simulation Errors

The system noise results from the signal reflections in the circuit. It may be masked by noises from the simulator. Simulator noise must be eliminated in order to obtain reliable system noise estimates. The following sections describes ways to solve problems with simulator noise.

Timestep Control Error

The default method of integrating inductors and capacitors is trapezoidal integration. While this method gives excellent results for most simulations, it can lead to what is called trapezoidal ringing. This is numerical oscillations that look like circuit oscillations, but are actually timestep control failures. In particular, trapezoidal ringing can be caused by any discontinuous derivatives in the nonlinear capacitance models, or from the exponential charge expressions for diodes, BJTs, and JFETs.

Set the .OPTION METHOD=GEAR to change the integration method from trapezoidal to Gear. The gear method does not ring and, although it typically gives a slightly less accurate result, is still acceptable for transient noise analysis.

Incorrect Number of Element Lumps

It is important to use the right number of lumps in a lossy transmission line element. Too few lumps results in false ringing or inaccurate signal transmission, while too many lumps leads to an inordinately long simulation run. Sometimes, as in verification tests, it is necessary to be able to specify the number of lumps in a transmission line element directly. The number of lumps in a lossy transmission line element may be directly specified, defaulted to an accuracy and limit based computation, or computed with altered accuracy and limit and risetime parameters.

Default Computation

In the default computation, LUMPS=1 until a threshold of total delay versus risetime is reached:

TDeff = RISETIME/20

where: TDeff = total end-to-end delay in the transmission line element

RISETIME = the duration of the shortest signal ramp, as given in the statement

.OPTION RISETIME = value

At the threshold, two lumps are used. Above the threshold, the number of lumps is determined by:

number of lumps = minimum of 20 or [1+(TDeff/RISETIME)*20]

The upper limit of 20 is applied to enhance simulation speed.

If the standard accuracy-based computation does not provide enough lumps, or if it computes too many lumps for simulation efficiency, you can use one of several methods to change the number of lumps on one or more elements:

1. Specify LUMPS=value in the element statement.
2. Specify MAXL=value and WLUMP=value in the .MODEL statement.
3. Specify a different RISETIME=value in the .OPTION statement.

Specify LUMPS=value (direct specification)

Direct specification overrides the model and limit based computation, applying only to the element specified in the element statement, as in the example below:

U35 n1 gnd n2 oref model lumps=31 L=5m

where 31 lumps are specified for an element of length 5 mm.

Specify MAXL and WLUMP (altered accuracy and limit parameters)

You can alter the default computation for all the elements that refer to a particular model by specifying the model parameters “MAXL” and “WLUMP” (which would otherwise default to 20). In the nondefault case the number of lumps, the threshold, and the upper limit all would be changed:

```
lumps = min{MAXL, [1+(TDeff/RISETIME)*WLUMP]}
Threshold: TDeff = RISETIME/WLUMP
Upper lim: MAXL
```

Specify a different “RISETIME” parameter in the .OPTION statement

You can change the threshold and number of lumps computed for all elements of all models, reduce or increase the analysis parameter “RISETIME”. Note that care is required if RISETIME is decreased, because the number of lumps may be limited by MAXL in some cases where it was not previously limited.

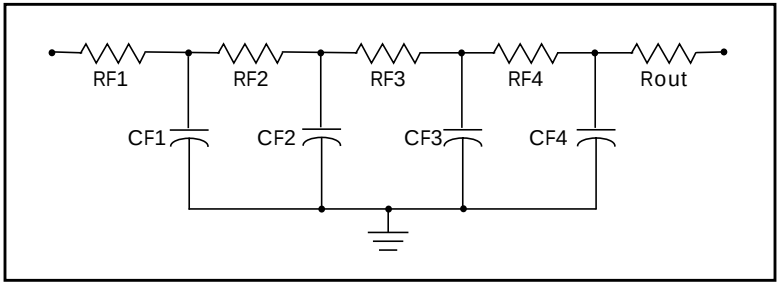
Using a Multistage RC Filter to Prevent Ringing

Artificial sources such as pulse and piecewise linear sources often are used to simulate the action of real output buffer drivers. Since real buffers have a finite cutoff frequency, a multistage filter can be used to give the ideal voltage source reasonable impedance and bandwidth.

You can place a multistage RC filter, shown below, between the artificial source and any U Element to reduce the unrealistic source bandwidth and, consequently, the unrealistic ringing. In order to provide as much realism as possible, the interposed RC filter and the PWL (piecewise linear) source must be designed together to meet the following criteria:

- Reduce the ringing to acceptable levels
- Preserve the realistic bandwidth of the source signal
- Provide a driver with any chosen impedance
- Provide accurately timed transient signals

Figure A-39: Circuit Diagram of an RC Filter



Example

```
.MACRO RCFNEW in out gnd_ref RFLT=50 TDFLT=100n
*
.PROT
*  Begin RCFILT.inc (RC filter) to smooth and match pulse
*  sources to transmission lines. User specifies impedance
*  (RFLT) and smoothing interval (TDFLT). TDFLT is usually
*  specified at about .1*risetime of pulse source.
*
*  cutoff freq, total time delay; and frequency dependent
*  impedance and signal voltage at “out” node:
*
```

```
* smoothing period = TDFLT.....(equivalent boxcar filter)
* delay= TDFLT
* fc=2/(pi*TDFLT).............(cuttoff frequency)
* Zo~ RFLT*(.9 + .1/sqrt( 1 + (f/fc)^2 )
*  V(out)/V(in)= [1 / sqrt( 1 + (f/fc)^2 )]^4
*
.PARAM TD1S='TDFLT/4.0'
RF1 in n1 '.00009*RFLT'
RF2 n1 n2 '.0009*RFLT'
RF3 n2 n3 '.009*RFLT'
RF4 n3 n4 '.09*RFLT'
Rout n4 out '.90*RFLT'
*
.PARAM CTD='TD1S/(.9*RFLT)'
CF1 n1 0 '10000*CTD'
CF2 n2 0 '1000*CTD'
CF3 n3 0 '100*CTD'
CF4 n4 0 '10*CTD'
*
.UNPROT
.EOM
```

From the comments embedded in the macro, the output impedance varies from RFLT in the DC limit to 3% less at FC and 10% less in the high frequency limit.

$$RFLT|_{DC} = 0.99999 \cdot RFLT$$

$$RFLT|_{FC} = 0.97 \cdot RFLT$$

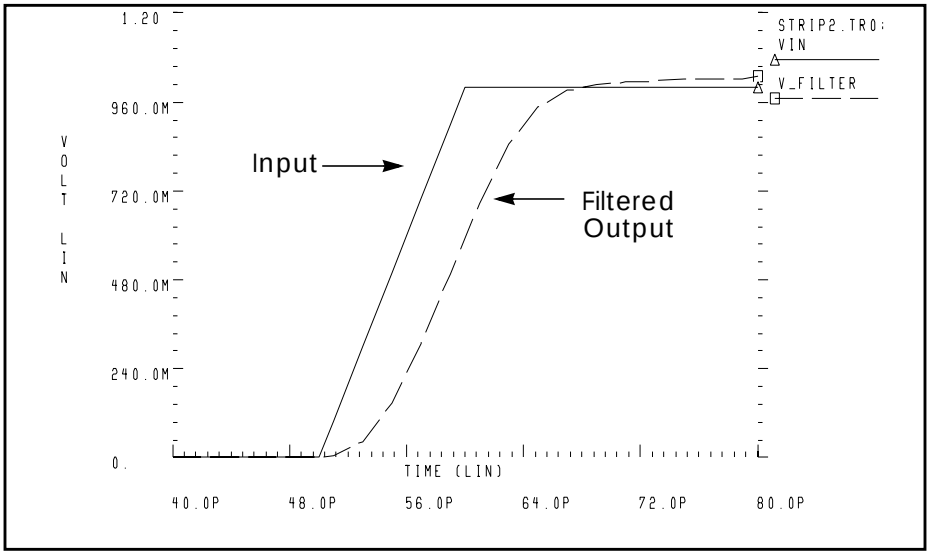
Therefore, setting RFLT to the desired driver impedance gives a reasonably good model for the corrected driver impedance. TDFLT is generally set to 40% of the voltage source risetime.

```
* excitation voltage + prefilter
V1 np1 0 PWL 0.0s 0v 50ps 0v 60ps 1v
xrI1 NP1 NI1 RCFNEW rflt=rx tdflt=4ps
```

Note: RCFNEW is an automatic include file named *$installdir/parts/behave/rcfilt.inc*, where *$installdir* is the installation directory.

Figure A-40 shows the input and output voltages for the filter.

Figure A-40: Multistage RC Filter Input and Output



Signal Reflections Due to Impedance Mismatch

The effect of impedance mismatch is demonstrated in the following example. This circuit has a 75 ohm driver, driving 3 inches of 8 mil wide PCB (middle layer), then driving 3 inches of 16 mil wide PCB.

The operational characteristics of such a circuit are shown in Figure A-41, Figure A-42, and Figure A-43. The first steady value of impedance is 75 ohms, which is the impedance of the first transmission line section. The input impedance falls to 56 ohms after about 2.5ns, when the negative reflection from the nx1 node reaches nil. This TDR displays one idiosyncrasy of the U Element. The high initial value of Zin (TDR) is due to the fact that the input element of the U Element is inductive. The initial TDR spike can be reduced in amplitude and duration by simply using a U Element with a larger number of lumped elements.

Figure A-41: Mathematical Transmission Line Structure

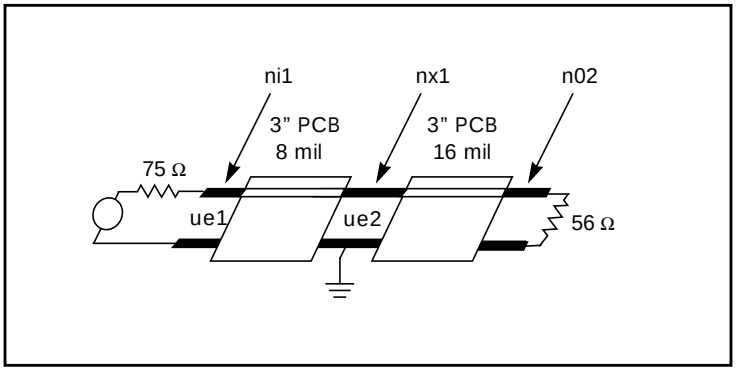


Figure A-42: Waveforms in Mismatched Transmission Line Structure

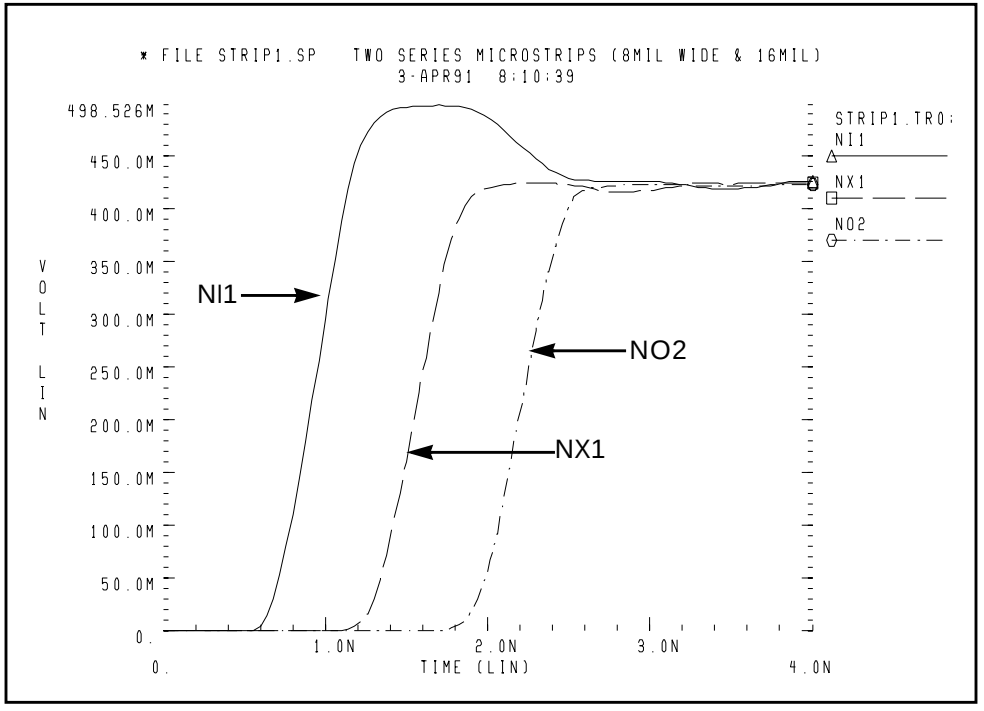
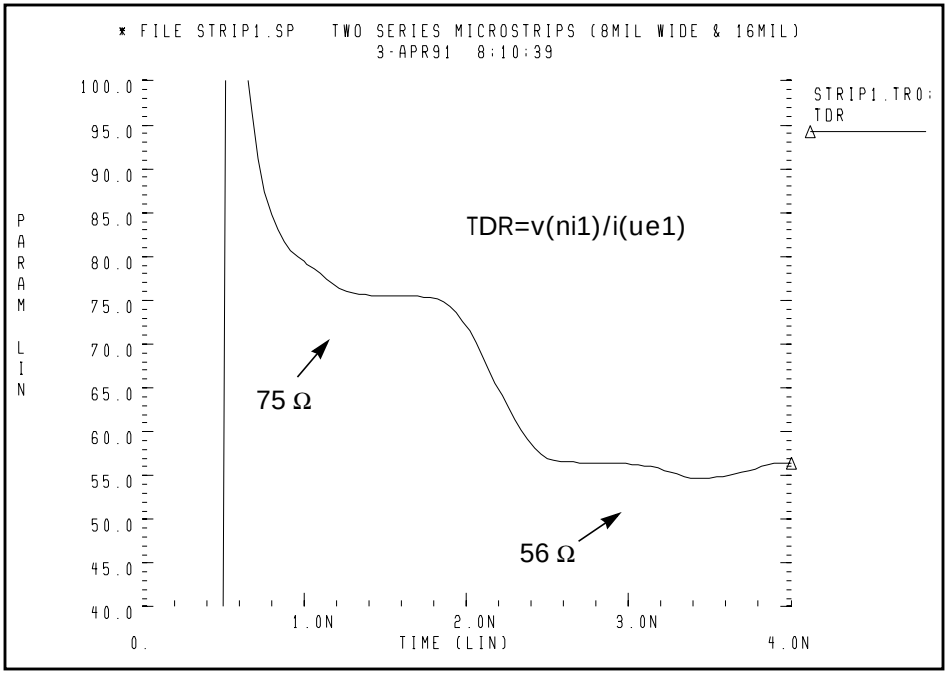


Figure A-43: Impedance from TDR at Input



Input File for Impedance Mismatch Example

```
* file strip1.sp
* Two series microstrips (8mil wide & 16mil) drive 3 inches
    of 8mil
* middle layer PCB, series connected to 3 inches of 16mil wide
* middle layer PCB, 500ns risetime driver. The tests
   following use
* geometric/physical model
.option acct post list
```

Signal Source

```
.tran 20ps 4ns
.probe tdr=par('v(ni1)/i(ue1)')
.PARAM R8mil=75 r16mil=56
* excitation voltage + prefilter
V1 np1 0 PWL 0.0s 0v 500ps 0v 1n 1v
xrI1 NP1 NI1 rcfilt rflt=r8mil tdflt=50ps
```

Circuit Definition

```
Ue1 NI1 0 NX1 0 u1 L=3000mil
Ue2 NX1 0 NO2 0 u2 L=3000mil
RO2 NO2 0 r16mil
* ...MODEL DEFINITION -- 8mil middle metal layer of a copper
   PCB
.MODEL u1 U LEVEL=3 plev=1 elev=1 nl=1
+ th=1.3mil ht=10mil ts=32mil kd=4.5 dlev=0
+ wd=8mil xw=-2mil
* ...MODEL DEFINITION -- 16mil middle metal layer of a copper
   PCB
.MODEL u2 U LEVEL=3 plev=1 elev=1 nl=1
+ th=1.3mil ht=10mil ts=32mil kd=4.5 dlev=0
+ wd=16mil xw=-2mil
.END
```

Transmission Line Theory

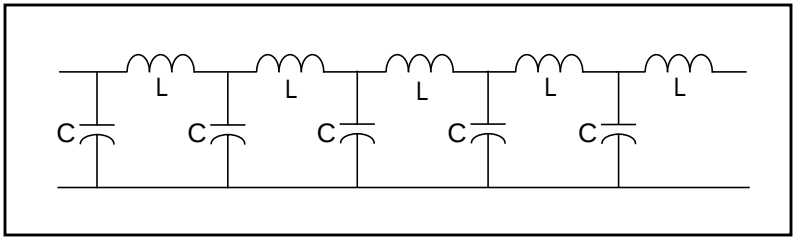
This section:

- Discusses how the discrete lumped model of the U Element transmission line explains characteristic impedance and transmission velocity
- Uses the concepts of self and mutual inductance to explain crosstalk
- Describes rules of thumb for various types of clock pulses
- Discusses the sources of transmission line attenuation

Lossless Transmission Line Model

As a signal propagates down the pair of conductors, each new section acts electrically as a small lumped circuit element. In its simplest form, called the lossless model, the equivalent circuit of a transmission line has just inductance and capacitance. These elements are distributed uniformly down the length of the line, as shown in Figure A-44.

Figure A-44: Equivalent Circuit Model of a Lossless Transmission Line



From this electrical circuit model, the two important terms that characterize a transmission line can be derived: the velocity of a signal (v) and the characteristic impedance (Z_0).

$$v = \frac{1}{\sqrt{L_L C_L}} \quad \text{and} \quad Z_0 = \sqrt{\frac{L_L}{C_L}}$$

L_L = inductance per length

C_L = capacitance per length

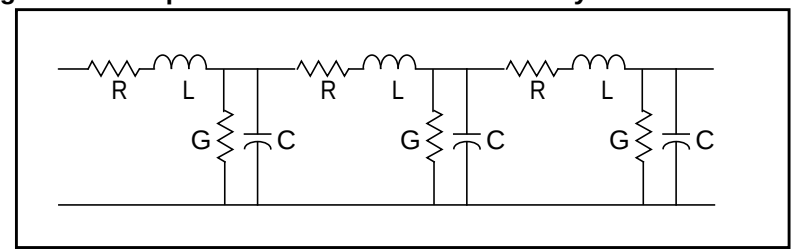
This is the basis for the T Element. It accounts for a characteristic impedance (Z_0) and a time delay (TD). The time delay depends on the distance (d) between the two ends of the transmission line:

$$TD = \frac{d}{v}$$

Lossy Transmission Line Model

When loss is significant, the effects of the series resistance (R) and the dielectric conductance (G) should be included. Figure A-45 shows the equivalent circuit model of a lossy transmission line, with distributed “lumps” of R, L, and C Elements.

Figure A-45: Equivalent Circuit Model of a Lossy Transmission Line



The U Element is the equivalent circuit model for the lossy transmission line. In a transient simulation, the U Element automatically accounts for frequency-dependent characteristic impedance, dispersion (frequency dependence in the velocity), and attenuation.

The most common types of transmission line cross sections are microstrip, stripline, coax, wire over ground, and twisted pair. There is no direct relationship between cross section, velocity of propagation, and characteristic impedance.

In a balanced transmission line, the two conductors have similar properties and are electrically indistinguishable. For example, each wire of a twisted pair has the same voltage drop per length down the line The circuit model for each wire has the same resistance capacitance and inductance per length.

This is not the case with a microstrip line or a coaxial cable. In those structures, the signal conductor has a larger voltage drop per length than the other conductor. The wide reference plane in a microstrip or the larger diameter shield

in a coax have lower resistance per length and lower inductance per length than the signal line. The equivalent circuit model for unbalanced lines typically assumes the resistance and inductance per length of the ground path is zero and all the voltage drop per length is on the signal conductor. Even though the inductance of the reference plane is small, it can play a significant role when there are large transient currents.

Impedance

The impedance of a device (Z) is defined as the instantaneous ratio of the voltage across the device (V) to the current through it:

$$Z = \frac{V}{I}$$

Impedance of Simple Lumped Elements

The impedance of a device can be thought of as the quality of the device that causes it to transform a current through it into a voltage across it:

$$V = ZI$$

The admittance (Y) is less often used to characterize a device. It is the inverse of the impedance:

$$Y = \frac{1}{Z} = \frac{I}{V}$$

There are three ideal circuit elements used to describe passive components: a resistor, a capacitor, and an inductor. They are defined by how they interact with voltage across them and current though them:

Resistor, with resistance (R):

$$V = IR$$

Capacitor, with capacitance (C):

$$I = C\frac{dV}{dt}$$

Inductor with inductance (L):

$$V = L\frac{dI}{dt}$$

When the voltage or current signals are time dependent, the impedance of a capacitive or inductive element is a very complicated function of time. You can simulate it, but it is difficult to build an intuitive model.

The impedance of a capacitor rotates the phase of the current 90° in the negative or direction to generate the voltage across the capacitor. The impedance of an inductor rotates the current 90° in the positive direction to generate the voltage across the inductor. For a resistor, the current and voltage have the same phase.

In the frequency domain, when all signals are sine waves in the time domain, the impedance of a capacitor and an inductor is frequency dependent, decreasing with frequency for a capacitor and increasing with frequency for an inductor. The impedance of a resistor is constant with frequency.

In the real world of finite dimensions and engineered materials, ideal circuit elements have parasitics associated with them, which cause them to behave in complex ways that are very apparent at high frequencies.

Characteristic Impedance

A controlled impedance transmission line is a pair of conductors that have a uniform cross section and uniform distribution of dielectric materials down their length. A short segment, Δx, of the transmission line has a small capacitance associated with it, ΔC, which is the capacitance per length, C_L, times the Δx:

$$\Delta C = C_L \Delta x$$

When a voltage signal is introduced at one end, the voltage between the conductors induces an electric that propagates the length of the line at the speed of light in the dielectric. As the voltage signal moves down the line, each new section of line charges up. The new section of line, Δx, is charged up in a time Δt:

$$\Delta t = \frac{\Delta x}{v}$$

If the voltage (V) moves down the line at a constant speed and the capacitance per length is uniform throughout the line, then the constant voltage applied to the front end draws a constant charging current (I):

$$I = \frac{\Delta Q}{\Delta t} = \frac{\Delta CV}{\Delta t} = \frac{C_L \Delta x V}{\Delta t} = C_L v V$$

This constant voltage with constant current has the behavior of a constant impedance (Z):

$$Z = \frac{V}{I} = \frac{V}{C_L v V} = \frac{1}{C_L v}$$

The impedance is determined by the speed of the signal and the capacitance per length of the pair of conductors, both intrinsic properties of the line. This intrinsic impedance is termed the characteristic impedance of the line (Z_0).

If a measurement is made at one end of the line in a short time compared to the round trip time delay, the line behaves like a resistor with a resistance equal to the characteristic impedance of the line. Transmission line effects are only important when rise times are comparable or shorter than the round trip time delay.

For example, if the rise time of a device is 1 ns, and it drives an interconnect trace in FR4 which is longer than three inches, the load on the device during the risetime is purely resistive. For CMOS devices, which are used to drive high resistance loads, the typical 50 ohm resistance they see initially can significantly distort the waveform from what is expected.

It is only during the initial surge of the voltage that a transmission line behaves as a constant impedance, with a value equal to its characteristic impedance. For this reason the characteristic impedance of a line is also called the surge impedance. The surge time during which the impedance is constant is the round trip time of flight, or twice the time delay. Reflections from the far end complicate the electrical behavior of the line after the surge time.

The instantaneous impedance measured at the front end of a transmission line is a complicated function of time. It depends on the nature of the terminations at the far end. When the line is shunted to ground with a resistor of value equal to the characteristic impedance of the line, there is no reflection back, and the front end of the line behaves as a resistive load. When the termination at the far end is

open, the impedance at the front end starts out at the characteristic impedance and eventually, after multiple reflections, approaches an infinite impedance. During some periods the instantaneous impedance may be zero. These transient effects are fully simulated with T Elements and U Elements.

Inductance

Mutual Inductance and Self Inductance

The most confusing, subtle and important parameter in high-speed packaging and interconnect design is inductance. It plays a key role in the origin of simultaneous switching noise, also called common ground inductance, and a key role in crosstalk between transmission line structures.

Operational Definition of Inductance

Consider an inductor to be any section of circuit element which carries current: an interconnect trace, a ground plane, a TAB lead frame, a lead in a DIP package, the lead of a resistor or a pin in a connector. An inductor does not have to be a closed circuit path, but can be a small section of a circuit path.

A changing current passing through an inductor generates a voltage drop. The magnitude of the voltage drop (ΔV) for an inductance (L) and change in current (dI/dt) is:

$$\Delta V = L\frac{dI}{dt}$$

This definition can always be used to evaluate the inductance of a section of a circuit. For example, with two long parallel wires, each of radius (r) and a center-to-center separation (s), you can measure the voltage drop per length for one of the wires when a changing current dI/dt flows through one wire and back through the other. The induced voltage per length on one of the wires is:

$$V_L = \frac{\mu_0}{2\pi} Ln\left(\frac{s}{r} - \frac{r}{s}\right)\frac{dI}{dt} \quad \text{[V in mV/inch, l in mA, t in ns]}$$

From this expression, the effective inductance per length of one wire is found to be:

$$L_L = \frac{\mu_0}{2\pi} Ln\left(\frac{s}{r} - \frac{r}{s}\right) \approx 5Ln\left(\frac{s}{r}\right) (s \gg r) \quad [nH/inch]$$

Mutual Inductance

A second effect also is important: the induced voltage from currents that are adjacent to, but not in, the same circuit path. This is caused by the mutual inductance between two current elements. A section of conductor in a circuit, labeled 1, may have an induced voltage generated across it because of currents not in circuit 1, but from circuits 2, 3, and 4.

The voltage generated across the section of circuit 1, V_1, is given in its general form by:

$$V_1 = L_{11}\frac{dI_1}{dt} + L_{12}\frac{dI_{I2}}{dt} + L_{13}\frac{dI_3}{dt} + L_{14}\frac{dI_4}{dt}$$

The notation for mutual inductance (L_{ab}) is related to the induced voltage on circuit element a, from the current element, b. In some texts, the symbol used is M, rather than L. The special case of the induced voltage on a circuit element from its own current (L_{aa}) is called self inductance.

Mutual inductance relates to the magnitude of induced voltage from an adjacent current. The magnitude of this voltage depends on the flux linkages between the two circuit elements.

Self Inductance

The self inductance of an isolated single trace is a well-defined, absolute mathematical quantity, but not a measurable physical quantity. There is always a return current path somewhere, and the mutual inductance from this return current path induces a voltage on the circuit element that subtracts from the self inductance. Self inductance can never be measured or isolated, independent of a mutual inductance of a return current path.

In the example above of two long parallel wires, the measured inductance per length (L_L) of one wire is neither the self inductance nor the mutual inductance of the wire. It is a combination of these two terms. If the universe contained just the two wires, the measured voltage drop per length would be:

$$V_L = L_{11}\frac{dI_1}{dt} - L_{12}\frac{dI_1}{dt} = (L_{11} - L_{12})\frac{dI_1}{dt} = L_L\frac{dI_1}{dt}$$

The minus sign reflects the opposite directions of the currents I_1 and I_2. Operationally, when the inductance per length of one wire is measured, what is really being measured is the difference between its self inductance and the mutual inductance of the return path. Because of this effect, it is clear that the nature of the return path greatly influences the measured inductance of a circuit element.

Reference Plane Return Paths

The capacitance per length (C_L) of any planar transmission line is:

$$C_L = \frac{85}{Z_0}\sqrt{\varepsilon_r} \quad [\text{pF/inch}]$$

The inductance per length of the signal line (L_L) is:

$$L_L = 0.085 Z_0 \sqrt{\varepsilon_r} \quad [\text{nH/inch}]$$

This is the self inductance of the signal line, minus the mutual inductance of the return current in the reference plane.

For example, the inductance per length of a transmission line with characteristic impedance of 50 ohms in an FR4 printed circuit board is 9.6 nH/inch. The capacitance per length is 3.8 pF/inch. In the equivalent circuit of a lossless transmission line, the series inductance per length is 9.6 nH/inch, and the shunt capacitance to ground is 3.8 pF/inch.

In the notation of the U Element, for an ELEV=2 (RCLK equivalent model) and a PLEV=1 (microstrip cross section), the parameters to model this lossless transmission line are

C11 = 3.8 pF/inch, L11 = 9.6 nH/inch

The LLEV=0 parameter simplifies the inductance problem by automatically calculating the inductance of the line, as the difference between the self inductance of the line and the mutual inductance of the return signal path.

In many texts, the term L11 is generically used as the self inductance. LLEV=1 assumes a circuit ground point, separate from the reference plane of the transmission line. Thus the LLEV=1 option includes an approximation to the self inductance of both the signal conductor and the reference plane, while LLEV=0 assumes a reference plane return current.

Crosstalk in Transmission Lines

When there are adjacent transmission lines, for instance line 2 and line 3, the coupling capacitance and inductance between them and the quiet line, line 1, lead to crosstalk.

In the notation of the Avant! transmission line models, the voltage per length on transmission line 1, V_1, including the mutual inductance to lines 2 and 3 is:

$$V_1 = L11\frac{dI_1}{dt} + L12\frac{dI_2}{dt} + L13\frac{dI_3}{dt}$$

LLEV=0 simplifies the inductance analysis by automatically including the effects of the return current path. The first inductance term (L11) is the inductance per length of the transmission line (1) including the self inductance of the line and the mutual inductance of the return ground path.

The second term, the coupling inductance of the second transmission line (L12), includes the mutual inductance of the second signal line and the mutual inductance of the return current path of the second line. Because these two currents are in opposite directions, the mutual inductance of the pair is much less than the mutual inductance of just the second signal trace alone.

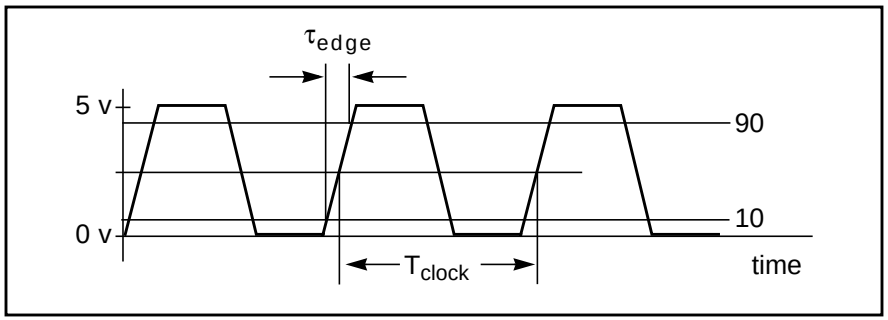
The third term (LL13) includes the mutual inductance of the signal path in the third transmission line and the mutual inductance of its return path through the reference plane.

The coupling inductances (L12 and L13) include the mutual inductances of the adjacent signal lines and their associated return paths. They are more than the mutual inductance of the adjacent traces. This is equivalent to the operational inductances that you can measure with a voltmeter and a dI/dt source.

Risetime, Bandwidth, and Clock Frequency

In the time domain, a clock waveform can be described in terms of its period (T_{clock}), its frequency (F_{clock}), and a risetime (τ_{edge}). Figure A-46 illustrates these features.

Figure A-46: Clock Waveform



The risetime is typically defined by the time between the 10% to 90% points.

To describe this waveform in terms of sine wave components, the highest sine wave frequency required (the bandwidth, BW) depends on the risetime. As the bandwidth increases and higher sine wave frequency components are introduced, the risetime of the reconstructed waveform decreases. The bandwidth of a waveform is determined by the fastest risetime it contains. The risetime and bandwidth are related by:

$$BW = \frac{0.35}{\tau_{edge}} \text{ or } \tau_{edge} = \frac{0.35}{BW}$$

The risetime of a clock waveform and the clock period are only indirectly related. The risetime of a system is determined by the output driver response and the characteristics of the packaging and interconnect. In general, the risetime is made as long as possible without degrading the clock period.

Without specific information about a system, it is difficult to know precisely what the risetime is, given just the clock frequency or period. In a fast system such as an oscillator with only one gate, the period might be two times the risetime:

$$T_{period} \approx 2\tau_{edge}$$

For a complex system such as a microprocessor board, the period might be 15 times as long as the risetime:

$$T_{period} \approx 15\tau_{edge}$$

In each case, the bandwidth is always related to the risetime by the first expression in this section, and the clock frequency and clock period are always related by:

$$F_{clock} = \frac{1}{T_{clock}}$$

The example of the microprocessor would give the worst case of the shortest risetime for a given clock period. Combining these expressions shows the relationship between clock frequency and bandwidth:

$$F_{clock} = \frac{1}{T_{clock}} = \frac{1}{15\tau_{edge}} = \frac{BW}{15 \cdot 0.35} \approx \frac{1}{5}BW \text{ or } BW \approx 5F_{clock}$$

In general, the highest sine wave frequency component contained in a clock waveform is five times the clock frequency. The important assumption is that there are about 15 risetimes in one period. If the risetime is actually faster than this assumption, the bandwidth is higher. To provide a safety margin, a package or interconnect is characterized or simulated at a bandwidth of about 10 to 20 times the clock frequency, which corresponds to roughly two to four times the bandwidth of the signal.

Definitions of Transmission Line Terms

Table A-10: Transmission Line Terms *(Sheet 1 of 3)*

F_{clock}	Clock frequency in units of frequency such as Hz
T_{clock}	Clock period in units of time such as secs or ns
t_{edge}	Rise or fall time in units of time such as sec or ns
BW	Bandwidth in units of frequency such as Hz or MHz
F	A repetitive frequency in units of Hz or MHz

Table A-10: Transmission Line Terms *(Sheet 2 of 3)*

f	A sine wave frequency in units of Hz or MHz
ω	An angular frequency in units of radians/sec
t	Time or a conductor thickness, units of sec or length
V(t)	Instantaneous voltage in units of volts
I(t)	Instantaneous current in units of amps or mA
Z(t)	Instantaneous impedance in units of ohms
$Z(\omega)$	Frequency domain, complex impedance in units of ohms
C	Capacitance in units of Farads or microFarads
R	Resistance in units of ohms
L	Inductance in units of Henrys or nanoHenries
v	Speed of light in the medium in units of length/time
d	A length in units such as inches
TD	Time delay in units of time such as sec or nsec
C_L	Capacitance per length in units such as pF/inch
L_L	Inductance per length in units such as nH/inch
R_L	Resistance per length in units such as ohms/inch
ε_r	Relative dielectric constant, $\varepsilon/\varepsilon_0$, dimensionless
r	Reflection coefficient, dimensionless
DZ	A small change in characteristic impedance
G_L	Conductance per length units of Mhos (Siemens)/length
$\tan(\delta)$	Dissipation factor of a material, dimensionless
d	Skin depth of a conductor, units of length such as meter

Table A-10: Transmission Line Terms *(Sheet 3 of 3)*

ρ	Resistivity of a conductor, units of ohm-length
μ_0	Permeability of free space = 4 p x 10-7 Henry/meter
α	Attenuation per length, units of dB/len or nepers/len
w	A conductor width
n	Number of squares in a planar conductor, dimensionless
R_{sq}	Sheet resistance of a planar conductor, units: ohms/sq
ε_0	Permittivity of free space=0.225 pF/inch=0.0885 pF/cm
ε_{eff}	Effective dielectric constant due to mixed dielectrics
h	A dielectric thickness in units of length such as mils
R	Resistance in ohms

Relationships and Rules of Thumb

Time and Frequency Relationships

$$F_{clock} = \frac{1}{T_{clock}}$$

$$BW = \frac{0.35}{\tau_{edge}} \text{ or } \tau_{edge} = \frac{0.35}{BW}$$

$$T_{period} \approx 15\tau_{edge}$$

$$F_{clock} \approx \frac{1}{5}BW \text{ or } BW \approx 5F_{clock}$$

Transmission Line Effects

Transmission line analysis recommended for:

$$BW > \frac{v}{10d} = \frac{1}{10 \cdot TD}$$

$$\tau_{edge} < \frac{5d}{v} = 5 \cdot TD$$

On FR4 material,

$$BW > \frac{600}{d} \quad [BW \text{ in MHz, d in inches}]$$

$$F_{clock} > \frac{120}{d} \quad [F_{clock} \text{ in MHz, d in inches}]$$

$$\tau_{edge} < \frac{d}{7.5} \quad \tau_{edge} \text{ [in ns, d in inches]}$$

Intrinsic Properties

$$Z_0 = \frac{1}{vC_L} = \sqrt{\frac{L_L}{C_L}} \quad [C_L \text{ is in pF/inch}$$

$$v = \frac{1}{\sqrt{L_L C_L}}$$

$$C_L = \frac{1}{vZ_0} = \frac{\sqrt{\varepsilon_r}}{cZ_0} = \frac{85}{Z_0}\sqrt{\varepsilon_r} \quad [pF/inch]$$

$$L_L = \frac{1}{C_L v^2} = \frac{7.3\varepsilon_r}{C_L} \quad [L_L \text{ in nH/inch, } C_L \text{ in pF/inch}]$$

Typical polymers

$$TD = \frac{d}{6} \quad \text{[TD in ns, d in inches]}$$

$$C_L = \frac{170}{Z_0} \quad \text{[pF/inch]}$$

$$L_L = 0.172 Z_0 \quad \text{[nH/inch]}$$

50 ohm lines

$$C_L = 1.7\sqrt{\varepsilon_r} \quad \text{[pF/inch = 3.4 pF/inch (typical polymer)]}$$

$$L_L = 4.3\sqrt{\varepsilon_r} \quad \text{[nH/inch = 8.6 nH/inch (typical polymer)]}$$

Transmission line of length d

$$C = C_L d = \frac{TD}{Z_0}$$

$$L = L_L d = Z_0 TD$$

Reflections

Reflection coefficient from Z_1 to Z_2:

$$r = \frac{Z_2 - Z_1}{Z_2 + Z_1}$$

Reflection from a ΔZ, of short length with time delay, TD, τ_{edge} > TD:

$$r = \frac{\Delta Z}{2Z_0}\left(\frac{TD}{\tau_{edge}}\right)$$

Reflection from a series lumped L surrounded by a transmission line:

$$r = \frac{L}{2Z_0\tau_{edge}}$$

Reflection from a lumped C load to ground, on a transmission line:

$$r = \frac{CZ_0}{2\tau_{edge}}$$

Loss and Attenuation

Skin depth of a conductor:

$$\delta = \sqrt{\frac{\rho}{\pi\mu_0 f}} = 500 \cdot \sqrt{\frac{\rho}{f}}$$

δ [in meters, ρ in ohm·meter, f in Hz: in copper, at f = 1e+9 and ρ =1.7e-8 ohm·meter, δ = 2.0e-6]

Low loss approximation for attenuation per length:

$$\alpha = \frac{1}{2}\left(\frac{R_L}{Z_0} + G_L Z_0\right) \quad \text{[nepers/length]}$$

$$\alpha = 4.34\left(\frac{R_L}{Z_0} + G_L Z_0\right) \quad \text{[dB/length]}$$

Attenuation per length due to just dielectric loss:

$$\alpha = 2.3 f \tan(\delta)\sqrt{\varepsilon_r} \quad \text{[dB/inch, f in GHz]}$$

$$\alpha \approx 0.05 \quad \text{[dB/inch for FR4 at 1 GHz]}$$

Attenuation per length due to metal, $t < \delta$:

$$\alpha = 43.4\frac{\rho}{twZ_0} \quad \text{[dB/inch, with } \rho \text{ in ohm·meter, t in microns, w in mils]}$$

For 1 ounce copper microstrip, 5 mils wide, 50 ohm:

$$\alpha = 0.01 \quad \text{[dB/inch]}$$

Attenuation per length due to metal, 50 ohm line, skin depth limited, $t > \delta$:

$$\alpha = 0.55\frac{\sqrt{\rho f}}{w} \quad \text{[dB/inch, with } \rho \text{ in ohm·meter, w in mils, f in GHz]}$$

For 1 ounce copper microstrip, 5 mils wide, 50 ohm, at 1 GHz:

$$\alpha = 0.15 \quad \text{[dB/inch]}$$

Physical Design Quantities

For a planar interconnect:

Sheet resistance:

$$R_{sq} = \frac{\rho}{t} \quad \text{[ohm/sq]}$$

Number of squares:

$$n = \frac{d}{w}$$

Resistance:

$$R_L = n \cdot R_{sq} \quad \text{[ohm/inch, } R_{sq} \text{ in ohm/sq]}$$

Resistance per length:

$$R_L = 10\frac{\rho}{tw} \quad \text{[ohm/inch, } \rho \text{ in ohm·meter, t in microns, w in mils]}$$

Parallel plate, no fringe fields:

$$C_L = 0.225\varepsilon_r\left(\frac{w}{h}\right) \quad \text{[pF/inch]}$$

Microstrip capacitance per length good to ~20%:

$$C_L = 0.45\varepsilon_r\left(\frac{w}{h}\right) \quad \text{[pF/inch]}$$

Microstrip capacitance per length, good to ~5%:

$$C_L = \frac{1.41\varepsilon_{eff}}{\ln\left(\frac{8h}{w} + \frac{w}{4h}\right)}$$

$$\varepsilon_{eff} = \left(\frac{\varepsilon_r + 1}{2}\right) + \left(\frac{\varepsilon_r - 1}{2}\right)\left(1 + \frac{10h}{w}\right)^{-\frac{1}{2}}$$

Stripline capacitance per length good to ~20%:

$$C_L = 0.675\varepsilon_r\left(\frac{w}{h}\right) \quad \text{[pF/inch]}$$

Stripline capacitance per length, good to ~5%:

$$C_L = \frac{0.9\varepsilon_r}{\ln\left(1 + \frac{2h}{w}\right)} \quad \text{[pF/inch]}$$

Inductance per length of one wire in a pair of two parallel wires:

(r = radius, s = center to center spacing, $s \gg r$)

$$L_L = 5Ln\left(\frac{s}{r}\right) \quad \text{[nH/inch]}$$

Inductance per length for a circular loop:

$$L_L = 26 \quad \text{[nH/inch of perimeter]}$$

Inductance per length of controlled impedance line, when the return line is a reference plane:

$$L_L = 0.086Z_0\sqrt{\varepsilon_r} = \frac{7.3\varepsilon_r}{C_L} \quad \text{[nH/inch with } C_L \text{ in pF/inch]}$$

Conductance per length:

$$G_L = \omega\tan(\delta)C_L$$

Attenuation in Transmission Lines

The T Element, common to most Berkeley-compatible SPICE tools, uses the lossless model for a transmission line. This model adequately simulates the dominant effects related to transmission behavior: the initial driver loading due to a resistive impedance, reflections from characteristic impedance changes, reflections introduced by stubs and branches, a time delay for the propagation of the signal from one end to the other and the reflections from a variety of linear and nonlinear termination schemes.

In systems with risetimes are on the order of 1 ns, transmission line effects dominate interconnect performance.

In some high-speed applications, the series resistance seriously effects signal strength and should be taken into account for a realistic simulation.

The first-order contribution from series resistance is an attenuation of the waveform. This attenuation decreases the amplitude and the bandwidth of the propagating signal. As a positive result, reflection noise decreases, so that a lossless simulation is a worst case. As a negative result, the effective propagation delay is longer because the risetimes are longer. A lossless simulation shows a shorter interconnect related delay than a lossy simulation.

The second-order effects introduced by series resistance are a frequency dependence to the characteristic impedance and a frequency dependence to the speed of propagation, often called dispersion. Both the first order and second order effects of series resistance generic to lossy transmission lines are simulated using the U model.

The Physical Basis of Loss

The origin of loss is the series resistance of the conductors and the dielectric loss of the insulation. Conductor resistance is considered in two parts, the DC resistance and the resistance when skin depth plays a role. The dielectric loss of the insulation, at low frequency, is described by the material conductivity (σ) (SIG in the Avant! U model), and at high frequency, by the dissipation factor, tan(δ). These material effects contribute a shunt conductance to ground (G).

In a planar interconnect such as a microstrip or stripline, the resistance per length of the conductor R_L is

$$R_L = \frac{\rho}{wt}$$

ρ = bulk resistivity of the conductor
w = the line width of the conductor
t = thickness of the conductor

Example 1: FR4, 5 mil wide line, half ounce copper:

R_L = 0.24 ohm/inch

Example 2: Cofired ceramic, 4 mil wide, 0.75 mils thick Tungsten:

R_L = 2.7 ohm/inch

Example 3: Thin film copper, 1 mil wide, 5 microns thick:

R_L = 3.6 ohm/inch

Skin Depth

At high frequency, the component of the electric field along the conductor, which drives the current flow, does not fully penetrate the conductor depth. Rather, its amplitude falls off exponentially. This exponential decay length is the *skin depth* (δ). When the signal is a sine wave, the skin depth depends on the conductor's resistivity (ρ), and the sine wave frequency of the current (f):

$$\delta = \sqrt{\frac{\rho}{\pi \mu_0 f}} = 500 \cdot \sqrt{\frac{\rho}{f}} \quad \delta \text{ [in meters, r in ohm·meter, f in Hz]}$$

A real signal has most of its energy at a frequency of $1/t_{period}$, where t_{period} is the average period. Because most of the loss occurs at this frequency, as a first approximation >> should be used to compute the skin depth. In practice, as mentioned previously, approximating tperiod by $15(\tau_{edge})$ works well. With a 1 ns rise time, the skin depth of copper is 8 microns, assuming $15(\tau_{edge})$ is used for $1/f_{skin}$. For half ounce copper, where the physical thickness is 15 microns, the skin depth thickness should be used in place of the conductor thickness to estimate the high frequency effects.

For thin film substrates with a physical thickness of the order of 5 microns or less, the effects of skin depth can, to the first order, be ignored. In cofired ceramic substrates, the skin depth for 1 ns edges with tungsten paste conductors is 27.6 microns. This is also comparable to the 19 micron physical thickness, and to the first order, the effects of skin depth can be ignored. At shorter rise times than 1 ns, skin depth plays an increasingly significant role.

Dielectric Loss

Two separate physical mechanisms contribute to conductivity in dielectrics, which results in loss: DC conduction and high frequency dipole relaxation. As illustrated in the following section, the effects from dielectric loss are in general negligible. For most practical applications, the dielectric loss from the DC conductivity and the high frequency dissipation factor can be ignored.

To be cautious, estimate the magnitude of the conductance of the dielectric and verify that, for a particular situation, it is not a significant issue. Exercise care in using these material effects in general application.

The bulk conductivity of insulators used in interconnects (σ), typically specified as between 10^{-12} and 10^{-16} siemens/cm, is often an upper limit, rather than a true value. It is also very temperature and humidity sensitive. The shunt conductance per length (G_L) depends on the geometrical features of the conductors in the same way as the capacitance per length (C_L). It can be written as:

$$G_L = \sigma \frac{C_L}{\varepsilon_0 \varepsilon_r}$$

At high frequencies, typically over 1 MHz, dipole relaxations begin to dominate the conduction current and cause it to be frequency dependent. This effect is described by the dissipation factor of a material, which ranges from 0.03 for epoxies down to 0.003 for polyimides and less than 0.0005 for ceramics and Teflon. The effective conductivity of a dielectric material at high frequency is:

$$\sigma = 2\pi f \varepsilon_0 \varepsilon_r \tan(\delta)$$

The shunt conductance per length of an interconnect, when dipole relaxation dominates, is:

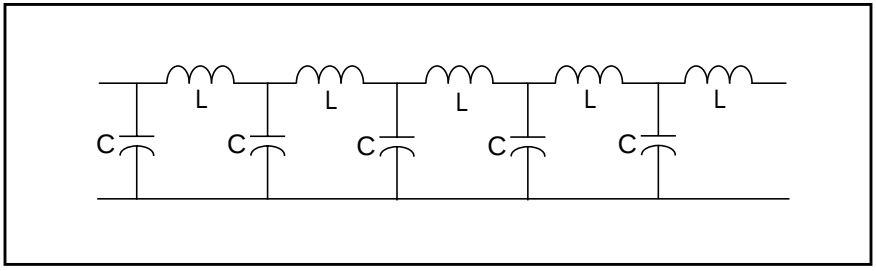
$$G_L = 2\pi f \tan(\delta) C_L$$

As a worst case, the frequency corresponding to the bandwidth of the signal can be used to estimate the high frequency conductivity of the material.

The Lossy Transmission Line Model

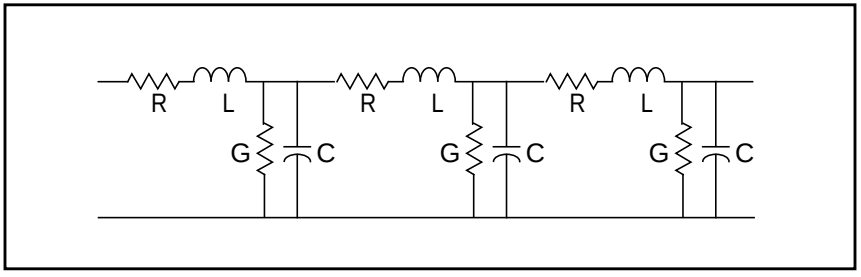
In the lossless transmission line model, only the distributed capacitance (C) and inductance (L) of the interconnect is considered:

Figure A-47: Lossless Transmission Line Model



In the lossy transmission line model, the series resistance and dielectric conductance are introduced into the equivalent circuit model:

Figure A-48: Lossy Transmission Line Model



These four circuit elements, normalized per unit length, can be used to describe all the high frequency properties of a transmission line. When the equivalent circuit equation is solved in the frequency domain, the characteristic impedance is modified to:

$$Z_0 = \sqrt{\frac{R_L + j\omega L_L}{G_L + j\omega C_L}}$$

and the propagation phase term, γ, is:

$$\Upsilon = \alpha + j\beta = \sqrt{(R_L + j\omega L_L)(G_L + j\omega C_L)}$$

In the propagation phase term, β is related to the phase velocity by:

$$v = \frac{\omega}{\beta}$$

To first order, when $R_L << \omega L_L$ and $G_L << \omega C_L$, the characteristic impedance and phase velocity (*v)* are unchanged from their lossless values. However, a new term, the attenuation per length (α) is introduced.

The attenuation per length is approximately:

$$\alpha = \frac{1}{2}\left(\frac{R_L}{Z_0} + G_L Z_0\right) \quad \text{[nepers/length]}$$

$$\alpha = 4.34\left(\frac{R_L}{Z_0} + G_L Z_0\right) \quad \text{[dB/length]}$$

The total attenuation (αd) determines the fraction of the signal amplitude that remains after propagating the distance (d). When α has the units of dB/length, the fraction of signal remaining is:

$$10^{\left(\frac{-\alpha d}{20}\right)}$$

It is useful to keep in mind that a 2 dB attenuation in a signal corresponds to a final amplitude of 80% of the original and 6 dB attenuation corresponds to a final amplitude of 50% of the original. Attenuation on the order of 6 dB significantly changes the signal integrity.

Attenuation Due to Conductor Resistance

In the typical case of a 50 ohm transmission line, the attenuation per length due to just the series resistance is

$$\alpha = 0.09 R_L \quad \text{[dB/length]}$$

When the resistance per length is of the order of 0.2 ohm/inch or less, as is the case in typical printed circuit boards, the attenuation per length is about 0.02 dB/inch. Typical interconnect lengths of 10 inches yields only 0.2 dB, which would leave about 98% of the signal remaining. Using the lossless T Element to approximate most applications provides a good approximation.

However, in fine line substrates, as the examples in the previous section illustrated, the resistance per length can be on the order of 2 ohms/inch. In such a case, the attenuation is on the order of 0.2 dB/inch. So a 10 inch interconnect line then has an attenuation on the order of 2 dB, which would leave only about 80% of the signal. This is large enough that its effects should be included in a simulation.

Attenuation Due to the Dielectric

When the dielectric completely surrounds the conductors, the attenuation due to just the conductance per length of the dielectric is:

$$\alpha_{dielectric} = 2.3 f \tan(\delta) \sqrt{\varepsilon_{eff}} \quad \text{[dB/inch, f in GHz]}$$

The worst case and highest attenuation per length is exhibited by FR4 boards, with tan(δ) of the order of 0.02 and a dielectric constant of 5. The attenuation at 1 GHz is about 0.1 dB/inch. For an interconnect 10 inches long, this is 1 dB of attenuation, which would leave about 90% of the signal remaining, comparable to the attenuation offered by a conductor with 1 ohm/inch resistance.

When the resistance per length is larger than 1 ohm/inch— for example in cofired ceramic and thin film substrates, and the dissipation factor is less than 0.005, the attenuation from the conductor losses can be on the order of 10 times greater than dielectric loss. In these applications, the dielectric losses can be ignored.

Integrating Attenuation Effects

All of the first-order effects of attenuation are automatically simulated with the U Element.

With ELEV=1, the inputs can be the cross sectional geometry and the material properties of the conductor, bulk resistivity (RHO), the relative dielectric constant of the insulation (KD), and the conductivity of the dielectric (SIG). From these features, the equivalent capacitance per length, inductance per length, series resistance per length, and conductance per length are calculated during simulation.

With ELEV=2, the equivalent capacitance per length, inductance per length, series resistance per length, and conductance per length are input directly using estimates, measurements or third-party modeling tools.

Simulation automatically generates a model for the specified net, composed of a series of lumped elements that resembles the model for a lossy transmission line. The parameter WLUMPS controls the number of lumped elements included per wavelength, based on the estimated rise time of signals in the simulation.

The attenuation effects previously described are a natural consequence of this model. The U Element allows realistic simulations of lossy transmission lines in both the AC and the transient domain.

References

Handbook of Electronics Calculations for Engineers and Technicians, McGraw Hill, pages 18-29, 18-23.

Avant!

Appendix B
Finding Device Libraries

For libraries with multiple models of a specific element, you need to be able to automatically find the proper model for each transistor size. Use the automatic model selector in Star-Hspice or Star-Sim (or in their XT versions) to accomplish this.

This chapter describes how to use the model selector, then provides listings of device libraries that you can use.

The following topics are covered in this chapter:

Selecting Models Automatically

The model selector uses the following criteria:

$$LMIN + XLREF \leq L + XL < LMAX + XLREF$$

$$WMIN + XWREF \leq W + XW < WMAX + XWREF$$

(If XLREF is not specified, XLREF is set to XL. If XWREF is not specified, XWREF is set to XW.)

The model selector syntax is based on a common model root name, with a unique extension for each model.

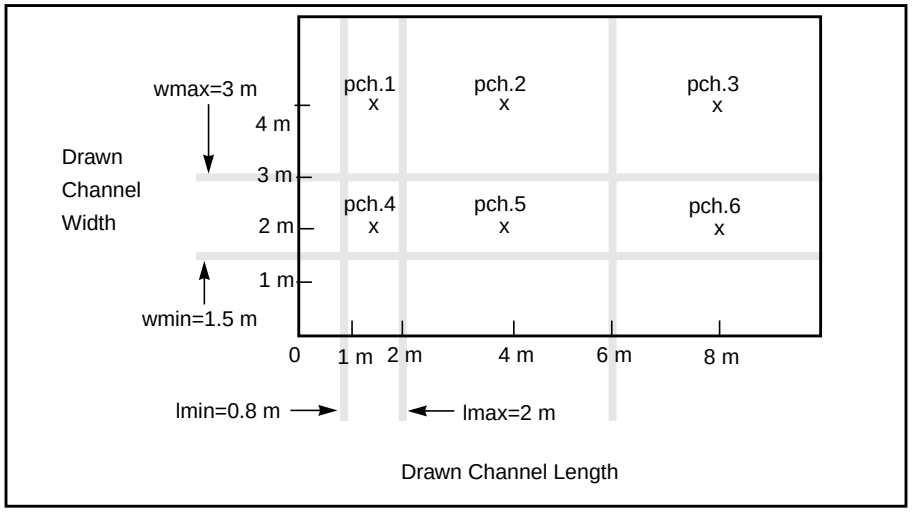
Note: The preceding does not apply to JFETs.

The following is an example of HSPICE syntax for models:

```
M1 drain gate source bulk NJ W=2u L=1u
.MODEL NJ4 NJF WMIN=1.5u WMAX=3u LMIN=.8u LMAX=2u
.MODEL NJ5 NJF WMIN=1.5u WMAX=3u LMIN=2u LMAX=6u
```

Figure B-1 illustrates the model selection method.

Figure B-1: Automatic Model Selector Method



For this example, there are several pch.*x* models, with varying drawn channel lengths and widths, in the model library. (The model root name is pch and the extensions are 1, 2, ..., 6). The NJ4 instance of the NJ Element (W=2 μ, L=1 μ) requires a model for which 1.5 μ ≤ channel width ≤ 3 μ, and 0.8 μ ≤ channel length ≤ 2 μ. The automatic model selector chooses the pch.4 model since that model satisfies these requirements. Similarly, the NJ5 transistor requires a model with 1.5 μ ≤ channel width ≤ 3 μ, and 2 μ ≤ channel length ≤ 6 μ. The pch.5 model satisfies these requirements. If a device size is out of range for all the models that exist, an error message is issued.

If a model within a sub-circuit cannot be found, the automatic model selector searches the top level. If the automatic model selector fails to find a model, simulation terminates.

The following combination of conditions causes the automatic model selector to fail and terminates simulation:

1. In the element statement, a model name is used which contains a period (.).
2. The model library was not designed for use with the automatic model selector.
3. Either a multisweep specification or a .TEMP temperature analysis statement is included in the simulation input.

The following example illustrates how a period in a model name can cause automatic model selection problems.

Case 1

```
M1 d g s b N.CHN W=10u L=5u                          * Element statement
.MODEL N.CHN LMIN=1u LMAX=4u WMIN=2u WMAX=100u      * .MODEL statement
```

Case 2

```
.TEMP 25
.M1 d g s b N.CHN W=10u L=5u                         * Element statement
.MODEL N.CHN LMIN=1u LMAX=4u WMIN=2u WMAX=100u      * .MODEL statement
```

In Case 1, since there is no multisweep or temperature analysis specified, the model selector feature is not invoked, so the N.CHN model is used with no problems.

In Case 2, however, the presence of the .TEMP statement invokes the model selector feature. The model selector tries to find a model named N.*nnn* that fits within the length and width ranges given in the element statement. Because the length given in the element statement (5 μm) is not within the 1 to 4 μm range specified in the .MODEL statement, the model selector cannot find a model that matches the element statement, and simulation issues a “device ‘N’ not found” error message.

Examining the Library Listings

The names of models that Avant! provides for its Star-Hspice and Star-Sim simulators are listed in the following sections. Each type of model is stored in a directory that has a name indicating the type of models it contains, such as *dio* for diodes and *bjt* for bipolar junction transistors. The path to the directory is shown for each model type. This path can be specified in a .OPTION SEARCH statement, such as:

```
.OPTION SEARCH '$installdir/96/parts/dio'
```

where *$installdir* is the environment variable set to the path to the software installation directory and 96 is the HSPICE release number. All model directories are under the *parts* directory.

Analog Device Models

Search path: *$installdir/parts/ad*

Table B-11: Analog Model Names (Sheet 1 of 4)

AD581	AD581J	AD581K	AD581L	AD581S
AD581T	AD581U	AD584	AD584J	AD584K
AD584L	AD584S	AD584T	AD587	AD587J
AD587K	AD587L	AD587S	AD587T	AD587U
AD600	AD600J	AD602	AD602J	AD620
AD620A	AD620B	AD620S	AD624	AD624A
AD624B	AD624C	AD624S	AD630	AD630A
AD630B	AD630J	AD630K	AD630S	AD633
AD633J	AD645	AD645A	AD645B	AD645J
AD645K	AD645S	AD704	AD704A	AD704B
AD704J	AD704K	AD704T	AD705	AD705A
AD705B	AD705J	AD705K	AD705T	AD706
AD706A	AD706B	AD706J	AD706K	AD706T

Table B-11: Analog Model Names (Sheet 2 of 4)

AD711	AD711A	AD711B	AD711C	AD711J
AD711K	AD711S	AD711T	AD712	AD712A
AD712B	AD712C	AD712J	AD712K	AD712S
AD712T	AD713	AD713A	AD713B	AD713J
AD713K	AD713S	AD713T	AD734	AD734A
AD734B	AD734S	AD743	AD743A	AD743B
AD743J	AD743K	AD743S	AD744	AD744A
AD744B	AD744C	AD744J	AD744K	AD744S
AD744T	AD745	AD745A	AD745B	AD745J
AD745K	AD745S	AD746	AD746A	AD746B
AD746J	AD746S	AD780	AD780A	AD780B
AD780S	AD797	AD797A	AD797B	AD797S
AD810	AD810A	AD810S	AD811	AD812
AD812A	AD813	AD813A	AD817	AD817A
AD818	AD818A	AD820	AD826	AD826A
AD828	AD828A	AD829	AD829A	AD829J
AD829S	AD830	AD830A	AD830J	AD830S
AD840	AD840J	AD840K	AD840S	AD843
AD843A	AD843B	AD843J	AD843K	AD843S
AD844	AD844A	AD844B	AD844S	AD845
AD845A	AD845B	AD845J	AD845K	AD845S
AD846	AD846A	AD846B	AD846S	AD847
AD847A	AD847J	AD847S	AD848	AD848A
AD848J	AD848S	AD9617	AD9618	AD9621
AD9622	AD9623	AD9624	AD9630	ADG411
ADG411B	ADG411T	ADG412	ADG412B	ADG412T
ADG413	ADG413B	ADG413T	AMP01	AMP02
BUF04	MAT02	MAT03	MAT04	MLT04

Table B-11: Analog Model Names (Sheet 3 of 4)

MLT04G	OP160	OP160A	OP160F	OP160G
OP176	OP176G	OP177	OP177A	OP177B
OP177E	OP177F	OP177G	OP20	OP200
OP200A	OP200E	OP200F	OP200G	OP20B
OP20C	OP20F	OP20G	OP20H	OP21
OP213	OP215	OP215A	OP215B	OP215C
OP215E	OP215F	OP215G	OP21A	OP21E
OP21F	OP21G	OP21H	OP220	OP220A
OP220C	OP220E	OP220F	OP220G	OP221
OP221A	OP221B	OP221C	OP221E	OP221G
OP249	OP249A	OP249E	OP249F	OP249G
OP260	OP27	OP275	OP275G	OP27A
OP27B	OP27C	OP27E	OP27F	OP27G
OP282	OP282G	OP283	OP285	OP285G
OP290	OP290A	OP290E	OP290F	OP290G
OP292	OP295	OP297	OP297A	OP297E
OP297F	OP297G	OP37	OP37A	OP37B
OP37C	OP37E	OP37F	OP37G	OP400
OP400A	OP400E	OP400F	OP400G	OP400H
OP41	OP41A	OP41B	OP41E	OP41F
OP41G	OP42	OP420	OP420B	OP420C
OP420F	OP420G	OP420H	OP421	OP421B
OP421C	OP421F	OP421G	OP421H	OP42A
OP42E	OP42F	OP42G	OP43	OP43A
OP43B	OP43E	OP43F	OP43G	OP44
OP467	OP467G	OP470	OP482	OP482G
OP490	OP490A	OP490E	OP490F	OP490G
OP492	OP497	OP497A	OP497B	OP497C

Table B-11: Analog Model Names (Sheet 4 of 4)

OP497F	OP497G	OP61	OP64	OP77
OP77A	OP77B	OP77E	OP77F	OP77G
OP80	OP80B	OP80E	OP80F	OP80G
OP90	OP90A	OP90E	OP90F	OP90G
OP97	OP97A	OP97E	OP97F	PM1012
REF01	REF01A	REF01C	REF01E	REF01H
REF02	REF02A	REF02C	REF02D	REF02E
REF02H	REF05	REF05A	REF05B	REF10
REF10A	REF10B	SSM2017	SSM2017P	SSM2131
SSM2210	SSM2220			

Behavioral Device Models

Required element syntax: Xyyyyy in- in+ out vcc vee modelname

- Search path: *$installdir/parts/behave*
- Optional parameters: vos=value, ibos=value, av=value

Table B-12: Behavioral Model Names

AD4BIT	AD8BIT	ALF155	ALF156	ALF157
ALF255	ALF347	ALF351	ALF353	ALF355
ALF356	ALF357	ALF3741	ALM101A	ALM107
ALM108	ALM108A	ALM111	ALM118	ALM124
ALM124A	ALM139A	ALM1458	ALM1558	ALM158
ALM158A	ALM201A	ALM207	ALM208	ALM208A
ALM224	ALM258	ALM258A	ALM2901	ALM2902
ALM2904	ALM301A	ALM307	ALM308	ALM308A
ALM318	ALM324	ALM3302	ALM339	ALM358
ALM358A	ALM725	ALM741	ALM747	ALM747C
AMC1458	AMC1536	AMC1741	AMC1747	ANE5534P
ANJM4558	ANJM4559	ANJM4560	AOP04	AOP07
AOP14	AOP15B	AOP16B	AT094CNS	ATL071C

Table B-12: Behavioral Model Names *(Continued)*

ATL072C	ATL074C	ATL081C	ATL082C	ATL084C
ATL092CP	ATL094CN	AUPC1251	AUPC358	GA201
RCFILT	TLINE			

Bipolar Transistor Models

Required element syntax: Xyyyy coll base emit modelname

- Search path: *$installdir/parts/bjt*
- Optional parameters: betaf=value, tauf=value

Table B-13: Bipolar Transistor Model Names

T2N1132A	T2N2102	T2N2219A	T2N2222	T2N2222A
T2N2369	T2N2369A	T2N2501	T2N2605	T2N2642
T2N2857	T2N2894	T2N2904	T2N2904A	T2N2905
T2N2905A	T2N2906	T2N2907	T2N2907A	T2N2945A
T2N3013	T2N3227	T2N3250	T2N3250A	T2N3251
T2N3251A	T2N3467	T2N3501	T2N3546	T2N3637
T2N3742	T2N3743	T2N3866	T2N3904	T2N3906
T2N3946	T2N3947	T2N3962	T2N4261	T2N4449
T2N5058	T2N5059	T2N5179	T2N6341	T2N6438
T2N706	T2N708	T2N869	T2N869A	T2N918
T2N930	T2SA1015	T2SA950	T2SA965	T2SA970
T2SC1815	T2SC1923	T2SC2120	T2SC2235	T2SC2669
TMPS6595	TNE741	TNE901		

Burr-Brown Devices

Search path: *$installdir/parts/burr_brn*

Table B-14: Burr-Brown Model Names

INA101	INA101E	INA102	INA102E	INA103
INA103E	INA105	INA105E	INA106	INA106E
INA110	INA110E	INA117	INA117E	INA120
INA120E	ISO120X	ISO121X	OPA101	OPA1013
OPA1013E	OPA101E	OPA102	OPA102E	OPA111
OPA111E	OPA121	OPA121E	OPA128	OPA128E
OPA177	OPA177E	OPA2107	OPA2107E	OPA2111
OPA2111E	OPA2541	OPA2541E	OPA2604	OPA2604E
OPA27	OPA27E	OPA27H	OPA27HE	OPA37
OPA37E	OPA404	OPA404E	OPA445	OPA445E
OPA501	OPA501E	OPA511	OPA511E	OPA512
OPA512E	OPA541	OPA541E	OPA602	OPA602E
OPA603X	OPA606	OPA606E	OPA620	OPA620E
OPA620X	OPA621	OPA621E	OPA621X	OPA627
OPA627E	OPA637	OPA637E	RCV420X	UAF42
UAF42E				

Comlinear Device Models

Search path: *$installdir/parts/comline*

Table B-15: Comlinear Model Names

CLC109	CLC111	**Table B-16: cl c400**	CLC401	CLC402
CLC404	CLC406	CLC409	CLC410	CLC414
CLC415	CLC420	CLC425	CLC426	CLC428
CLC430	CLC431	CLC432	CLC501	CLC502
CLC505	CLC520	CLC522	CLC532	

Diode Models

Required element syntax: Xyyyyy anode cathode modelname

- Search path: *$installdir/parts/dio*
- Optional parameters: isat=value, tt=value

Table B-17: Diode Model Names (Sheet 1 of 3)

D12BG11	D12BH11	D12DG11	D12DH11	D12FG11
D12FH11	D12GG11	D12GH11	D12JG11	D12JH11
D1N3016	D1N3017	D1N3018	D1N3019	D1N3020
D1N3021	D1N3022	D1N3023	D1N3024	D1N3025
D1N3026	D1N3027	D1N3028	D1N3029	D1N3030
D1N3031	D1N3032	D1N3033	D1N3034	D1N3035
D1N3036	D1N3037	D1N3038	D1N3039	D1N3040
D1N3041	D1N3042	D1N3043	D1N3044	D1N3045
D1N3046	D1N3047	D1N3048	D1N3049	D1N3050
D1N3051	D1N3821	D1N3822	D1N3823	D1N3824
D1N3825	D1N3826	D1N3827	D1N3828	D1N3829
D1N3830	D1N4001	D1N4002	D1N4003	D1N4004
D1N4005	D1N4006	D1N4007	D1N4148	D1N4149

Table B-17: Diode Model Names (Sheet 2 of 3)

D1N4150	D1N4370	D1N4371	D1N4372	D1N4446
D1N4447	D1N4448	D1N4449	D1N4728	D1N4729
D1N4730	D1N4731	D1N4732	D1N4733	D1N4734
D1N4735	D1N4736	D1N4737	D1N4738	D1N4739
D1N4740	D1N4741	D1N4742	D1N4743	D1N4744
D1N4745	D1N4746	D1N4747	D1N4748	D1N4749
D1N4750	D1N4751	D1N4752	D1N4753	D1N4754
D1N4755	D1N4756	D1N4757	D1N4758	D1N4759
D1N4760	D1N4761	D1N4762	D1N4763	D1N4764
D1N5221	D1N5222	D1N5223	D1N5224	D1N5225
D1N5226	D1N5227	D1N5228	D1N5229	D1N5230
D1N5231	D1N5232	D1N5233	D1N5234	D1N5235
D1N5236	D1N5237	D1N5238	D1N5239	D1N5240
D1N5241	D1N5242	D1N5243	D1N5244	D1N5245
D1N5246	D1N5247	D1N5248	D1N5249	D1N5250
D1N5251	D1N5252	D1N5253	D1N5254	D1N5255
D1N5256	D1N5257	D1N5258	D1N5259	D1N5260
D1N5261	D1N5262	D1N5263	D1N5264	D1N5265
D1N5266	D1N5267	D1N5268	D1N5269	D1N5270
D1N5271	D1N5272	D1N5333	D1N5334	D1N5335
D1N5336	D1N5337	D1N5338	D1N5339	D1N5340
D1N5341	D1N5342	D1N5343	D1N5344	D1N5345
D1N5346	D1N5347	D1N5348	D1N5349	D1N5350
D1N5351	D1N5352	D1N5353	D1N5354	D1N5355
D1N5356	D1N5357	D1N5358	D1N5359	D1N5360
D1N5361	D1N5362	D1N5363	D1N5364	D1N5365
D1N5366	D1N5367	D1N5368	D1N5369	D1N5370
D1N5371	D1N5372	D1N5373	D1N5374	D1N5375

Table B-17: Diode Model Names (Sheet 3 of 3)

D1N5376	D1N5377	D1N5378	D1N5379	D1N5380
D1N5381	D1N5382	D1N5383	D1N5384	D1N5385
D1N5386	D1N5387	D1N5388	D1N5817	D1N5818
D1N5819	D1N5913	D1N5914	D1N5915	D1N5916
D1N5917	D1N5918	D1N5919	D1N5920	D1N5921
D1N5922	D1N5923	D1N5924	D1N5925	D1N5926
D1N5927	D1N5928	D1N5929	D1N5930	D1N5931
D1N5932	D1N5933	D1N5934	D1N5935	D1N5936
D1N5937	D1N5938	D1N5939	D1N5940	D1N5941
D1N5942	D1N5943	D1N5944	D1N5945	D1N5946
D1N5947	D1N5948	D1N5949	D1N5950	D1N5951
D1N5952	D1N5953	D1N5954	D1N5955	D1N5956
D1N746	D1N747	D1N748	D1N749	D1N750
D1N751	D1N752	D1N753	D1N754	D1N755
D1N756	D1N757	D1N758	D1N759	D1N914
D1N957	D1N958	D1N959	D1N960	D1N961
D1N962	D1N963	D1N964	D1N965	D1N966
D1N967	D1N968	D1N969	D1N970	D1N971
D1N972	D1N973	D1N974	D1N975	D1N976
D1N977	D1N978	D1N979	D1N980	D1N981
D1N982	D1N983	D1N984	D1N985	D1N986
D1S1585	D1S1586	D1S1587	D1S1588	D1SV147
D1SV149	DMBR115P	DMBR120P	DMBR130P	DMBR140P
DSK4A3				

FET Models

Required element syntax: Xyyyy drain gate source modelname

- Search path: *$installdir/parts/fet*
- Optional parameters: vt = value, betaf = value

Table B-18: FET Model Names

J108	J109	J110	J111	J112
J113	J2N3330	J2N3460	J2N3824	J2N4391
J2N4392	J2N4393	J2N4856	J2N4857	J2N5457
J2N5458	J2N5459	J2N5460	J2N5461	J2N5462
J2N5463	J2N5465	J309	J511	J557
JSJ74	JSK170	M2N6755	M2N6756	M2N6757
M2N6758	M2N6759	M2N6760	M2N6761	M2N6762
M2N6763	M2N6764	M2N6765	M2N6766	M2N6767
M2N6768	M2N6769	M2N6770	M2N6787	M2N6788
M2N6789	M2N6790	M2N6791	M2N6792	M2N6793
M2N6794	M2N6795	M2N6796	M2N6797	M2N6798
M2N6799	M2N6800	M2N6801	M2N6802	MBUZ10
MBUZ20	MBUZ23	MBUZ24	MBUZ32	MBUZ35
MBUZ36	MBUZ42	MBUZ45	MBUZ46	MBUZ60
MBUZ63	MBUZ64	MBUZ71	MBUZ72A	MBUZ74
MBUZ76	MIRF120	MIRF121	MIRF122	MIRF123
MIRF130	MIRF131	MIRF132	MIRF133	MIRF140
MIRF141	MIRF142	MIRF143	MIRF150	MIRF151
MIRF152	MIRF153	MIRF220	MIRF221	MIRF222
MIRF223	MIRF230	MIRF231	MIRF232	MIRF233
MIRF240	MIRF241	MIRF242	MIRF243	MIRF250
MIRF251	MIRF252	MIRF253	MIRF320	MIRF321
MIRF322	MIRF323	MIRF330	MIRF331	MIRF332

Table B-18: FET Model Names *(Continued)*

MIRF333	MIRF340	MIRF341	MIRF342	MIRF343
MIRF350	MIRF351	MIRF352	MIRF353	MIRF420
MIRF421	MIRF422	MIRF423	MIRF430	MIRF431
MIRF432	MIRF433	MIRF440	MIRF441	MIRF442
MIRF443	MIRF450	MIRF451	MIRF452	MIRF453
MIRF510	MIRF511	MIRF512	MIRF513	MIRF520
MIRF521	MIRF522	MIRF523	MIRF530	MIRF531
MIRF532	MIRF533	MIRF540	MIRF541	MIRF542
MIRF543	MIRF610	MIRF611	MIRF612	MIRF613
MIRF620	MIRF621	MIRF622	MIRF623	MIRF630
MIRF631	MIRF632	MIRF633	MIRF640	MIRF641
MIRF642	MIRF643	MIRF710	MIRF711	MIRF712
MIRF713	MIRF720	MIRF721	MIRF722	MIRF723
MIRF730	MIRF731	MIRF732	MIRF733	MIRF740
MIRF741	MIRF742	MIRF743	MIRF810	MIRF811
MIRF812	MIRF813	MIRF820	MIRF821	MIRF822
MIRF823	MIRF830	MIRF831	MIRF832	MIRF833
MIRF840	MIRF841	MIRF842	MIRF843	MIRF9020
MIRFF110	MIRFF111	MIRFF112	MIRFF113	MIRFF120
MIRFF121	MIRFF122	MIRFF123	MIRFF130	MIRFF131
MIRFF132	MIRFF133	MIRFF210	MIRFF211	MIRFF212
MIRFF213	MIRFF220	MIRFF221	MIRFF222	MIRFF223
MIRFF230	MIRFF231	MIRFF232	MIRFF233	MIRFF310
MIRFF311	MIRFF312	MIRFF313	MIRFF320	MIRFF321
MIRFF322	MIRFF323	MIRFF330	MIRFF331	MIRFF332
MIRFF333	MIRFF430	MIRFF431	MIRFF432	MIRFF433

Linear Technology Device Models

Search path: *$installdir/parts/lin_tech*

Table B-19: Linear Technology Model Names

113090	LF155	LF155A	LF156	LF156A
LF355	LF355A	LF356	LF356A	LF412
LF412A	LM101A	LM107	LM108	LM108A
LM10C	LM118	LM301A	LM307	LM308
LM308A	LM318	LT1001	LT1001A	LT1006
LT1006A	LT1006S8	LT1007	LT1007A	LT1008
LT1012	LT1012A	LT1012D	LT1012S8	LT1013
LT1013A	LT1013D	LT1022	LT1022A	LT1028
LT1028A	LT1037	LT1037A	LT1055	LT1055A
LT1055S8	LT1056	LT1056A	LT1056S8	LT1057
LT1057A	LT1057S	LT1078	LT1078A	LT1097
LT1101	LT1115	LT1122	LT1178	LT1178A
LT118A	LT1220	LTC1049	LTC1050	LTC1050A
LTC1051	LTC1052	LTC1150	OP05	OP05A
OP05C	OP05E	OP07	OP07A	OP07C
OP07E	OP15A	OP15B	OP15C	OP16A
OP16B	OP16C	OP215A	OP215C	OP27A
OP27C	OP37A	OP37C	OP97	

Intel PCI Speedway Models

Search path: *$installdir/parts/pci*

Table B-20: Intel PCI Speedway Model Names

PCI_II_B	PCI_II_T	PCI_II_W	PCI_IN_W	TRACE

Signetics Device Models

Search path: *$installdir/parts/signet*

Table B-21: Signetics Model Names

AC109EQ	AC240EQ	AC833OD	AC86EQ	ACTINPUT
CL10X10	CL30X10	DIP14	DIP16	DIP20
DIP24	DIP28	DIP8	DIP80001	SO16
SO20	SO24	SO28	SO8	

Texas Instruments Device Models

Search path: *$installdir/parts/ti*

Table B-22: TI Model Names

ICL7652	LF347	LF351	LF353	LF411C
LF412C	LM101A	LM107	LM301A	LM307
LM308	LM318	LM324	LM348	LM358
LT1001	LT1008	LT1012	LT1013	LT1028
LT1037	LTC1052	MC1458	MC3403	NE5534
OP-07C	OP-07D	OP-07E	OP-27C	OP-27E
OP-27G	OP-37A	RC4136	RC4558	RC4559
TL022C	TL031	TL032	TL034	TL044C
TL051	TL052	TL054	TL060	TL061
TL062	TL064	TL066	TL070	TL071
TL072	TL074	TL075	TL080	TL081
TL082	TL083	TL084	TL085	TL087
TL088	TL136	TL287	TL288	TL321
TL322	TLC1078	TLC1079	TLC2201	TLC251H
TLC251L	TLC251M	TLC252C	TLC254C	TLC25L2C
TLC25L4C	TLC25M2C	TLC25M4C	TLC2652	TLC2654

Table B-22: TI Model Names *(Continued)*

ICL7652	LF347	LF351	LF353	LF411C
TLC271H	TLC271L	TLC271M	TLC272	TLC274
TLC277	TLC279	TLC27L2	TLC27L4	TLC27L7
TLC27L9	TLC27M2	TLC27M4	TLC27M7	TLC27M9
TLE2021	TLE2022	TLE2024	TLE2061	TLE2062
TLE2064	TLE2161	UA741	UA747	UA748

Transmission Line Models

Search path: *$installdir/parts/tline*

Table B-23: Transmission Line Model Names

RCFILT	RG11_U	RG11A_U	RG15_U	RG180B_U
RG188A_U	RG53_U	RG54A_U	RG58A_U	RG58C_U
RG59B_U	RG62_U	RG62B_U	RG71_U	RG71B_U
RG9_U	RG9B_U	TW_SH_U	TW_UN_U	

Xilinx Device Models

Search path: *$installdir/parts/xilinx*

Table B-24: Xilinx Model Names

FOUTPUT	OUTPUT	XC7236A	XC7272A	XC7336A
XIL_IOB	XIL_IOB4			

Avant!

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