Data Converter Terminology

1. Introduction

This application note describes a number of parameters related to "binary" and "linear" data converters, as specified in Atmel's datasheets, and discusses to what point they can be tested. "Binary" means that the converter uses all binary code combinations. "Linear" means that there is no non-linearity other than that of quantization: all steps of the related ideal converters are equal in size. The following definitions assume that converters operate over their entire full-scale range, using a straight binary code format. Nevertheless, they can be easily adapted for converters operating over a limited range, or using another binary code format. In particular, binary-coded decimal (BCD) converters and floating-point (FP) converters are not considered in this document, because the first are “non-binary" converters, and the later are “non-linear" converters.

Cell-based Application Specific Products

Application Note

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2. Definition of Terms

2.1 Acronyms

A list of acronyms used in this document is detailed below.

ADC	Analog-to-Digital Converter
A2D	see ADC
A/D	see ADC
ATE	Automatic Test Equipment
BSL	Best-fit Straight Line
DAC	Digital-to-Analog Converter
DFT	Discrete Fourier Transform
DLE	Differential Linearity Error
DNL	Differential Non-linearity (a.k.a. DLE: Differential Linearity Error)
DUT	Device Under Test
D2A	see DAC
D/A	see DAC
dBc	dB with respect to the Carrier
dBfs	dB with respect to the Full-Scale
ENOB	Effective Number of Bits (a.k.a. Equivalent Number of Bits)
ESL	End-point Straight Line
FFT	Fast Fourier Transform
FSR	Full-scale Range
ILE	Integral Linearity Error
INL	Integral Non-linearity (a.k.a. ILE: Integral Linearity Error)
ISL	Ideal Straight Line
LSB	Least Significant Bit
NFSE	Negative Full-scale Error
PFSE	Positive Full-scale Error
RMS	Root-Mean-Square
RSL	Reference Straight Line
SFDR	Spurious-Free Dynamic Range
SINAD	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
S/N	see SNR
SQER	Signal-to-Quantization Error Ratio
THD	Total Harmonic Distortion
UPD	Uniform Probability Density
UTP	Unit Test Period

2.2 Number of Bits

The Number of Bits, N, is the logarithm to the base 2 of the number of code levels. Accordingly, let N be the converter's resolution. N equals 3 in most examples.

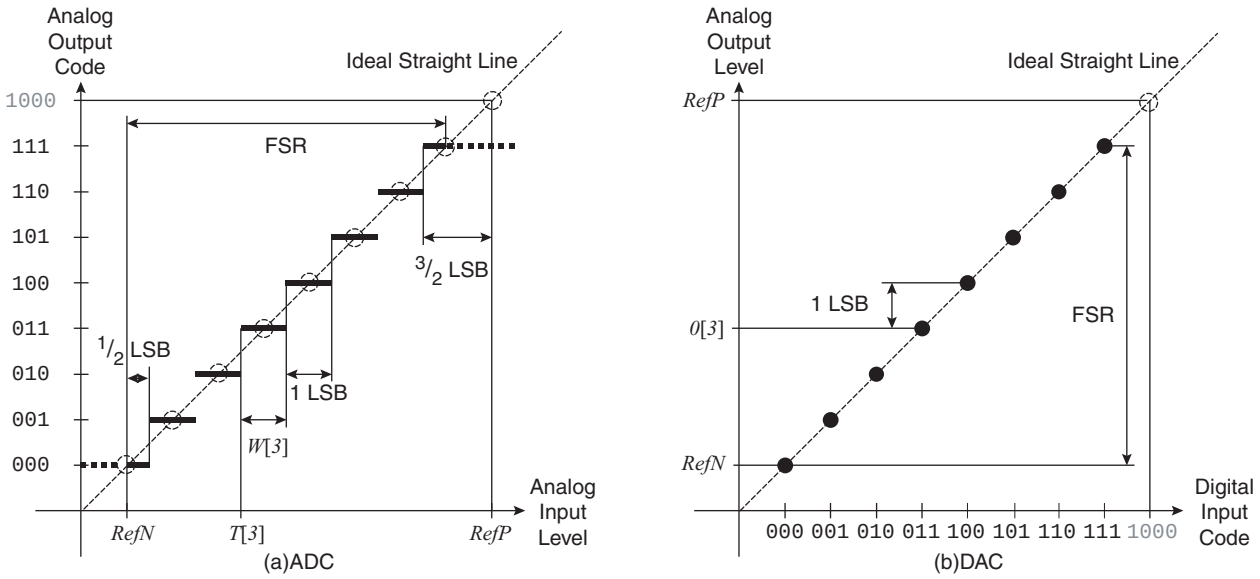
2.3 Ideal Characteristics

The ideal characteristics of a data converter are described in the sections that follow.

2.3.1 Ideal Transfer Functions

Ideal transfer functions are shown below in Figure 2-1.

Figure 2-1. Ideal Transfer Functions



2.3.2 Ideal ADC Transition Levels

There are an infinite number of possible states for the analog input of an ADC, whereas there are a limited number of digital output codes determined by the resolution of the converter. Levels between two adjacent transition levels are translated to the same code. The ideal transition level $T[i]$ of code i is defined as the analog input level, for which the output code switches from code i – 1 to code i.

2.3.3 Ideal Least Significant Bit

The ideal least significant bit (LSB) is the size of a code step in the analog domain. For an ADC, the code width of code i is defined as $W[i] = T[i+1] - T[i]$, which is ideally the same for all codes and yields one LSB. For a DAC, one LSB is the difference between analog output levels related to two adjacent input codes:

$$LSB_{ADC} = \frac{T[2^N - 1] - T[1]}{2^N - 1} = \frac{RefP - RefN}{2^N}$$

$$LSB_{DAC} = \frac{O[2^N - 1] - O[0]}{2^N - 1} = \frac{RefP - RefN}{2^N}$$

2.3.4 Ideal Straight Line

The ideal straight line (ISL) is the straight line, which passes through ($RefN$, 0) and ($RefP$, 2^N), and fully characterizes the ideal converter. In particular, it crosses the ADC

ideal transfer curve at midstep points $\left(\frac{T[i]+T[i+1]}{2}, i\right)$ for a given digital output code i in

[1; 2^N –2]. For a DAC, all points of the ideal transfer function are on the ISL. One can also notice, that, once symmetry with respect to the ISL has been applied on the ADC transfer function, mid-step points feature the corresponding DAC transfer curve. Midstep points are shown as dashed circles in the illustrations. The ISL can be mathematically defined as follows:

$$ISL_{ADC}(in) = \frac{in - RefN}{LSB}$$

$$ISL_{DAC}(i) = RefN + i \times LSB$$

2.3.5 Ideal Full-scale Range

For an ADC, the ideal full-scale range (FSR) is the difference between the analog input levels corresponding to the intersections at end codes of the ideal transfer curve and the ISL. For a DAC, it is the difference between analog outputs corresponding to end codes:

$$FSR = (2^N - 1) \times LSB = \frac{2^N - 1}{2^N} \times (RefP - RefN) = RefP - RefN - 1LSB$$

A full-scale signal extends from $RefN$ to $RefP$ – 1 LSB on the analog axis.

2.3.6 ADC Clipping Levels

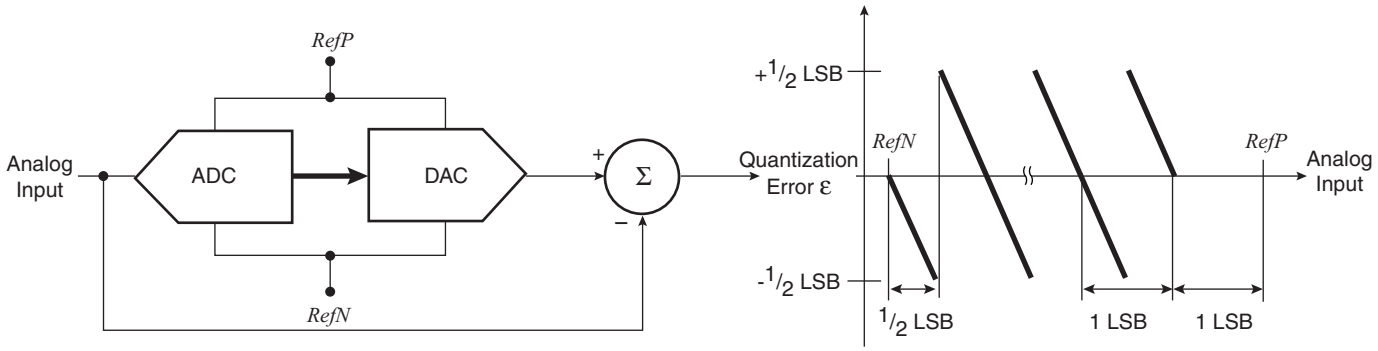
The two end steps have no outer bounds, of course, and so do not actually have centers. To analyze the ADC behavior however, centers for all code steps can be assumed by adopting the AT&T® convention and accordingly assign virtual edges (i.e. hypothetical transition levels, placed where edges would exist if the transfer curve were to continue). These virtual edges are the clipping levels of the ADC.

They are located at $T[0] = RefN - \frac{1}{2}LSB$ and $T[2^N] = RefP - \frac{1}{2}LSB$

2.3.7 ADC Inherent Quantization Error

The analog input range is quantized by partitioning the continuum into 2^N discrete ranges. Hence, some information is lost during the conversion process and, due to this quantization, quantization noise is introduced into the input signal. The difference (error) between the actual input and its digital form is called quantization error. It can be seen by looking at the output of the system, as shown in Figure 2-2 below, provided that both the ADC and the DAC share the same references and have the same resolution.

Figure 2-2. ADC Quantization Error



The RMS uncertainty of the quantization, as seen by an observer looking back into the output of the system, is the RMS amplitude of the “saw tooth” as shown above in Figure 2-2. This amplitude is also the RMS value of the error introduced into a random input signal, which would be transmitted through the system, because the quantization error has a uniform probability density (UPD) function if the input signal is assumed to be random. Since the quantization error is a periodic function of the analog input, the mean square of the quantization error over an integral number of code steps is the same as the mean square of the error over one step. If Q features a quantum (LSB) of the analog continuum, the RMS level of the quantization error E is:

$$E_{RMS} = \sqrt{\frac{1}{Q}\int_{-Q/2}^{+Q/2}(-l)^2 dl} = \frac{Q}{\sqrt{12}}$$

Although it is not featured beyond the FSR on the drawing shown in Figure 2-2 on page 5, the saw tooth error function can extend to the clipping levels. The clipping levels are the extreme levels wherein the quantization error remains within ±½ LSB. Therefrom, accordingly apply a hypothetical clipping sinusoid to the ideal ADC input (i.e. the sinusoid peaks just reach the clipping levels): its peak amplitude is hence $A_{CS} = 2^{N-1}Q$.

The sinusoid looks like:

$$S(t) = \frac{RefN + RefP - 1LSB}{2} + 2^{N-1}Q\sin\omega t$$

The AC RMS level of this signal is:

$$S_{RMS} = \sqrt{\frac{1}{2\pi}\int_{0}^{2\pi/\omega}(2^{N-1}Q\sin t)^2 dt} = \frac{2^N Q}{\sqrt{8}}$$

Although the input sine wave is not a UPD function, the UPD assumption is still valid since it is locally applied over each code bin. The deviation from a UPD over each code bin is very small, so the errors in using sine waves to approximate UPD inputs are negligible. Dividing the signal RMS level into the RMS quantization error, and expressing this ratio in dB, a signal-to-quantization error ratio, relative to a clipping sinusoid is obtained:

$$SQER_{CS} = 20\log_{10}\left(\frac{S_{RMS}}{E_{RMS}}\right) = 20\log_{10}\left(\frac{2^N Q\sqrt{12}}{Q\sqrt{8}}\right) = 20\log_{10}(2^N\sqrt{3/2})$$

$$SQER_{CS} = N\cdot 20\log_{10}(2) + 10\log_{10}(1{,}5) \approx 6{,}02N + 1{,}76[\text{dBc}]$$

This is neither the signal-to-noise ratio of the ADC, nor a harmonic distortion, but it is the amount of ADC errors relative to the level of a hypothetical clipping sinusoid. The formula applies exclusively to linear conversion.

If we had chosen a sinusoid of smaller amplitude A:

$$SQER_A = 20\log_{10}\left(\frac{A\sqrt{12}}{Q\sqrt{2}}\right) = 20\log_{10}\left(\frac{2^N A\sqrt{6}}{2\cdot 2^{N-1}Q}\right) = 20\log_{10}\left(\frac{2^N A\sqrt{1{,}5}}{A_{CS}}\right)$$

$$SQER_{CS} \approx 6{,}02N + 1{,}76 - 20\log_{10}\left(\frac{A_{CS}}{A}\right)[\text{dBc}]$$

In particular, a full-scale sinusoid has the same $SQER$ as a clipping sinusoid, because the peak-to-peak amplitude of the full-scale sinusoid is only one LSB less than that of the clipping sinusoid:

$$SQER_{FS} = SQER_{CS} - 20\log_{10}\left(1 - \frac{1}{2^N}\right) \approx SQER_{CS} \text{ when } N \text{ is large enough.}$$

When the input is randomly sampled by the ADC, quantization error is white noise, and will show up as an elevated noise floor on the power spectrum during frequency analysis. That is why the quantization error is also known as quantization noise. In linear ADCs, the power of the error is essentially independent of the signal level, as long as quantization is actively taking place (i.e. so long as a signal is applied that is at least several LSBs in amplitude). It can therefore be used as an approximate signal-to-noise and distortion ratio (SINAD), if it is adjusted to reflect the actual power level of the test signal, which may not be a sinusoid, or may be under the clipping levels. The relationship between a measured SINAD and an effective or equivalent number of bits (ENOB) is discussed in the section, "Transmission Parameters" on page 14, which deals with transmission parameters of real converters.

2.4 Parameters of Real Converters

Depending on the intended converter application, only some of the parameters described hereafter are relevant. This particular subset is used both to specify and test the converter.

2.4.1 Intrinsic Parameters

Intrinsic parameters characterize the converter itself, indicating some ideally invariant circuit property; existing internally, independent of the input signal.

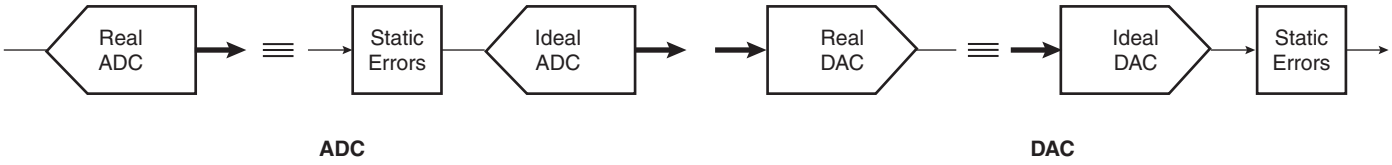
2.4.1.1 Static Error Models

Static errors, which affect the accuracy of converters when they are converting static (DC) signals, can be completely described by just four terms:

- offset and gain (linear errors)
- integral non-linearity and differential non-linearity (non-linear errors)

Since these errors occur in analog stages, real converters with static errors can be modeled as follows:

Figure 2-3. Static Error Models

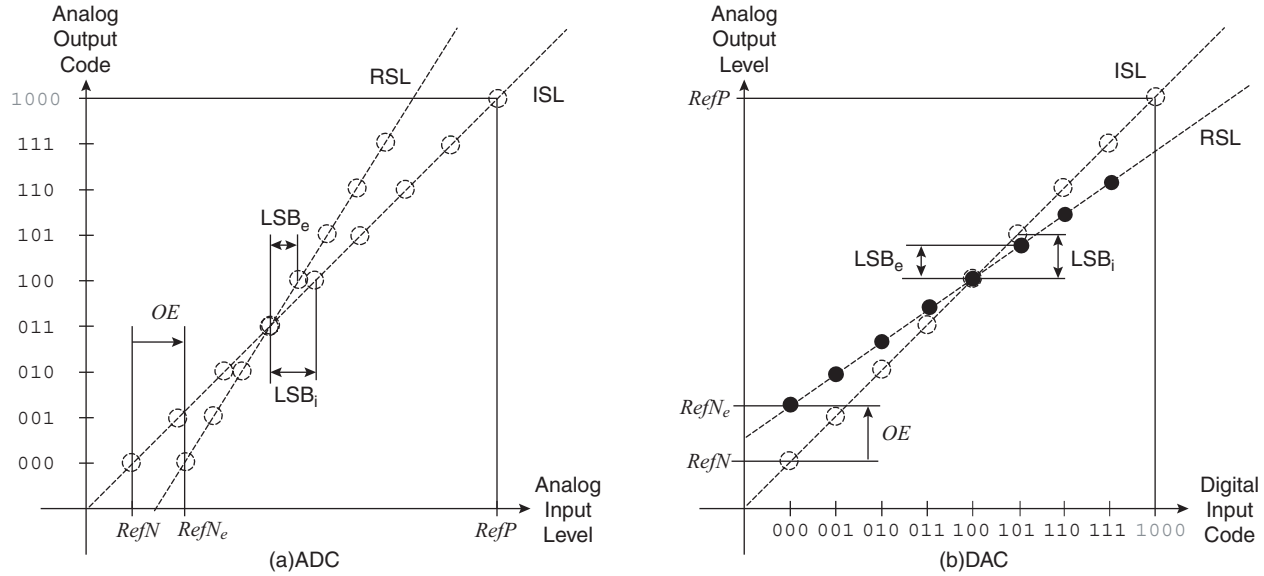


Thus, static errors appear as displacements on the analog axis from the ideal locations. Each error can be expressed in LSB units, or as a percentage of the FSR, or in the unit of the analog domain (usually Volts or Amperes). For instance, ½ LSB error corresponds to roughly 0.05% FSR for a 10-bit converter.

2.4.1.2 Linear Errors

Offset error is a uniform displacement of all points, while improper gain appears as analog displacements proportional to digital codes. Consider an actual converter, which has no other static error but linear ones. The points on the ISL of the corresponding ideal converter are moved to new locations by a linear operation, and thus build up a new reference straight line (RSL), which can be fully characterized by $RefN_e$ and LSB_e (the e index stands for "effective" or "equivalent").

Figure 2-4. Linear Errors



$$RSL_{ADC}(in) = \frac{in - RefN_e}{LSB_e} \qquad RSL_{DAC}(i) = RefN_e + i \times LSB_e$$

The question arises as to what happens when the converter is also affected by non-linear errors? How can an observer, looking back at the output of such an actual converter, determine the RSL, in order to retrieve $RefN_e$ and LSB_e? In fact, the choice of the RSL depends on the converter's architecture and on its typical usage. Refer to, "Choice of the Reference Straight Line" on page 11.

- Effective LSB

The effective LSB is the analog step size on the RSL for a unity increment along the digital axis.

- Offset Error

Once the RSL has been chosen, the offset error (OE) is always defined as the analog distance between the RSL and the ISL at code 0, that is to say:

$$OE = RefN_e - RefN$$

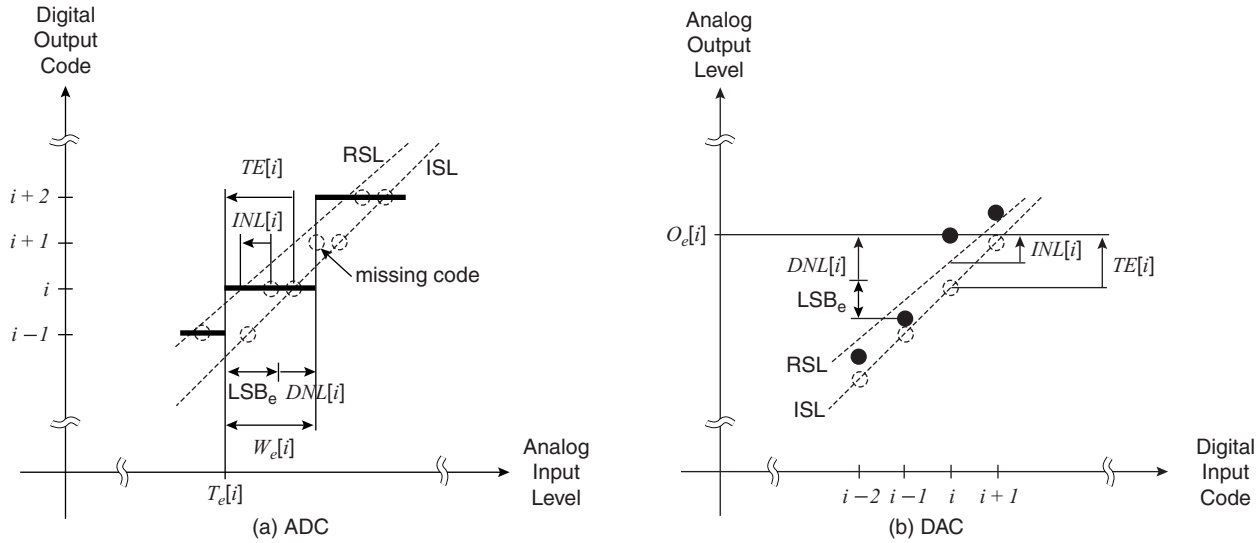
- Gain Error

Since the definition of gain error (GE) depends on the chosen RSL, it is specified in further paragraphs. In any case, it is a function of the ratio between the slope of the RSL and the slope of the ISL. It is likewise a function of the ratio between LSB_e and LSB_i (the ideal LSB).

2.4.1.3 *Non-linear Errors*

Non-linear errors should be evaluated once gain and offset errors have been canceled by trimming (if possible), or compensated for (nullified) by mathematical operations, so that they can be distinguished from linear errors. Thus, a three step process would normally be required to measure the non-linear errors: first of all determine the linear errors, then compensate for these errors, and finally measure non-linear errors. There is fortunately an equivalent one step process: simply measuring analog distances with respect to the RSL, since the actual compensation for linear errors would transform the RSL into the ISL. Hence, measuring $xLSB_e$ error with respect to the RSL without compensation is the same as measuring $xLSB_i$ with respect to the ISL. That is why the preferred unit of non-linear errors is the LSB (without specifying i "ideal" or e "effective").

Figure 2-5. Non-linear Errors



- Differential Non-linearity

The differential non-linearity (DNL) is a measure of the irregularity, or non-uniformity, in the size of analog steps. It is defined as the difference between an actual analog step size and one LSB_e, normalized to one LSB_e:

$$DNL_{ADC}[i] = \frac{T_e[i+1] - T_e[i]}{LSB_e} - 1 = \frac{W_e[i]}{LSB_e} - 1\ [LSB]$$

$$DNL_{DAC}[i] = \frac{O_e[i] - O_e[i-1]}{LSB_e} - 1\ [LSB]$$

- ADC Missing Code

Since $T[i+1] \geq T[i]$ by definition, the DNL of an ADC is thus always greater than or equal to –1.

$$\text{No missing code in ADC} \Leftrightarrow DNL > -1LSB$$

Note: Some standards (IEEE Std 1057-94 (R2001), IEEE Std 1241-2000) require the DNL to be greater than -0.9 LSB.

- ADC Hysteresis

If the transition level between codes i and $i-1$ is not the same as the transition level between codes $i-1$ and i, there is hysteresis in the transfer function. According to negative or positive input slope, the ADC has two different transfer functions in the case of hysteresis.

- Monotonicity

A converter is monotonic if its output either increases or remains constant as the input increases:

$$\text{Monotonic DAC} \Leftrightarrow DNL > -1LSB$$

Note: Due to the definition of transition levels, ADCs are assumed to be monotonic in the model used in this Application Note.

- Superposition Error

Superposition refers to the fact, that ADC transition levels and DAC output levels can be a linear sum of many components, which are ideally independent of each other. However, complete independence is impossible to achieve in real designs, so the contribution of a bit in the converter's analog levels depends to some extent on what other bits are activated. Hence, superposition error is the result of non-constant bit weights, and appears as part of the INL, the next defined parameter.

- Integral Non-linearity

Integral non-linearity (INL) is defined as the analog distance of a point on the actual transfer function (a midstep point for an ADC) from the RSL, normalized to one LSB_e:

$$INL_{ADC}[i] = \frac{\frac{T_e[i+1] + T_e[i]}{2} - RSL[i]}{LSBe}\ [\text{LSB}]$$

$$INL_{DAC}[i] = \frac{O_e[i] - RSL[i]}{LSB_e}\ [\text{LSB}]$$

Integral non-linearity is aptly named, because the INL of a given code can be obtained by integrating the DNL from the lowest code up to the code in question:

$$INL[i] = INL[0] + 0{,}5 \times DNL[i] + \sum_{k=1}^{i-1} DNL[k] \text{ [LSB]}$$

$$= INL[i-1] + \frac{DNL[i] + DNL[i-1]}{2}$$

If $INL[2^N - 1] = INL[0]$, the sum of DNL is zero, as well as the average. This is especially the case when the RSL passes through end-points.

2.4.1.4 *Other Static Parameters*

- Negative Full-scale Error

For an ADC, the negative full-scale error (NFSE) is the deviation from $RefN$ of the actual transition level of code 1 minus half an effective LSB. For a DAC, it is the deviation of the actual analog output related to code 0 from $RefN$. When the RSL passes through the actual transfer point relative to code 0, the NFSE is the same as the offset error.

$$NFSE_{ADC} = \frac{T_e[1] - \frac{1}{2}LSB_e - RefN}{LSB_i} \text{ [LSB]}$$

$$NFSE_{DAC} = \frac{O_e[0] - RefN}{LSB_i} \text{ [LSB]}$$

- Positive Full-scale Error

For an ADC, the positive full-scale error (PFSE) is the deviation from $RefP$ minus one ideal LSB of the actual transition level of code 2^N -1 plus half an effective LSB. For a DAC, it is the deviation of the actual analog output related to code 2^N -1 from $RefP$ minus one ideal LSB:

$$PFSE_{ADC} = \frac{T_e[2^N - 1] + \frac{1}{2}LSB_e - (RefP - LSB_i)}{LSB_i} \text{ [LSB]}$$

$$PFSE_{DAC} = \frac{O_e[2^N - 1] - (RefP - LSB_i)}{LSB_i} \text{ [LSB]}$$

- Total Error

The total error (TE), a.k.a. absolute accuracy error or maximum static error, is the maximum deviation of the actual transfer function from the ISL. Hence, it encompasses gain, offset, and integral non-linearity errors, as well as the inherent quantization error for an ADC (the total error

of an ideal ADC is thus ±½ LSB). It is expressed in ideal LSB:

$$\left|TE_{ADC}[i]\right| = \frac{max(\left|T_e[i+1]-ISL[i]\right|,\left|T_e[i]-ISL[i]\right|)}{LSB_i} \text{ [LSB]}$$

$$TE_{DAC}[i] = \frac{O_e[i]-ISL[i]}{LSB_i} \text{ [LSB]}$$

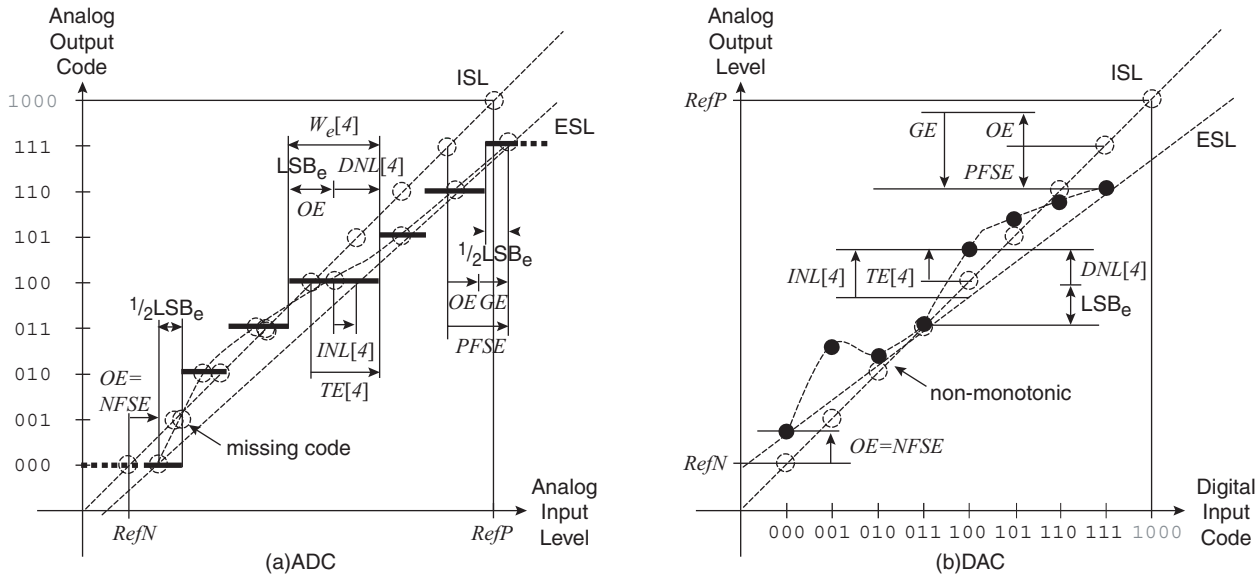
2.4.1.5 *Choice of the Reference Straight Line*

The two most significant reference straight lines (RSL) are the end-point straight line (ESL) and the best-fit straight line (BSL). The ESL is aptly named, because it passes through actual end-points, whereas the BSL is defined so as to minimize the mean square of INL values (i.e. it is the simple linear regression of the actual transfer points).

- End-point Straight Line

Static errors used to be (and are often still) expressed in relation to the ESL, because they can be checked quite directly, insofar as the ESL is easy to find, especially for a DAC. For an ADC, it is a bit trickier, because it passes through the virtual midstep points related to end codes, that is to say the points which are used to compute the NFSE and the PFSE. But both parameters call for the value of one effective LSB, which depends on the slope of the RSL, which is precisely the (yet unknown) ESL. The solution consists of first determining the effective LSB, by using the first formula described in the section, "Ideal Least Significant Bit" on page 3.

Figure 2-6. End-point Static Errors



When the RSL passes through the end-points, the gain error (GE) is defined as the analog difference between the actual end-point and the ideal end-point (after the offset error has been corrected to zero):

$$GE_{ADC} = PFSE - OE = T_e[2^N - 1] + \frac{1}{2}LSB_e - (RefP - LSB_i) - \left(T_e[1] - \frac{1}{2}LSB_e - RefN\right)$$

$$= T_e[2^N - 1] - T_e[1] + LSB_e - (RefpP - RefN - LSB_i) = FSR_e - FSR_i$$

$$GE_{DAC} = PFSE - OE = O_e[2^N - 1] - (RefP - LSB_i) - (O_e[0] - RefN)$$

$$= O_e[2^N - 1] - O_e[0] - (RefP - RefN - LSB_i) = FSR_e - FSR_i$$

$$GE = \frac{FSR_e - FSR_i}{LSB_i} = (2^N - 1) \times \left(\frac{LSB_e}{LSB_i} - 1\right) \text{ [LSB]}$$

Therefore, GE is the sum over the FSR of the same average error for each step, effectively $LSB_e - LSB_i$.

- Best-fit Straight Line

Although the ESL is easy to use, there may be drawbacks in specifying errors with respect to this line.

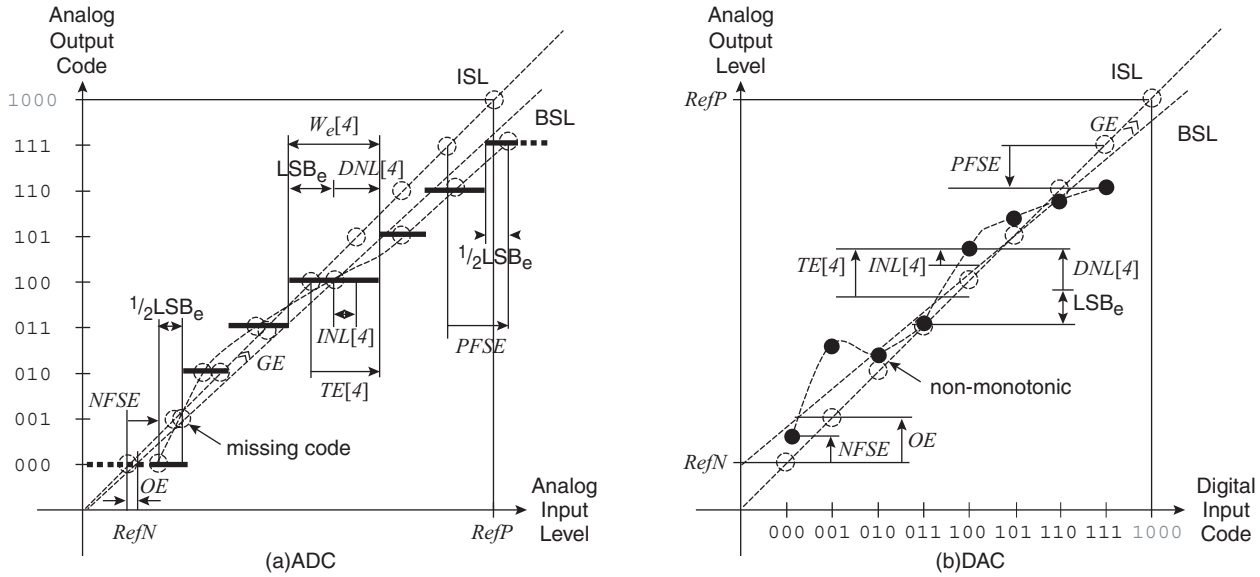
Depending on the converter's architecture, it is sometimes not possible to perform accurate conversions near end codes. For instance, Sigma-Delta converters exhibit poor linearity near full-scale.

Another drawback is that the ESL may induce asymmetric INL (as shown in Figure 2-6, above) and thus lead to an overestimated conversion uncertainty range, because INL is often specified as a single figure in datasheets (plus or minus the absolute value of worst case).

An additional aspect to consider is that using the two end-points (only) to determine the FSR should not be trusted for accurate slope measurements, especially in dynamic testing, or when small signals around the middle of the converter's range are concerned. Note also that with the ESL definition, the gain error of an ADC is positive when the actual FSR is greater than the ideal one, whereas the actual digital output amplitude is smaller than the ideal digital output amplitude for the same analog input amplitude.

Specifying errors with respect to the BSL is often more worthwhile insofar as it reduces the uncertainty range of the converter; also the slope of the BSL is a better indicator of the gain. The choice of the reference line is specified in the specific converter datasheets.

Figure 2-7. Best-fit Static Errors



When the reference line is the BSL, the gain error is defined as the ratio between the slope of the BSL and the slope of the ISL, minus one:

$$GE_{ADC} = \frac{LSB_i}{LSB_e} - 1 \qquad GE_{DAC} = \frac{LSB_e}{LSB_i} - 1$$

The best-fit reference line passes through end-points if, and only if, bit-weight ratios are constant, even though incorrect.

2.4.1.6 Other Intrinsic Parameters

- Startup Time

The DAC startup time is the time required for the output to reach and remain within a specified error band approximate to its final value, measured starting from the activation of the DAC.

The ADC startup time is the time required for the ADC to output a stable code, measured starting from the activation of the ADC.

- DAC Settling Time

The settling time is the time required for the output to reach and remain within a specified error band approximate to its final value, measured starting from the beginning of the output transition.

- DAC Output Drive Capability

The output drive capability (a.k.a. compliance range) is the range of allowable current (respectively voltage) at the output of a voltage (respectively current) output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in non-linear performance.

- DAC Glitch Energy

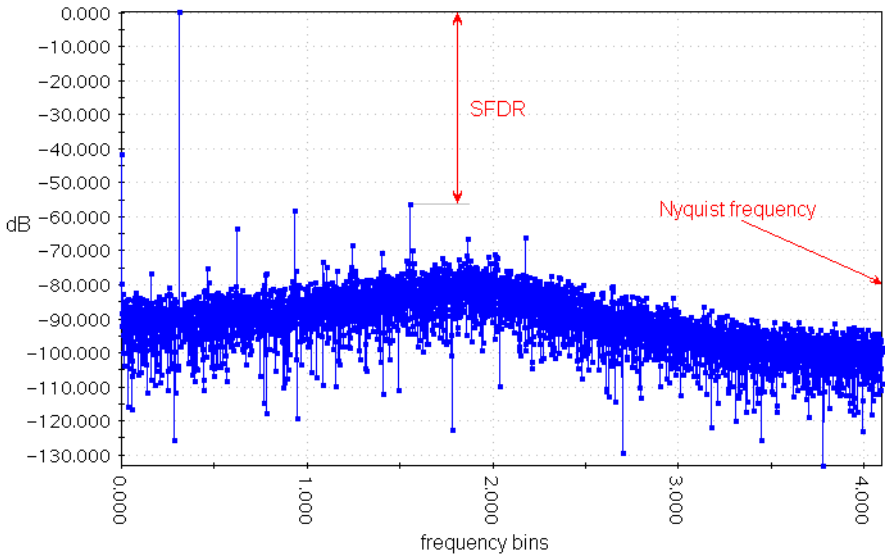
Asymmetrical switching times in a DAC give rise to undesired output transients, which are quantified by a glitch impulse. It is specified as the net area of the glitch in Joules (J) or equivalently in

V·s (respectively A·s), of a rectangle $x[s]\cdot y[\mathrm{V}]$ (respectively $x[s]\cdot y[\mathrm{A}]$), the area of which is the same as the impulse.

2.4.2 Transmission Parameters

Transmission parameters (also known as performance parameters) characterize the channel in which the converter under test is embedded, usually by its affect on a conventional (sinusoid or multitone) test signal. In They are computed from the DFT of the converter's output when submitted to a pure sine wave input signal, the amplitude of which reaches the full-scale (unless otherwise noted). The following definitions assume that a single tone signal is used.

Figure 2-8. Discrete Power Spectrum of an Actual Converter



2.4.2.1 *Spurious Free Dynamic Range*

The spurious free dynamic range (SFDR) is the difference in dB in the output spectrum (or over the specified bandwidth) between the RMS amplitude of the input signal and the highest peak of spurious signal (possibly harmonic component), excluding DC offset. It is expressed in dBc.

2.4.2.2 *Total Harmonic Distortion*

The total harmonic distortion (THD) is the ratio of the RMS sum of the harmonic components to the RMS level of the measured fundamental. It is expressed in dB. Let H_1 be the fundamental frequency. The harmonics are integral multiples of the fundamental frequency: $H_i = i \times H_1$ for $i \leq 2$. H_0 is defined as the DC component, and H_2 is the first harmonic. Five harmonics are usually taken into account, but another bandwidth may be specified:

$$THD = 20\log_{10}\left(\frac{\sum_{i=2}^{\circ} Level_{RMS}(H_i)}{Level_{RMS}(H_1)}\right) = 10\log_{10}\left(\frac{\sum_{i=2}^{\circ} Power(H_i)}{Power(H_1)}\right) \quad [\mathrm{dBc}]$$

Usually, odd harmonics H_{2j+1} are induced by integral non-linearities, whereas even harmonics H_{2j} of the DACs are due to excessive load or update rate.

2.4.2.3 Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is the ratio of the power of the measured output signal to the noise power, which is defined as all spectral components below the Nyquist frequency, but the fundamental frequency, harmonics and dc:

$$SNR = 10\log_{10}\left(\frac{Power(H_1)}{Power(Noise)}\right) = 10\log_{10}\left(\frac{Power(H_1)}{Power(All) - \sum_{i=0}^{6} Power(H_i)}\right) \text{ [dBc]}$$

2.4.2.4 Signal-to-Noise and Distortion

The signal-to-noise and distortion (SINAD) is the ratio of the power of the measured output signal to the noise plus harmonics power:

$$SINAD = 10\log_{10}\left(\frac{Power(H_1)}{Power(All) - \sum_{i=0}^{1} Power(H_i)}\right)$$

$$= -10\log_{10}\left(10^{\frac{THD}{10}} + 10^{-\frac{SNR}{10}}\right) \text{ [dBc]}$$

Noise and harmonics power arise from linearity errors and other noise sources, like random (Boltzmann's) noise. Integral non-linearities tend to increase harmonic distortion, while differential non-linearities show up as an elevated noise floor.

2.4.2.5 Equivalent Number of Bits

The equivalent number of bits (ENOB), also known as the effective number of bits, is an important figure because it informs as to which ideal converter the real converter is equivalent to in terms of transmission performance. See “ADC Inherent Quantization Error” on page 4 for a description of a relationship between the number of bits of the ideal ADC and its SQER for a sinusoid with amplitude A:

$$SQER_A = 20\log_{10}(2) \cdot N + 10\log_{10}(1,5) - (20\log_{10})\left(\frac{A_{CS}}{A}\right)$$

$$\approx 6,02N + 1,76 - 20\log_{10}\left(\frac{A_{CS}}{A}\right)$$

For an actual ADC, non-linearities increase the RMS level of the quantization error, and thus decrease the SQER, which is precisely the SINAD. When a signal is synthesized with a DAC, the quantization is performed by an ideal ADC (a DSP or a general purpose CPU), but non-linearities of an actual DAC also result in the elevation of the noise floor. Thus, for real converters, replacing SQER by SINAD, and N by ENOB leads to:

$$SINAD = 20\log_{10}(2) \cdot N + 10\log_{10}(1,5) + 20\log_{10}\left(\left(1 - \frac{1}{2^N}\right) \times \frac{A}{A_{FS}}\right)$$

For a large enough N, it can be derived that:

$$ENOB \approx \frac{SINAD - 1{,}76 + 20\log_{10}\left(\frac{A}{A_{FS}}\right)}{6{,}02} \quad [bits]$$

For a full-scale, single tone signal:

$$ENOB = \frac{SINAD - 10\log_{10}(1{,}5)}{20\log_{10}(2)} \approx \frac{SINAD - 1{,}76}{6{,}02} \quad [bits]$$

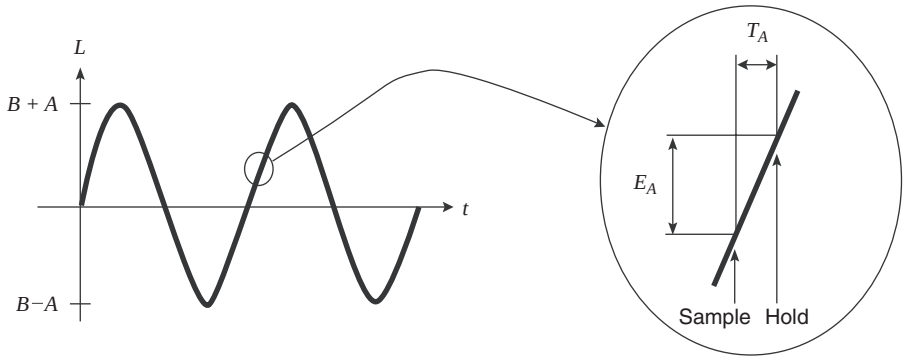
Knowing the desired transmission performance at a given signal frequency and the converter's data rate, this formula enables to choose a converter according to its ENOB. For instance, one bit less in ENOB results in 6dB less in SINAD; in worst cases, a non-linearity as small as ±½ LSB may have this same effect.

2.4.2.6 *Aperture Uncertainty and Induced Jitter Noise*

No real ADC is capable of perfectly regular sampling. Likewise, no real DAC has identical transition delay each time it is clocked and no real timing logic can produce perfectly regular clock spacing. The result is jitter, or random clock-to-clock timing errors, causing each ADC sample, or DAC transition, to occur sooner or later than its ideal time. In ADC sampling, this random irregularity is the uncertainty in the time at which the sample/hold goes from sample mode to hold mode; it is termed the aperture uncertainty, T_A.

When a moving analog signal is sampled at any portion of the waveform with non-zero slope, timing error induces a level error, which is termed aperture error, E_A, in ADCs. The induced jitter noise varies in direct proportion with signal amplitude, whereas level errors induced by intrinsic errors do not. The effect of the aperture error is to set a limitation on the maximum frequency of the input sine wave, because it defines the maximum slew rate of that signal.

Figure 2-9. ADC Aperture Error



For a signal $L(t) = B + A\sin\omega t$ the maximum slew rate occurs when $\omega t = 0[\pi]$. At these moments, it equals:

$$\left|\frac{dL}{dt}\right| = \omega A = 2\pi f A$$

Thus, the highest slew rate is achieved for a clipping sinusoid, the amplitude of which is $A = 2^{N-1}Q$ where Q is the quantum (i.e. 1 LSB). The corresponding maximum aperture error is:

$$E_A = T_A \left.\frac{dL}{dt}\right|_{max} = 2\pi f T_A A$$

If the aperture error is not to affect the accuracy of the converter, it must be less than ½ LSB at the point of maximum slew rate:

$$E_A \le \frac{1}{2} LSB \Rightarrow 2\pi f T_A A \le \frac{A}{2^N}. \text{ There comes: } f_{signal} \le \frac{1}{2^{N+1}\pi T_A}$$

A histogram of timing errors usually shows a roughly Gaussian distribution. The standard deviation of this distribution is the RMS jitter, and the peak-to-peak error is roughly six times this. If the clock signal does not have a low jitter and fast rise and fall times, the induced jitter noise will affect the SNR as follows:

$$\text{induced } SNR = 20\log_{10}\left(\frac{1}{2\pi} \times \frac{T_{signal}}{T_A}\right) \approx 20\log_{10}\left(\frac{T_{signal}}{jitter_{RMS}}\right) - 16 \quad [\text{dB}]$$

3. Test Methods

3.1 Intrinsic Parameter Measurements

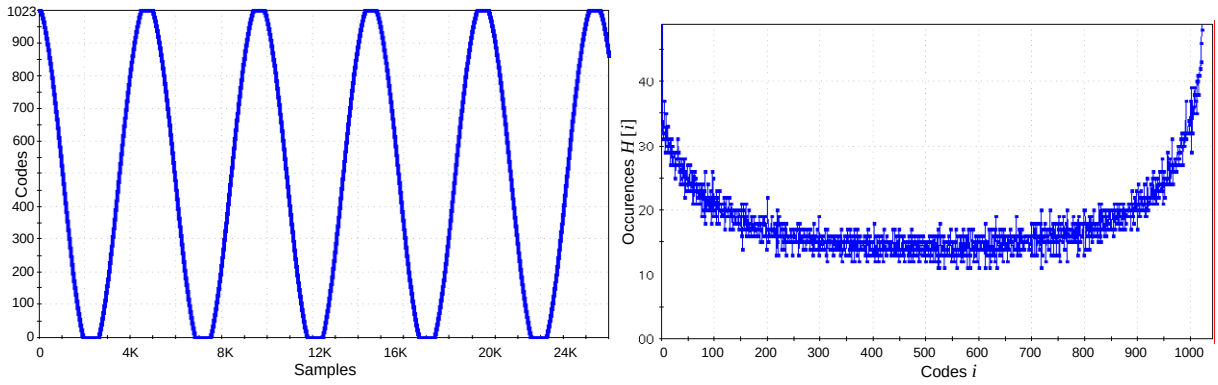
3.1.1 DAC Static Parameters

DAC static parameters are usually measured by sending a digital ramp. The output levels related to a same code may be averaged, in order to separate the actual DAC errors from the test environment noise.

3.1.2 Sine Wave Histogram Testing of ADCs

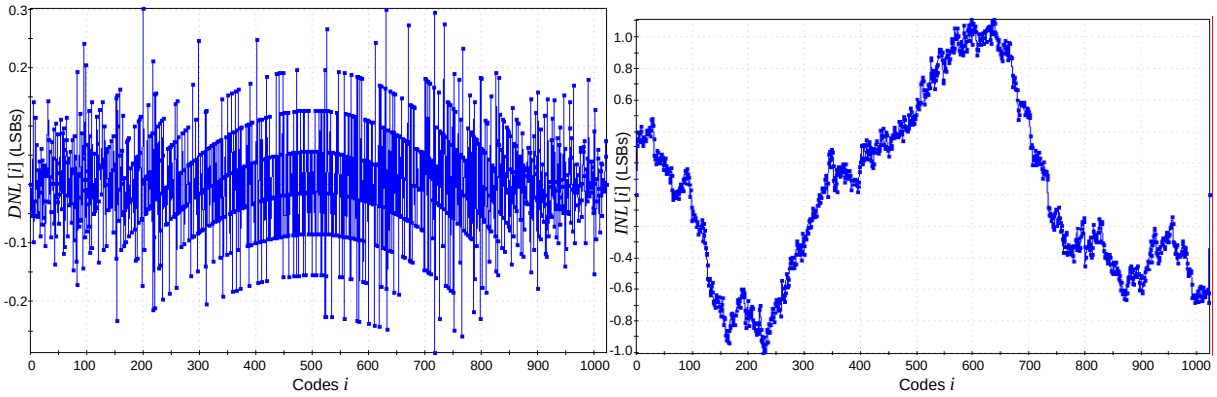
Static parameters of ADCs are usually not tested with a ramp in production testing, because it is quite difficult to build an accurate enough ramp or saw tooth signal. Since it is easier to get a relatively pure sinusoid (DAC + Low Pass Filter or Band Pass Filter, or Low Frequency Generator), ADC static errors are rather computed by sending a slow, clipped, analog sine wave and performing statistics on the resulting code histogram (IEEE Std 1057-94 (R2001), IEEE Std 1241-2000), in order to compute an estimate of the actual transition levels. Furthermore, the statistical nature of the code density test gives a more accurate characterization of the converter's noise compared to a conventional test in which each output code is attained only once.

Figure 3-1. Sine Wave Code Histogram of an Actual 10-bit ADC



Once transition levels have been estimated, normalized RSL and effective LSB can be defined as explained in the paragraph “Choice of the Reference Straight Line” on page 11. Since nonlinearities are expressed in effective LSB, they can be computed using normalized transition levels, without the need of actual transition levels.

Figure 3-2. Best-fit DNL and INL Plots of an Actual 10-bit ADC Using Sine Wave Histogram Testing



Since the evaluation of other static errors relies on the estimation of the actual transition levels, the accuracy of such measurements is strongly in function of how accurate the offset and amplitude of the input signal are and how well the references of the ADC are known.

Code histogram testing is blind to hysteresis and non-monotonicity. In literature, "two dimensional" modified histogram tests have been devised but none as yet have become a standard. (See “References” on page 20. numbers 3 and 4.)

Depending on the maturity of the ADC and the process, the sine wave histogram testing is sometimes replaced by a functional test. This functional test aims to assure that the total error remains within specification on some points only (functional test with a given number of well defined analog input levels).

3.1.3 Transient Parameters

Transient parameters are usually not measured as it is even impossible to measure some of them with currently available automatic test equipment (ATE).

3.2 Transmission Parameter Measurements

All these measurements consist in applying a sine wave and performing an FFT on the output samples, then applying the previously specified computations. Depending on the tester used, there are limitations on accuracy, signal and/or sampling frequency. The ratio between signal and sampling frequencies is usually chosen so that measured frequency domain parameters take as many error sources as possible, including especially linearity errors.

3.3 Test Methods Comparison

The following table features the benefits of both histogram and FFT testing in terms of checked errors:

Table 3-1. Summary of Errors Checked by Histogram and FFT Testing

Error	Histogram	FFT
DNL	yes (spikes in histogram)	appears as elevated noise floor
INL	yes	appears as harmonic distortion
Missing Codes	yes (bins with 0 count)	appears as elevated noise floor

Table 3-1. Summary of Errors Checked by Histogram and FFT Testing

Error	Histogram	FFT
Aperture Uncertainty	no (averaged out)	appears as elevated noise floor
Noise	no (averaged out)	appears as elevated noise floor
Gain error	yes (peak-to-peak spread of distribution)	no

4. References

1. IEEE Std 1057-94 (R2001) "IEEE Standard for digitizing waveform recorders", SH94245, ISBN 1-55937-488-8, pp. 4-15, June 1994, September 2001. Approved January 2002 by ANSI.
2. IEEE Std 1241-2000 "IEEE Standard for Terminology And Test Methods for Analog-to-Digital Converters", SH94902, ISBN 0-7381-2724-8, pp. 37-40, December 2000.
3. J. Larrabee, F.H. Irons, D.M. Hummels, "using sine wave histograms to estimate analog-to-digital converter dynamic error functions", IEEE Trans. on Instrum. and Meas., vol.IM-47, No.6, pp.1448-1456, 1998.
4. P. Arpaia, A.C. Serra, P. Daponte, C.L. Monteiro, "ADC Testing Based on IEEE 1057-94 Standard - Some Critical Notes", IEEE 0-7803-5890-2/00/$10.00, pp. 119-124, 2000.

Revision History

Doc. Rev	Comments	Change Request Ref.
6022B	*Section 2.4.1.4 "Other Static Parameters" on page 10*: *NFSE* equation corrected. Pagination and numbering changed with updated document format.	5162
6022A	First issue	

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