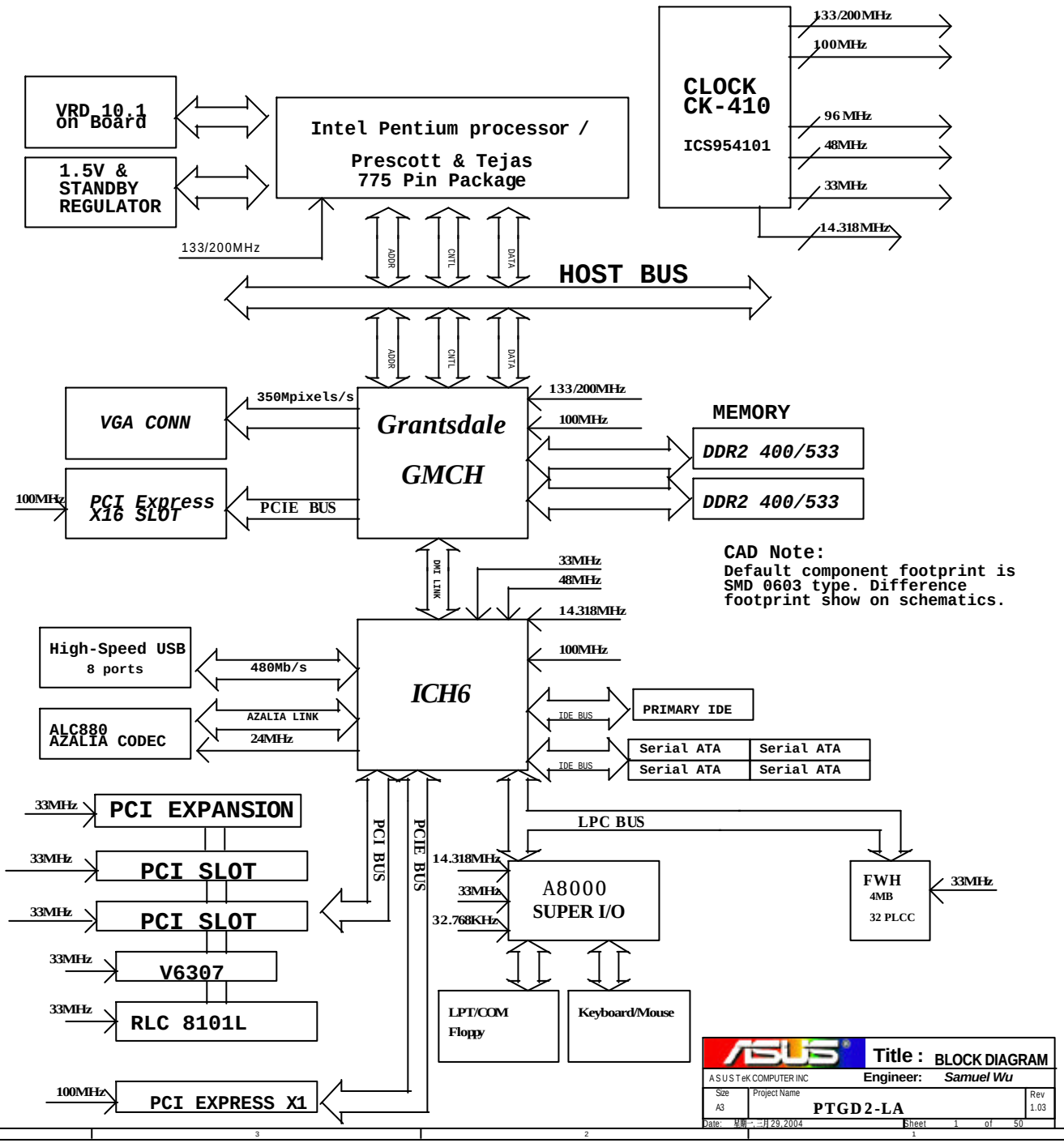
PTGD2-LA

Revision: 1.03 - A19 (3/24/2004) DDR2



ASUS ECN Control Table

ECN Document Number	DATE	Schematics Revision	BOM Part Number	PCBA Revision	PCB Revision

ASUSTeK COMPUTER INC	Title : ECN CONTROL		
	Engineer: *Samuel Wu*		
Size: A3	Project Name: PTGD2-LA		Rev: 1.03
Date: 星期一, 二月 29, 2004	Sheet 2 of 50		

Schematics Change History

Version	Date / Author	Comments
1.01	11/30/2003 John Hong	1. Change RN61 net from +3VSB to +3V (page 27) 2. Change Q122 to P-MOS Vgs(th)=2.4V, 07-005002110 (page 26) 3. Remove R983 (page 26) 4. Change SYS_RESET# PU RN from RN62 to RN61 (page 26) 5. Change ICH_W6_PU RN from RN61 to RN62 (page 26) 6. Change FP_LINE pin define 7. Change EXP_SLR PU voltage to +1.5V 8. Change Azalia port define 9. Change R491 to 18.2K ohm (making +1.2V_HT=1.189V) 10. Change DDR2 termination res to 39 ohm (only for CS#, CKE, ODT), this changing will improve DDR2 margin. 11. Change to HP naming rule. 12. Change VGA HSYNC and VSYNC level shift P-MOS. 13. Change FLOPPY pin3 to pin7 as GPIO. 14. Change SIO and NIC 15. Change NIC and 1394 ID to 17 and 18

SSID List

SUBSYSTEM ID	DESCRIPTION
CLK	CLOCK GENERATOR
CORE	CPU CORE
NB	NORTH BRIDGE GMCH
MEM	MEMORY
VGA	INTERNAL VGA
PE16	PCI EXPRESS x16
SB	SOUTH BRIDGE ICH6
RTC	RTC
CCMOS	CLEAR CMOS
SMBUS	SMBUS
IDE	UATA IDE CONNECTOR
SATA	SERIAL ATA CONNECTOR
FWM	FIRMWARE HUB ROM
LAN	LAN CONNECTOR
USB	USB
EMI	EMI
AUD	AC97 AUDIO CODEC
F_AUD	FRONT AUDIO
PE1	PCI EXPRESS x1
PCI	PCI SLOT
PECTL	PCI EXPRESS CONTROLLER
PS2	PS2 KB & MOUSE
COM	SERIAL PORT
E1394	IEEE 1394
PANEL	HPQ PANEL
VCORE	VCORE
ITP	PROCESSOR ITP
LPT	PARALLEL PORT
THERM	THERMALTRIP
V_DDR	VTT_DDR
R_1.5V	+1.5V
V_PCI	+3.3V_PCI
5V_DUAL	+5V_DUAL
3VSB	+3VSB
VTT_CPU	VTT_CPU
LED	LED
ATX	ATX POWER SUPPLY
VRM	VRM POWER SUPPLY
1.8V_DUAL	+1.8V_DUAL

ASUS

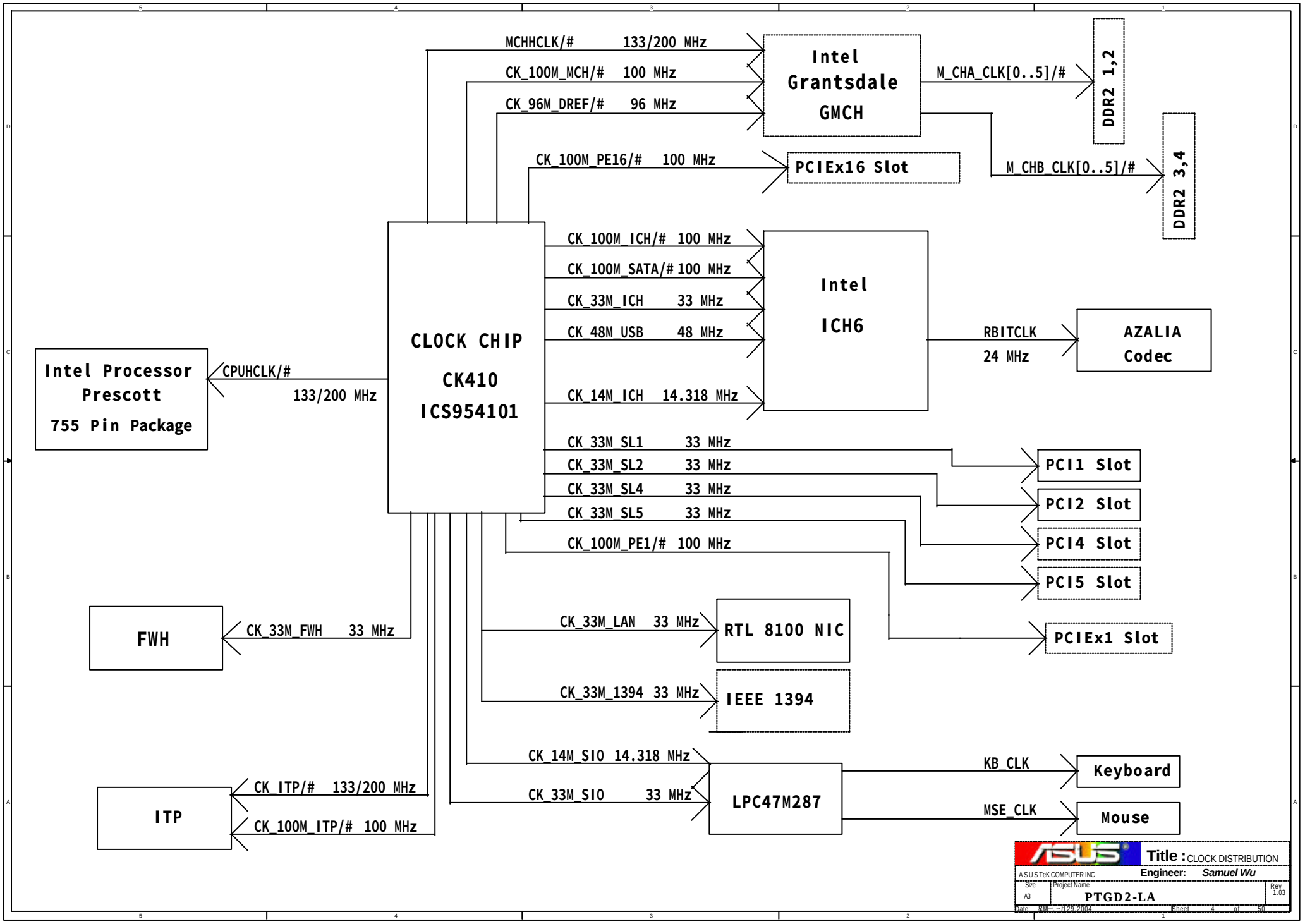
Title : CHANGE HISTORY

A S U S TeK COMPUTER INC

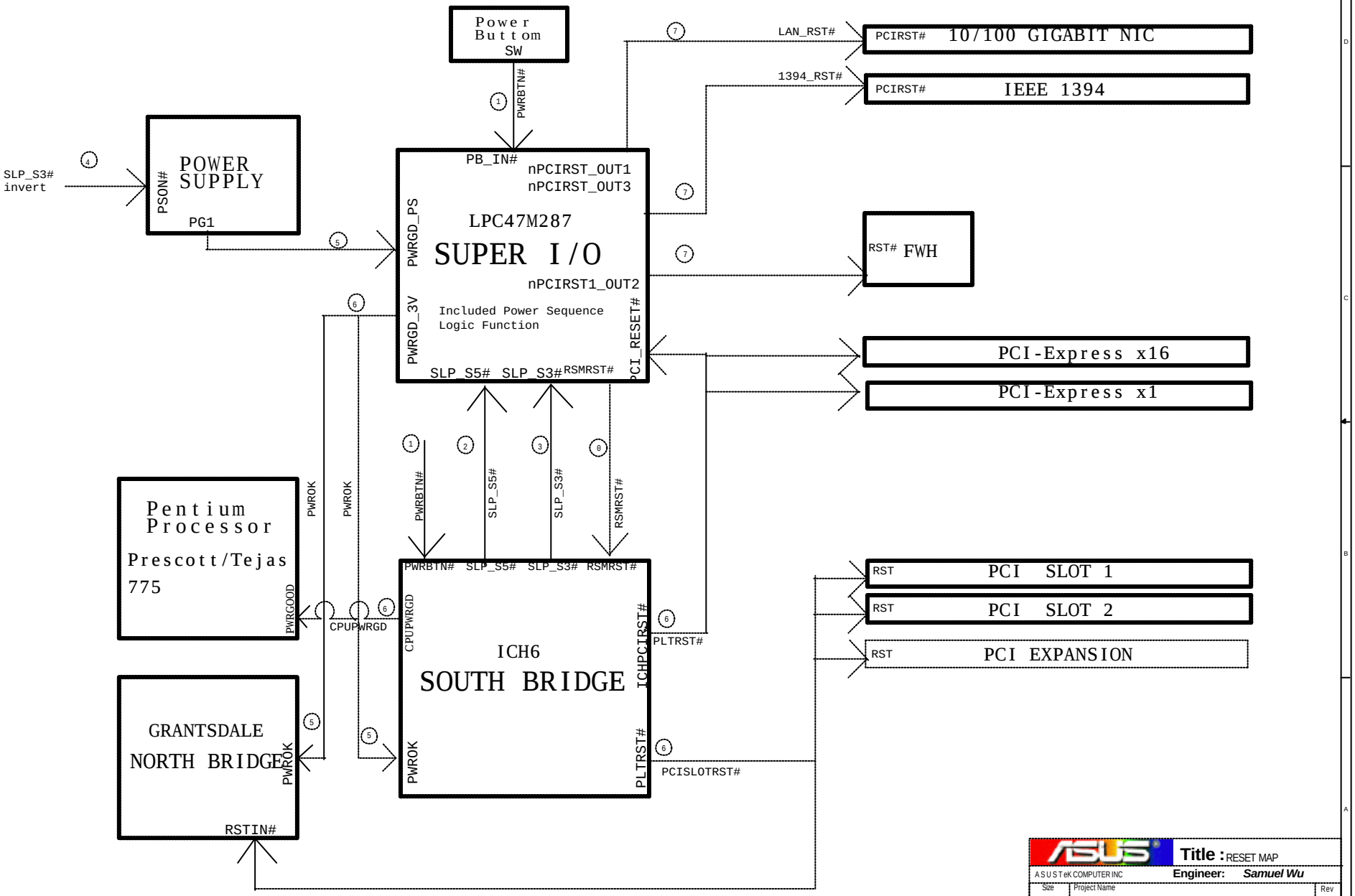
Engineer: *Samuel Wu*

Size	Project Name	Rev
A3	PTGD2-LA	1.03

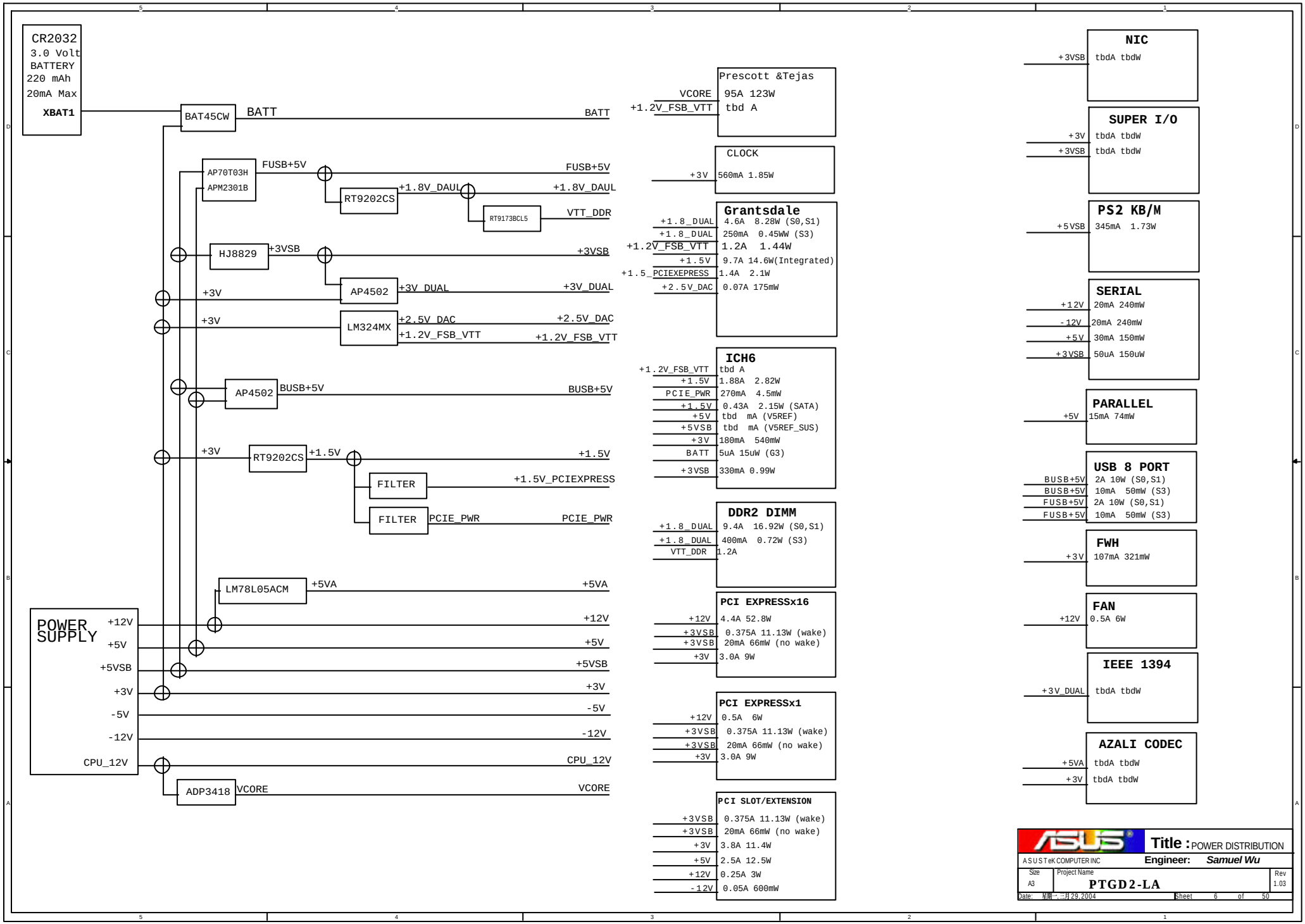
Date: Tuesday, March 29, 2004 Sheet 3 of 50

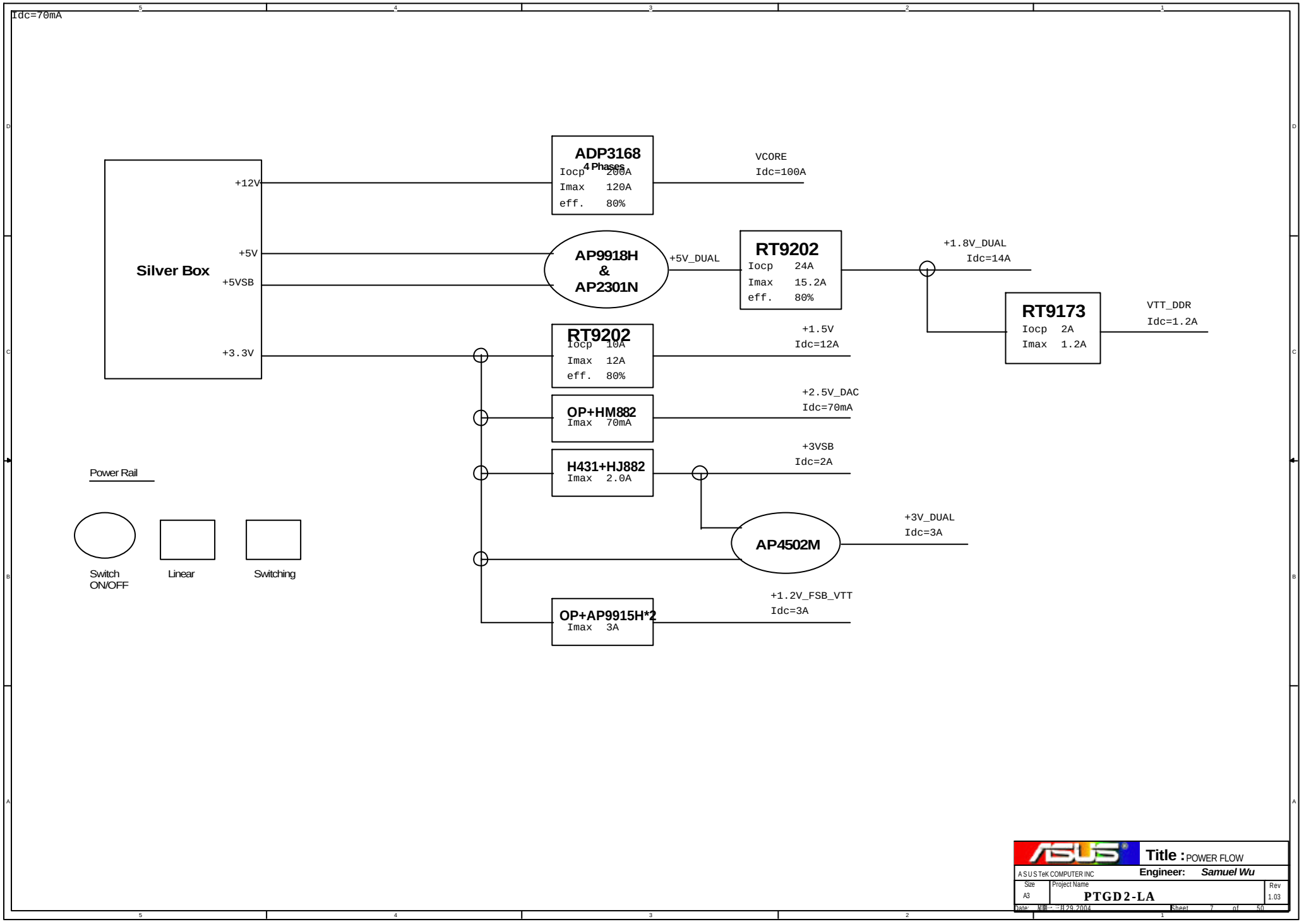


G0-to-G3 State Explain:
a. VCCSUS dirves high when PWR CONN plugd in.
b. RSMRST# drives high from SIO to ICH6.
c. SUSCLK sent out CLK from ICH6 to SIO.

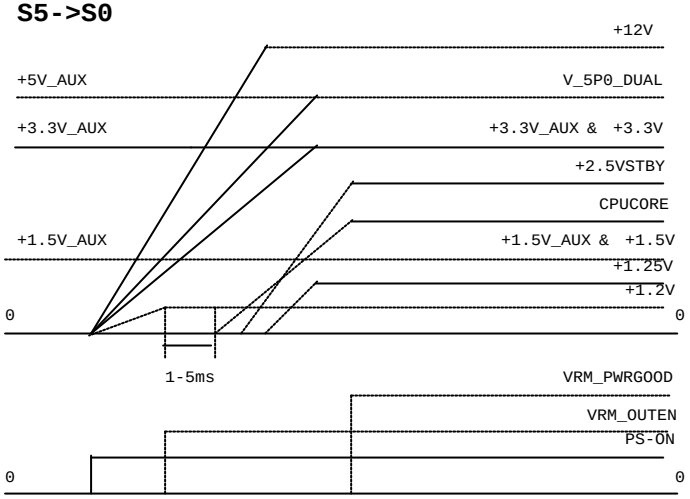


ASUSTeK COMPUTER INC
Title : RESET MAP
Engineer: Samuel Wu
Size: A3 | Project Name: PTGD2-LA | Rev: 1.03
Date: 11/29/2004 | Sheet 5 of 50

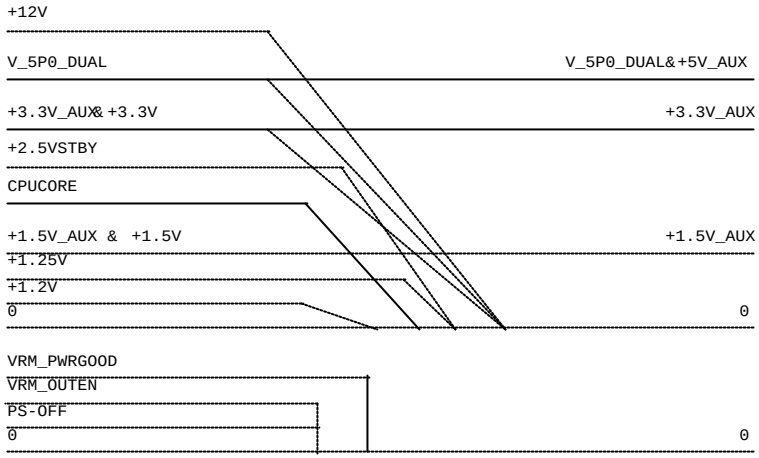




S5->S0

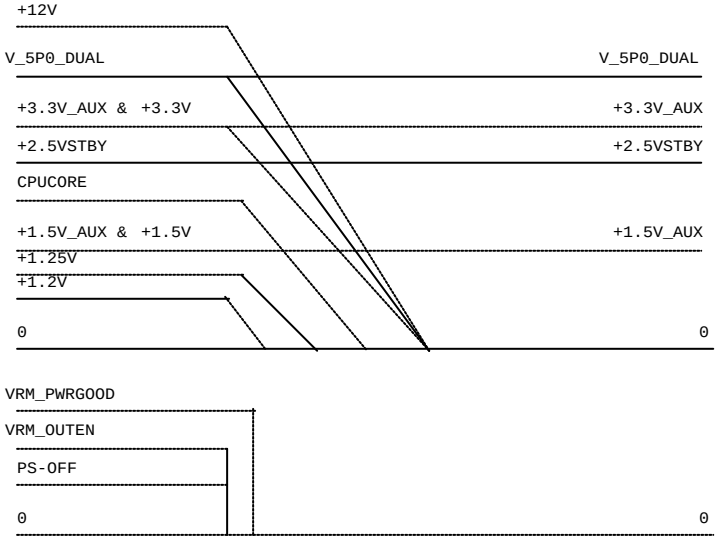


S0->S5

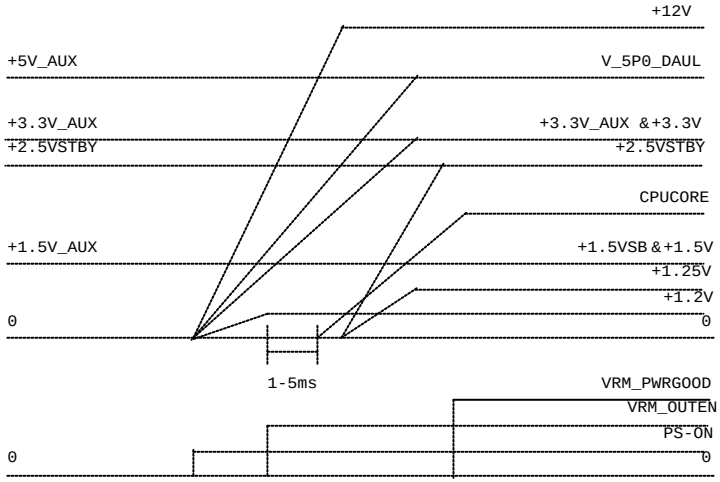


1.CPUCORE must rise after the voltage across 90% of +1.2V,andthe interval is within 1-5ms
2.VRM_OUTEN rises after the voltage across 90% of its specified value

S0->S3



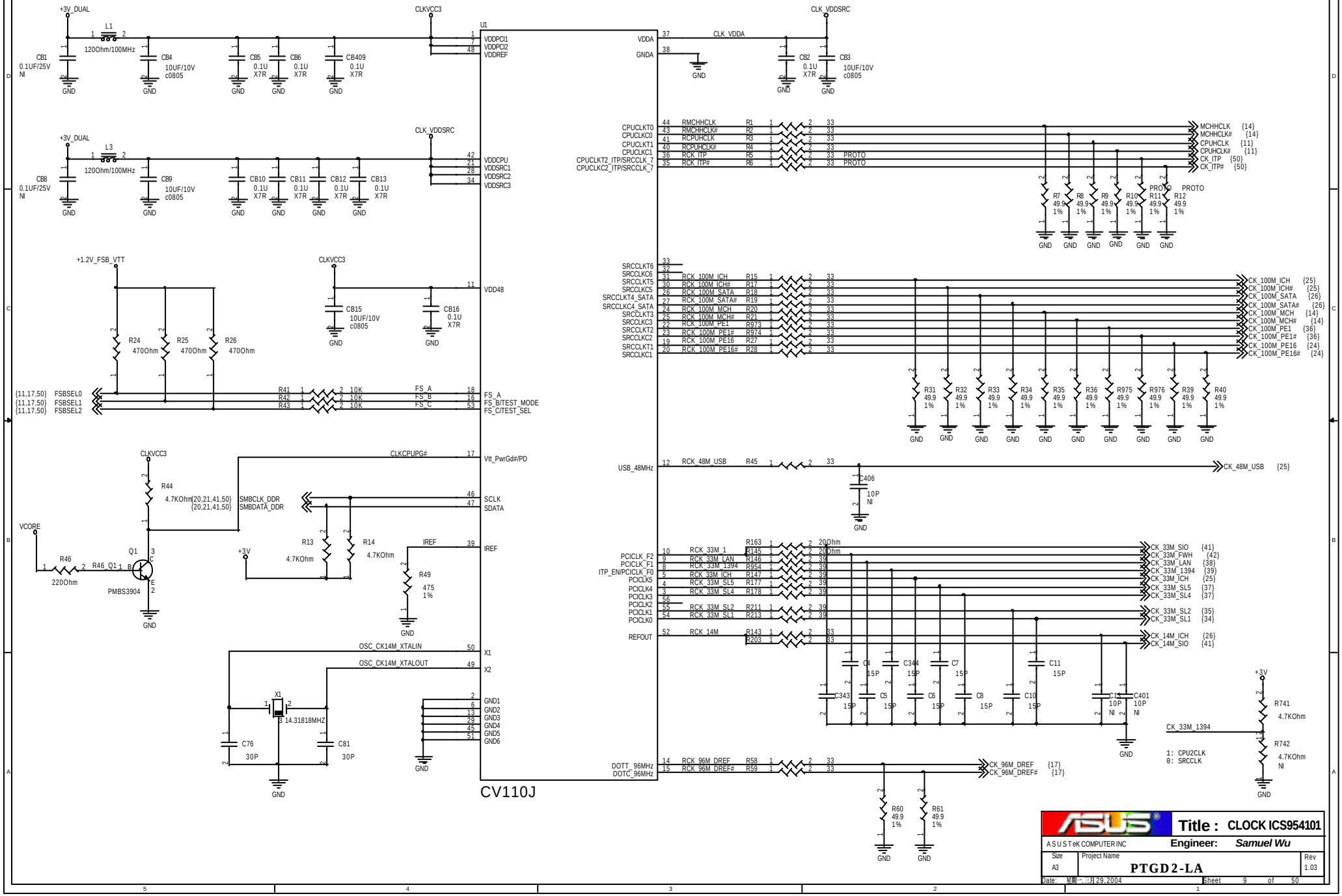
S3->S0

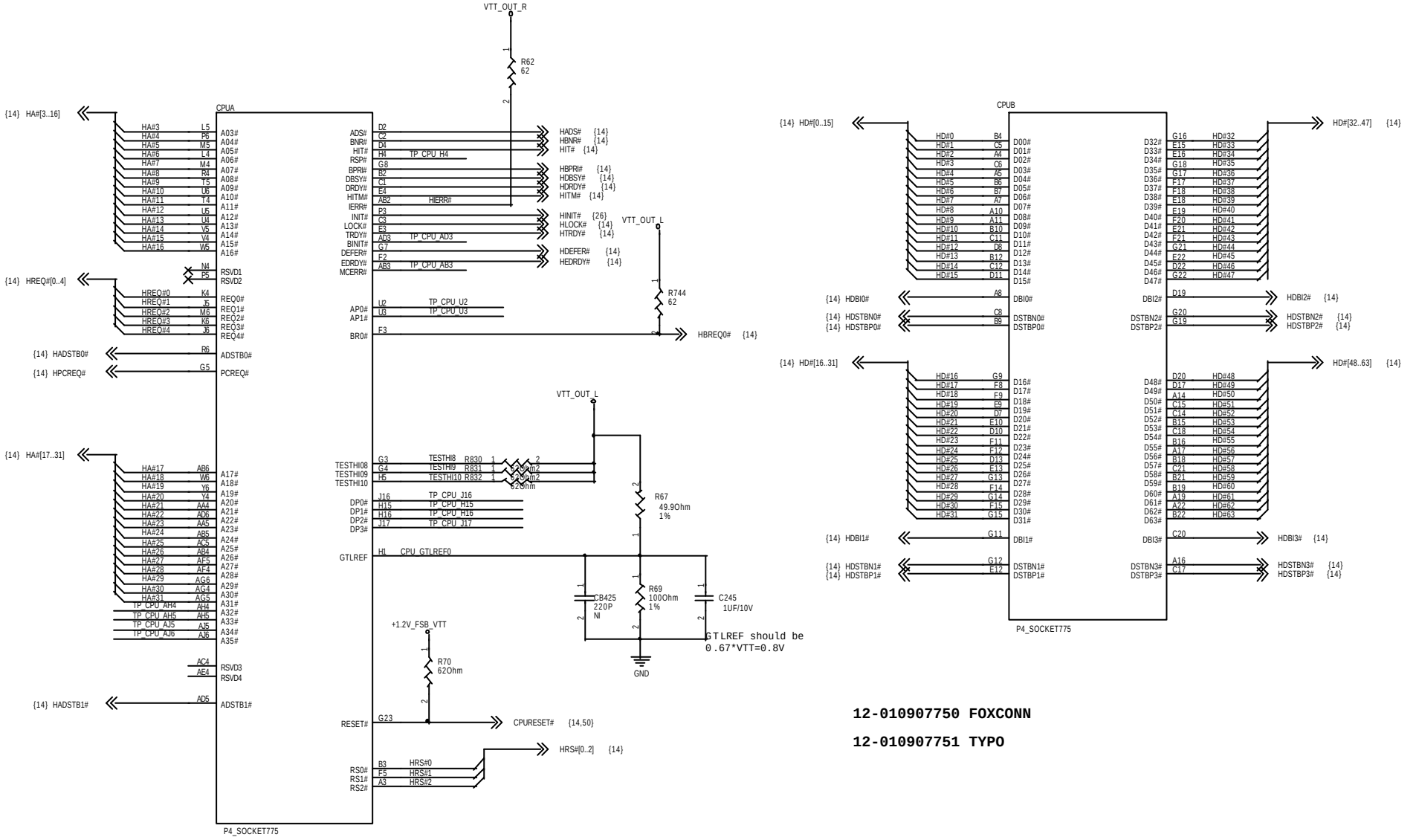


1.CPUCORE must rise after the voltage across 90% of +1.2V,andthe interval is within 1-5ms
2.VRM_OUTEN rises after the voltage across 90% of its specified value

S0: Windows Running+12V,V_5P0_DUAL,+3.3V,+3.3V_AUX,+2.5VSTBY,CPUCORE,+1.5V,+1.5V_AUX,+1.25V,+1.2V existed
S3: Windows StandbyV_5P0_DUAL,+3.3V_AUX,+1.5V_AUX,+2.5VSTBY existed
S5: AC Power On Only+5V_AUX,+3.3V_AUX,+1.5V_AUX existed

ASUSTeK COMPUTER INC	Title : POWER SEQUENCE	
	Engineer: Samuel Wu	
Size: A3	Project Name: PTGD2-LA	Rev: 1.03
Date: Monday, November 29, 2004	Sheet 8 of 50	



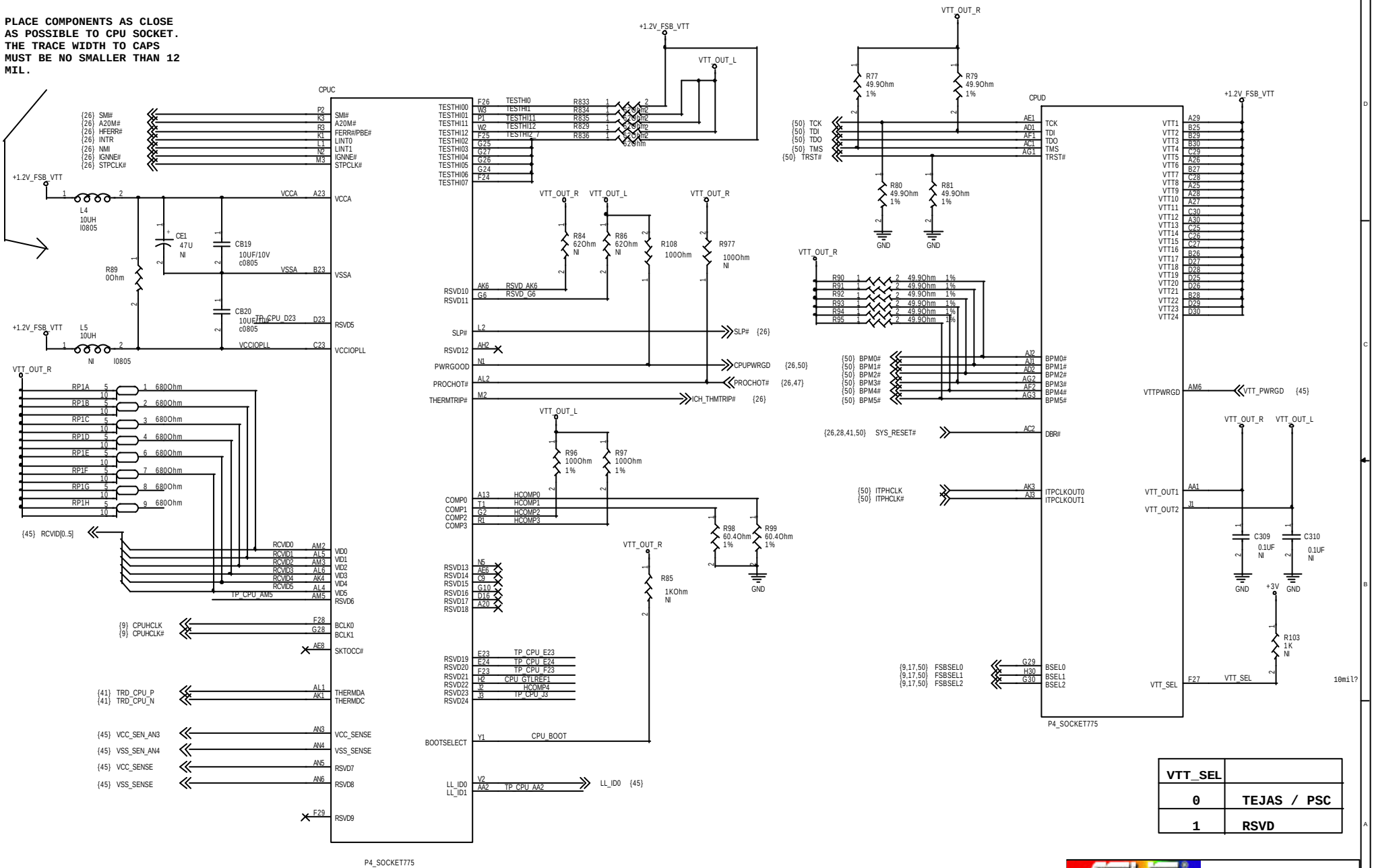


12-010907750 FOXCONN

12-010907751 TYPO

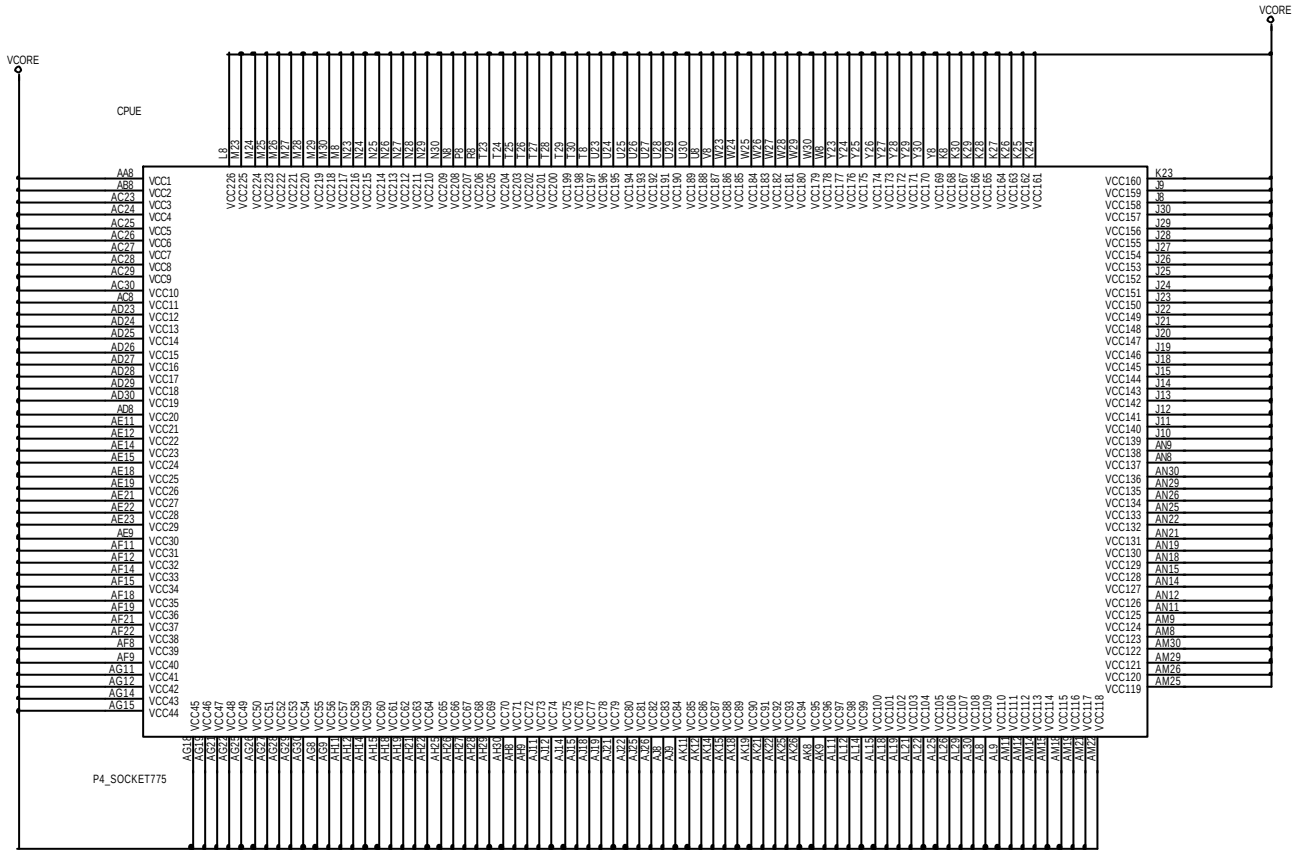
ASUSTeK COMPUTER INC	Title : PRESCOTT / TEJAS -1	
	Engineer: *Samuel Wu*	
Size: A3	Project Name: PTGD2-LA	Rev: 1.03
Date: 星期一, 三月 29, 2004	Sheet 10 of 50	

PLACE COMPONENTS AS CLOSE AS POSSIBLE TO CPU SOCKET. THE TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12 MIL.

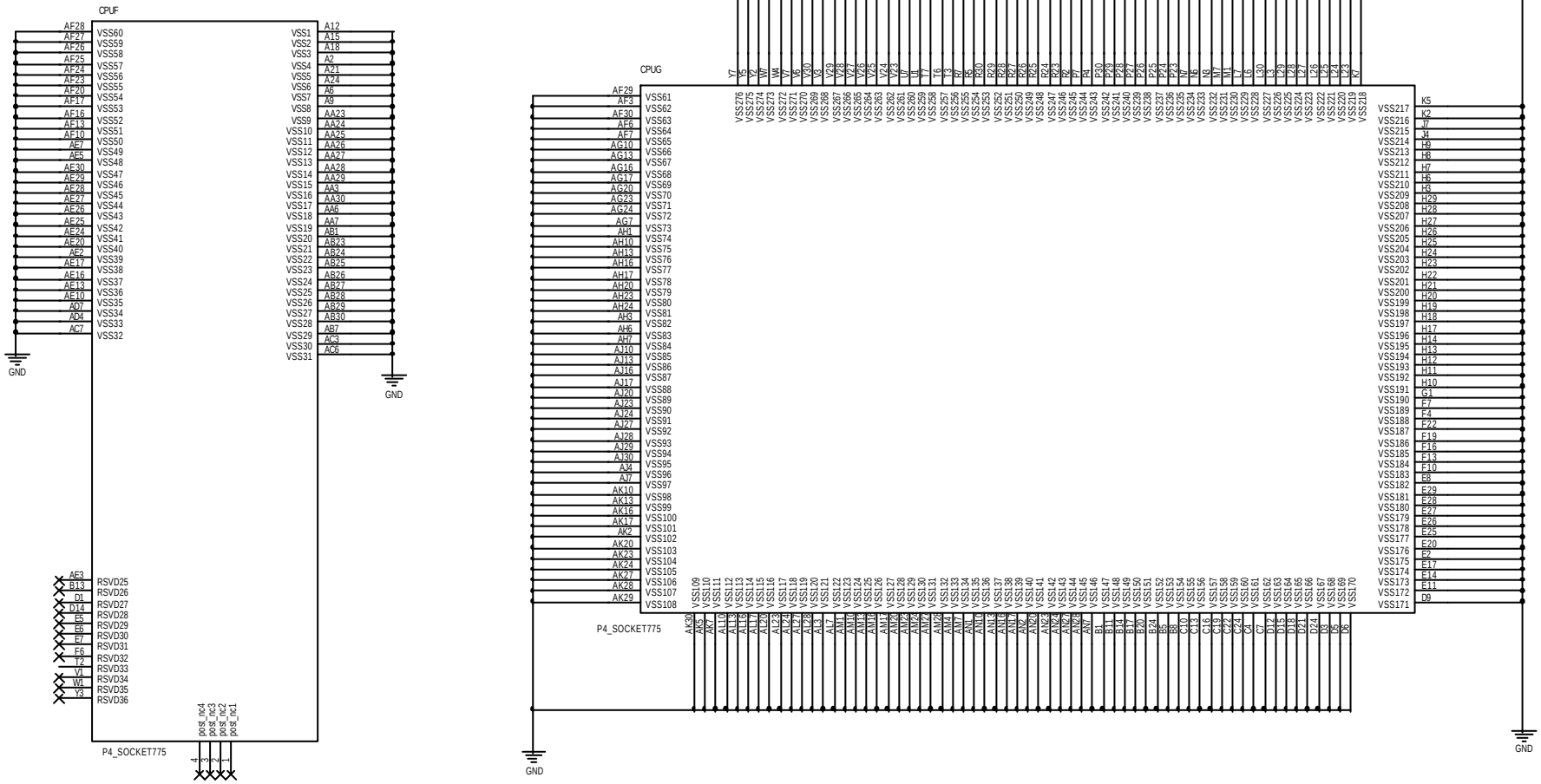


VTT_SEL	
0	TEJAS / PSC
1	RSVD

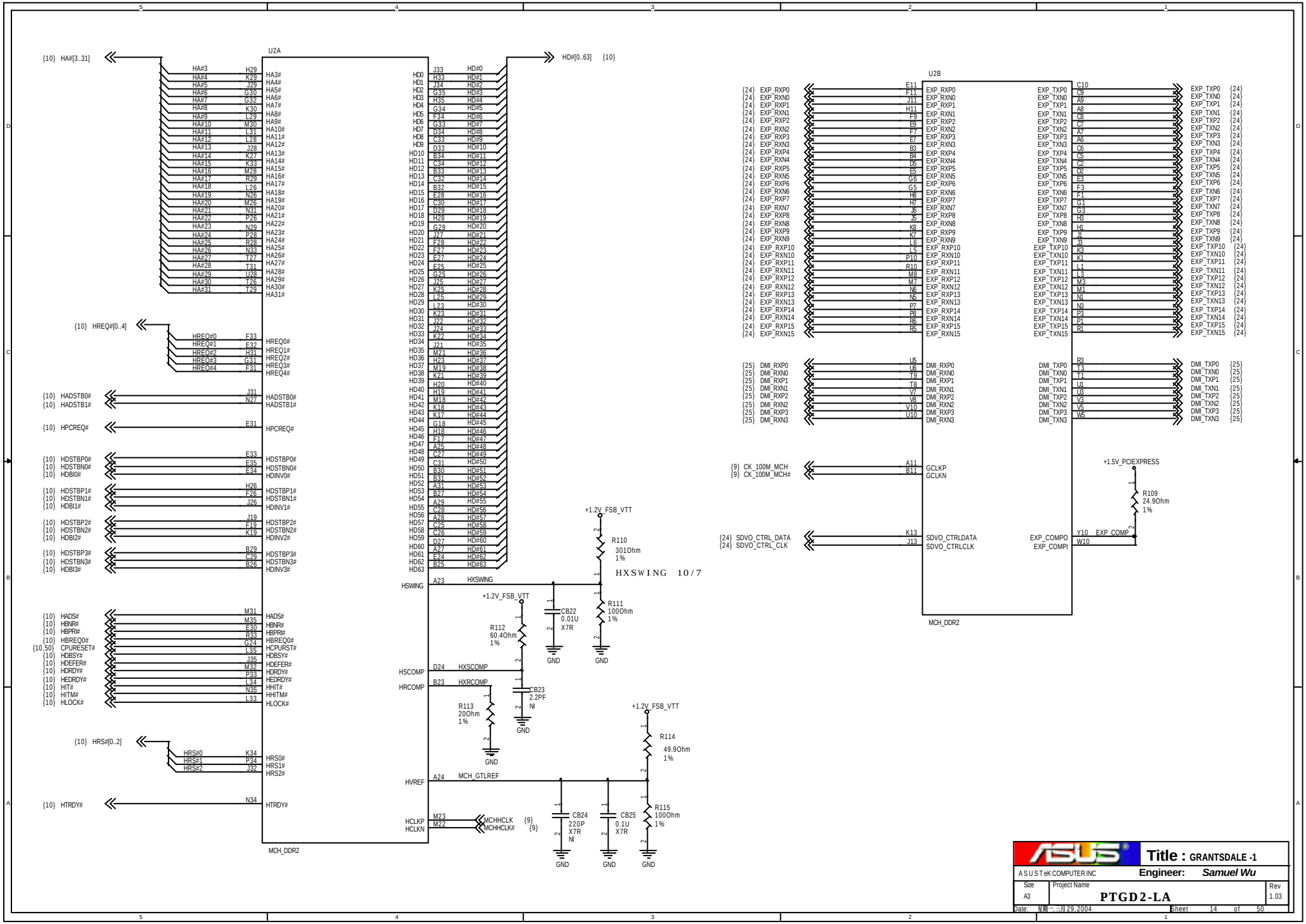
ASUS	Title : PRESCOTT / TEJAS -2
A S U S TeK COMPUTER INC	Engineer: Samuel Wu
Size: A3	Project Name: PTGD2-LA
Rev: 1.03	
Date: 星期一, 三月 29, 2004	Sheet 11 of 50

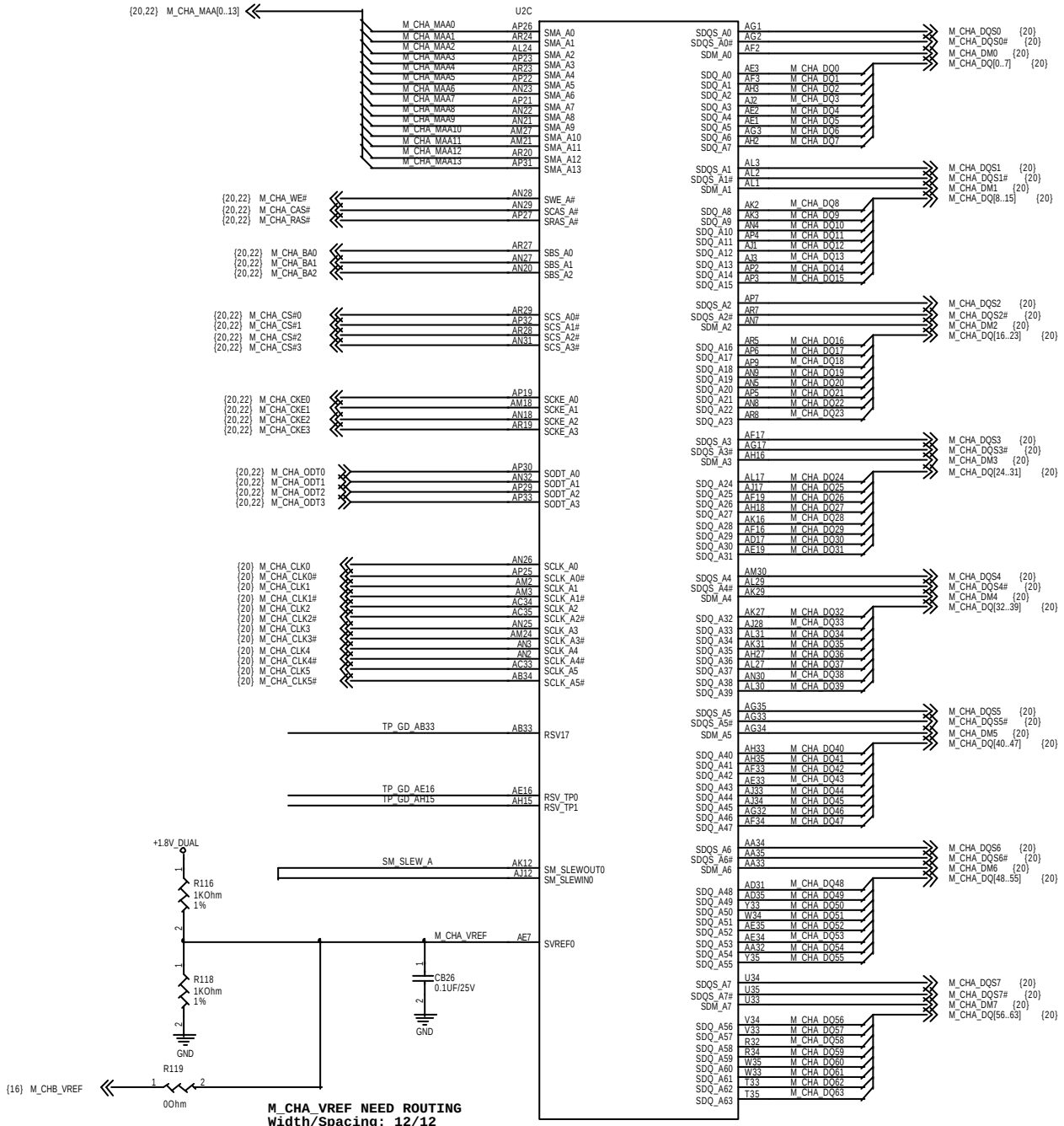


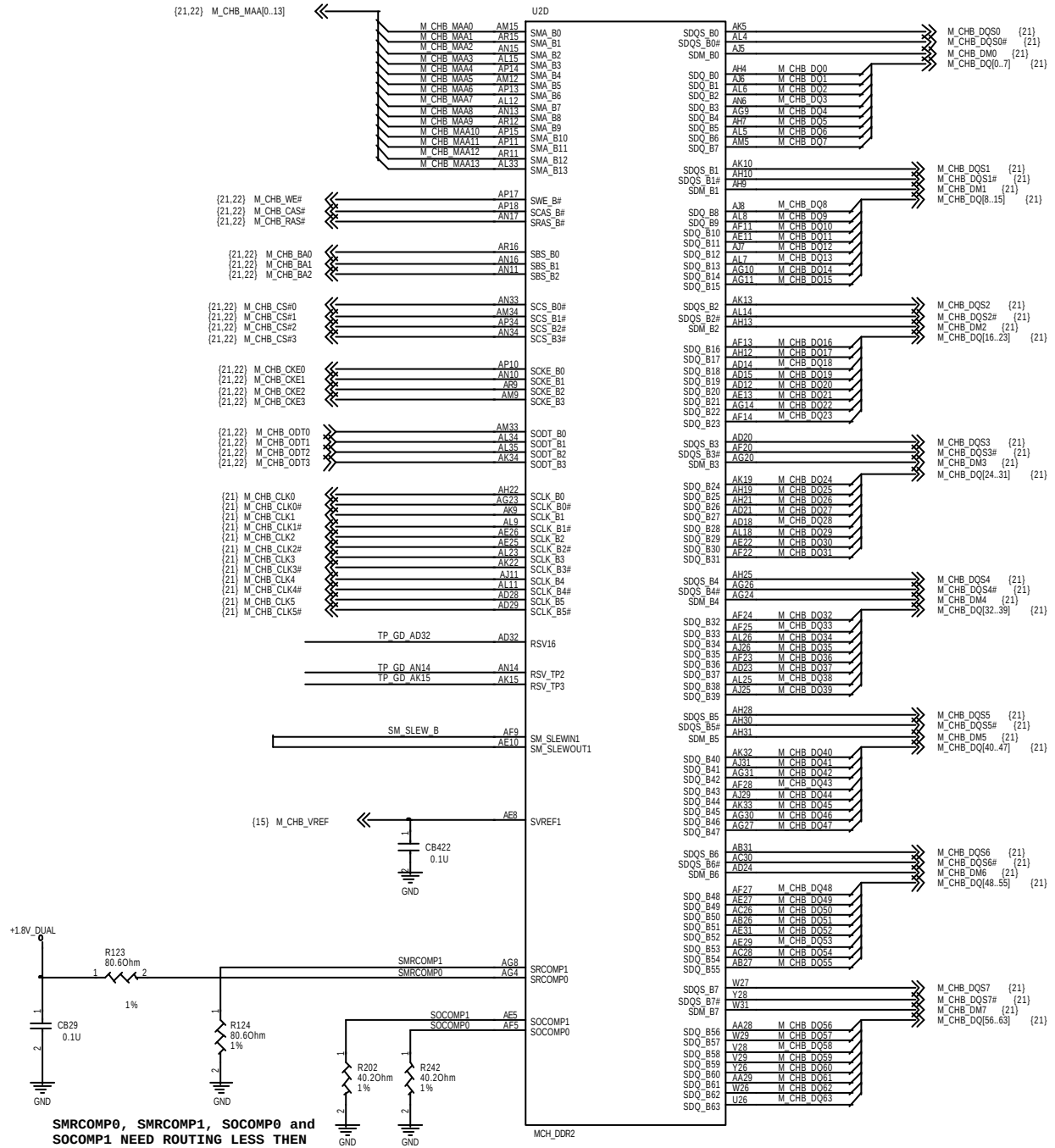
Title : PRESCOTT / TEJAS -3			
A S U S TeK COMPUTER INC	Engineer: Samuel Wu		
Size: A3	Project Name: PTGD2-LA		Rev: 1.03
Date: 星期一, 三月 29, 2004	Sheet 12 of 50		

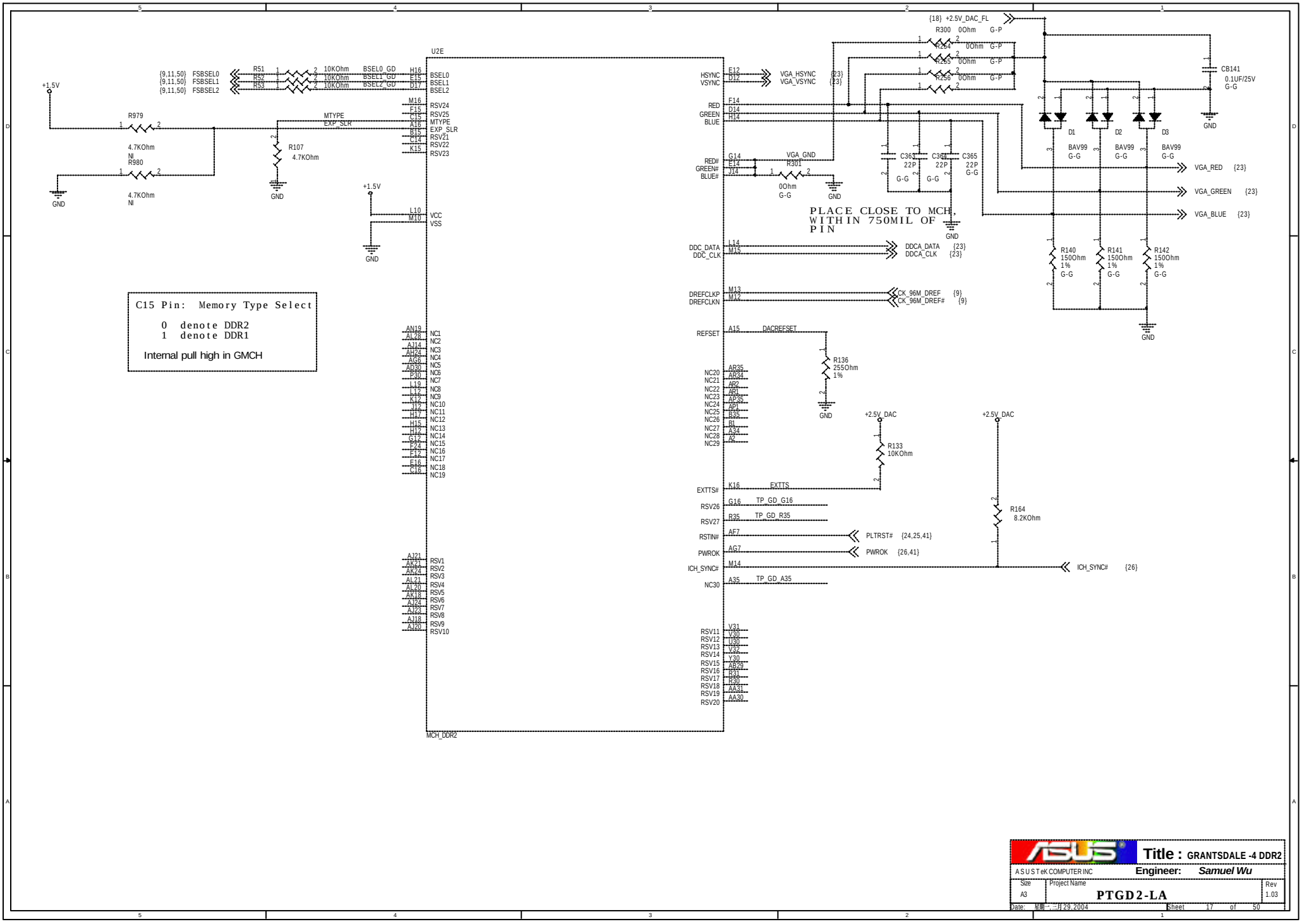


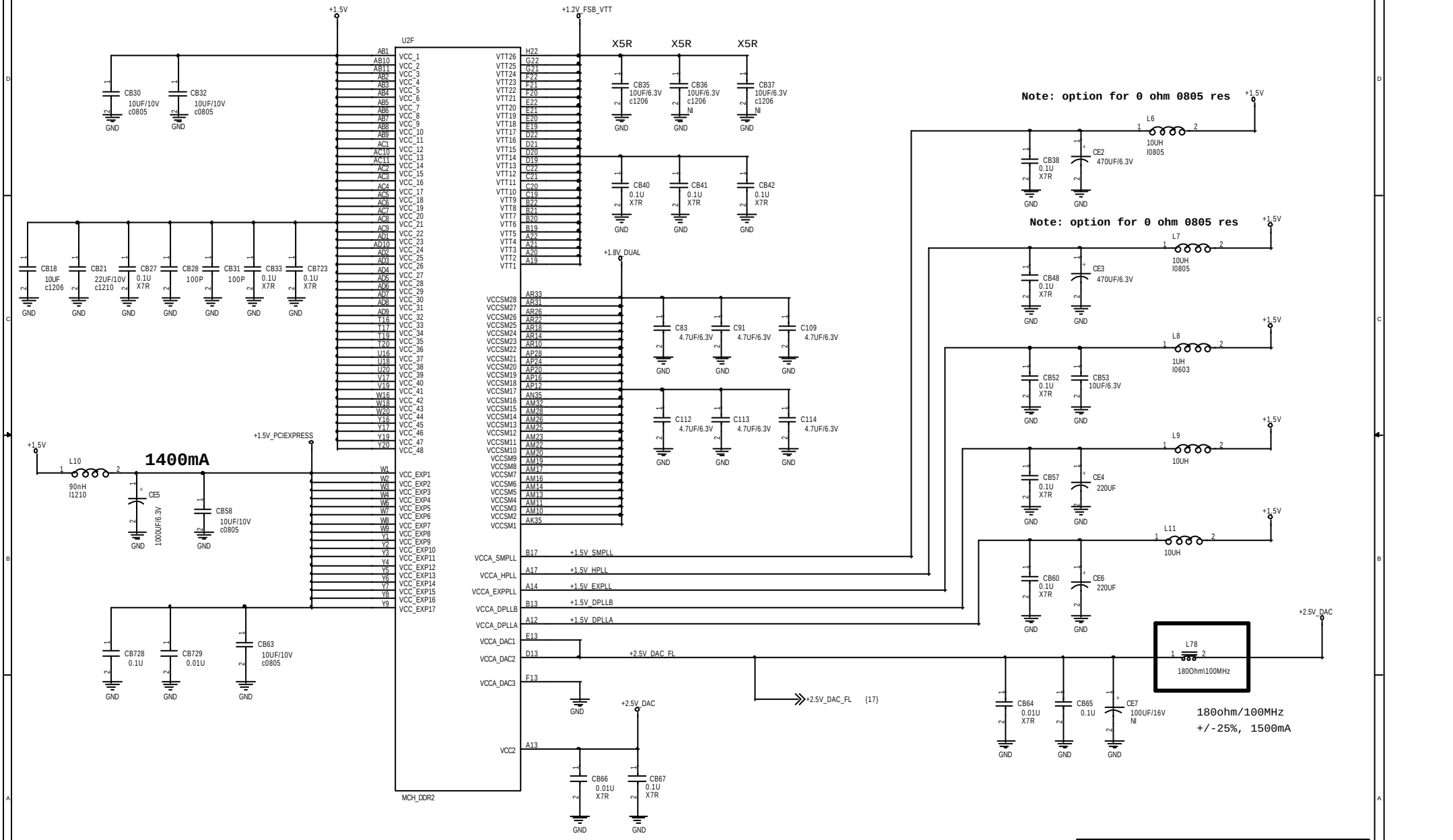
ASUSTeK COMPUTER INC	Title : PRESCOTT / TEJAS -4	
	Engineer: *Samuel Wu*	
Size: A3	Project Name: PTGD2-LA	Rev: 1.03
Date: 星期一, 三月 29, 2004	Sheet 13 of 50	

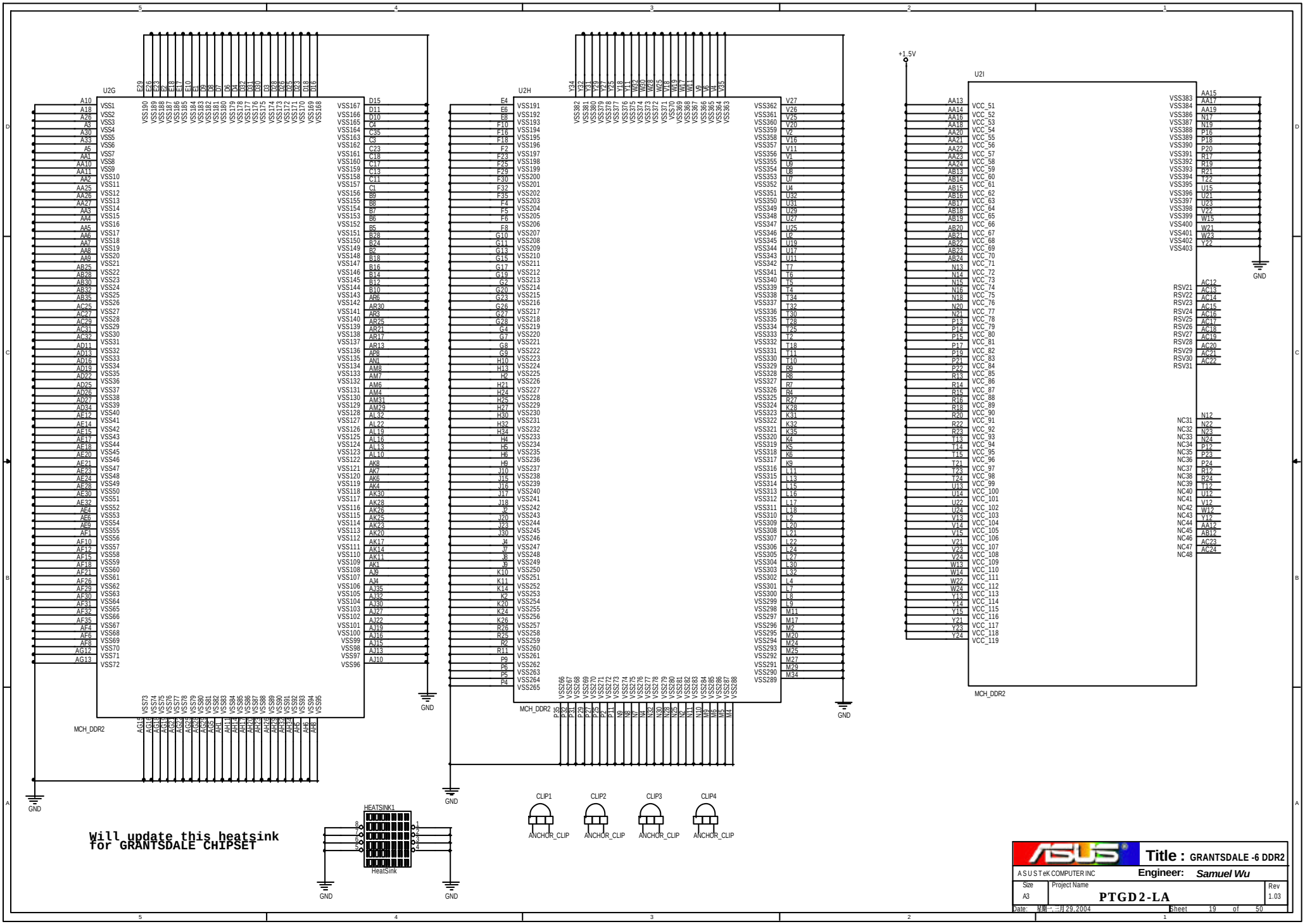


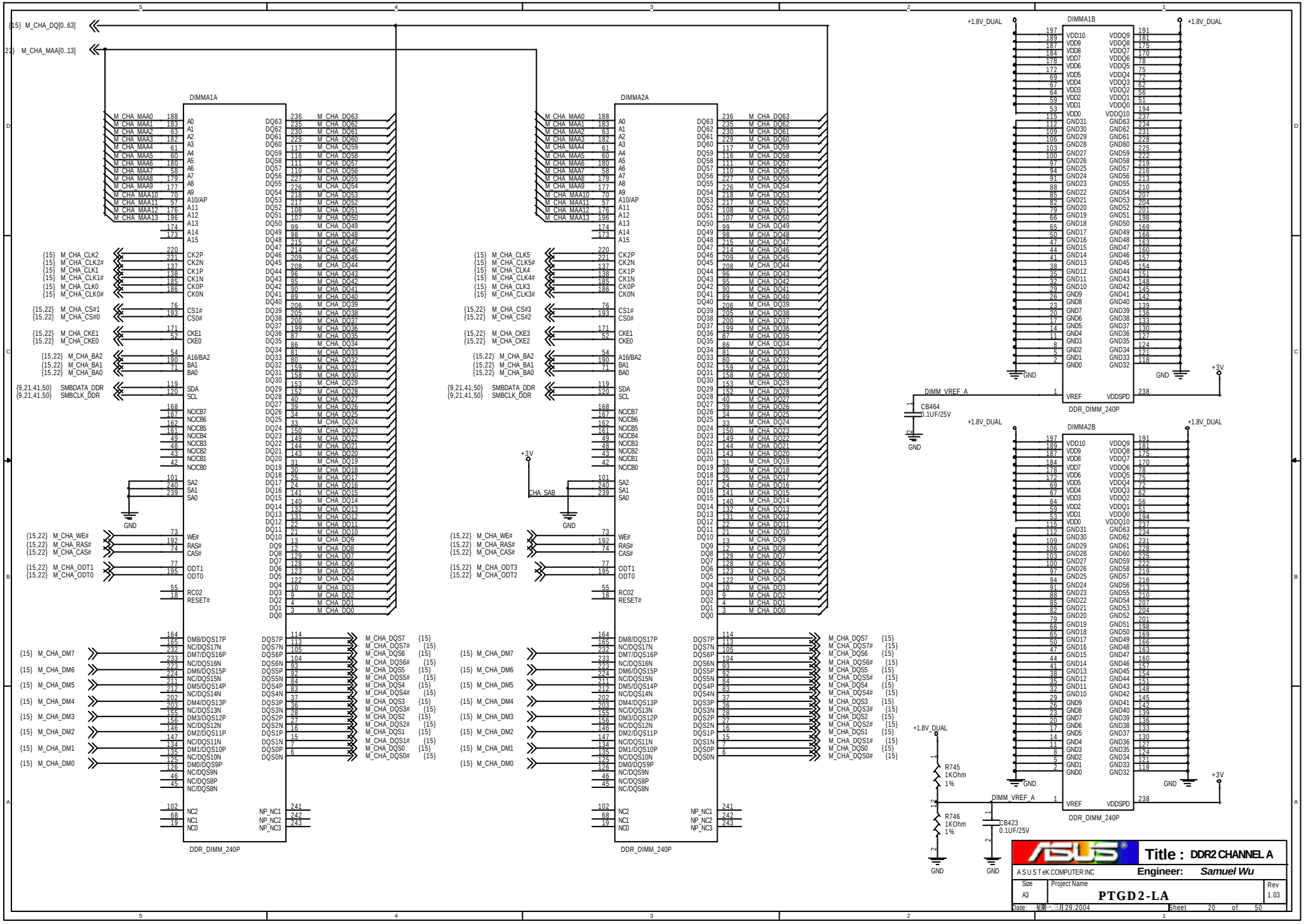


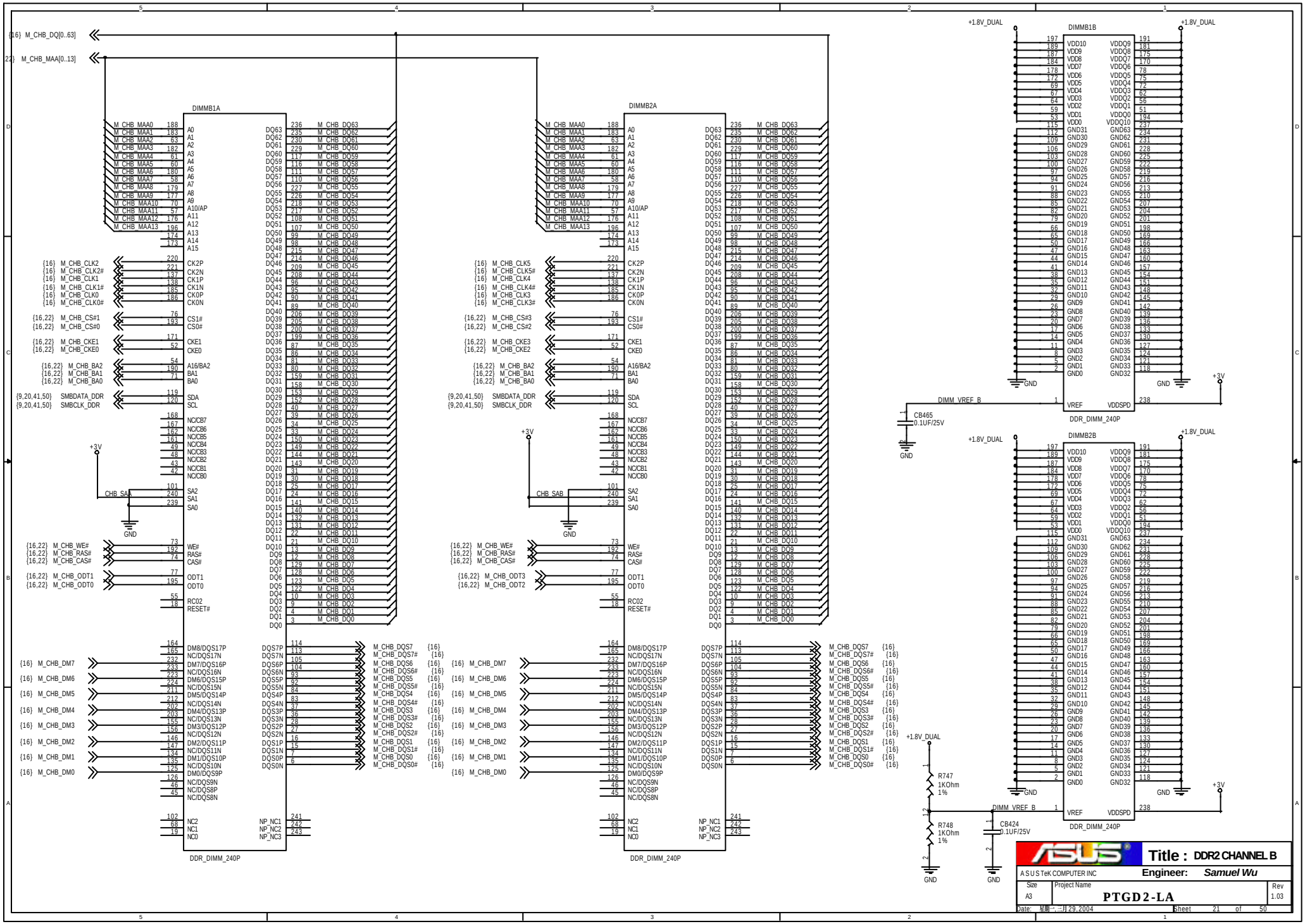


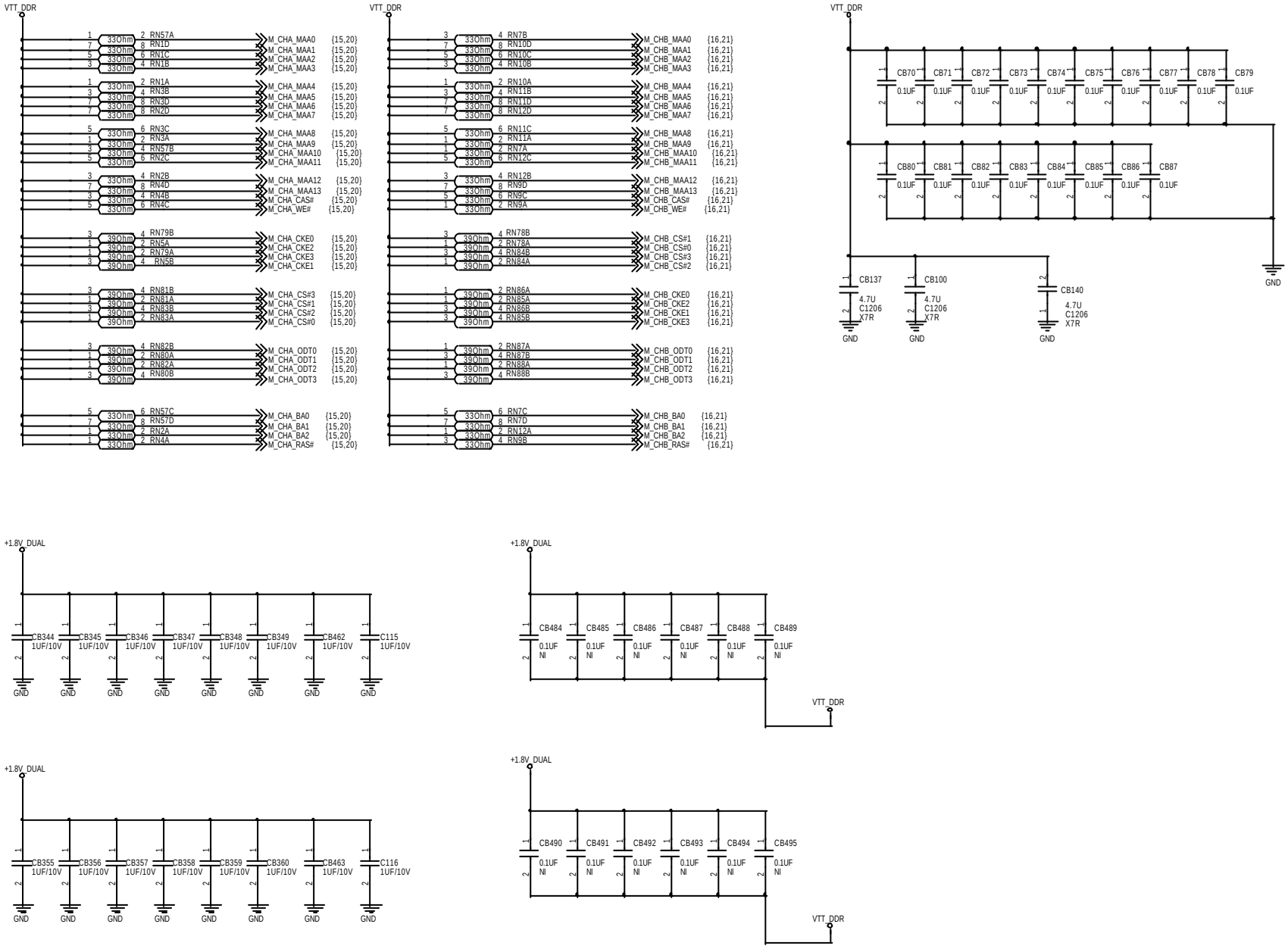


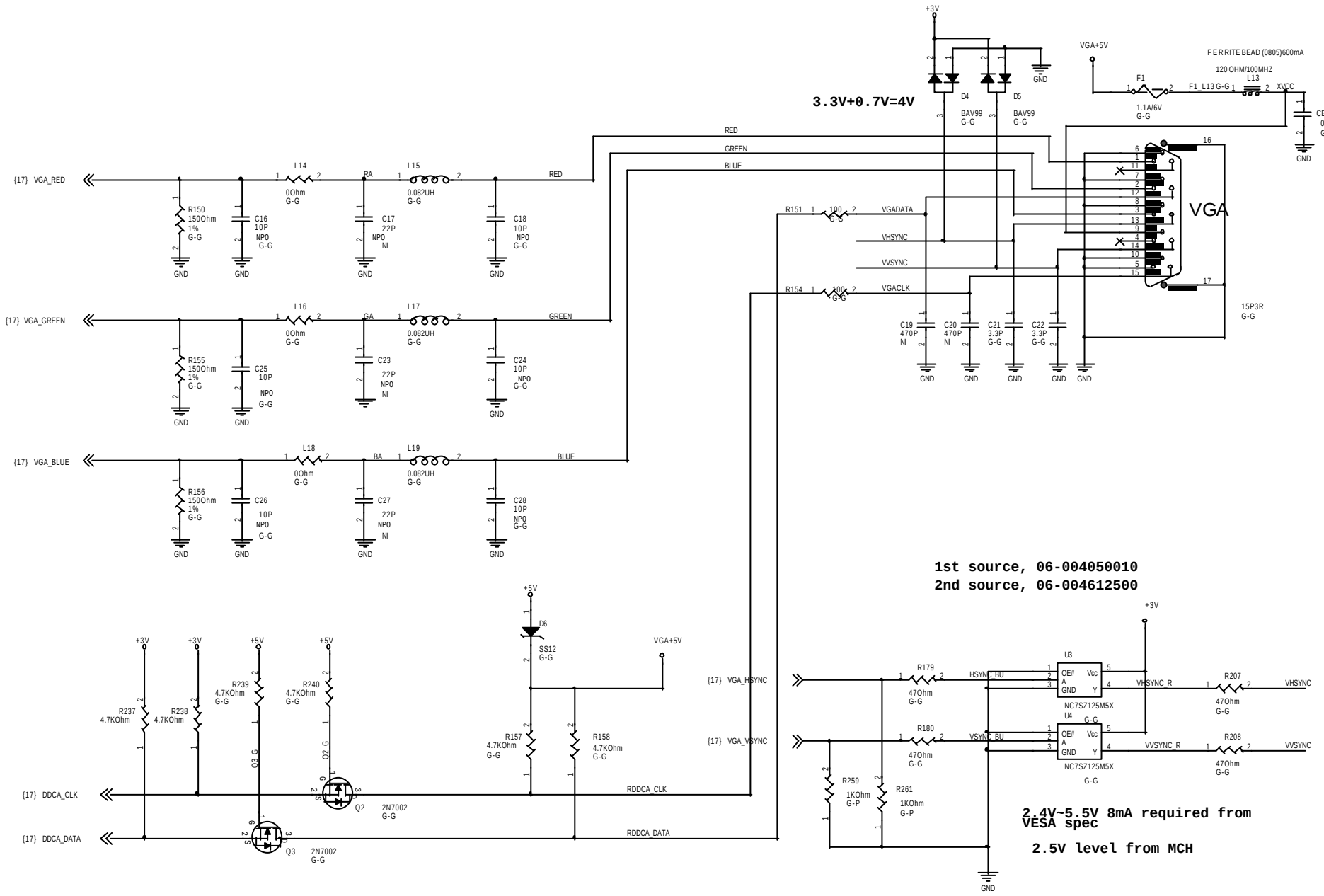


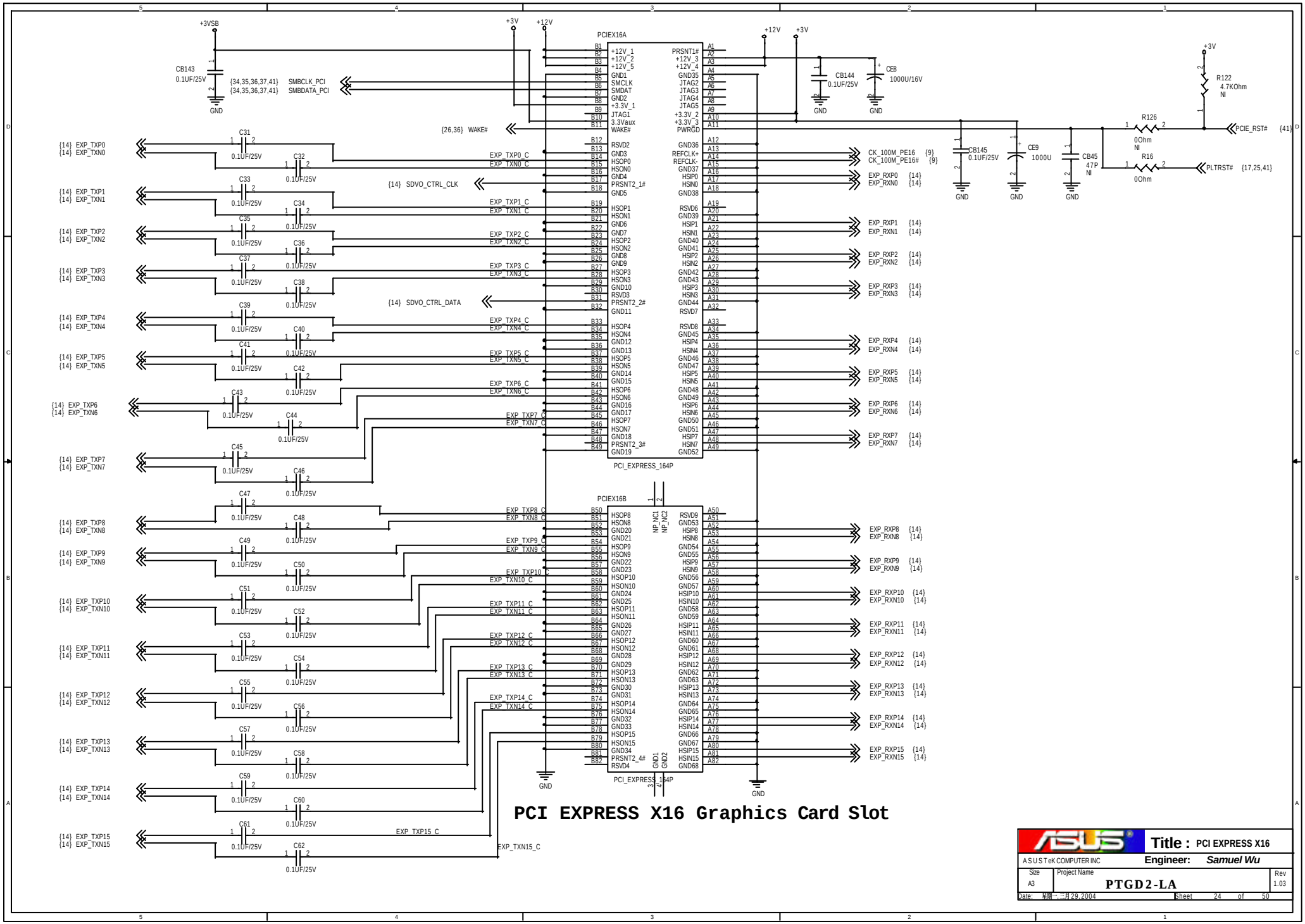


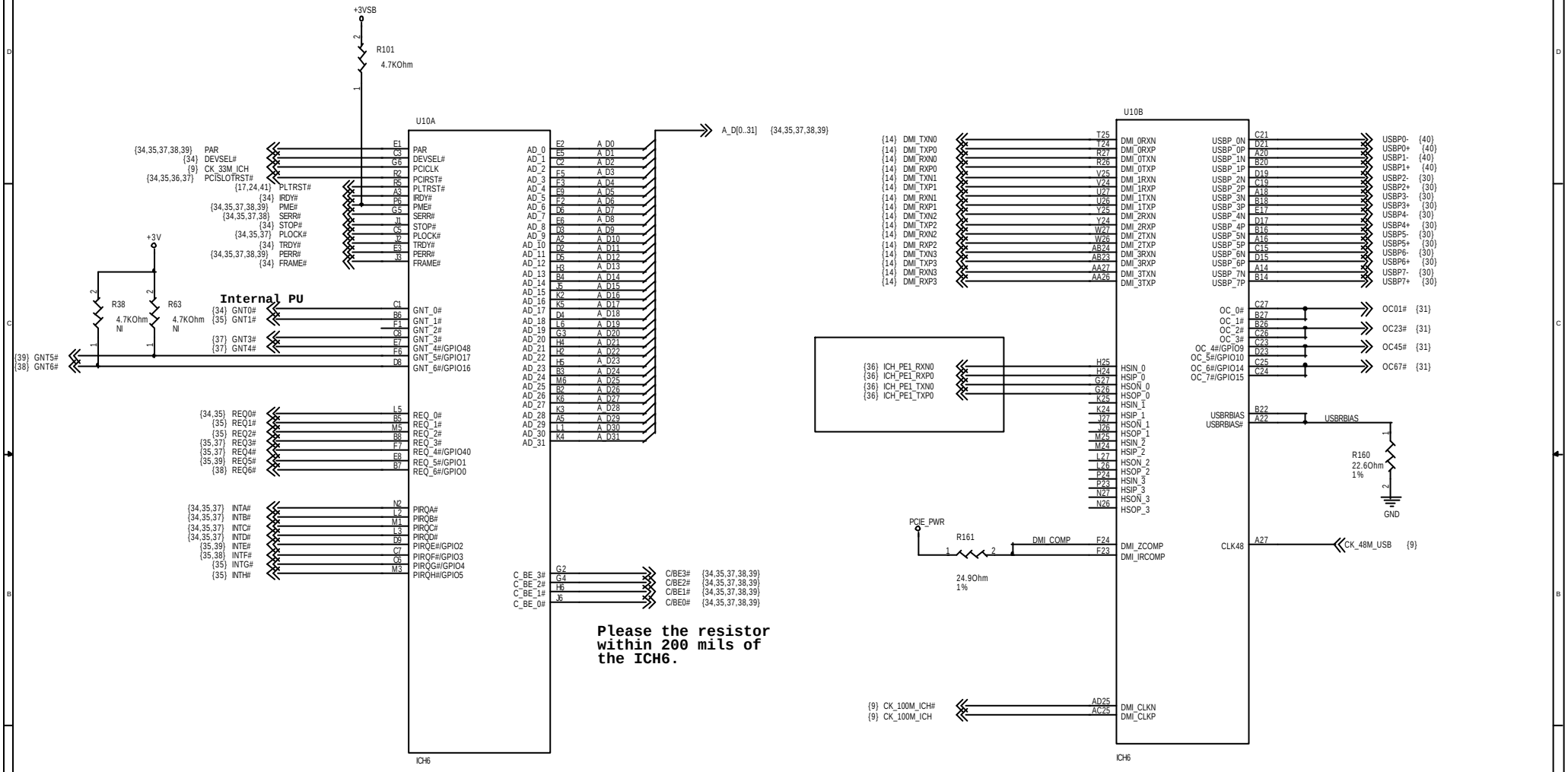




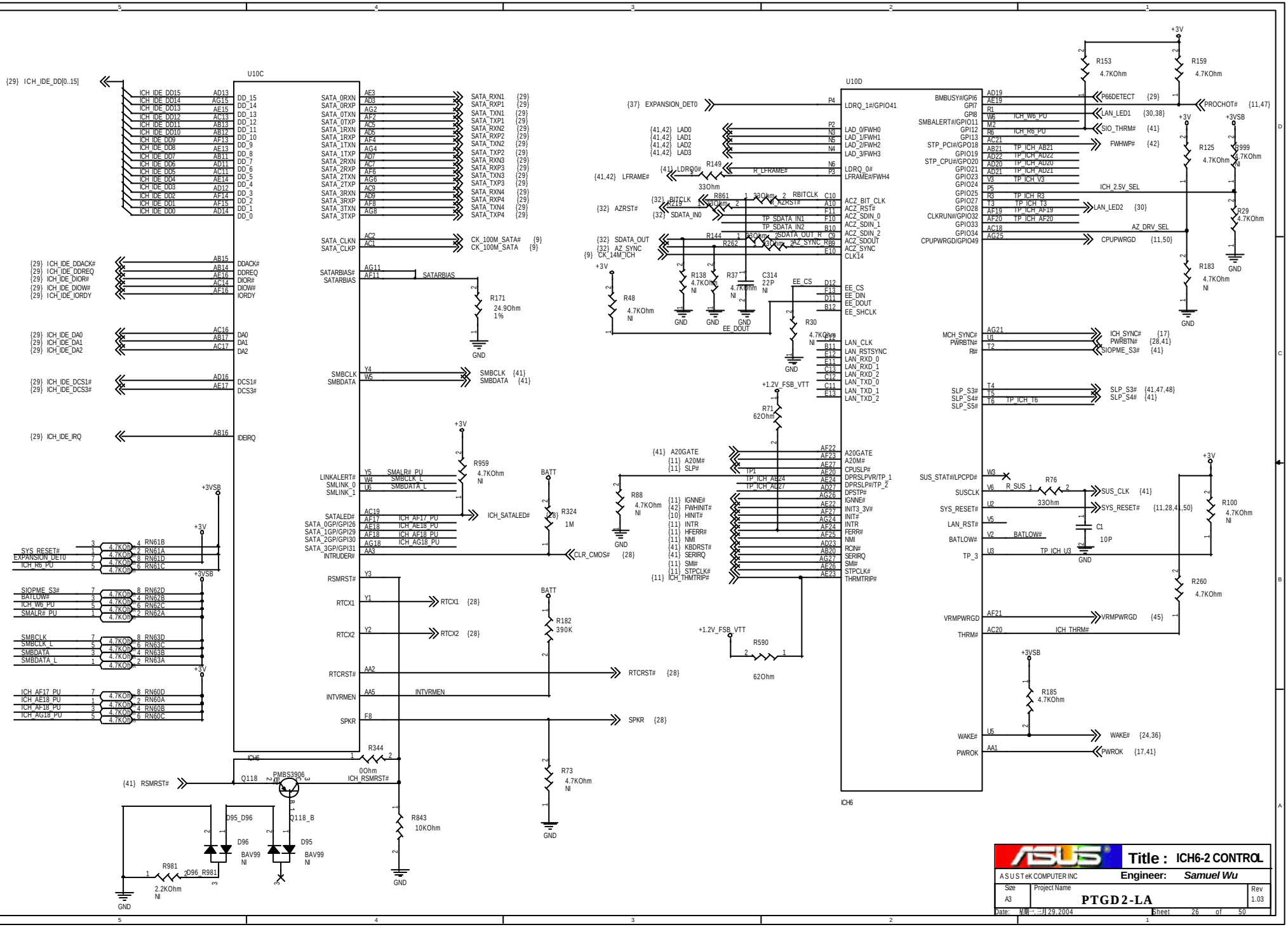




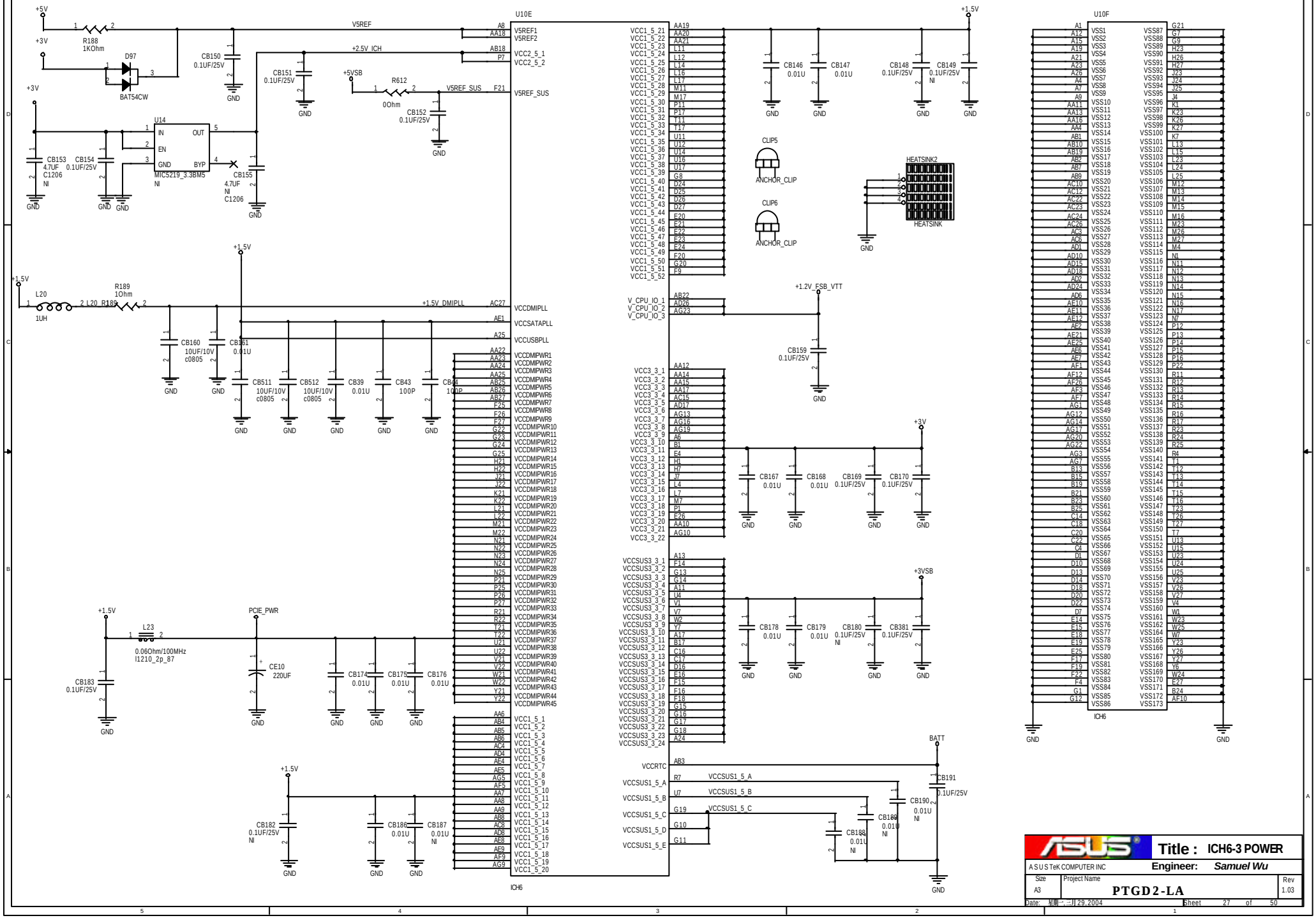




ASUSTeK COMPUTER INC	Title : ICH6-1 CONTROL		
	Engineer: *Samuel Wu*		
Size: A3	Project Name: PTGD2-LA		Rev: 1.03
Date: 星期一, 三月 29, 2004	Sheet 25 of 50		



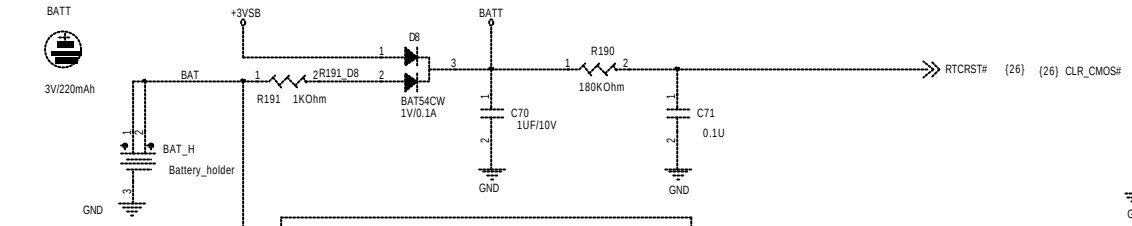
DESIGN NOTE:LEVEL SHIFTING FOR INIT# TO

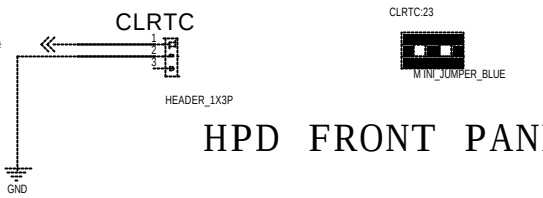


External RTC Circuitry

CLEAR CMOS

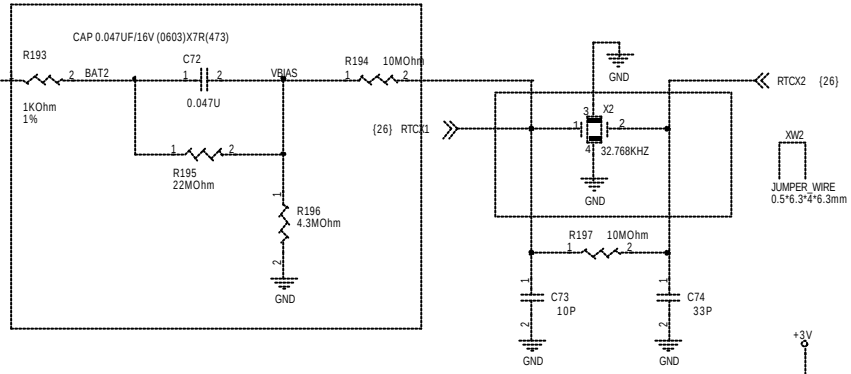
	CMOS DATA
1-2	CLEAR
2-3	Default

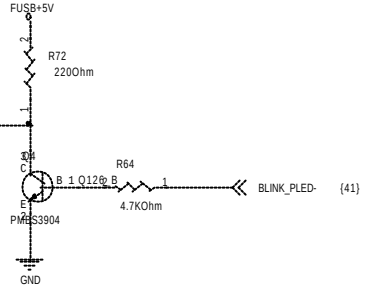




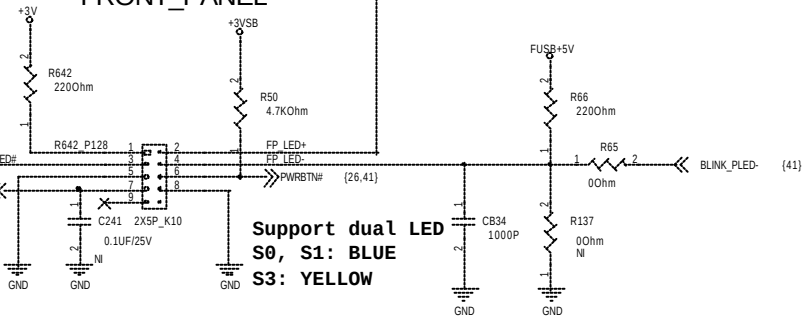
HPD FRONT PANEL

Battery Socket



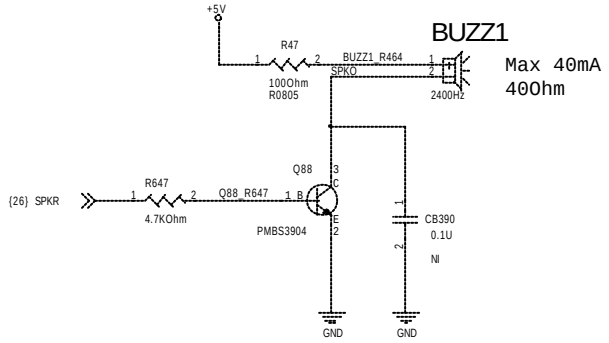


FRONT_PANEL

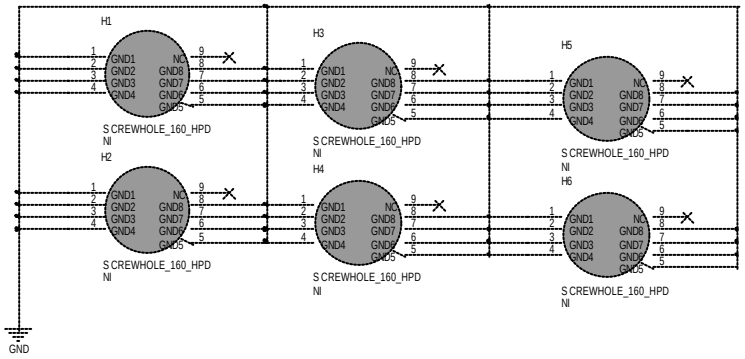


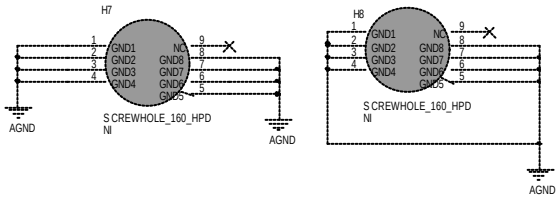
I=5/(100+40)=35.7mA

Internal PU to 3.3V~2.8V



Support dual LED
S0, S1: BLUE
S3: YELLOW





ONLY FOR SCREW HOLE

<Core Design>

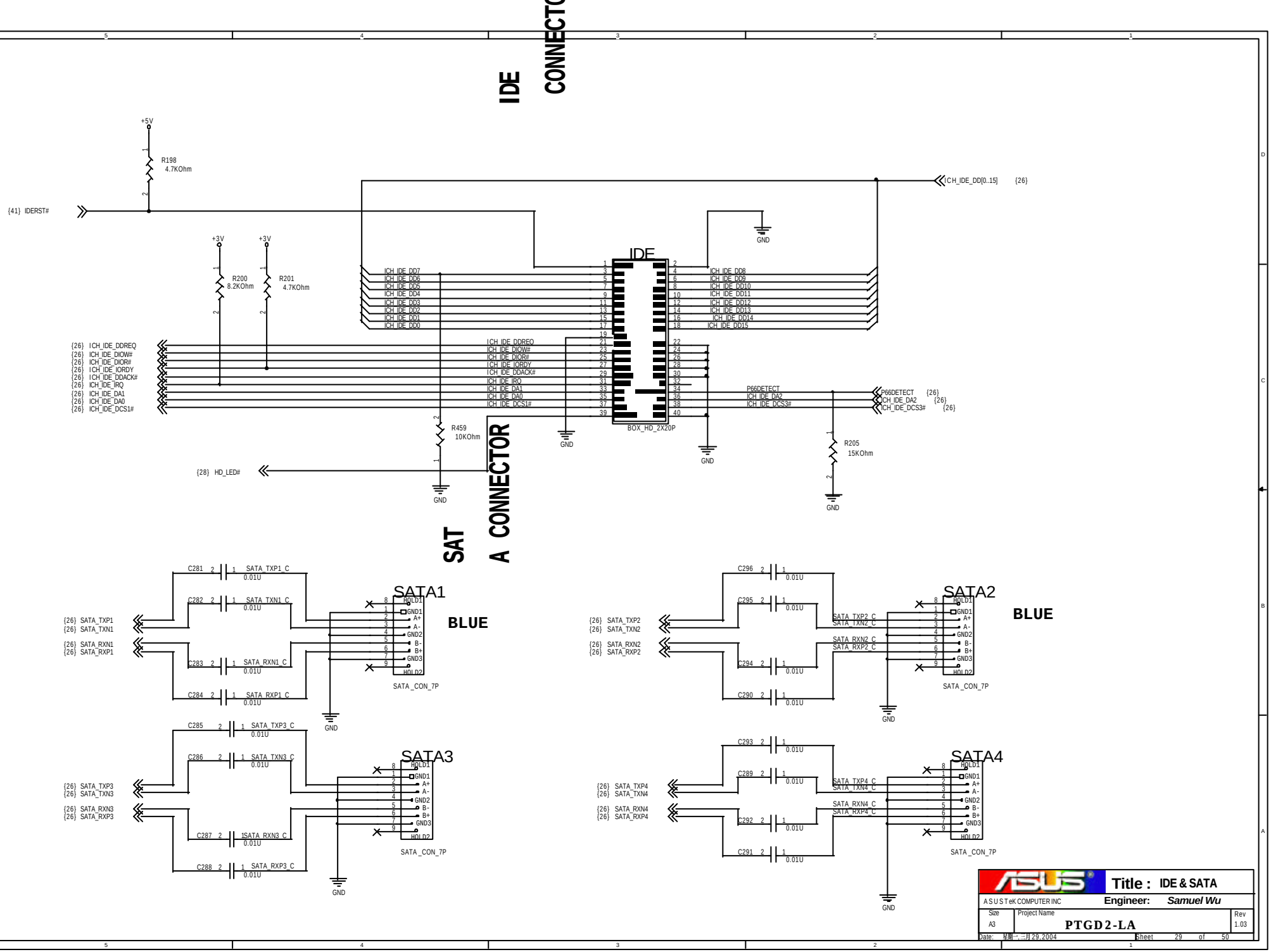
ASUSTeK COMPUTER INC

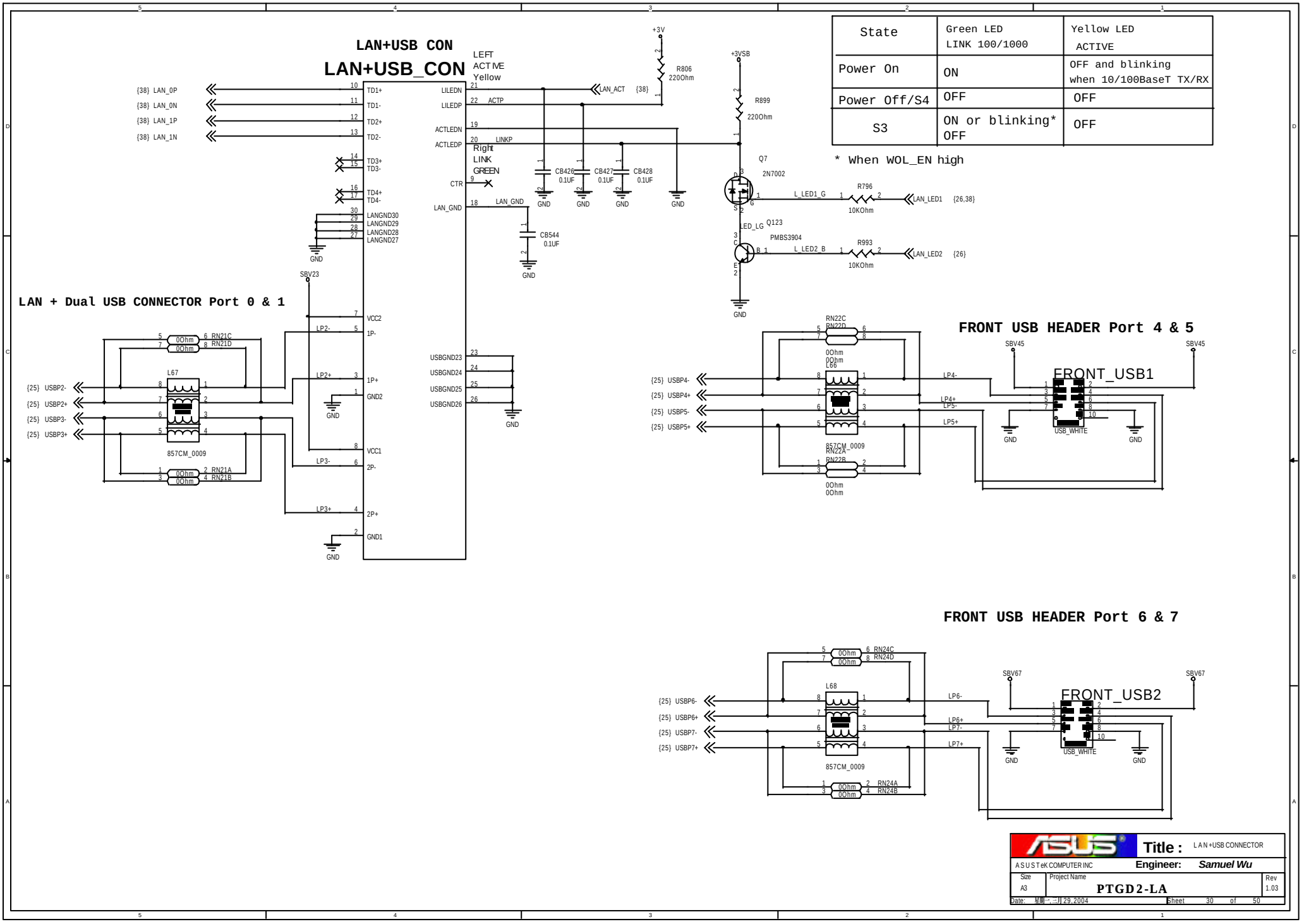
Title :RTC & PANNEL & MH

Engineer: *Samuel Wu*

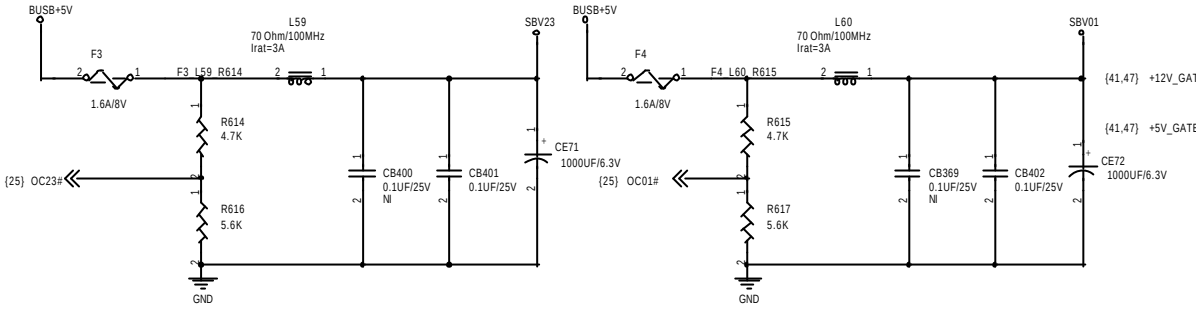
Size	Project Name	Rev
A3	PTGD2-LA	1.03

Date: MM - H 29, 2004 Sheet 28 of 50

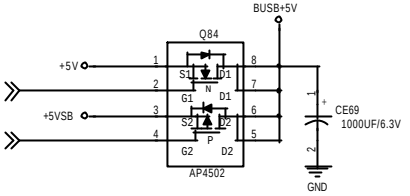




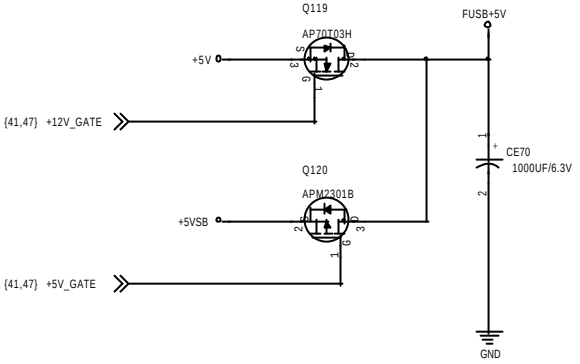
USB POWER CIRCUIT

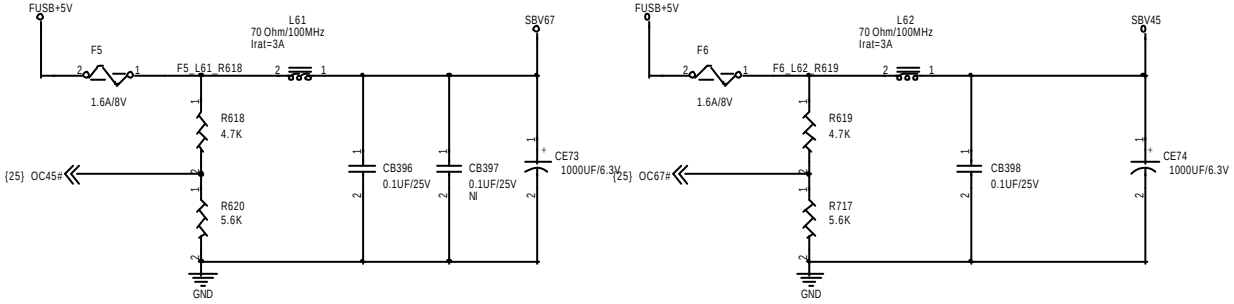


USB POWER OF REAR PORTS



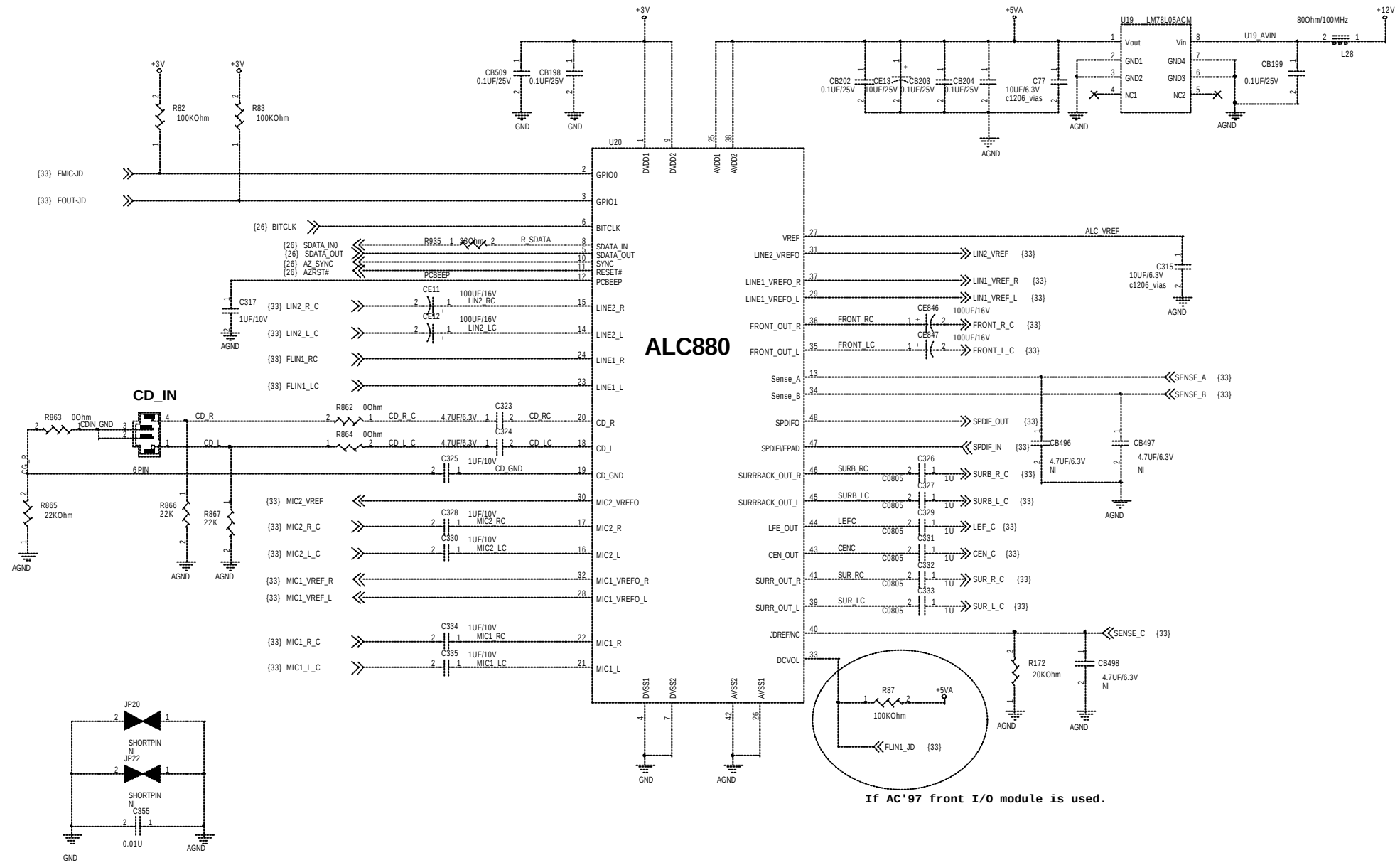
NMOS Suppose to 8.3A
PMOS Suppose to 5.7A



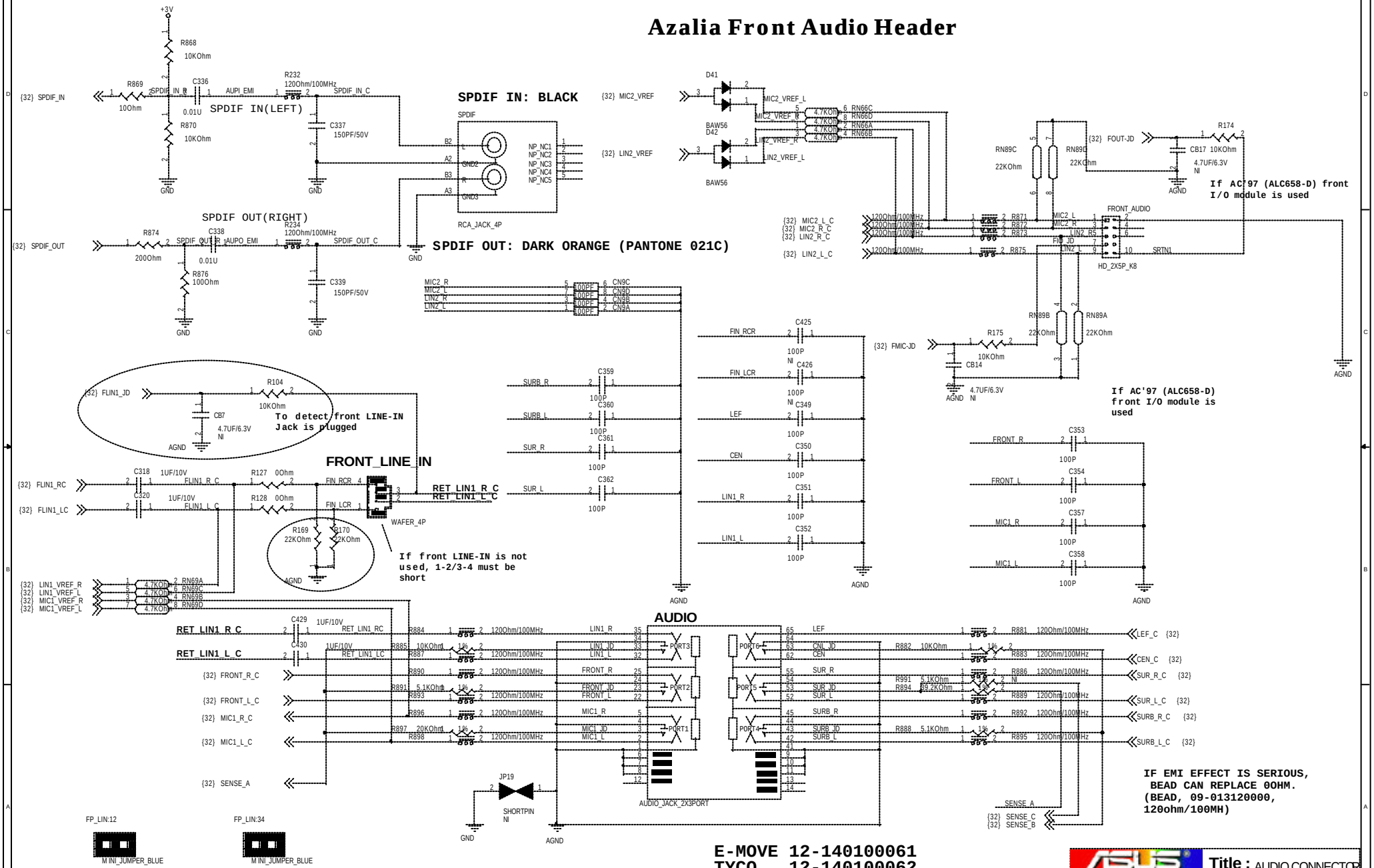


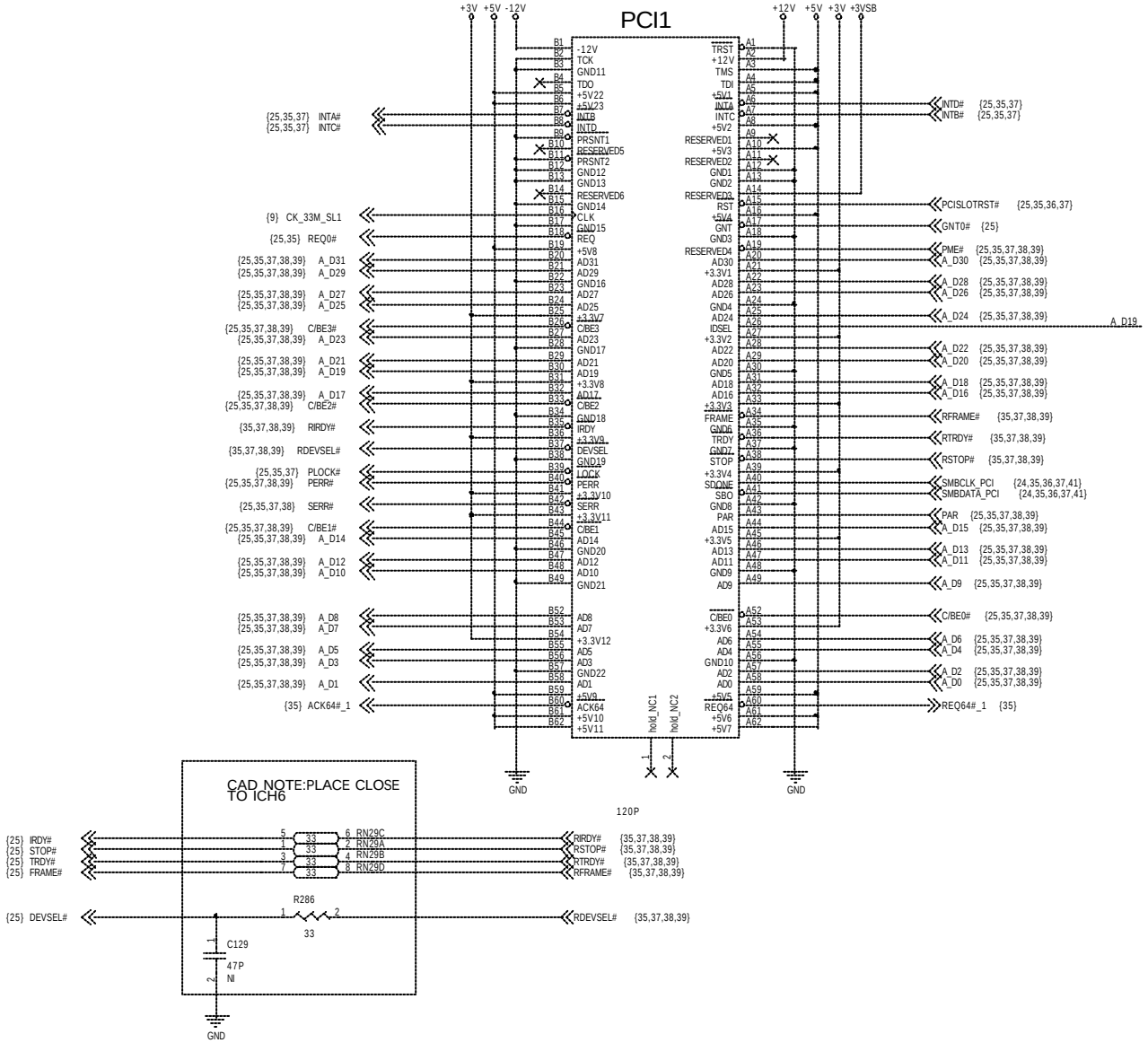
USB POWER OF FRONT I/O PORTS

ASUSTeK COMPUTER INC	Title : USB POWER	
	Engineer: Samuel Wu	
Size: A3	Project Name: PTGD2-LA	Rev: 1.03
Date: 星期一, 三月 29, 2004	Sheet 31 of 50	



Azalia Front Audio Header





DEVICE	REQ#	GNT#	INTERRUPT	ID_SEL
PCI SLOT 1	0	0	DABC	AD_19
PCI SLOT 2	1	1	ABCD	AD_20
NA	**NA**	**NA**	**NA**	**NA**
PCI SLOT 4	**3**	**3**	**DABC**	**AD_22**
PCI SLOT 5	**4**	**4**	**ABCD**	**AD_23**
IEEE 1394	5	5	E	AD_17
LAN	6	6	F	AD_18

```
BUS0:DEVICE 31:Function 0    LPC Controller
BUS0:DEVICE 31:Function 1    IDE Controller
BUS0:DEVICE 31:Function 2    SATA Controller
BUS0:DEVICE 31:Function 3    SMBus Controller

BUS0:DEVICE 30:Function 0    PCI-to-PCI Bridge
BUS0:DEVICE 30:Function 2    AC'97 Audio Controller
BUS0:DEVICE 30:Function 3    AC'97 Modem Controller

BUS0:DEVICE 29:Function 0    USB UHCI Controller #1
BUS0:DEVICE 29:Function 1    USB UHCI Controller #2
BUS0:DEVICE 29:Function 2    USB UHCI Controller #3
BUS0:DEVICE 29:Function 3    USB UHCI Controller #4
BUS0:DEVICE 29:Function 7    USB 2.0 EHCI Controller

BUS0:DEVICE 28:Function 0    PCI Express Port 0
BUS0:DEVICE 28:Function 1    PCI Express Port 1
BUS0:DEVICE 28:Function 2    PCI Express Port 2
BUS0:DEVICE 28:Function 3    PCI Express Port 3

BUS0:DEVICE 27:Function 0    Azalia Controller

BUS1:DEVICE 8:Function 0     LAN Controller
```

SLOT 4 and SLOT 5 are extended card config.

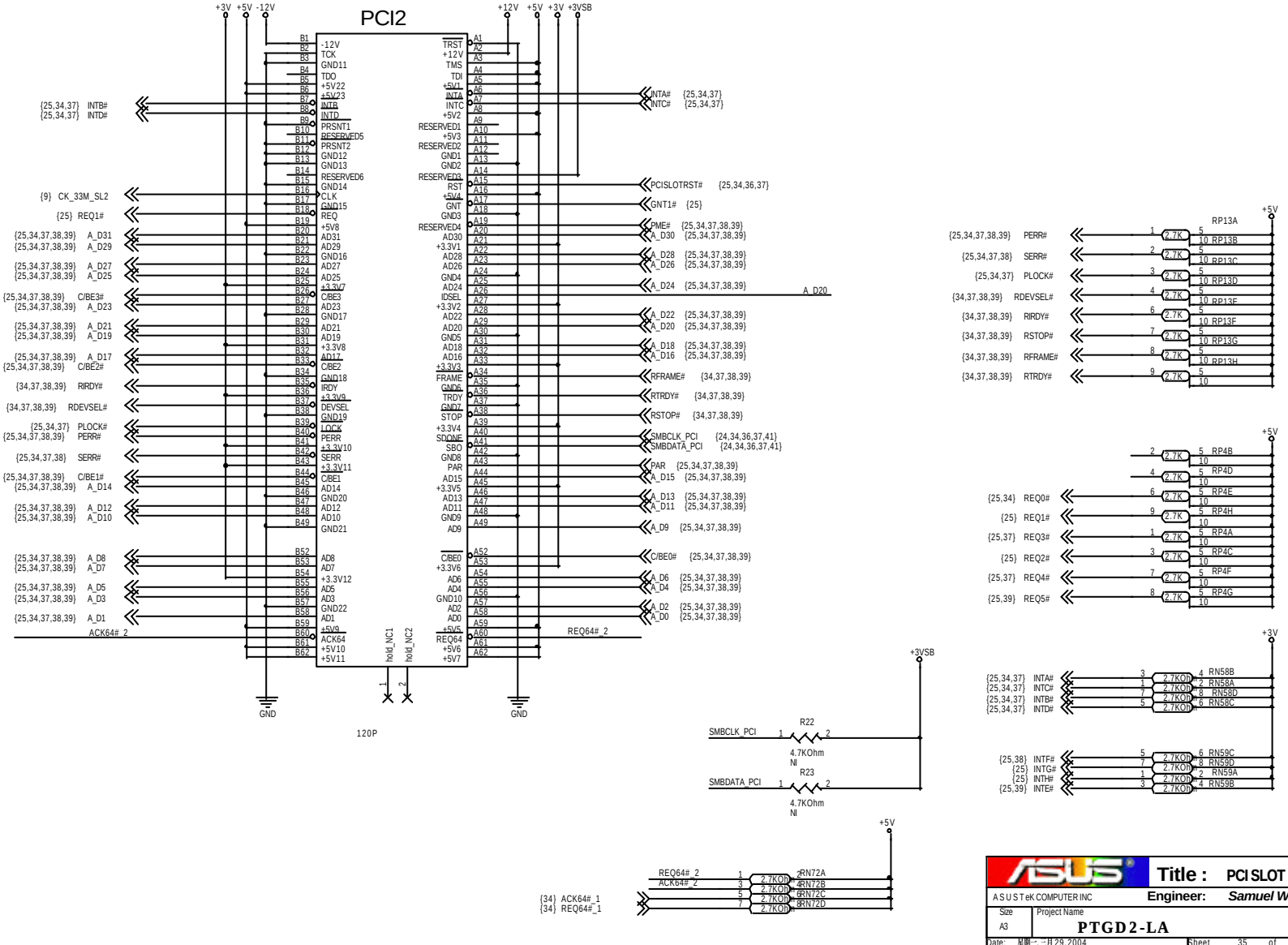
ASUSTeK COMPUTER INC

Title : PCI SLOT 1

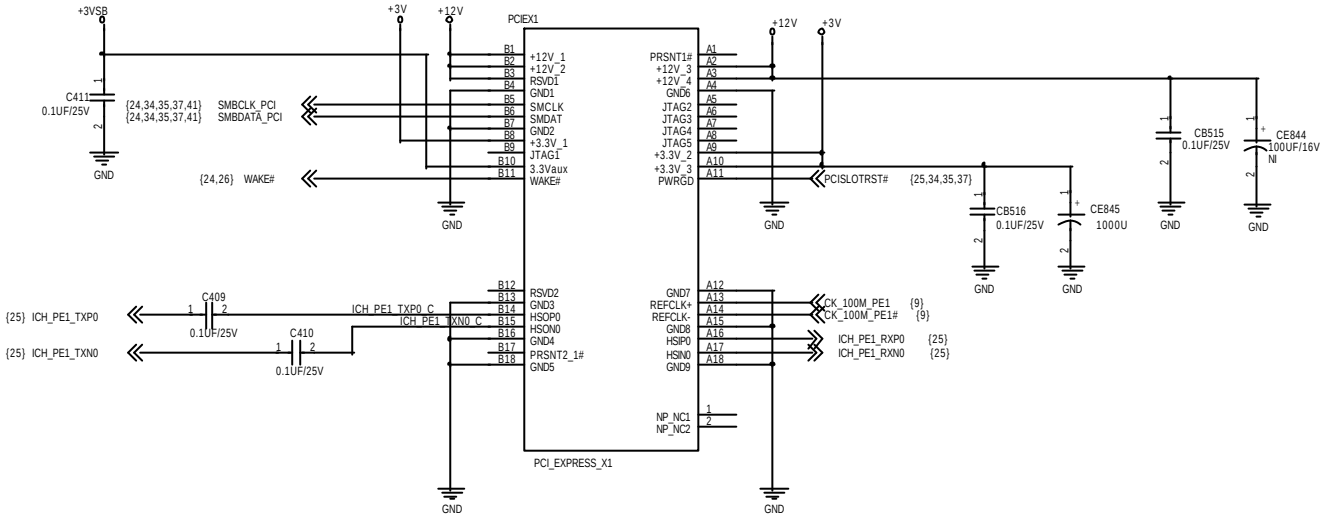
Engineer: *Samuel Wu*

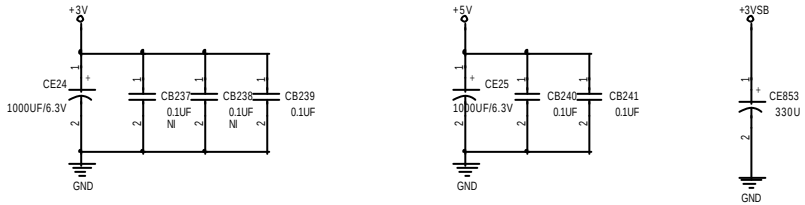
Size	Project Name	Rev
A3	PTGD2-LA	1.03

Date: 星期一, 三月 29, 2004 Sheet 34 of 50



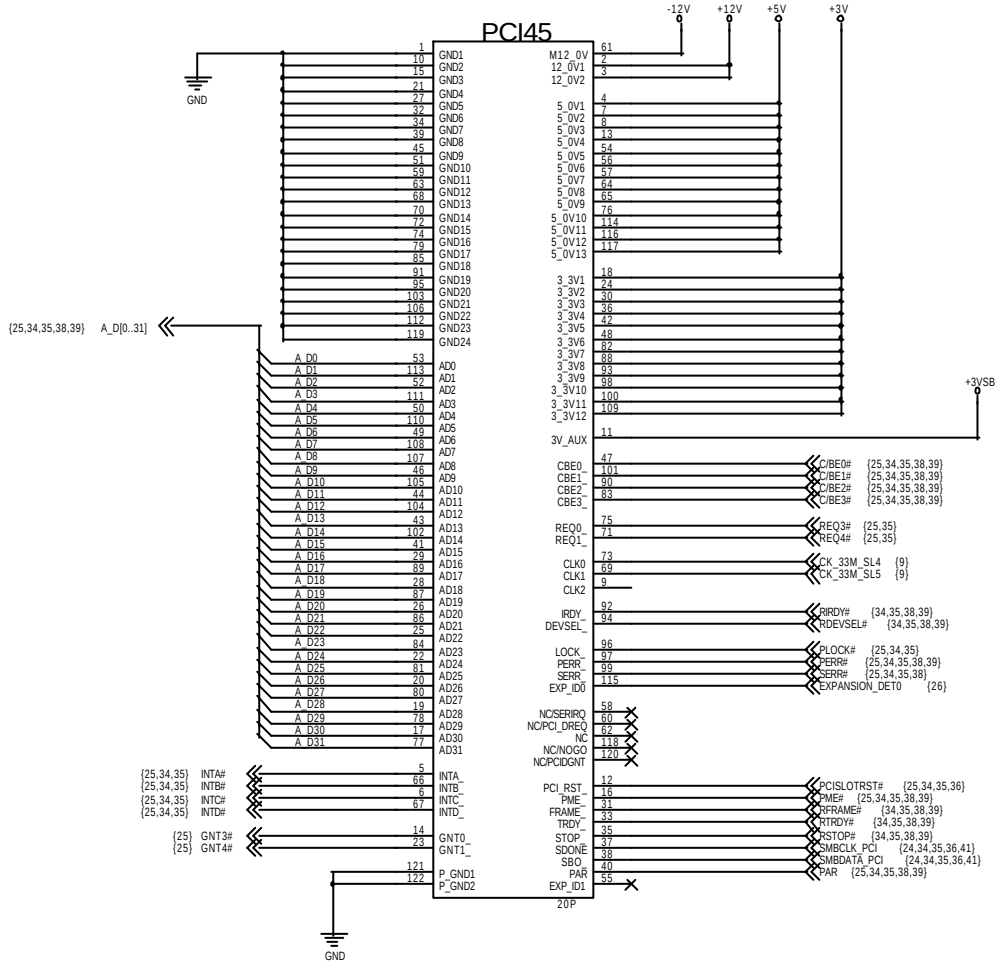
PCIEX1 SLOT CONNECTOR



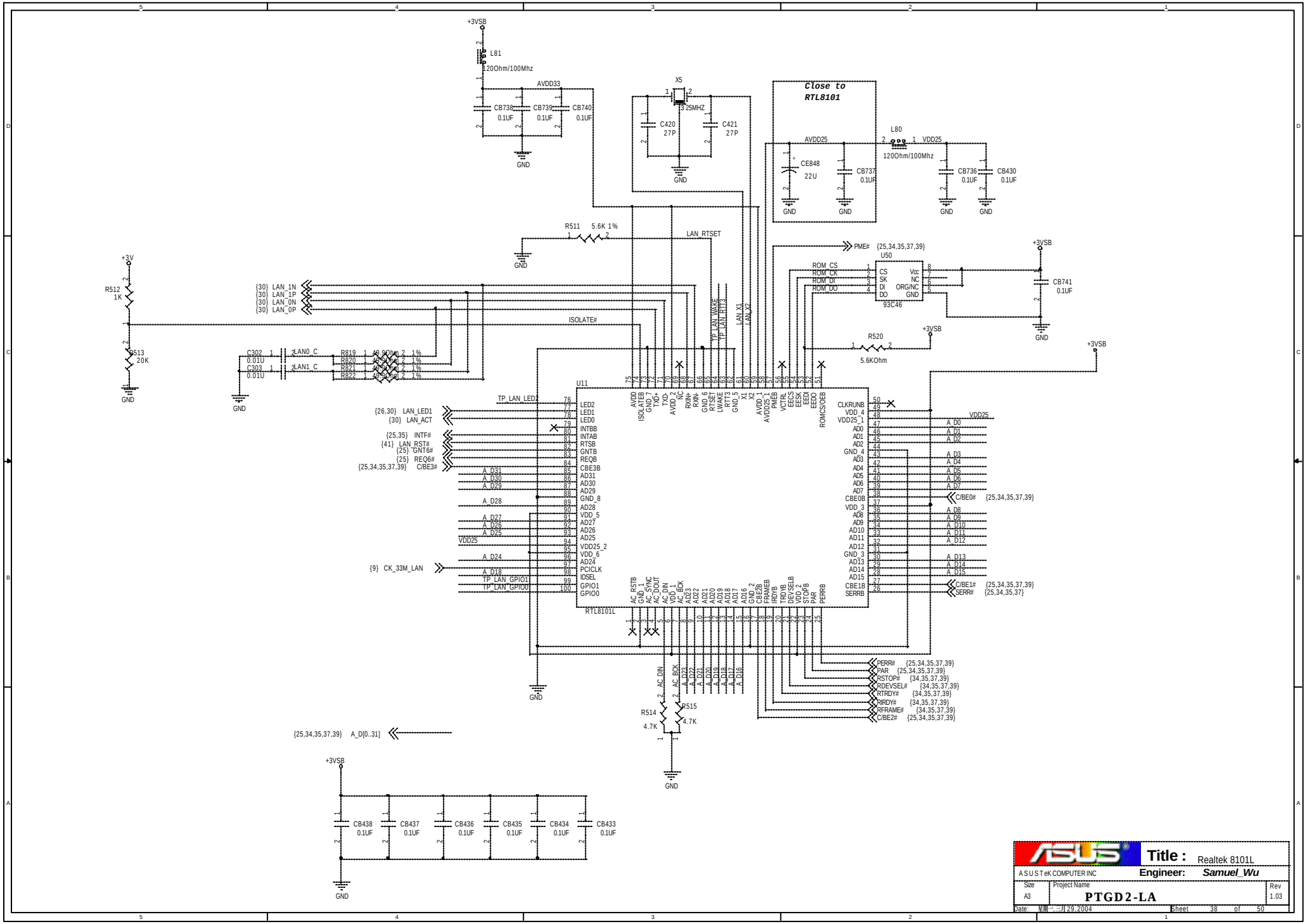


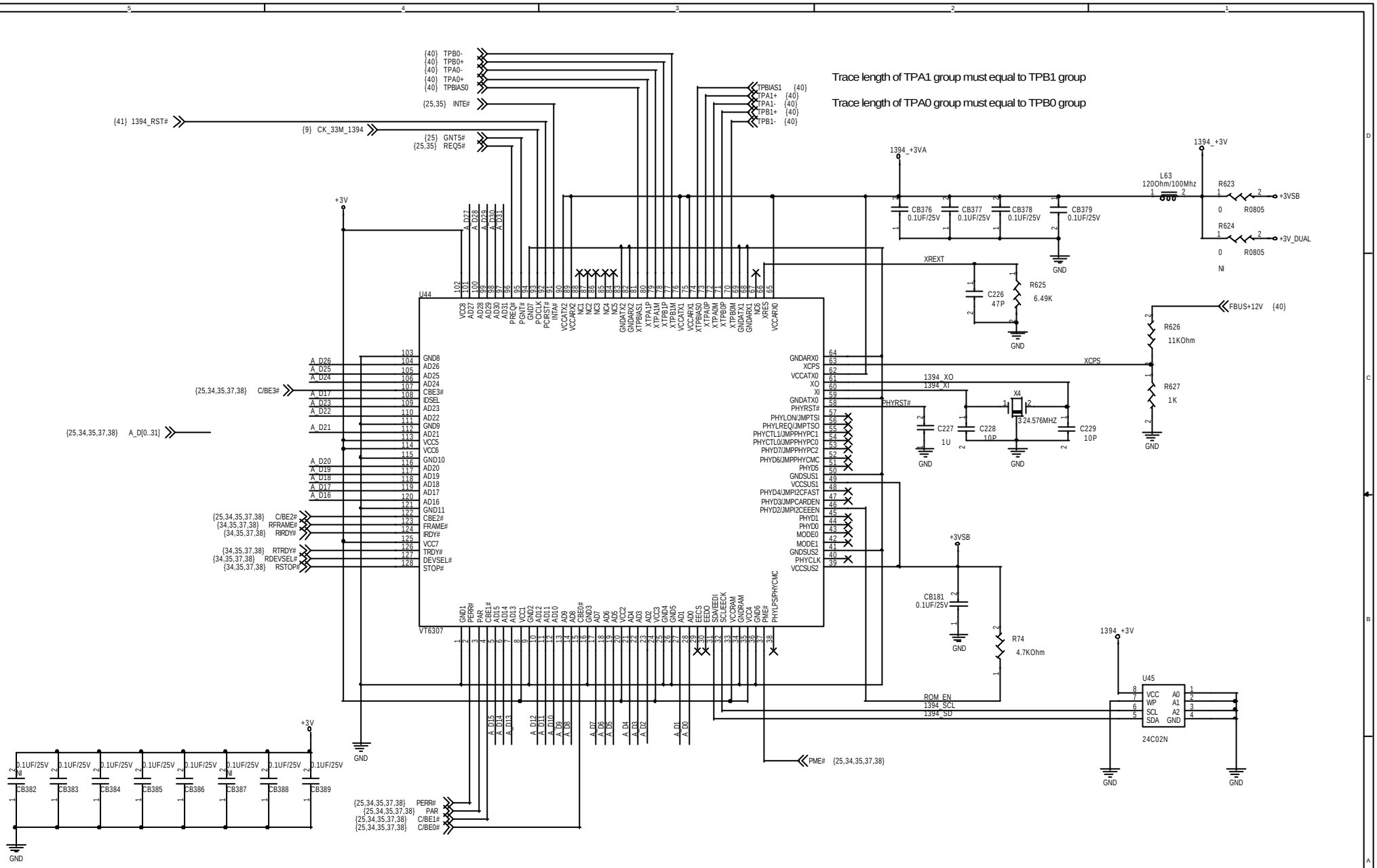
ASUSTeK COMPUTER INC	Title : PCI SLOT 2	
	Engineer: *Samuel Wu*	
Size: A3	Project Name: PTGD2-LA	Rev: 1.03
Date: 星期一, 三月 29, 2004	Sheet 36 of 50	

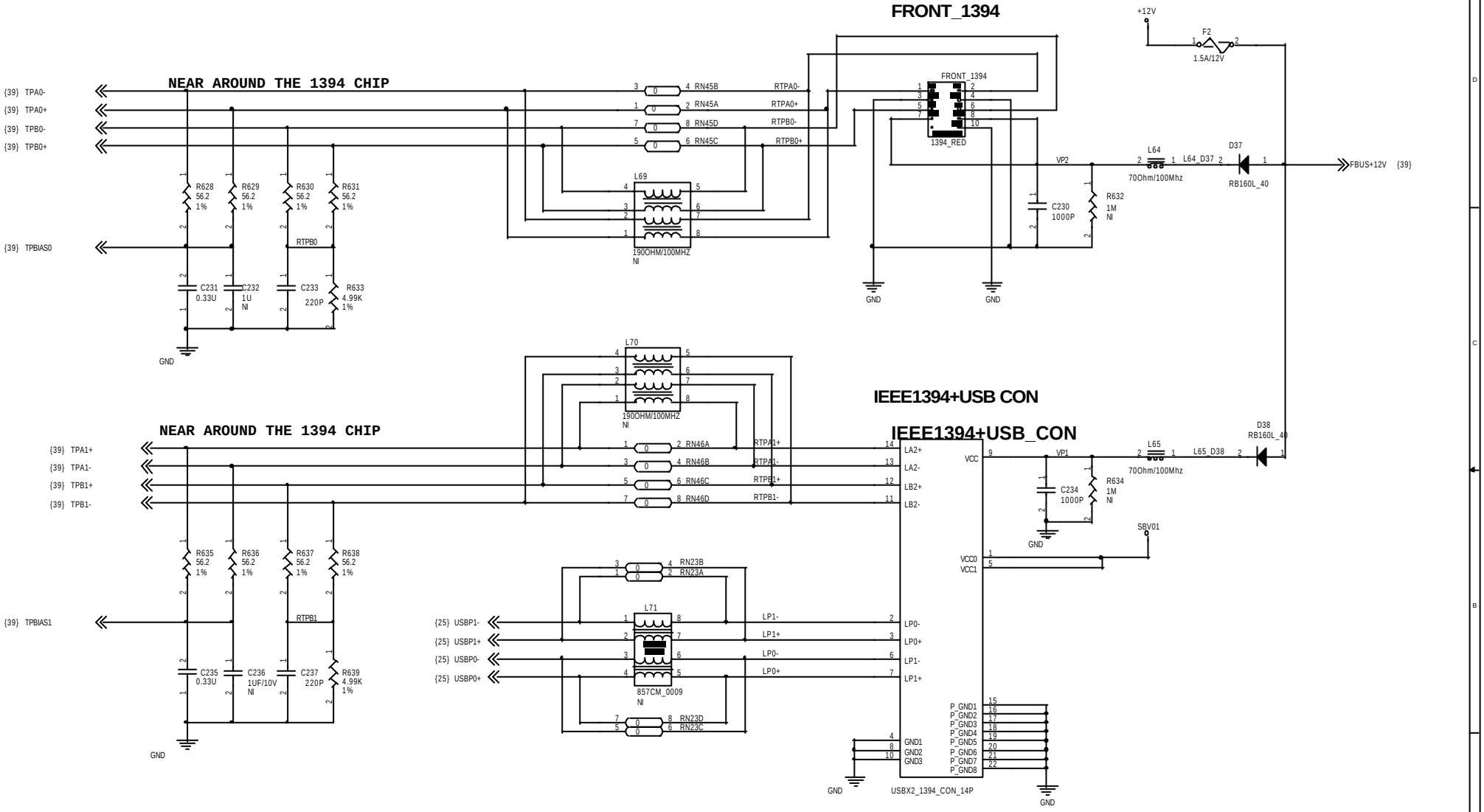
120 PIN EXPANSION RECEPTACLE (FEMALE)



ASUS	Title : EXPANSION RECEPTACLE	
ASUSTeK COMPUTER INC	Engineer: Samuel Wu	
Size: A3	Project Name: PTGD2-LA	Rev: 1.03
Date: 日期二 十一月 29, 2004	Sheet 37 of 50	

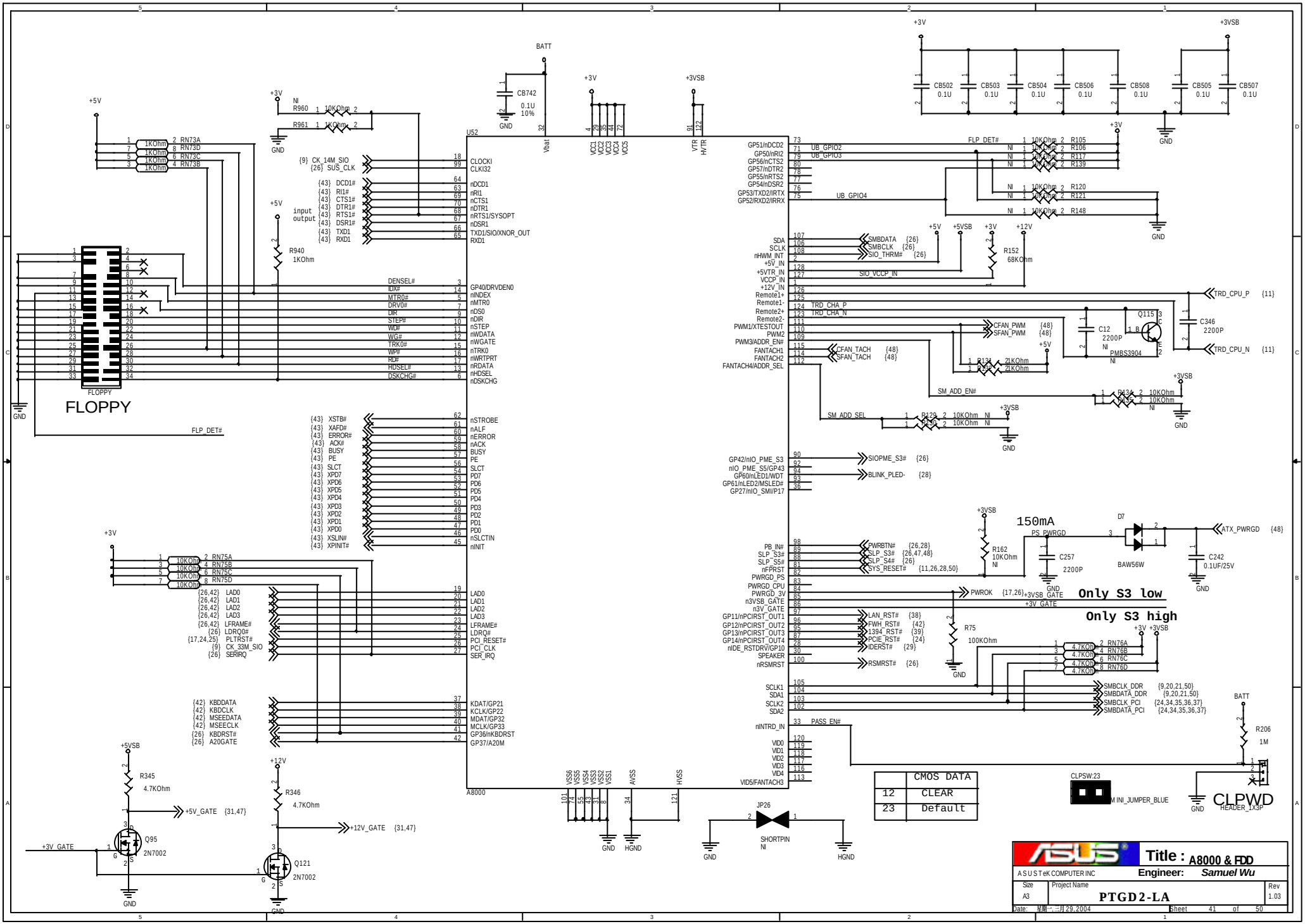




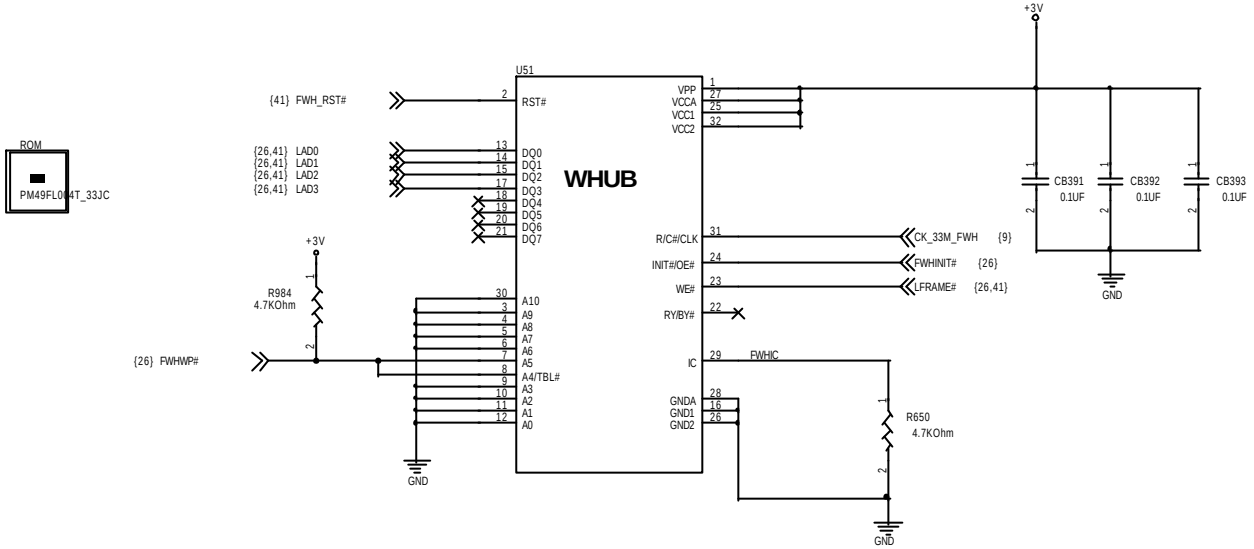


<Core Design>

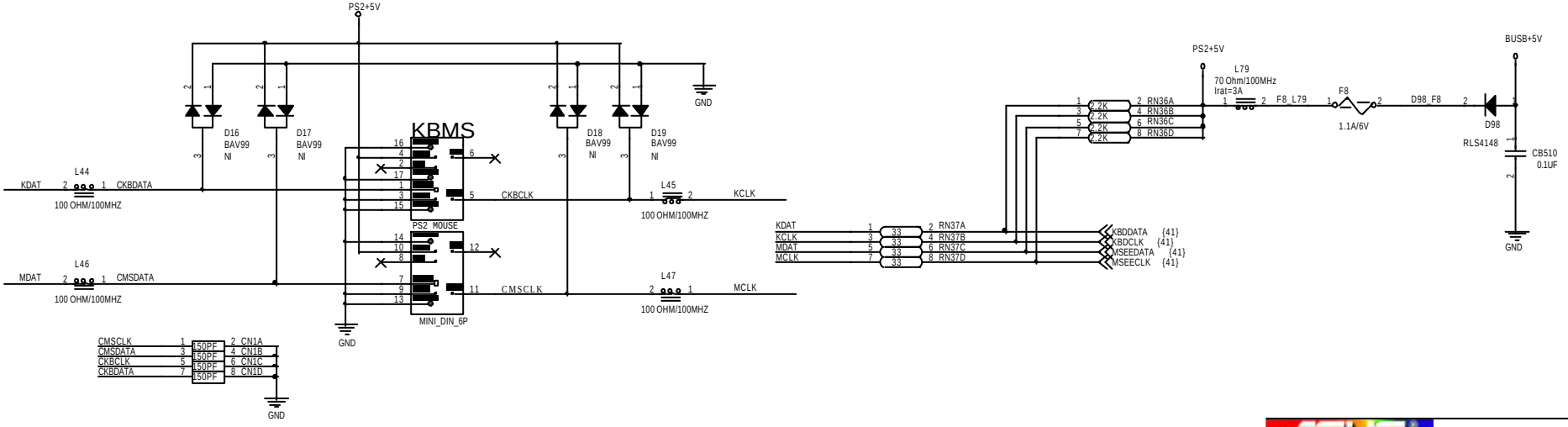
ASUS	Title : 1394 & USB CONNECTOR	
ASUS TeK COMPUTER INC	Engineer: Samuel Wu	
Size: A3	Project Name: PTGD2-LA	Rev: 1.03
Date: 星期一, 二月 29, 2004	Sheet 40 of 50	



FWH BIOS ROM

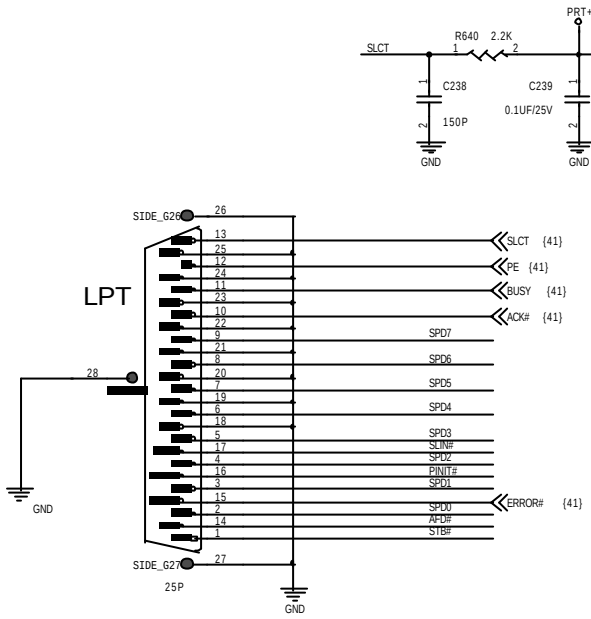


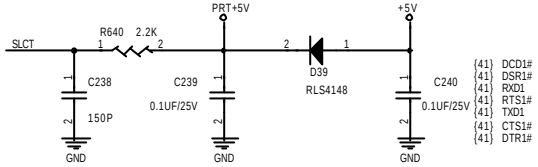
PS/2 KEYBOARD & MOUSE

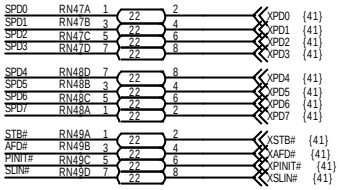


ASUSTeK COMPUTER INC	Title : FWH & KB MS		
	Engineer: *Samuel Wu*		
Size: A3	Project Name: PTGD2-LA		Rev: 1.03
Date: Wednesday, July 28, 2004	Sheet 42 of 50		

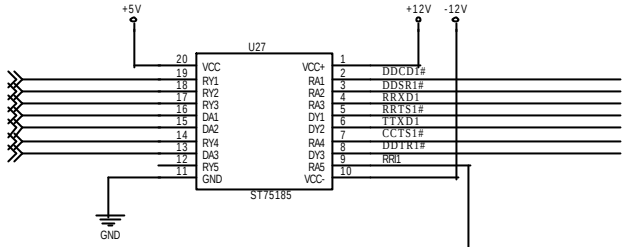
LPT PORT

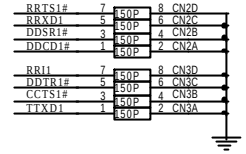


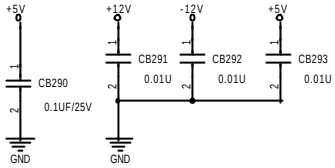


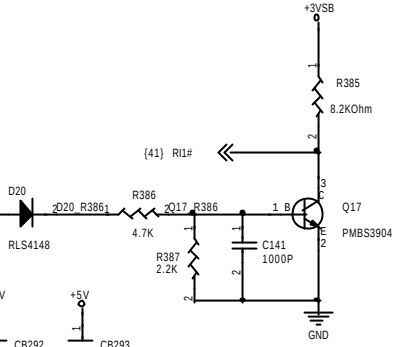


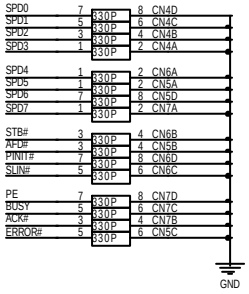
SERIAL PORT

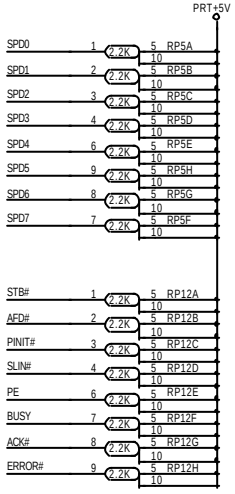




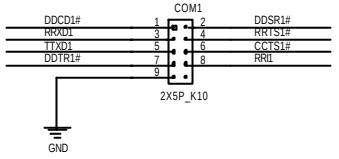




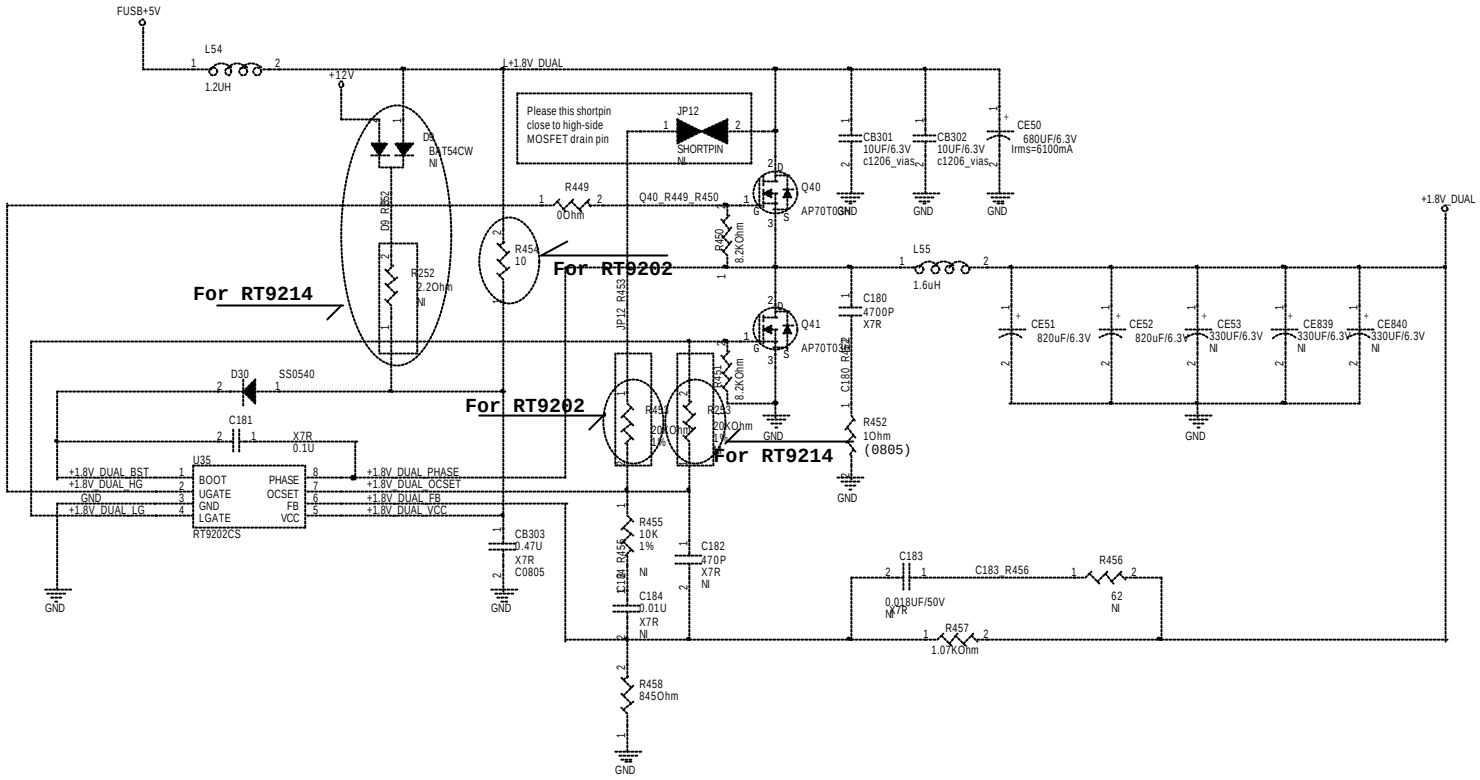




Using floating COM port for HPD

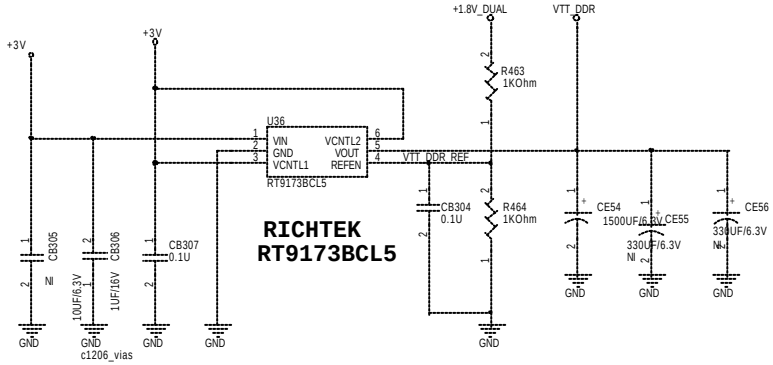


ASUSTeK COMPUTER INC	Title : Serial & Paralle Port		
	Engineer: Samuel Wu		
Size: A3	Project Name: PTGD2-LA		Rev: 1.03
Date: Wednesday, April 28, 2004	Sheet 43 of 50		



CAE NOTE: PROVIDE 1.2cm x 1.2cm COPPER PAD

FOR DPAK(TO252) LET Tja OF 20C/W FOR 1.2A ON DDR VTT



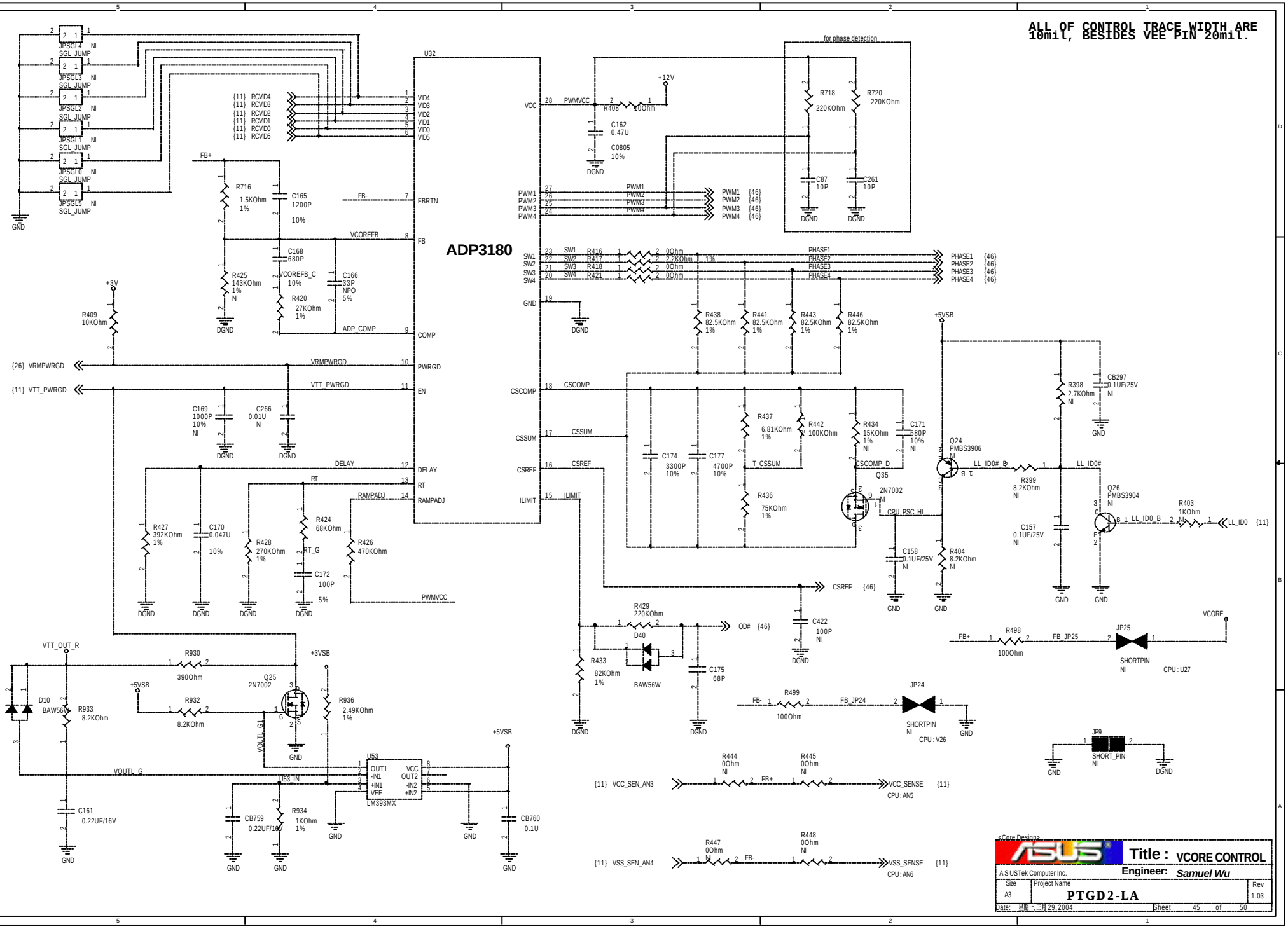
<Core Design>

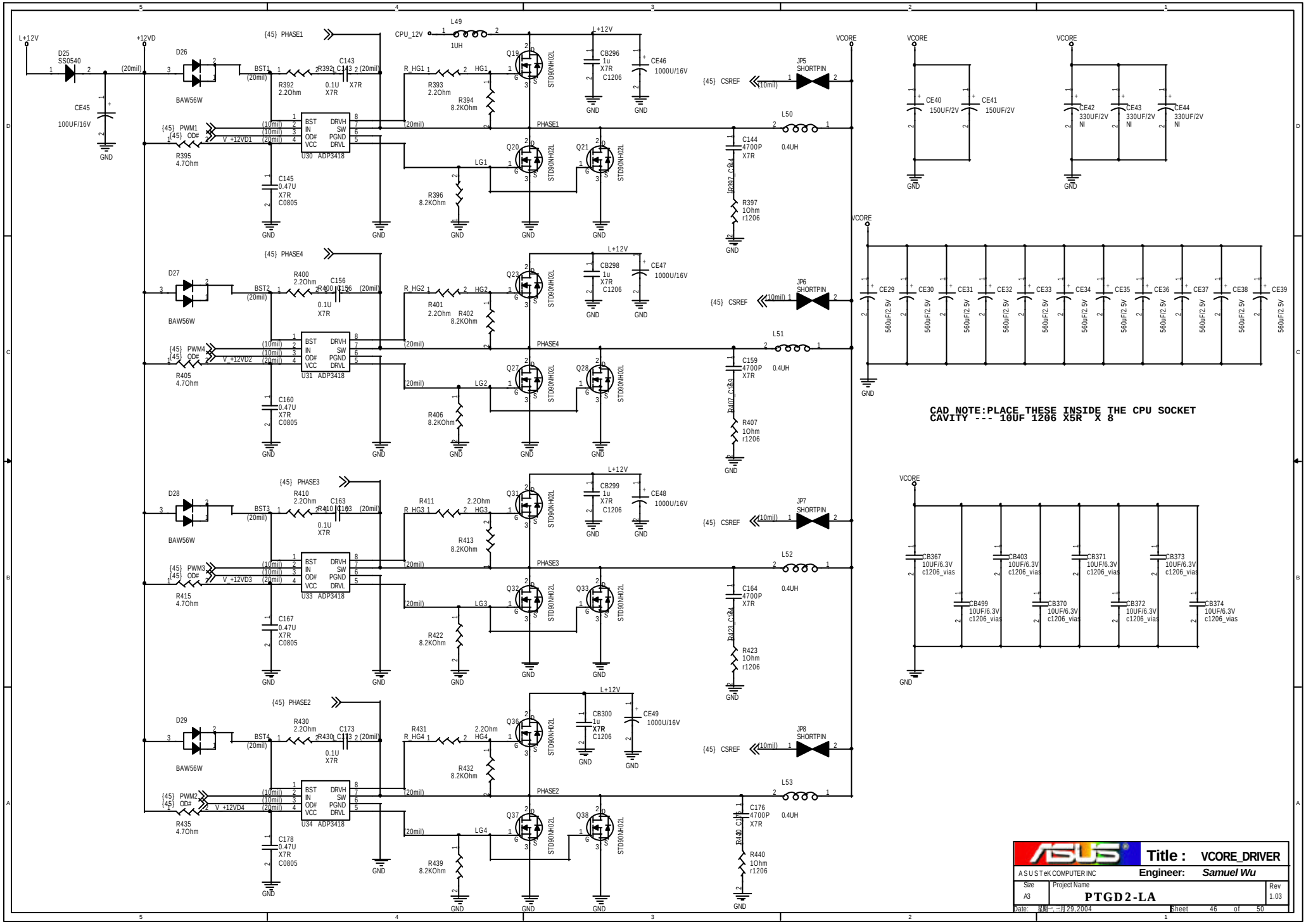
Title : DDR-DUAL, +1.8_DUAL

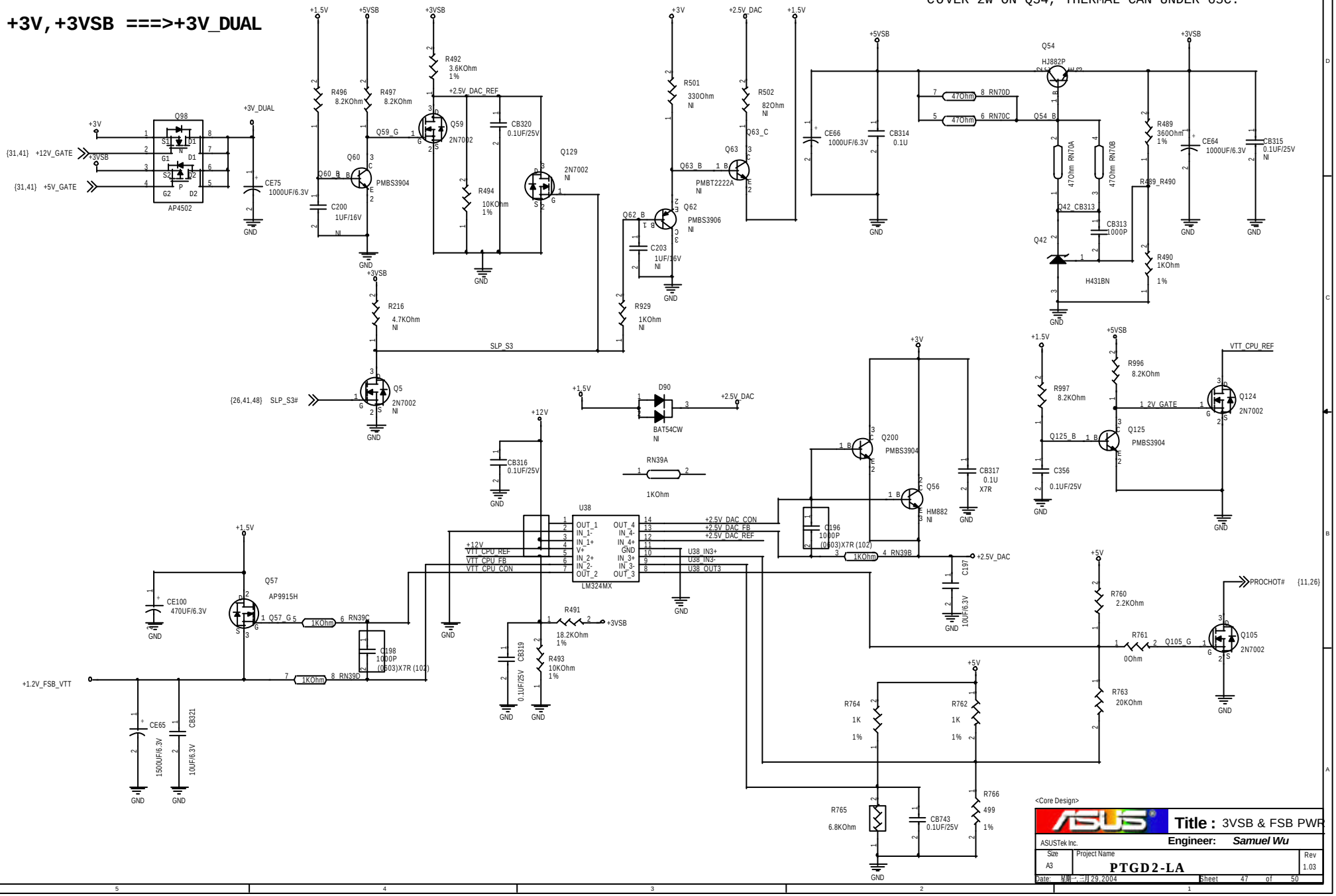
ASUSTek Inc. Engineer: Samuel Wu

Size	Project Name	Rev
A3	PTGD2-LA	1.03

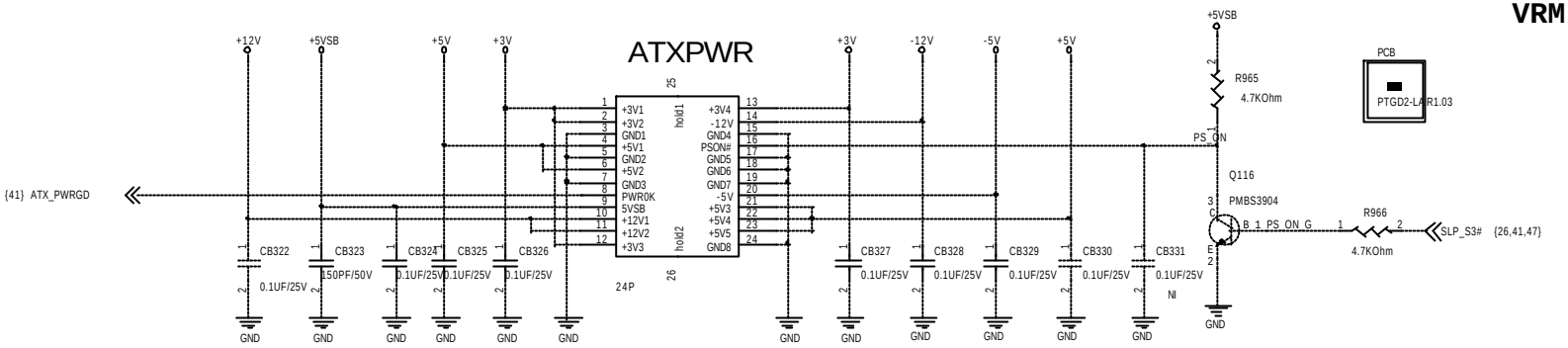
Date: 星期一, 三月 29, 2004 Sheet 44 of 50



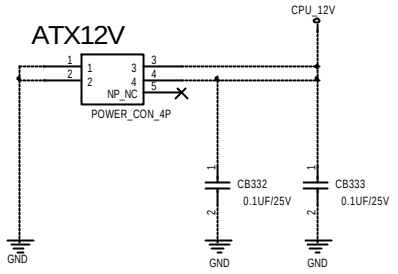




ATX POWER SUPPLY CONNECTOR

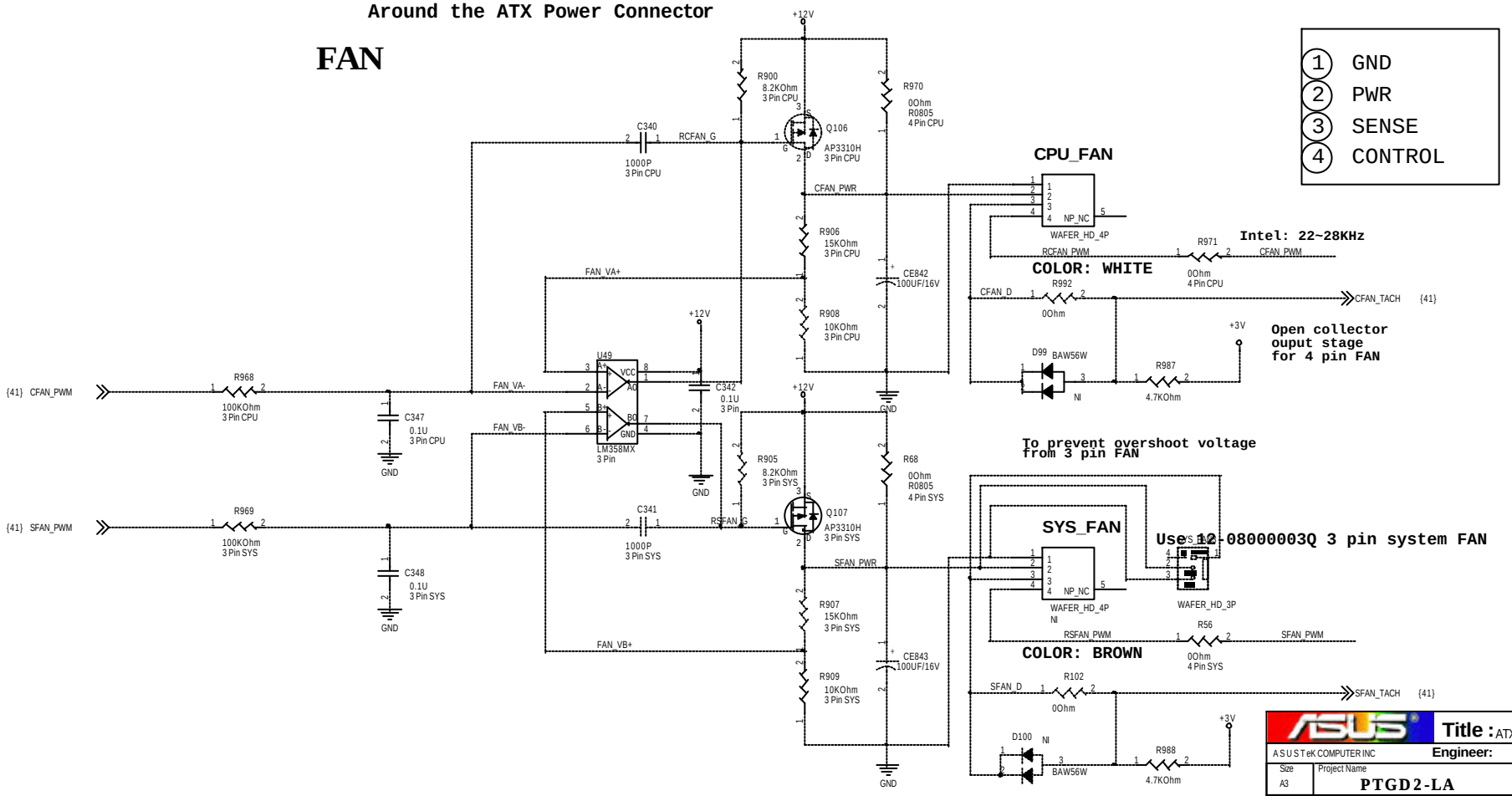


VRM POWER SUPPLY CONNECTOR



Around the ATX Power Connector

FAN



1. GND
2. PWR
3. SENSE
4. CONTROL

ASUSTeK COMPUTER INC

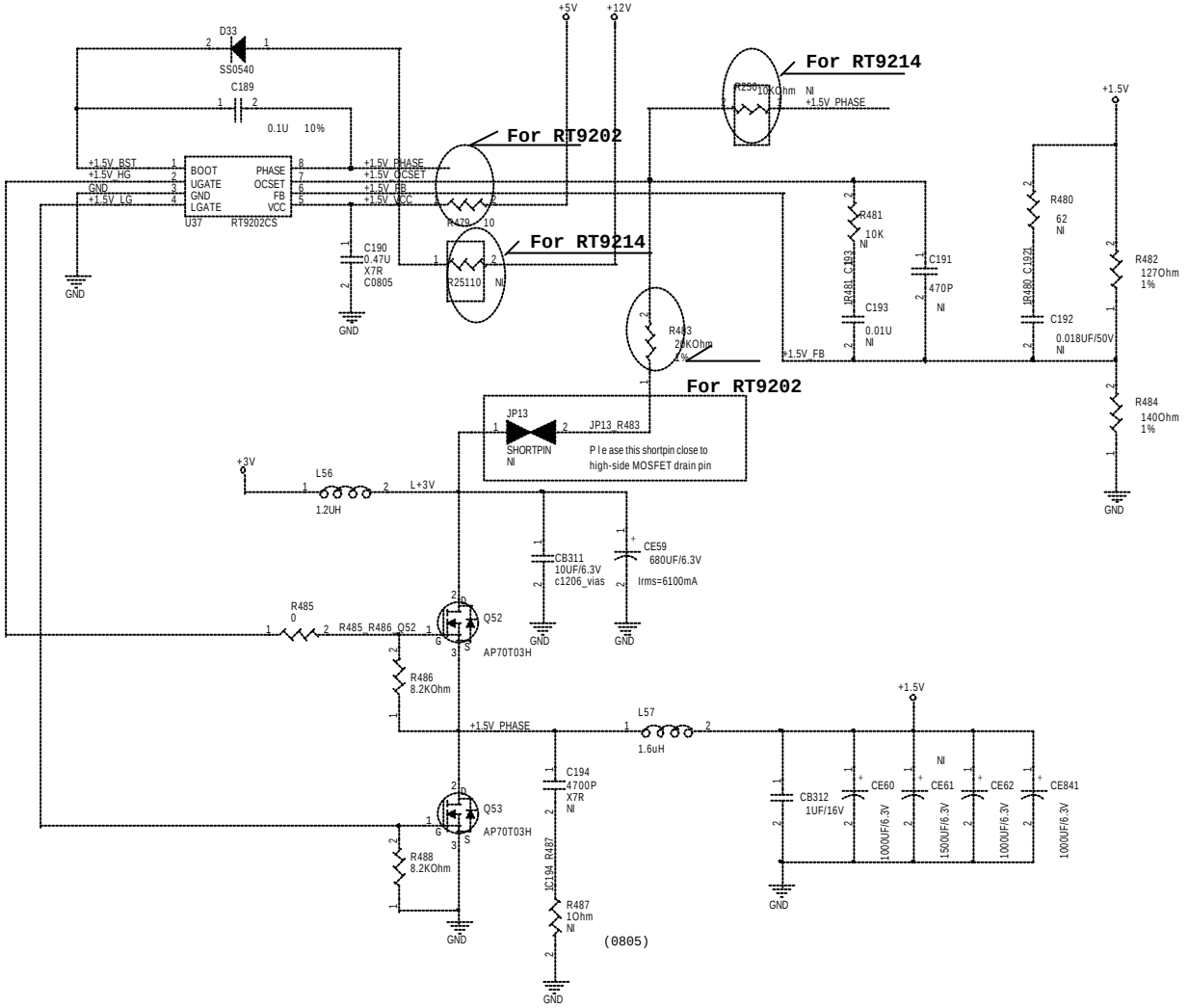
Title : ATX PWR & FAN

Engineer: Samuel Wu

Size	Project Name	Rev
A3	PTGD2-LA	1.03

Date: 星期一, 三月 29, 2004 Sheet 48 of 50

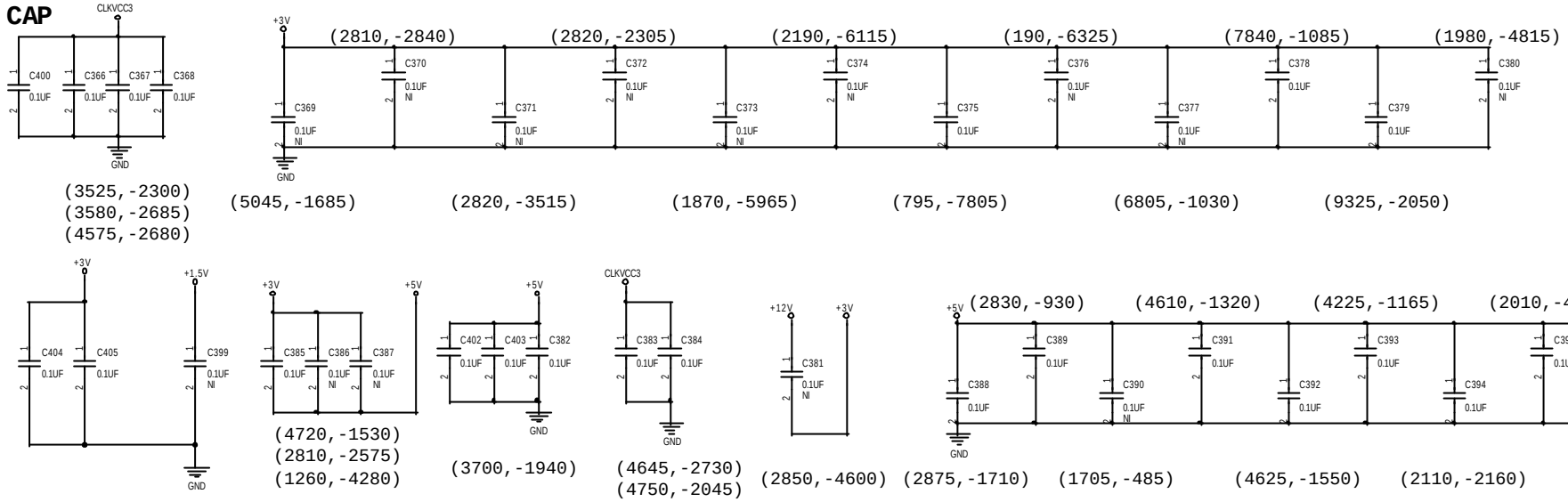
GMCH CORE



<Core Design>

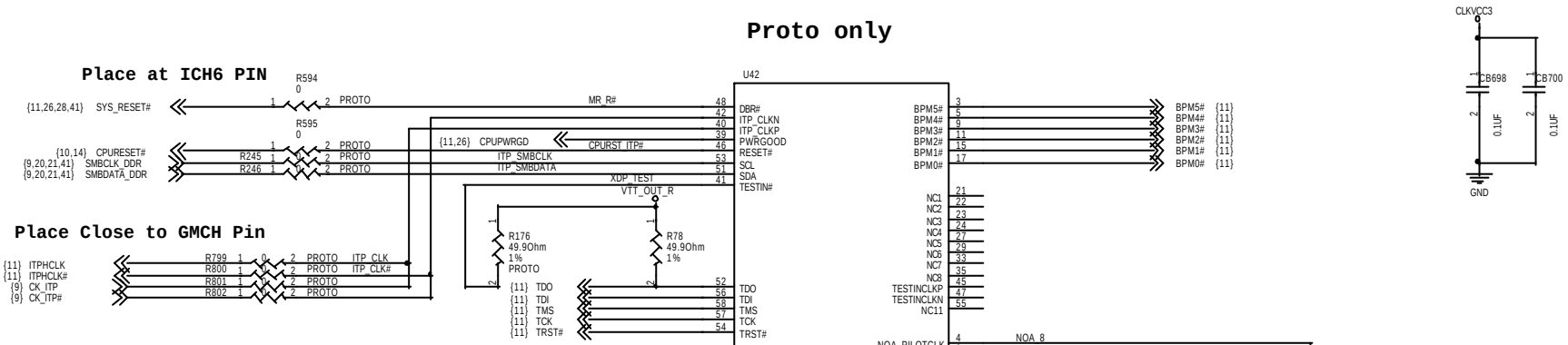
ASUSTek Inc.	Title : GMCH & THROTTLE	
	Engineer: Samuel Wu	
Size: A3	Project Name: PTGD1-LA	Rev: 1.03
Date: 星期一, 二月 29, 2004	Sheet 49 of 50	

EMI CAP



Proto only

Place at ICH6 PIN



Place Close to GMCH Pin

Proto only

PROCESSOR XDP
RIGHT-ANGLE, SURFACE
MOUNT XDP CONNECTOR

ASUS	Title : XDP CONNECTOR&EMI	
A S U S TeK COMPUTER INC	Engineer: Samuel Wu	
Size: A3	Project Name: PTGD2-LA	Rev: 1.03
Date: 星期一, 二月 29, 2004	Sheet 50 of 50	