It should be noticed that, as explained at the end of Section 5.8.1, the source voltage should be as small as possible in order eliminate the effect of Δn (mismatch of slope factors). This means that, for minimizing the input voltage offset, the two transistors should be put in a separate well connected to their sources, as illustrated in dotted line in Figure 8.3(a). In single-well processes, this is unfortunately only possible for one type of transistors (P-channel for N-well process).

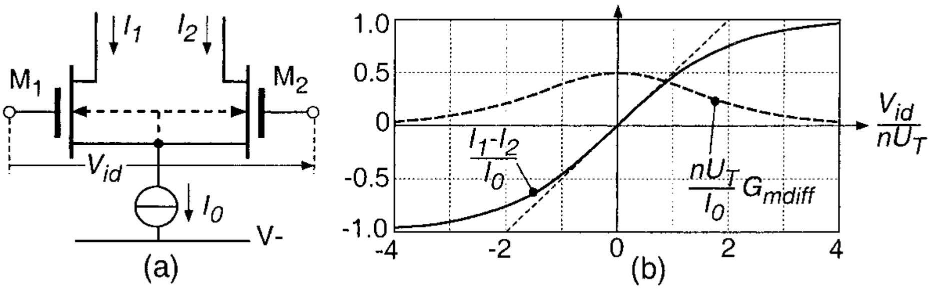

Fig. 8.3. Differential pair; (a) circuit; (b) transfer characteristics and transconductance.

The transfer characteristics of the saturated differential pair in weak inversion can be calculated by using equation (5.40) of the drain current, giving

$$I_1 = \frac{I_0}{1 + \exp\frac{-V_{id}}{nU_T}} \quad \text{and} \quad I_2 = \frac{I_0}{1 + \exp\frac{+V_{id}}{nU_T}}, \tag{8.14}$$

or for the difference of output currents

$$I_1 - I_2 = I_0 \tanh \frac{V_{id}}{2nU_T}, \tag{8.15}$$

which is represented in Figure 8.3(b). As can be seen, a major drawback of a differential pair in weak inversion is its limited input range of linearity. This is best illustrated by the differential transconductance

$$G_{mdiff} = \frac{\mathrm{d}(I_1 - I_2)}{\mathrm{d}V_{id}} = \frac{I_0}{2nU_T} \cdot \left(\cosh \frac{V_{id}}{2nU_T}\right)^{-2} \tag{8.16}$$

plotted in the same figure.

The linear range can be extended by using the circuit of Figure 8.4(a) [164], which can be analyzed by means of the concept of pseudo-resistors introduced in Section 5.5, as shown by Figure 8.4(b). The saturated transistors M_1 and M_2 correspond to grounded resistors R_1 and R_2 in the resistor prototype. The linearization transistors M_{1a} and M_{2a} correspond to two resistors of K-times larger values. The difference of output currents can now be calculated by using the resistor prototype, giving