AN57821

PSoC® 3 and PSoC 5 Mixed Signal Circuit Board Layout Considerations

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AN57821 introduces basic PCB layout practices to achieve 16 to 20 bit performance for the PSoC® 3 and PSoC 5 family of devices. The design practices covered in this application note are good rules to use in any mixed signal design for any accuracy.

Contents

Introduction

To better understand the problems that may arise when using ADCs above 12 bits; it is a good idea to understand just how small a voltage an ADC can actually resolve. An 8-bit ADC with a range of 2 V detects a minimum value of 2 V/256 = 0.008 V or about 8 mV. Although 8 mV seems small, let us compare this to ADCs with higher resolutions. Table 1 compares ADCs with an input range of ±1 V and with resolutions between 8 and 20 bits.

Table 1. ADC Resolution

Range ± 1.024 Volts		
Bits	**Resolution**	**Units**
8	8.000	mV
9	4.000	mV
10	2.000	mV
11	1.000	mV
12	0.500	mV
13	0.250	mV
14	125.0	µV
15	62.5	µV
16	31.3	µV
17	15.6	µV
18	7.8	µV
19	3.9	µV
20	2.0	µV

When the resolution is 20-bits, it resolves down to 2 µV. Add a little gain and you can resolve voltages less than a single µV. Also, do not forget that a system with a low resolution ADC and a narrow input range (high ADC gain) may resolve voltages in the microvolt range as well.

Offsets and noise sources below 100 µV, which were insignificant with a low resolution ADC, are now significant when using a 16 to 20 bit ADC. These errors can easily be overlooked by designers who are not used to sensitive analog circuits. Today's electronics are smaller than ever before and the small circuit board geometries alone are enough to cause many problems.

Trace Resistance Does Matter

As PCBs get smaller, trace widths continue to get narrower and closer than ever before. 6 mil (0.006") or less trace widths and spaces between traces are common for today's electronics. Even if you specify 6 mil traces, they can easily be over etched down to 4 or 5 mils.

So why do you care about traces getting smaller? One problem is that as traces get narrower the trace resistance increases. The standard equation for trace resistance is;

$$\text{Resistance} = \text{Resistivity} \times \frac{Length}{(Width \times Thickness)} \qquad \text{Equation 1}$$

Where;

Resistivity for copper is about 6.787×10^{-7} ohms/inch

Thickness of copper for a 1 oz copper PCB equals 1.378 mils.

A one inch trace 8 mils wide, on a 1 oz copper PCB is about 0.062 ohms. Table 2 shows calculated resistance values for several combinations of trace length and widths.

Table 2. Trace Resistance

Trace Resistance in ohms				
Width (mils)	Trace Length (inches)			
	0.1"	0.5"	1"	2"
15	0.0033	0.0164	0.0328	0.0657
10	0.0049	0.0246	0.0493	0.0985
8	0.0062	0.0308	0.0616	0.1231
6	0.0082	0.0410	0.0821	0.1642
4	0.0123	0.0616	0.1231	0.2463

As shown in Table 2, all combinations are well under an ohm. That does not sound too bad, right? But it all depends on where it is with respect to the circuit. If it is the trace to the input of a high impedance amplifier, it may not matter, but in other cases, you may not be so lucky. Let us take this same table and pass 5 mA current through each of these trace combinations. Although 5 mA is not much current and trace resistances less than an ohm seem small, the combined offsets are significant when using a high resolution ADC.

Table 3. Trace Voltage Offset

Offset Due to 5 mA Current (microvolts)				
Width (mils)	Trace Length (inches)			
	0.1"	0.5"	1"	2"
15	16.42	82.10	164.20	328.40
10	24.63	123.13	246.25	492.50
8	30.79	153.93	307.85	615.70
6	41.05	205.23	410.45	820.90
4	61.57	307.83	615.65	1231.30

In this table, if 5 mA flows through a 1 inch long trace that is 6 mils wide, the voltage drop is about 410 µV or 0.41 mV. In Table 1, note that this voltage drop does not become significant until your system is using a 12 bit or higher resolution ADC.

An example application where this magnitude of offset causes significant error is measuring temperature with a thermocouple. With a K-type thermocouple, the output is about 40 µV per degree centigrade. The 410 µV offset equates to an error in excess of 10 °C. If the same trace is over etched to 4 mils, the error is 50 percent higher. From this example, you can see how important it is to evaluate every PCB trace in your signal path.

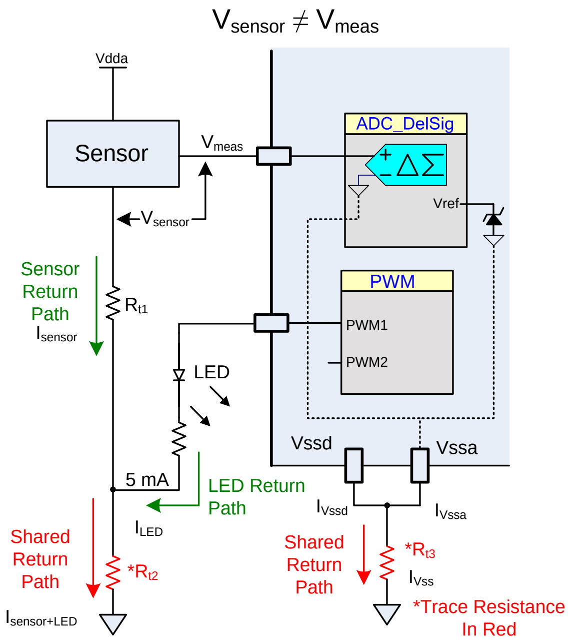
Shared Return Paths

When designing a circuit board with mixed signals or high precision ADCs, you should know where current is flowing in the PCB. Trace currents of just a few milliamperes (mA) can be enough to cause significant problems.

Trace resistance usually causes a problem when a sensitive analog signal's return path is shared by a digital or high current analog device. In these cases, high current does not mean amperes, but instead mA. In the previous example, the thermocouple shared the same return path as a 5 mA load. If you reduce that load down to 0.5 mA, the error remains 1 °C. Therefore, even currents in the 100s of µA are significant.

Figure 1 shows an example where return current paths are shared between the analog and digital grounds, and between a sensor and an LED. Both these shared paths can cause problems that may appear as system offsets or gain errors.

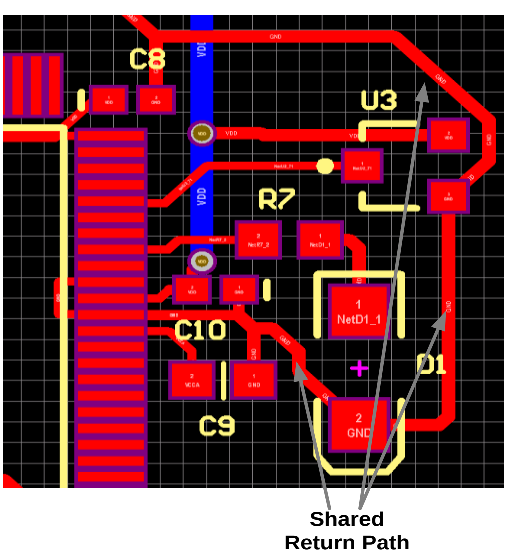
Figure 1. Resistance in Signal Return Path



$$V_{meas} = V_{sensor} + (I_{sensor} * R_{t1}) + (R_{t2} * (I_{sensor} + I_{LED}))$$
$$- (R_{t3} * (I_{Vssd} + I_{Vssa}))$$

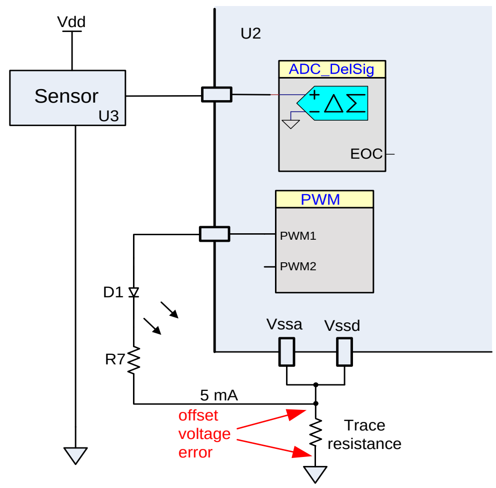
When the ADC in this example measures the output of the sensor, it also measures the voltage across the trace resistance. Depending on the length of the trace between where the sensor and LED currents combine and to the common ground point, a significant voltage offset error may occur. How significant depends on the desired accuracy of the system, the voltage gain of the sensor, and the magnitude of the offset error voltage. An example of the PCB layout is shown in Figure 2.

Figure 2. Example Layout with Shared Return Paths



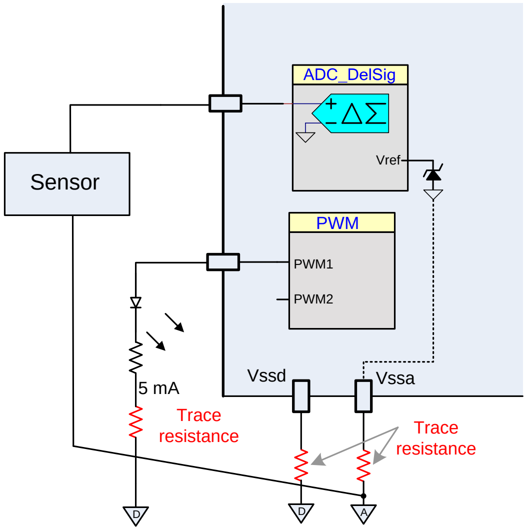
The PSoC 3 and PSoC 5 analog ground (Vssa) is as important as any of the signals you are measuring. The trace between the PSoC's Vssa pin and the system ground must be as short and low impedance as possible. Sharing this path with any component that uses even a few 100 µA can cause problems when measuring µV signals. An offset here can translate into a measurement offset when using single ended measurements. In Figure 3, the LED's current flows in the same path back to the supply, but the sensor has its own path. The internal bandgap reference is also connected to Vssa. Any voltage induced by sharing the return path with the LED causes the ADC's reference to fluctuate by the I*R drop. This offset between the reference and Vssa causes an ADC gain error.

Figure 3. Current in Analog Ground Path



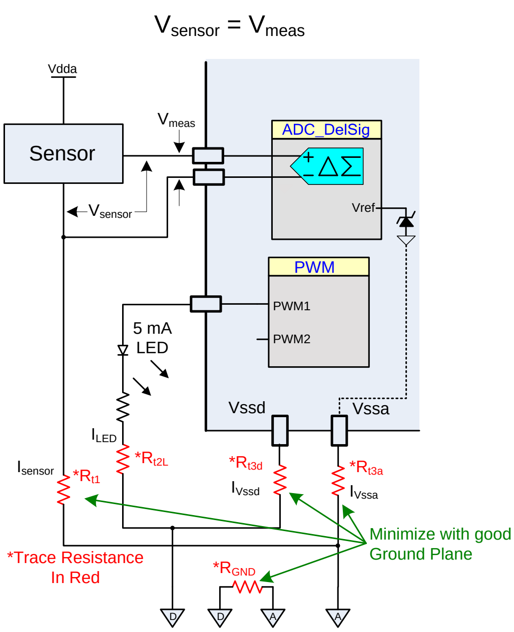
By providing separate ground paths for the digital ground (Vssd), analog ground (Vssa), the sensor, and the LED, there are no shared return paths (See Figure 4). The sensor, ADC and reference are at the same analog ground reference, so changing current in the LED has little or no affect on the sensor's output. Also note in the figure that the sensor and Vssa connect to the analog ground at the same location. This can physically be the same point or to a very low impedance plane.

Figure 4. Good Ground Connections



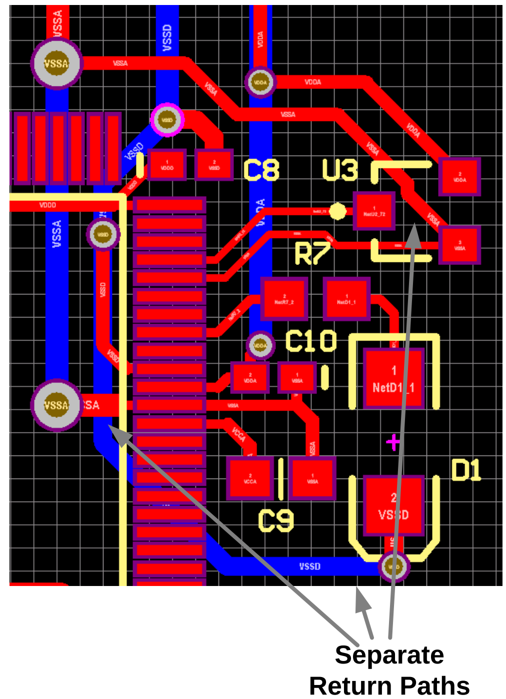
Using a differential ADC connection to the sensor helps eliminate common mode voltage offsets caused by sharing a sensor return with a high current path; see Figure 1. A common voltage is an offset common to both the sensor Vss and the sensor output. However, a differential connection to the sensor does not help errors caused by shared ground paths with Vssa (Figure 3). See Figure 5.

Figure 5. Differential ADC and Separate Return Paths



An example of an improved routing that maintains separate return paths, separate analog and digital supplies, and differential connection to the sensor is shown in Figure 6.

Figure 6. Example Layout with Separate Return Paths



Beware of the Hidden Killer

When sharing return paths with sensors or the Vssa pin with a modulated load, such as a LED driven by PWM, errors may not always be apparent at first. If the load is modulated in perfect sync with the ADC, the errors induced may be large or insignificant. If synchronization does not cause measurable errors on the bench, then no problem is seen in the initial development and testing. The problem is that with a change in either the ADC sample rate or the PWM frequency in this case, the error or noise can change significantly. This can be hard to test because in many applications, the change in the load modulation can vary due to environmental or software changes. So a board design that appears to be working at one time may fail at others. This is why it is imperative to follow good design rules even if a design appears to be working properly.

Routing Analog and Digital Signals

Ideally, analog and digital signals should be kept on opposite sides of the board, but this is usually impractical. Many designs require both analog and digital signals in the same area. Unfortunately, running relatively high impedance analog signals in the same area as digital signals can cause unwanted crosstalk which can add excessive noise to the analog signal.

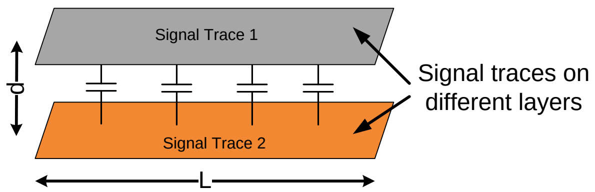
What is Crosstalk?

Crosstalk is when one signal affects another signal without being directly connected. This is most common when a digital signal with fast rise and fall times affects an analog signal with much high impedance. Digital signals are not immune to crosstalk either. High speed digital signals can easily affect other digital signals. Crosstalk between signals is usually one of three types, conductive, capacitive or inductive. In all cases increasing the distance between signals and decreasing the parallel length between signals will help to reduce the problem.

Conductive crosstalk is usually not a problem and only an issue when signals have very high impedance, such as more than 10 MΩ. This is usually caused when foreign materials such as dirt, oil, salt, or other liquids contaminate a PCB and cause the PCB material between traces to become more conductive. This decrease in resistance may cause enough crosstalk to adversely affect circuit operation. Solder mask can protect the PCB in some cases, but there are always areas such as where components are attached to the PCB that are exposed. Measures should be taken to isolate the PCB from these materials if they are found in the environment where the product is used. If it is impossible to insulate the PCB from foreign materials, a conformal coating can be applied to the PCB, but with added costs.

Capacitive coupling may occur when one trace is directly above the other on a different layer. A capacitor is formed between the copper traces. The more overlap of the copper between these traces the higher the capacitance. Decreasing the overlapping area between the signals will decrease the capacitance and therefore decrease the coupling. In some situations, especially with only two layer boards, it may be impossible to eliminate instances where a sensitive analog signal crosses over a fast digital signal. In these cases, the signals should cross at 90 degree angles to minimize the capacitance formed between these signals. If using multi-layer boards with more than 2 layers, make sure a power plane is between the two signals where they intersect to minimize coupling. Notice in Figure 7 that a capacitor is formed between the two traces which is directly proportional to the overlapping area.

Figure 7. Capacitive Coupling of Parallel Traces



If a two layer board is used make sure the analog and digital traces intersect at a 90 degree angle. This way the overlapping area is much less and therefore creates less capacitive coupling between the signals. See Figure 8 for an example.

Figure 8. Capacitive Coupling of Traces Running Perpendicular

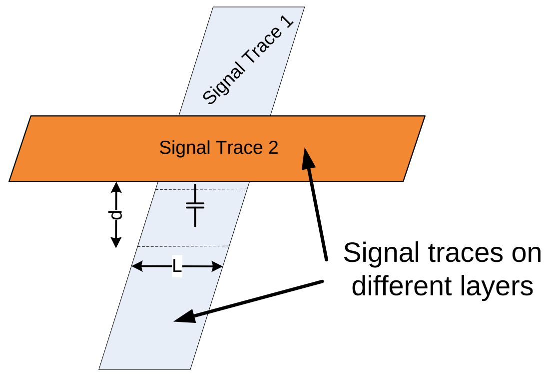
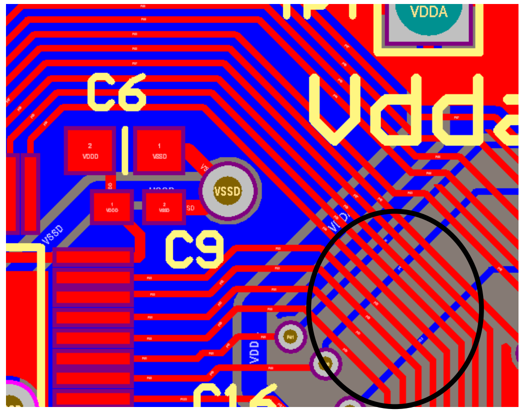


Figure 9 shows an example PCB layout where the analog traces (red) must cross over digital (blue) traces. Notice the 90 degree angles between the analog and digital traces.

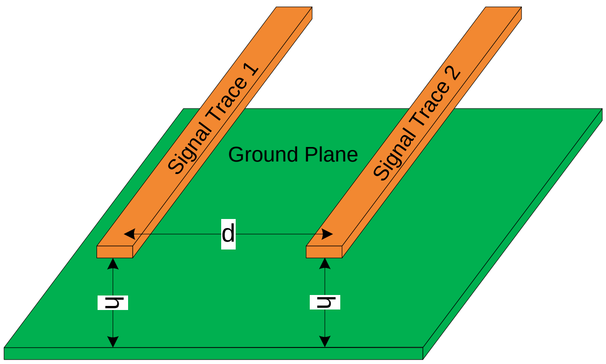
Figure 9. Digital Traces Cross Analog Traces at 90 Degrees



Traces that run next to each other on the same or near layer may be coupled magnetically. This is referred to as Inductive coupling. Inductive coupling is a function of three mechanical features, 1) the separation between traces, 2) the distance which the two traces are parallel, and 3) the distance between the trace and the nearest power plane. The distance between the signals and the distance between the signals and the ground plane are the biggest contributors as shown in the simplified Equation 2 and Figure 10.

$$Crosstalk \cong \frac{1}{1+(\frac{d}{h^2})}$$ Equation 2

Figure 10. Spacing for Inductive Coupling

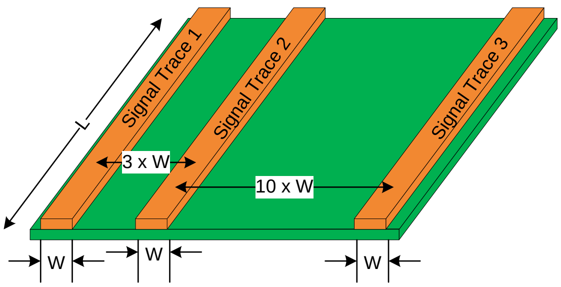


As you can see, the height the trace is above the ground plane is a huge factor. By reducing this distance, the crosstalk is reduced by the square of the height. If you need to run digital and analog traces near each, keeping them close to the ground plane may be the best option to reduce crosstalk.

3-W Rule

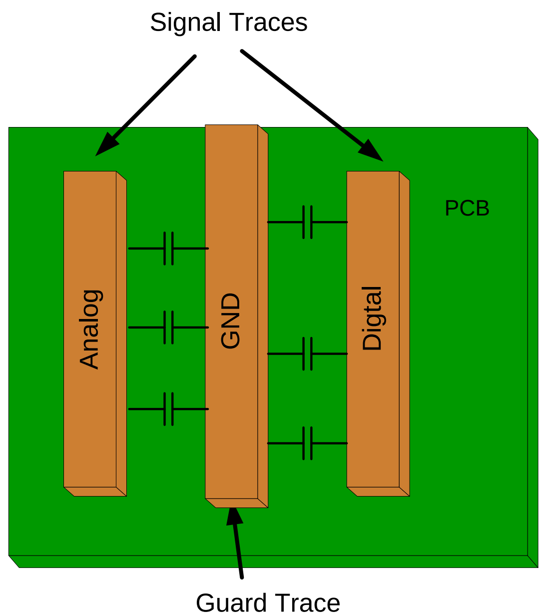
The 3-W rule states that the separation between logic traces (center to center) should be three times the width of the traces. For example, if the traces on a PCB are 0.008" wide, the distance between trace's centers would be 0.024" (0.008"x3) and the distance between trace edges would be 0.016" (0.008"x2). This puts each trace outside the 70% magnetic flux boundary of the other trace. To be outside the 98% flux boundary the spacing between the traces needs to be ten times the width of the traces. Of course all of this is dependent on the impedance of the traces and the rise time of the signals. See Figure 11.

Figure 11. Example of 3W Rule



Another option to reduce coupling between signals that must run near each other and on the same side of the board, is to use a guard trace connected to ground between the signals. This helps to reduce the capacitive coupling between the signals. See Figure 12.

Figure 12. Using Guard Traces



In multilayer boards, some layers are closer to some layers than others. For example, with a common 4-layer 0.062" thick board, layers 1 and 2 are closer together than layers 2 and 3. When routing analog and digital signals in the same area, separate the traces on non adjacent layers, to ensure maximum separation.

Multiple Power Domains

Sensitive analog systems make it desirable to maintain separate analog and digital power supplies. The PSoC 3 and PSoC 5 families provide separate power and ground pins for the analog and digital blocks. The GPIOs are also divided into four groups, but this is mainly to provide multiple logic levels to external components. A summary of the power supply connections follows.

- **Vssd** – Ground for all digital logic and I/O pins.
- **Vddd** – Supply for all digital peripherals and digital core regulator. Vddd must be less than or equal to Vdda.
- **Vssa** – Ground for all analog peripherals.
- **Vdda** – Supply for all analog peripherals and analog core regulator. Vdda must be the highest voltage present on the device. All other supply pins must be less than or equal to Vdda.
- **Vccd** – Output of digital core regulator and input to digital core. Requires a 1 µF cap to Vssd. Regulator output not for external use.

- **Vcca** – Output of analog core regulator and input to analog core. Requires a 1 µF cap to Vssa. Regulator output not for external use.
- **Vddio0, 1, 2, 3** – Supplies for I/O pins. The GPIOs are grouped into four groups, each with its own power pin. Vddio must be less than or equal to Vdda.

The use of separate external analog and digital regulators is always a good idea. If the cost of an additional regulator is prohibitive and the digital section of your design does not contain high speed or high current switching, it is possible to use a single regulator. One important factor is to always wire your design as if you have separate regulators. Separate both power and ground signals for the analog (Vdda, Vssa) and digital supplies (Vddd, Vssd). Make the connection between these two supplies (analog and digital) as close to the power supply source as possible. Usually the output impedance of the power supply is low and with such a connection, the digital supply has less of an effect on the analog supply.

Ground Planes

Ground planes are always beneficial in a mixed signal design, but additional layers may be expensive for a given design. Even with two layer boards it is possible to provide partial planes under sensitive analog sections of the design. Whether you use ground planes or not, make sure the return paths are as direct to the power supply as possible. Remember, ground planes may not improve your design if the path to the supply is not low impedance, or the plane is too fragmented. On two sided boards do not rely on just using fill; it can lead to narrow high resistance paths that are not obvious without careful inspection. Route the ground with traces and supplement with fill.

If care is taken when selecting pins, the board layout can be much easier and enables partial analog and digital power planes. Figure 13 shows how the analog and digital sections of the chip are placed in the PSoC 3 and PSoC 5 with respect to the I/O ports.

Figure 13. PSoC 3 / PSoC 5 Analog/Digital Layout

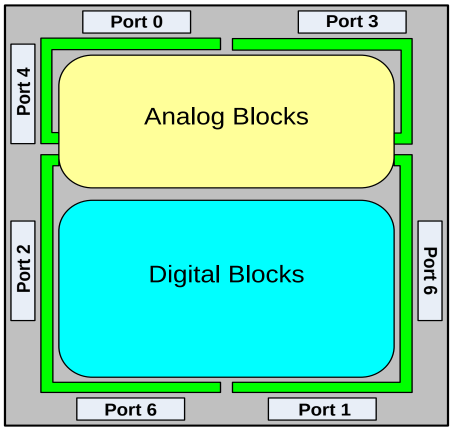
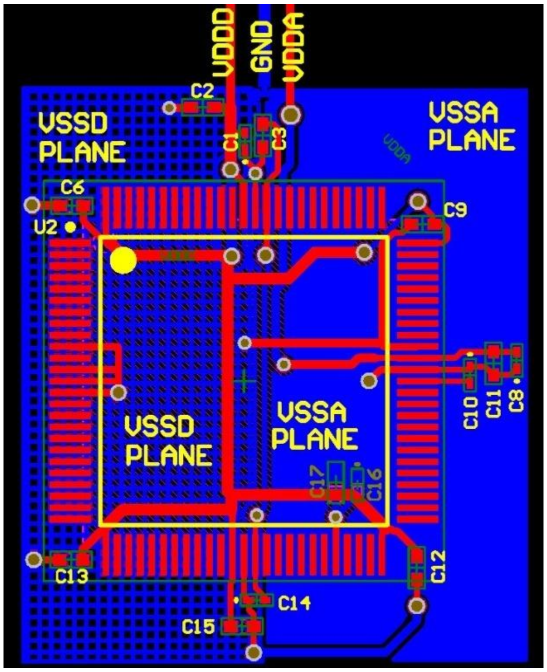


Figure 14 is an example two-layer board layout. The PSoC is rotated 90 degrees clockwise with respect to the image in Figure 13. The blue is the bottom layer and the red is the top layer. Notice that there is adequate room to route the signals away from the PSoC on the top layer even with all power supply pins connected and good power grounds on the bottom layer. The VSSD plan was hatched intentionally so that it is easy to distinguish between the VSSD and VSSA power planes. Normally it is recommended to make your power planes solid, unless there is a special case, such as Cap Sense buttons and controls.

If separate analog and digital ground planes can be used in your design, they should be connected at a single point in most cases. This single point should be between the power supply source and the PSoC itself.

With a single regulator it is possible to use a single ground plane, but only if the analog and digital components are well isolated from each other.

Figure 14. Example 2-Layer Board Layout



See Appendix A for example layouts for 48-pin QFN, 48-pin SSOP, and 68-pin QFN packages.

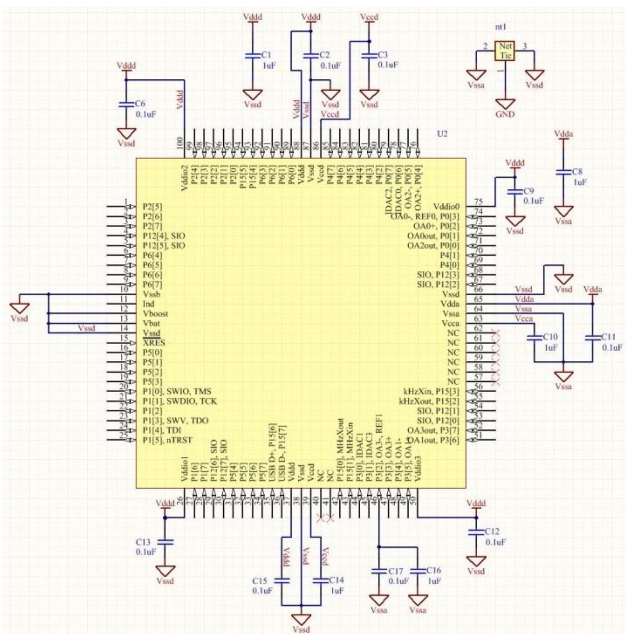
Bypass Capacitors

As mentioned earlier, there are several power domains with the PSoC 3 and PSoC 5 parts. Each of these domains has individual bypass capacitor requirements. Table 4 summarizes these requirements and Figure 15 shows an example schematic with these capacitors in place.

Table 4. Bypass Capacitor Connection Summary

Power Supply	Bypass Capacitors
Vddd - Vssd	0.1 µF ceramic at each pin plus bulk capacitor 5 to 10 µF. (C1, C2, C15)
Vdda - Vssa	0.1 µF ceramic at pin (C11). Additional 1 µF to 10 µF (C8) if more than an inch from power supply.
Vddio0,1,2,3 - Vssd	0.1 µF ceramic at each Vddio pin. Additional 1 µF bulk capacitor if several pins are switching 5 to 10 mA. (C9, C13, C6, C12)
Vcca - Vssa	1 µF at the Vssa pin. (C9)
Vccd - Vssd	1 µF ceramic at one Vccd pin and a 0.1 µf at the other Vccd pin. The Vccd pins should be connected together. (C3, C14)
Vref - Vssa (optional)	The internal bandgap may be bypassed with a 1 µF to 10 µF capacitor. (C16, C17)

Figure 15. Example Schematic of Power Connections



Capacitor Selection

There are two types of capacitors used for power supply stability: bypass and bulk. Bulk capacitors are sometimes referred to as reservoir capacitors as well. The bypass capacitors must be placed near the power supply pins of the component. Bypass capacitors help to eliminate high frequency noise and supply current for short transients. These capacitors are usually between 0.001 µF and 0.1 µF. Capacitors with dielectric of NPO, X5R, and X7R make excellent bypass capacitors and are available in values between 100s of pF to several µFs.

The reservoir capacitors are usually placed near the regulators. They are also spread around the board if it is more than a few square inches in size and contains several active components. The capacitors are used to supply power for longer periods and filter low frequency noise. Reservoir capacitors range in size between 1 µF and 100 µF or even larger for boards with high current signals or power supplies. X5R, tantalum, and some surface mount electrolytic capacitors work well for this purpose.

Often the 0.01 µF or 0.1 µF capacitor is sufficient for a bypass capacitor. For reservoir capacitors, it is recommended to do some simple calculations to make sure you have the optimum value. Too big and you are spending more than you need. Too little and your power supply ripple may be excessive and cause noise. Start with the equation:

$$I = C * \frac{dV}{dT}$$

Solving for C:

$$C = I * \frac{dt}{dV}$$

Dt = Clock or highest frequency component (fclk * π)

I = Average current

dV = Acceptable ripple voltage

$$C = \frac{I_{ave}}{(f_{clk} * \pi * dV)}$$

Mixed Signal PCB Rules Summary

The following is a list of rules to keep in mind when designing mixed signal boards.

1. Consider separate analog and digital supplies.
2. Understand all return paths.
3. Four layer boards with power planes are preferable, although not always affordable.
4. Do not run analog signals parallel to clocks or fast digital signals.
5. If analog and digital signals must cross, make the intersection at 90 degrees to keep the coupling capacitance to a minimum.
6. Power planes should be used in similar areas. For example, only run analog signals over analog power planes.
7. Keep bypass capacitors as close to ICs as possible. Also make sure bypass connections to power signals are low impedance.

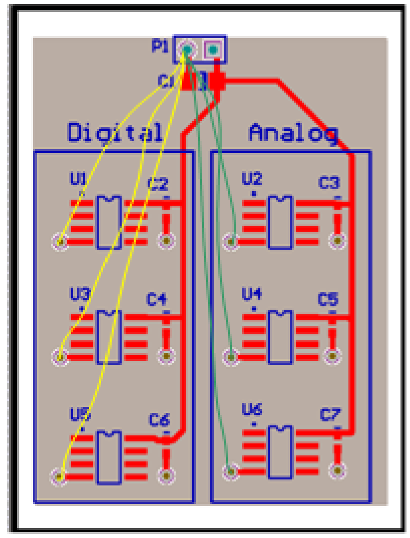
8. Separate analog and digital signals and components on the board if possible. Designate “Analog” and “Digital” areas of the PCB.
9. Avoid long traces into a high impedance input. These act as antennas.
10. Keep power traces as wide (low impedance) as possible.
11. Keep analog signals close to the ground plane to minimize inductive crosstalk.
12. Use large or multiple vias when connecting power signals between plans to reduce impedance.
13. Minimize digital rise and fall times of digital signals.
14. Use guard traces to isolate analog and digital signals.

PCB Layout and Auto Routing Tools

PCB layout tools have come a long way in the last 20 years. Many of these tools allow signals to be grouped and create different rules for trace widths and distance between traces. These rules keep you from inadvertently making mistakes. Auto routers have also become more powerful and many common tools follow the same rules as when you route by hand. A skilled PCB layout designer can use these rules to enhance the quality of the auto router. Although these tools are very powerful, be careful how these automated tools route analog and digital signals. You may find it worthwhile to hand route the sensitive part of your board then let the auto router complete the least critical section of the board. Either way, make sure you review the final routing.

Placing the parts in optimal locations can also greatly aid in either hand routing or auto routing. After the parts placement and board layout is complete, a simple test can be used to validate if shared return paths could cause a problem. Print out your board layout and draw the most direct path between your power supply and each of the components. Use one color for analog parts and another for digital parts. If the different colors cross, you may want to re-evaluate your design. See the following example.

Figure 16. Draw Return Paths on PCB Layout



Summary

The design tips discussed in this application note help you recognize the following concepts: 1) Understand your signal return path and do not share analog and digital return paths, if possible. 2) Trace resistance does matter and it is as simple as Ohms Law to determine just how much. 3) There is capacitive coupling between any two adjacent traces, so keep digital signals away from analog signals.

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Appendix A

Layouts for 48-pin QFN, 48-pin SSOP, and 68-pin QFN packages

Figure 17. Example Layout for 48-pin QFN Package

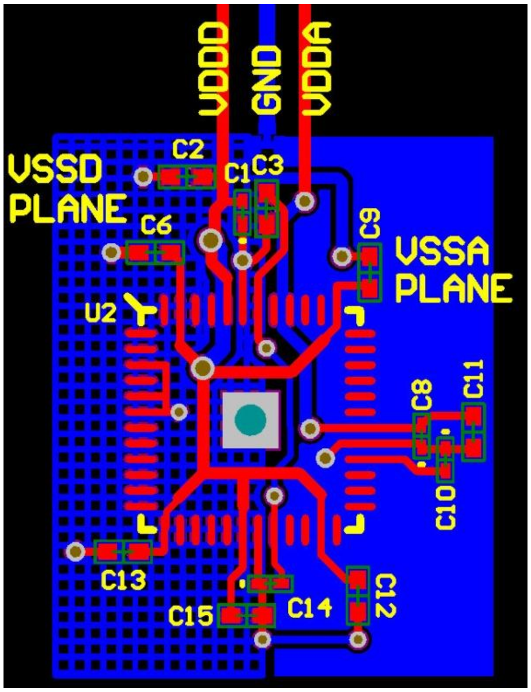


Figure 18. Schematic for 48-pin QFN Package

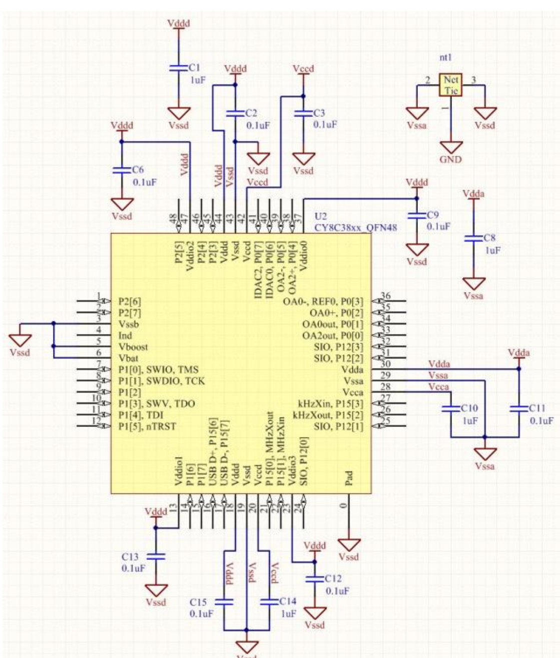


Figure 19. Example Layout for 48-pin SSOP Package

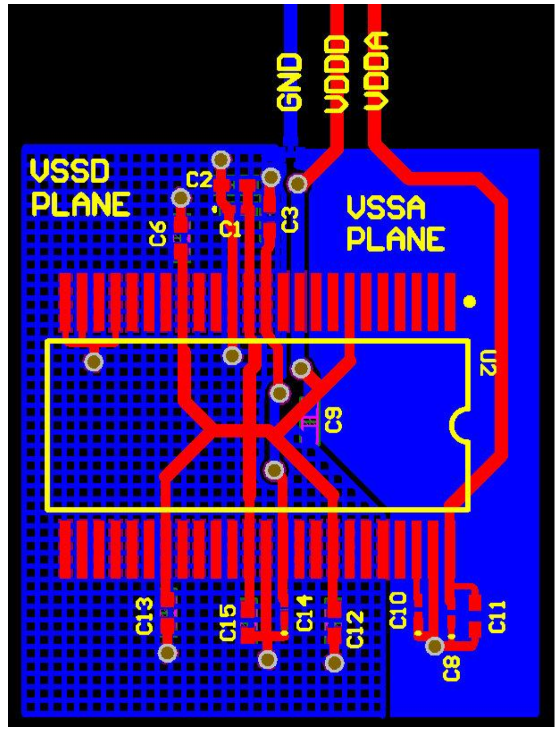


Figure 20. Schematic for 48-pin SSOP Package

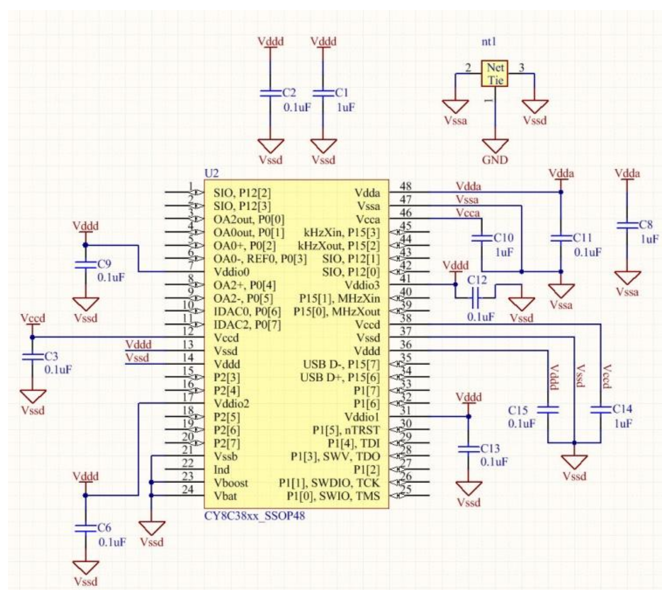


Figure 21. Example Layout for 68-pin QFN Package

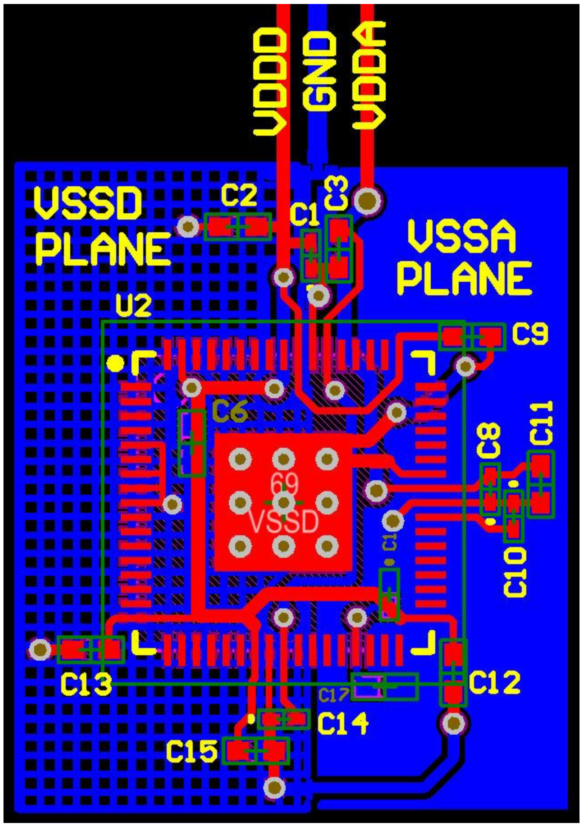
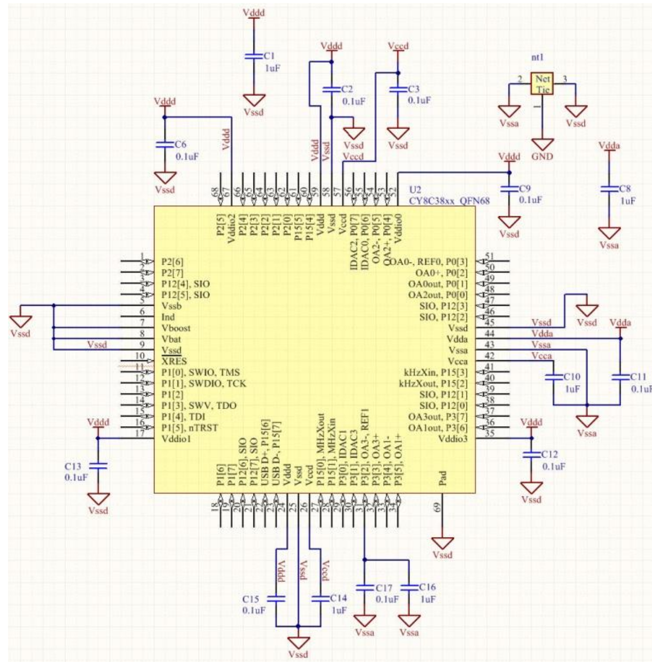


Figure 22. Schematic for 68 QFN Package



Document History

Document Title: AN57821 - PSoC® 3 and PSoC 5 Mixed Signal Circuit Board Layout Considerations

Document Number: 001-57821

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2818833	MEH	12/01/2009	New application note
*A	2896385	MEH	3/19/2010	Changed connection to Vboost from Vddd to Vssd
*B	2991511	SRIH	07/22/2010	Fixed branding discrepancies
*C	3095205	MEH	11/25/2010	Changed the title, updated abstract, and fixed a few minor typos.
*D	3460049	MEH	12/09/2011	Changed Title Updated Figures 1, 3, 4, and 5, and Tables 2 and 3 Several minor changes throughout document Changed abstract Updated template
*E	3656888	MEH	6/26/2012	Updated Routing Analog and Digital Signals. Updated Ground Planes. Updated Mixed Signal PCB Rules Summary. Added Appendix A. Updated in new template.
*F	3719890	MEH	8/23/2012	Updated capacitor designators to match the schematic changes in rev *E.

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