Keywords: logic-level translation, MAX1840, MAX1841, MAX3001, MAX3370-MAX3393, MAX8860, MAX8867 Jul 21, 2004

APPLICATION NOTE 3007

# Logic-Level Translation

*Abstract: Logic level translation techniques and pitfalls - and Maxim solutions.*

*Electronic design has changed considerably since the days when TTL and 5V CMOS were the dominant standards for logic circuits. The increasing complexity of modern electronic systems has led to lower voltage logic, which in turn can cause incompatibility between input and output levels for the logic families within a system. It is not unusual, for example, that a digital section operating at 1.8V must communicate with an analog subsection operating at 3.3V. This article examines the basics of logic operation and considers, primarily for serial-data systems, the available methods for translating between different domains of logic voltage.*

## The Need for Logic-Level Translation

The growth of digital ICs that feature incompatible voltage rails, lower $V_{DD}$ rails, or dual rails for $V_{CORE}$ and $V_{I/O}$ has made the translation of logic levels necessary. The use of mixed-signal ICs with lower supply voltages that have not kept pace with those of their digital counterparts also creates the need for logic-level translation.

Translation methods vary according to the range of voltages encountered, the number of lines to be translated (e.g., a 4-line Serial Peripheral Interface (SPI™) versus a 32-bit data bus), and the speed of the digital signals. Many logic ICs can translate from high to low levels (such as 5V to 3.3V logic), but fewer can translate from low to high (3.3V to 5V). Level translation can be accomplished with single discrete transistors or even with a resistor-diode combination, but the parasitic capacitance inherent in these methods can reduce the data-transfer rate.

Although byte-wide and word-wide level translators are available, they are not optimal for the < 20Mbps serial buses discussed in this article (SPI, I²C, USB, etc.). Thus, translators that require large packages with high pin counts and an I/O-direction pin are not meant for small serial and peripheral interfaces.

The Serial Peripheral Interface consists of the unidirectional control lines data in, data out, clock, and chip select. Data in and data out are also known as master in, slave out (MISO) and master out, slave in (MOSI). SPI can be clocked in excess of 20Mbps, and is driven by CMOS push-pull logic. As SPI is unidirectional, translation in both directions on the same signal line is unnecessary. This makes level translation simpler, because you can employ simple techniques involving resistors and diodes (**Figure 1**) or discrete/digital transistors (**Figure 2**).

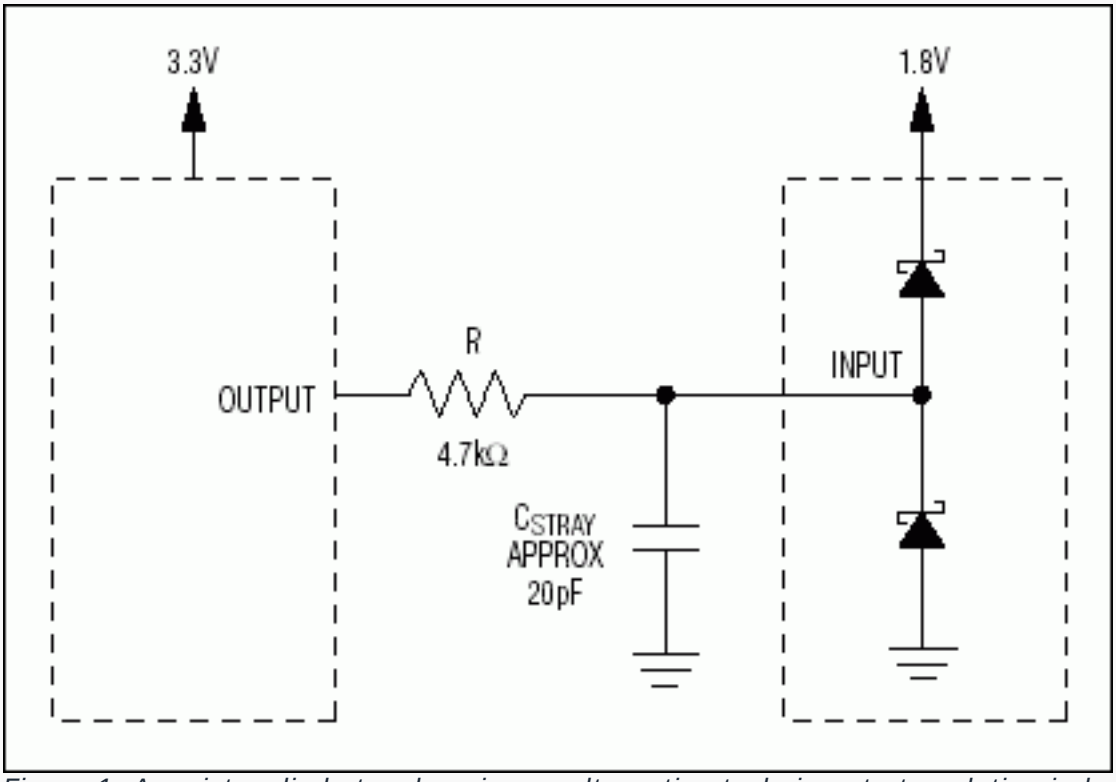

*Figure 1. A resistor-diode topology is one alternative technique to translation in both directions on the same signal line.*

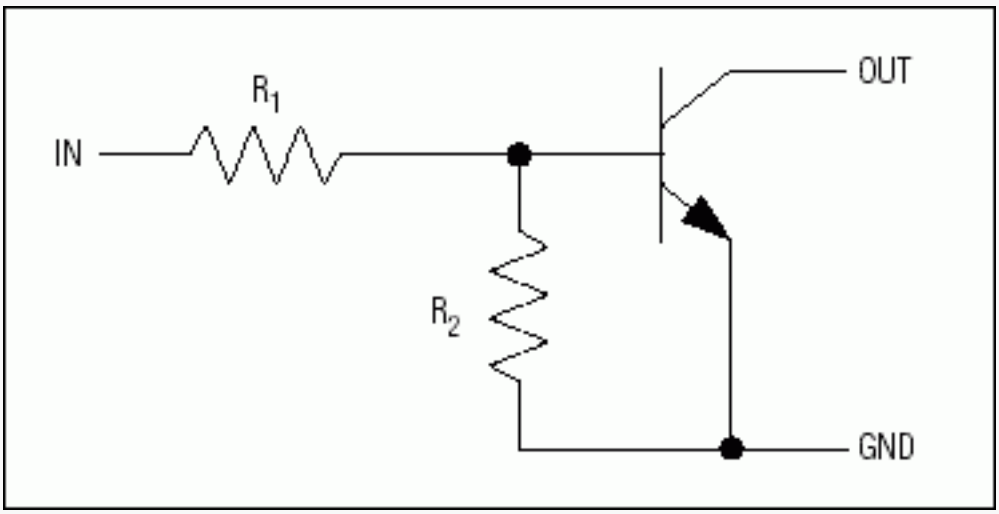

*Figure 2. Using discrete/digital transistors is another alternative to bidirectional translation.*

The I²C, SMBus™, and 1-Wire®, interfaces are all bidirectional, open-drain I/O topologies. I²C has three speed ranges: standard mode at ≤ 100kbps, fast mode at ≤ 400kbps, and high-speed mode at ≤ 3.4Mbps. Level translation for bidirectional buses is more difficult, because one must translate in both directions on the same data line. Simple topologies based on resistor-diode and single-stage-transistor translators with open collector or drain do not work because they are inherently unidirectional.

## Unidirectional High- to Low-Level Translation—Input Overvoltage Tolerance

To translate from higher to lower logic levels, IC manufacturers produce a range of devices that are said to tolerate overvoltage at their inputs. A logic device is defined as input-overvoltage protected if it can withstand (without damage) an input voltage higher than its supply voltage. Such input-protected devices simplify the task of translating from higher- to lower-$V_{CC}$ logic while increasing the signal-to-noise margin.

Overvoltage-tolerant inputs, for example, allow a logic device to cope with logic levels of 1.8V and higher while powered from a 1.8V supply. Devices in the LVC logic family, which are mostly input-overvoltage protected, work well in applications requiring high-to-low translations. The opposite situation of low-to-high translation is not as easy. It may not be feasible to generate higher voltage logic-level thresholds ($V_{IH}$) from lower voltage logic.

When designing a circuit for which connectors, high fanout, or stray load capacitance produce a high capacitance load, you should remember that for all logic families, reducing the supply voltage also decreases the drive capability. An exception occurs between 3.3V CMOS or TTL (LV, LVT, ALVT, LVC, and ALVC) and 5V standard TTL (H, L, S, HS, LS, and ALS). In these logic families, the 3.3V and 5V logic activation points ($V_{OL}$, $V_{IL}$, $V_{IH}$, and $V_{OH}$) match each other.

## Mixed High-Low and Low-High Translation

Applications like the SPI bus require a mixture of high-low and low-high translation. Consider, for example, a processor at 1.8V and a peripheral at 3.3V. Though it is possible to mix techniques as described above, a single chip such as the MAX1840, MAX1841, or MAX3390 can implement the necessary translation by itself (**Figure 3**).

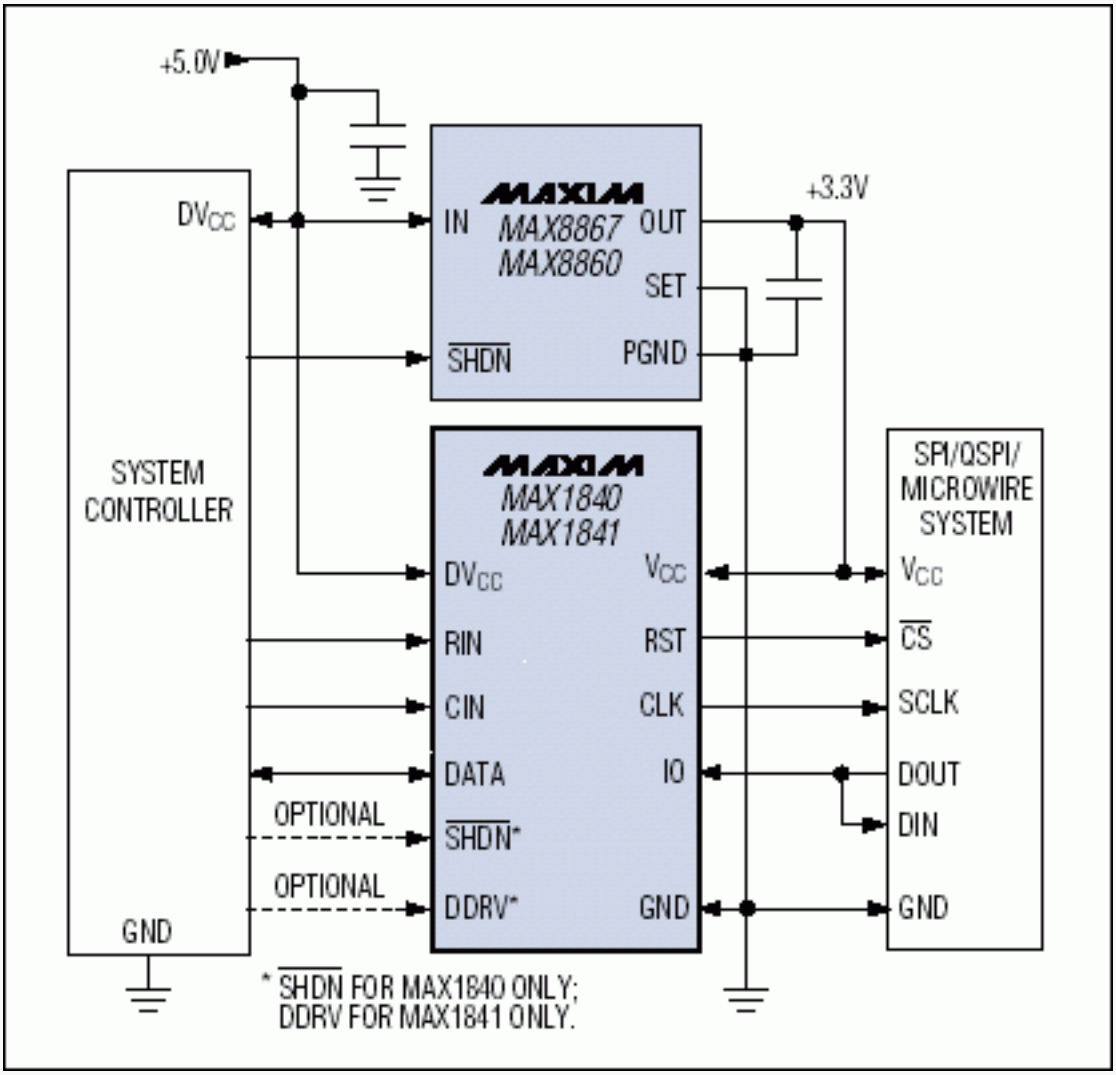


*Figure 3. This diagram shows an example of an IC level translator with an SPI/QSPI™/MICROWIRE™ interface that can implement the necessary mixture of high-low and low-high translation.*

Other systems, such as I²C and 1-Wire buses, require logic translation in both directions. Simple topologies, based on a single transistor with open collector or drain, do not work in a bidirectional bus because they are inherently unidirectional.

## Bidirectional Transceiver Methods

For the larger byte- and word-wide buses where WR and RD signals already exist, one method for transferring data across the voltage levels is a bus switch such as the 74CBTB3384. Such devices are typically optimized for operation between 3.3V and 5V. For smaller 1- and 2-wire buses, this approach raises two issues. Firstly, it requires a separate enable pin to control the direction of data flow, and this ties up valuable port pins. Secondly, it requires large ICs that take up valuable board space.

All techniques have their pros and cons. Nonetheless, designers need a universal device that works across all translation levels, enables mixed low-to-high and high-to-low logic transitions, and includes unidirectional and/or bidirectional translation. A next-generation bidirectional level shifter (the MAX3370 in the MAX3370–MAX3393 family of ICs) fulfills those needs while overcoming some of the problems associated with alternative approaches.

The MAX3370, which implements a transmission-gate method of level translation (**Figure 4**), relies on external output drivers to sink current, whether they operate in a low-voltage or higher voltage logic domain. That capability enables the device to work with either open-drain or push-pull output stages. The relatively low on-resistance of a transmission gate (less than 135Ω), moreover, limits the speed of operation much less than the series resistor of Figure 1.

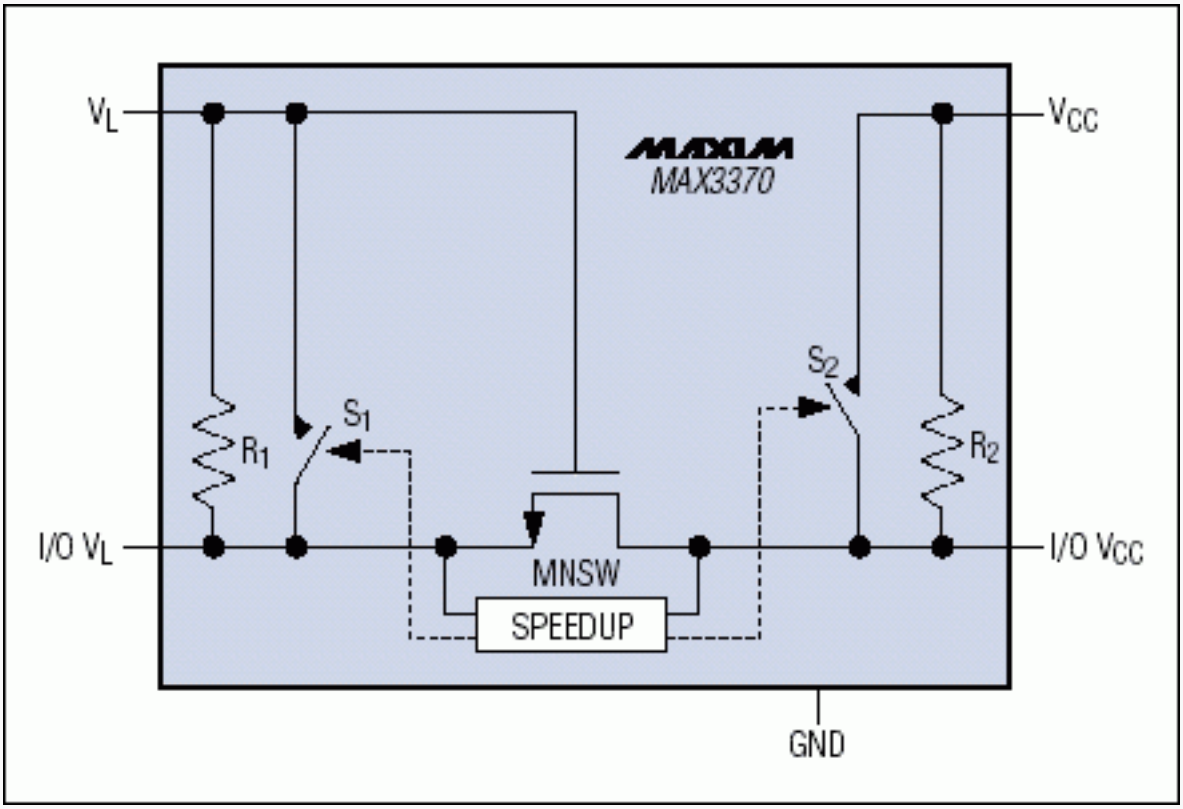


*Figure 4. The MAX3370 implements a transmission-gate method of level translation.*

The design in Figure 4 offers two other advantages. Firstly, for open-drain topologies, the MAX3370 includes 10kΩ pull-up resistors paralleled by a "speed-up" switch. This minimizes the need for external pull-up resistors while reducing the RC time-constant ramp associated with traditional open-drain topologies. Secondly, the MAX3370's tiny SC70 package also conserves valuable board space.

## Solving the Speed Problem

RC time constants limit the effective data rate for most other open-drain approaches (**Figures 5** and **6**). The MAX3370 IC family includes a speed-up scheme that actively pulls up rising edges, thereby minimizing the effect of capacitive loads as illustrated in **Figures 7**, **8**, and **9**. When the input goes above a predefined threshold, the device actively pulls up the rising edge, thereby minimizing any skew caused by external parasitic components. That capability can allow data rates as high as 20Mbps for signals produced by a push-pull driver. The speed of signals from open-drain drivers tends to be slower. As for other open-drain topologies, however, you can

improve their speed by adding external pull-up resistors.

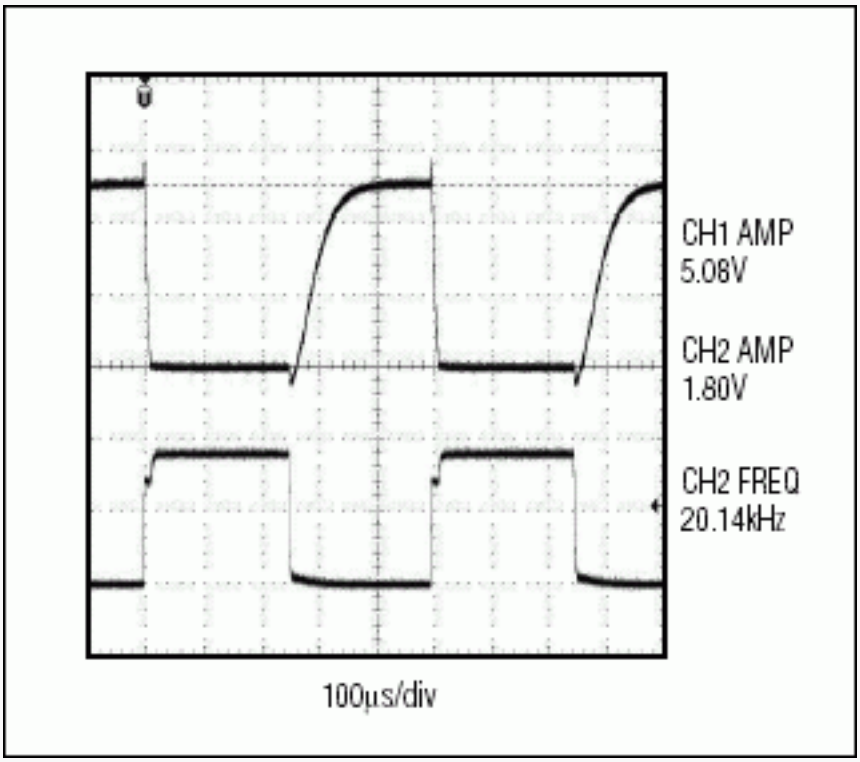


*Figure 5. The scope plot of single FET open-drain output at 20kHz shows a limited effective data rate due to RC time constants.*

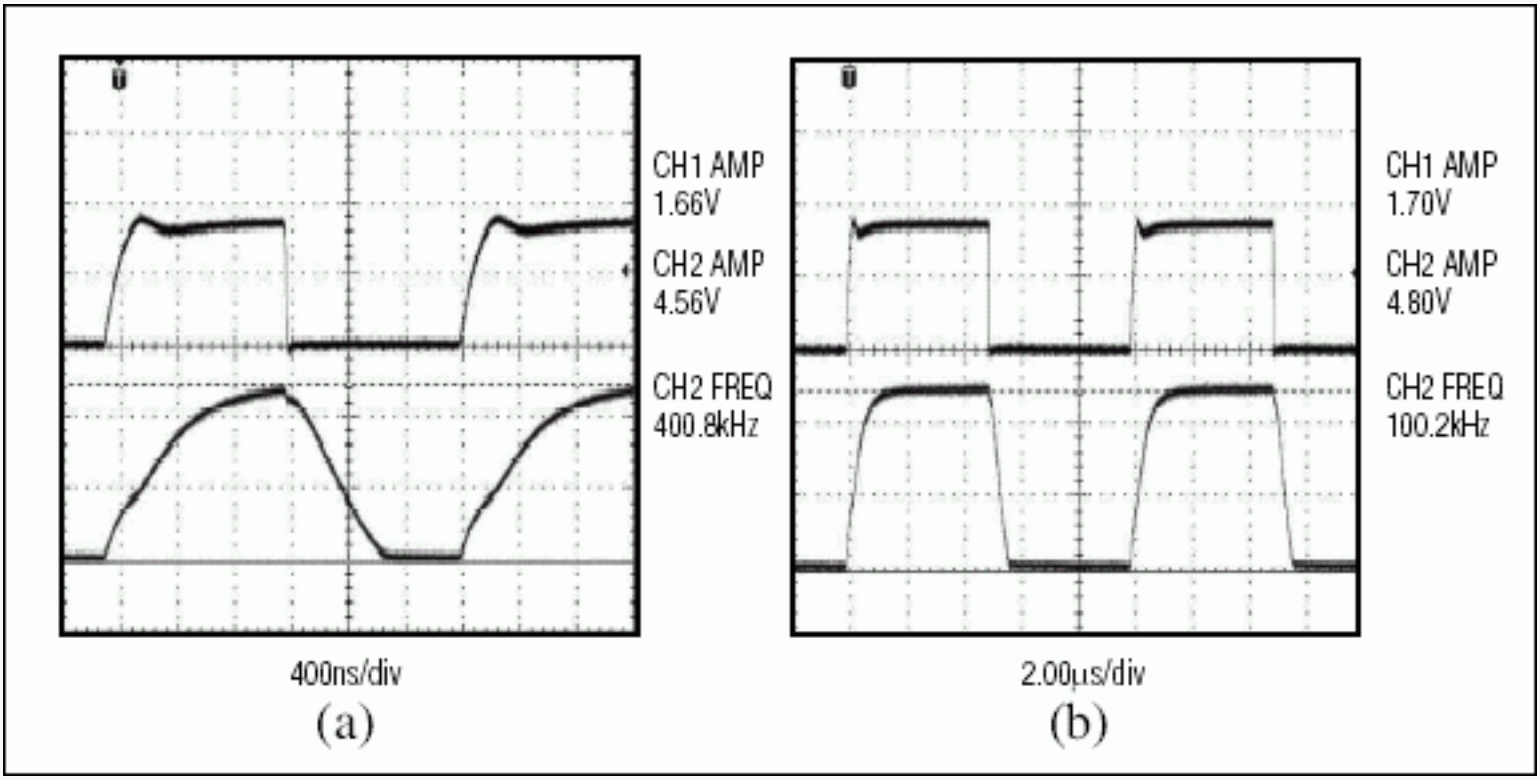


*Figure 6. Scope plots of a dual-transistor transceiver translating 1.8V to 5V at 400kHz (a) and at 100kHz (b) illustrate limited effective data rates.*

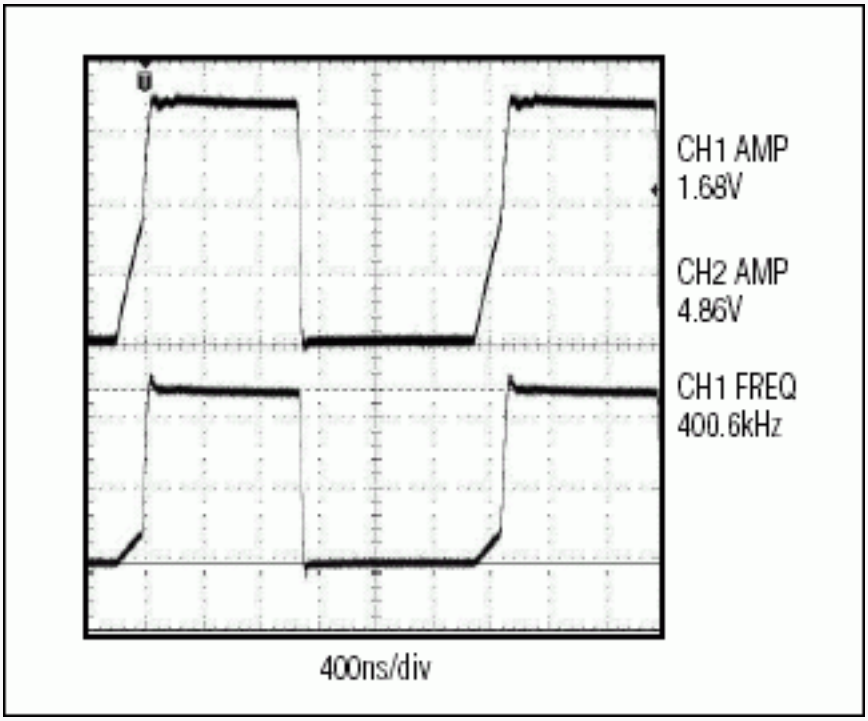


*Figure 7. A scope plot of MAX3370 output with a translation of 1.8V to 5V at 400kHz shows minimized capacitive load effects.*

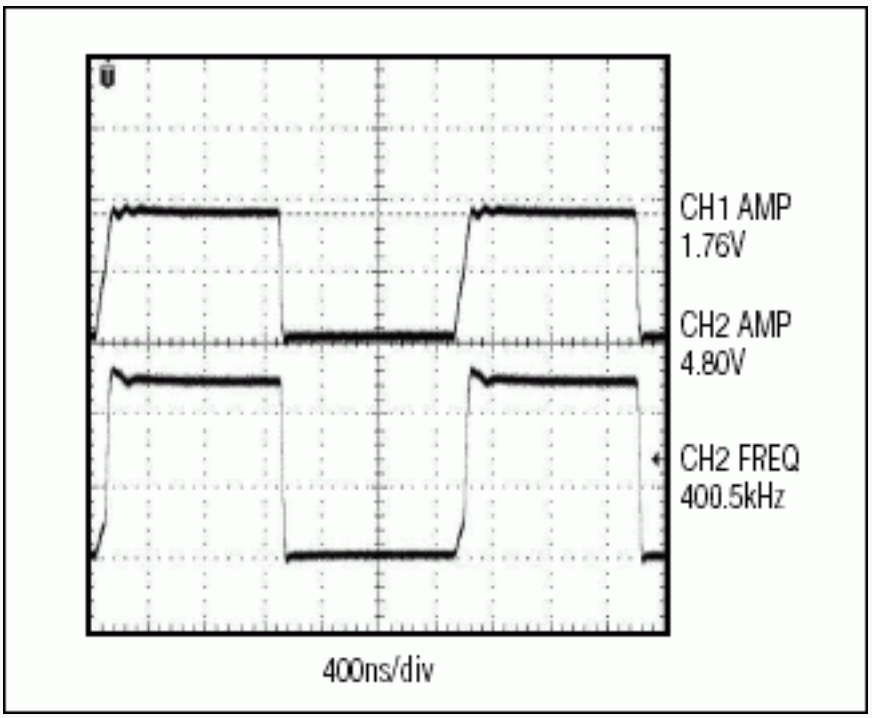


*Figure 8. This scope plot of the MAX3370 output at 400kHz with 4.7kΩpullup resistors shows the minimized effect of capacitive loads.*

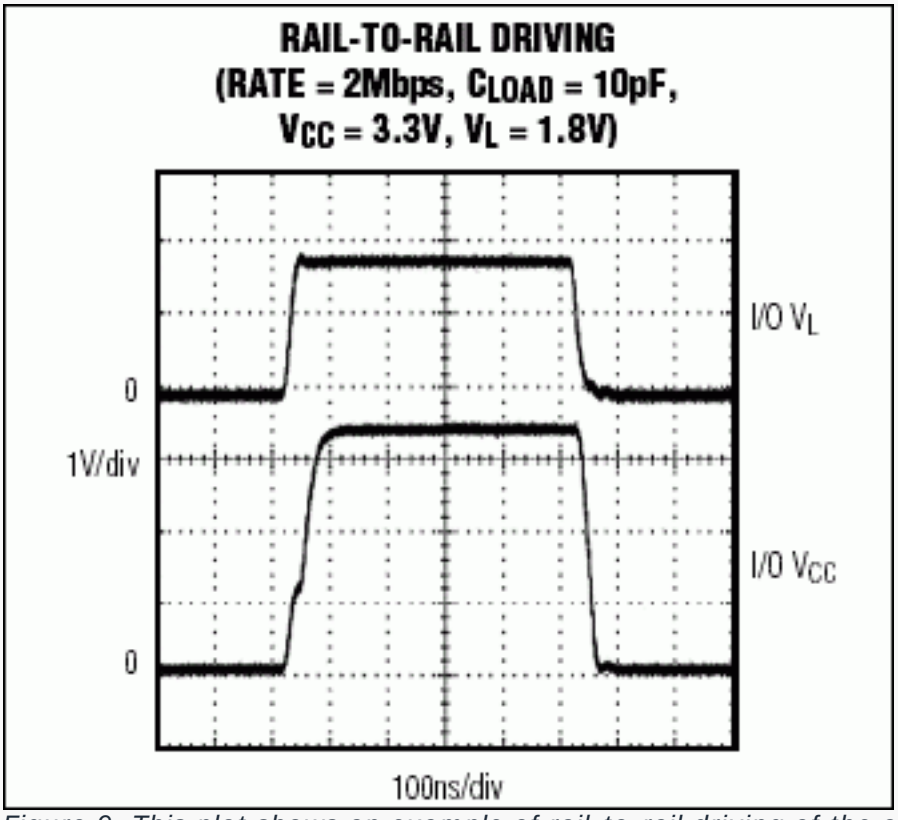


*Figure 9. This plot shows an example of rail-to-rail driving of the output from a MAX3370 high-speed test circuit.*

## Solving the Universal Voltage Problem

An application ideally requires a single component that can translate between any two logic levels at any speed. The ICs in the MAX337x family are designed for logic levels as low as 1.2V and as high as 5.5V. Consequently, this single component can provide the level translation required in most cases, without needing to select a logic device for each level-translator requirement.

Formerly, the need for low-to-high and high-to-low translations in the same circuit could be met only with separate chips. Now the bidirectional and topology-independent features (push-pull or open-drain) of a single chip from the MAX337x family solve both problems. The MAX3370 is a single-line, universal logic-level translator. For translating a larger number of I/O lines, consult the devices listed in **Table 1**.

**Table 1. Multiline logic-level translators**

| Part | No. of I/O Channels | Unidirectional/ Bidirectional Rx/Tx | VL Range (V) | $V_{CC}$ Range (V) | Separate Enable | Speeds Up to: (bps) |
|---|---|---|---|---|---|---|
| MAX3000/1 | 8 | Bi, 8 | 1.2 to 5.5 | 1.65 to 5.5 | Yes | 230k/4M |
| MAX3002/3 | 8 | Bi, 8 | 1.2 to 5.5 | 1.65 to 5.5 | Yes | 20M |
| MAX3013/23 | 8/4 | Bi, 8/4 | 1.2 to ($V_{CC}$ - 0.4) | 1.65 to 3.6 | Yes | 100M |
| MAX3014-28 | 8 | Uni, full mix | 1.2 to ($V_{CC}$ - 0.4) | 1.65 to 3.6 | Yes | 100M |
| MAX3370/1 | 1 | Bi, 1 | 1.65 to 5.5 | 2.5 to 5.5 | No/Yes | 2M |
| MAX3372/3 | 2 | Bi, 2 | 1.2 to 5.5 | 1.65 to 5.5 | Yes | 230k |
| MAX3374<br>MAX3375<br>MAX3376 | 2 | Uni, 2/0<br>Uni, 1/1<br>Uni, 0/2 | 1.2 to 5.5 | 1.65 to 5.5 | Yes | 16M |
| MAX3377/8 | 4 | Bi, 4 | 1.2 to 5.5 | 1.65 to 5.5 | Yes | 230k |
| MAX3379 | 4 | Uni, 4/0 | 1.2 to 5.5 | 1.65 to 5.5 | Yes | 16M |

| | | | | | | |
|---|---|---|---|---|---|---|
| MAX3390 | 4 | Uni, 3/1 | 1.2 to 5.5 | 1.65 to 5.5 | Yes | 16M |
| MAX3391 | 4 | Uni, 2/2 | 1.2 to 5.5 | 1.65 to 5.5 | Yes | 16M |
| MAX3392 | 4 | Uni, 1/3 | 1.2 to 5.5 | 1.65 to 5.5 | Yes | 16M |
| MAX3393 | 4 | Uni, 0/4 | 1.2 to 5.5 | 1.65 to 5.5 | Yes | 16M |
| MAX13013/14 | 1/2 | Bi, 1/2 | 1.2 to ($V_{CC}$ - 0.4) | 1.65 to 3.6 | Yes | 100M |

As the number of I/O voltages per system increases, the need for level-translation techniques becomes more acute. Load capacitance, the magnitude of $V_{CC}$ differences, and speed compound the problem. For high-to-low translation, the problem is less acute if the difference in translation voltages is minimal and off-the-shelf devices (such as logic ICs tolerant of input overvoltage) are available.

However, finding ICs and discrete-component circuits capable of handling ICs with wide differences in $V_{CC}$ and of translating from low to high logic levels becomes difficult. Bidirectional and open-drain topologies do not lend themselves well to high-speed data rates. Maxim's level translators ease the problem of level translation for a wide range of bi-/unidirectional, push-pull, and open-drain topologies. The ICs are available in ultra-small packages and require no external components for standard operation.



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**Related Parts**

MAX1840: QuickView -- Full (PDF) Data Sheet -- Free Samples

MAX1841: QuickView -- Full (PDF) Data Sheet -- Free Samples

MAX3370: QuickView -- Full (PDF) Data Sheet -- Free Samples

MAX8860: QuickView -- Full (PDF) Data Sheet -- Free Samples

MAX8867: QuickView -- Full (PDF) Data Sheet -- Free Samples

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