# An Ultrasonic Transducer Interface IC With Integrated Push-Pull 40 Vpp, 400 mA Current Output, 8-bit DAC and Integrated HV Multiplexer

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***Abstract*—We present an ultrasonic transducer interface IC that includes an 8-bit, 40 $V_{pp}$, 400 mA current output DAC for arbitrary waveform transducer excitation and a ±25 V analog multiplexer. The IC was fabricated using a 0.35 $\mu$m, 50 V CMOS process.**

**The design eliminates the need for an external power amplifier as the piezoelectric transducer is driven directly from a segmented push-pull current output DAC, which simplifies the overall system design. This approach has the advantage of simple and rapid glitch-free power-up/down, which is especially important in integrated high-output-power drivers.**

**The DAC has been evaluated when operating at a 150 MHz sampling rate with a ±400 mA output current and a 50 Ω load. Measured performance includes 37 dB SNDR and 46 dB SFDR at 10 MHz output frequency.**

**By implementing an additional reference DAC and extending the receiver isolation switch into an analog multiplexer, we enable on-line calibration for the purpose of reducing the driver and receiver signal path uncertainty. Measurements show a greater than ten-fold improvement in delay uncertainty to approximately 20 ps for temperature variations of 0 to 70 degrees Celsius.**

***Index Terms*—Current-output DAC, digital-analog converter, digital-analogue conversion, driver circuits, field effect transistor switches, high-voltage integrated circuits, high voltage level shifter, mixed analogue-digital integrated circuits, on-chip calibration technique, segmented thermometer coded DAC, supply voltage sensitivity, ultrasonic measurement.**

## I. Introduction

ULTRASOUND is well established as a technique in a wide variety of noninvasive material evaluation techniques used industrially to measure flows, material compositions and material flaws. Medical applications of ultrasound are mainly concerned with imaging internal organs and distinguishing between different types of soft tissue with high spatial resolution. Almost all ultrasound devices are based on either piezoelectric or electrostatic transducers, which convert an electrical pulse (the excitation) into an acoustic wave and then back into an electrical signal after the wave has interacted with the sample of interest.

An ultrasonic measurement application typically uses 1–2 channels, in contrast to the tens to hundreds of transducers used in imaging applications, and is concerned with bulk properties rather than the location of features. In measurement applications, an ultrasonic pulse with a central frequency in the range of 500 kHz to 50 MHz and a pulse length in the range of 0.1–10 $\mu$s is applied to the material of interest (a solid, liquid, or less commonly, a gas). As the acoustic wave propagates through (or is scattered by) the material, information about the material can be obtained from the amplitude, delay, Doppler shifts, and speed of sound, as well as the frequency dependence of these characteristics. In addition, nonlinear acoustics within the material may also be observed.

Traditionally, discrete transducer excitation and receiver circuits have provided sufficient performance for measurement applications, and integrated solutions have mainly focused on reduction of size and power consumption [1], [2]. However, as the techniques used for ultrasound measurement are refined, the possibilities available with integrated solutions for excitation and reception are becoming more important. These features include predictable transfer function, interfaces that present a stable impedance to the transducer, and low spurious transducer excitation. Additionally, the possibility to generate arbitrary excitation waveforms allows the dynamic range requirements on the receiver to be relaxed by optimizing the frequency contents of the transmitted signal, avoiding excitation of unwanted resonant modes of the transducer.

This paper presents an integrated ultrasonic transducer interface circuit that provides two functions to an ultrasonic measurement system: a high-voltage arbitrary waveform transducer driver, and high-voltage switches for isolating off-chip LNAs from the high voltages present at the transducer during excitation. The work, to our knowledge, represents the first published integrated arbitrary excitation waveform ultrasonic transducer interface.

The target applications require low driver and receiver path delay uncertainty. In this work this is achieved by driving the output directly from a fast, high output voltage, high output current, DAC. This eliminates the need for a power amplifier and allows two DACs implemented on the same die to achieve a high degree of delay matching, This, in turn, makes it possible to perform on-line delay characterization using the second auxiliary DAC as a reference. Fig. 1 gives an overview of the chip functionality in a possible measurement system.

Manuscript received March 02, 2010; revised November 10, 2010; accepted November 14, 2010. Date of publication January 06, 2011; date of current version January 28, 2011. This paper was approved by Associate Editor Andreas Kaiser. This work was supported by the European Union European Regional Development Fund project ESIS, and also supported by the Fraunhofer Institute of Integrated Circuits.

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Digital Object Identifier 10.1109/JSSC.2010.2096113

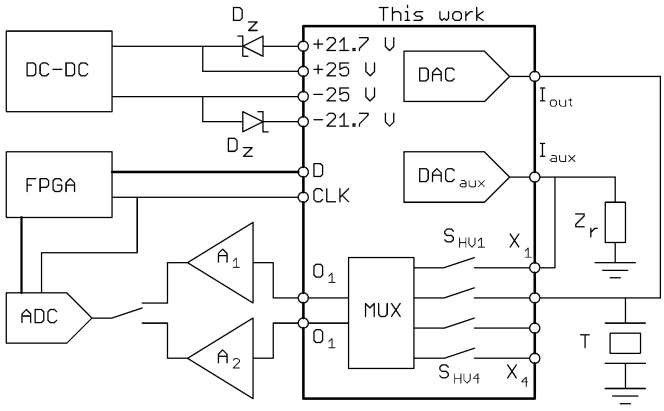


Fig. 1. A possible ultrasonic measurement system built around the device presented in this work. A transducer $T$ is connected to the output $I_{out}$ driven by the integrated 40 $V_{pp}$ 400 mA current output DAC. This node is also connected to one of the inputs $X$. The received signal is routed through a high voltage switch $(S_{HV2})$ and a 4:2 analog multiplexer to one of the of the off-chip LNAs. The signal path can be calibrated by performing measurements on an external reference impedance $Z_r$ using $\mathrm{DAC}_{aux}$ and one of the other inputs $X$. An FPGA or a digital ASIC will handle the data $D$ and clock $CLK$ to the driver DAC as well as an ADC digitizing the received signal. The chip does not include the DC-DC converter for generating the excitation voltage, and the floating 3.3 V supplies for floating logic are generated using external shunt regulators $D_z$.

We present measured performance data for the 150 MHz, 40 $V_{pp}$ segmented current source DAC, as well as on the delay matching between two such converters. Similarly the performance and matching of the implemented analog switches has been evaluated. We also present the intended calibration scheme used for minimizing measurement uncertainty degradation.

Section II of this paper presents the target specifications. In Section III we expand on the calibration of the device, followed by implementation details in Section IV. Measurement results from both the DAC and analog switches are presented in Section V, including matching between channels implemented on the same die. A brief comparison to other work is given in Section VI, and Section VII summarizes the conclusions of this work.

## II. Specifications

In order to enable flow-meter applications where the reciprocal property of the measurement cell is utilized, the interface should present the transducer with the same impedance during reception and transmission [3]–[5]. With a high output impedance driver a high input impedance receiver can be used. Thus, a higher on-resistance can be tolerated for the HV isolation switches, saving area and reducing the parasitic capacitance. Based on this, a segmented current source topology was selected as it provides a high output impedance, as compared to alternative solutions such as an R-2R DAC. Additionally, in the chosen topology any glitches produced when the current sources switch has little impact on distortion [6].

The higher the resolution of the DAC, the more accurately the excitation waveform can be tuned. Thus, for this work we explored the resolution limits achievable with a high speed, high voltage, high output current DAC. The output capacitance of the current source transistors can limit the achievable high-frequency distortion performance of a segmented current source DAC [7]. Initial simulations showed that no more than 8-bit resolution could be motivated, based on the limited linearity achievable when using the high-voltage transistors available in the chosen process.

TABLE I
Summary of Target Performance

| DAC: | |
|---|---|
| Resolution | 8-bits |
| Output current | ± 600 mA |
| Output voltage swing | 40 $V_{pp}$ |
| Sample frequency | 200 MHz |
| **Analog multiplexer:** | |
| On resistance (HV) | 20 Ω |
| On resistance (LV) | 4 Ω |

As the intention with this work was to produce a generic interface device, we elected to specify and evaluate the device in terms of driving capability, rather than with an electrical model [8], [9] of one specific type of transducer. The target output current of the driver was about 600 mA, sufficient for driving low-impedance transducers such as the Panametrics V3456, a popular choice at our department, to 40 $V_{pp}$. In order to provide some margin for process variations and model inaccuracies the output current of the simulated design was increased by 33% and set to 800 mA.

The received signal passes through one high voltage switch and one low-voltage switch in the multiplexer (Fig. 1). The sum of these on-resistances should be smaller than the real part of the impedance of the transducer in order to minimize the thermal noise contribution. The driver was designed targeting transducer impedances as low as 33 Ω. Thus, the target on-resistances for the receiver isolation switches and the switches of the low-voltage multiplexer were set to 20 Ω and 4 Ω, respectively.

The target performance of the device is summarized in Table I.

## III. Calibration

As temperature and supply voltage change, so will the clock to output delay of the DAC and the transfer function of the receiver isolation switches and the external LNA. In applications where the delay stability is critical, such as transit-time flow meters, measurement accuracy can be improved by compensating for these variations. The measured voltage over a reference impedance, observed through the whole receiver signal path when a test current waveform is generated by the DAC, can be used to characterize the combined effects of driver and receiver imperfections, and thus also to compensate for these effects.

One way to perform this measurement is to disconnect the transducer and connect a reference impedance in its place. This would require switches, either solid state or mechanical. While the former consume excessive amounts of chip area, the later are relatively large and slow. We have instead elected to implement a second auxiliary driver DAC and extra receiver isolation switches. The reference impedance can then be perma-

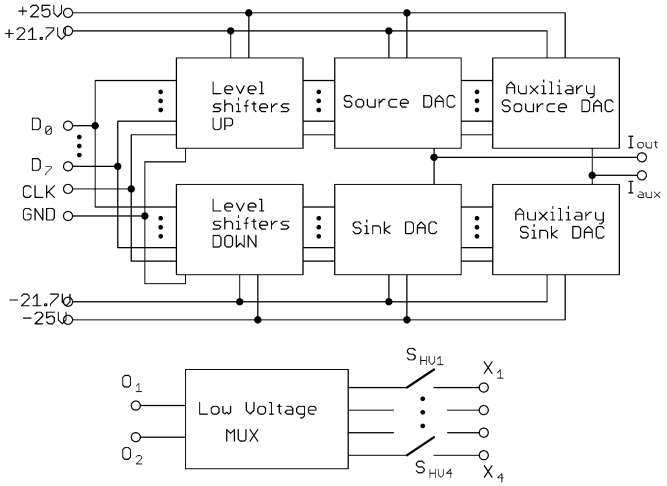


Fig. 2. Block diagram of the proposed IC. $D_7 \ldots D_0$ are data inputs, $CLK$ is the sample clock. $I_{out}$ and $I_{aux}$ are the main and auxiliary outputs, respectively. The low voltage multiplexer is isolated from the high voltages present at the inputs $X$ during transmission by the high voltage switches $S_{HV}$. $O$ are outputs to externally connected LNAs.

nently connected to this extra input/output node, eliminating the need for switches. This arrangement relies on a high degree of matching between the main and the auxiliary channels. In this work this is achieved by implementing the main and the auxiliary drivers as DACs directly driving the outputs, using shared clock signals and bias voltages.

## IV. Implementation

Fig. 2 presents a block diagram illustrating the basic building blocks of the presented IC. All functions except the data for the DACs are controlled through an on-chip shift register. This register controls for example power down of the level shifters and the DACs as well as all individual control signals for the analog switches. Details on the implementation of different blocks are given in the following subsections.

### A. HV-DAC

The circuit drives the output directly from a DAC with a high output current and a large output voltage swing. The selected solution eliminates the need for an intermediate power amplifier stage between the DAC and the output. This reduces the clock to output delay and, much more importantly, reduces the delay variations between DACs on the same die which is critical when attempting to calibrate the driver against the on-chip auxiliary driver.

Bipolar output current was implemented using one sink (NMOS) and one source (PMOS) DAC per output. These operate from −25 V and +25 V supplies, respectively. The DACs use a segmentation of 63 unary current sources controlled using a 6-bit thermometer code, and two binary weighted LSB at 1/2 and 1/4 of the unary current source size. Fig. 3 shows the architecture of the sink DAC, the source DAC was implemented using essentially the same structure. The sink and source unary current sources as used for the thermometer coded 6 MSB is shown in Fig. 4. The buffers are powered from the floating 3.3 V supplies and are essential in achieving high switching speed. The structure of the auxiliary driver is identical except

thermo code用来控制Iout

15个current source

it only contains 15 unary current sources, implementing 1/4 of the output current capability at a 6-bit resolution.

One advantage of a segmented current source DAC is that glitches generated when the output word changes mainly contribute to the linear (gain) error and do not significantly affect linearity because the number of switching current sources depends directly on the change in the input data [6]. This is especially important in a design in which the RF characteristic of the switch transistors is not fully specified and large process variations are expected, because these factors make it very difficult to achieve glitch-free switching or even to reliably estimate the glitch magnitude from simulations.

The main disadvantage of the selected approach is the distortion generated as the output impedance of the DAC changes as a function of the number of active current sources [10]. While using differential DACs with one output terminated to a supply can offer advantages in terms of speed [11], the marginal improvements observed in simulations did not justify the additional area and circuit complexity.

Some care is neccecary when powering the device up or down, in order to ensure that no significant spurious output current pulses are generated. One option would be to use the sink DAC for input words “below zero” and vice versa for the source DAC (in a “Class-B” fashion). Using this approach, no current flows through the DACs when the code corresponding to zero total output current is used, and no special power-up/down handling is necessary. Unfortunately, any mismatch in average gain between the DACs results in severe INL degradation.

Another option is to use the DACs in anti-phase (more similar to “class-A” amplifier operation) where the upper DAC provides a current $1 - I$ and the lower DAC provides $I$ (normalized to full-scale output current). Here, a gain mismatch does not affect linearity, but a (normalized) current of 0.5 flows through each DAC when the net output current is zero. Thus, the DACs need to be powered down when not in use. As both the sink and the source current are generated directly by DACs, it is simple to perform a gentle transition between zero and 0.5 (normalized) “bias” current, minimizing the spectral contents of the glitch generated due to any mismatch between the DACs. This latter “class-A” mode of operation was used in all the chip measurements presented below.

To achieve fast switching, to avoid having to level-shift the decoded data, and to enable synchronization of the data before driving the unit current sources, floating 3.3 V logic was used. This includes thermometer decoding, synchronization latches, and gate-drivers; all of which operate from 3.3 V supplies at +25 V and −25 V. Because the average supply current of the floating logic is extremely low, off-chip shunt regulators in combination with moderately large decoupling capacitors are sufficient to generate these supplies.

Gate oxide thickness/dopant concentration gradients and other effects tend to modulate the current of the unary current sources that form MSBs of the DAC as a function of position. If these current sources are switched on with a strong correlation between position and input value, the linearity of the DAC will degrade [12]. A number of solutions to this problem have been proposed and implemented [13]–[15]. Whereas the earliest methods used the simple solution of separate shuffling of the

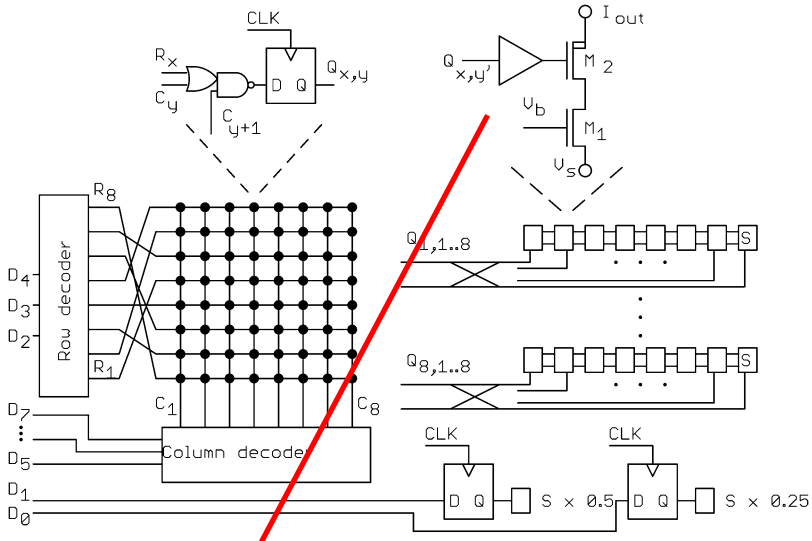


Fig. 3. The architecture of the sink portion of the main DAC. All the logic shown here operates from a 3.3 V supply with ground at −25 V. The data signals $D_4 \ldots D_2$ and $D_7 \ldots D_5$ are decoded to 8 level thermometer code for the rows $(R_y)$ and the columns $(C_x)$ of the main decoder matrix ($R_1$ and $C_1$ are always active). The output from the row thermometer decoder $(R1 \ldots 8)$ and the outputs from each row of the main decoder matrix $(Q_{x,y})$ were scrambled. This greatly simplifies routing compared to arbitrary switch scrambling, but still achieves good tolerance to transistor parameter gradients. All the output nodes $(I_{out})$ are connected, as are all the source nodes $(V_s)$.

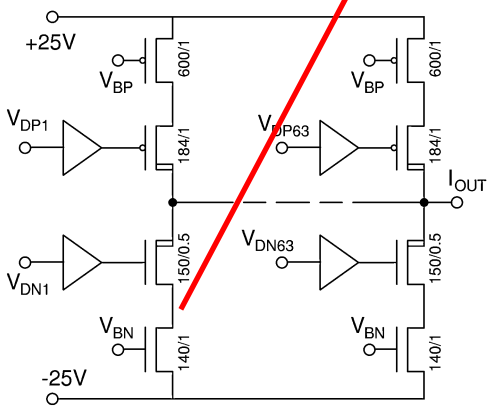


Fig. 4. Unary current sources of the sink and source DACs, binary weighted 2 LSB not shown. $V_{BP}$ and $V_{BN}$ are the bias voltages that set the output current. The input signals $V_{DP1...63}$ and $V_{DN1...63}$ for the floating buffers are generated by the decoder matrix shown in Fig. 3.

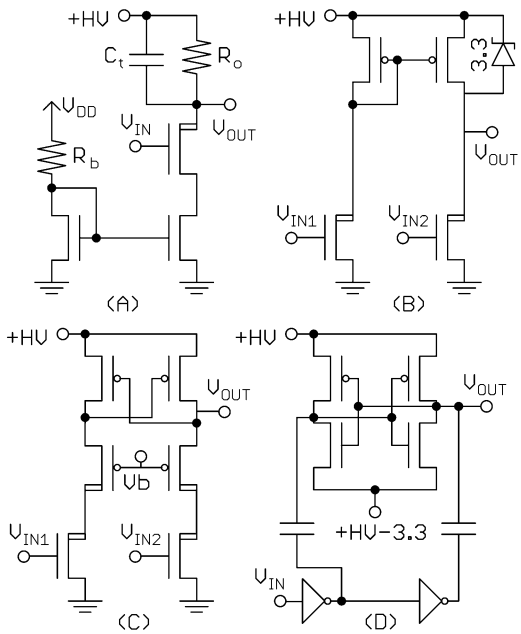


Fig. 5. Common level shift circuits; (a) is used in this work to level shift data and control signals. The value of the bias resistor $R_b$ is selected to yield a 3.3 V drop over the load resistor $R_o$. Additional capacitance $(C_t)$ was added to the output node in order to reduce bandwidth and improve high frequency PSRR.

rows and columns of the DAC, better results can generally be achieved by scrambling the source positions in a more arbitrary manner at the cost of much higher routing and/or decoding logic complexity. As a compromise, a sequence was chosen in which the elements on each row, and then the rows themselves are shuffled, but the set of elements present in each row remain fixed (Fig. 3). This allows row-column decoding to be used (placed outside the array of switches), and only requires at most 8 signals (in the case of a 6-bit unary DAC) to change positions at any one point.

### B. Level Shifters

The use of floating logic makes it is necessary to level shift the sample clock, data and some control signals up or down to each DAC. As the current through the DAC can change by as much as 400 mA in a few nanoseconds, the high-voltage supplies are expected to be very noisy. Thus, good power supply noise tolerance was deemed critical when implementing the level-shift circuits.

Common level shift circuits (Fig. 5) often use one or more current source(s) controlled by the signal to be level-shifted, with resistors, (zener-) diodes, cross-connected MOSFETs, or current mirrors as loads [16]. Four-phase circuits have also been reported in which each phase discharges the next [17], as well as capacitive level-shifters [18].

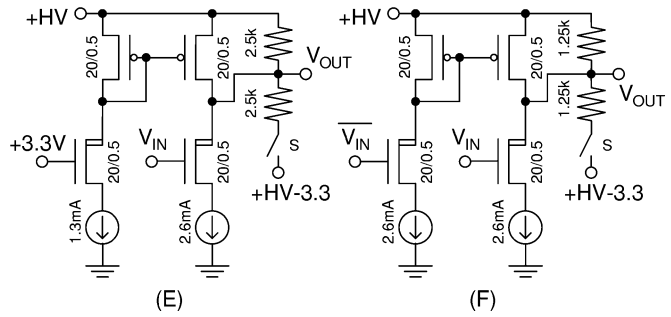


Fig. 6. Level shift circuits with improved noise tolerance; (E) was used in this work for level-shifting clock signals.

The main advantage of circuits (B) and (C) in Fig. 5 is the reduced or eliminated static power dissipation with a minimal sacrifice in terms of speed. However, for our application in which the power consumption of the level-shifters is of little interest, the simplicity and small area of circuit (A) were deemed preferable for level-shifting data-bits and control signals. Capacitive level-shifting as shown in Fig. 5(d) was rejected because any power supply noise is added directly to the control signal, which yields poor high-frequency noise tolerance.

In contrast to the data signals, which only need to meet setup and hold times of the buffers following the level-shifters, the clock signal is very sensitive to jitter which can cause the performance of the DAC to deteriorate. For this work we have evaluated the merits of using balanced level shifters. The circuit in Fig. 6(e) uses a fixed mid-level current at one input and applies the clock signal at the other input, whereas (F) applies a differential clock signal at both inputs. The signal $s$ is used to power down the level shifters, as a significant current would otherwise be drawn from the floating supply even when the DAC is inactive. The bias currents that determine the output signal level are set using a current mirror driven by a resistor of the same type as used for the load.

Fig. 7 shows simulation results for power supply noise tolerance of these circuits, and of the circuit in Fig. 5(a). The circuits were evaluated in terms of (RMS) rising/falling edge jitter, with a 1 V amplitude sine wave disturbance added to the HV supply. The circuit in Fig. 5(a) was scaled to the same power consumption and HV transistor size as the other two circuits. Because of an error in an earlier version of this data, circuit (E) was thought to be superior at the time of tape-out and was used on the chip presented in this work.

By driving both the main and the auxiliary DACs from the same clock level shifters any slow delay variations affect the main DAC and the auxiliary DAC equally, and can thus be mitigated completely as outlined in Section III.

Almost identical circuits were used to level-shift the signals down to the −25 V supply rail. All level shifted signals were buffered using inverters and latches operating at the 3.3 V supply floating at the respective rail.

### C. Analog Switches

The analog switches used to disconnect the signal routing and receiver circuitry from the excitation signal were implemented using "thick" gate oxide HV NMOS transistors sized for a total

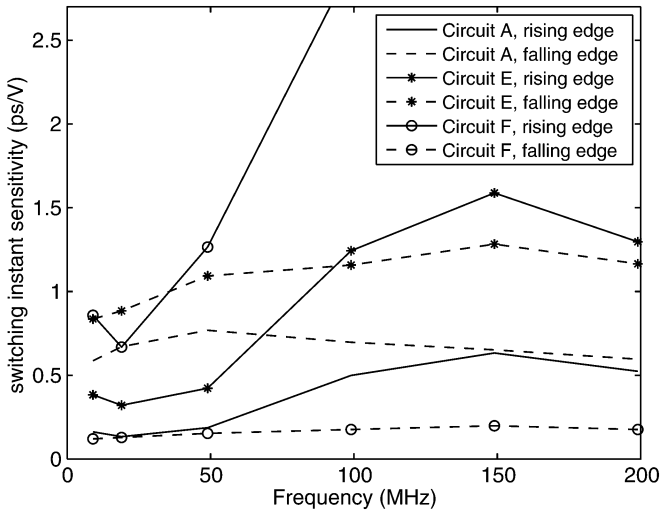


Fig. 7. Simulated RMS clock jitter as a function of frequency of the sinusoidal disturbance (1 V amplitude) added to the HV supply.

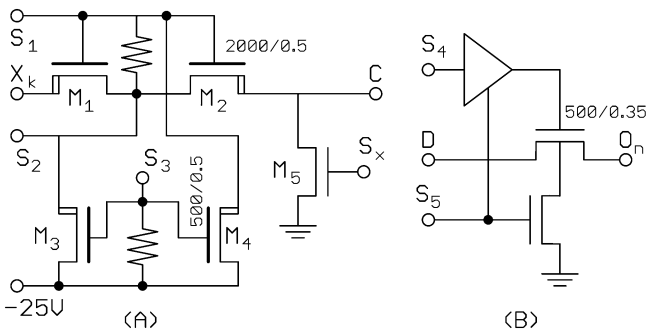


Fig. 8. (a) 50 V switch circuit. (b) Low voltage switch circuit. Two low-voltage switches (node $D$) are connected to each high-voltage switch output (node $C$), forming the multiplexer. Control signals $S_1 \ldots S_3$ are activated by sinking or sourcing the appropriate amount of current. In order to achieve full supply voltage tolerance this current is buffered using a HV current mirror at the appropriate HV supply. $S_4$, $S_5$ and $S_x$ are controlled by logic level signals directly.

on-resistance of approximately 20 Ω. The floating gate drive voltage (≈15 V) was generated directly as the voltage drop over a resistor [Fig. 8(a)].

Although high-voltage analog switch drivers without static power consumption have been published [19], [20], the increased complexity of these drivers could not be justified in this design. Instead, fairly large (800 kΩ) resistor loads implemented using high-resistivity poly-silicon allowed us to achieve static power consumption from the 50 V supply of 20 $\mu$A (1 mW), which is significantly lower than the power that either an off-chip low noise amplifier or an off-chip ADC is expected to consume.

Discharging $S_1$ and $S_2$ to negative supply when the HV switch is off avoids the distortion and charge injection into the substrate which would occur if this node was left to be discharged by the input signal (through the parasitic diode of transistor $M_1$). Discharging $S_2$ also improves the isolation of the switch because junction capacitances drop with increased reverse bias. For example, simulations with a 10 MHz input signal and a 1 MΩ load show an attenuation of only 5 dB with all transistors off but the intermediate node floating at analog

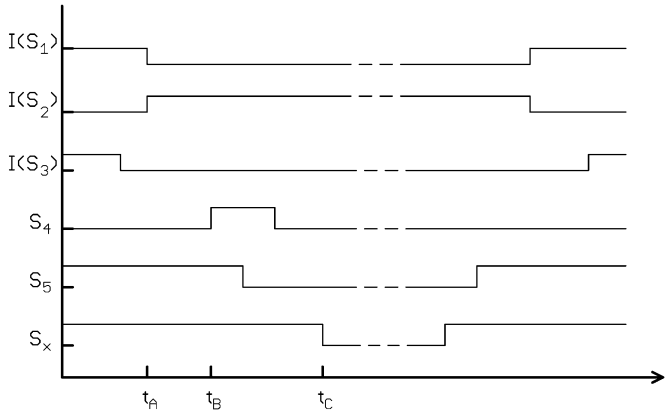


Fig. 9. Intended switching order for the control signals of the analog switches shown in Fig. 8.

ground; an attenuation of 13 dB occurs when the node has been discharged to −25 V, and an attenuation of 54 dB occurs when $M_3$ and $M_4$ are conducting. The same simulation indicates on and off capacitances (as seen from one side of the switch) of about 5 pF each. The circuit generating the current through the gate biasing resistor was designed to be slow $(\tau_r, \tau_f \approx 2\,\mu)$ to minimize the high-frequency content of any glitches generated by the switches.

The expected on-time of the switches is in the range 10 $\mu$s–1 ms. As a result, dynamic biasing of the low-voltage switches can be used [Fig. 8(b)]. In this circuit, the gate of the switch transistor (floating 3.3 V NMOS) is charged from the analog 3.3 V supply with its bulk connection connected to ground; both the gate and the bulk are then disconnected from the supply and ground, respectively. This improves linearity and reduces on-state capacitance to ground.

Each HV switch is connected to a pair of low-voltage switches that are connected to form a 4×2 multiplexer. An auxiliary transistor [$M_5$ of Fig. 8(a)] is used to ground the intermediate node between the high- and low-voltage switches when neither of the low-voltage switches are on.

The intended switching order for the control signals of the analog switches is shown in Fig. 9. First the shorting of the nodes $S_1$ and $S_2$ to the negative supply is disabled by discontinuing the sourcing of current into node $S_3$. Current is then sourced into $S_1$ and sunk from $S_2$ at $t_A$ to turn the HV switch on. The gate of the low voltage switch is charged at time $t_B$. The gate and bulk drivers for the low voltage transistor remain active while the switch is off, but are disabled after the gate has been charged, as discussed above. Once both switches are on, the transistor grounding the node that connects the low and the high voltage switches is disabled using $S_x$ at $t_C$. The shorting of this node to ground not only improves isolation, but also minimizes charge injection to the transducer and ensures that it is charged to a suitable DC level for the LNA.

## V. Results

The chip was manufactured using an AMS 50 V, 0.35 $\mu$m, CMOS process. A photograph of the chip outlining the main parts of the design is shown in Fig. 10.

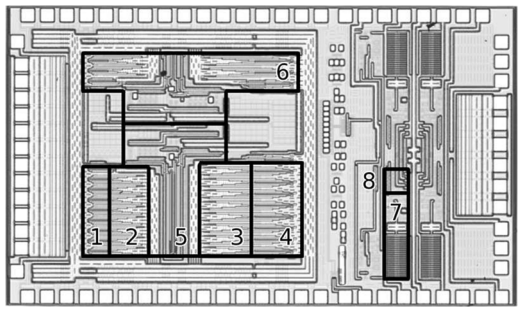


Fig. 10. Photograph of the chip presented in this paper. 1: NMOS current sources; 2: 50 V NMOS cascodes and gate drivers; 3: PMOS cascodes and gate drivers; 4: PMOS current sources; 5: level-shifters/thermometer decoding/MOSFET drivers; 6: auxiliary 4 + 2DAC; 7: 1 × 50 V NMOS analog switch; 8: 3 × 3.3 V NMOS analog switch; total chip size is 3.7 × 2.2 mm.

TABLE II
Summary of Measured Performance

| DAC: | |
|---|---|
| Output current | ± 400 mA |
| Output voltage swing | 40 $V_{pp}$ |
| Sample frequency | 150 MHz |
| Settling time constant | 2.2 ns |
| SFDR | 46 dBFS @10 MHz |
| SNDR | 37 dB @10 MHz |
| Delay matching | 12 ps |
| Analog multiplexer: | |
| On resistance | 26 Ω |
| Isolation | 90 dB @10 MHz |
| Phase delay matching | 3 ps |

The measurements of the chip have two main purposes: first, to evaluate the chip with regard to the specific targets set for this design, such as current output capacity, timing and amplitude stability, and switch isolation; and second, to evaluate the performance of the chip in standard DAC terms such as INL, SFDR and SNDR.

The three main blocks of the chip are the HV-DAC, the level-shifters, and the analog switches. As the level-shifters are completely integrated in the design, separate measurements were not possible. Thus, measurement data are presented below for the HV-DAC and the analog switches, with a summary in Table II.

### A. HV-DAC

The INL of the DAC was measured with four different load impedances (Fig. 11). For each load the bias current was adjusted to give a full-scale output voltage swing of 40 V. Note the sharp transition from the central region where nonlinearity is mainly due to finite current source output impedance to the region where the output impedance of every active switch starts dropping as the cascode transistor approaches linear (ohmic) operation.

Fig. 12 shows the current per current source estimated from the data presented in Fig. 11. In contrast to a DAC operating in “class-B” mode, the contributions of the sink and source current sources to the output current cannot be separated for

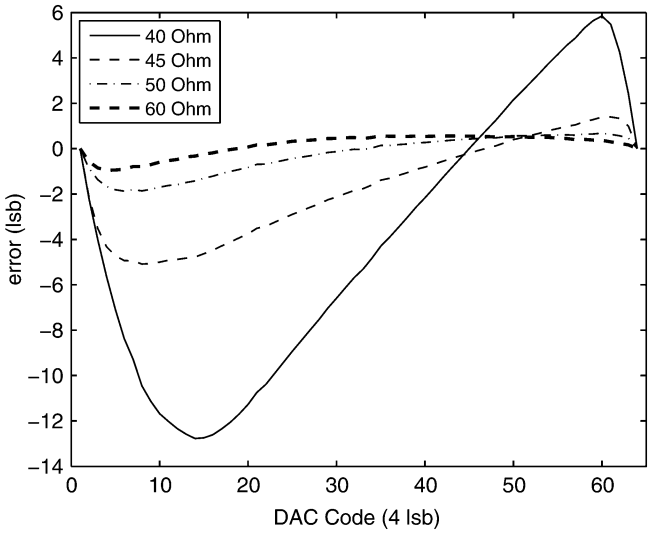


Fig. 11. INL for different load impedances with a fixed swing of 40 $V_{pp}$.

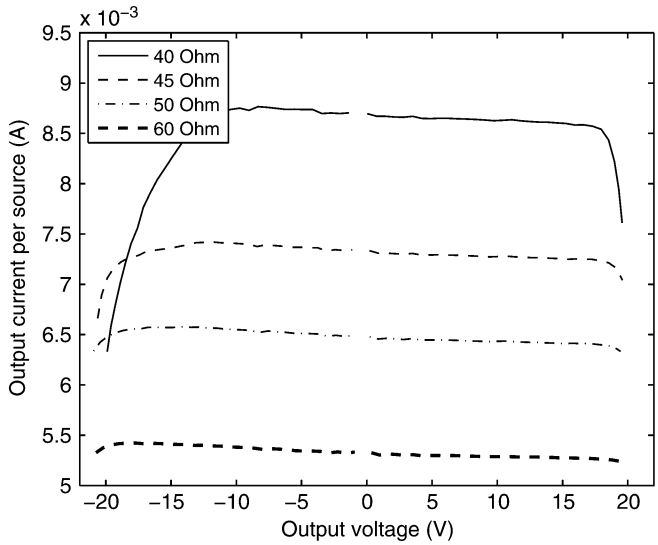


Fig. 12. Current per current source for different loads with a fixed output voltage swing of 40 $V_{pp}$.

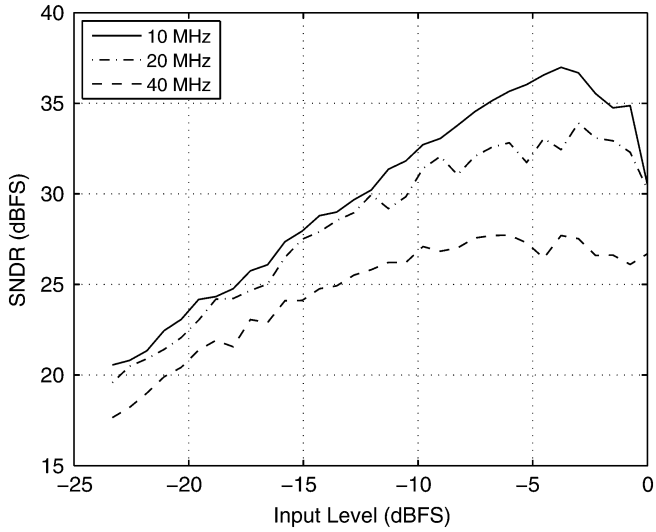


Fig. 13. SNDR, 40 $V_{pp}$ full scale with a 50 Ω load.

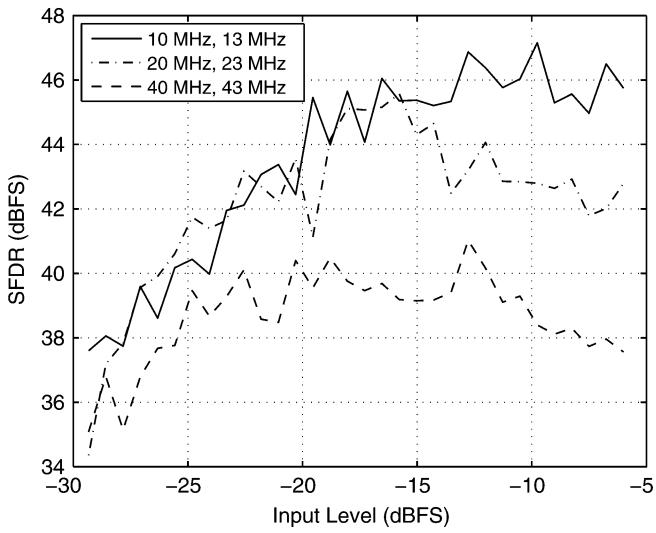


Fig. 14. Two-tone SFDR, 40 $V_{pp}$ full scale with a 50 Ω load.

this "class-A" mode DAC. However, the deviations from the ideal output current will in practice be dominated by the current sources with the smaller voltage drop. This representation shows the effects of operating too close to the supplies and demonstrates the relationship between output current and required headroom. It is also interesting to note that the linear trend in the middle portion of the curves corresponds directly to the finite output-impedance of the current sources of the DAC, and to the quadratic trends seen in Fig. 11.

The results in Fig. 11 and Fig. 12 indicate a maximum usable output current for a swing of 40 $V_{pp}$ of about 6.5 mA per unary source, which yields a total of ±410 mA from 63 sink and 63 source unary current sources; the effect of the 2 binary weighted LSBs is ignored. Compared to simulations performed using a typical mean setting, this corresponds to an almost two-fold lower output current capability of the manufactured circuit. On the other hand, a worst-case simulation indicates an output current capability in the order of 660 mA. Part of the remaining discrepancy with measured results can be attributed to a documented model inaccuracy for the high voltage transistors. In addition to a direct effect on the output current the inaccuracy also makes the simulation under-estimate the output resistance of the HV current sources. This leads to over-estimation of the INL in the simulation, which to some extent masks the effects of dropping output current at high output voltage swing.

High-frequency performance was evaluated in terms of SNDR and two-tone SFDR as shown in Fig. 13 and Fig. 14. The measurements were performed with a 150 MHz sample rate, a 50 Ω load and biasing selected to yield a 40 $V_{pp}$ full scale output voltage swing. As both linearity and noise degrade sharply as the signal frequency reaches 40 MHz, operation at higher output frequencies should be limited to applications that tolerate excitation waveform distortion and uncertainties.

Band limited pulses selected to resemble waveforms used in practical ultrasonic measurement applications (Fig. 15) were used to evaluate amplitude stability and delay matching between the main and auxiliary DAC on the same die. As

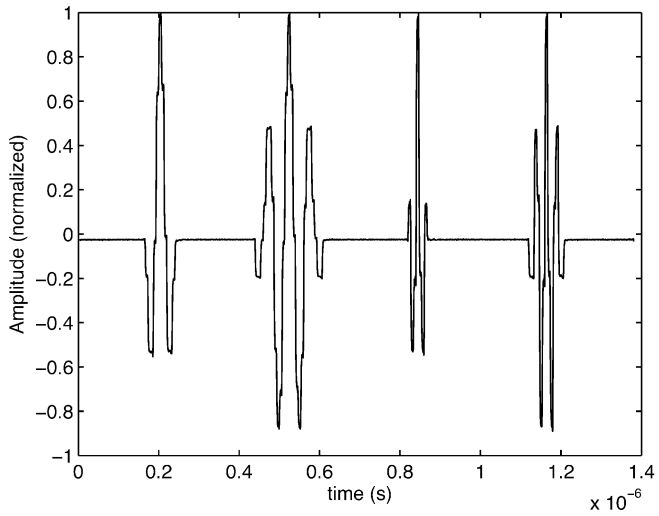


Fig. 15. Pulse waveforms used to evaluate DAC delay and amplitude variations.

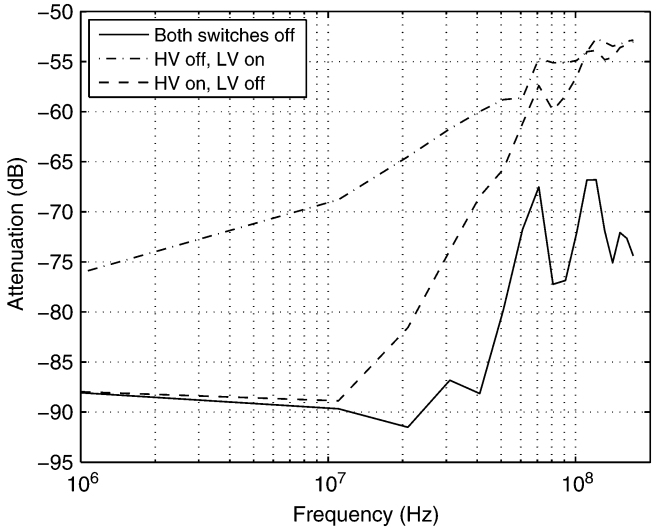


Fig. 17. Switch attenuation, 50 Ω load.

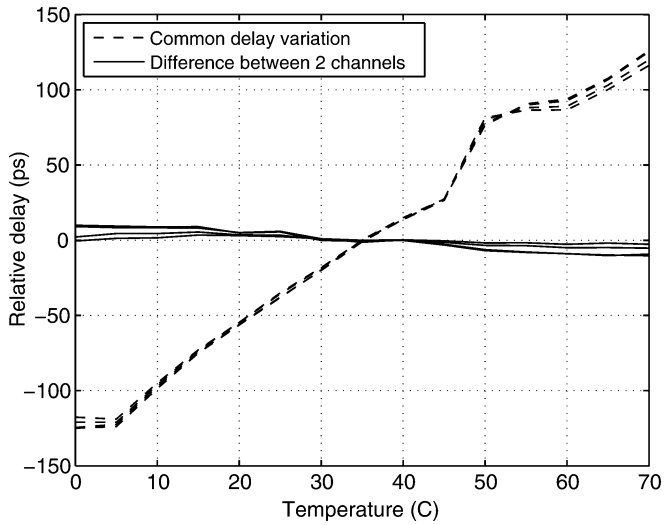


Fig. 16. DAC output delay variations and differences between main and auxiliary DACs on the same chip.

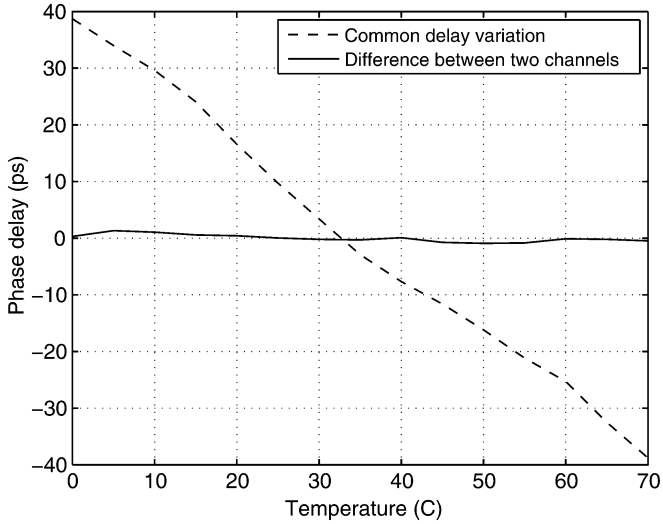


Fig. 18. Phase delay variation over temperature, and its difference between two channels of the analog multiplexer, at 9 MHz.

illustrated by Fig. 16, the delay changes up to 250 ps over the range 0–70 °C, but the difference between the two DACs remains below 21 ps. Similarly, but much less dramatically, the output amplitude varies with temperature by about 3%, and the two outputs are within about 1.5% of each other.

### *B. Analog Switches*

As shown in Fig. 17, the off isolation of both the 50 V NMOS and the regular 3.3 V NMOS switches is fairly good at low frequencies, but degrades as the frequency increases. However, the attenuation of the series combination of both switches remains high over the measured frequency range. The measured on-resistance is 26 Ω for the series combination of one HV and one LV switch, which agrees well with the simulations. Only the combined capacitance of the DAC output and one switch was available for direct measurement, yielding about 36 pF. This compares favorably to the corresponding simulated total capacitance of 44 pF, where 5 pF stems from the HV switch and the remaining 39 pF is the output capacitance of the DAC.

The temperature stability and the matching over temperature of the channels of the multiplexer were measured over the 0–70 °C range. This measurement was performed with an off-chip high-input impedance buffer connected to the output of the multiplexer. The buffer presents the output of the multiplexer with a load of 10 kΩ in parallel with a capacitance of about 2 pF. As seen in Fig. 18, the phase delay of a single switch varies significantly as the temperature changes, but the matching between channels is very good, with less than 3 ps of difference as the frequency ranges from 5 to 40 MHz, which is an improvement by a factor 30 on average. Moreover, the matching is approximately 6 times better than the already highly acceptable matching of the DACs; thus, we conclude that the on-chip multiplexer can be used for signal routing when calibrating the system.

The amount of time the low-voltage switches can remain on is limited by the time it takes for the gate charge to leak out. As this leakage depends on temperature, the maximum on-time depends on the operating temperature. For example, the measured maximum on-time at room temperature is 0.4 s, and it drops rapidly to about 15 ms at 100 °C.

## VI. Comparison to Other Work

The presented chip incorporates a fast high voltage DAC and high voltage isolation switches. Although we have found no devices with the same functionality available for direct comparison, the performance of the main blocks can be compared to relevant parts of other published works.

The speed of the presented DAC is limited by the performance of the high voltage transistors available in this process. Thus, it is hardly surprising that a regular differential segmented current output DAC implemented using 0.35 $\mu$m CMOS such as [6] is significantly faster and achieve higher output impedance per current source, as required for high linearity. The presented DAC is however considerably faster than any previously published high-voltage DAC known to the authors: In [21] a 0–40 V "11/12-bit" R-2R DAC is reported. This design exhibits a conversion time of 4 $\mu$s. The much higher output voltage (300 V) DAC of [22] similarly exhibits an output settling time constant in the order of 2.5 $\mu$s. In comparison, our work achieves a settling time constant of about 2.2 ns and a sample rate of 150 MHz. We attribute this improvement to the use of floating 3.3 V supplies used for buffering the control signals for the current sources. This allows significantly faster charging and discharging of the large gate capacitances than would be realistic when driving the high-voltage transistors directly from the level-shifters.

The high voltage isolation switches implemented in this work are similar to the switches presented in [20], where a 32×32 array of high voltage switches without static power dissipation achieves an isolation at 4 MHz of ≈40 dB, or 53 dB with a transistor shorting the output to ground active. This should be compared to better than 70 dB for our high voltage switches and better than 85 dB for the whole LV-HV switch combination used in this work.

## VII. Conclusions

We have presented an ultrasonic transducer interface IC for high performance ultrasonic measurement applications. The device has an integrated 8-bit, 40 $V_{pp}$, ±400 mA current output DAC for arbitrary waveform transducer excitation. The IC also hosts a ±25 V analog multiplexer that allow receiver isolation during transmission as well as injecting auxiliary signals into the receiver chain for calibration purposes. This multiplexer together with an auxiliary on-chip DAC, allows the device to be calibrated for clock-to-output delay and receiver phase delay variations, both in single and multi-channel systems.

These results show that integrating a complete high voltage arbitrary waveform ultrasonic transducer interface IC is both feasible and practically achievable. With a size of 3.7×2.2 mm, the chip also offers a clear size reduction over traditional discrete designs.

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