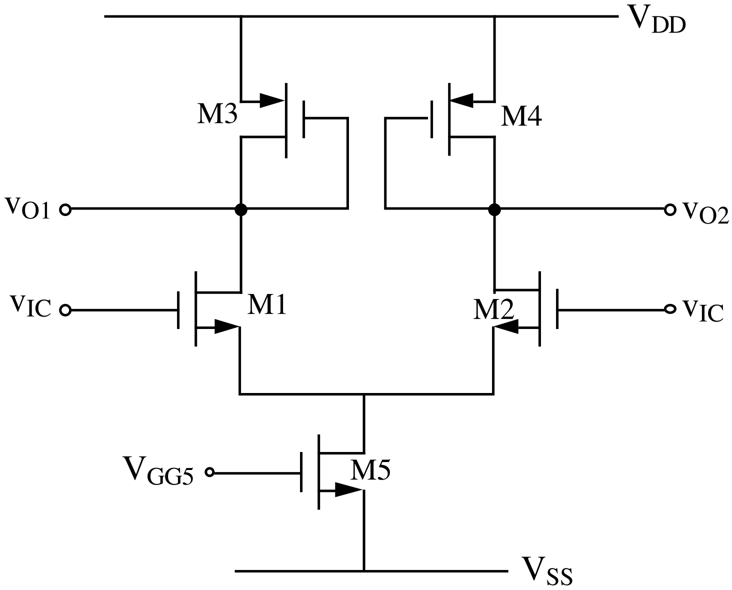
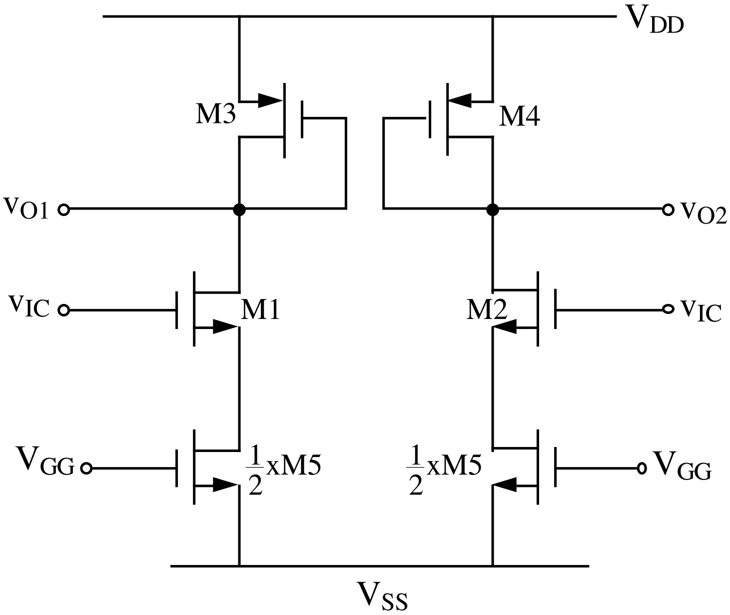
CMOS DIFFERENTIAL AMPLIFIER

Consider the following differential amplifier -



Use of symmetry to simplify gain calculations -



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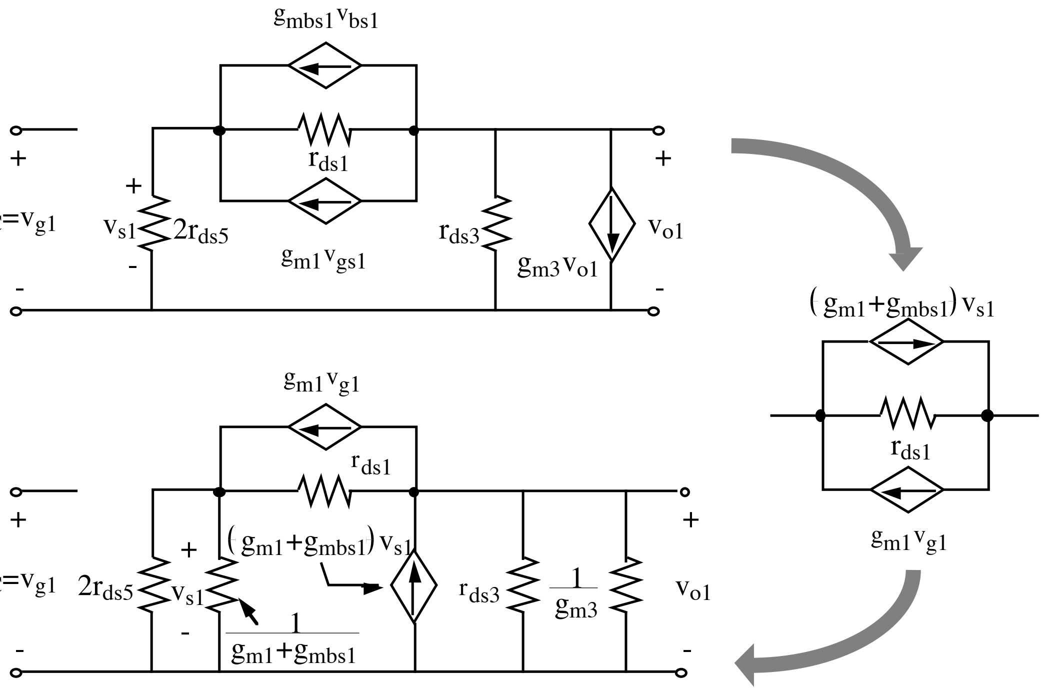
Small signal model -



Writing nodal equations -

$$\left[0.5g_{ds} + g_{ds1} + g_{mbs1}\right] v_{s1} - \left[g_{ds1}\right] v_{o1} = g_{m1}v_{IC}$$
$$-\left[g_{ds1} + g_{m1} + g_{mbs1}\right] v_{o1} + \left[g_{ds1} + g_{ds3} + g_{m3}\right] v_{o1} = -g_{m1}v_{IC}$$

Solving for $\frac{v_{o1}}{v_{IC}}$ gives,

$$\frac{v_{o1}}{v_{IC}} = \frac{-0.5g_{m1}g_{ds5}}{(g_{ds3}+g_{m3})\left[0.5g_{ds} + g_{m1} + g_{mbs1} + g_{ds1}\right] + 0.5g_{ds1}g_{ds5}}$$

or

$$\frac{v_{o1}}{v_{IC}} \approx \frac{-0.5g_{m1}g_{ds5}}{g_{m3}(g_{m1} + g_{mbs1})} \approx \frac{-g_{ds5}}{2g_{m3}}$$

COMMON MODE REJECTION RATIO (CMRR)

$$\text{CMRR} = \frac{\text{Differential mode gain}}{\text{Common mode gain}} = \frac{A_{vd}}{A_{vc}}$$

For the previous example,

$$|\text{CMRR}| = \frac{\left(\dfrac{g_{m1}}{g_{m3}}\right)}{\left(\dfrac{g_{m1}g_{ds5}}{2g_{m3}(g_{m1} + g_{mbs1})}\right)} = \frac{2(g_{m1} + g_{mbs1})}{g_{ds5}} \approx \frac{2g_{m1}}{g_{ds5}}$$

Therefore, current sinks/sources with a larger output resistance(r_{ds5}) will increase the CMRR.

Example

Let all W/L ratios be unity, I_{SS} = 100µA, and use the values of Table 3.1-2 to find the CMRR of a CMOS differential amplifier.

$$g_{m1} = \sqrt{2\text{x}17(\mu\text{A/V}^2)\text{x}100\mu\text{A}} = 58.3\mu\text{S}$$

$$g_{ds5} = 0.01\text{V}^{-1} \text{ x } 100\mu\text{A} = 1\mu\text{S}$$

Therefore, |CMRR| = 116