Advanced Expedition PCB

Module 1

Graphics and Board Outlines

April 2005

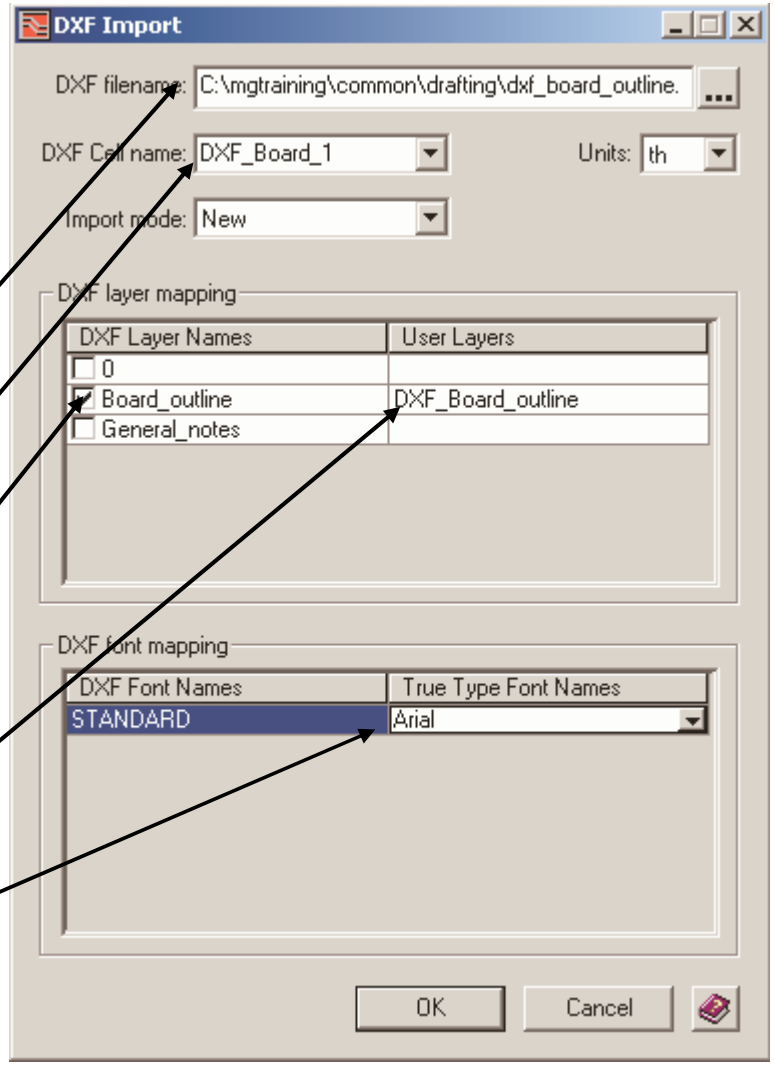
Objectives

Upon completion of this lesson and lab, you will be able to:

- **Understand the DXF In function of Expedition PCB**
- **Effectively use the graphics Snap commands in Expedition PCB**
- **Use Graphics commands to compose or decompose polygons**
- **Create complex graphical Board Outlines in Expedition PCB.**
- **Create a Route Border from existing Board Outline Graphics**
- **Create Contour (Cutout) elements in Expedition PCB**

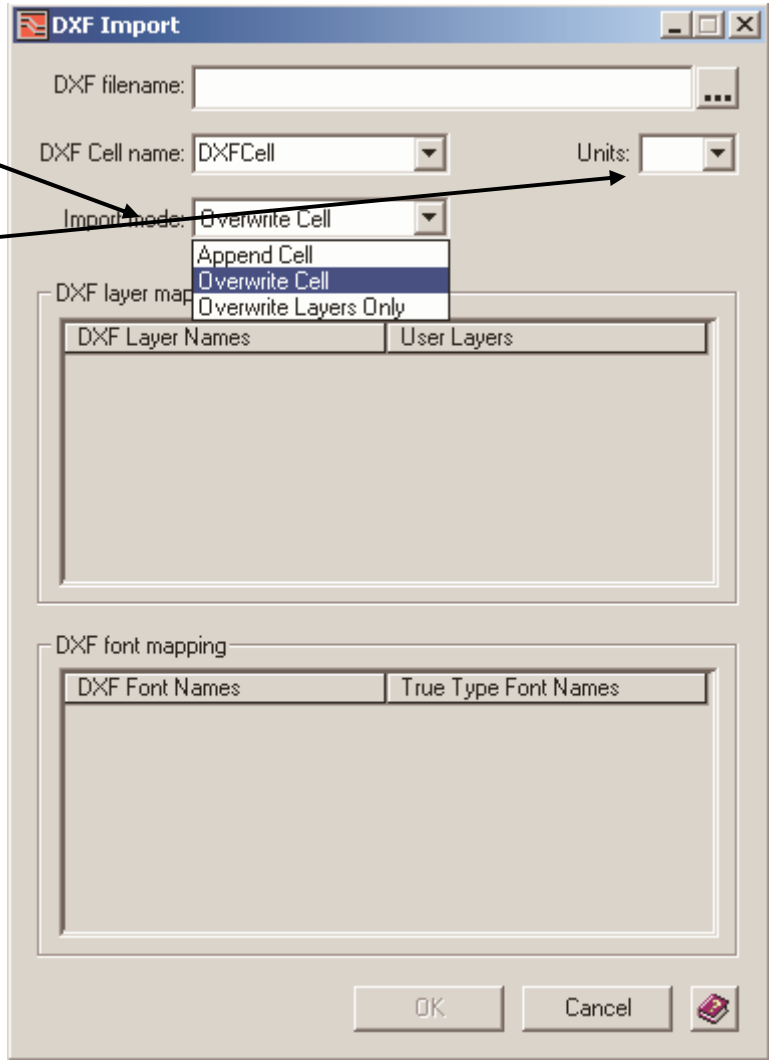
DXF In

- **DXF (Drawing Interchange) is a file format created by AutoDesk, Inc. which you can use to exchange data between Expedition PCB and many CAD and graphical applications.**
  - **Enter or browse to the DXF file location**
  - **Enter Drawing Cell name to be created and Import Mode for that cell**
  - **Enable a DXF file layer for import by checking the box.**
  - **DXF data is only allowed to be imported onto user defined layers.**
  - **Enable Font substitution.**



DXF In (Cont.)

- **Select the Import mode.**
  - **DXF graphics is imported as a drawing cell**
  - **Make sure units are set correctly.**
  - **DXF cell names must start with characters “DXF”**
  - **DXF cells are then placed using the Place > Place Parts and Cells command**
- **Imported Elements are:**
  - **Line**
  - **Arc**
  - **Polygon**
  - **Text**
  - **Dimensions - converted to polylines**
  - **Circles**
  - **Ellipse - converted to arcs**

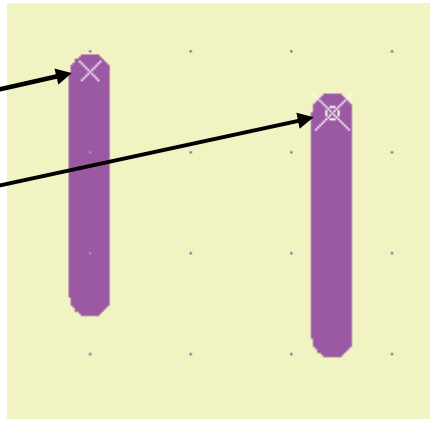


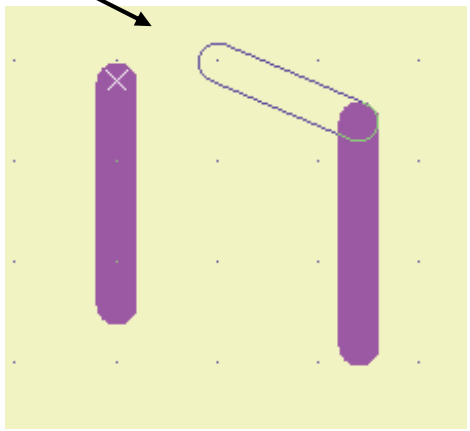
DXF In (Cont.)

- **Using DXF Input as the Board Outline**
  - **Import the DXF Cell**
  - **Place the DXF in the Design**
    - **Make sure it is placed correctly relative to the origin**
  - **Select the Board Outline graphics in the DXF cell in Draw Mode and copy the graphics out of the cell**
    - **Make sure it is a closed element**
  - **Select the copied graphics and change its type to Board Outline.**

Snap Commands

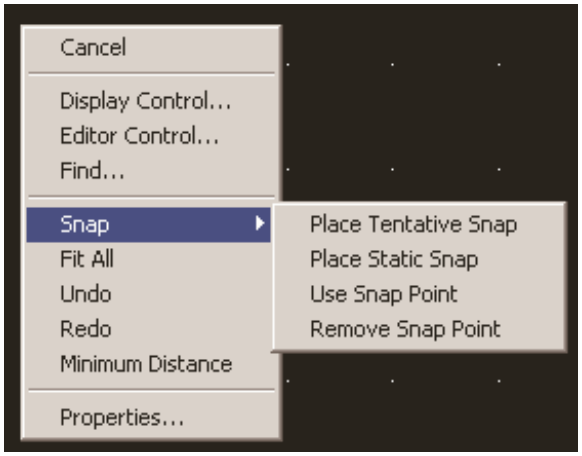
- **Snap allows graphics to snap into key points of existing graphics.**
  - **Set the point**
  - **Snap to the point**
- **Concepts**
  - **Static Snap Point**
  - **Tentative Snap Point**
  - **Snap Point Priority**
    - **Uses Tentative Snap Point first.**





Snap Commands (Cont.)

- **Snap Points can be placed and used via keyboard or pop-up commands.**
  - **Set the point**
    - **Tentative Snap Point**
      - **Chose command from pop-up menu.**
      - **Click on the element to snap to.**
    - **Static Snap Point**
      - **Choose command from pop-up menu - OR - Press “s” on keyboard.**
      - **Click on the element to snap to.**
  - **Issue the command to use the snap point.**
  - **Use the snap point**
    - **Choose command from pop-up menu OR <Ctrl><Right-Click>.**

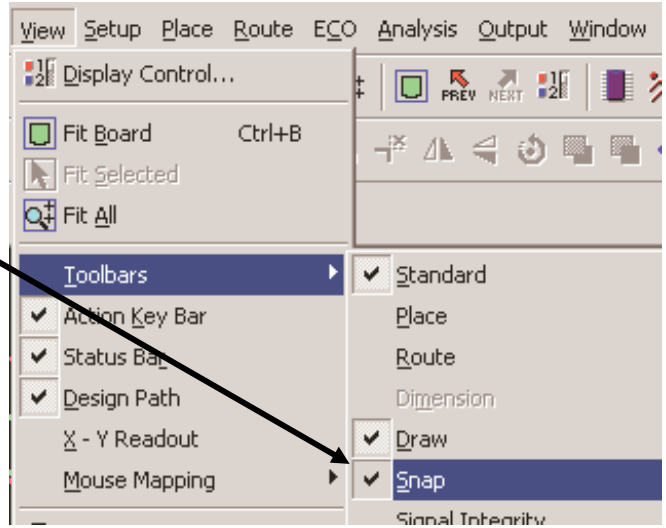


Snap Commands (Cont.)

- Snap Points can be placed while in the process of other commands.
  - Place one point for a line, then before ending the line, add a snap point to use for the second point.
- Each element has a different set of Snap Points:
  - Line - end points and center points
  - Circle - quadrant points and center point
  - Arc - quadrant points, end points, center point
  - Polygon, Polyline - any key point
- After placing a Snap Point, <Tab> to move the Snap Point to another point on the graphic element.
- There is a Snap Point at the intersection of two elements. Click close to the intersection to locate the intersection Snap Point.

Snap Command Menu

- **You can turn on a menu bar containing snap commands.**

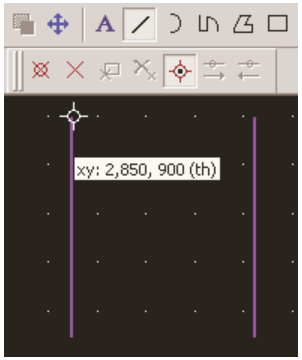


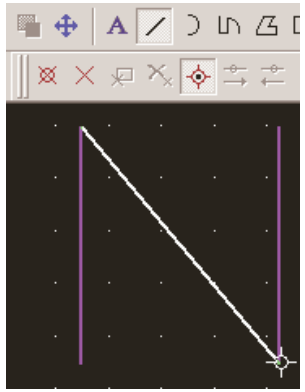
  - **Tentative Snap Point**
  - **Static Snap Point**
  - **Use Snap Point**
  - **Delete Snap Point**
    - **Follows Snap Point priority**
    - **Tentative Snap Point deletes if it is assigned.**
  - **Hover Snap toggle**
  - **Move Snap Point in either direction**
    - **Follows Snap Point priority**
    - **Tentative Snap Point moves if it is assigned.**

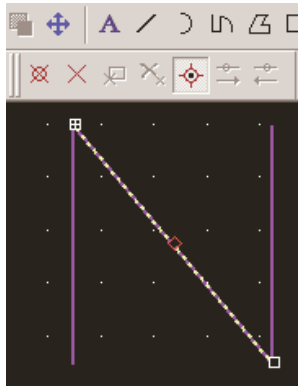
Hover Snap

- **Hover Snap is a dynamic snap mode.**
  - **Turn on Hover Snap**
  - **Issue the command - for instance Line**
  - **Move cursor near an existing element**
  - **The Hover Snap point will appear**
  - **Click the Left mouse button to use the Hover snap point**
  - **Move to next point**

- **If you put your cursor on the Hover Snap point symbol, it will report the X,Y coordinates of the key point.**





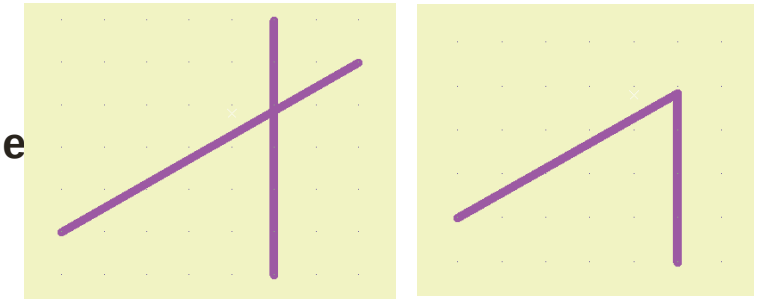


Composing Polygons

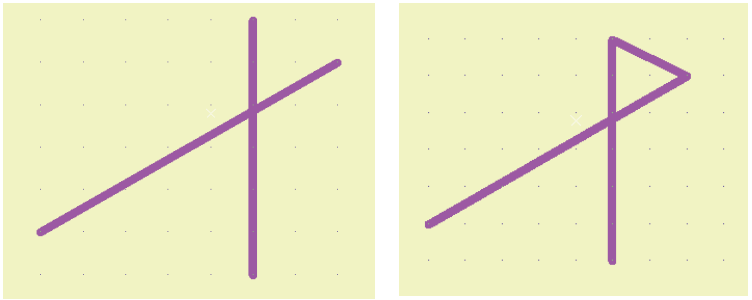
- **Many Expedition PCB items MUST be closed elements:**
  - **Board Outlines, Route Borders, Placement Obstructs, Rule Areas, etc.**
- **Draw them as closed elements (Polygons, Rectangles, Circles) OR**
- **Draw them as string elements, then compose them into a closed element.**
  - **In many cases, they must be drawn on a user defined layer, then moved to the proper layer.**
    - **Board Outline**
    - **Route Border**

Composing Polygons (Cont.)

- **Commands**
  - **Trim -**
    - **Select the two lines to trim**
    - **Lines are trimmed by cutting off the shortest ends**
    - **Lines are left as separate segments.**



  - **Join -**
    - **Select two elements to join**
    - **Lines are joined into a Polyline**
    - **If no common endpoint, a segment is drawn between the closed ends, and then the three segments are combined into a Polyline**



Composing Polygons (Cont.)

- **Commands**
  - **Create Polygon/Polyline -** 
    - **Select multiple elements with common end points.**
    - **Elements are composed into a Polyline.**
    - **If the elements create a closed area, they will be composed into a Polygon.**
  - **Dissolve Polygon/Polyline -** 
    - **Select Polygon or Polyline**
    - **Elements are broken into lines and arcs.**

Graphics Copy to Make a Board Outline

- **Because Board Outlines must be closed elements, it is not possible to draw Lines, Arcs or Polylines on the Board Outline layer.**
- **These elements must be:**
  - **Drawn on a User Defined Layer**
  - **Composed into a Polygon**
  - **Copied to the Board Outline layer**
    - **It is desirable to change a copy of the composed Polygon into the Board Outline, simplifying edits on the User Defined Layer if they become necessary.**
    - **The original Board Outline will be deleted - there can only be one Board Outline.**
- **Copy in Place**
  - **Select the element**
  - **<Ctrl><Double-click>**
  - **The copy remains selected.**

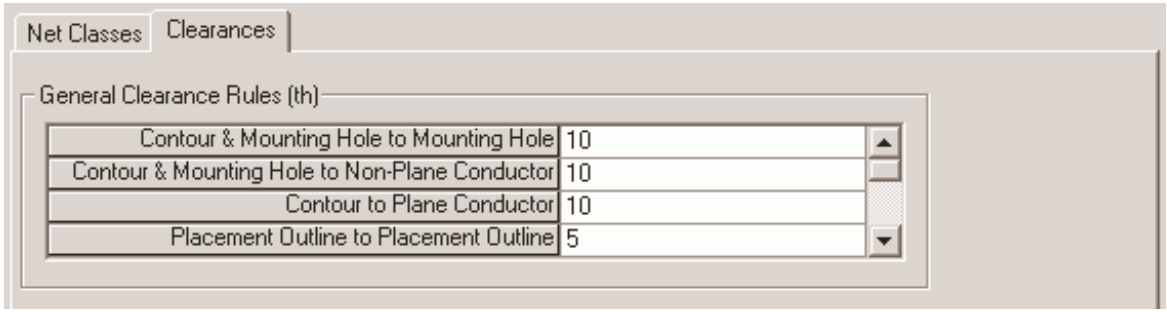
Graphics Copy to Make a Route Border

- **Many time the Route border will be exactly the same shape as the Board Outline, but slightly smaller.**
  - **Select the Board Outline.**
  - **<Crtl><Double-click> to copy the Board Outline.**
  - **The copy is put on a drafting layer and remains selected.**
  - **On the Properties dialog, change the type to Route Border.**
  - **On the Properties dialog, enter a negative value in the Grow/Shrink field to shrink the Route Border.**

- **The Original Route Border will be deleted, there can only be one Route Border.**

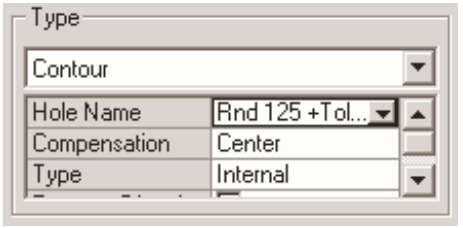
Contours

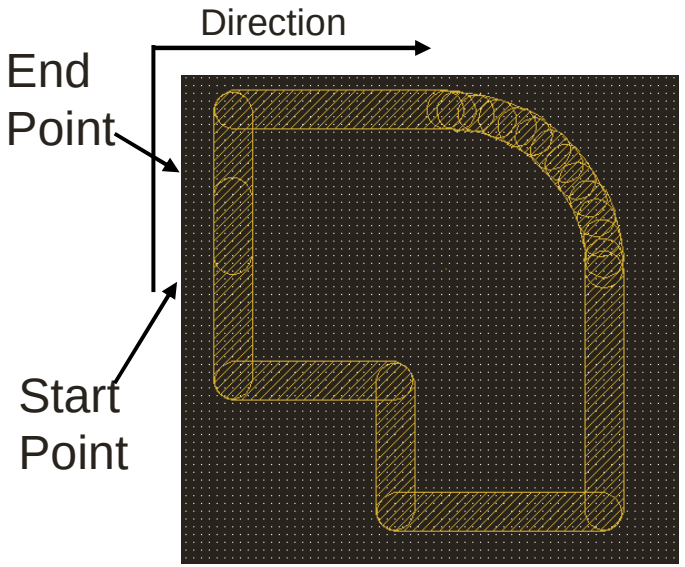
- Contours are board cutouts.
- There are two types of contours:
  - Board - represents the cut of the Board Outline.
    - NC Drill processes board types last to makes sure the board does not get cut out of the panel before the internal cuts are complete.
  - Internal - represents a cutout in the board area.
    - Treated as a Route Obstruct
- Clearances to Contours are set in Net Classes and Clearances.



Contours (Cont.)

- **Contour Properties**
  - **Hole Name - defines hole size when contour drill files are created.**
  - **Compensation - aids in the placement of the contour by allowing the contour to be placed by its Center, Left or Right sides.**
  - **Type - defined as Internal or Board.**
  - **Reverse Direction - output as the points were initially placed, or in the reverse direction from the initial placement.**



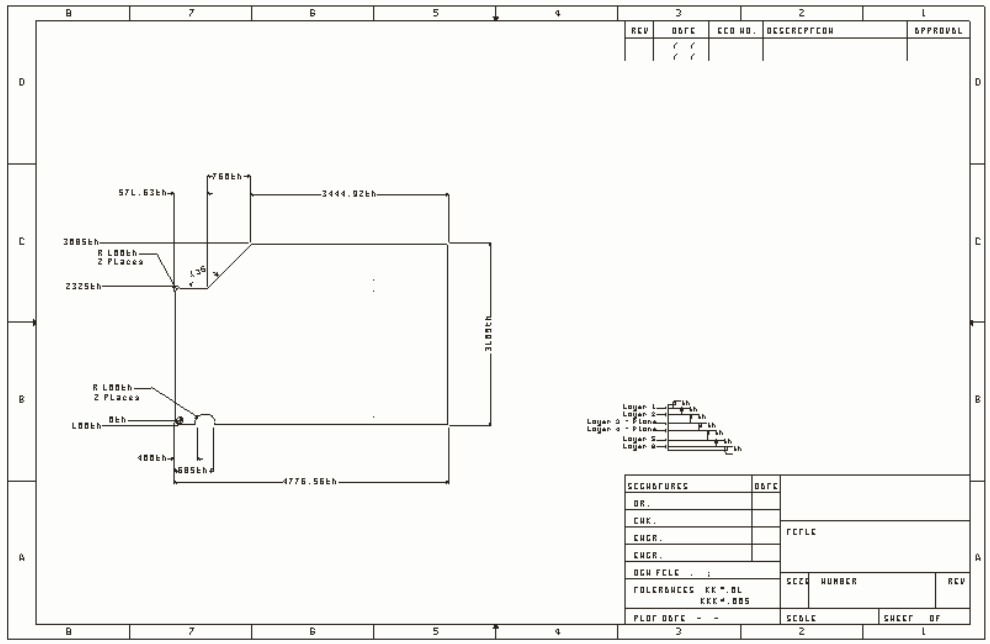


Contours (Cont.)

- **Contour Output**
  - **Output is created by the NC Drill command**
  - **All Contours created using plated hole definitions are written to a file named “ContourPlated.ncd”.**
  - **All Contours created using non-plated holes are written to a file named “ContourNonPlated.ncd”.**
  - **The Board cut definition, if any is written to the output file last.**

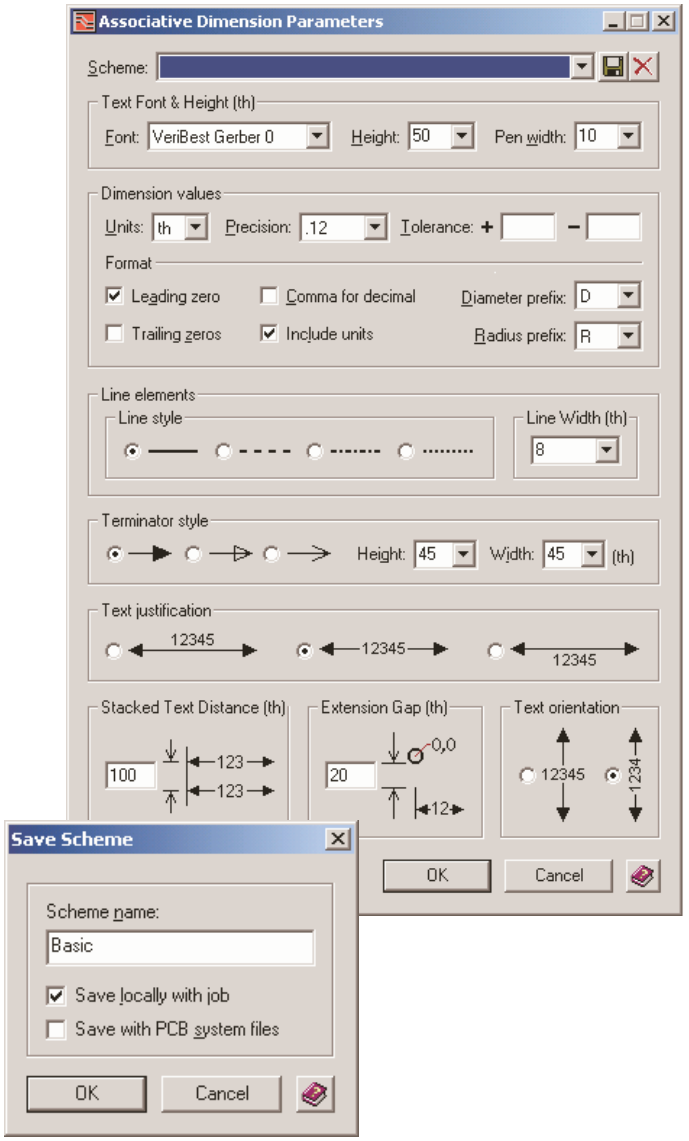
Dimension Review

- **Dimensioning is configurable.**
- **Dimensioning is available in Draw Mode**
  - **Dimensioning mode is a sub-mode of Graphics.**
- **Dimensioning Editing in Dimension mode only.**
- **Dimensions are associative.**



Dimension Review (Cont.)

- **Setup>Dimensioning Parameters OR  while in Dimension Mode.**
  - **Set Font and Height for Dimension Text**
  - **Set Units, Precision and Tolerance**
  - **Set Format Options**
  - **Set Line Style and Line Widths**
  - **Set Terminator Styles and Parameters**
  - **Set Text to Line Justification**
  - **Set Text Stacking Distance**
  - **Set the Extension Gap**
  - **Set the Text Orientation**
  - **Dimensioning Setup can be saved as a scheme.**



Dimension Review (Cont.)

- In Draw Mode, select the Dimension Icon

- Display the Dimensioning Toolbar
- Set the Dimensioning Parameters
- Set the active layer for Dimension graphics

- Select the Dimensioning Commands
- Dimensioning Commands automatically Snap to graphics because they are Associative
- Right Click to cancel Dimensioning Mode

Lab Preview

- **This Exercise has 4 Labs.**
  - **Lab 1 — DXF Import**
    - Database “control2_reva” - import a DXF file, change graphics to Board Outline, create Route Border, add Mounting Holes.
  - **Lab 2 — Creating a Board Outline from Template Graphics**
    - Database “control1_reva” - use existing graphic construction lines to draw Board Outline graphics using Hover Snap. Compose graphics into a polygon and create a Board Outline and Route Border - Add Mounting Holes.
  - **Lab 3 — Creating Contours**
    - Database “control2_reva” - copy the Board Outline - modify graphics and turn them into board cut Contours - Run NC Drill to get Contour output.

Advanced Expedition PCB

Module 2

Placement

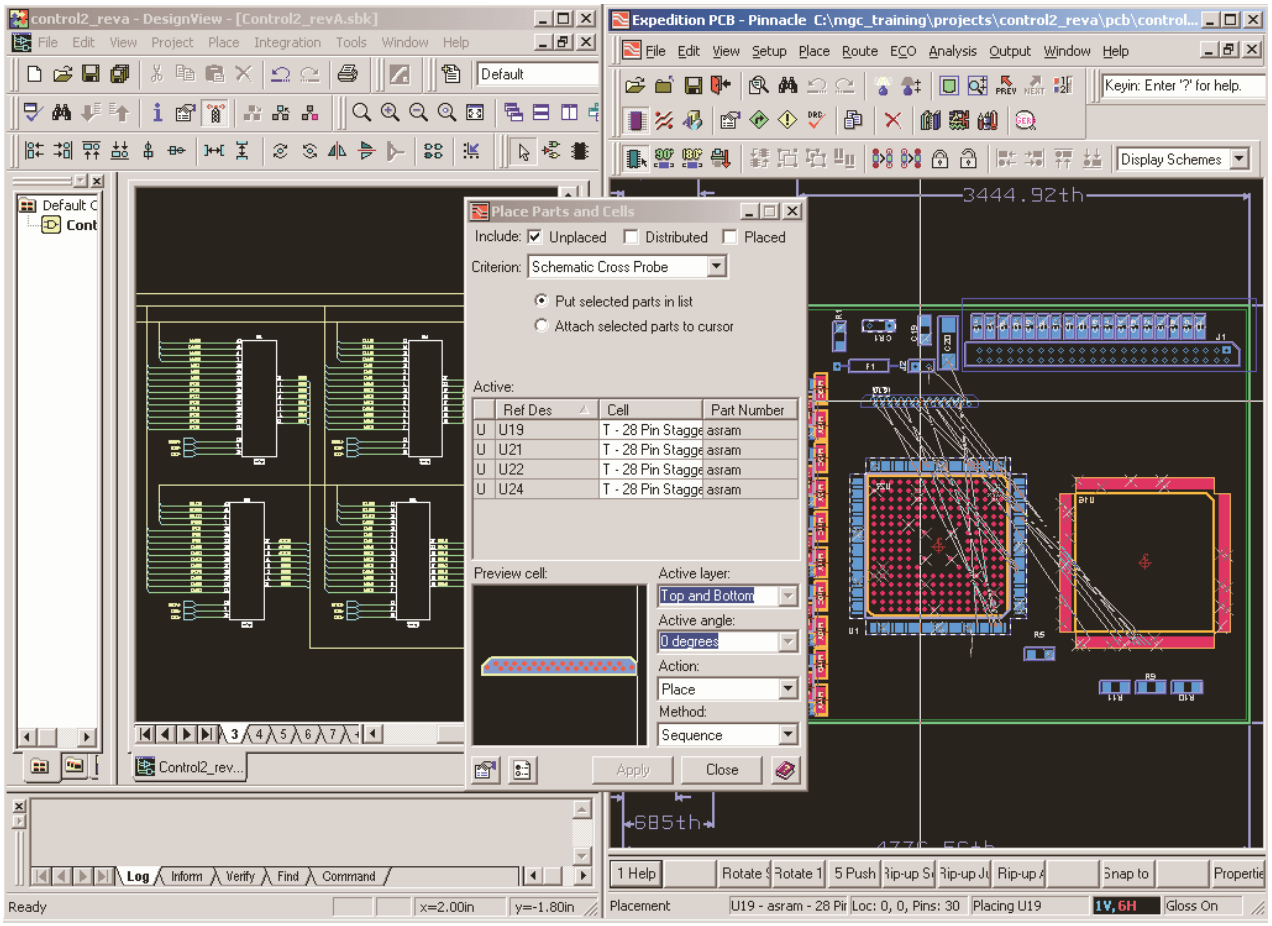
Objectives

Upon completion of this lesson and lab, you will be able to:

- **Place from the schematic.**
- **Using Placement Key-in commands.**
- **Polar Array Placement.**
- **Copy Circuit.**
- **Editing and Grouping Parts.**
- **Automatic positioning and swapping.**
- **Cross Probing.**

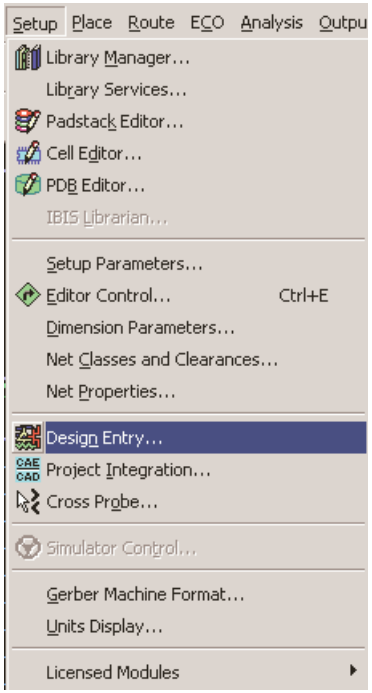
Place from Schematic

- **During Placement in Expedition PCB, you can interactively select parts from Design Capture or Design View.**



Place from Schematic (Cont.)

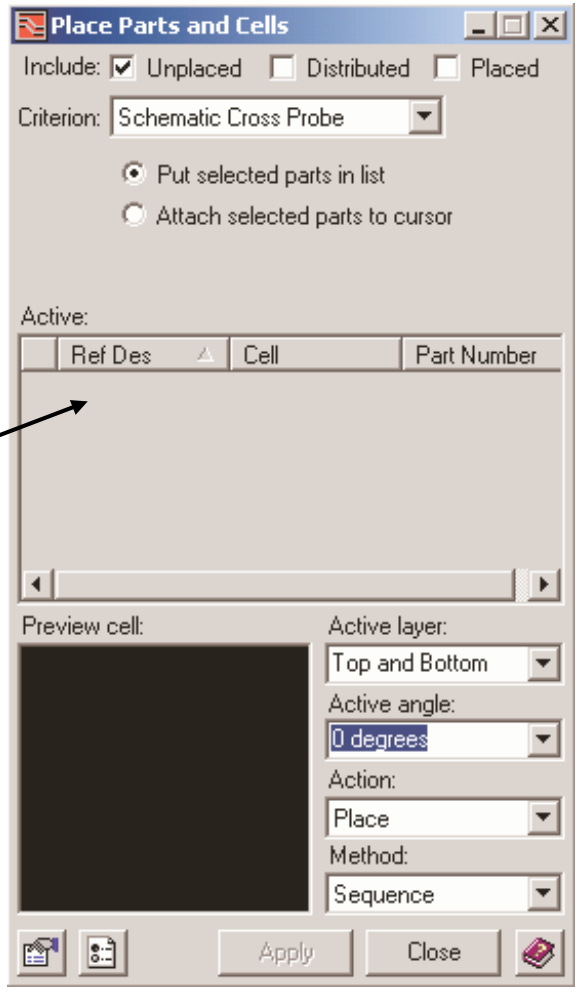
- **Making it work.**
  - **Expedition PCB and Design Capture open.**
    - **Invoke Design Capture from Expedition PCB.**
      - **Opens the correct project.**
      - **Puts Design Capture in Transmit mode.**
  - **Design Capture must be in Transmit Mode** 
    - **Waiting for interaction with another project - Inter-process Communication**
      - **Invoking Design Capture from Expedition PCB automatically invokes Transmit Mode.**
  - **For Hierarchical Designs (Design Capture)**
    - **Use Edit > Set Instance to set the Instance path for the Design Root**



Or 

Place from Schematic (Cont.)

- In Expedition PCB, issue Place > Parts and Cells.
  - Set Criterion to Schematic Cross Probe.
- In Design Capture, select the symbol for the Part to be placed.
  - Action depends on Option in Expedition PCB.
    - Part is placed in the parts list.
    - OR Part is attached immediately to the cursor for placement.

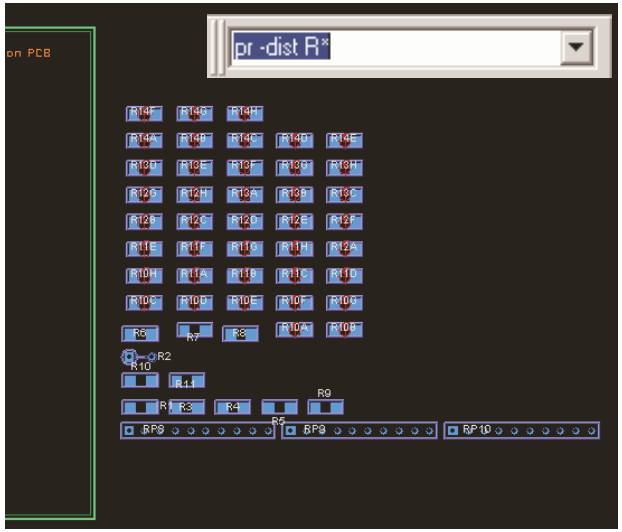


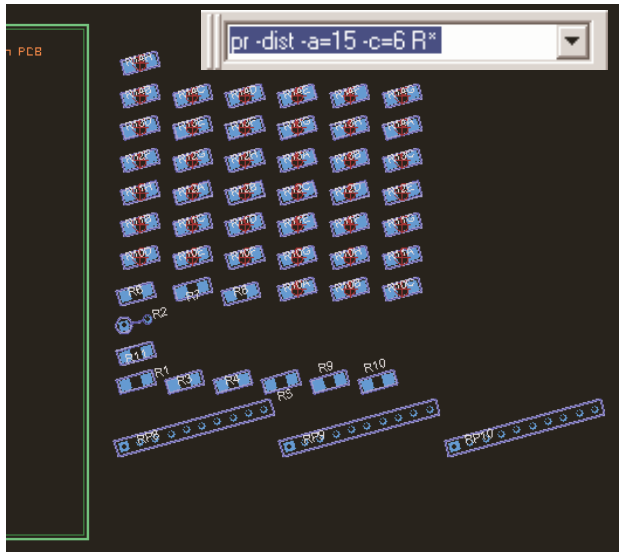
Key-in Placement Commands

- **Place Identified Part**
  - **pr Ref-Des-List**
    - **Attaches the specified Part to the cursor for placement.**
    - **Examples:**
      - **pr U1**
      - **pr U***
- **Place at Coordinate**
  - **pr Coord -angle=a Ref-Des**
    - **Places the part at the specified location**
    - **Examples:**
      - **pr 500,1000 U11**
      - **pr 1225, 790 -a=90 C1**

Key-in Placement Commands (Cont.)

- **Placing Outside the Board Outline**
  - **pr -dist Ref-Des-List**
    - **Places qualified parts in an array to the right of the Board graphics.**
    - **Examples**
      - **pr -dist U1**
      - **pr -dist R***
      - **pr -dist ***
    - **Options**
      - **-cols=n (-c) - number of columns in the array**
        - **pr -dist -c=7 R***
        - **Default is “5”**
      - **-angle=a (-a) - rotate the parts to the specified angle**
        - **pr -dist -a=45 -cols=8 C***





Key-in Placement Commands (Cont.)

- **Placing by ASCII file Input**
  - **pr -file=[filename]**
    - **Places parts based on coordinates and information in an ASCII file.**
    - **Examples**
      - **pr -file=placement.txt**
    - **Options**
      - **-x - creates a file based on current placement**
        - **pr -file=current.txt -x**
    - **Default location for placement file is the “pcb” folder.**
    - **File line format**
      - **.ref RefDes X,Y Rot Side**

```
.units th
!
!.ref RP8 (unplaced)
.ref R13B 1305,2275 90 bottom
.ref R10H 1170,700 90 bottom
.ref C7 3200,2925 90 top
.ref R1 1550,2850 90 top
.ref R10B 1305,700 90 bottom
.ref C15 4200,2925 90 top
.ref C13 3800,2925 90 top
.ref R14B 1305,175 90 bottom
.ref R4 775,1800 90 top
.ref R11F 905,1225 90 bottom
.ref R11B 1305,1225 90 bottom
.ref U11 1105,1250 0 top
.ref C2 4300,2925 90 top
.ref R12B 1305,1750 90 bottom
.ref J1 4500,2750 180 top
.ref U12 1105,1775 0 top
.ref R14H 905,175 90 bottom
.ref C5 3300,2925 90 top
.ref R13C 1405,2450 90 bottom
.ref R13A 1405,2175 90 bottom
.ref R9 3925,175 0 top
.ref R10G 1035,700 90 bottom
.ref R11 3650,175 0 top
.ref R11E 805,1125 90 bottom
.ref C3 3400,2925 90 top
```

Key-in Placement Commands (Cont.)

- **Move by Reference Designator**
  - **mr Ref-Des-List**
    - **Attaches placed parts, one after the other, to the cursor for move.**
    - **Examples**
      - **mr U1**
      - **mr U1 , U16 , C***
- **Move a Distance by Reference Designator**
  - **mr dx=x,y Ref-Des-List**
    - **Move the placed parts in the reference Designator list by the x,y delta.**
    - **Examples**
      - **mr dx=0,100 I***
      - **mr dx=-50 U1 , U16**
        - **Assumes only x direction move**
      - **mr dx=,25 C***
        - **Assumes only y direction move**

Key-in Placement Commands (Cont.)

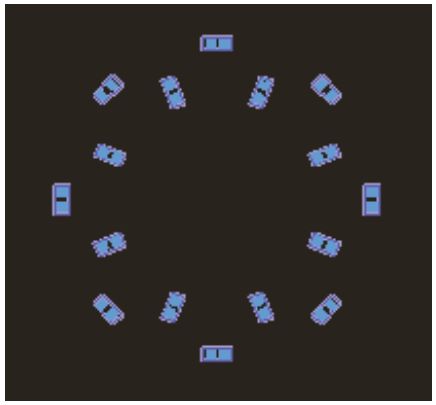
- **Move a Part to an absolute coordinate**
  - **mr x,y Ref-Des**
    - **Moves the specified part to the x,y location.**
    - **Examples**
      - **mr 1200, 2725 U1**
    - **Options**
      - **-a=angle**
        - **mr 1200,2725 -a=90 U1**
- **Move Selected Part to absolute coordinate**
  - **ms x,y**
    - **Move the selected part to the x,y location.**
    - **Only one part can be selected.**
    - **Examples**
      - **ms 1200, 2725**

Key-in Placement Commands (Cont.)

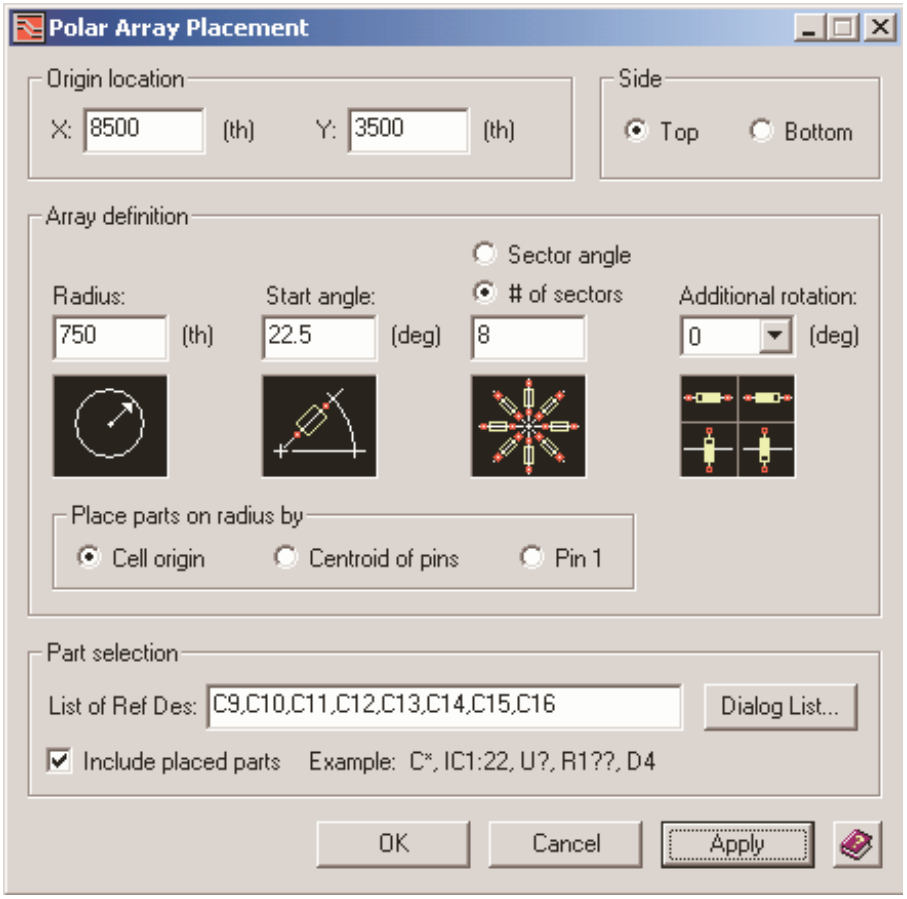
- **Move Selected Parts a delta distance**
  - **ms dx=x,y**
    - **Move the selected Parts by the x,y delta.**
    - **Examples**
      - **ms dx=0,100**
      - **ms dx=-50**
        - **Assumes only x direction move**
      - **ms dx=,25**
        - **Assumes only y direction move**
    - **This command is also active for draw objects.**

Polar Array Placement

- **Placement in a Circular Array.**

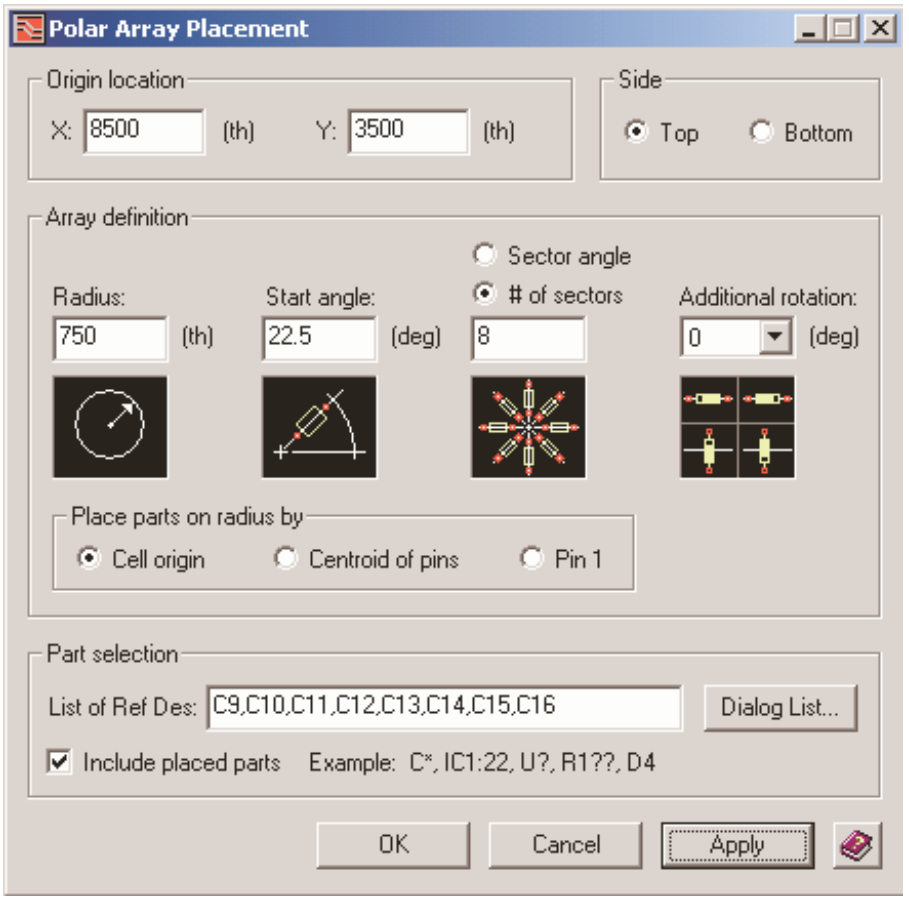


- **Origin Location - the x,y location of the center of the array.**
- **Side - which side of the board to place on.**



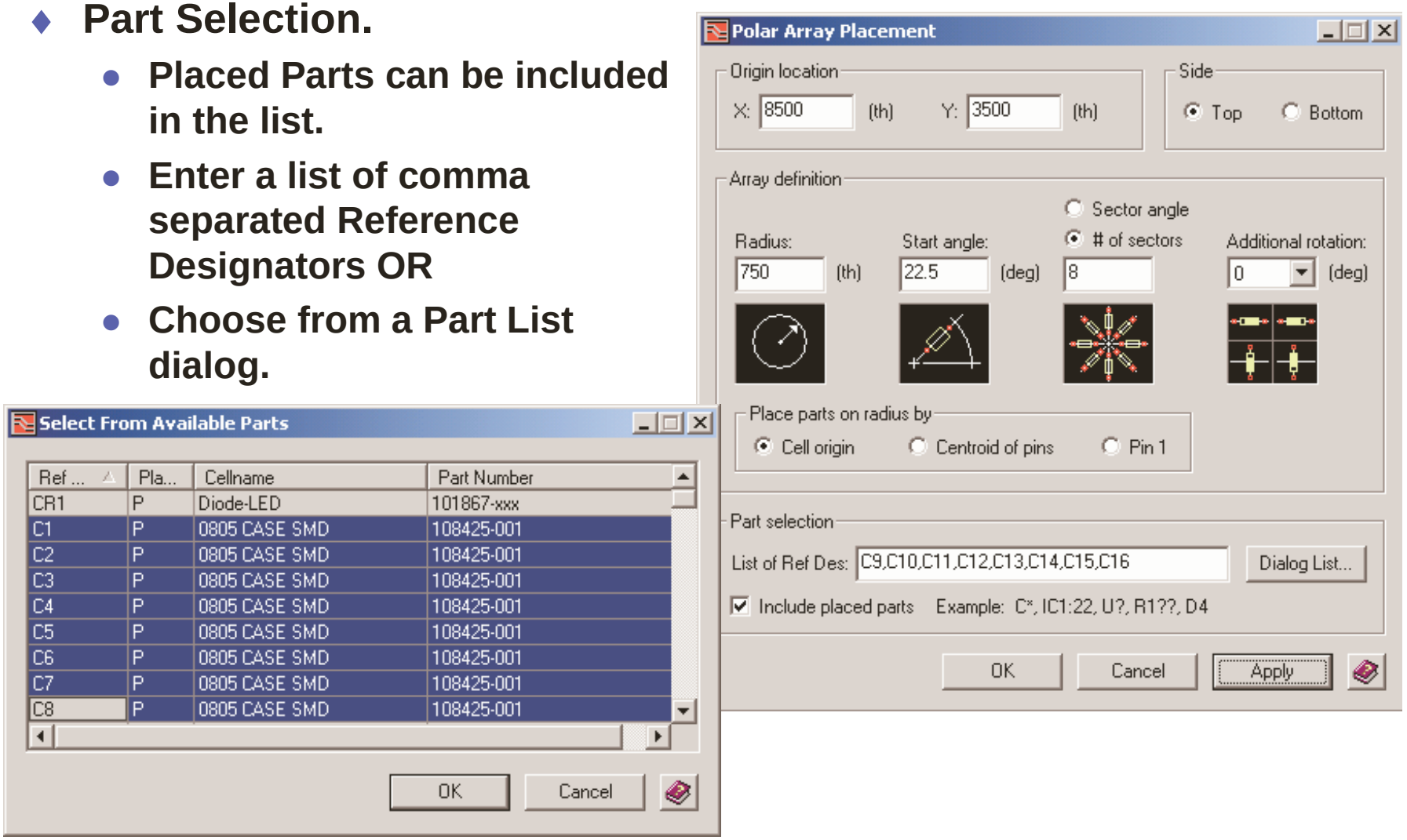
Polar Array Placement (Cont.)

- **Array definition.**
  - **Radius - of the origin circle of the array.**
  - **Start angle - the angle of the first part in the array from the X axis.**
  - **Divisor**
    - **Sector angle - the angle between each element of the array.**
    - **# of Sectors - divide the origin circle into that many parts.**
  - **Additional rotation - rotate the part before placing.**
  - **Placed on radius - what point on the part is placed on the origin circle of the array.**



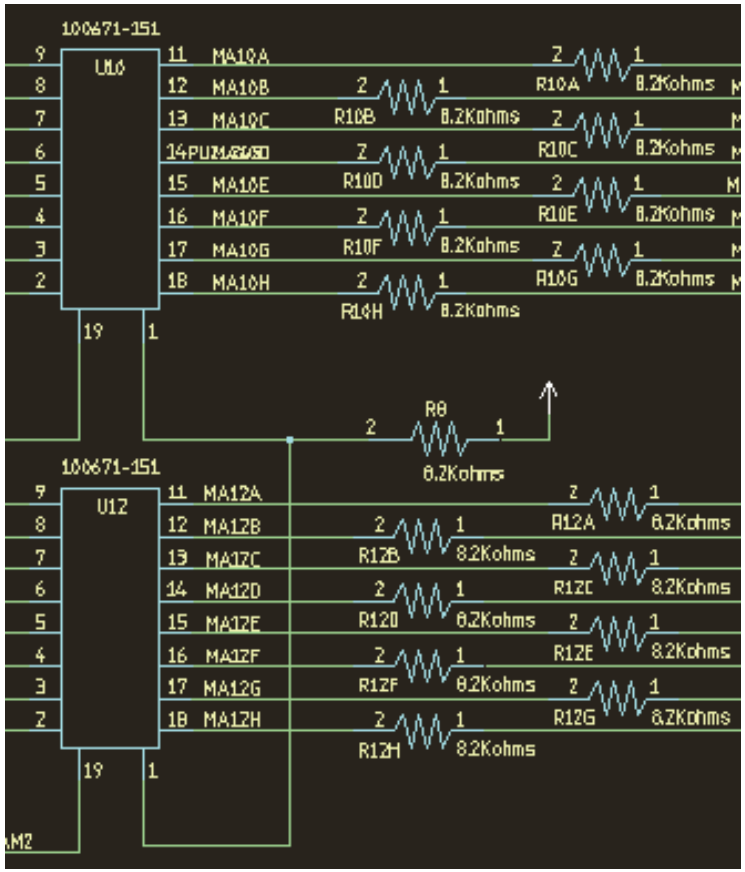
Polar Array Placement (Cont.)

- **Part Selection.**
  - **Placed Parts can be included in the list.**
  - **Enter a list of comma separated Reference Designators OR**
  - **Choose from a Part List dialog.**



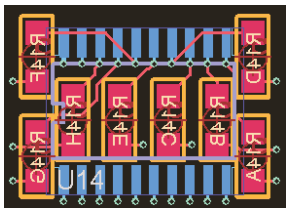
Copy Circuit

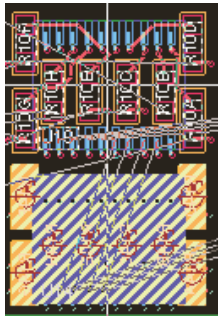
- **Replicates like circuits.**
  - **Schematic Setup**
    - **Parts in like circuits must have:**
      - **The same Part Numbers**
      - **The same Cell names**
      - **The same connectivity, if traces are to be included in the circuit copies**
    - **Expedition PCB evaluates the design to find like circuits to use in the process**

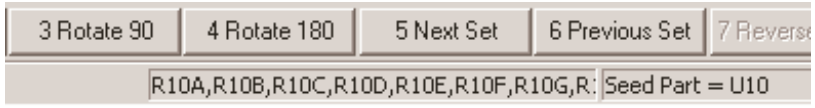


Copy Circuit (Cont.)

- **Replicates like circuits.**
  - **PCB Implementation**
    - **Place one of the circuits in Expedition PCB. Route the nets in the circuit if the connections are identical.**
    - **Enter Place > Copy Circuit mode.**
    - **Select the pre-placed circuit.**
    - **Press the Copy action key.** 2 Copy
    - **A copy of the circuit is attached to the cursor. Position the copy, then click to place.**
    - **If another copy of the circuit is available, it will attach to the cursor to be placed.**
      - **Auto Finish** 9 Auto Finish **will place any other copies with vector placement the same as the first copy placement - same direction - same distance.**
    - **Take Expedition PCB out of Copy Circuit mode.**

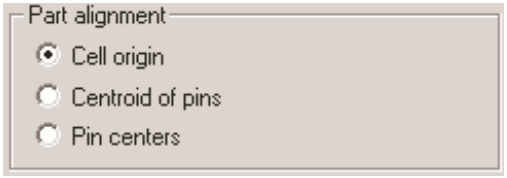






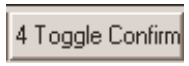
Grouping and Aligning Parts

- **Group**
  - Select parts to group.
  - Issue Place > Group
    - Select any part in a group and all parts select.
    - Editing, including rotates act on the whole group.
- **Ungroup**
  - Select any part in the group.
  - Issue Place > Ungroup
- **Align**
  - Select parts to align.
  - Issue the appropriate Align command.
  - Alignment point is set in Editor Control > Part tab.

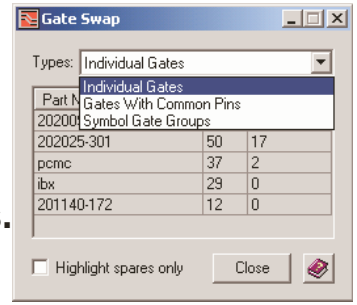


Swapping

- **Swap**
  - **Place > Swap Parts - select first part, select second part, click to confirm.**
  - **Route > Swap > Gates - select pin in the first gate, select equivalent pin in the second gate, click to confirm.** 

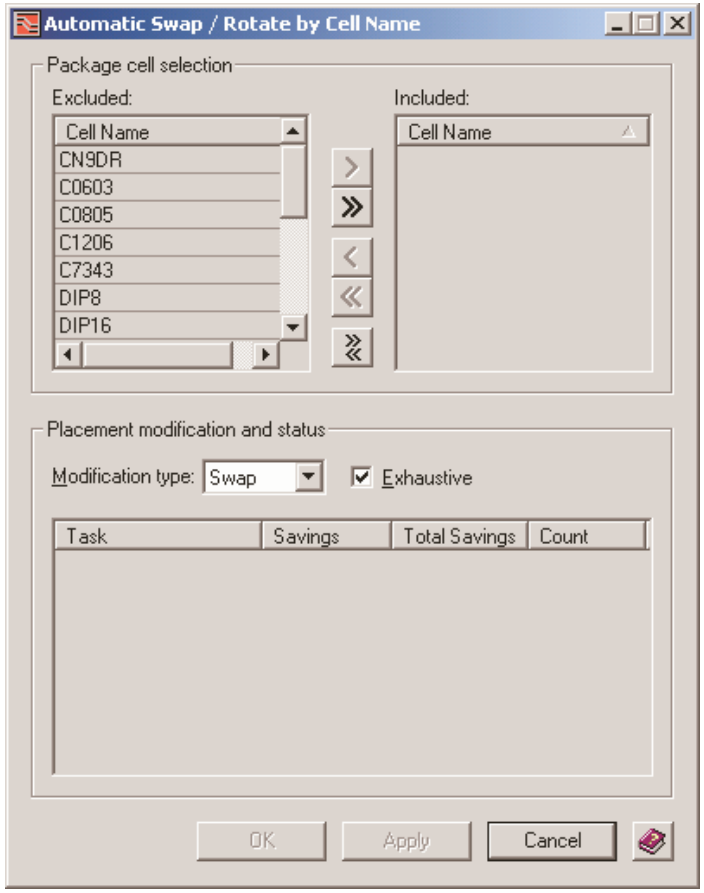
    - **Swap Dialog**
      - **Individual Gates - default - swap with any like gate.**
      - **Common Pins - gates that have common pins swap.**
      - **Symbol Gate Groups - no swapping with unfilled gates.**
      - **Select a gate from the dialog to display equivalent gates.**
    - **Toggle Confirm** 

- eliminates the confirming click.
  - **Route > Swap > Pins - select first pin, select equivalent pin, click to confirm.**
- **Swapping gates or pins requires Back Annotation.**



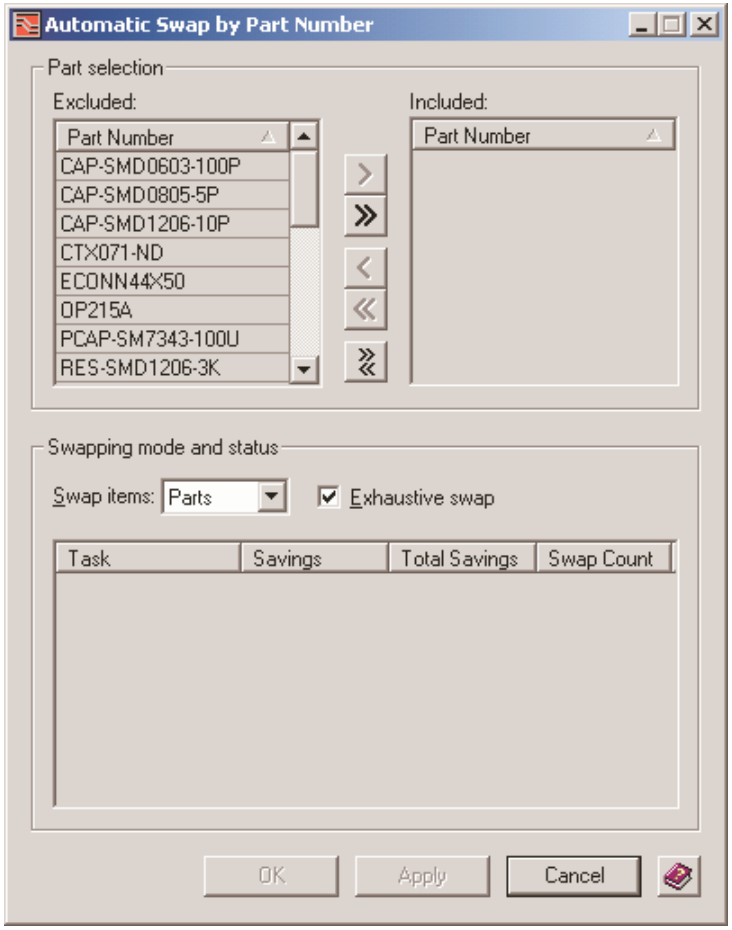
Auto Swap by Cell Name

- **Place > Automatic > Swap/Rotate by Cell Name**
  - **Move cell types to include in the operation to the Include table.**
  - **Set Modification type**
    - **Swap - only swaps like cell names.**
    - **Rotate - rotates square outlines 90 degrees, rotates other cells 180 degrees.**
    - **Flip - rotates all cells 180 degrees.**
  - **Operation statistics shown in the task table after each Apply.**



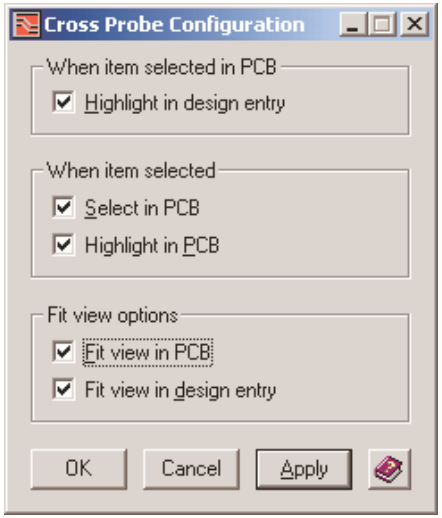
Auto Swap by Part Number

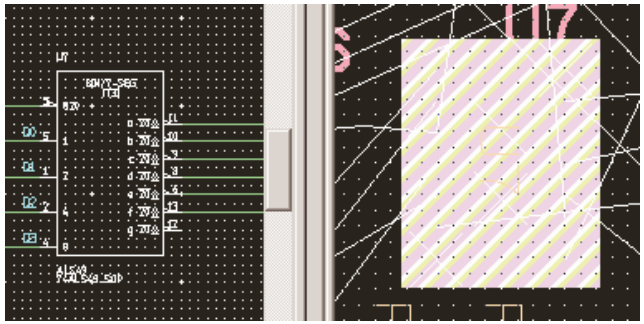
- **Place > Automatic > Swap by Part Number**
  - **Move Part Numbers to include in the operation to the Include table.**
  - **Set Swap type**
    - **Part - swaps Parts.**
    - **Gates - swaps Gates as defined in the PDB.**
    - **Pins - swaps equivalent Pins as defined in the PDB.**
  - **Operation statistics shown in the task table after each Apply.**



Schematic and Expedition PCB Cross Probing

- **Setup - Cross Probe**
  - **Settings determine - when you do something in one application - what happens in the other application.**
  - **Apply or OK will automatically invoke Design Capture if it is not active. It will open in Transmit mode.**





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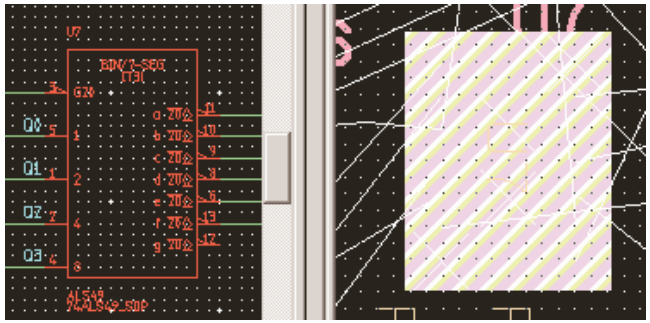

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Lab Preview

- **This Exercise has 2 Labs.**
  - **Lab 1 — Place by Schematic and Key-ins**
    - Partially place the “control1_reva” database by using Schematic Cross Probe and placement Key-in commands.
  - **Lab 2 — Other Placement Aids**
    - Database “control1_reva” - Use Polar Placement, Copy Circuit and other Placement utilities.

Advanced Expedition PCB

Module 3

IDF Interface

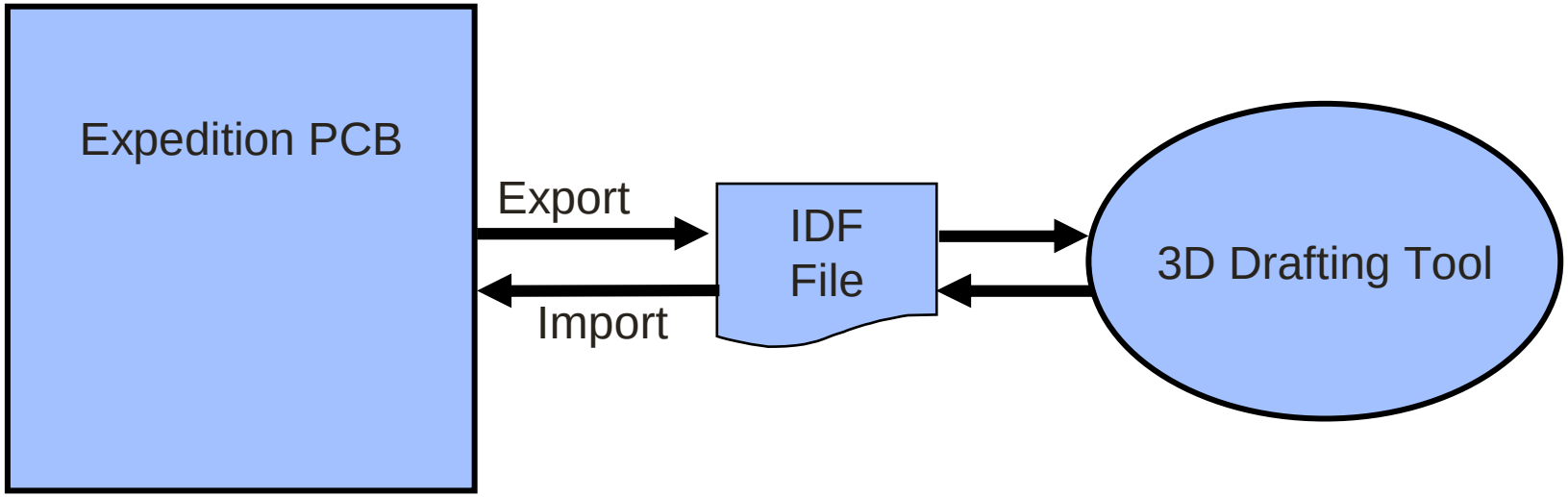
Objectives

Upon completion of this lesson and lab, you will be able to:

- **Understand the usage of IDF formatted files with Expedition PCB**
- **Output IDF files from Expedition PCB**
- **Input IDF files into Expedition PCB**

The IDF Workflow

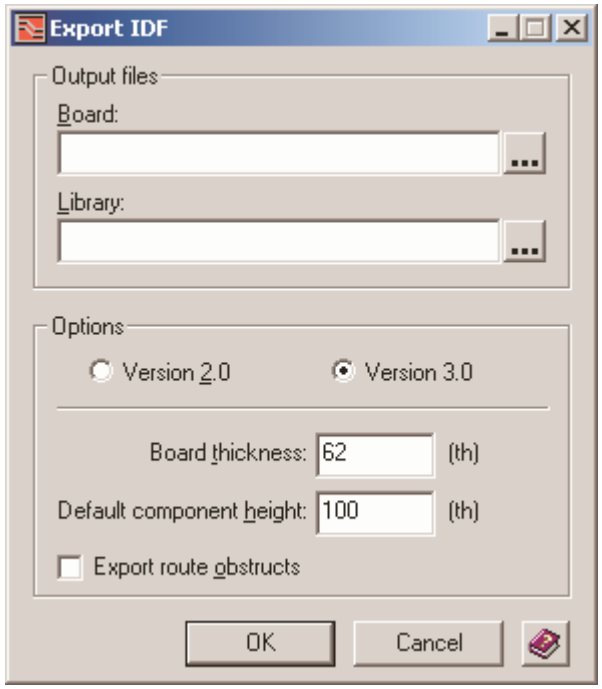
- **IDF allows a two way transfer of data from Expedition PCB to a 3D mechanical package.**



- **IDF Extracts the following information from Expedition PCB**
  - **Parts Board Outline Contours Mounting Holes Route Border Placement Obstructs Floorplan Rooms**
    - **The transfer does not include Netlines, Traces or Vias**
    - **Test Points are only transferred if they are defined as Parts on the schematic and placed as components on the board.**

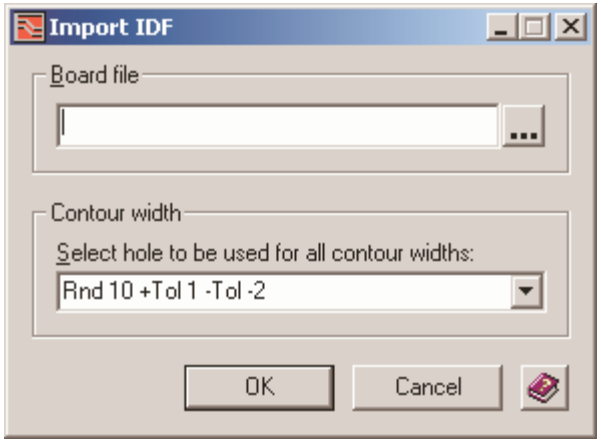
IDF Export

- File > Export > IDF
  - Supply the name of the desired Board and Library Files.
    - Board file contains board definition plus X,Y location of parts - extension ".emn"
    - Library file contains part geometry data - extension ".emp"
  - Choose the IDF version to produce
  - Supply the thickness of the board for 3D modeling
  - Supply a default component height for parts which do not have a height specified in the PDB or the Cell.
  - If you want route obstructs exported, check to include.
- The default location for the files is the "output" sub-directory of the database.



IDF Import

- File > Import > IDF
  - Specify the name of the board file (.emn) to import.
    - The Library file is not necessary - Expedition PCB already has local library data.
  - Chose a hole definition to be used for all imported contours.



- Imported changes are made directly to the data.
  - Parts can be moved
  - Board can be edited
  - Mounting holes, obstructs and contours can be placed

IDF Import Issues

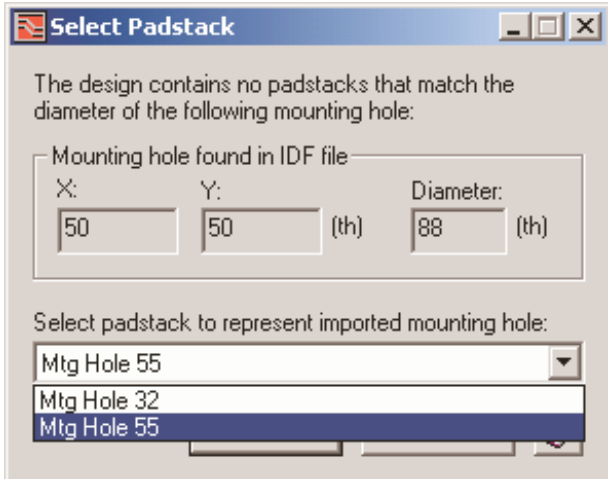
- **IDF to Expedition PCB layer interface:**
  - **Layer mapping between IDF files and Expedition PCB is:**

IDF Name	Expedition PCB Name
Component Placement*	Parts*
Board outline	Board outline
Board outline (cutout option)	Contours
Drilled Holes	Mounting holes
Route outline	Route border
Route keepout	Route obstruct
Via keepout	Via obstruct
Place keepout	Placement obstructs
Place region	Floorplan rooms

IDF Import Issues (Cont.)

- **Line items are imported into Expedition PCB with 0 width. If a larger width is required, it must be re-set in Expedition PCB.**

- **When importing mounting holes, a padstack containing a hole size and plating setting that matches the IDF mounting hole size is automatically selected.**
  - **If no matching hole size is found, you are asked to select a padstack that contains a hole size smaller than the hole size found in the IDF file.**



Lab Preview

- **This Exercise has 2 Labs.**
  - **Lab 1 — IDF Import**
    - Database “control2_reva” - Import an IDF file for placement, provided by your friendly mechanical staff.
  - **Lab 2 — IDF Export**
    - Database “control2_reva” - Export an IDF file, edit the file, then re-Import the file.

Advanced Expedition PCB

Module 4

Reusable Blocks

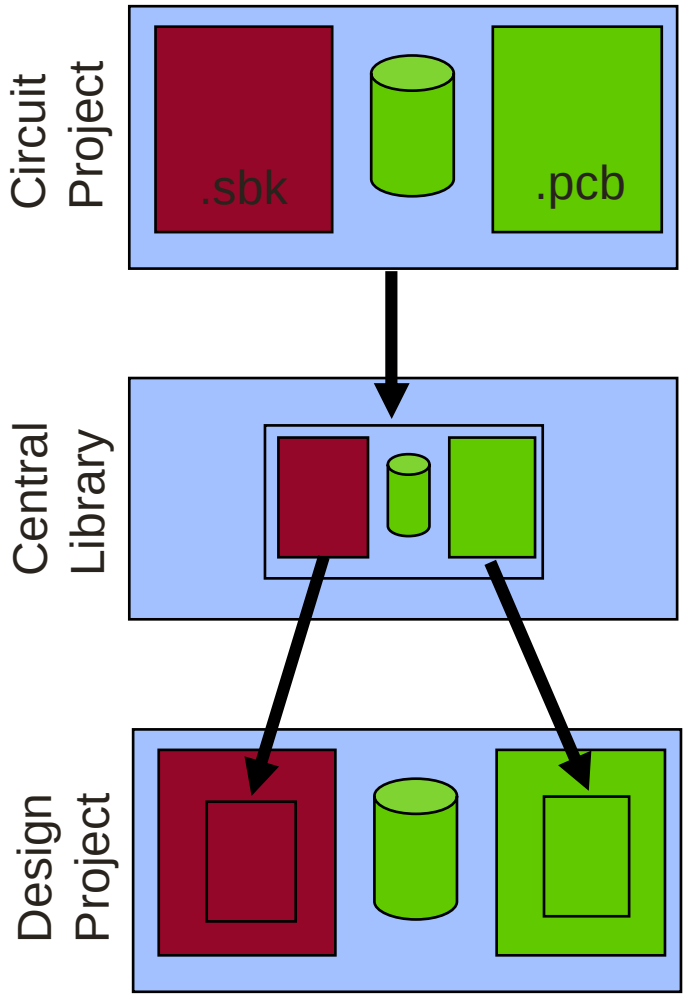
Objectives

Upon completion of this lesson and lab, you will be able to:

- **Understand how Block Reuse works in the Expedition PCB Environment.**
- **Create Schematic Reusable Block data.**
- **Create Reusable Block information in Expedition PCB.**
- **Store Reusable Block data in a Central Library.**
- **Use Reusable Blocks in Design Capture.**
- **Use Reusable Blocks in Expedition PCB.**
- **Explode Reusable Blocks in Expedition PCB for Editing.**
- **Change Reusable Blocks in the Central Library.**

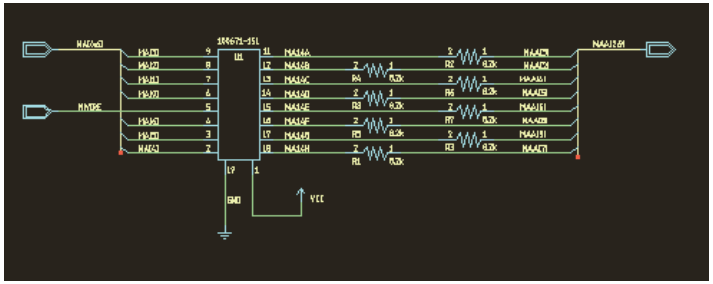
Reusable Block Overview

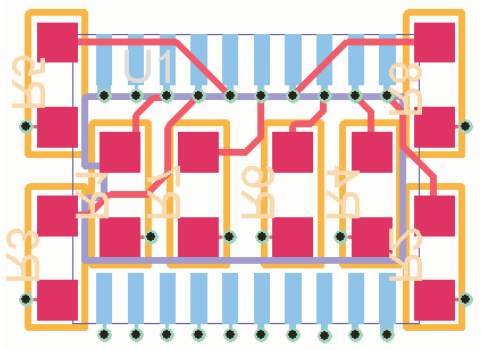
- A Project is created for the Reusable Block
  - Schematic defined
  - Compiled
  - Forward Annotated and Laid Out
- That Project is imported into the Central Library as a Reusable Block
- In the Design Project
  - The schematic portion of the Reusable Block is placed as a Hierarchical Block
  - The design is compiled and Forward Annotated into Expedition PCB
  - The layout portion of the Reusable Block is placed on the printed circuit board



Step 1: Defining the Reusable Block Project

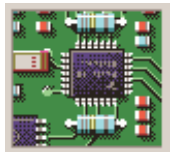
- **Just like any other project:**
  - **Start Project**
    - **Assign Central Library**
    - **Assign Search order**
  - **Draw Schematic**
    - **Hierarchical Connections to “outside”**
      - **Hierarchical Connectors**
      - **Hierarchical Pin Name properties**
  - **Compile and Package**
  - **Forward Annotate to Expedition PCB**
    - **Setup Parameters**
    - **Set Net Classes**
    - **Set Net Properties**
  - **Place and Route, Edit, etc.**

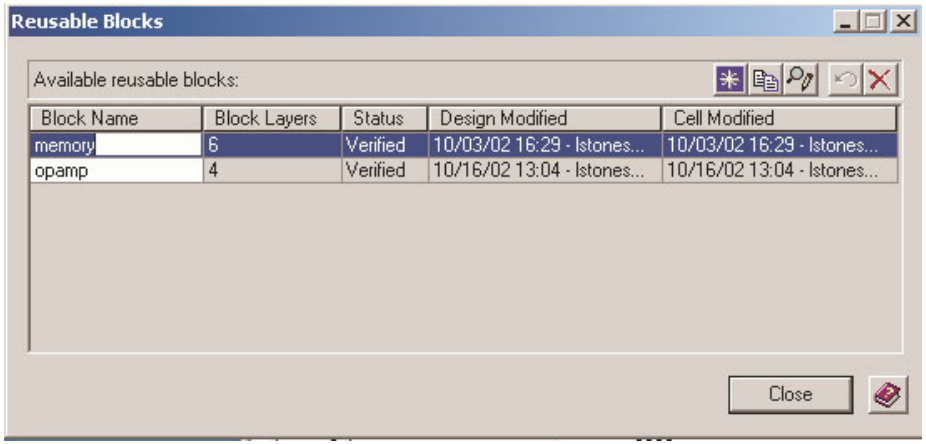




Step 2: Instantiation in the Central Library

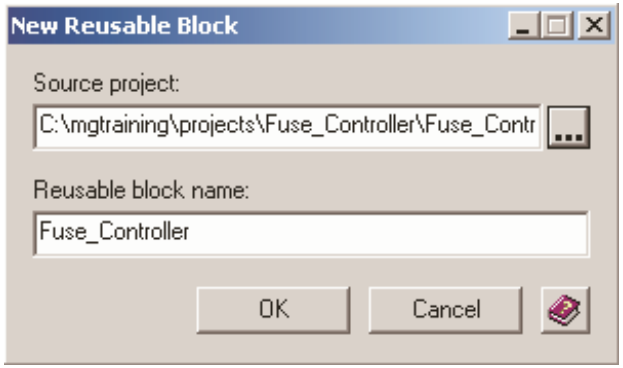
- **Invoke Library Manager**
  - **Stand Alone or From Expedition PCB**
- **Click on the Reusable Blocks Icon**
- **Use the dialog to review current Reusable Blocks**
  - **Copy a Reusable Block using the Copy Icon.**
  - **Delete a Reusable Block using the Delete Icon.**





Step 2: Instantiation in the Central Library (Cont.)

- **Starting a new Reusable Block**
  - **Click on the New icon.**
  - **On the dialog**
    - **Browse to find the Project file.**
    - **Enter a Reusable Block name**
  - **The Reusable Block is added to the list.**

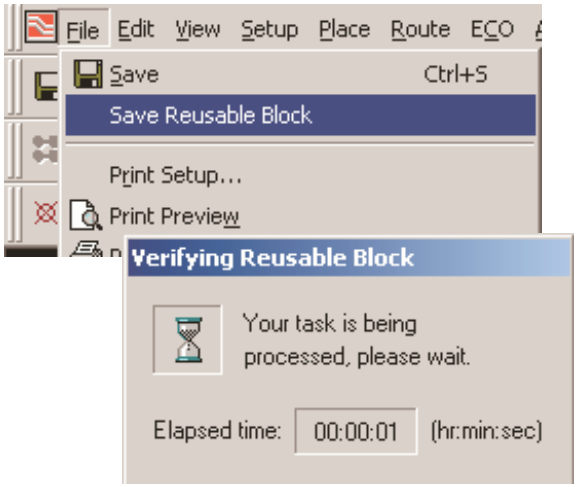


Block Name	Block Layers	Status	Design Modified	Cell Modified
memory	6	Verified	10/03/02 16:29 - lstones...	10/03/02 16:29 - lstones...
opamp	4	Verified	10/16/02 13:04 - lstones...	10/16/02 13:04 - lstones...
Fuse_Controller	4	Unverified	10/16/02 13:23 - lstones...	Unmodified

  - **It will be marked as "Unverified" and "Unmodified"**

Step 2: Instantiation in the Central Library (Cont.)

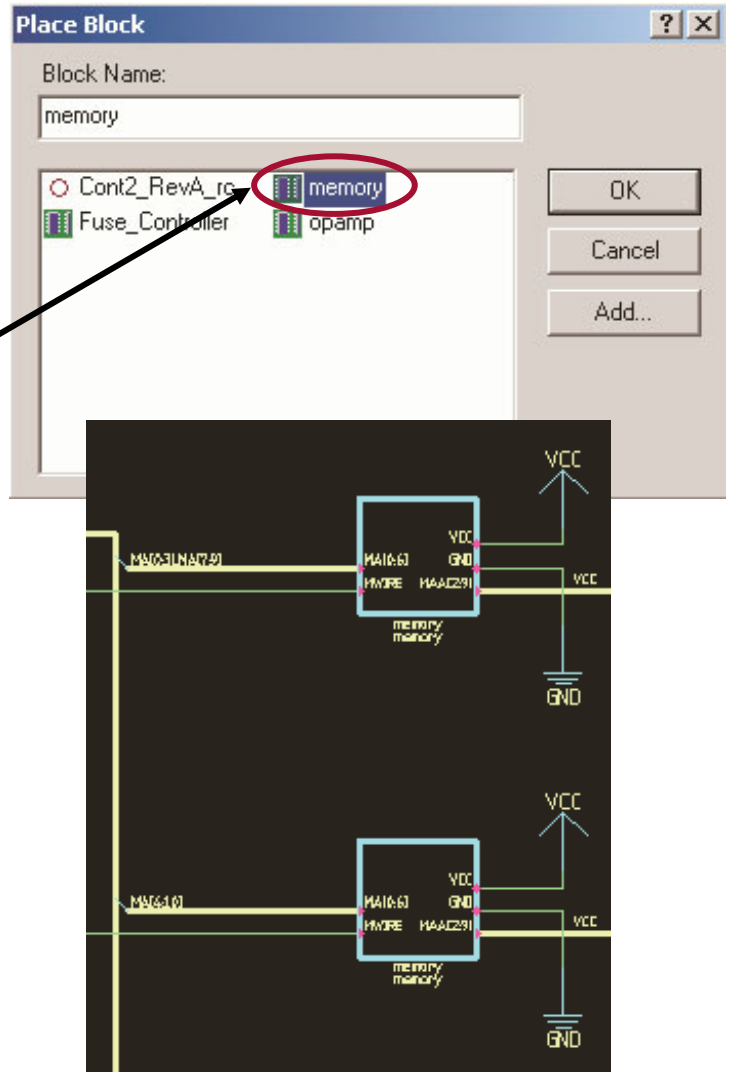
- **Verifying a Reusable Block**
  - **Click on the Edit icon.**
    - **Opens the Reusable Block in Expedition PCB-Reusable Block mode.**
    - **Prompted to Forward Annotate changes - do it.**
    - **Check the layout to make sure it is what you really want.**
  - **Issue File >Save Reusable Block**
    - **This will Verify and save the Reusable Block**



Block Name	Block Layers	Status	Design Modified	Cell Modified
Fuse_Controller	4	Verified	10/16/02 13:36 - lstones...	10/16/02 13:37 - lstones...
memory	6	Verified	10/03/02 16:29 - lstones...	10/03/02 16:29 - lstones...
opamp	4	Verified	10/16/02 13:04 - lstones...	10/16/02 13:04 - lstones...

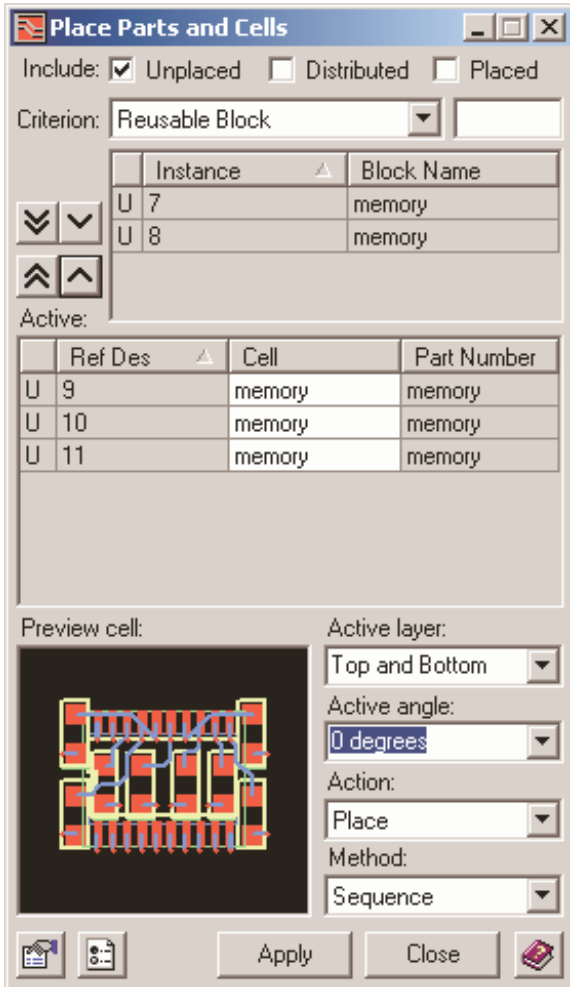
Step 3: Using the Reusable Block in Design Schematics

- **Just like any other project:**
  - **Start Project**
    - **Assign Central Library**
    - **Assign Search order**
- **To place a Reusable Block, use the Place > Block command.**
  - **Reusable Blocks appear on the dialog with a Reuse Block symbol**
  - **An Auto-generated block is provided for the schematic. Place it as many times as needed for the design.**
- **Save, Compile and Package**
  - **Reusable Block Reference Designators prepend the block instance number.**



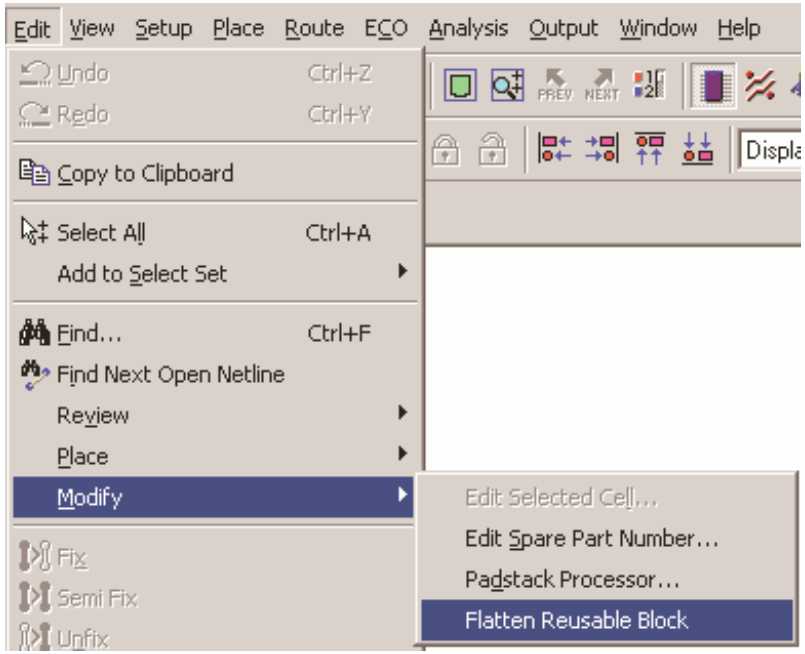
Step 4: Reusable Blocks in Expedition PCB

- **Forward Annotate design to Expedition PCB**
  - **Search Path considerations**
- **Place the Reusable Block**
  - **Place > Place Parts and Cells**
    - **Criterion - Reusable Blocks**
    - **Move Reusable Blocks to active list**
    - **Place as if it were a regular part**
      - **Trace Considerations**
      - **Layer Considerations**
      - **Net Class Considerations**
      - **Net Properties Considerations**
      - **Via Span Considerations**



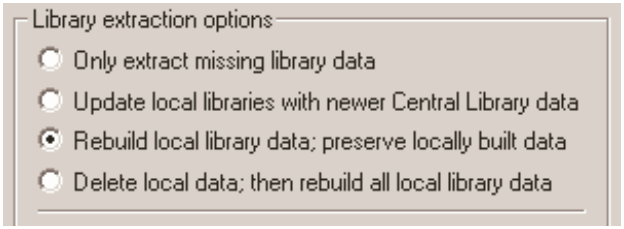
Step 4: Reusable Blocks in Expedition PCB (Cont.)

- **Flattening Reusable Blocks**
  - Select the block, then issue the Edit > Modify > Flatten Reusable Block command.
  - What you get:
    - Allows changes to Reference Designators
    - Allows changes to placement
    - Allows changes to routing
  - What you lose:
    - Ability to manipulate as a block
    - Ability to update as a block with library changes
  - No - once a block is flattened, it can not be re-composed as a block



Reusable Block Modifications

- **To change the layout portion of a Reusable Block:**
  - **Library Manager**
    - **Reusable Blocks**
      - **Select the Reusable Block then go into edit mode**
      - **Make the changes to the Reusable Block circuit**
      - **Save the Reusable Block**
  - **Expedition PCB**
    - **Setup > Project Integration**
    - **Choose an option to update the library data**
    - **Forward Annotate**

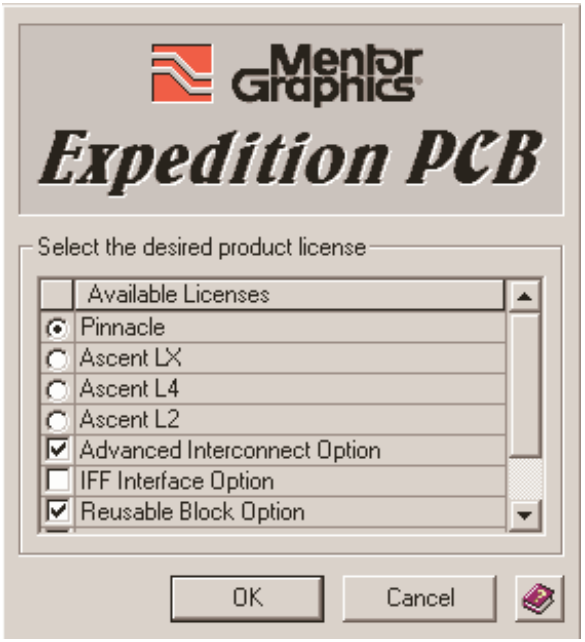


Reusable Block Modifications (Cont.)

- **To change the schematic portion of a Reuse Block:**
  - **Copy the original Reusable Block**
  - **Edit the block in PCB, then enter Design Entry from PCB**
    - **Make the changes**
    - **Save, Compile, Package**
  - **In PCB, make changes necessary from the schematic changes**
    - **Save and verify**
  - **In Design schematic, delete and change the block representing the Reusable Block to the newly modified block.**
    - **Save and verify**
  - **In Expedition PCB**
    - **Forward annotate**
    - **Place new version of the reusable block.**

Licenses Considerations

- **Reusable Blocks is a licensable application.**
- **You need a license to work in Expedition PCB in a design that has Reusable Blocks.**
  - **If you attempt to open a design that has Reusable Blocks, and you didn't check the license, Expedition will obtain an available license.**
  - **If no license is available, you will not be able to open a database that has reusable blocks.**
  - **If Reusable Blocks are "flattened", the license is not necessary.**



Lab Preview

- **This Module has 3 Labs.**
  - **Lab 1 — Creating a Reusable Block**
    - A Reusable Block project is supplied for you. You will examine the project, then import it as a Reusable Block into the Central Library.
  - **Lab 2 — Using Reusable Blocks**
    - You will use the reusable block you just created in the “control2_reva” project schematics. You will then Open the PCB design, Forward Annotate and place the Reusable Blocks on your design.
  - **Lab 3 — Reusable Block Modifications**
    - You will change the Reusable Block layout in the Central Library and then update the block on the board design. You will also flatten a block.

Advanced Expedition PCB

Module 5

Net Classes and Rule Areas

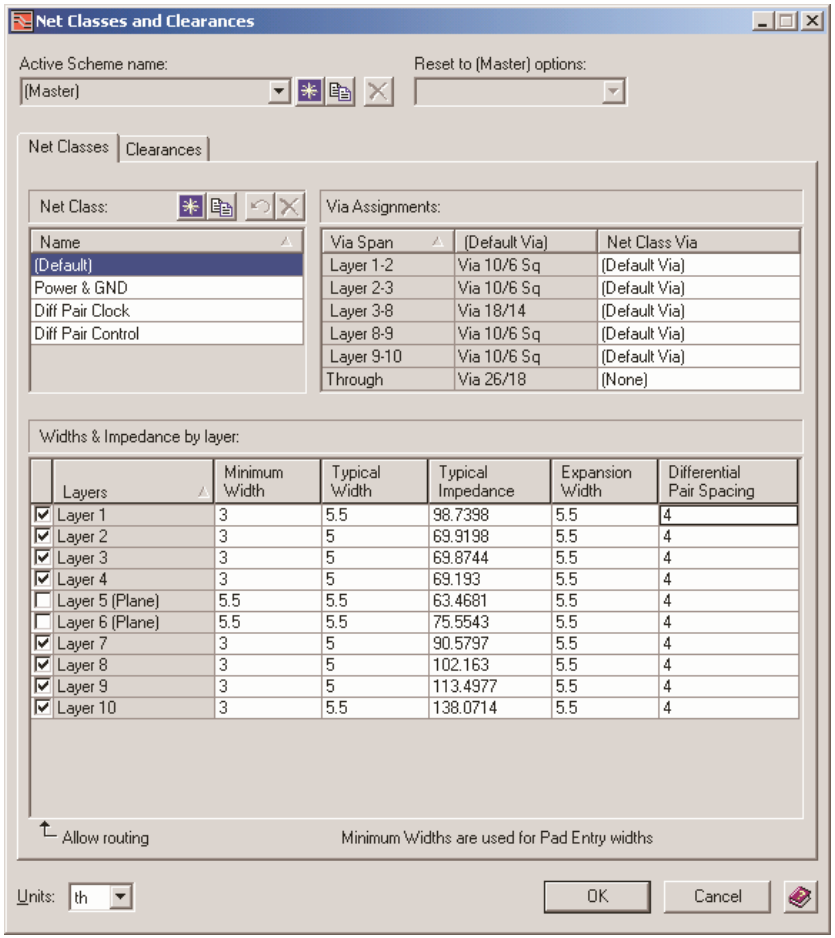
Objectives

Upon completion of this lesson and lab, you will be able to:

- **Create and set Net Classes.**
- **Calculating Typical Impedance.**
- **Create and set Clearance Rules.**
- **Create Net Class Schemes.**
- **Create Rule Areas.**
- **Use Rule Areas to solve routing problems.**
- **Check Net Class and Proximity Hazards.**

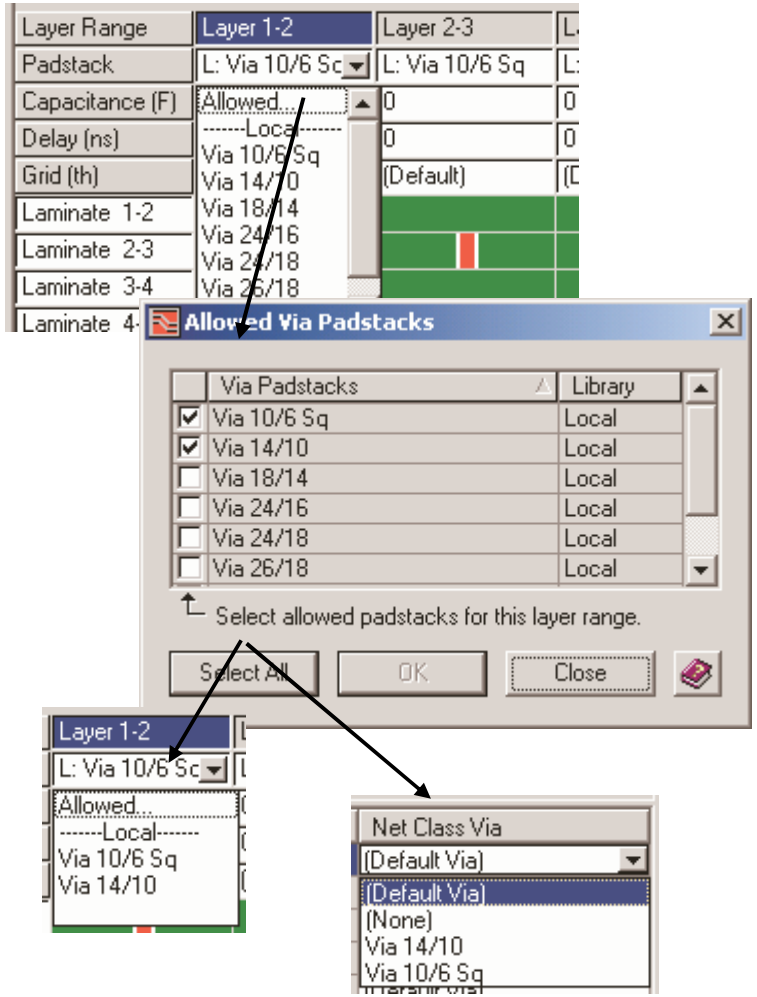
Net Classes

- **Set Properties for Classes of Nets.**
  - **New Net Class - click the New icon then change the name.**
  - **Via Usage for each Net Class be set to differ from the default.**
  - **For each Net Class set layer restrictions.**
  - **For each Net Class set Minimum, Typical and Expansion width on a per layer basis.**
    - **Setting Typical Width will calculate the Typical Impedance.**
    - **Setting Typical Impedance will calculate the Typical Width.**
  - **For each Net Class set the Differential Pair Spacing.**



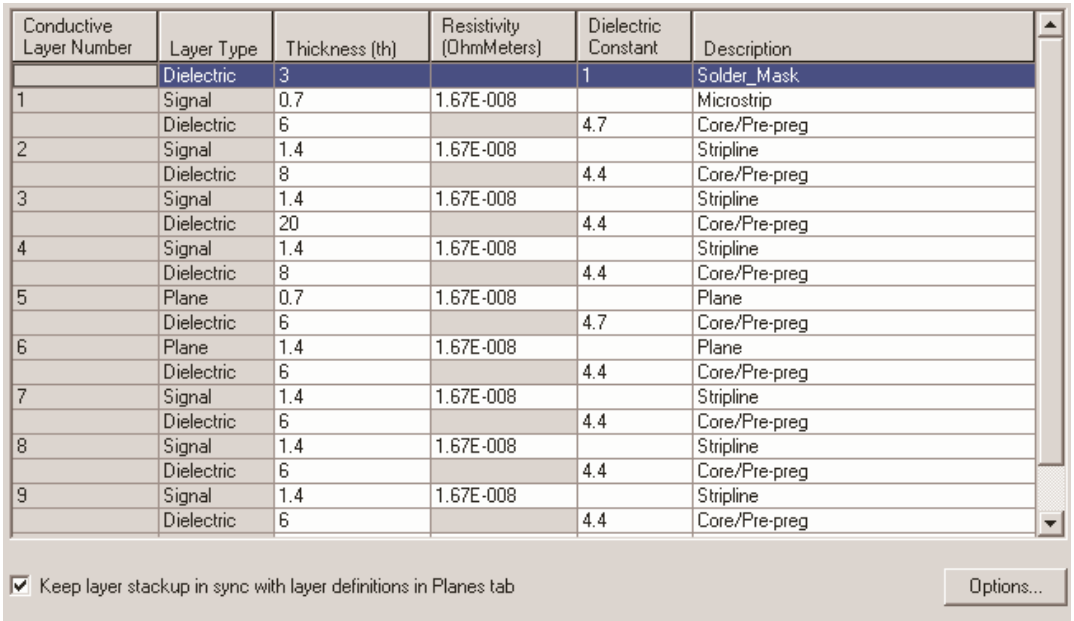
Setup Parameters — Allowed Vias

- **Setup > Setup Parameters**
  - **Vias**
    - **For each Via span, the menu has an Allowed entry which displays a dialog.**
    - **Select which Local vias are allowed for that span.**
    - **The selection on Setup Parameters and Net Classes is then limited to the allowed via padstacks.**



Setup Parameters — Layer Stackup

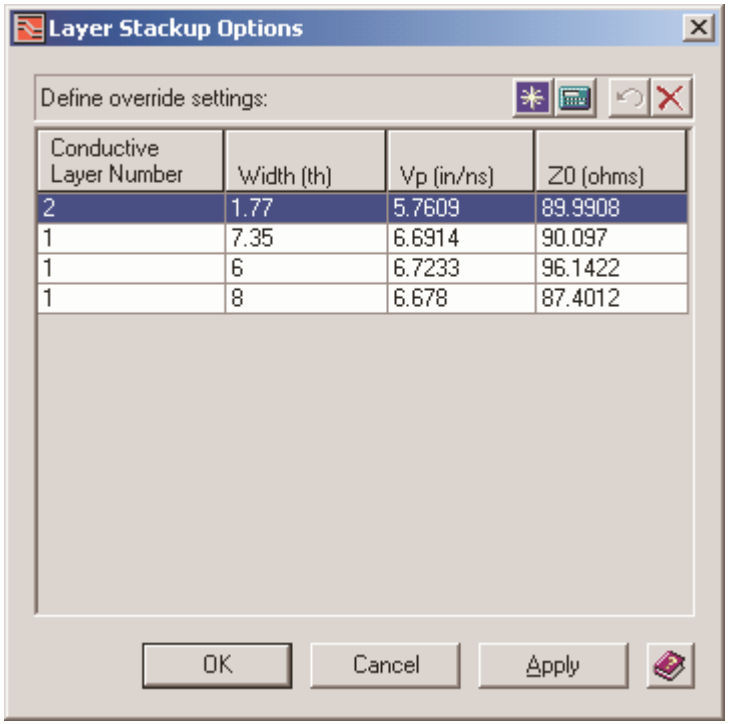
- **Setup > Setup Parameters**
  - **Layer Stackup**
    - **Layer Type, Thickness, Resistivity and Dielectric Constant must be accurate for the 2D field solver to give good results when figuring Characteristic Impedance and Velocity of Propagation.**
    - **Characteristic Impedance and Velocity of Propagation are used in Signal Integrity checking of delays.**
  - **Keep Stackup in Sync**
    - **If checked, then plane and signal layers match the Setup Parameter definition**
    - **If not checked, plane and signal layers can be defined on the dialog to enable "what if" calculations.**



Conductive Layer Number	Layer Type	Thickness (th)	Resistivity (OhmMeters)	Dielectric Constant	Description
	Dielectric	3		1	Solder_Mask
1	Signal	0.7	1.67E-008		Microstrip
	Dielectric	6		4.7	Core/Pre-preg
2	Signal	1.4	1.67E-008		Stripline
	Dielectric	8		4.4	Core/Pre-preg
3	Signal	1.4	1.67E-008		Stripline
	Dielectric	20		4.4	Core/Pre-preg
4	Signal	1.4	1.67E-008		Stripline
	Dielectric	8		4.4	Core/Pre-preg
5	Plane	0.7	1.67E-008		Plane
	Dielectric	6		4.7	Core/Pre-preg
6	Plane	1.4	1.67E-008		Plane
	Dielectric	6		4.4	Core/Pre-preg
7	Signal	1.4	1.67E-008		Stripline
	Dielectric	6		4.4	Core/Pre-preg
8	Signal	1.4	1.67E-008		Stripline
	Dielectric	6		4.4	Core/Pre-preg
9	Signal	1.4	1.67E-008		Stripline
	Dielectric	6		4.4	Core/Pre-preg

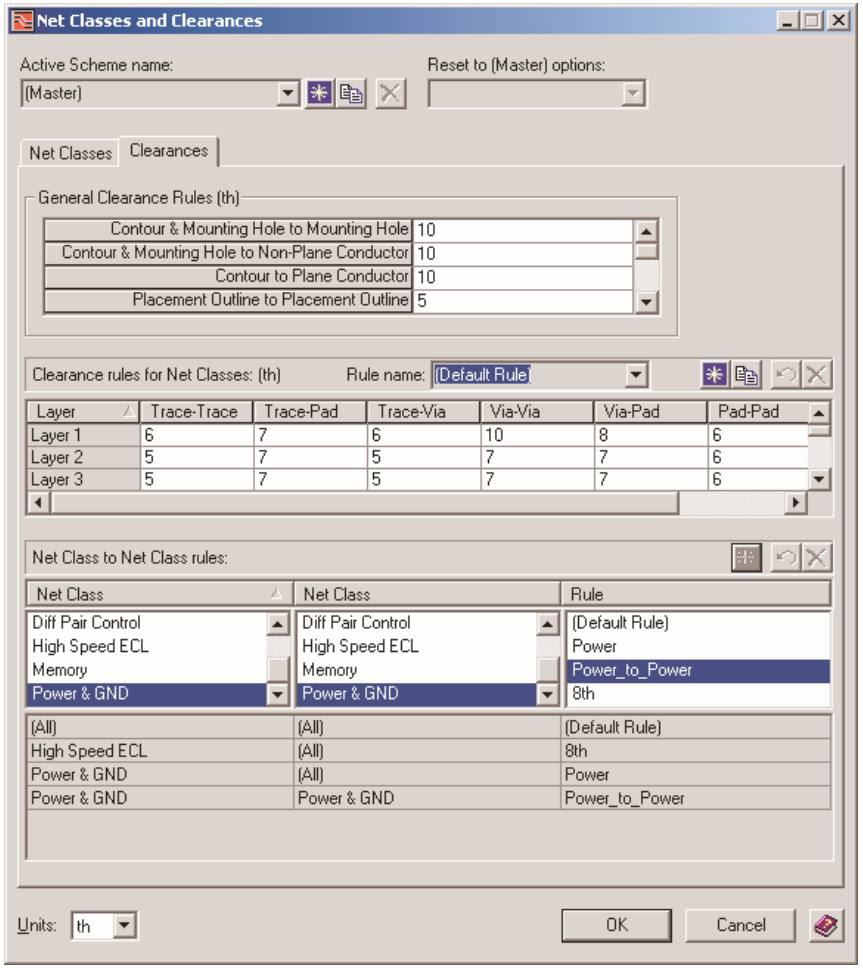
Setup Parameters — Layer Stackup Options

- **Setup > Setup Parameters**
  - **Options Button** Options... **has two functions.**
    - **Calculator**
      - **Select Layer - Enter Trace width - Calculates Characteristic Impedance (Z0) and Velocity of Propagation.**
      - **Select Layer - Enter desired Z0 - Calculates Trace Width.**
    - **Field Solver Override**
      - **Any value left in the Layer Stackup Options dialog will be used for all delay calculations, rather than the values derived from the 2D Field Solver.**



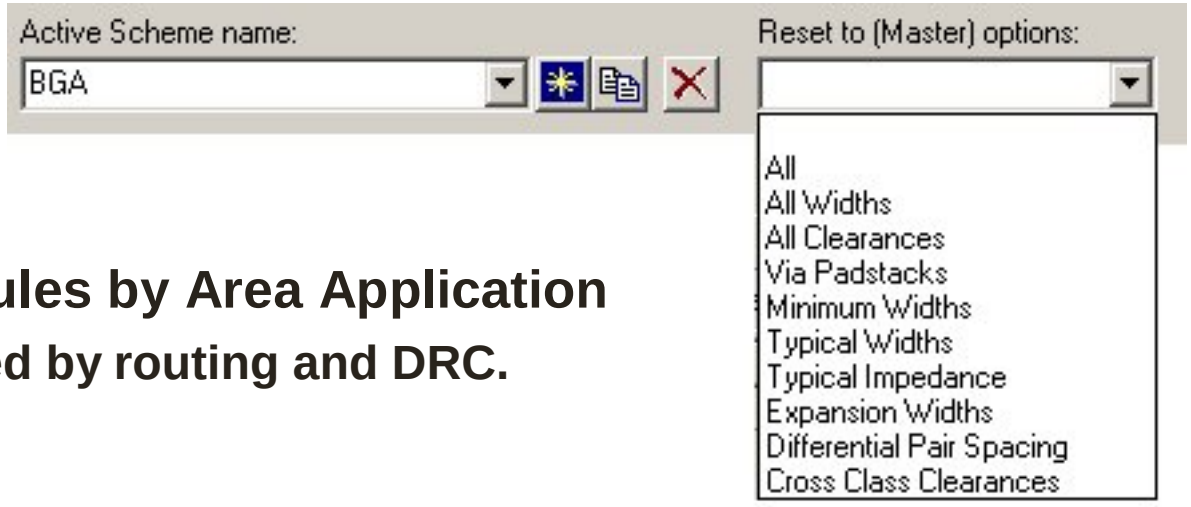
Clearances

- **Clearances Rules.**
  - **General Clearances**
    - **Clearances between objects to be checked by DRC.**
  - **Creating and Setting New Rules for Net Classes - Copper to Copper Clearances**
    - **Click the New icon.**
    - **Enter a Rule name.**
    - **Change any needed values on a per layer basis.**
  - **Net Class to Net Class Rules**
    - **Setup Net Classes and Rule Name first.**
    - **Select one from each column - between this Net Class and this Net Class use this rule.**
    - **Click the New icon.**



Net Class Schemes

- **How it works.**
  - **Set up the Master Scheme.**
    - **Net Classes and Clearances**
  - **New Icon.**
  - **Enter Scheme name.**
  - **Change values for Net Classes or Clearances.**
  - **Reset options allow you to return values by type back to the master scheme.**

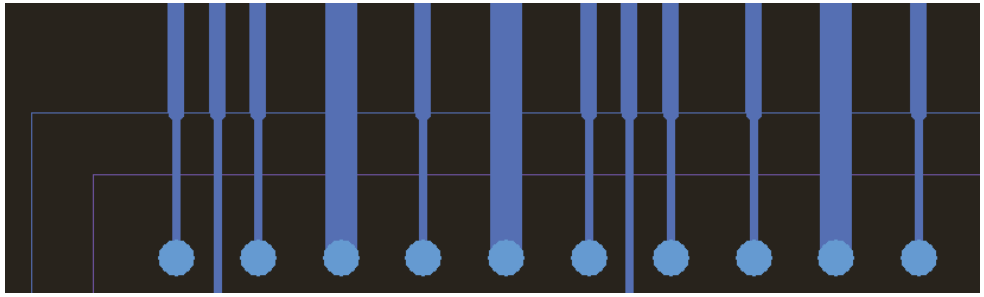


- **Used in Rules by Area Application**
  - **Followed by routing and DRC.**

Rule Areas

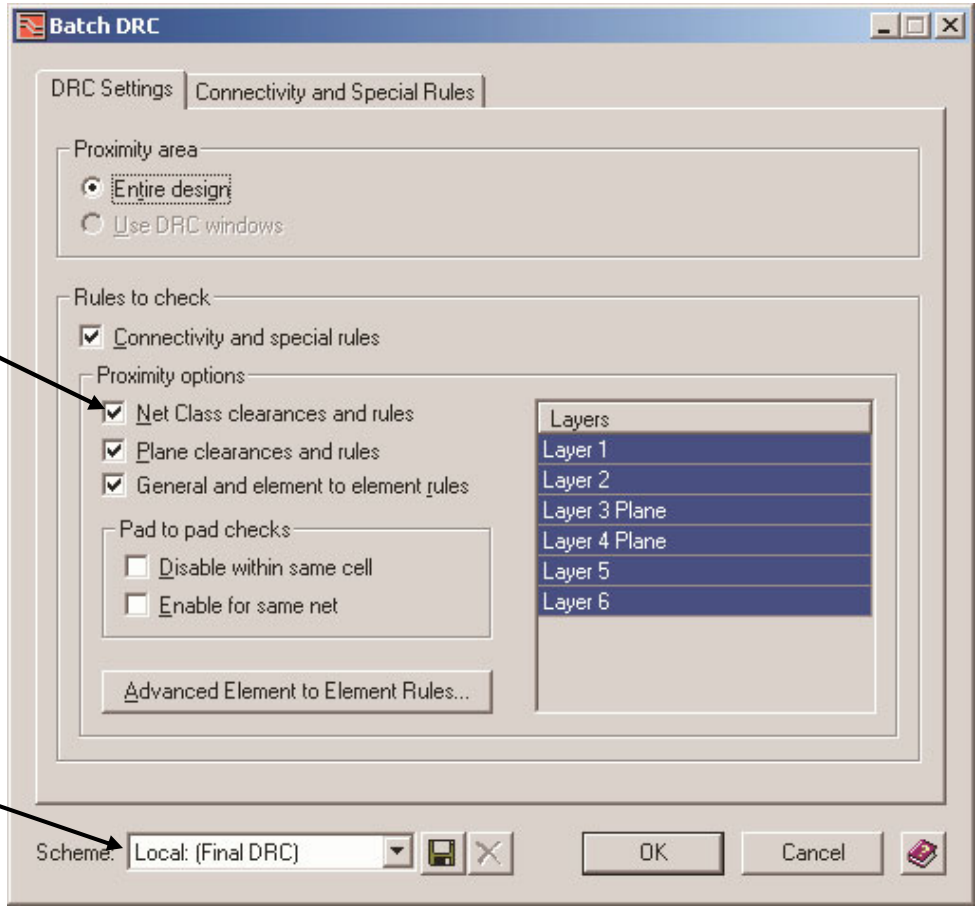
- Sets an area of the board to use a Net Class scheme rather than the Net Class Master settings.
  - Followed by Online DRC, Routing, Batch DRC.
- How to make one.
  - Create Net Class Scheme
  - Draw Mode
    - Type - Rule Area
      - Set Layer
      - Choose Scheme Name
    - Draw as a closed element.

- Used to resolve rule bottle-necks.
  - Connector escape patterns
  - BGA Fanouts
  - Analog sections



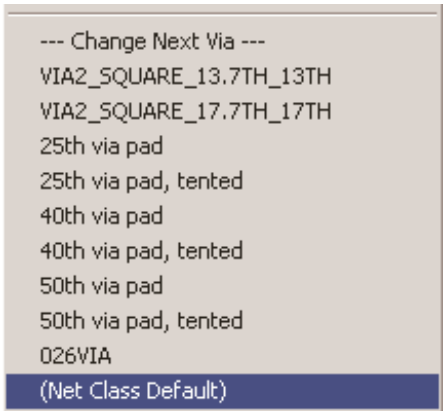
DRC for Net Class Proximity Values

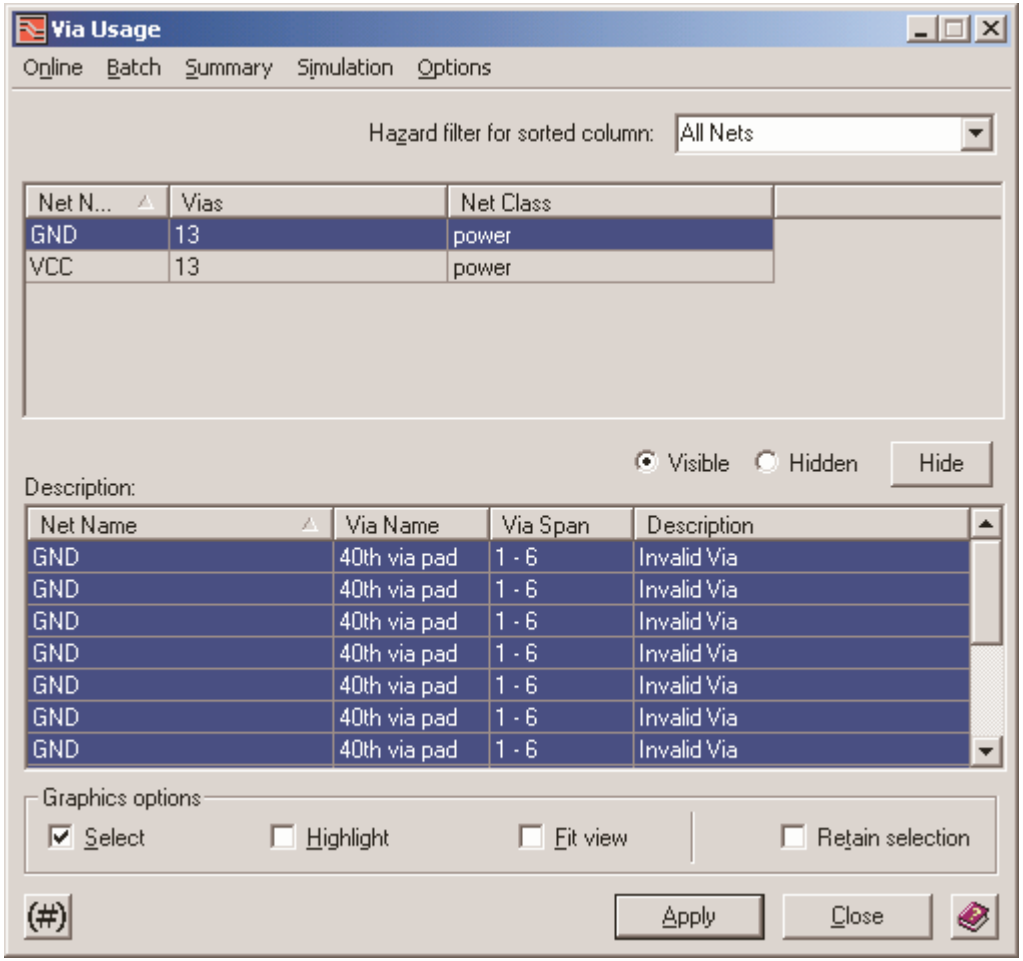
- **To run Batch DRC checks on Net Classes and Clearances:**
  - **Turn on Net Class and Clearance Rules**
  - **DRC setup can be saved in a scheme.**



Hazards — Online

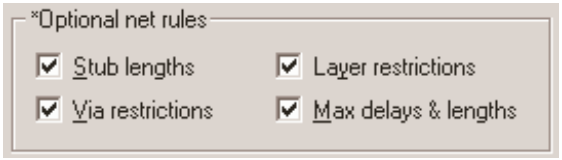
- **Via Usage**
  - **When a non-Net Class specified via is used.**
  - **How did I get this?**
    - **Select a via - Properties, change the Padstack name - OK.**
    - **While routing, use a popup menu to use a non-standard via.**

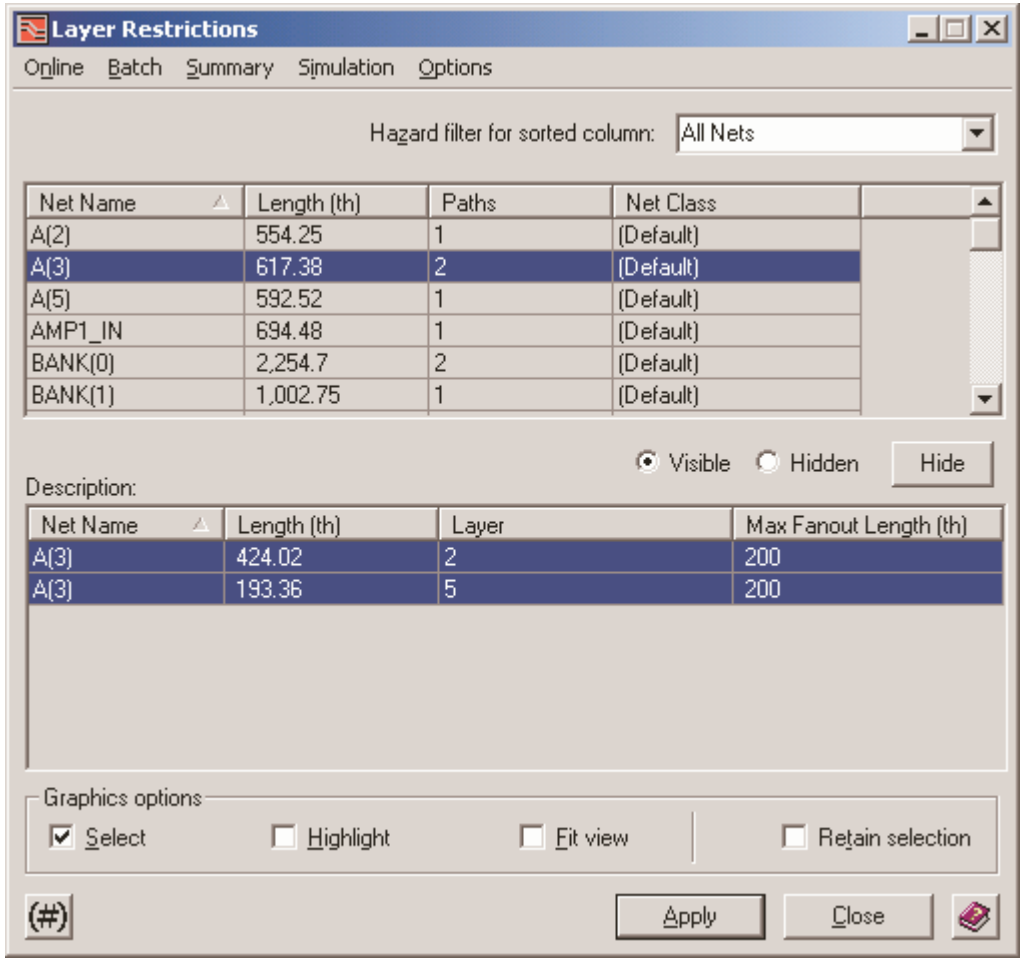




Hazards — Online (Cont.)

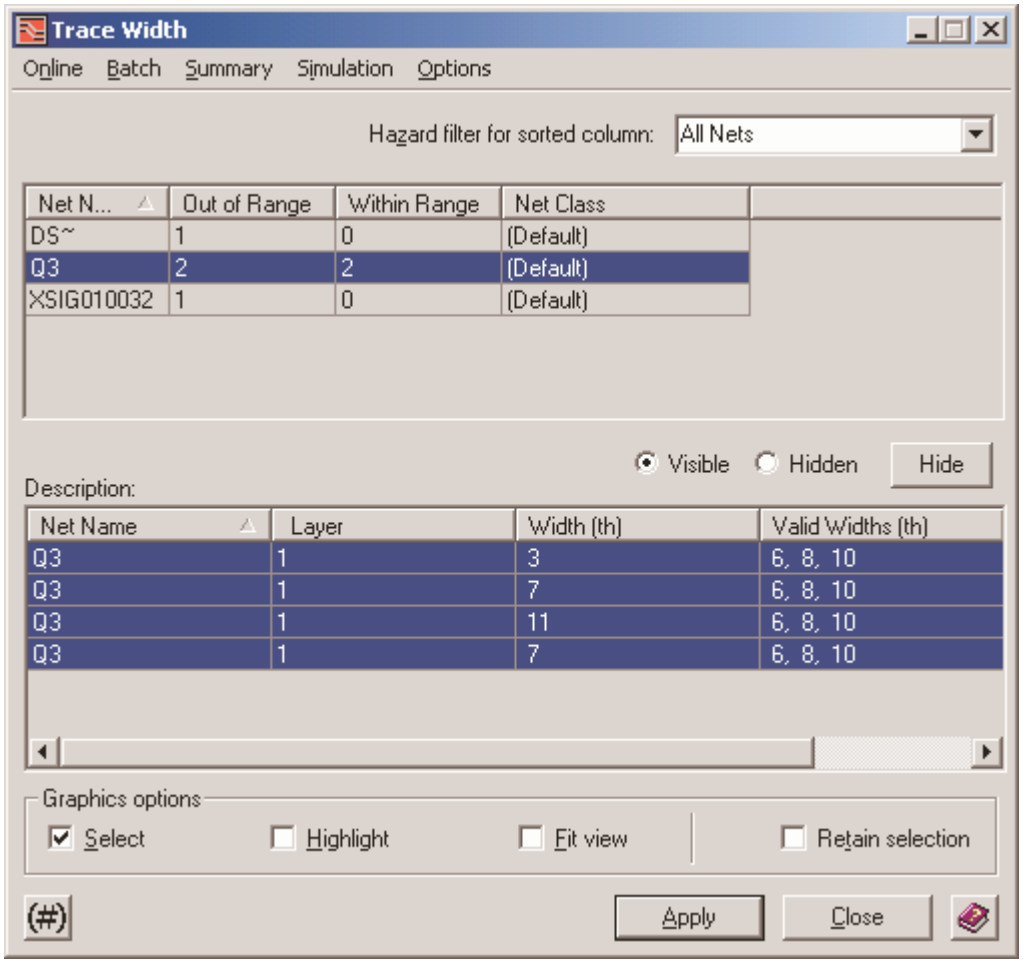
- **Layer Restrictions**
  - **When a signal is routed on a Restricted layer.**
  - **How did I get this?**
    - **Interactive Editing with Editor Controls - Routes tab - Optional Net Rules - Layer Restrictions turned Off.**





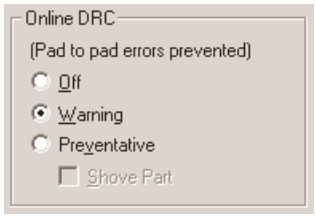
Hazards — Online (Cont.)

- **Trace Widths**
  - **Out of range**
    - **There are widths that are greater than the Expansion width or less than the Minimum Width.**
  - **Within Range**
    - **Widths are between the Minimum width and the Expansion width, but not equal to the Minimum, Typical or Expansion widths.**
  - **How did I get this?**
    - **While routing - cw =**
    - **Use the Change Width command.**

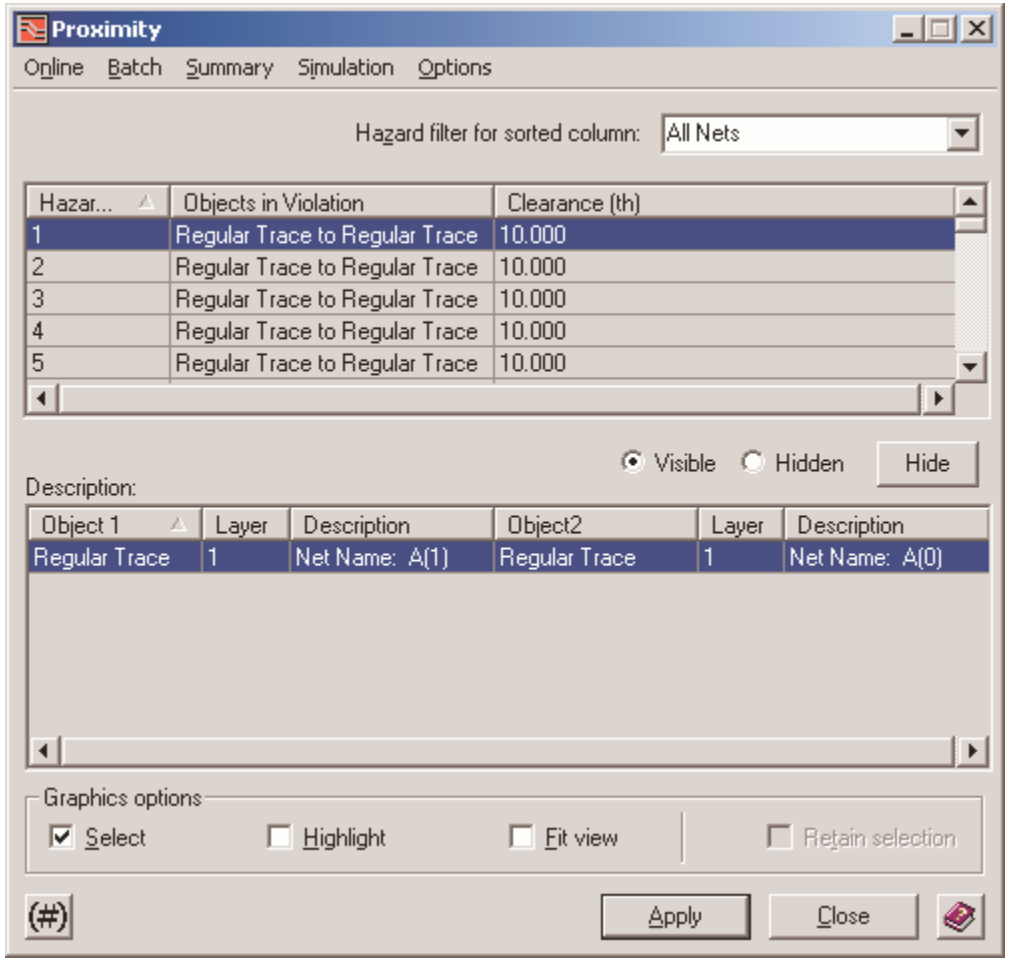


Hazards — Batch

- **Proximity**
  - **One element is too close to another element.**
  - **How did I get this?**
    - **Placement - Online checking in Editor Control is set to Off or Warning.**



    - **Copper to Copper - the Clearance values in Net Classes and Clearances were changed after the routing was done. Copper to Copper clearances can not be violated in any other way.**



Lab Preview

- **This Module has 3 Labs.**
  - **Lab 1 — Using Layer Stackup**
    - In the Control1_reva database, you will use The Setup Parameters: Layer Stackup command to investigate options for your board, then make assignments in Net Classes.
  - **Lab 2 — Rules Schemes and Rule Areas**
    - In the Control1_reva database, you will create a Rules Scheme and a Rule area to solve a DRC problem on the board.
  - **Lab 3 — Rules Schemes and Rule Areas (Optional)**
    - With minimum instruction, you will do the same operation as in Lab 2 on the Control2_reva database.

Advanced Expedition PCB

Module 6

Vias, Fanouts and Pads

Objectives

Upon completion of this lesson and lab, you will be able to:

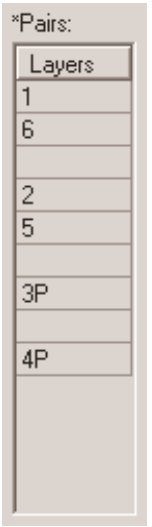
- **Interactively Place Vias.**
- **Effectively Create Fanouts from SMD Pads.**
- **Use the Copy Trace Command to Create Fanouts.**
- **Do Editor Control Settings for Via Control.**
- **Use Cells with Embedded Fanout Patterns.**
- **Use the Padstack Processor.**

Interactive Vias

- **Interactively add the via.**
  - **6 Ways to add a via:**
    - **Space Bar**
      - **Uses Layer Pairs**
    - **Double Click**
      - **Uses Layer Pairs**
      - **Enabled on Editor Control - General Tab**

    - **v - keyin**
      - **Uses Layer Pairs**
    - **Display Control**
      - **Click on the “to go to” layer to make it active.**
    - **Arrow Keys on Key Pad**
      - **Move up and down one layer at a time.**
      - **View Active Layer in Status Bar.**

    - **cl # - keyin**
      - **Changes to the specified layer number.**



Layer Pairs setup on Editor Control - General Tab

Fanouts

- **Why it is important.**
  - **Surface Mount Devices need access to inner layer.**
    - **Routing without fanouts has a tendency to block exits from SMD pads.**
    - **Routing without fanouts gives access to only the surface layers bias routing direction.**
  - **If Fanout vias are later found to be unnecessary, they are removed.**

Auto-Active Fanout

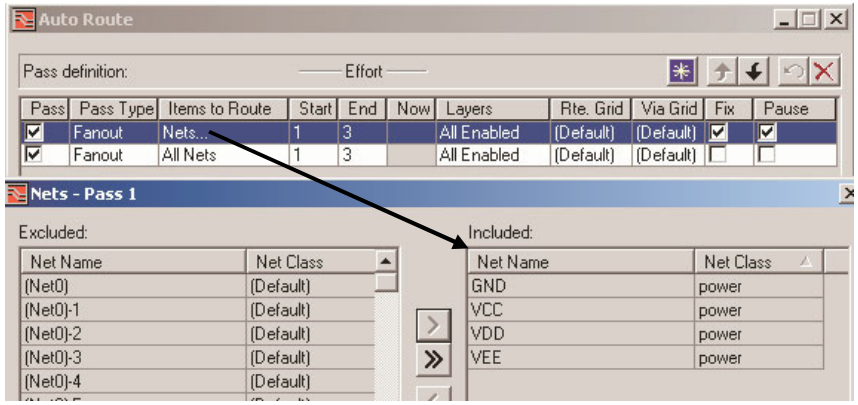
- **Semi-Automatic Fanout Generation**
  - **Select the pins to fanout.**
  - **Issue the command**
    - **Route > Interactive > Fanout**
    - **Action Key** 

    - **Tool Bar** 

- **Difference between Semi-Automatic Fanout and Auto Router fanout.**
  - **Semi-Automatic fanout is truly “gridless” unless a via grid is specified.**
  - **Auto Router fanout develops a “virtual grid” unless a via grid is specified.**
    - **Virtual grid will allow at least one of the most standard typical trace width between the vias using the most typical clearance.**

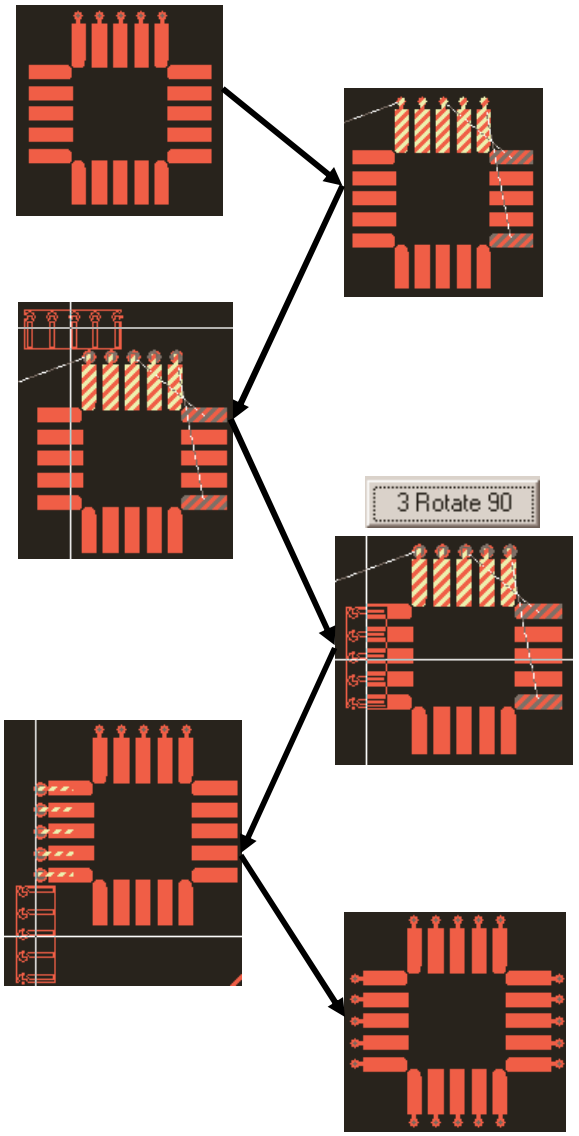
Automatic Fanout

- **Use the Auto Router**
  - **Set up Fanout Passes**
    - **Effort Levels**
      - **1 - Uses closest available “virtual grid”**
      - **2 - Expands possibilities for other grid points - some push and shove**
      - **3 - Further expands search for grid points - more push and shove**
  - **Strategies**
    - **Separate Passes for Wide Traces**
      - **Pause**
      - **Use review Hazards to find uncompleted fanouts.**
    - **Saved fanout schemes**
    - **Check for Open Fanout hazards before continuing with the route.**



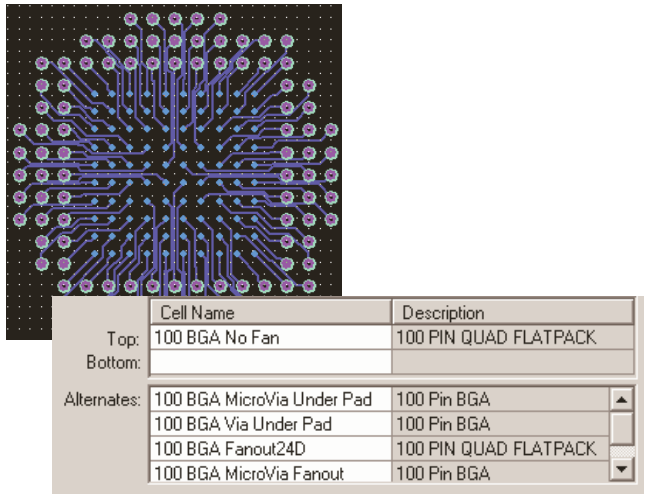
Copy Trace — Fanouts

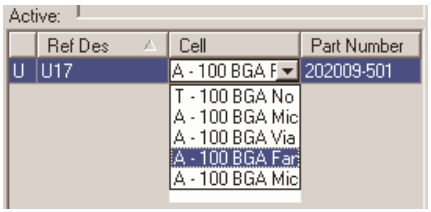
- The Copy Trace command can be used to copy one or multiple traces from one location to another.
  - When placing the copy, it must make a “legal” connection.
  - The copy can be rotated or pushed to another layer.
- How to use it:
  - Memory array traces
  - Fanout control
  - Any trace duplication
- How it works
  - Add traces to copy
  - Select traces to copy
  - Issue Copy Trace command
  - Click to place copy of trace



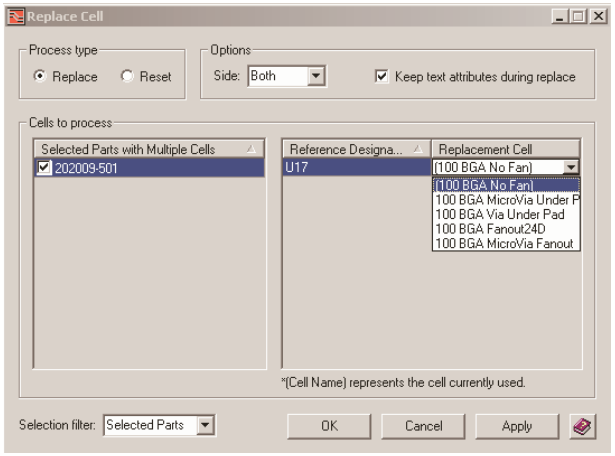
Fanouts in Cells

- Fanouts can be built into a cell in the Cell Editor.
- Cells with fanouts are included as Alternate Cells in the PDB definition.
- In Expedition PCB, to use the Alternate Cell:
  - Place the Part using the Alternate cell. - OR -
  - After placement, use ECO > Replace Cell
    - Select the Part.
    - Issue the command.
    - Check the Part on the list.
    - Select the Alternate from the menu.
    - Apply.



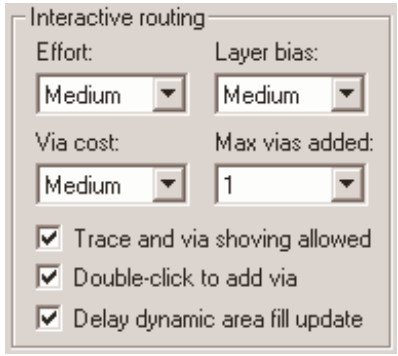


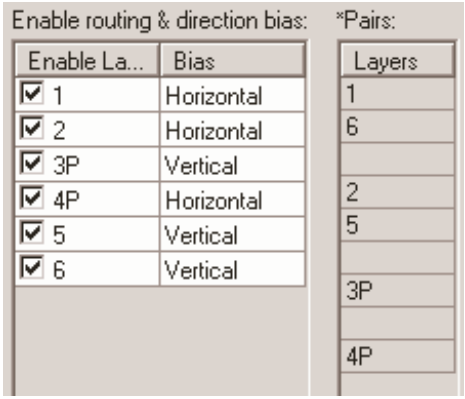
Place Parts and Cells



Editor Control — Vias and Fanouts

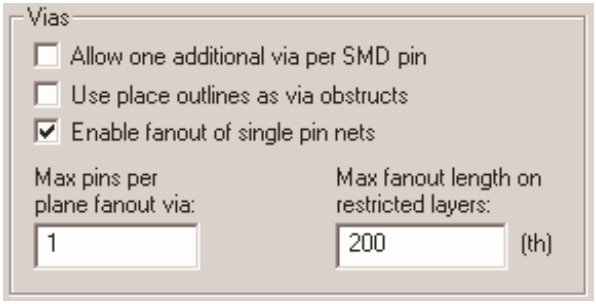
- **General Tab**
  - **Effort Level - Layer Bias - Via Cost**
    - **These three settings work together to determine "how hard" the Auto Active routing commands work.**
    - **Higher Layer bias will force more vias as the router changes layer to maintain layer bias.**
    - **Higher Via cost will force more routing against the bias as the router avoids putting in vias.**
  - **Max vias added**
    - **Sets the number of vias that can be added by the Auto Active commands.**
    - **If Layer bias is high, many times Auto Active routing will fail if it is not set to at least two.**
  - **Layer Bias and Pairs**
    - **A good plan is to set layer pairs to have opposing layer bias.**
    - **The Auto Router does not use Layer Pairs at all.**



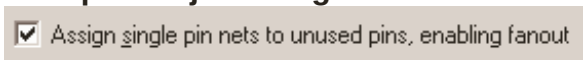


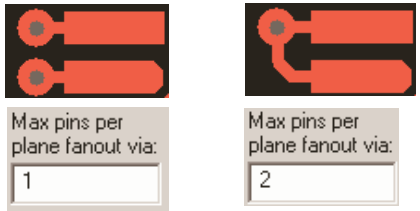
Editor Control — Vias and Fanouts (Cont.)

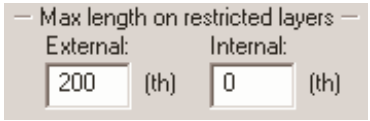
- **Route Tab**
  - In conjunction with limiting vias for a signal, you can allow one fanout per SMD pad for the fanout.
  - Placement Outline on cells can by used as a via obstruct, ensuring that all fanouts are external to the part.
  - You can enable the fanout of single pin nets.
    - (Net0)-n - assigned by Forward Annotation
    - These fanouts are removed by a Remove Hanger command.
  - The number of pads that can be attached to one plane connection via is controlled.
  - If an external layer is restricted for a Net Class, the fanout can still be enabled by setting a maximum fanout length.



Setup > Project Integration command

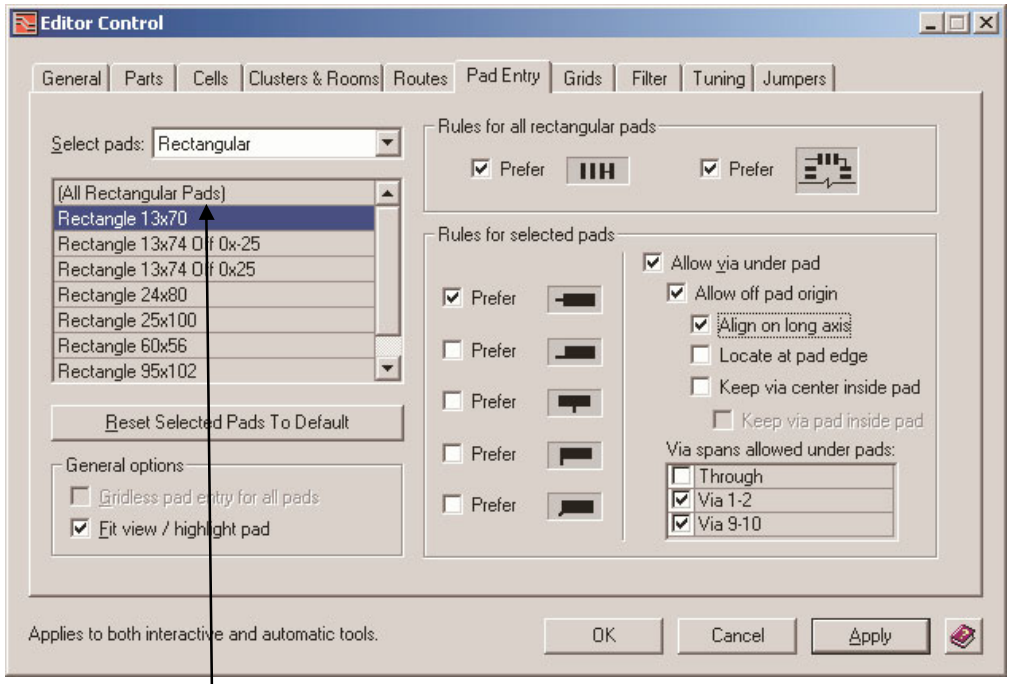






Editor Control — Vias and Fanouts (Cont.)

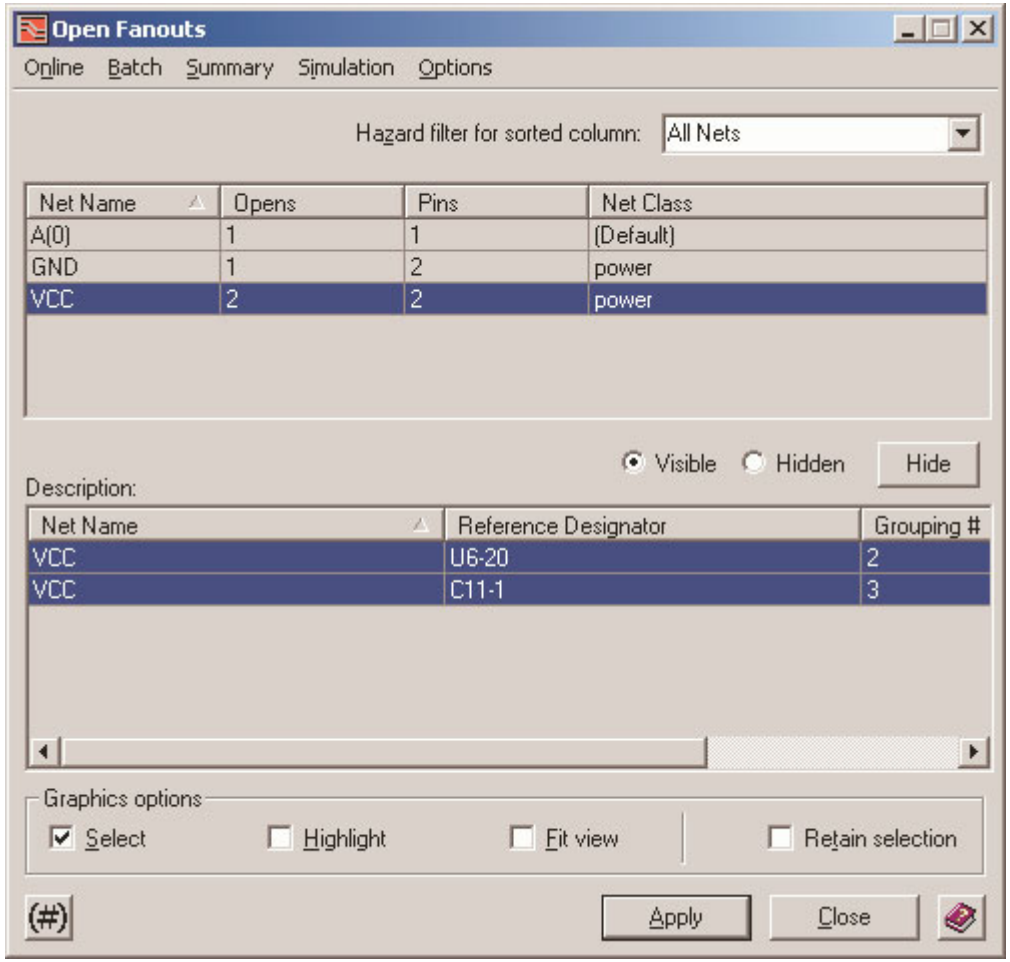
- **Pad Entry Tab**
  - Select Pad type.
  - Select Pad name.
  - Set preferences for Pad entry on the selected Pad.
    - Notice the term is “prefer”.
    - Non-preferred Pad Entry is reported as a Hazard.
  - Set Via under pad preferences.
    - Selections are hierarchical
    - Generally via under pad applications are only allowed for blind via spans.



- **Pad entry preferences can be set for all pads of a type, and then those preferences can be over-ridden for a specific pad name.**

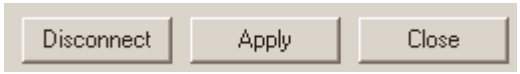
Online Hazards — Open Fanout

- **Open Fanout**
  - **When a SMD pad that does not have a completed connection, also does not have a Fanout for access to inner layers..**
  - **How did I get this? Something obstructed the fanout command, or the fanout command wasn't executed on the hazard signal.**



Online Hazards — Pad Entry

- **Pad Entry**
  - **When a signal enters a pad in a non-preferred manner.**
    - **Non Preferred**
    - **Bend adjacent to pad**
    - **Misaligned trace**
  - **How did I get this?**
    - **Pad Entry is a preference. The router will violate Pad Entry rules in favor of a higher completion rate.**
  - **Disconnect**
    - **Disconnects the offending trace segment on the selected hazard.**



Net Name	Violations	Net Class
ACLK[0]	1	(Default)
HD[11]	1	(Default)
PWROK	1	(Default)

Visible Hidden Hide

Description:

Net ...	Pad Name	Pin	Layer	Violation Type
ACLK[0]	Rectangle 13	U1-18	10	Non Preferred

Net Name	Violations	Net Class
ACLK[0]	1	(Default)
HD[11]	1	(Default)
PWROK	1	(Default)

Visible Hidden Hide

Description:

Net ...	Pad Name	Pin	Layer	Violation Type
HD[11]	Rectangle 13	U1-14	10	Bend adjacent to pad

Net Name	Violations	Net Class
ACLK[0]	1	(Default)
HD[11]	1	(Default)
PWROK	1	(Default)

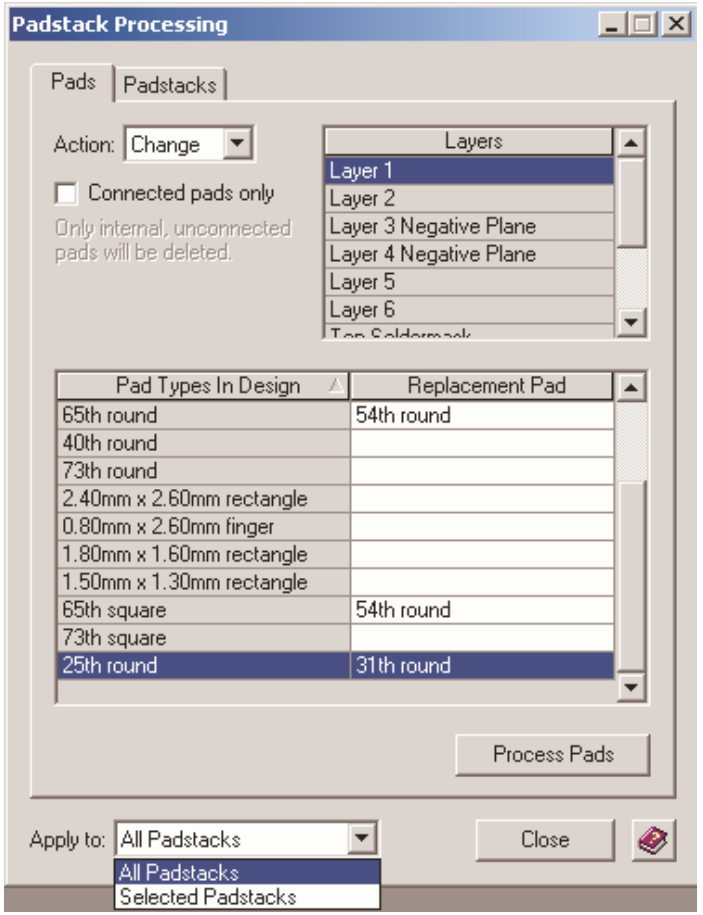
Visible Hidden Hide

Description:

Net ...	Pad Name	Pin	Layer	Violation Type
PWROK	Rectangle 13	U1-19	10	Misaligned trace

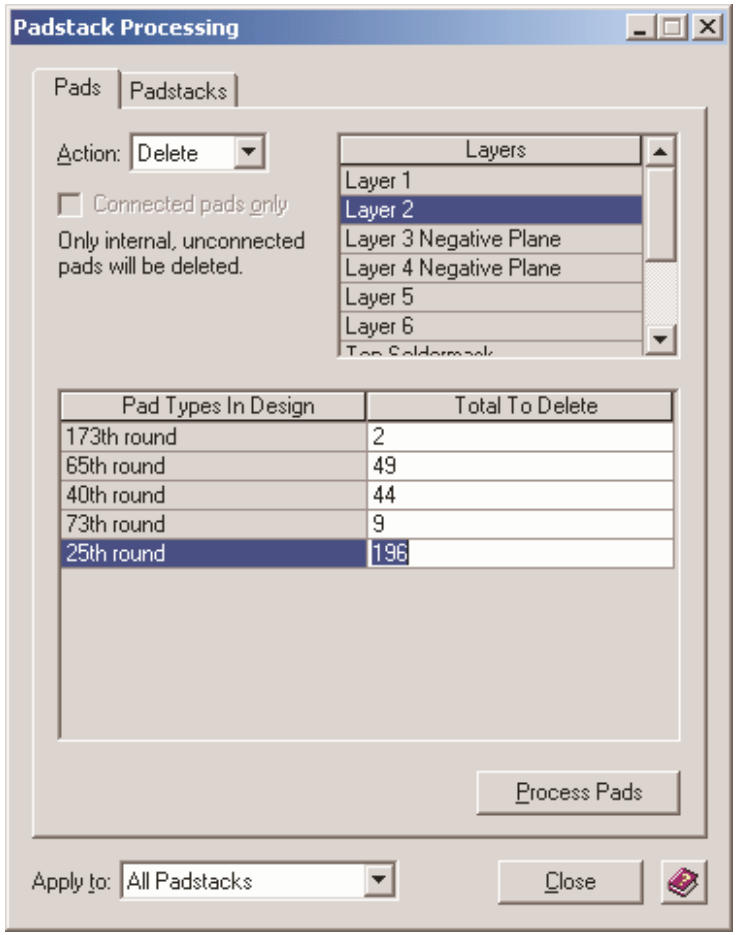
Padstack Processor — Pads

- **Padstack Processor can only do 4 things.**
  - **Change Pads**
    - **Select layer(s) to change on.**
    - **Set a replacement pad for pads to change.**
    - **Apply to:**
      - **All Pads of that name on the selected layers.**
      - **Only Padstacks that are selected in graphics.**
    - **Click on Process Pads.**



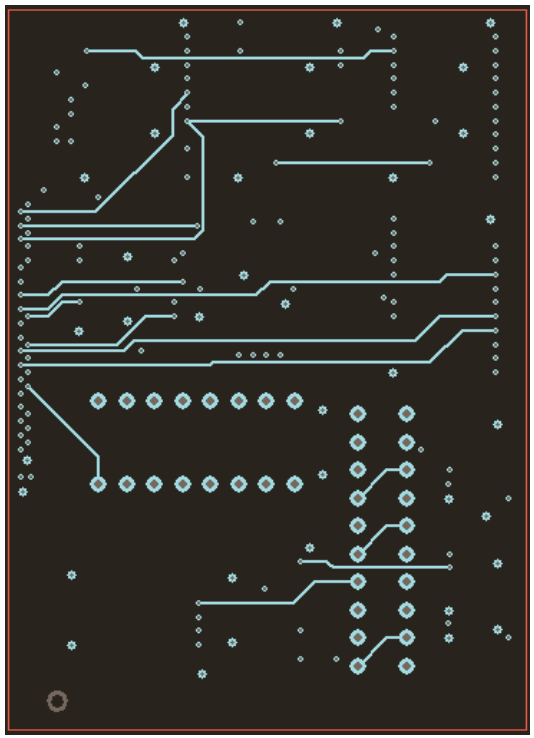
Padstack Processor — Pads (Cont.)

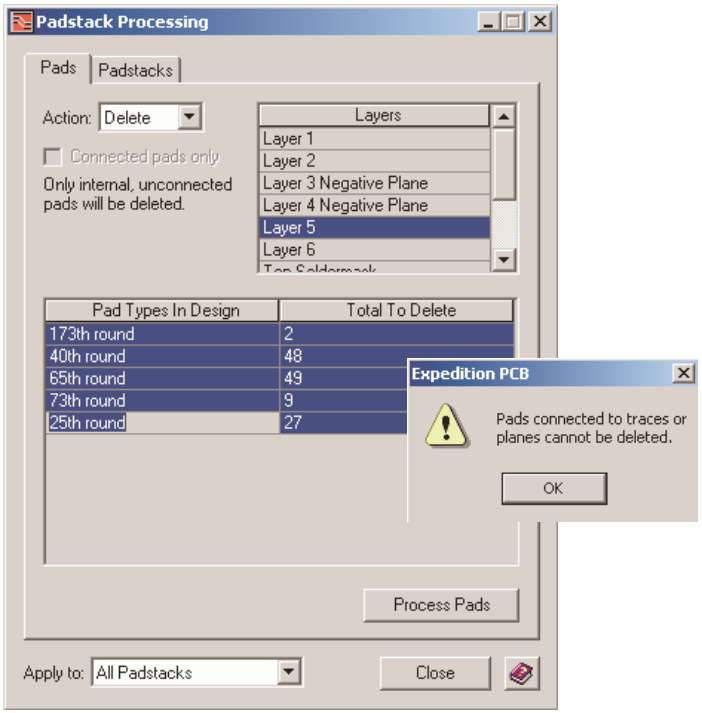
- **Padstack Processor can only do 4 things.**
  - **Delete Pads**
    - **Select layer(s) to delete from.**
    - **Select the Pad name to delete.**
      - **The number of Pads that will be qualified is shown.**
    - **Apply to:**
      - **All Pads of that name on the selected layers.**
      - **Only Padstacks that are selected in graphics.**
    - **Click on Process Pads.**

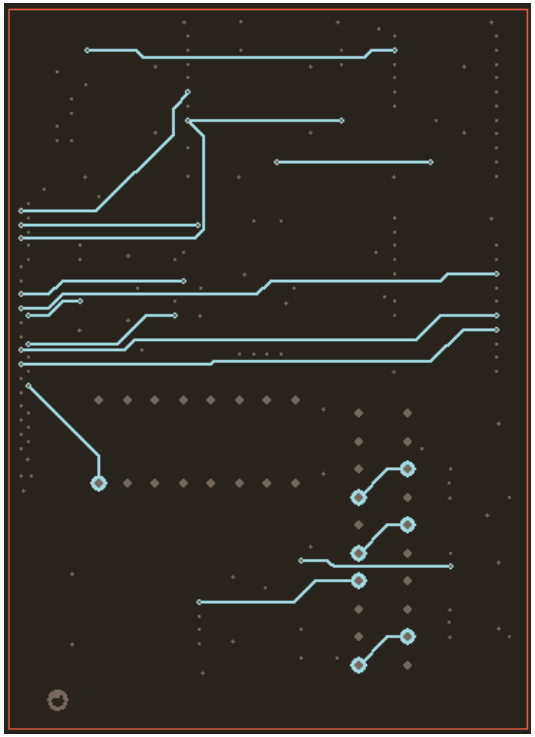


Padstack Processor — Inner Layer Pad Removal

- **If you want unconnected pads removed from pins and vias on inner layers, use the Padstack Processor.**
  - **Edit > Modify > Padstack Processor**

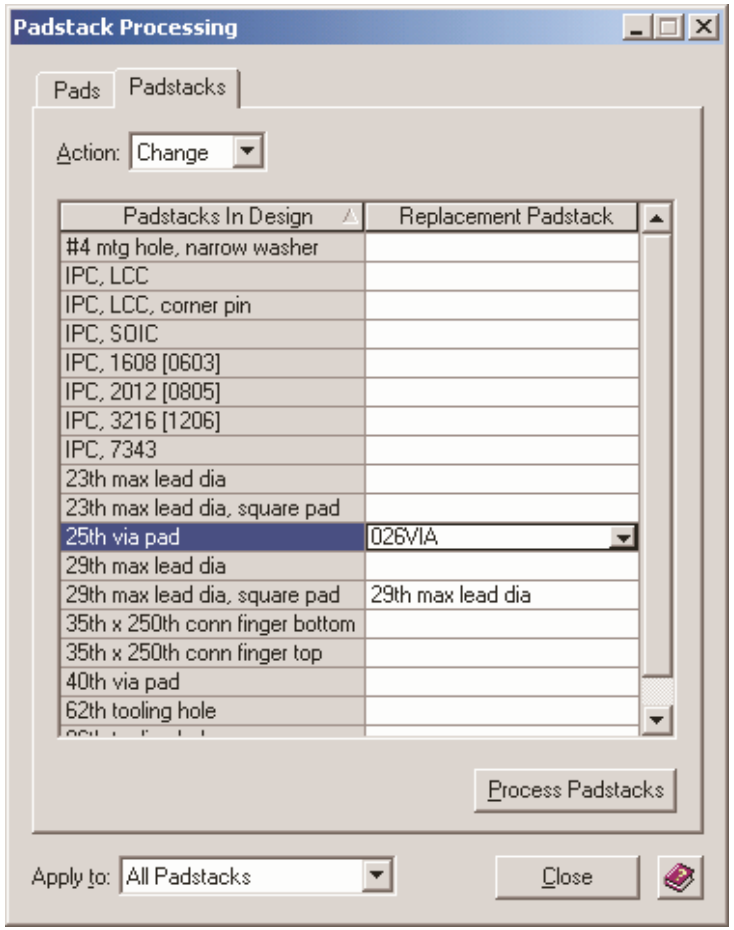






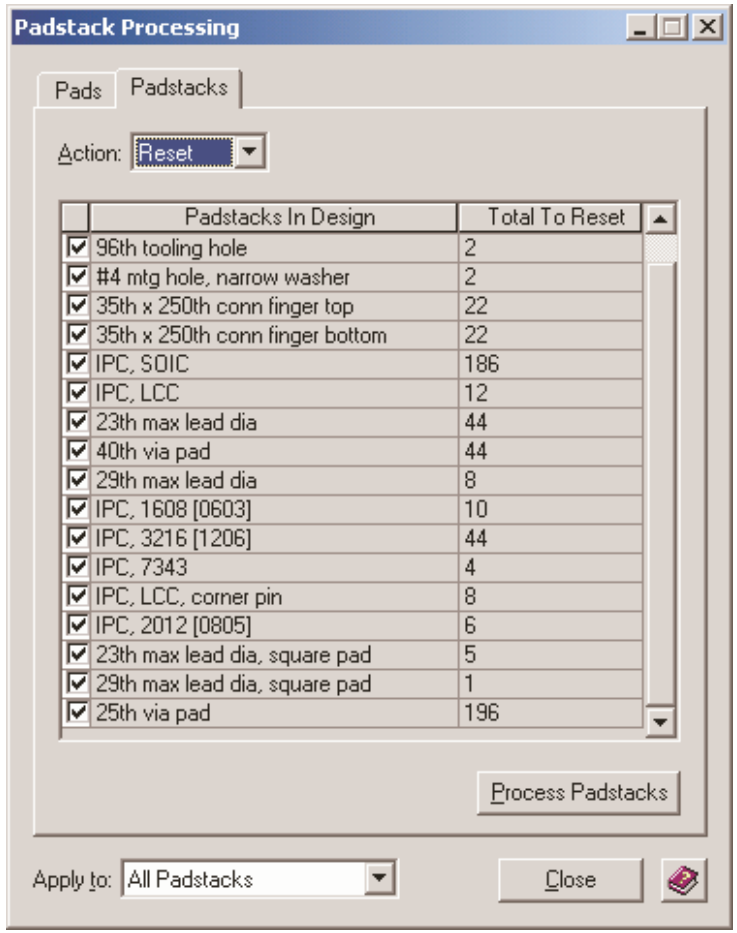
Padstack Processor — Padstacks

- **Padstack Processor can only do 4 things.**
  - **Change Padstacks**
    - **Select a Replacement Padstack for Padstacks to change**
    - **Apply to:**
      - **All Padstacks of that name.**
      - **Only Padstacks that are selected in graphics.**
    - **Click on Process Padstacks.**



Padstack Processor — Padstacks (Cont.)

- **Padstack Processor can only do 4 things.**
  - **Reset Padstacks**
    - **Check the Padstacks to be reset.**
    - **Apply to:**
      - **All Padstacks of that name.**
      - **Only Padstacks that are selected in graphics.**
    - **Click on Process Padstacks.**
    - **Reset is used if Pads in a Padstack have been changed or deleted and you want to rebuild the Padstack as per the definition in the Local Padstack Library.**
    - **If you have changed a Padstack, Reset WILL NOT change it back to the original.**



Lab Preview

- **This Module has 2 Labs.**
  - **Lab 1 — Fanout Mechanisms**
    - Simple - Get 100% fanout of the Control1-reva database. You will use Rule Areas, Copy Trace the AutoRouter, Review Hazards and Interactive editing to meet the goal.
  - **Lab 2 — Fanout (Optional)**
    - With little direction, you will get 100% fanout of the Control2_reva database.

Advanced Expedition PCB

Module 7

Routing Issues

Objectives

Upon completion of this lesson and lab, you will be able to:

- **Better use interactive routing commands**
- **Place conductive shape elements**
- **Move routed circuits**
- **Change existing trace widths**
- **Create Curved Traces**
- **Use Dynamic Area Fills**
- **Create Breakout Traces**
- **Create Teardrops**

Plow Modes

- There are four Plow Modes during Interactive Routing.
  - Forced
  - Angle
  - Route
  - Dyna Plow
- Plow modes must be enabled in Editor Control - Routes Tab.

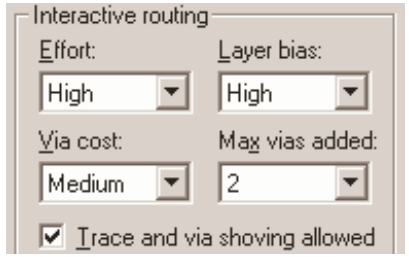
- The command is modal - once in plow mode, simply select another pad, trace or via to start a new plow operation.
  - Escape or Right Click to leave plow mode.
- Toggle between Plow modes using the Toggle Plow Action Key.

Plow Modes — Forced Plow

- **The default state once you select the Plow command.**
  - **Select a part pin, trace or via to begin placing a trace in your design.**
  - **Prospective trace follows the cursor and displays as a hockey stick.**
  - **Click to set an “anchor point”.**
  - **Trace flows around any obstacles or pads.**
  - **Traces are pushed aside if possible.**
  - **Vias are NOT added automatically.**
- **Undo**
  - **During Forced Plow removes to the last anchor point**
  - **After Forced Plow removes the last plow results.**
- **Via locations are shown during plow. Vias can be added using any interactive method.**

Plow Modes — Route Plow

- An Auto-Active/Interactive Plow solution.
  - Select a part pin, trace or via to begin placing a trace in your design.
  - Prospective trace follows a Netline path to the cursor (straight Line).
  - Click to set an “anchor point”.
  - Trace is auto-actively routed to the new “Anchor Point”.
  - Traces are pushed aside if possible.
  - Vias are added automatically.
- Undo
  - During Route Plow removes to the last anchor point
  - After Route Plow removes the last plow results.
- Via is controlled by Editor Control - General tab.
- Layer choice is left to the routing algorithms.
  - Follows all bias and restriction settings.



Plow Modes — Angle Plow

- An Any Angle routing solution.
  - Select a part pin, trace or via to begin placing a trace in your design.
  - Prospective trace follows a Netline path to the cursor (straight Line).
  - Click to set an “anchor point”.
  - Trace is routed directly to the new “Anchor Point”.
- Undo
  - During Angle Plow removes to the last anchor point
  - After Angle Plow removes the last plow results.
- There is no online control of acute angles.
- Traces or vertexes may be moved.
- Angle traces can not be pushed.

Plow Modes — Dyna Plow

- **A dynamic Forced Plow operation - lays copper as you plow.**
  - **Press and drag a part pin, trace or via to begin placing a trace in your design.**
  - **The trace follows the cursor as dynamically placed copper.**
  - **Automatically pushes and shoves traces and vias out of the way.**
  - **Release the mouse to change to the active Route Mode.**
  - **During a the active Route Mode, press and drag to enter Dyna Plow mode.**
- **Release the mouse key (leave Dyna Plow) to add a via.**

Gloss Modes

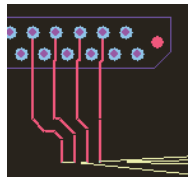
- **There are three Gloss Modes. Change between Gloss Modes using the Toggle Gloss Action Key.**

  - **Gloss On (Default) - Glosses all the way back to the source pin when each new anchor point is created, giving the most direct, shortest path while manually plowing the trace.**
  - **Gloss Partial - Glosses from anchor point to anchor point, with less strength than Gloss On.**
  - **Gloss Off - No Glossing.**
    - **The trace will be laid down as semi-fixed pattern.**
      - **Auto Router can't move it.**
      - **Auto-Active or interactive push and shove can't move it.**
      - **Interactively, you CAN move it.**

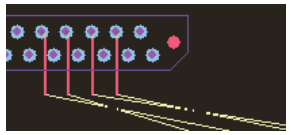
Multi-Plow

- **Multi-Plow routes multiple selected signals all at one along the same path.**
  - **Select the starting pads for the multiple signals.**
  - **Issue the Multi-Plow command (Action Key - F5)**
  - **Action Keys can be used to modify the operation.**

    - **Converge In (F2) lessens the Multi-Plow trace spacing.**



    - **Converge (F3) Out increases the Multi-Plow trace spacing.**

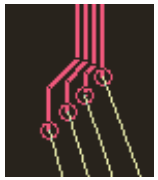


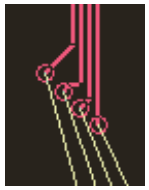
    - **Toggle Finish (F4) controls how gloss and finishing work.**
    - **Auto Finish (F5) uses AutoActive routing to finish the trace paths if possible.**
      - **During Multi-Plow, pressing the <Alt> key temporarily displays the Auto Finish path**

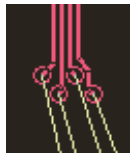
Multi-Plow (Cont.)

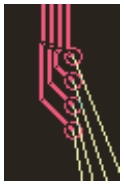
- **Multi-Plow via usage is controlled by action keys.**
  - **When you want to place multiple vias for the Multi=Plow signals, press the Place Via Action Key (F10).**

  - **The via pattern can be changed using the Toggle Via Action Key (F9).**

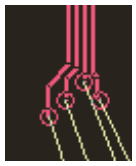

Diagonal 1

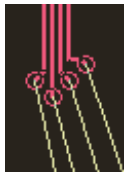

Diagonal 2


Staggered


Parallel


Perpendicular

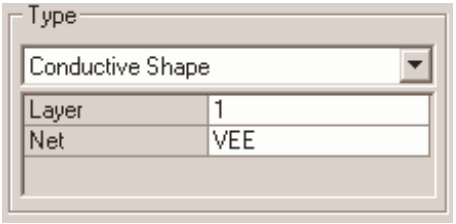


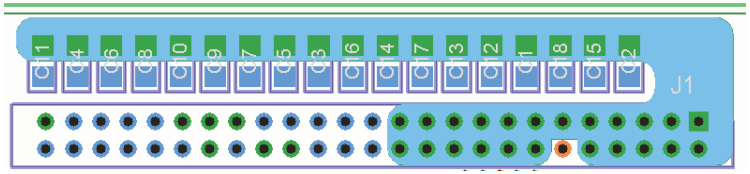


  - **After placing the vias, you can change to a different layer.**
  - **Changing vias using other than (F10) uses the current active via pattern.**

Conductive Shapes

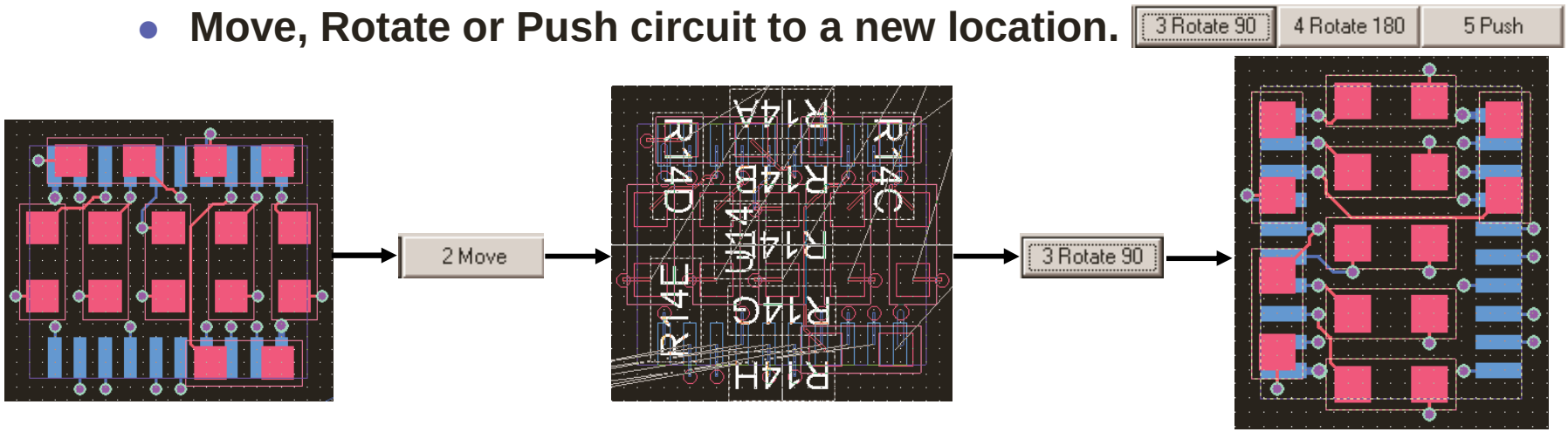
- **A conductive Shape is a coppered area that creates connectivity.**
  - **Used to replace traces for connectivity**
    - **Cross between traces and planes**
    - **Looks like plane but doesn't need to be processed**
    - **Drc'd like a trace**
      - **No online DRC when adding conductive shapes - Only Batch DRC.**
  - **Place in Draw Mode**
    - **Type - Conductive Shape**
    - **Must be a closed element.**





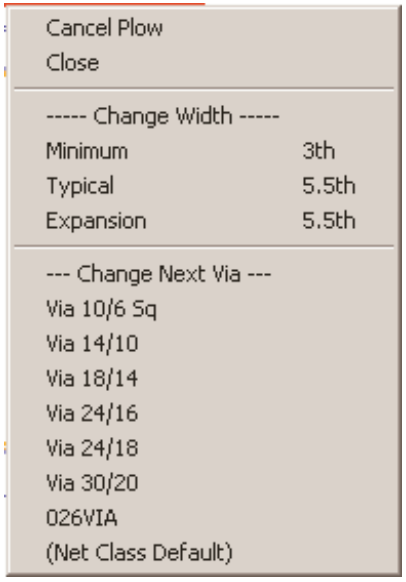
Move Circuit

- **When a circuit is placed and routed, the Place > Move Circuit command can move or rotate the circuit without disturbing the local traces.**
  - **Issue the Place > Move Circuit command.**
    - **The command is modal - it must be turned off to leave Move Circuit mode.**
    - **The command automatically activates Move Mode.**
  - **Select Parts in the circuit.**
  - **Press the Move Action Key.**
  - **Move, Rotate or Push circuit to a new location.**



Change Width

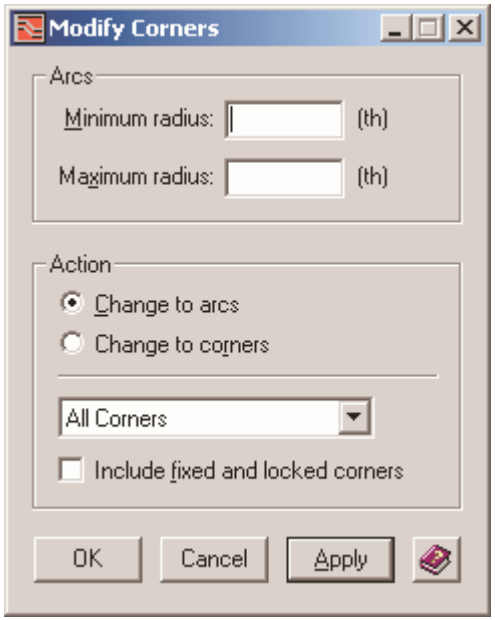
- To change width of routed traces:
  - Select the trace to change.
  - Issue the Route > Change Width command.
  - Enter the New width.
  - Click on Apply
    - Only selected segments will change if the change does not create DRC violations.
- To change Width during routing:
  - Use a pop-up menu to select the Minimum, Typical or Expansion width as set in Net Classes.
  - Keying during routing:
    - cw n - change to the width “n”
    - cw m - change to the Minimum width
    - cw t - change to the Typical width
    - cw e - change to the expansion width

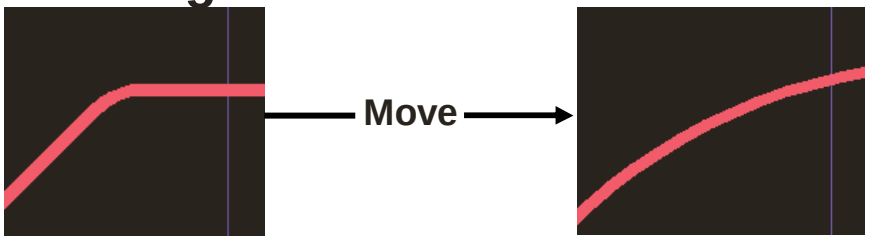


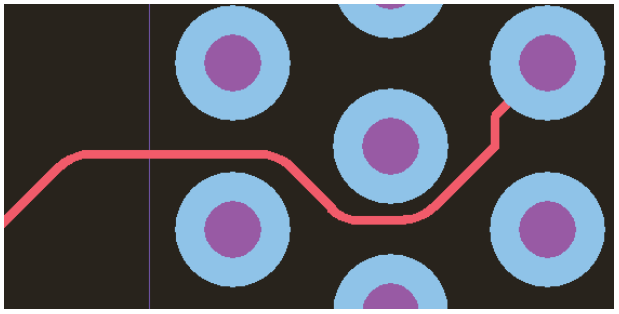
Modify Corners

- **While Plow Routing, F11 will toggle manual curved trace routing.**

- **The Route > Modify Corners command changes trace bends from or to arcs.**
  - **Set a minimum or a maximum radius to allow a variable radius. Set them the same to set the radius.**
  - **The command can work on all corners on the board or just selected corners.**
- **Traces attached to curved traces can not be moved.**
- **Curved traces can be moved, which will change the radius on the curve.**





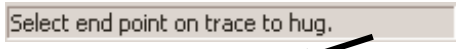


Hug Trace

- **The Hug Trace command allows routing one signal exactly next to another trace.**
  - **Issue the command using the icon or on the Route menu.**

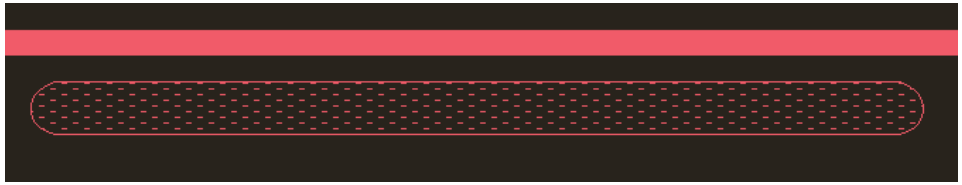
  - **Select a pin or net line on the to be routed net**

  - **Select a start point on the trace to hug**



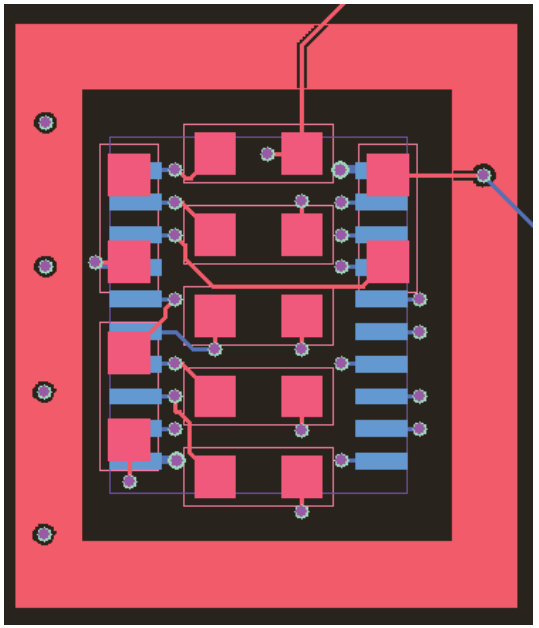
  - **Select an end point on the trace to hug**

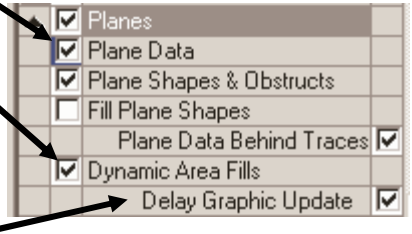
  - **click on the side of the trace to hug to set the side**



Dynamic Area Fill

- **Dynamic Area fill is an operation which will dynamically show plane shape “healing” as traces or vias pass through the area.**
- **How it works:**
  - **Draw the Plane shape in Draw Mode.**
  - **Enable Dynamic Area Fill AND Plane data on Display Control – Layer tab.**
  - **You must be in Route Mode.**

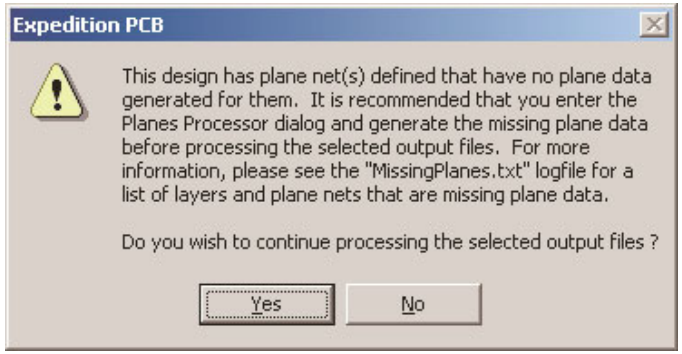




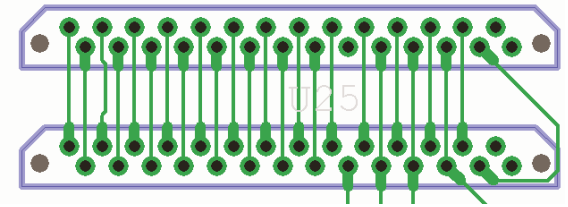
- **On Display Control you can have updates to healing delayed during DynaPlow or Move operations.**

Dynamic Area Fill (Cont.)

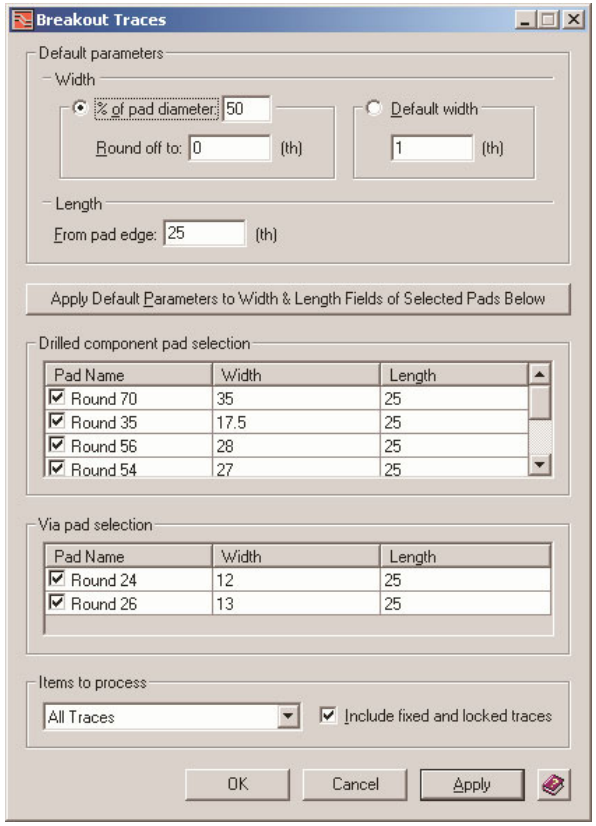
- **Remember - Dynamic Area Fill only works on Plane Shapes that have NOT been processed.**
- **Remember - Dynamic Area Fill graphics are not stored in the database as coppered area.**
  - **They MUST be processed using the Planes Processor.**
- **If you attempt Gerber output without using the Planes Processor to create "real copper" in Plane Shapes, there will be a warning prompt issued.**



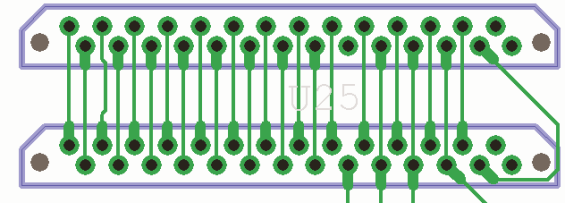
Breakout Traces



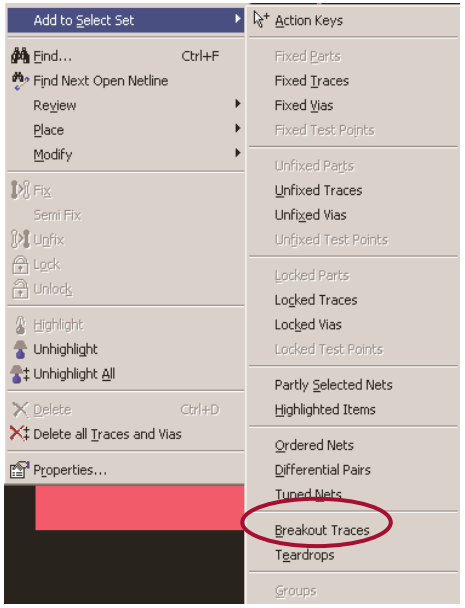
- **Breakout Traces is a methodology to add extra copper at the point where a trace leaves a pad to prevent misaligned drill outs from breaking the trace/connectivity to the pad.**
  - **Widens the trace at the pad entry point.**
- **Route > Teardrops and Breakout Traces > Breakout Traces**
  - **Set Breakout Parameters - how thick and long is the Expansion.**
  - **Check Pads and Vias which need Breakout Traces.**
    - **Width and Length can be customized for each pad - OR**
    - **Click the Apply Default . . button to use the parameters to set the Width and Length.**
  - **Set the Items to Process.**



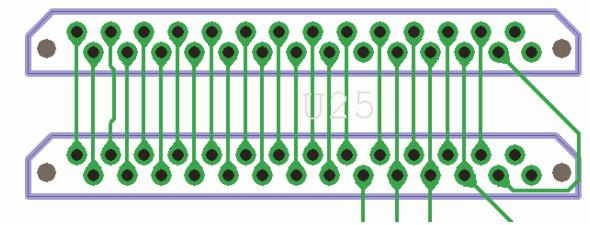
Breakout Traces (Cont.)



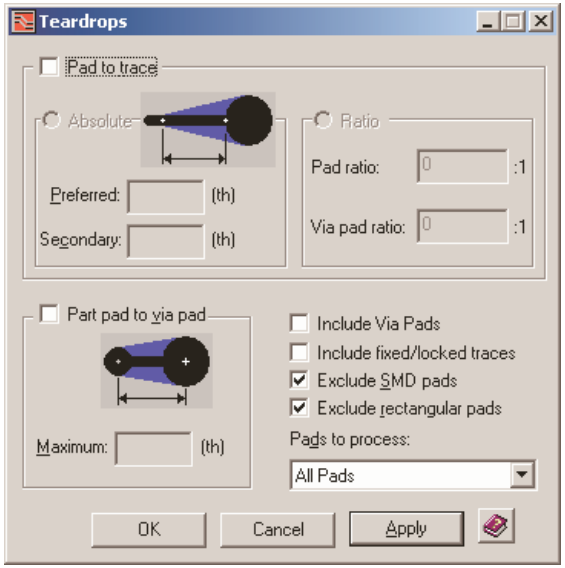
- Breakout Traces can be a Post-processing task - OR
- Set the parameters then turn on Dynamic Breakout Traces to redo Breakout Traces during editing.
- The Edit > Add to Select Set command can add Breakout Traces to the selection list.
- Visibility of Breakout Traces is controlled by Pad graphics in Display Control.



Teardrops

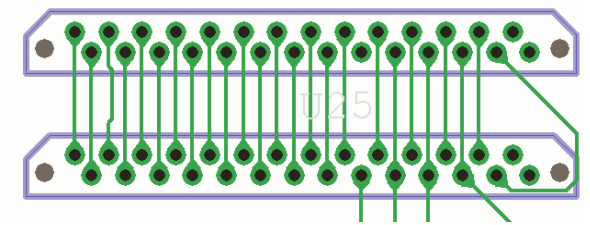


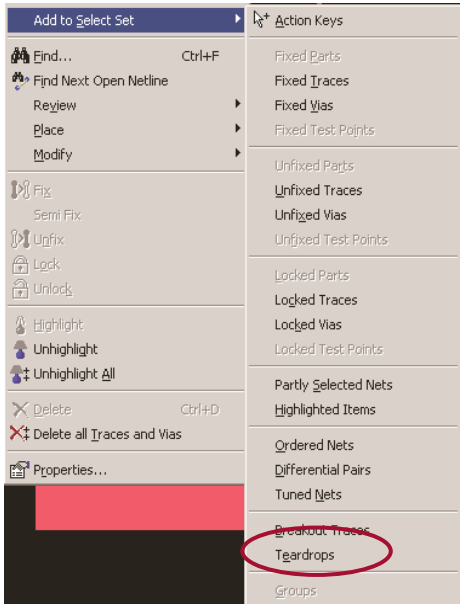
- Teardrops is a methodology to add extra copper at the point where a trace leaves a pad to prevent misaligned drill outs from breaking the trace/connectivity to the pad.
  - Teardrops the trace at the pad entry point.
- Route > Teardrops and Breakout Traces > Teardrops
  - Set Teardrop Parameters.
  - Check Pads and Vias which need Breakout Traces.
  - Set the Pads to Process.



Teardrops (Cont.)

- Teardrops can be a Post-processing task - OR
- Set the parameters then turn on Dynamic Teardrops to redo Teardrops during editing.
- The Edit > Add to Select Set command can add Teardrops to the selection list.
- Visibility of Teardrops is controlled by Pad graphics in Display Control.





Lab Preview

- **This Module has 2 Labs.**
  - **Lab 1 — Manual Routing Tools**
    - You will be putting a Conductive Shape in Control2_reva. In Control1_reva, you will be putting a ground shield, using a Rule Area, Playing with Trace Widths and manual routing techniques.
  - **Lab 2 — Post-Process Routing (Optional)**
    - In Control1_reva, you will be investigating Breakout Traces, Teardrops and Curved Traces. Alas, you will not be saving any of this work.

Advanced Expedition PCB

Module 8

Signal Integrity Issues

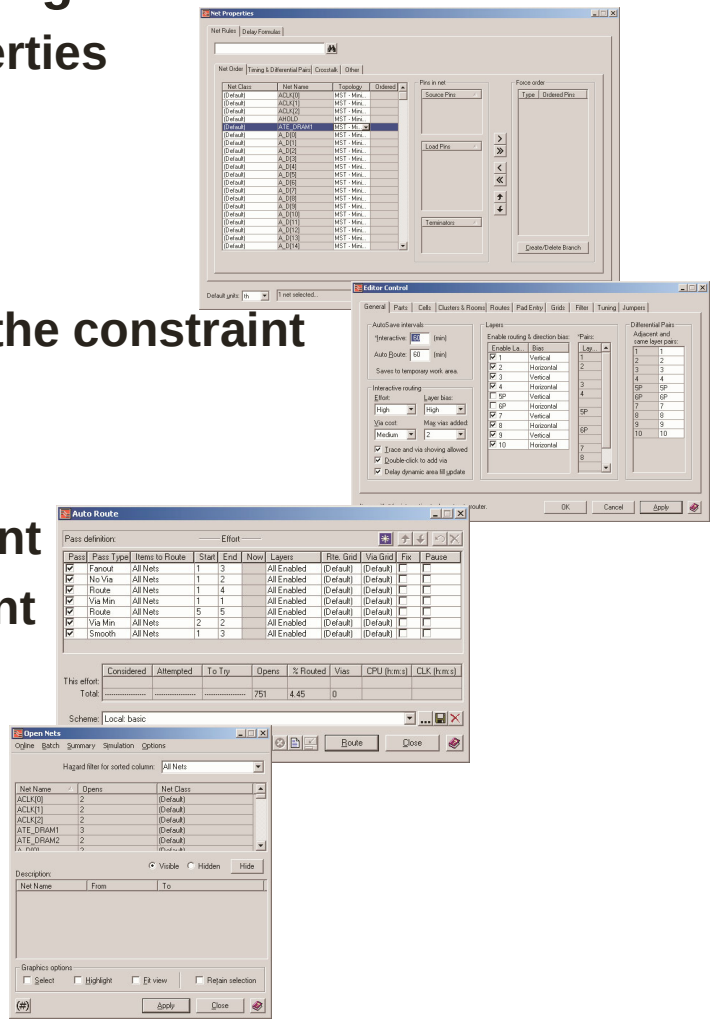
Objectives

Upon completion of this lesson and lab, you will be able to:

- **Assign Nets to Net Classes**
- **Set and Route Net Routing Order**
- **Create Virtual Pins**
- **Set Maximum and Matched Net Lengths**
- **Set and Route Differential Pairs**
- **Set Crosstalk and Parallelism Values**
- **Set Maximum Stub Length and Maximum Vias per Net**
- **Build Pin to Pin Delay Formulas**
- **Route to Signal Integrity Constraints**
- **Review and Repair Signal Integrity Hazards**

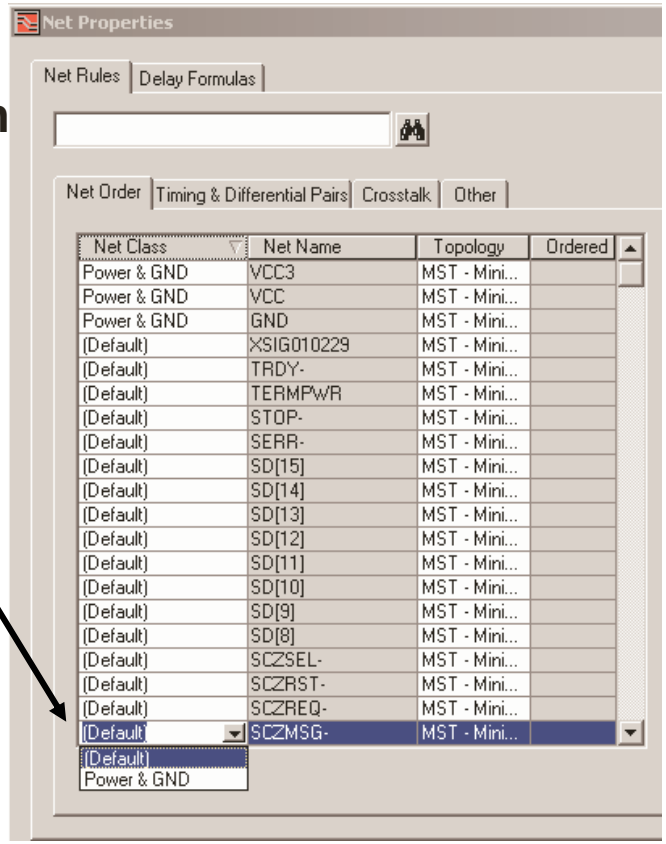
Discussion Topics

- **Each Topic will discuss the following issues:**
  - **Setting the constraint in Net Properties**
  - **Editor Control issues concerning the constraint**
  - **Interactive Routing of the constraint**
  - **Automatic Routing of the constraint**
  - **DRC checks on the constraint**
  - **Other issues about the constraint**



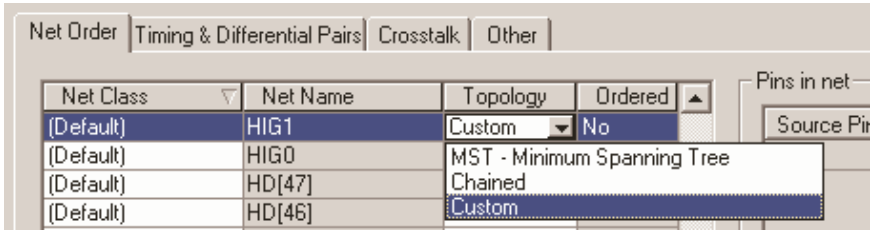
Assigning Net Classes

- **Signals are assigned to Net Classes on the Net Properties dialog — Net Order tab.**
  - **Select the net**
  - **Use the Net Class column drop down**
  - **Choose the Net Class**



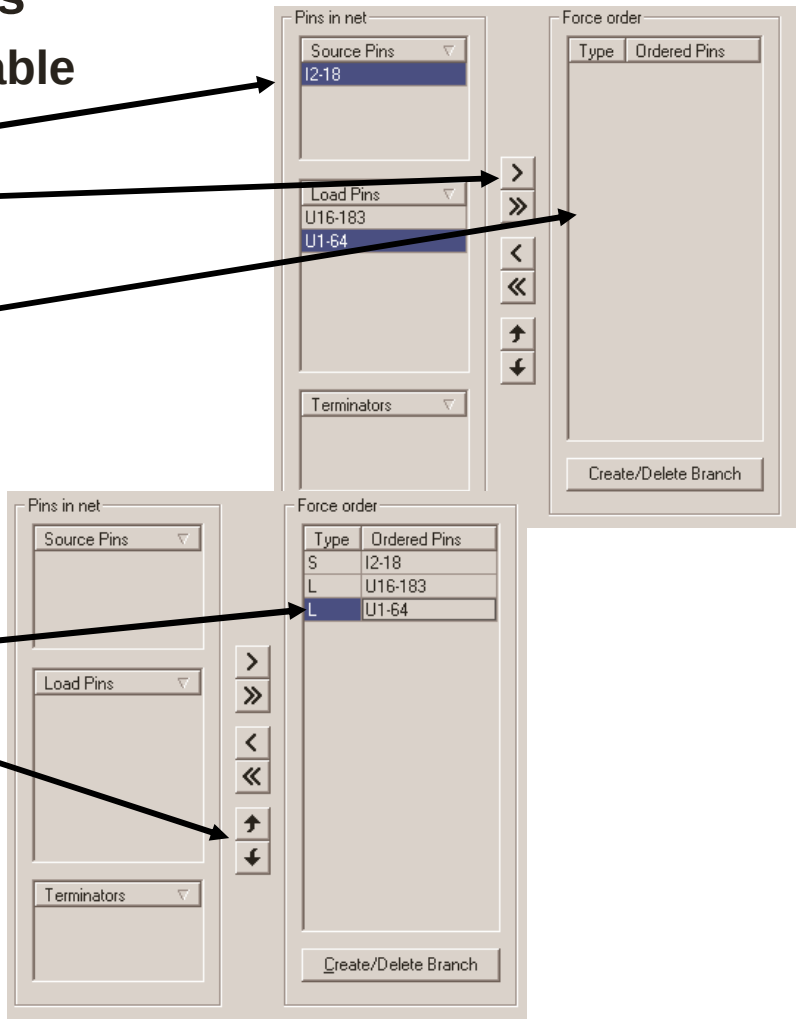
Routing Order

- **Signals are assigned a Net order topology on the Net Properties dialog — Net Order tab.**
  - **Select the signal**
  - **Choose the order topology**
    - **MST — Minimum Spanning Tree**
    - **Chained**
    - **Custom**
      - **Ordered is set to Yes or No depending on if the order has been set.**



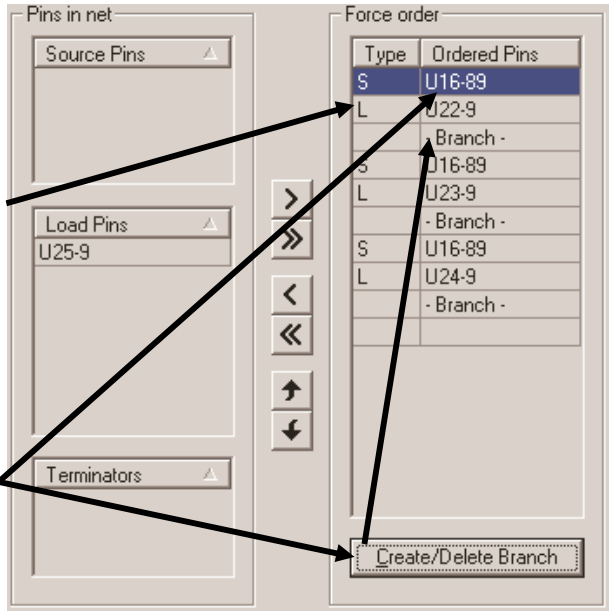
Routing Order (Cont.)

- **Setting the Order on Custom Nets**
  - **Pins are shown on Pins in Net Table**
    - **Select pin to place in order**
    - **Click the Move Arrow**
      - **OR Double Click on Pin**
    - **Pin moves to Force Order list**
  - **Repeat for other ordered pins**
  - **Pin Order can be changed**
    - **Select the pin to change**
    - **Use Up and Down arrows**



Routing Order (Cont.)

- **Branched Nets Use a pre-assigned pin as a branch point for the net**
  - **Move the first pins to the Force order table**
  - **Click the Create/Delete Branch button to put in a branch statement**
  - **Click the pin, in the Force order table to branch from**
  - **Continue with pin ordering as normal**



Routing Order — Netline Manipulation

- **Nets can be ordered graphically using the Route > Netline Manipulation command. This command enters a Mode.**

  - **Toggle View** 

    - **Toggles net visibility from Standard, to Selected Net only, to Selected Net with Shadow Mode**
  - **Toggle Topology** 

    - **Toggles the selected net from MST, to Chained, to Custom Topology.**
    - **Current status of the selected net is shown in the Status Bar**

  - **Setting Custom Order**
    - **Select and delete Netlines**
    - **Re-order Netlines by clicking pin to pin**
  - **Revert** 

    - **Returns the selected net to its initial topology**
  - **Finish** 

    Exits Netline Manipulation Mode

Routing Order — Virtual Pins

- Virtual Pins are non-schematic routing nodes that can be inserted into a nets routing order.
- Virtual Pins can only be added to Custom ordered nets.
- Virtual Pins can be used as branch points.
- Virtual Pins can be used as nodes in Delay Formulas.
  - Select Place VP 

 Drag and click to place the Virtual Pin
  - Click pin to Virtual pin connections to add Netlines

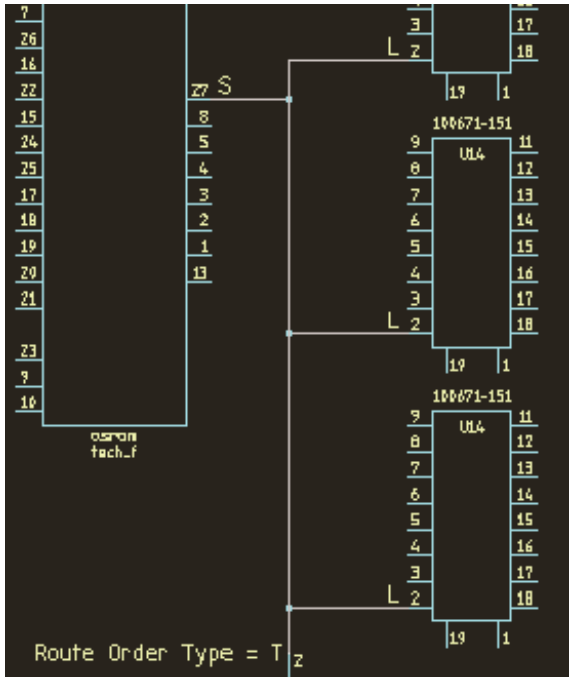
- Guide Pins are non-schematic routing nodes that guide trace to a certain point during routing.
- Guide Pins can only be added to Custom ordered nets.
  - Select the Netline to Guide
  - Select Place GP 

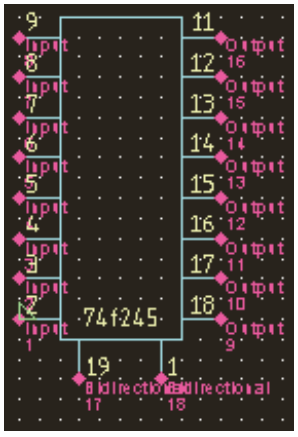
 Drag and Click to place the Guide Pin
  - Click to place another Guide pin, or use a pop-up menu to accept the Guide Pins

Pin Types

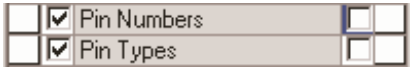
- **Pin Types come from:**
  - **The schematic “Route Pin Type” property**
    - S S
    - L L
    - T T
  - **PDB Pin Properties**
    - Terminator T
    - Input L
    - Schmidt L
    - Bidir S
    - Output S
    - Tristate S
    - OpenCollector S
    - OpenEmitter S
  - **Built in Symbol Pin Types**
    - Input L
    - Schmitt L
    - Output S
    - Tristate S
    - OpenCollector S
    - OpenEmitter S
    - Digital S
    - Power L
    - Ground L
    - Analog L

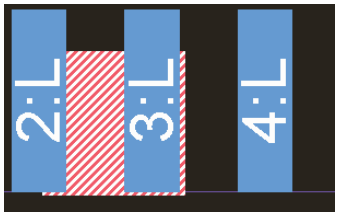
Gate	
Pin Type	Output
Pin Type	Output
Pin Type	Input
Pin Type	Input
Pin Type	Input





Make Pin Type visible in Display Control - Parts Tab

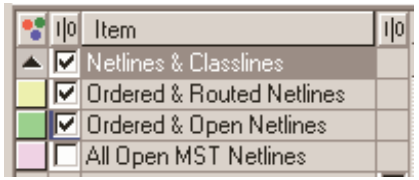




Routing Order — Behavior

- **Interactive Routing must follow the Custom order. Attempting to connect out of order causes a Stub Length violation.**
- **Automatic Routing will always follow the Custom order.**
- **Review Hazards does not have a Custom order check. Violations will be reported as a Stub Length violation.**
  - **How would you get a violation?**
    - **Set the Custom order after the net is routed. If this is done graphically, a prompt dialog will display.**

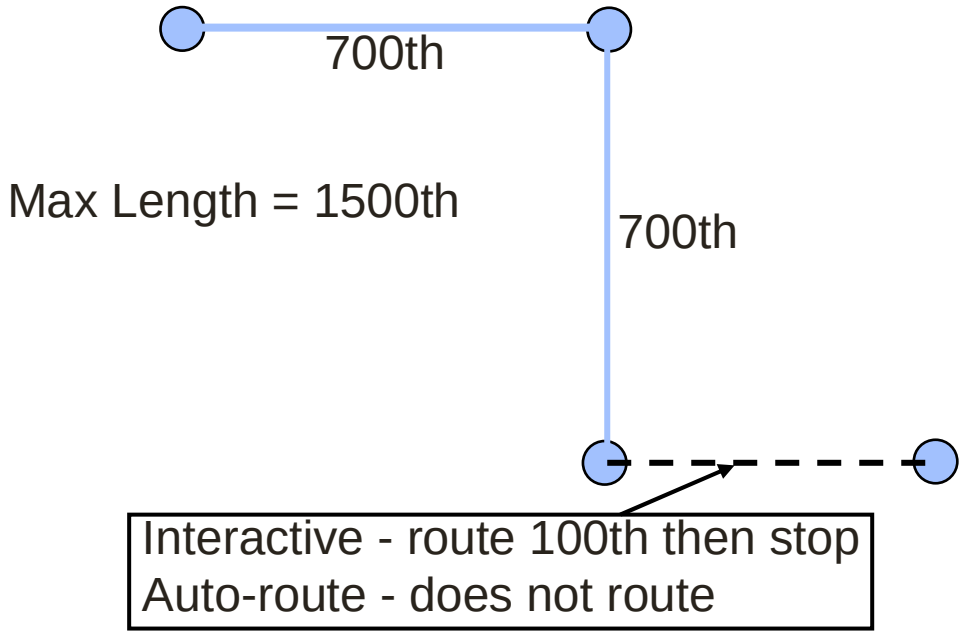
  - **Other issues — Custom ordered signals have netline visibility settings.**

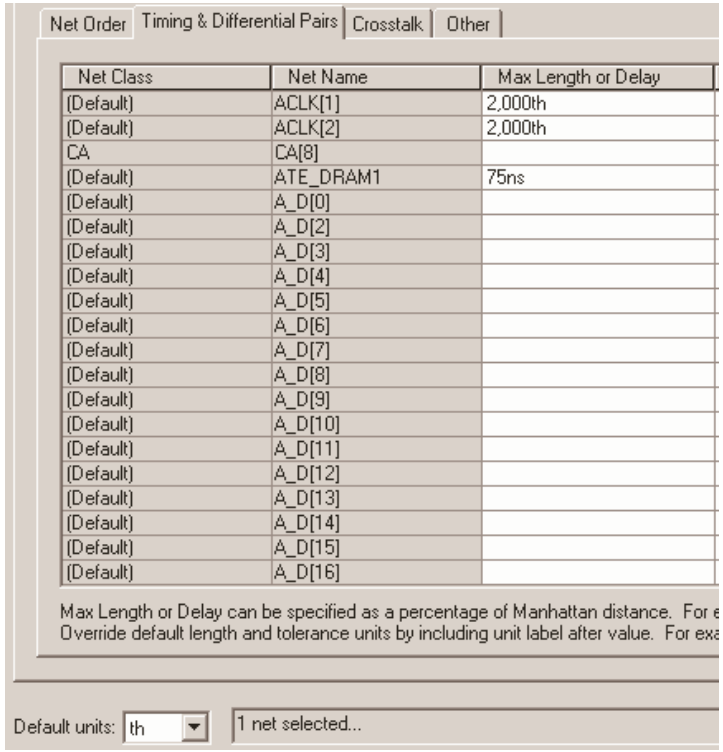


	Auto Router	Interactive	Editor Control	Hazard	Other Issues
Net Order	Constraint	Constraint based on Stub Length	No Direct Control Stub Length Override	No Direct Hazard Stub Length Violations	Must have Max Stub Length Must Custom Order for Delay Formulas Special Netlines Modify Netline Order Command Virtual and Guide Pins Pin Types – Source, Load, Terminator

Maximum Length

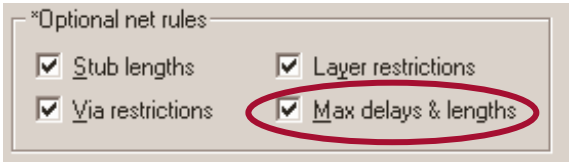
- **Signals are assigned a Maximum Length on the Net Properties dialog — Timing and Differential Pairs tab.**
  - **Select the signal**
  - **Enter the maximum length**
    - **If using other than the default units, enter the units**
    - **Length is for the entire net**



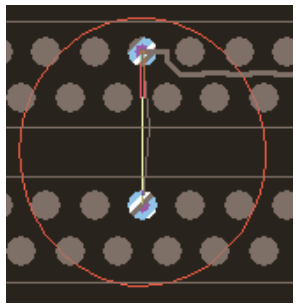


Maximum Length — Behavior

- **Interactive routing will not route beyond the Maximum Length**
  - **Editor Control — Route option will turn the constraint off.**



  - **While routing a net with a Maximum Length, a Max-Length_Ellipse dynamically displays the remaining available length.**



- **The Auto Router will not violate Maximum Length.**
- **Review Hazards has a check for Max Length violations.**
  - **Unrouted nets based on Manhattan**
  - **Routed based on actual length**

Net N...	Excess (th)	Net Class
ACLK[1]	414.67	(Default)
ACLK[2]	545	(Default)

Net N...	Max Len...	Manhatta...	Open (th)	Routed (th)
ACLK[2]	1,000	1,545	1,545	0

Net N...	Max Len...	Manhatta...	Open (th)	Routed (th)
ACLK[1]	900	1,250.5	0	1,314.67

	Auto Router	Interactive	Editor Control	Hazard	Other Issues
Max Length	Constraint	Constraint (Override)	Override	Max Length Hazard	

Matched Length

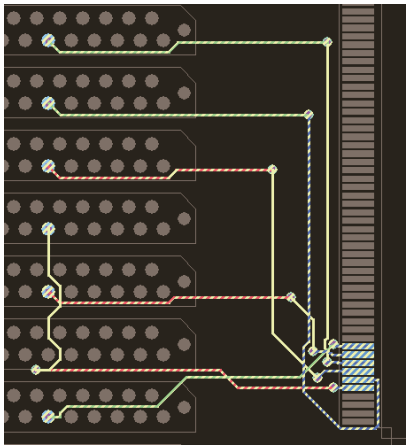
- **Signals are assigned a Matched Length Group on the Net Properties dialog — Timing and Differential Pairs tab.**
  - **Select the signal**
  - **Enter the Match Length Group number.**
    - **Different numbers set up different groups.**
  - **Enter the tolerance for the group.**
    - **All group members must have the same tolerance.**

CWE[2]-	2,000th	1	10th
CWE[3]-	2,000th	1	10th
CWE[4]-	2,000th	1	10th
CWE[5]-	2,000th	1	10th

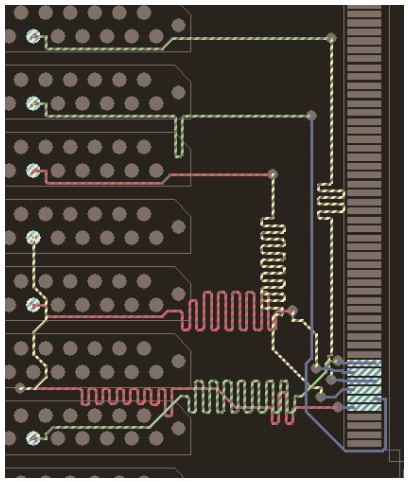
    - **If signals in a Matched Length Group have a Maximum Length, they must all be the same.**

Matched Length — Behavior

- **Interactive Routing**
  - Route all members of the Matched Length Group.
  - Select any segment of any of the group signals.
  - Press the Tune action key. 7 Tune



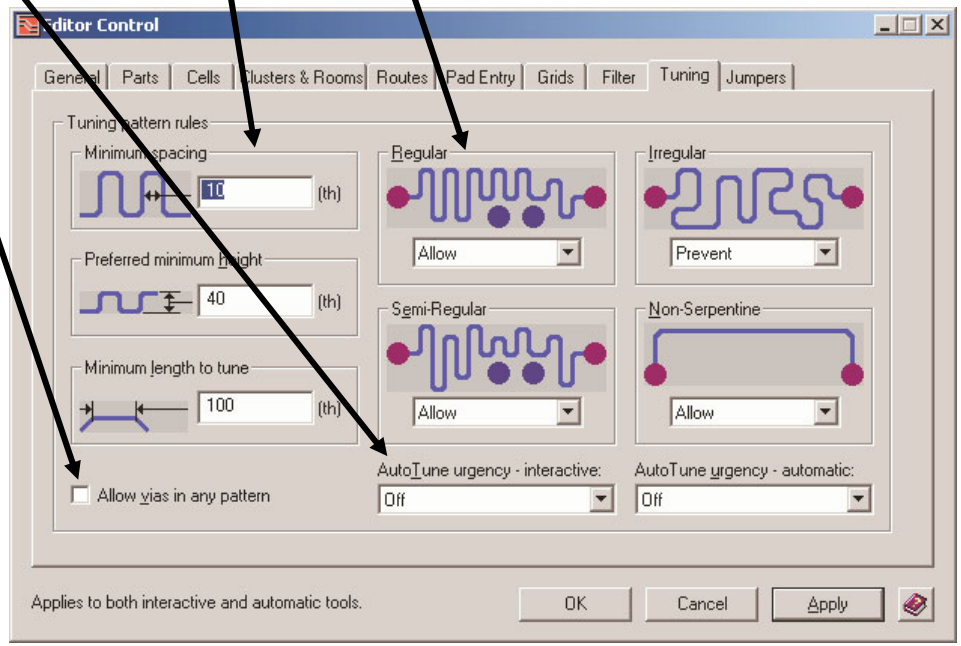
- **Automatic Routing**
  - Route all Members of the Matched Length Group
  - Run a Tune Pass.
    - Items to route includes an option for only working on nets that need tuning.
    - Tuned nets are set to Fix by default.
    - Tuning passes can be saved as a Tuning scheme.



Pass	Pass Type	Items to Route	Start	End	Now	Layers	Rte. Grid	Via Grid	Fix	Pause
☑	Fanout	Tuned Pin-Pairs	1	3		All Enabled	(Default)	(Default)	☐	☐
☑	Route	Tuned Pin-Pairs	1	3		All Enabled	(Default)	(Default)	☐	☐
☑	Tune	Tuned Pin-Pairs	1	1		All Enabled	(Default)	(Default)	☑	☐

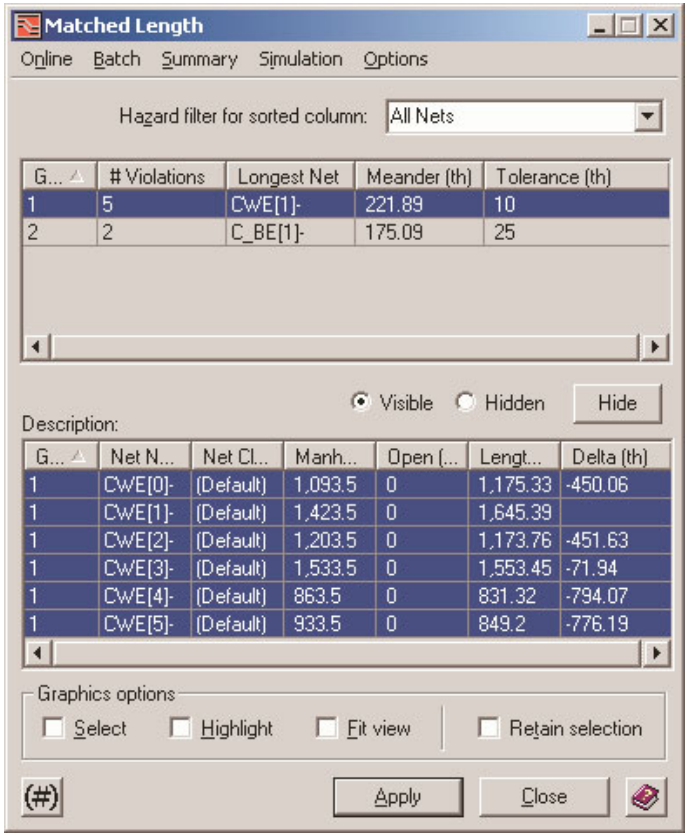
Tuning Controls

- **Tuning is controlled by settings on the Editor Control — Tuning tab.**
  - **Enable tuning patterns**
  - **Set serpentine pattern parameters**
  - **Set Auto-Tune urgency**
  - **Allow vias in patterns**



Matched Length — Behavior

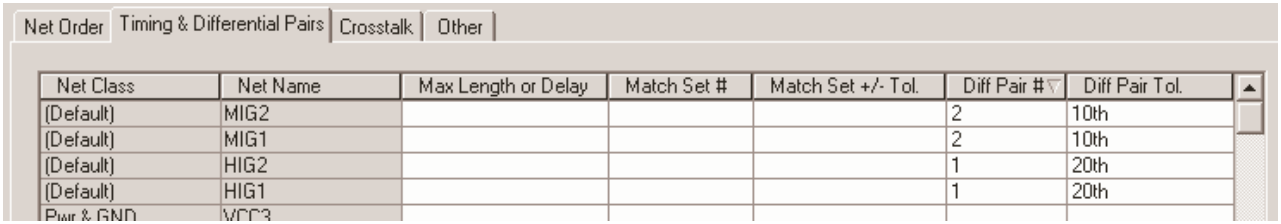
- **Review Hazards has a check for matched length violations.**



	Auto Router	Interactive	Editor Control	Hazard	Other Issues
Match Length	Route then Tune (Fix)	Route then Tune (Fix)	Tuning Tab Urgency	Match Length Hazard	Find Category Route, Tune, Lock

Differential Pairs

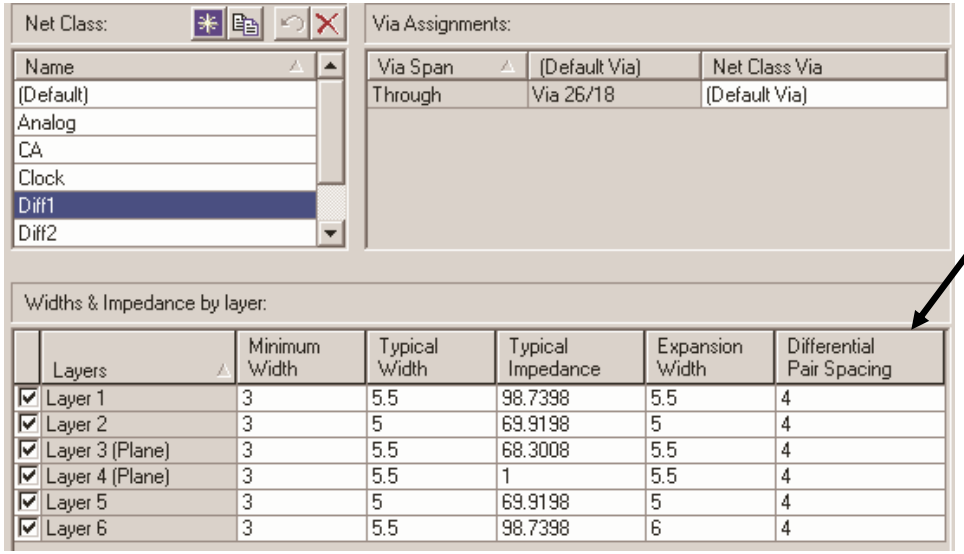
- **Signals are assigned to a Differential Pair on the Net Properties dialog — Timing and Differential Pairs tab.**
  - **Select the signal**
  - **Enter the Differential Pair Group number.**
    - **Different numbers set up different groups.**
    - **Only two signals can be assigned to each group.**



  - **Differential Pairs must be Custom Ordered. If you do not set the Custom Order, the system will automatically set it for you.**
  - **Tolerance sets the value for a Hazard report showing how close to the same length the Differential Pair nets are.**

Differential Pairs — Spacing

- **Differential Pair spacing is set in Net Classes and Clearances**

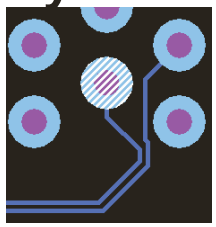


- **For Differential Pairs that require different spacing, assign them to different Net Classes.**

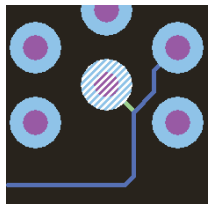
Diff1	HIG1
Diff1	HIG0
Diff2	MIG1
Diff2	MIG0

Differential Pairs — Layer Usage

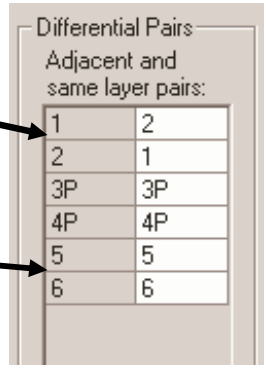
- **Differential Pairs can be routed in two ways:**
  - **Side by Side**



  - **Broad side (on adjacent layers)**

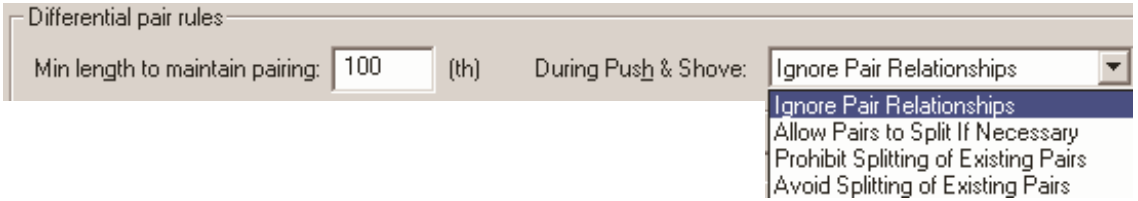


- **This setting is made in Editor Controls - General Tab.**
  - **Adjacent Layers set**
  - **Same Layer set**



Differential Pairs — Behavior

- **Interactive Routing**
  - **Select one of the Differential Pair nets, then Multiplow. - OR**
  - **Select one of the Differential Pair nets, then Route.**
    - **Control of Differential Pair routing and editing is set in Editor Control - Routes tab.**



- **Automatic Routing**
  - **The Auto-router will route with Differential Pair relationships.**
    - **Items to route includes an option for only working on Differential Pair nets.**
    - **Differential Pair passes can be saved as a Differential Pair scheme.**

Pass	Pass Type	Items to Route	Start	End	Now	Layers	Rte. Grid	Via Grid	Fix	Pause
☑	Fanout	Differential Pairs	1	3		All Enabled	(Default)	(Default)	☐	☐
☑	Route	Differential Pairs	1	3		All Enabled	(Default)	(Default)	☐	☐
☑	Tune	Differential Pairs	1	1		All Enabled	(Default)	(Default)	☐	☐

- **Review Hazards**
  - **There is not a hazard check for Differential Pairs.**

Differential Pairs — Matched Length

- If the members of a Differential Pair group must also be Matched Length:
  - Give them a Differential Pairs Tolerance
  - Check that Tolerance in Review Hazards
  - Manually adjust lengths at connections
- If multiple Differential Pairs Groups must be Matched Length:
  - Set them in the same Match Length Group.
  - Tune — the differential pair Groups will then tune to each other.

	Auto Router	Interactive	Editor Control	Hazard	Other Issues
Differential Pairs	Route Diff. Pairs No Via or Bias Diff. Pairs Net Type	Multi Plow or Hug Trace or F8 Route	Broadside vs. Edge Coupled Interactive Push and Shove Controls	Diff. Pairs Tolerance Hazard	Must be in Same Net Class Net Class setting for Spacing Must Be Custom Ordered

Maximum Crosstalk

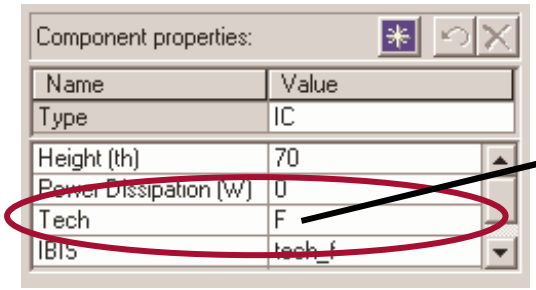
- **Signals are assigned a Maximum Crosstalk voltage on the Net Properties dialog — Crosstalk tab.**
  - **Select the victim signal**
  - **Enter the Maximum Crosstalk Value.**
    - **Default unit is Volts (V) — enter mV for millivolts.**

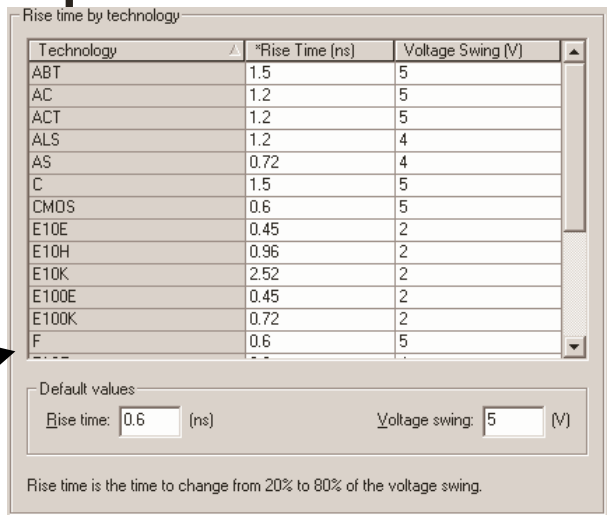
Net Class	Net Name	Max Crosstalk...
Multi Width	HIG4	150mV
(Default)	HIG3	150mV
(Default)	MP[1]	100mV
(Default)	MD[12]	100mV

- **Maximum Crosstalk is not a routing constraint.**
  - **Signals are routed and then violations are reported as hazards.**
  - **Hazards must be manually corrected.**

Maximum Crosstalk — Calculations

- **Maximum Crosstalk is estimated based on:**
  - **Space between the traces**
  - **Parallel distance of the trace runs**
  - **Rise time for the source pin on the aggressor net**
  - **Voltage swing for the source pin on the aggressor net**
- **Rise Time and Voltage Swing are set on Setup Parameters — Buried Resistors and Rise Time tab.**
- **Device Technology**
  - **From a Property in the PDB**

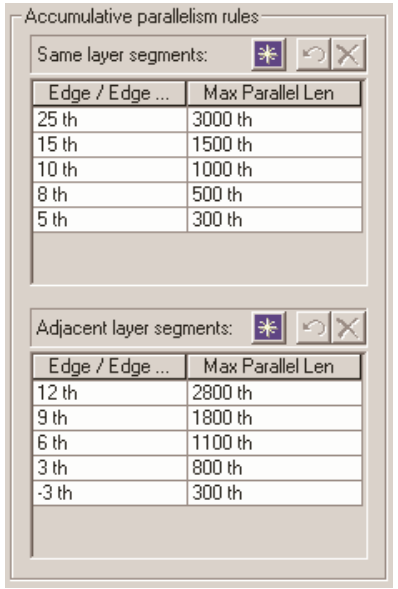




	Auto Router	Interactive	Editor Control	Hazard	Other Issues
Cross Talk	Not a Constraint	Not a Constraint	No Control	Estimated Crosstalk Hazard Cumulative Worst Case	Signal Type on source Derived from PDB – Type Property Rise Time/Voltage Swing on Setup Parameters

Parallelism

- **Signals are assigned a Max Parallelism value on the Net Properties dialog — Crosstalk tab.**
  - **Create the Rules Table**
    - **One table is for same layer parallelism**
    - **One table is for adjacent layer parallelism**
    - **Values are for trace edge to trace edge distance**
      - **Adjacent layers can have negative values, indicating edge overlap**
  - **Select the victim signal**
  - **Enter the Parallelism rule factor**
    - **Simplicity — multiply the factor by the Parallel length in the table to get the allowable length**
    - **Smaller factors are assigned to more sensitive nets**
- **Parallelism is not a routing constraint.**
  - **Signals are routed and then violations are reported as hazards.**
  - **Hazards can be automatically corrected.**



Net Name	Max Crosstalk (V)	Parallel Rules Factor
CA[8]		0.5
ATE_DRAM1		1
A_D[0]		1.2

Crosstalk and Parallelism Hazards

- **Hazards for Crosstalk and Parallelism are reported as "cumulative worse case".**
  - **All signal segments that are aggressors are considered.**
  - **The effect for all aggressor segments is totaled.**
  - **If the total effect is greater than the allowable value (Crosstalk Voltage of Parallelism Factor), then it is reported as a hazard.**

Net N...	Rule (mV)	Total (mV)	Worst N...	Worst S...	Net Class
HIG3	150.0000	293.7589	94.6085	66.1606	(Default)

Visible Hidden Hide

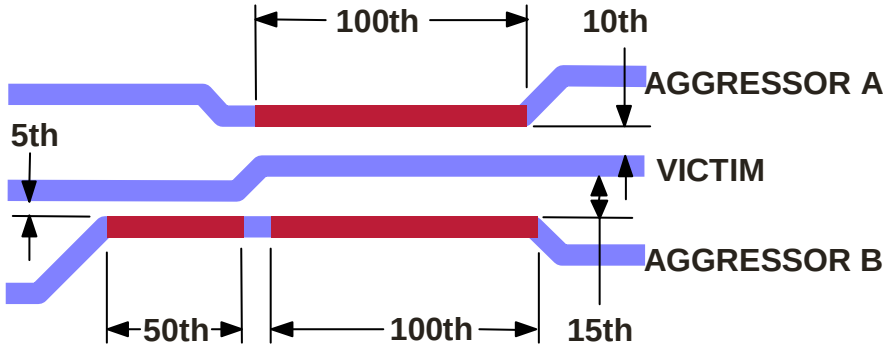
Description:

Victim Net	Aggressor Net	Crosstalk (mV)	Segment Length...	Spacing	Layer
HIG3	HIG2	26.5513	217	16.25	1
HIG3	HD[42]	6.9978	92.69	19	5
HIG3	HD[42]	66.1606	249.91	6	5
HIG3	HIG4	60.9413	215.44	6	6
HIG3	HIG4	28.8243	233.8	18	6
HIG3	HIG4	4.8429	48.51	21.5	6
HIG3	MAA[4]	44.5534	202.53	8	6

Crosstalk and Parallelism Example

Accumulative Parallelism Rules

Edge/Edge Gap	Max Parallel Length
20	500
15	300
10	150
5	100



MAXIMUM ALLOWABLE FACTOR FOR VICTIM = 1

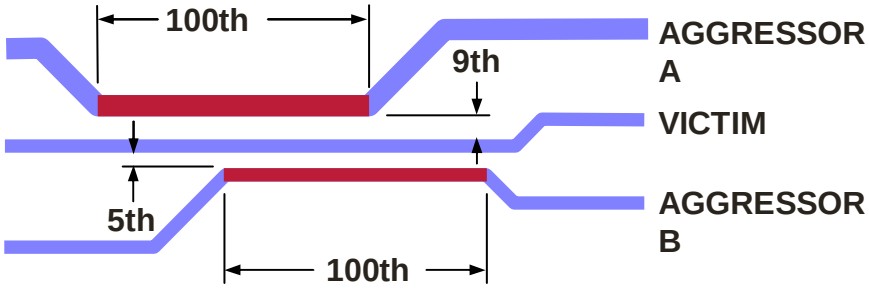
	GAP	PARALLEL DISTANCE
A	10th	100th
B	5th	50th
	15th	100th

ACCUMULATIVE PARALLELISM				
DISTANCE	/	MAX LENGTH	=	FACTOR
100th	/	150th	=	.66
50th	/	100th	=	.5
100th	/	300th	=	.33
TOTAL FACTOR				1.49

Crosstalk and Parallelism Example (Cont.)

Accumulative Parallelism Rules

Edge/Edge Gap	Max Parallel Length
11	700
9	500
7	350
5	200



MAXIMUM ALLOWABLE FACTOR FOR VICTIM = 0.65

	GAP	PARALLEL DISTANCE
A	9th	100th
B	5th	100th

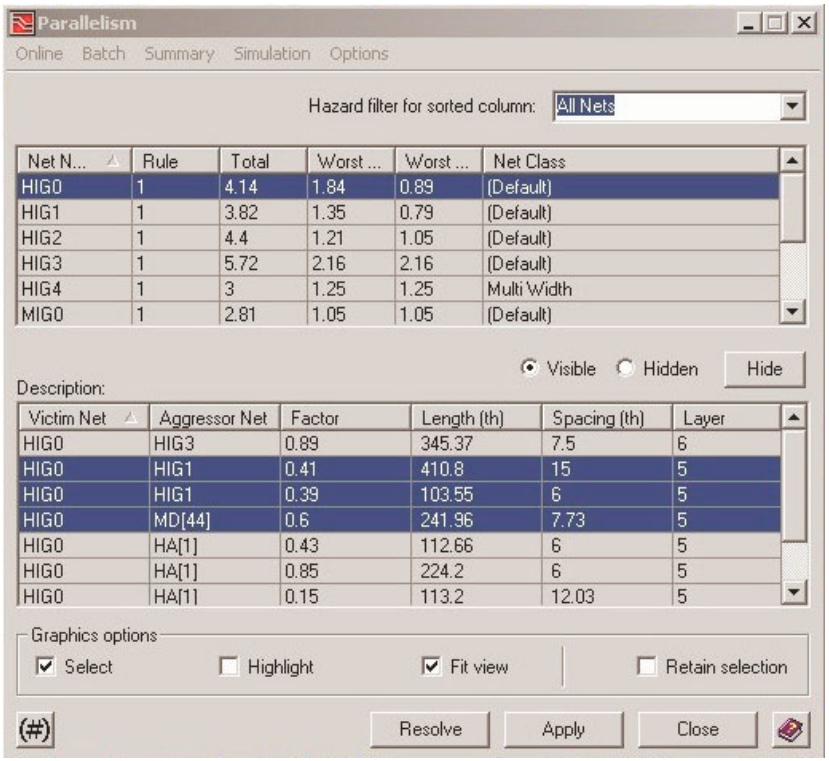
ACCUMULATIVE PARALLELISM				
DISTANCE	/	MAX LENGTH	=	FACTOR
100th	/	500th	=	.2
100th	/	200th	=	.5
			TOTAL FACTOR	.7

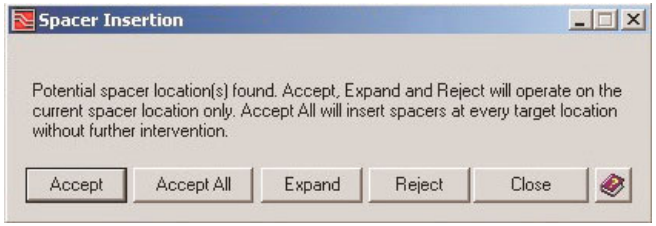
Crosstalk Hazards

- **Crosstalk hazards must be manually repaired.**
  - **Evaluate whether the cumulative hazard is really a problematic situation.**
  - **Sort descriptions based on worst hazard value.**
  - **Select the description line to correct — then turn on Graphic Options**
    - **Select - will select the victim net**
    - **Highlight - will highlight the aggressor net**
    - **Fit View**
  - **Correct hazard by separating the victim and aggressor nets.**

Parallelism Hazards

- **Parallelism hazards can be automatically repaired.**
  - **Auto Router has a Tune Crosstalk pass that will correct Parallelism.**
  - **Review Hazards for Parallelism has an automatic solution capability.**
    - **Select the description line(s) to correct.**
    - **Click Resolve**
    - **As solutions are found, a dialog prompts for options.**
  - **Resolution is by inserting "Spacers" between offending traces.**

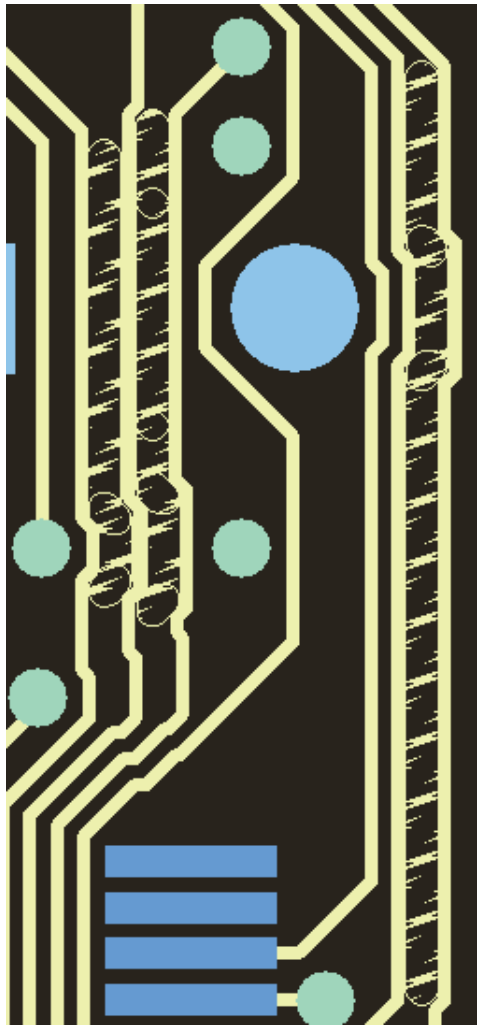




	Auto Router	Interactive	Editor Control	Hazard	Other Issues
Parallelism	Not a Constraint Tuning Pass for Spacers	Not a Constraint	No Control	Parallelism Hazard Cumulative Worst Case Interactive Spacer Insertion	

Parallelism Hazards — Spacers

- **Spacers are specialized graphics that are inserted between traces that cause Parallelism violations.**
  - **Spacer visibility can be controlled on the Layer tab of Display Control.**
  - **Spacers can be selected in Route or Draw mode.**
  - **Spacers report values in the Status Bar.**
  - **Spacers can be selected using Edit > Add to Select List.**
  - **Spacers can be pushed and shoved by Plow routing or Auto Routing routines.**

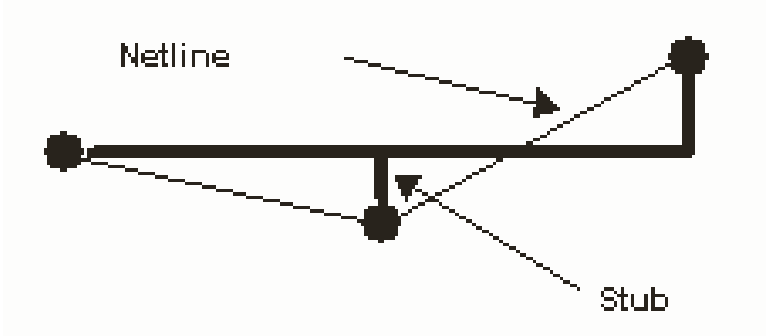


Stub Length

- **Signals are assigned a Max Stub Length on the Net Properties dialog — Other tab.**
  - **Select the signal**
  - **Enter the Stub Length value**
    - **All Chained and Custom net ordered signals are assigned a default Stub Length of 300 th.**

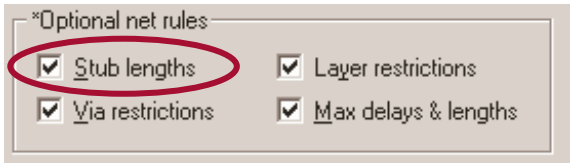
Net Name	Max Stub L...
RCLK[2]R	300th
RCLK[2]	100th
RCLK[1]R	300th
RCLK[1]	100th
RCLK[0]R	300th
RCLK[0]	100th

    - **A Stub is defined as an area where multiple netline connections share the same copper.**

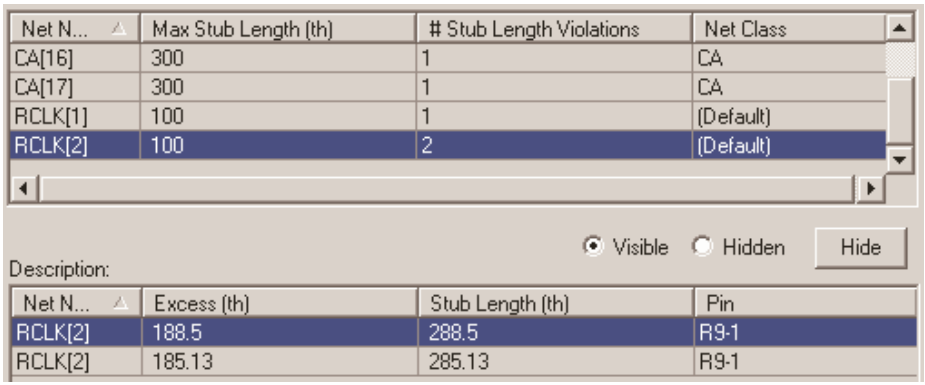


Stub Length — Behavior

- **Interactive routing will not allow stubbing beyond the Maximum Stub Length.**
  - **Editor Control — Route option will turn the constraint off.**



  - **The Auto Router will not violate Maximum Stub Length.**
  - **Review Hazards has a check for Max Stub Length violations.**



	Auto Router	Interactive	Editor Control	Hazard	Other Issues
Max Stub Length	Constraint	Constraint	Override	Max Stub Length Hazard	Route Order Violations Report as a Stub Length Hazard

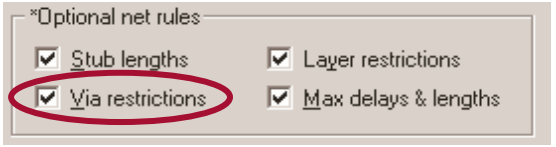
Maximum Vias

- **Signals are assigned a Maximum Via Count on the Net Properties dialog — Other tab.**
  - **Select the signal**
  - **Enter the Maximum number of Vias**

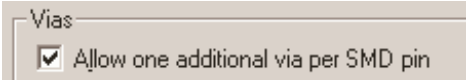
Net Name	Max Stub Length	Max ...	# Pins on Net
MIG1	50th	2	3
EOL		2	3

Maximum Vias — Behavior

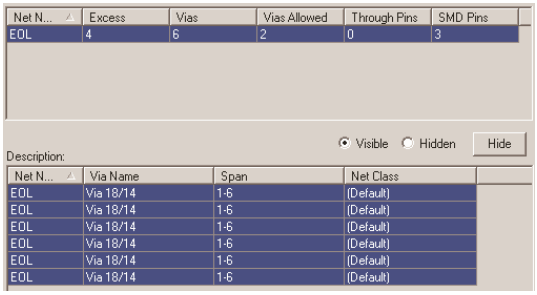
- **Interactive routing will not allow more vias than the Maximum Via Count.**
  - **Editor Control - Route option will turn the constraint off.**



  - **The Auto Router will not violate Maximum Via Count.**
  - **Both interactive and Auto-Routing can add an additional via per SMD pin if that is enabled in Editor Control - Routes Tab.**



  - **Review Hazards has a check for Max Via Count violations.**



	Auto Router	Interactive	Editor Control	Hazard	Other Issues
Max Vias	Constraint	Constraint	Override Allow Additional Via for SMD Pins	Max Vias Hazard	

Supply Voltage

- **Signals are assigned a Voltage on the Net Properties dialog — Other tab.**
  - **Select the signal**
  - **Enter the Supply Voltage**

Net Name	Max Stub Length	Max Vias	# Pins on Net	Supply Voltag...
VCC3			20	5V
VCC			61	5V
GND			118	0V

- **Signals with Supply Voltages assigned will not be aggressors during Crosstalk and Parallelism calculations.**

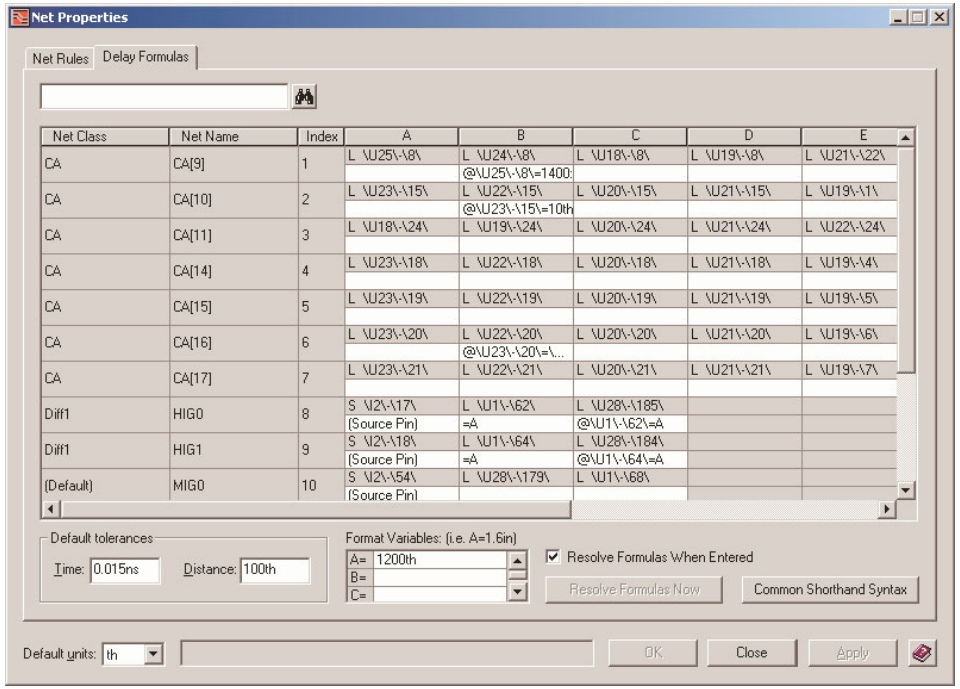
- **Supply Voltages are used during Signal Analyzer calculations.**

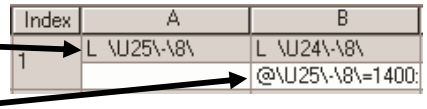
Delay Formulas

- **General Notes**
  - **While other Net Property functions operate on the entire net, Delay Formulas set pin to pin delays.**
  - **Only nets that have a Custom order can be assigned Delay Formulas.**
  - **It is helpful to have Source pins identified in Delay Formula operations.**
  - **Formulas can use operators (+ - < > =)**
  - **Formulas have tolerances. The default tolerance can be set and used, or overrides can be written into individual formulas (+/-N +N/-N N:N)**
  - **Default units for Delay Formulas can be used or units can be specified in the formula. (ps, ns, in, th, mm, um)**
  - **Formulas can be entered in shorthand syntax, then expanded to Ref-pin syntax (@D13=2000th --- @\R2\-\2\=2000th)**
  - **Formulas can include numeric values, Variables or references to other cells.**

Delay Formulas (Cont.)

- **Delay formulas are entered in a Spread Sheet like format.**
  - **Cells are referenced by row and column addresses.**



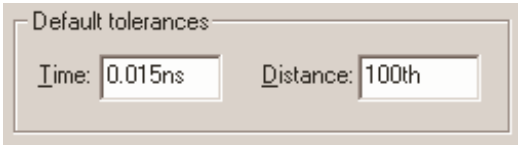


- **Upper field shows the ref-pin for the cell.**
- **Lower field is for entry of the formula for that pin.**

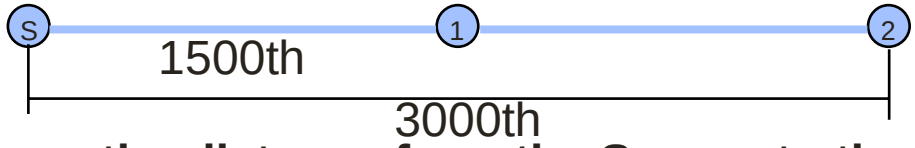
Delay Formulas — Source and Cell References

- **Example Formulas**

HIG0	8	S \I2\-\17\	L \U1\-\62\	L \U28\-\185\
		(Source Pin)	=1500th	=3000th
HIG1	9	S \I2\-\18\	L \U1\-\64\	L \U28\-\184\
		(Source Pin)	=B8	=C8



- **If only an equal sign (=) is used, the formula is "from" the right most source pin.**
  - **For HIG0 — the formula says that the distance from the Source (\I2\-\17\ ) to the first load pin (\U1\-\62\ ) is 1500 th. The distance from the Source pin to the second load pin is 3000 th. (Plus or minus the default tolerance.)**

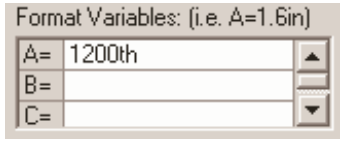


  - **For HIG1 — the formula says the distance from the Source to the first load pin is the same as the routed distance from HIG0's Source to the first load pin (plus or minus the default tolerance).**
    - **Be aware of additive tolerances — in this case the distance to HIG0 first load could be 1400th:1600th — meaning the distance for HIG1 first load could be 1300th:1700th.**

Delay Formulas — Non-Source “from” and Variables

- **Example Formulas**

HIG0	8	S \I2\-\17\	L \U1\-\62\	L \U28\-\185\
		(Source Pin)	=A	@B8=A
HIG1	9	S \I2\-\18\	L \U1\-\64\	L \U28\-\184\
		(Source Pin)	=A	@B9=A



  - **Use the “@” sign plus a cell reference to designate a non-source “from” pin. For HIG0, the second load pin formula is “from” the first load pin — B8.**
    - **If nets do not have a source pin, all formulas must use an “@” reference to designate the “from” pin for the formula.**
  - **Variable values are set in the variable table. Variables are useful for commonly used values or for values that may be changed.**

Delay Formulas — Examples

- **Example Formulas — Non-Default Tolerances**

HIG0	8	S \I2\-\17\	L \U1\-\62\	L \U28\-\185\
		(Source Pin)	=1200th +/-25th	@B8=100th +50/-25th
HIG1	9	S \I2\-\18\	L \U1\-\64\	L \U28\-\184\
		(Source Pin)	=1200:1300th	@B9=A

- **Example Formulas — Using Operands**

HIG0	8	S \I2\-\17\	L \U1\-\62\	L \U28\-\185\
		(Source Pin)		>3000th
HIG1	9	S \I2\-\18\	L \U1\-\64\	L \U28\-\184\
		(Source Pin)		<3000th
MIG0	10	S \I2\-\54\	L \U28\-\179\	L \U1\-\68\
		(Source Pin)	=1200th	@B10=1400th
MIG1	11	S \I2\-\71\	L \U28\-\178\	L \U1\-\69\
		(Source Pin)	=B10+500th	>C8+C9

  - **HIG0 must be greater than 3000 th total length.**
  - **HIG1 must be less than 3000 th total length.**
  - **MIG1 to the first load pin must be 500 th longer than the distance to the first load pin on MIG0.**
  - **The total length of MIG1 must be longer that the combined length of HIG0 and HIG1.**

Delay Formulas — Behavior

- **Interactive Routing — Route then Tune.**
- **Auto Routing — Route then Tune.**
- **Review Hazards**
  - **Gives information in multiple formats.**

Description:

	Net N...	Excess ...	Equivalent Dist...	Formula Location	Formula	Net-based Formula	Expanded Formula	Numerical Formula	Computed Formula
6	HIG1	0.4190ns	2,439.88	U28-184	@\U1\-\64\=	HIG1=HIG0	U28-184@U1-64=U28	0.2618ns=0.695803ns	0.2618ns=0.680803:0.710803ns
6	HIG0	357.56		U1-62	=2000th	HIG0=2000th	U1-62@I2-17=2000th	2457.56th=2000th	2457.56th=1900:2100th !!!
6	HIG0	1,096.69		U28-185	@\U1\-\62\=27(	HIG0=2700th	U28-185@U1-62=270(	1503.31th=2700th	1503.31th=2600:2800th

  - **If formulas can not be resolved, the Computed Formula will be followed by 3 exclamation points (!!!).**
  - **Formulas that are derived from other net references will be expressed using delay (ns) units.**
    - **Make sure the Layer Stackup is set correctly for delay calculations.**
  - **Hazards can be checked prior to routing.**

Delay Formulas (Cont.)

- **Delay formulas can be used instead of Max Length.**

MIG1	11	S \I2\-\71\	L \U28\-\178\	L \U1\-\69\
		(Source Pin)		<3500th

  - **Max Length will not route over the length. Delay Formulas will, and then report the Hazard.**
- **Delay formulas is the only way to specify a Min Length.**

MIG1	11	S \I2\-\71\	L \U28\-\178\	L \U1\-\69\
		(Source Pin)		>3500th

- **Tuning — when tuning signals, a log file is created called TuneLog.txt. It contains formulas that could not be tuned.**

```
*** Appended errors for tuning run: 1

* Tuning selected sets

No automatic solution possible in Set #6:
U1-62 = 2000th   in net HIG0
U1-64 = U1-62   in net HIG1
U28-185@U1-62 = 2700th   in net HIG0
U28-184@U1-64 = U28-185   in net HIG1
```

	Auto Router	Interactive	Editor Control	Hazard	Other Issues
Delay Formulas	Route then Tune (Fix) Route then Report	Route then Tune (Fix) Route then Report	Tuning Tab Urgency	Delay Formula Hazard	Nets Must Be Custom Ordered

Signal Integrity Routing

- Check Length and Delay Hazards before routing.
  - Are any formulas unresolved because of placement?
- Fanout entire board.
  - Routing could block fanouts from pins.
- Route Critical nets
  - Differential Pairs — manual or automatic (setup a scheme).
  - Tuned Nets — manual or automatic (setup a scheme).
- Check and repair Hazards on Critical nets.
- Lock Critical Nets.
  - If the percentage of critical nets is high, consider not Locking nets but instead setting the AutoTune Urgency in Editor Control - Tuning tab.
- Back up the Database.
- Finish routing.

Lab Preview

- **This Module has 4 Labs.**
  - **Lab 1 — Differential Pairs**
    - You will be setting and routing 2 sets of differential Pairs.
  - **Lab 2 — Matched Length and Tuning**
    - You will be setting up and Tuning a set of Match Length nets.
  - **Lab 3 — Virtual Pins**
    - You will be adding virtual pins and ordering three nets.
  - **Lab 3 — Delay Formulas**
    - You will be Custom Ordering nets, adding Delay Formulas to those nets and then routing and Tuning to meet the tolerances.
  - **Lab 4 — Crosstalk and Parallelism**
    - You will be setting Crosstalk and Parallelism rules, and then solving to those rules.

Advanced Expedition PCB

Appendix A

Team PCB

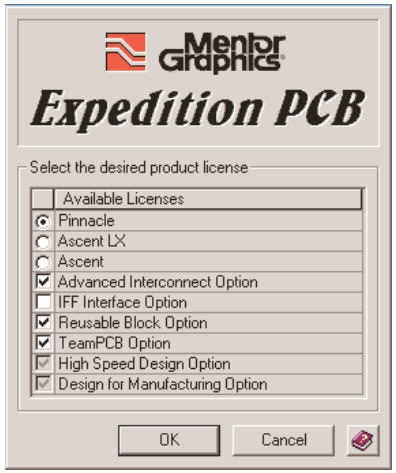
Objectives

Upon completion of this lesson and lab, you will be able to:

- **Describe the Use and Functionality of Team PCB.**
- **Explain the Team PCB Design Flow.**
- **Build Team PCB Reserved Areas.**
- **Setup for Initial Placement in Team PCB.**
- **Split a Team PCB Design Into Partitions.**
- **Perform Team PCB Placement Activities**
- **route in a Team PCB Partition**
- **Use Graphic Commands in Team PCB Partitions**
- **Do Team PCB Peer Updates**
- **Join Edited Partitions to the Original Design**
- **Manage a Team PCB Project**

What is Team PCB

- **A design strategy that allows multiple designers to work on a design simultaneously with automatic and interactive tools.**
  - **Provided through “split” and “join” processes**
  - **Designs are broken into user defined partitions to allow editing for different design teams**



- **Licensing**
  - **Team PCB is a licensed module**
  - **Partition designs can only be opened using a Team PCB license**
  - **Team PCB only with Pinnacle or Ascent LX**
  - **Team PCB uses the Team PCB license AND an Expedition PCB license.**

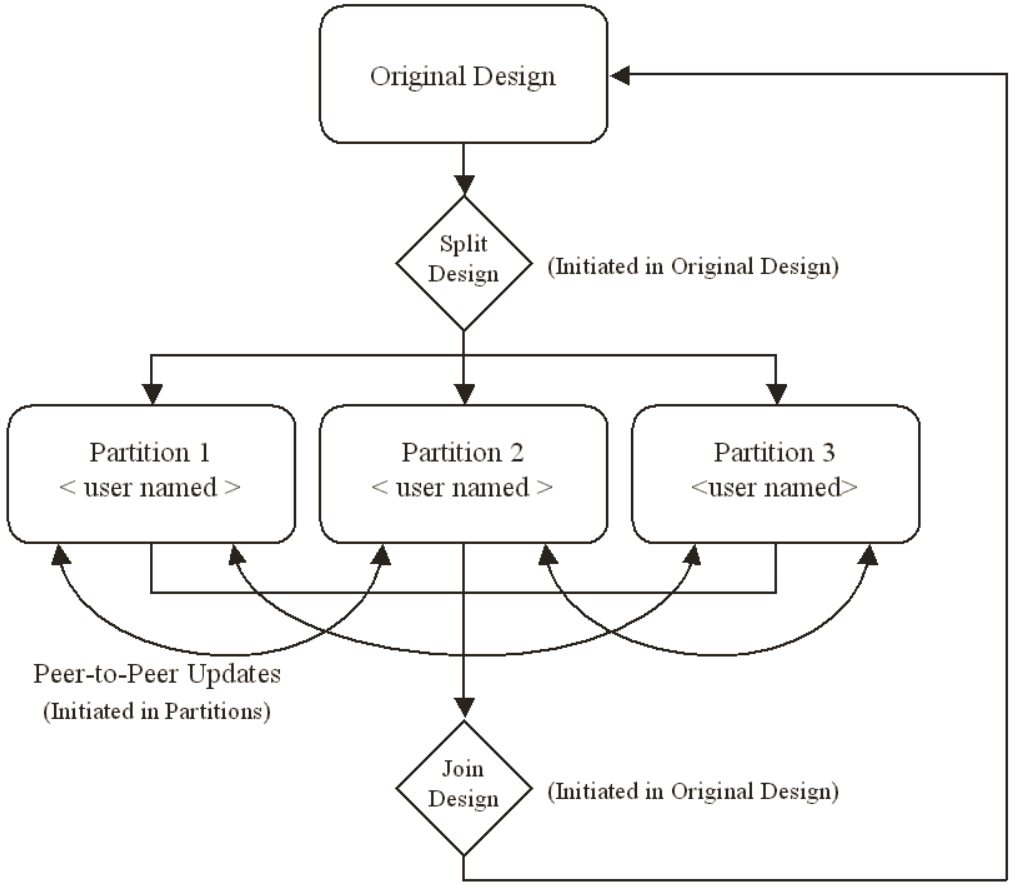
Terminology

- **Original Design**
  - The design before any splitting has occurred
  - Reserved Areas and Placement Authorization are done in the Original Design
- **Reserved Area**
  - A closed polygon that defines the area for a team partition
  - There can, and will probably be multiple Reserved Areas in a Team PCB design
- **Partition**
  - The design database used for a design team
  - There will be a Partition design for each Reserved Area
  - In the Partition, only the area of the board in the Reserved Area is active
- **Unreserved Area**
  - A special Partition containing all of the Original Design data.
  - Uneditable

Let's see how it works!!!

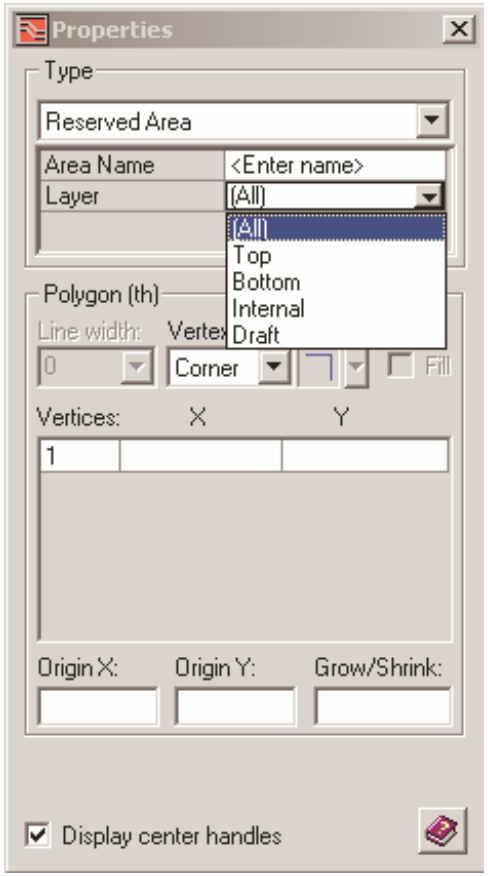
Workflow

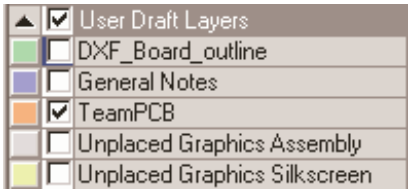
- Reserved Areas are defined in the Original Design
- Design is Split
- Each Partition is edited by the responsible team
  - Peer to peer updates can be done so one team can see what another team is doing
- Partitions are Joined back onto the Original Design



Reserved Areas

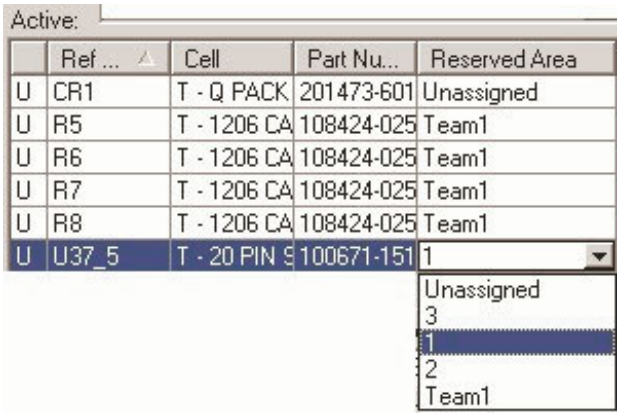
- Reserved Areas are drawn as a Polygon or Rectangle in Draw Mode
  - Type - Reserved Area
  - Supply a unique user defined name
    - No Spaces
  - Select an editable layer
  - Draw Area
- Reserved Areas may extend beyond Board Outline
- Reserved Areas may overlap - but
  - The smaller of the reserved areas will include the overlap area after the split
- Display of Reserved Areas is controlled by a User Defined layer - TeamPCB





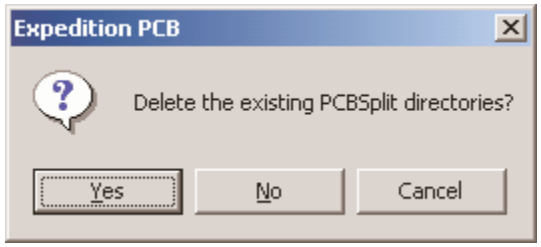
Initial Placement Preparation

- **All Placement could be done in the Original Design - or**
- **Initial Placement or Placement editing could be done in the Partitions**
  - **To setup for Initial Placement - in the Original Design**
    - **Create Reserved Areas**
    - **Place > Place Parts and Cells**
    - **Move Parts for Reserved Area to active table**
    - **Set the Reserved Area for the active Parts**



Split the Design

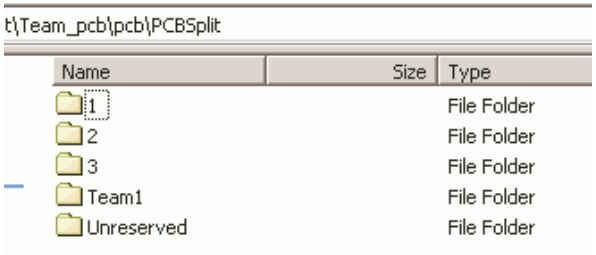
- **To Split the Original Design into the Partitions:**
  - **File > Split Design**
- **Will prompt to Save the Original Design if changes have not been saved**
- **Will Prompt for permission if the Original Design has been split previously**



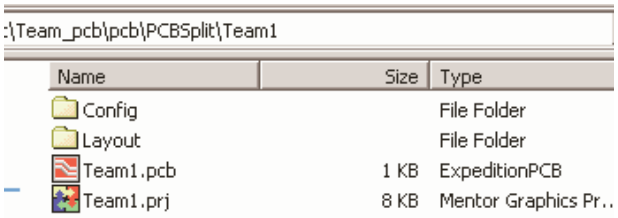
Split the Design (Cont.)

- After the Split, a new sub-folder is created in the PCB folder for the Original Design - “PCBSplit”

- Inside the “PCBSplit” sub-folder:
  - A folder for each Partition is created
  - An Unreserved Partition folder is created containing the Original Design as it was at the time of the Split
    - This Partition is uneditable



- Inside each partition folder is an Expedition PCB design



Opening the Partition

- **To open a Partition for editing, simply open the ".pcb" file in the Partition design folder**

- **Conditions:**
  - **All Parts that are totally or partially outside of the Reserved Area will be Locked**
  - **All Routing that is totally outside of the Reserved Area will be locked**
  - **All Routing that crosses the Reserved Area boundary will be locked outside of the boundary, but editable within**
  - **Netlines will display for all nets**
  - **graphics that are totally or partially outside of the reserved area are uneditable**
  - **THE UNLOCK COMMAND IS DISABLED (as are a number of other commands**
  - **You can only work in the Reserved Area**

Partition Placement

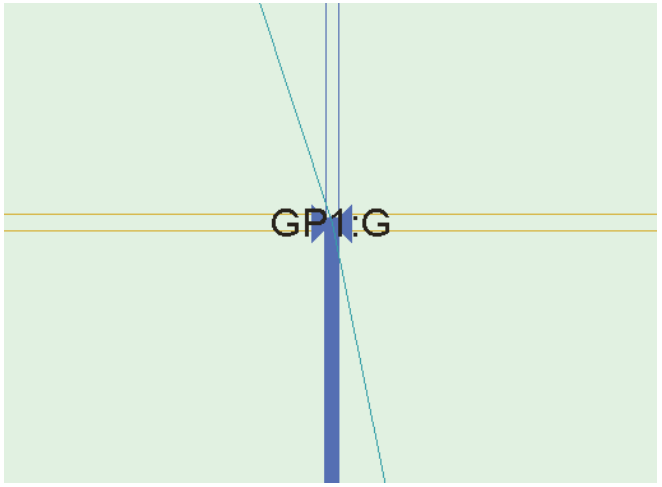
- **You can only initially place Parts that have been authorized for the Partition during work in the Original Design**
  - **Place > Place Parts and Cells**
  - **Only authorized Parts will display in the tables**
- **You can only unplace parts that are totally in the Partition Reserved Area**
- **You can only edit Part placement within the Partition Reserved Area**

Partition Routing

- Interconnects completely within a the Partition's Reserved Area can be totally routed using interactive or automatic commands
- Interconnects that cross the partition's Reserved Area boundary can be routed to the boundary and left dangling
- Traces within the Partition's Reserved Area can be edited
- Multiplow is available within the Partition's Reserved Area
- Teardrops can be added within the Partition's Reserved Area
- Test Points can be added within the Partition's Reserved Area
- Net Classes and Clearances can be changed in the Partition
  - Changes in Net Classes and Clearances WILL NOT propagate back to the Original Design
- Editor Control settings can be changed in the Partition
  - Changes in Editor Control WILL NOT propagate back to the Original Design

Partition Routing (Cont.)

- **Guide Pins can be located in the Original Design to facilitate Inter-Area connections.**
  - **Original Design**
    - **Modify Netline Order**
    - **Set Net to Custom Order**
    - **Place Guide Pin at the Center of the boundary between Areas**
  - **Remember - Guide Pins must be placed in the Original Design**
  - **Remember - the signal must be Custom Ordered to place Guide Pins**
  - **Remember - all pins on the net must be placed before the Modify Netline Order command can be used**

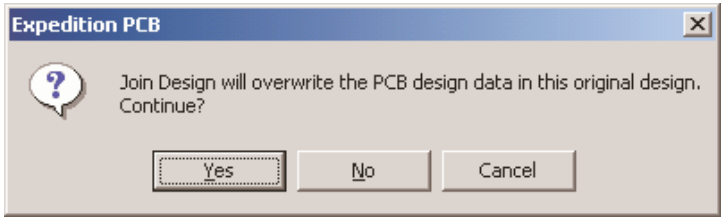


Partition Graphics

- **Drafting functions are enabled within the Partition's Reserved Area**
  - **Place Plane Shapes for Area Fills**
    - **Dynamic Area Fills is enabled**
  - **Only Draw Objects completely within the Partition's Reserved Area can be edited**
  - **New Draw Objects must be completely enclosed within the partition's Reserved Area**

Peer to Peer Updates

- **While working in a Partition, you can update your graphics to show other Partition's saved graphics**
  - **Save your own Partition**
    - **If not, your edits since the last save will be lost**



  - **File > Update From Other Partitions**
    - **You will be prompted for other Partition Graphics to update**

Joining Partitions

- **To join Partitions:**
  - **Have teams save each Partition**
  - **Issue File > Join Design**

  - **WARNING:**
    - **Join Design will restore the Unreserved Partition in order to perform the Join because join needs the initial Split environment to join to**
    - **Join always joins all Partitions - have them all saved and current before Join**
    - **WHILE TEAMS ARE EDITING THE PARTITIONS, DO NOT EDIT IN THE ORIGINAL DESIGN - THOSE EDITS WILL BE LOST DURING A JOIN**

Lab Preview

- **This Module has 3 Labs.**
  - **Lab 1 — Building Reserved Areas and Partitions**
    - **In this lab you will be setting up an Original Design for Team PCB. You will define the reserved areas, set some placement authorizations, and place some guide pins. You will then split the design into Partitions.**
  - **Lab 2 — Partition Editing**
    - **In this lab you will be editing the three Partitions from your Original Design.***
  - **Lab 3 — Joining Partitions**
    - **In this lab you will join the Partitions back to the Original Design.**

***There may be alternate instructions**

Advanced Expedition PCB

Appendix B

Report Writer

Objectives

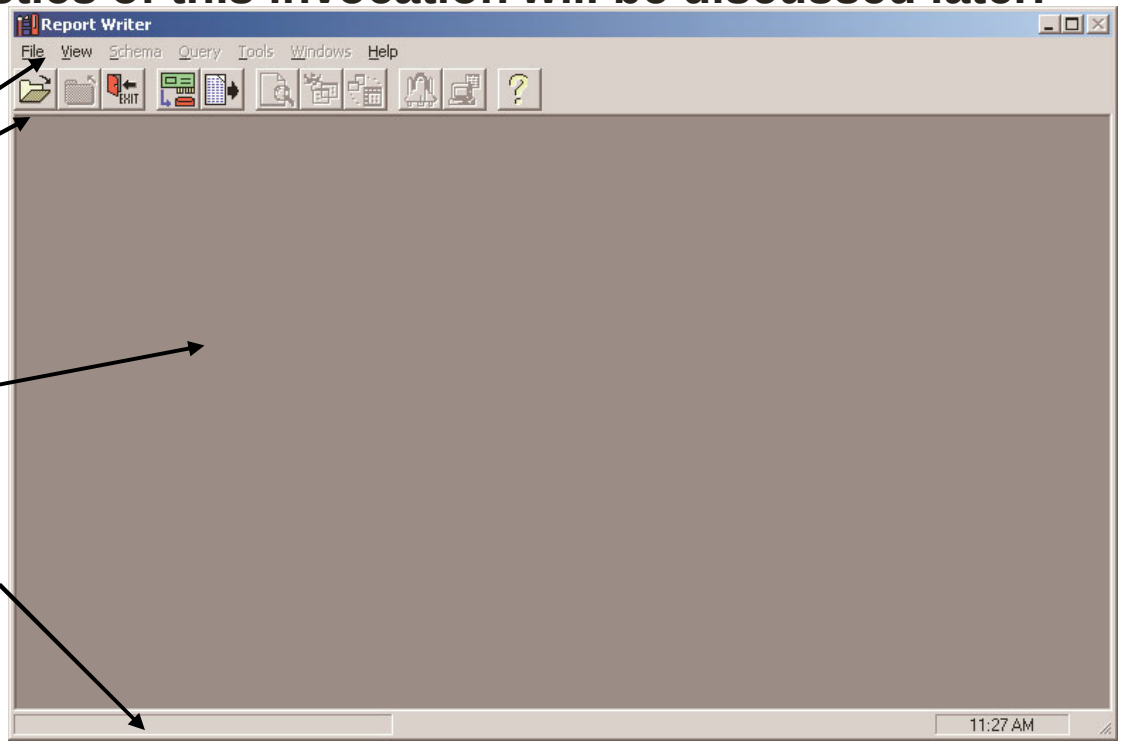
Upon completion of this lesson and lab, you will be able to:

- **Invoke the Report Writer**
- **Use the Report Writer Environment**
- **Understand the Report Writer Process**
- **Add and Use Report Writer Tools**
- **Use Report Writer Standard Reports**
- **Create Interactive Queries**
- **Save and re-run Queries**
- **Link Tables in Queries**
- **Do Cross Tab Queries**

Invoking the Report Writer

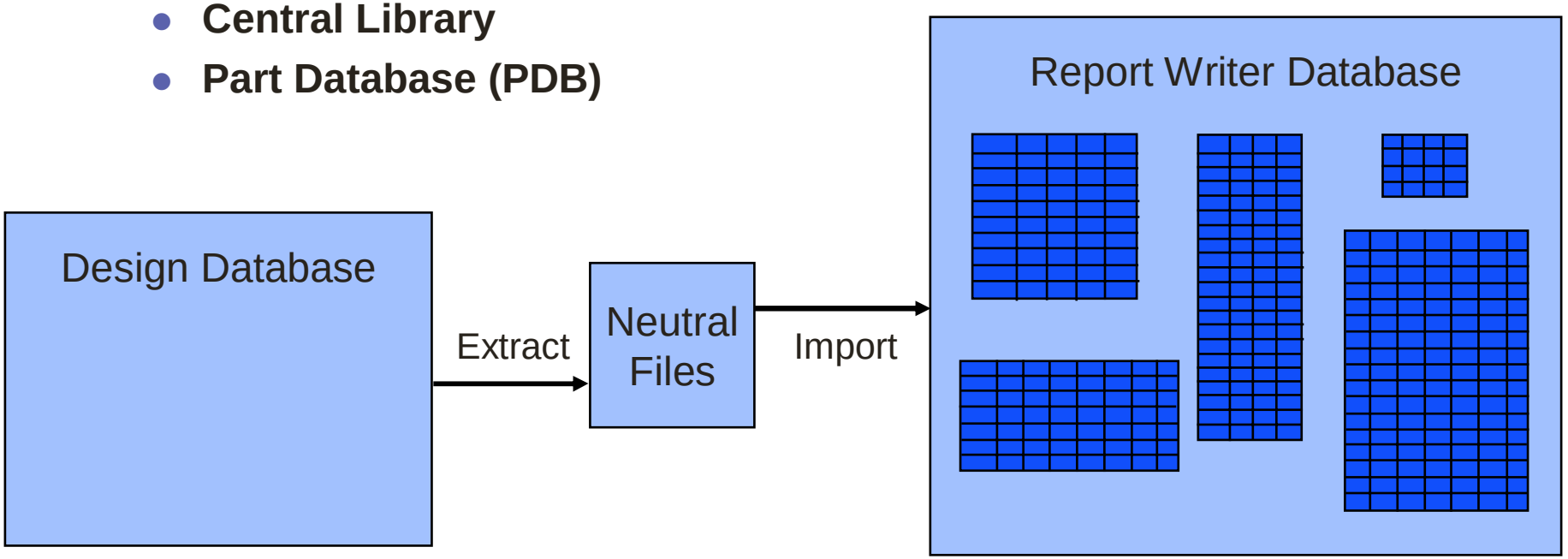
- Start > Programs > Mentor Graphics SDD > WG2004 > Report Writer >Report Writer
- Report Writer can also be  voked from inside Expedition PCB.
  - Output > Report Writer
  - Special characteristics of this invocation will be discussed later.

- Pull Down Menus
- Tool Bar
- Work Area
- Status/Prompt Area



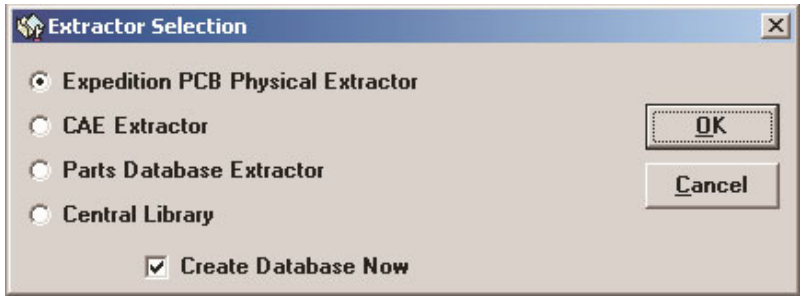
Report Writer Database

- **A Report Writer database is in an ACESS format.**
  - **Tables of information**
- **Data can come from:**
  - **Design Entry (CAE)**
  - **Expedition PCB**
    - **2 formats**
  - **Central Library**
  - **Part Database (PDB)**



Creating a Database

- File > Extract Data
  - Choose Data Type
  - Click on Apply
  - Displays a Browser
    - Browse to find the key file for the data type.

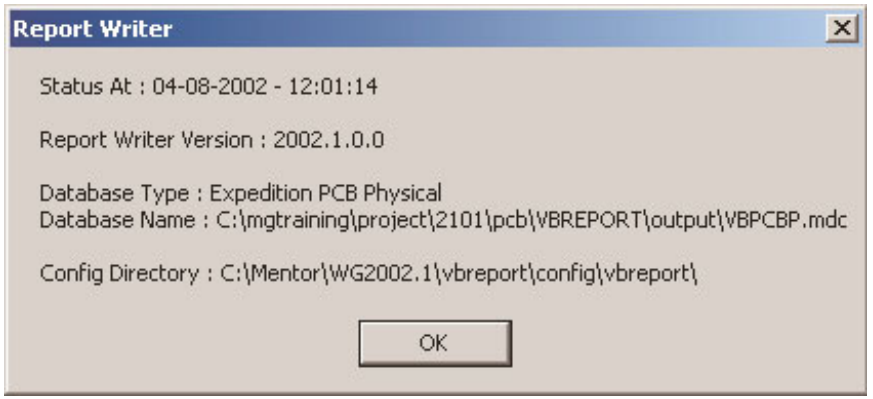


- File > Import Data
  - Choose Data Type
  - Click on Apply
  - Displays a Browser
    - Browse to find the files created by Extract.

- Most of the time, check “Create Database Now” to automatically run the Import after the Export.

File Commands

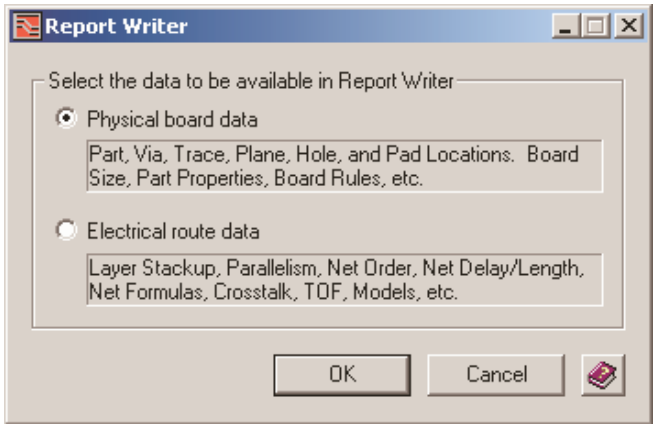
- File > Close Database
- File > Open Database
  - Displays a Browser
- File > Status
  - Shows current database type and location.



- Recent Menu
  - Lists last databases opened.

Invoke from Expedition PCB

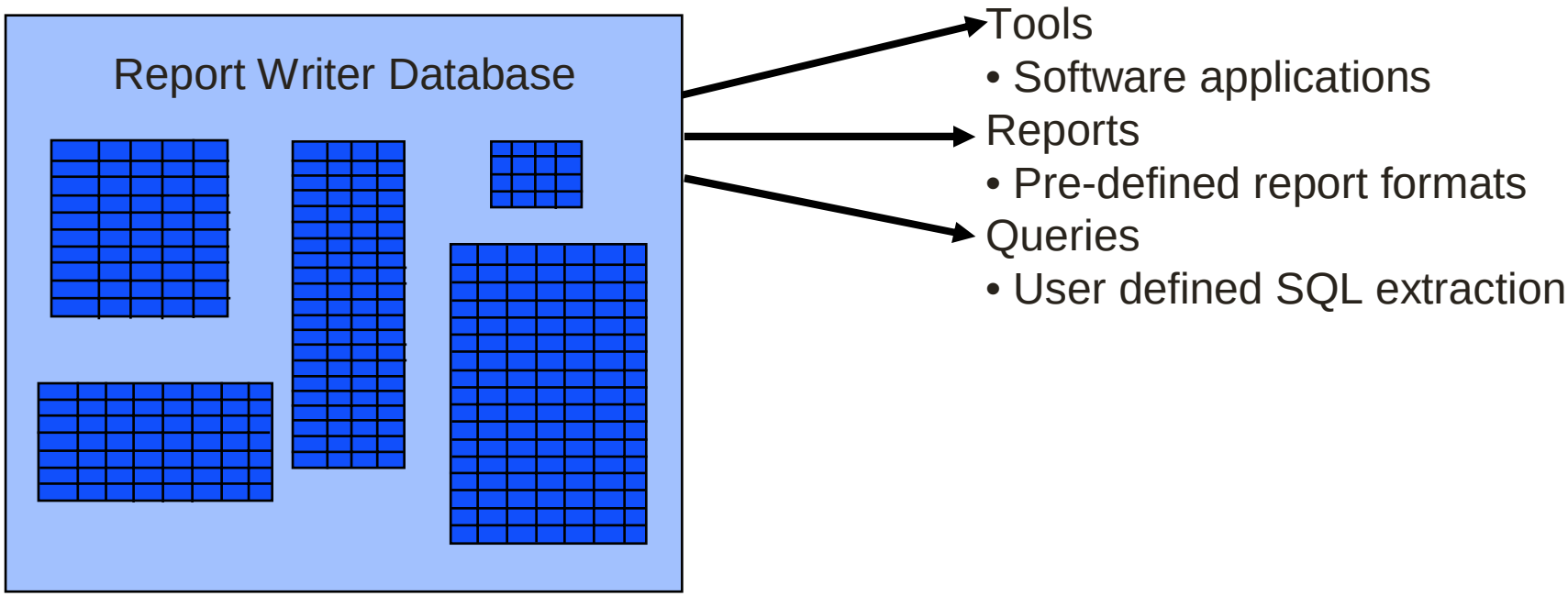
- **Inside Expedition PCB — Output > Report Writer**



  - **Option to produce a database with Physical Board data.**
    - **Default**
    - **Same data as if creating from inside Report Writer.**
  - **Option to produce a database with Electrical Route data.**
    - **Signal Integrity, Delay data**
    - **Only produced using Expedition PCB invocation of Report Writer.**
- **Command automatically invokes Report Writer.**
- **Command automatically Extracts and Imports data.**

Data Extraction from Report Writer

- **Once the database is created, you must extract data from the database in a meaningful format.**
- **This can be done in three ways**

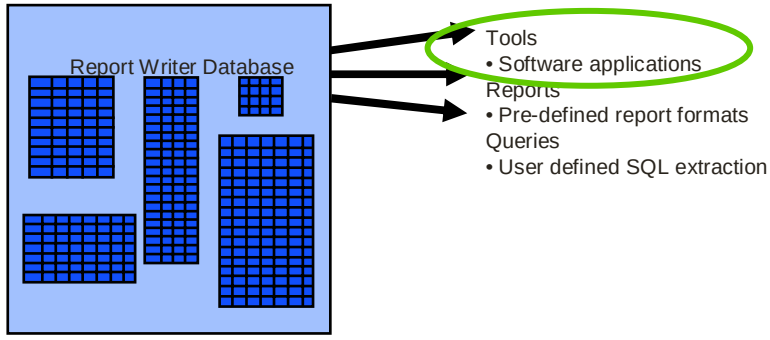


Tools

- **Tools are software applications that extract, add or format data from the database.**
  - **There are some which are supplied by Mentor Graphics:**
  - **Located at “<load directory>/vbreport/bin”**
    - **Expedition PCB**
      - **Expedition PCB Physical Tool**
      - **IPC-D-356**
      - **FabMaster (License Required)**
      - **C-Link (License Required)**
      - **HyperLynx (License Required)**
      - **Incases - Sultan (License Required)**
    - **Design Capture**
      - **Design Capture Tool**
      - **Reference Designator Tool**
    - **Part Database**
      - **Parts Database Tool**
    - **Central Library**
      - **Central Library Tool**

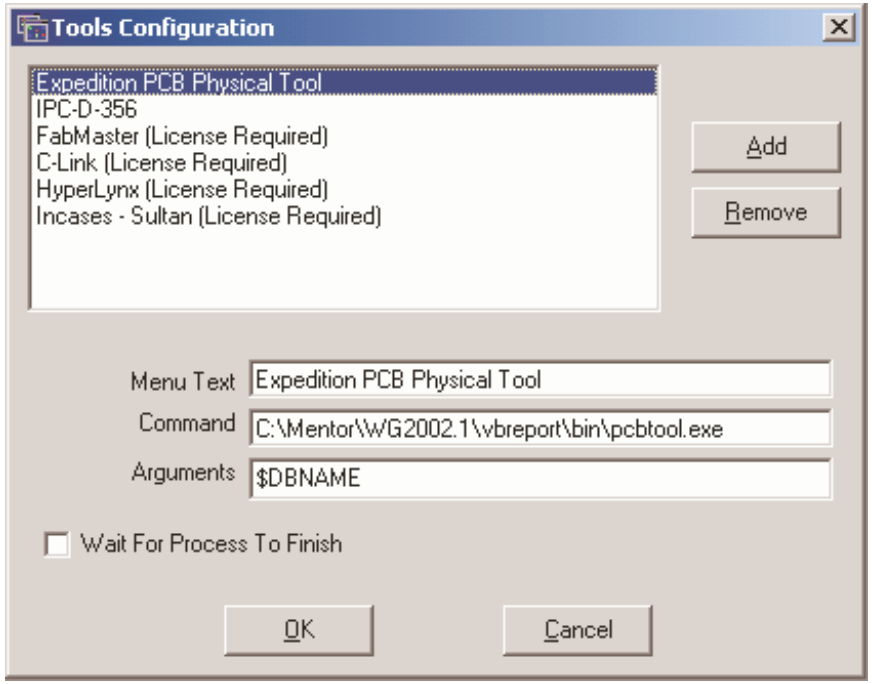
Default Load Directory:

C:\Mentor Graphics\2004\wg\win32



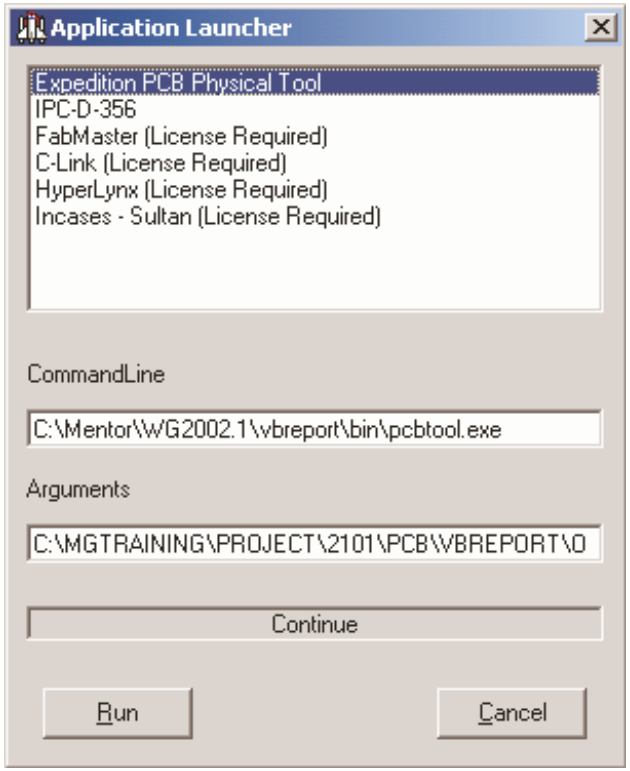
Configuring Tools

- **Tools>Configure Tools**
  - **Click on Add. Displays a browser to find the executable for the tool. Then:**
    - **Enter the text to appear on the menu.**
    - **Path to the Command executable**
    - **Arguments for the command.**
      - **The only recognized argument for Mentor supplied tools is $DBNAME, causing the executable to open the current database.**

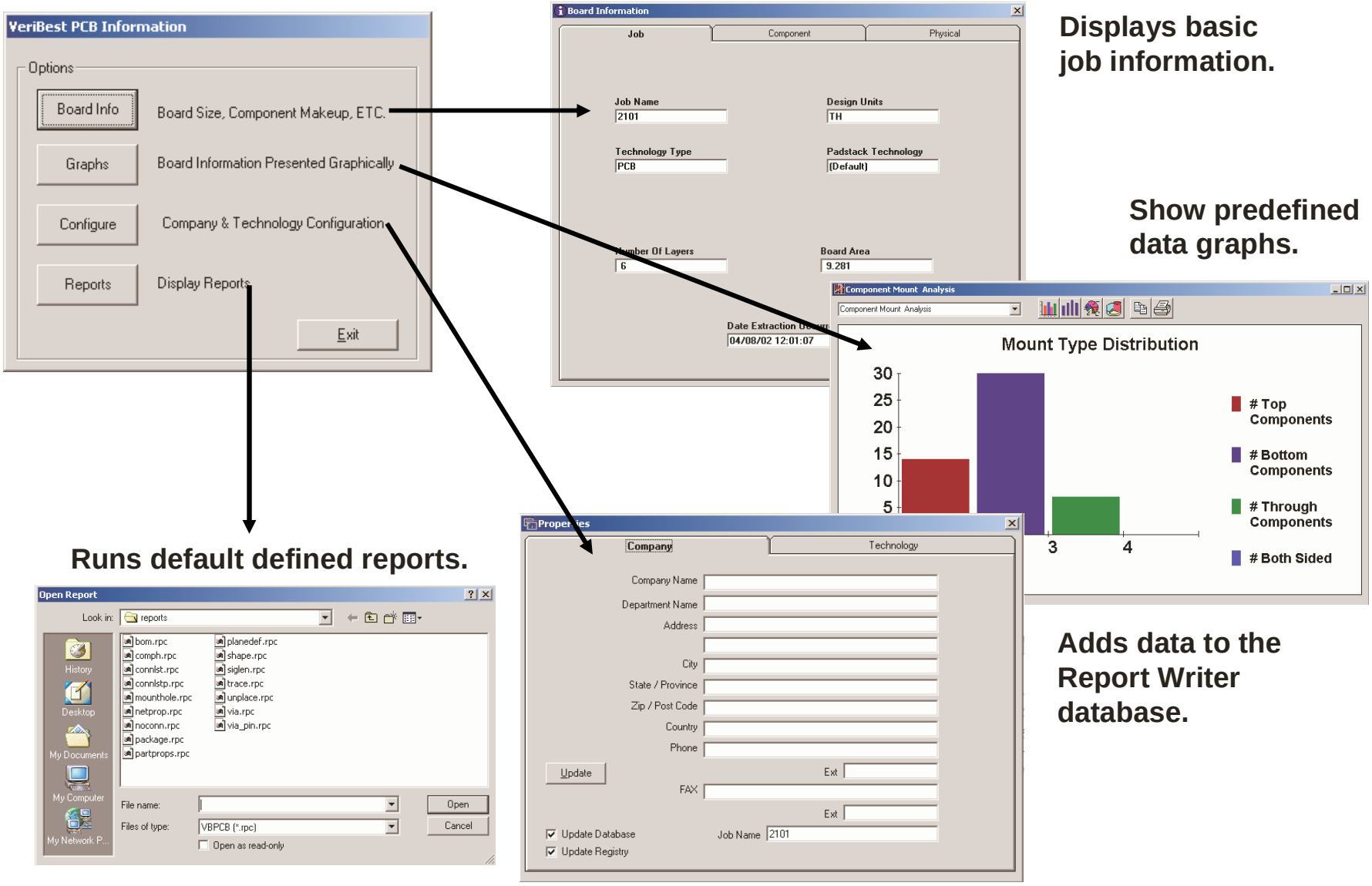


Running Tools

- **Tools > Launcher**
  - **Select the tool to run.**
  - **Click on Run.**



Expedition PCB Tools



Displays basic job information.

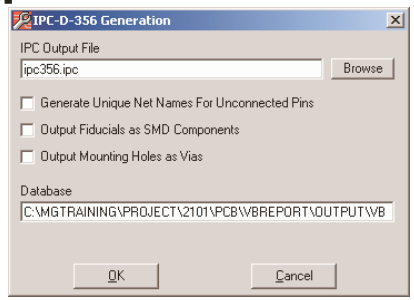
Show predefined data graphs.

Runs default defined reports.

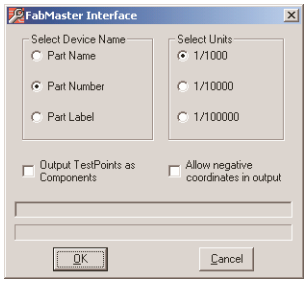
Adds data to the Report Writer database.

Other Expedition PCB Tools

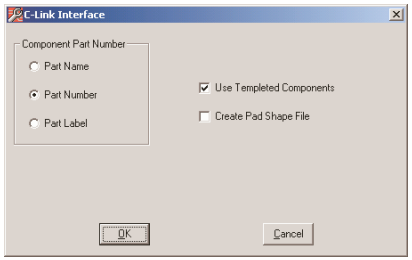
- **Other Mentor delivered tools provide industry standard outputs.**
  - **IPC-D-356**



  - **Fabmaster**

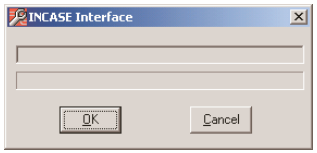


  - **C-Link**



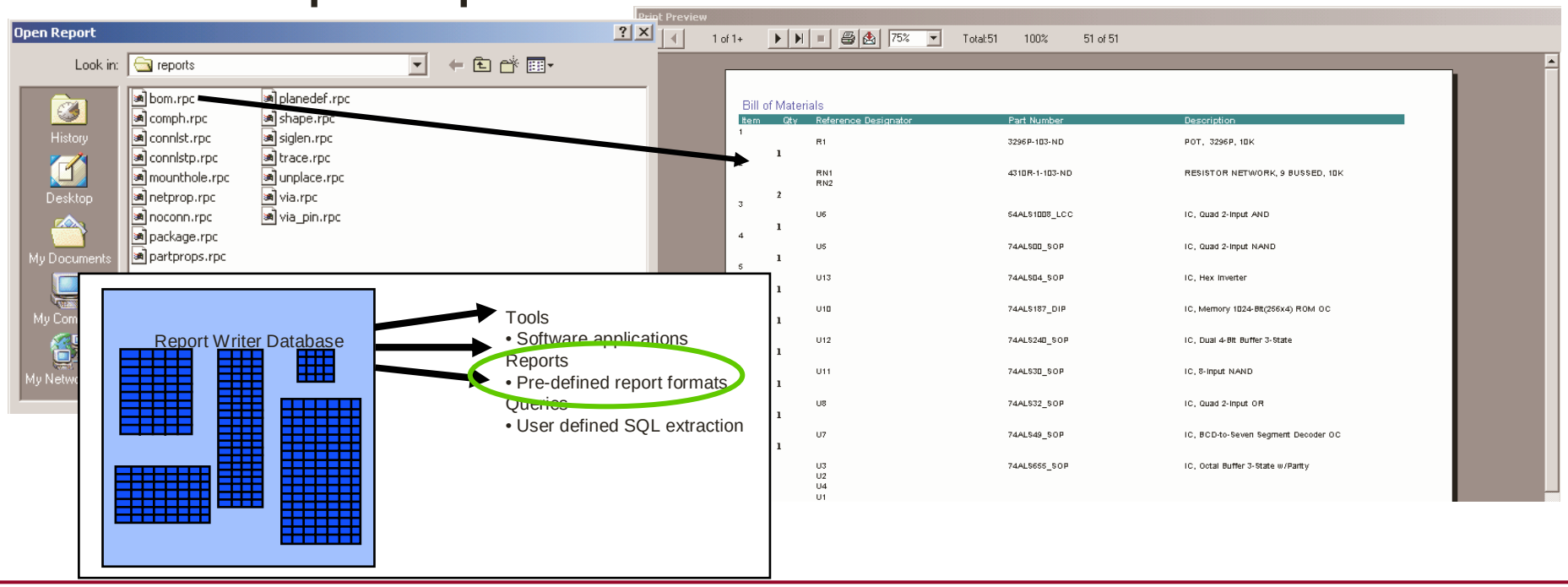
  - **HyperLynx**

  - **InCase**



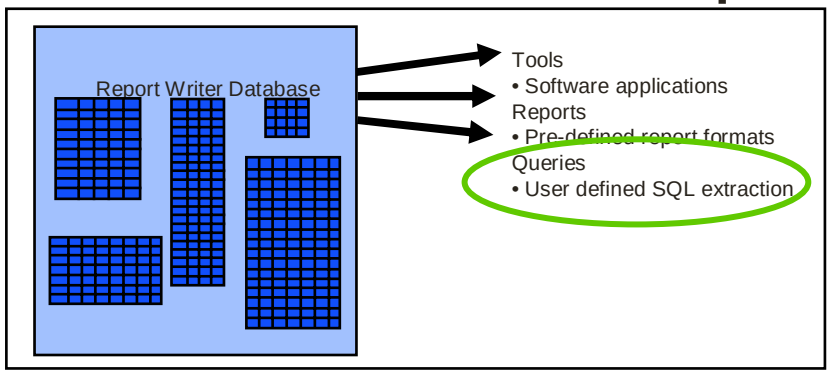
Defined Reports

- Defined report formats can be developed using Access or a tool such as Crystal Report Writer.
- Mentor delivered report formats are developed using Crystal Report Writer.
  - Stored at <load directory>\vbreport\report
- File > Open Report

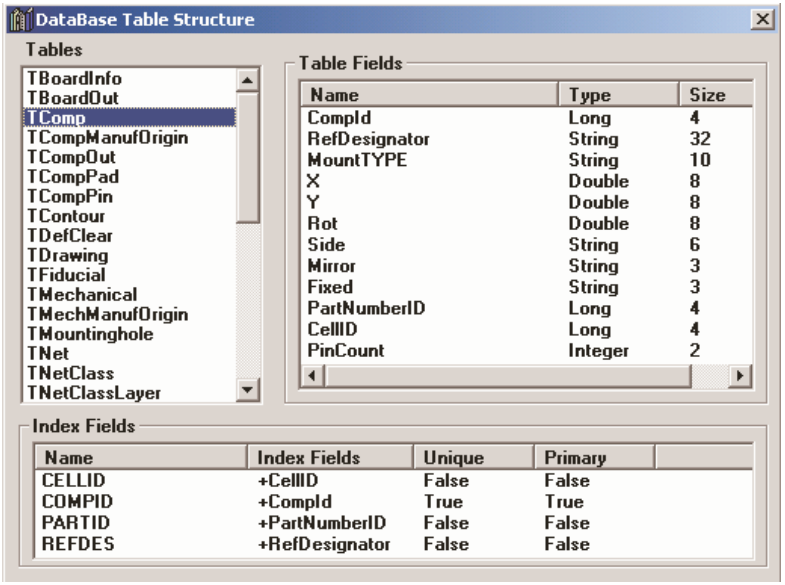


Queries

- **User defined extraction from the Report Writer Database tables.**

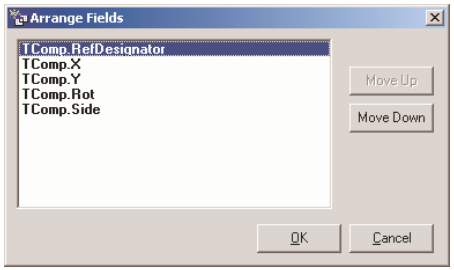


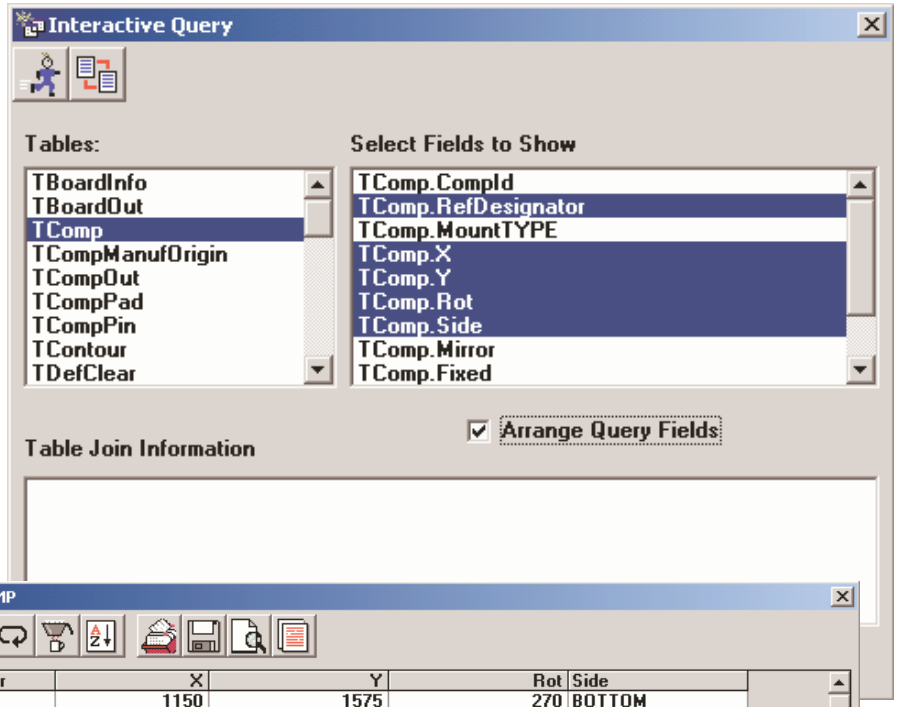
- **Can be saved and rerun.**
- **Need to understand table structure.**
  - **Schema > Show Tables**
    - **Select table name**
    - **Displays table's fields**



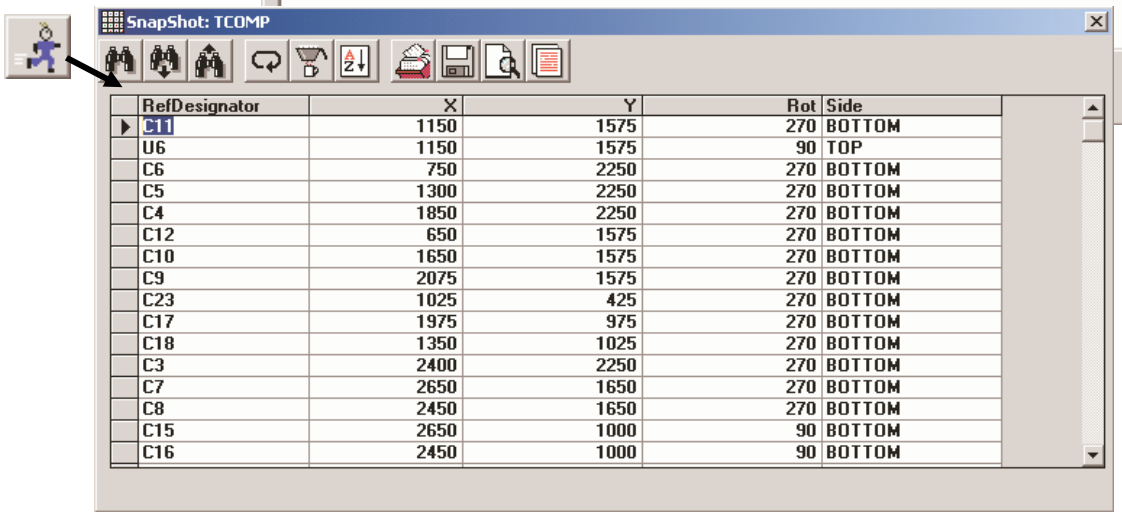
Basic Interactive Query

- **Query > Interactive Query**
  - **Select table**
  - **Select Fields - <Ctrl>**
  - **Select Arrange Query Fields**



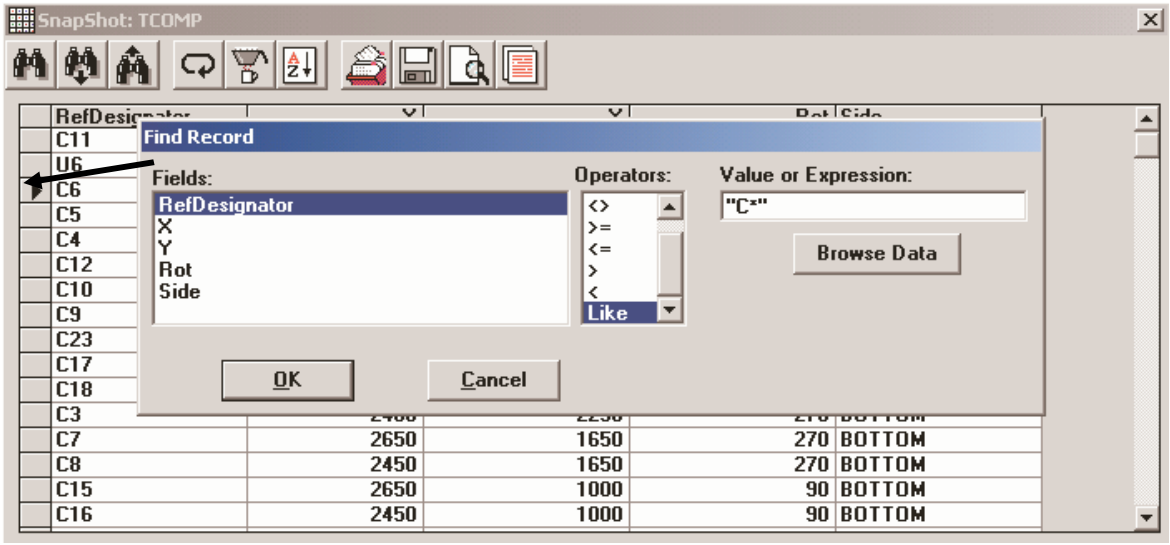


- **Click on Run SQL**

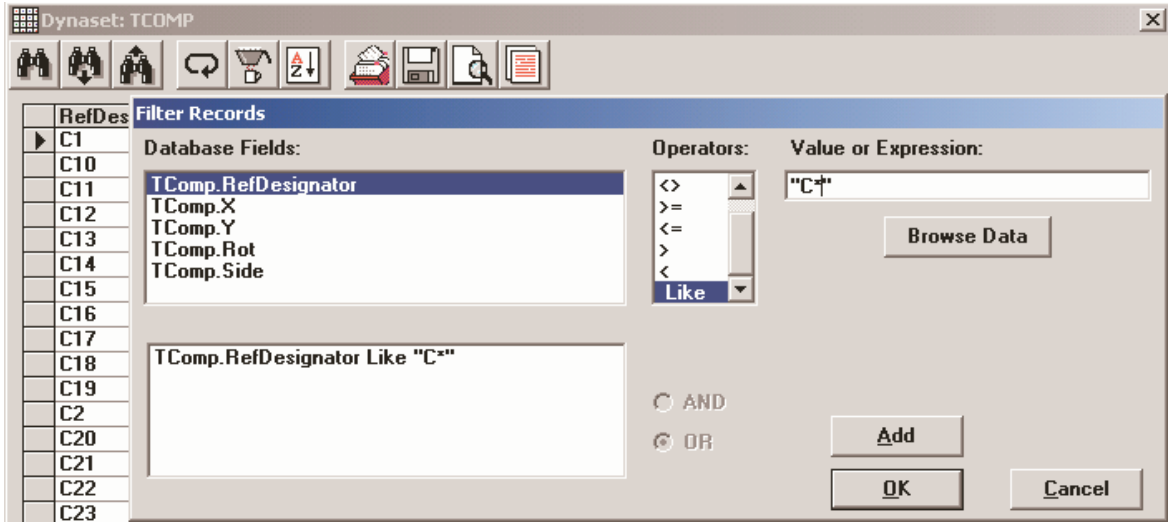


Query Snap Shot Features

- **Find**
  - **Find Next**
  - **Find Previous**

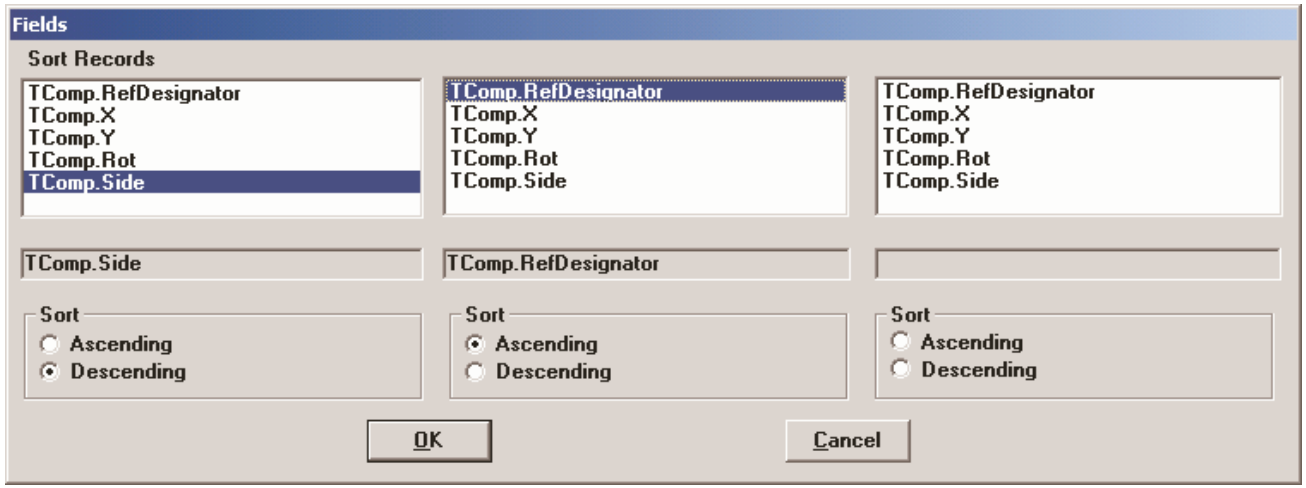


- **Filter**



Query Snap Shot Features (Cont.)

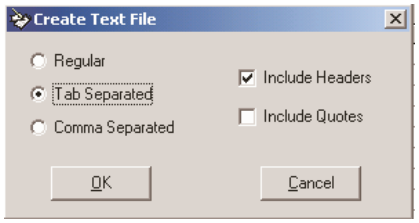
- **Sort**



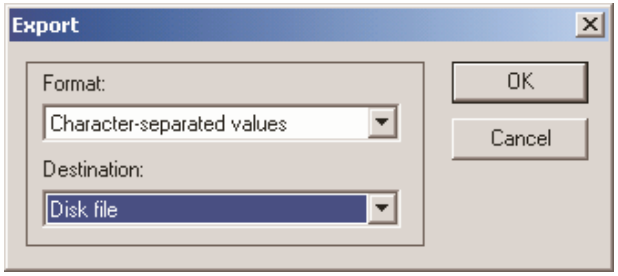
- **Reload Grid**

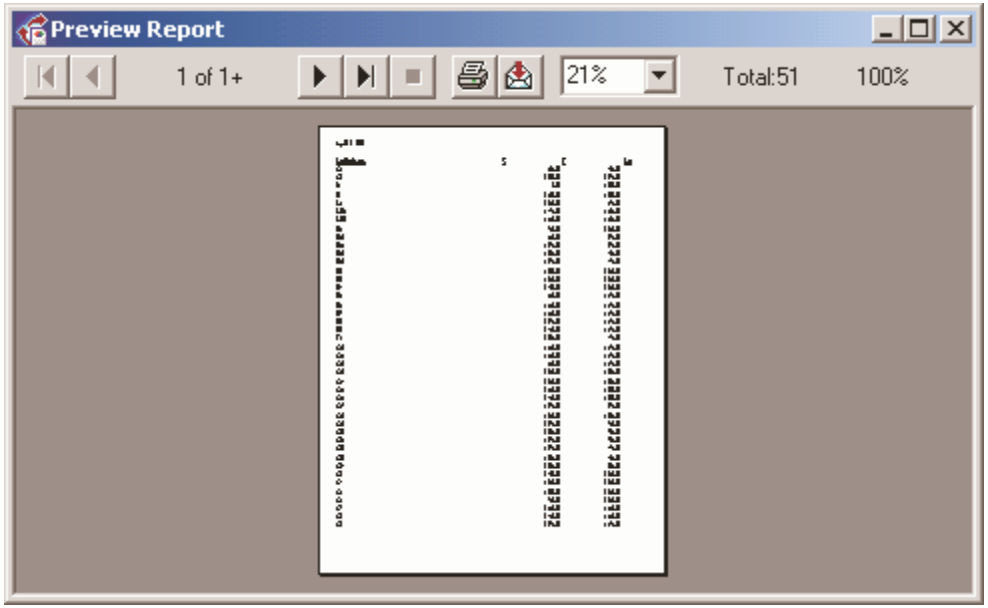
Query Snap Shot Features (Cont.)

- **Create a Text File**
  - **Browser/prompt to enter a file name**



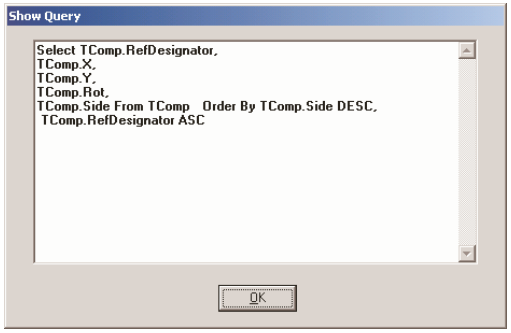
- **Preview Report**
  - **Allows exporting report in many formats.**



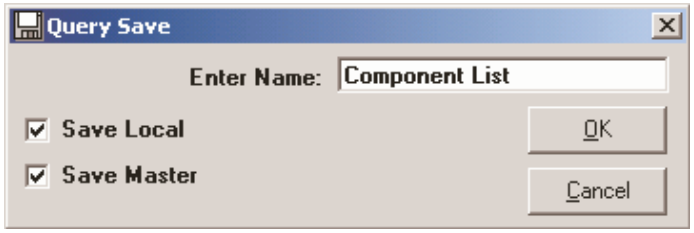


Query Snap Shot Features — Saving Queries

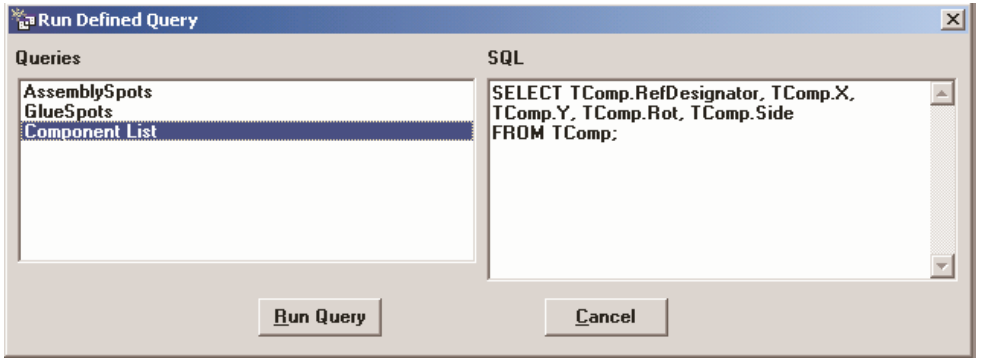
- **Show SQL** 



- **Save SQL** 
  - **Local — in the database**
  - **Master — in SQL storage file**
    - **Stored SQLs loaded into database at time of Import.**

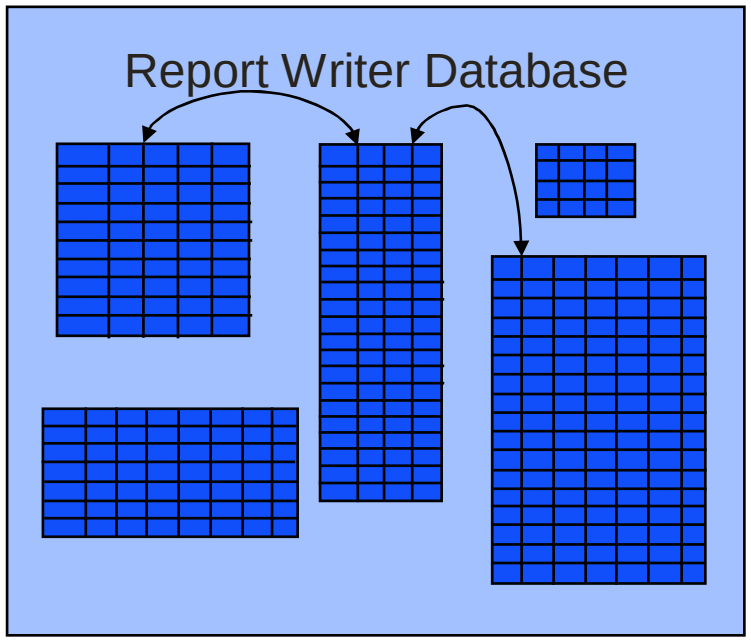


- **Query > Run Defined Query**
  - **Delivered Saved Queries**
    - **Assembly Spots**
    - **Glue Spots**



Queries — Joining Tables

- **The Problem**
  - **All of the data for a certain report may not be in one table.**
  - **Tables must be joined by common fields.**



- **What we want:**
  - **Reference Designator**
  - **Pin Number**
  - **Net Name**
  - **Pin X Location**
  - **Pin Y Location**
- **Where do we find that information?**

Queries — Joining Tables (Cont.)

- **The Problem**
  - **All of the data for a certain report may not be in one table.**
  - **Tables must be joined by common fields.**
    - **Figure out where the data is.**
    - **Figure out how to join the tables**

- **What we want:**
  - **Reference Designator**
  - **Pin Number**
  - **Net Name**
  - **Pin X Location**
  - **Pin Y Location**

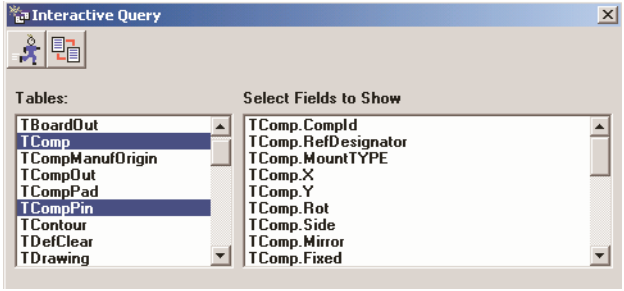
What	Table	Join #1	Join #2
Ref. Des	TComp	TComp:CompID	
Pin Nunb.	TCompPin	TCompPin:CompID	TCompPin:Net_No
Net Name	TNet		Tnet:Net_No
X	TCompPin		
Y	TCompPin		

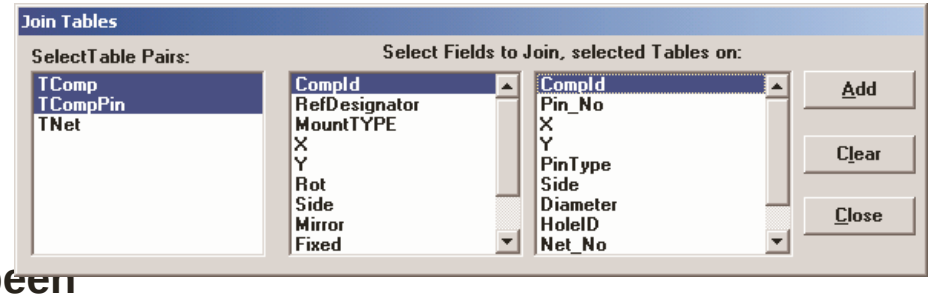
***** Three tables requires 2 joins

So - How do I do this???

Queries — Joining Tables (Cont.)

- **Step 1:**
  - **Join Tables**
    - **Query — Interactive Query**
    - **Select the tables to Join**
    - **Click Join Tables icon** 
    - **Click 2 tables to join**
      - **Fields will display in 2 columns**
    - **Select common fields**
      - **One in each column**
    - **Click on Add**





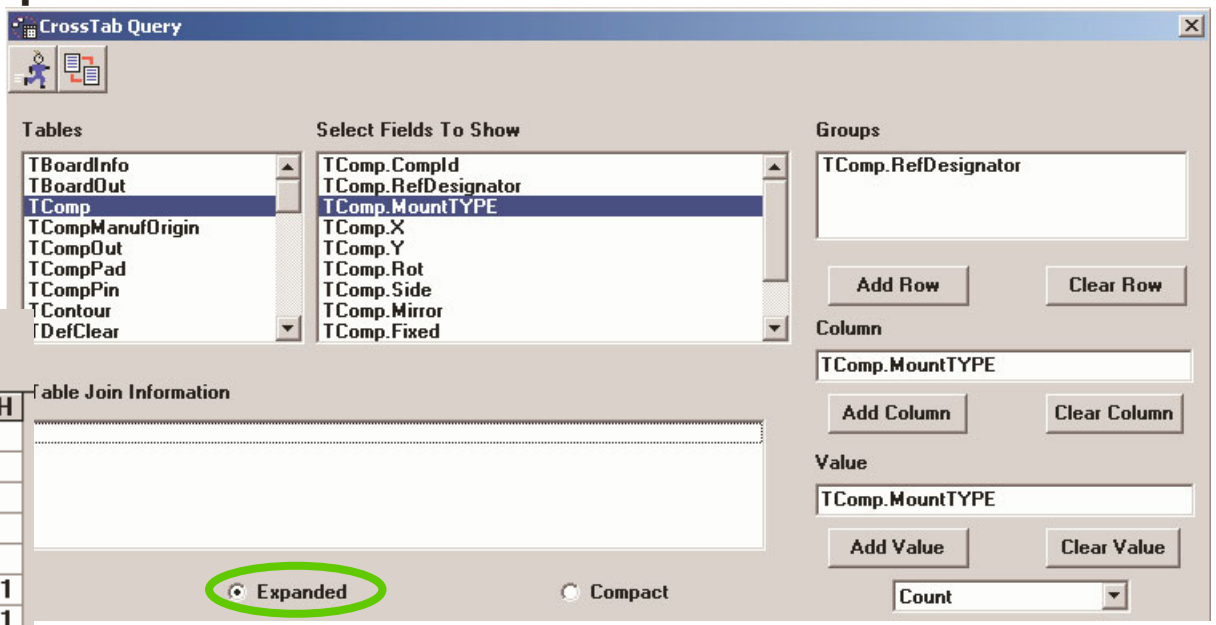
- **Step 2:**
  - **Define the Query**
    - **Select the tables that have been joined.**
    - **Select the fields to include.**
    - **Run the Query.**

Cross Tab Queries

- Data in a Spread Sheet format.
- Can do computations on columns of data.
- Needs definitions for three sets of data:
  - Row (Groups) — one or more fields to group data
  - Columns — builds column headers
  - Value — used to build the actual values in the table
- Computation functions are called Qualifiers:
  - Average
  - Count
  - Sum
  - Max
  - Min
- Cross Tab data can be organized into graphs.

Cross Tab Queries (Cont.)

- **Example 1:**
  - **A Mount Type Report**
    - **Expanded**



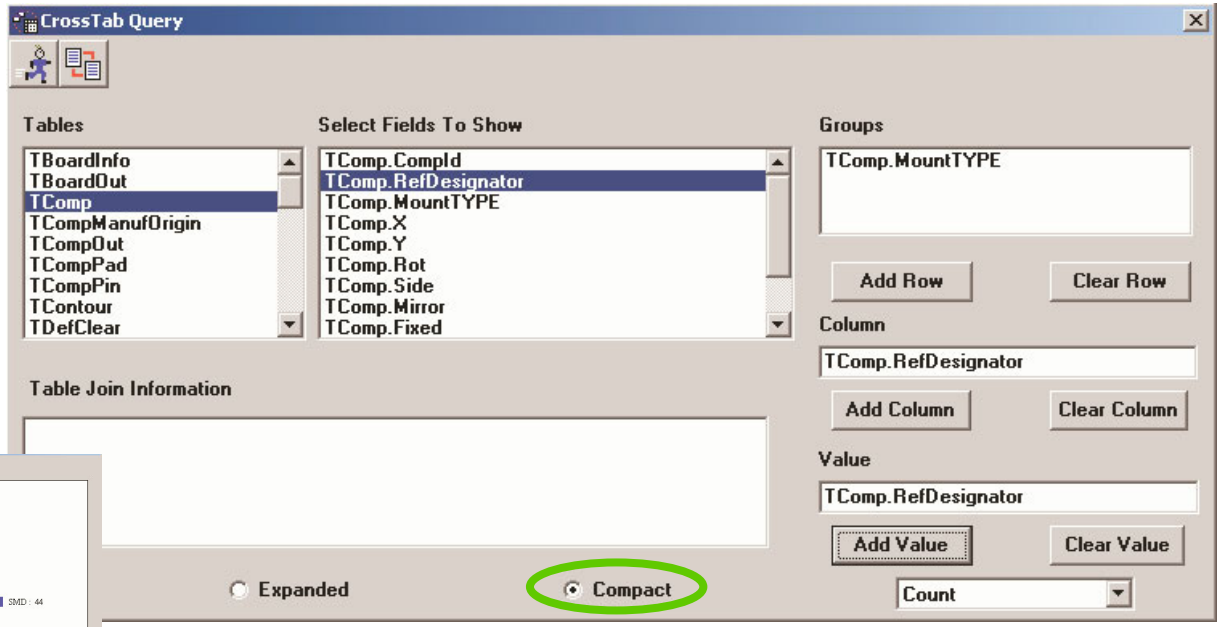
RefDesignator	SMD	THROUGH
R5	1	
R6	1	
R7	1	
R8	1	
R9	1	
RN1		1
RN2		1
U1	1	
U10		1
U11	1	
U12	1	
U13	1	
U2	1	
U3	1	
U4	1	
U5	1	

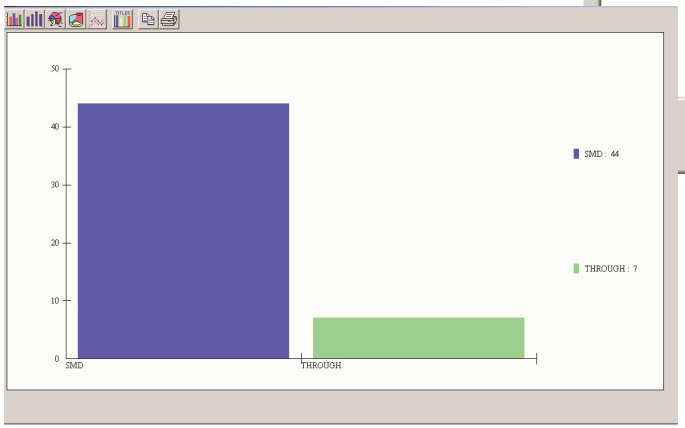
Groups (Rows) are based on Ref. Designator.
Columns are based on Mount Type.
Values are counted and put into the column - each Ref. Designator only has 1 Mount Type, so the array shows a 1 in the appropriate column for each reference designator.
This is Expanded format.

Cross Tab Queries (Cont.)

- **Example 2:**
  - **A Mount Type Report**
    - **Compact**

	MountTYPE	CountOf
▶	SMD	44
	THROUGH	7



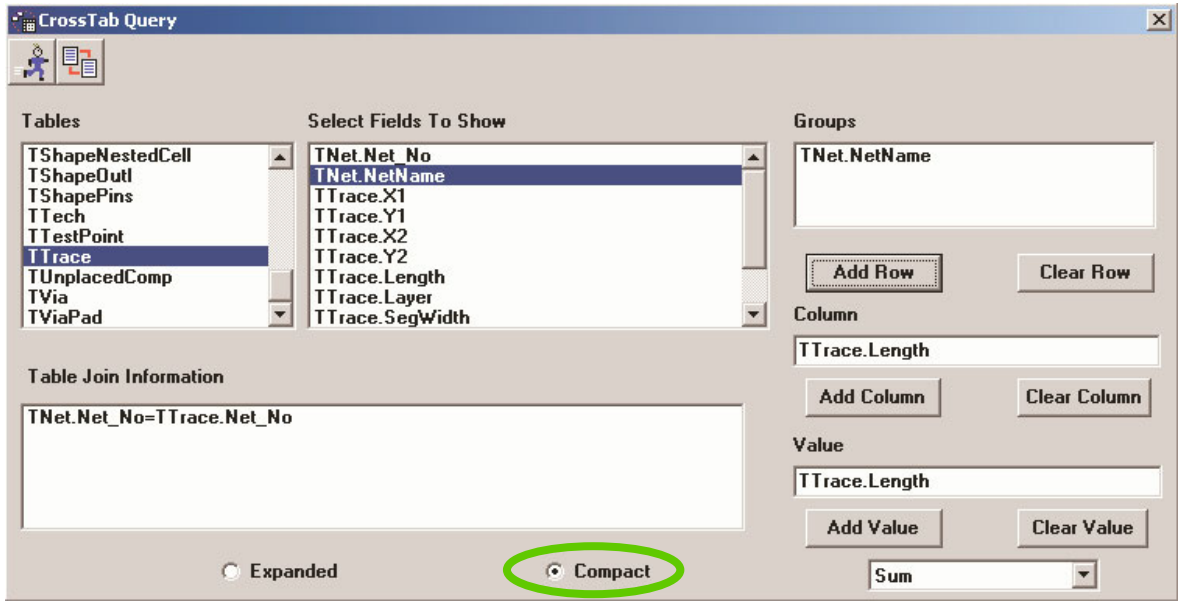


Groups (Rows) are based on Mount Type.
Columns are based on References Designators - but.
Values are counted and put into the column and compacted on the operation - Count.
This is Compact format.
Compact format can be Graphed using the Graph icon on the Snap Shot.

Cross Tab Queries (Cont.)

- **Example 2:**
  - **A Trace Length Report**
    - **Joined Tables**
    - **Compact**

	NetName	SumOf
	XSIG010006	793.566
	AMP2_IN	793.731
	AMP1_IN	816.98
	Q0	844.988
	HS(1)	1014.638
	RAMWR(0)	1038.244
	HS(2)	1059.908
	XSIG010038_6	1064.453
	Q1	1106.748
	XSIG010038	1224.438
	HS(6)	1313.705
	XSIG010002_2	1372.01
	HS(5)	1413.054
	HS(3)	1575.301
	D(3)	1586.195
	D(0)	1638.443
	D(4)	1703.462
	D(1)	1718.147
	HS(0)	1730.852
	D(2)	1749.746
	XSIG010047	1758.08
	HS(4)	1762.704
	D(5)	1777.642



Groups (Rows) are based on Net Name.
Columns are based on Trace Length - but.
Values are added and put into the column and compacted on the operation - Sum.
This is Compact format.

Lab Preview

- **This Module has 4 Labs.**
  - **Lab 1 — Report Writer Database**
    - You will make Report Writer databases based on the control1_reva database.
  - **Lab 2 — Interactive Queries**
    - You will do two or three queries based on the control1_reva database.
  - **Lab 3 — Cross Tab Queries**
    - You will create a net length report based on the control1_reva database.
  - **Lab 4 — Signal Integrity Reports (Optional)**
    - You will do two queries based on the control1_reva database using the electrical Report Writer database.

Advanced Expedition PCB

Appendix C

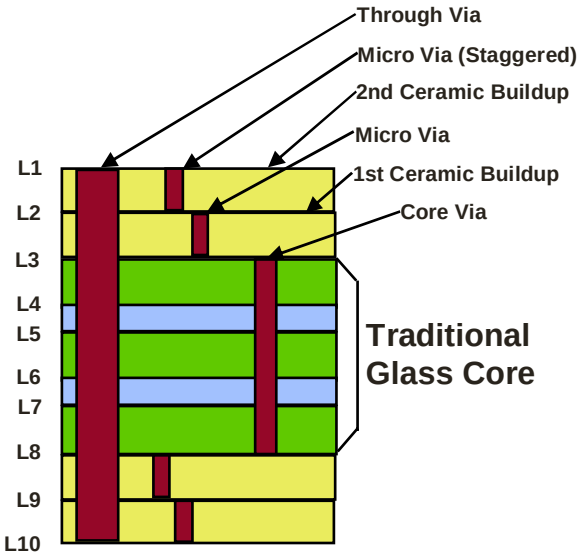
Micro Vias

Objectives

Upon completion of this lesson and lab, you will be able to:

- **Define Blind and Buried Vias**
- **Define Micro Vias**
- **Define Special Micro Via Clearances**
- **Run the Auto Router Using Micro Via Span Definitions**
- **Interactively Add Micro Vias**

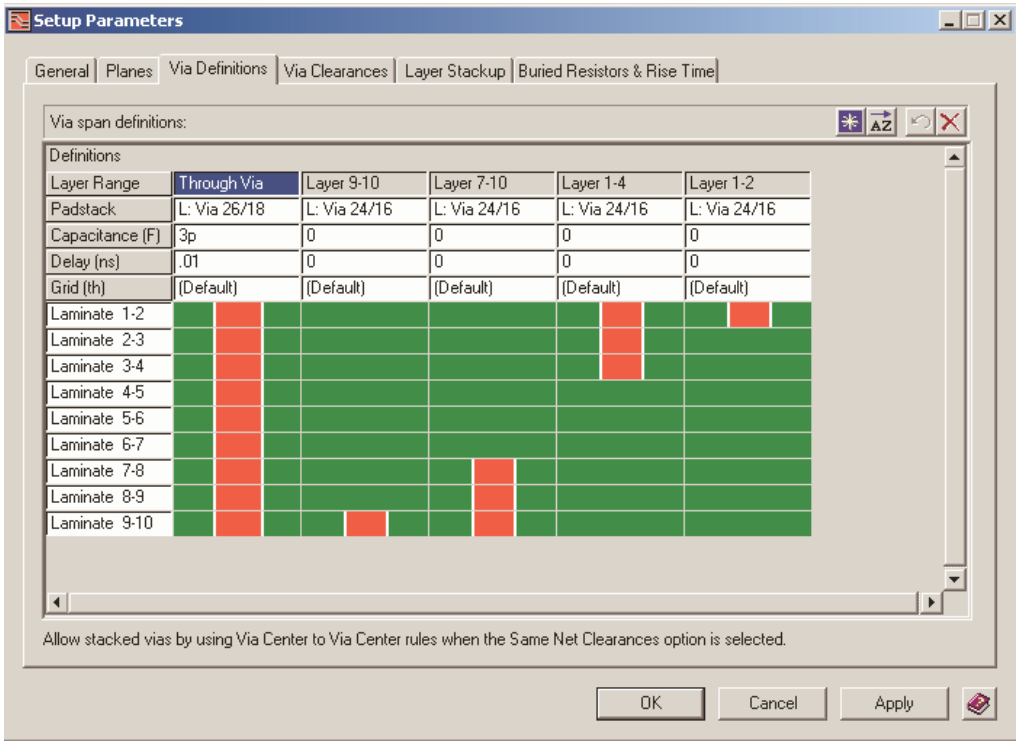
Micro Vias



- **Typically a Micro Via is:**
  - **Small via size ranging from 4 to 7 th.**
  - **Defined with a blind or buried characteristic.**
  - **Used on Ceramic build up boards.**
    - **Traditional glass core.**
    - **Ceramic build up on outside.**
      - **Glass core manufactured using standard PCB process first.**
      - **Ceramic build up followed by etch and via operation.**
      - **Ceramic buildup can be repeated for multiple ceramic layers.**
  - **Vias produced by non-mechanical means through the ceramic.**
    - **Allows process to work though one layer of ceramic.**
    - **Vias through multiple ceramic layer may need to be “staggered”.**
      - **Laser drilling.**
      - **Chemical etch process.**
      - **Photo etch process.**
  - **Generally associated with fine trace width on ceramic layers.**

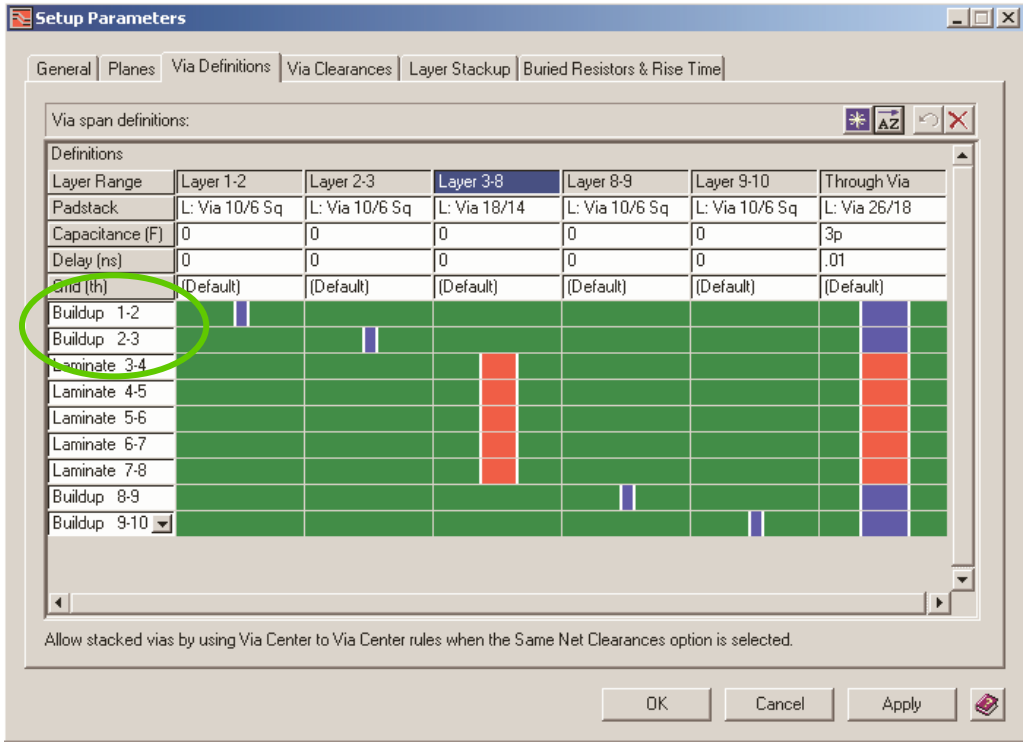
Blind and Buried Via Definitions

- **Setup > Setup Parameters — Vias Tab**
  - **Click New icon to start a new Via Span.**
  - **Click in the column to establish the layer span.**
  - **Choose the Padstack.**
- **Rules for Standard Manufacturing**
  - **Via Spans can not overlap.**
    - **1-4 & 3-6 is illegal.**
  - **Via Spans can be totally inclusive.**
    - **1-6 & 3-4 is legal.**
  - **Via Spans can not start at the top of prepreg or end at the bottom of prepreg.**
    - **1-3 & 2-4 are illegal.**



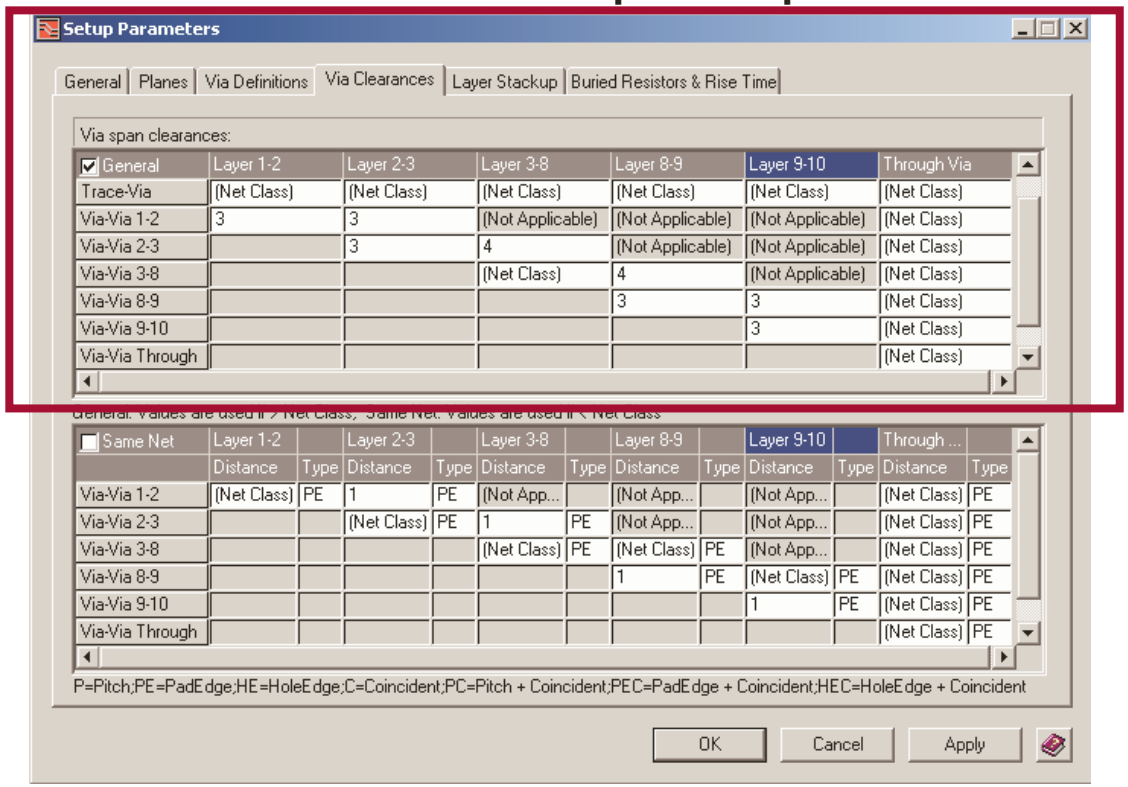
Micro Via Definitions

- **Setup > Setup Parameters — Vias Tab**
  - **Set the Buildup layers.**
  - **Click New icon to start a new Via Span.**
  - **Click in the column to establish the layer span.**
  - **Choose the Padstack.**
- **Rules for Micro Via Manufacturing**
  - **Laminate glass core follows Standard Manufacturing rules.**
  - **Micro Vias can be layer to layer.**



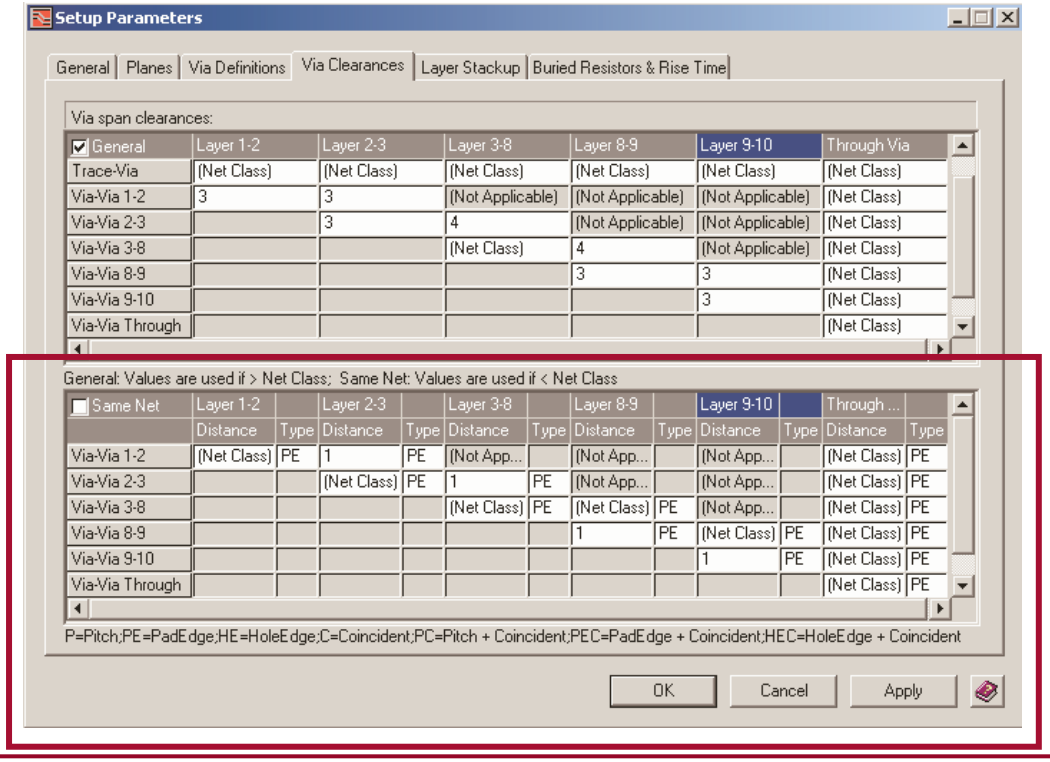
Micro Via Clearances

- **Special Clearances can be setup between Micro Via padstacks.**
  - **General clearances are for vias carrying different signals.**
  - **The array initially sets all to Net Class Clearance values.**
    - **Overrides can be set for each Span to Span definition.**



Micro Via Clearances (Cont.)

- **Special Clearances can be setup between Micro Via padstacks.**
  - **Same Net clearances are for vias carrying the same signals.**
  - **The array initially sets all to No Rule — meaning they are treated with the General clearances.**
    - **Overrides can be set for each Span to Span definition.**

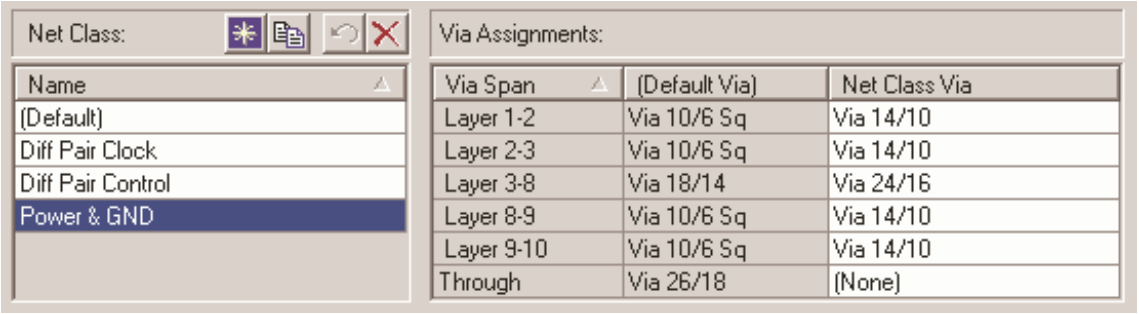


Same net clearance values can be set between:

PE – Pad Edges
HE – Hole Edge
P – Pitch
C – Coincident
Coincident Combinations

Micro Vias in Net Classes

- **Like other vias, Micro Vias padstacks can be assigned on a Net Classes basis.**



  - **In this example, the Power & GND Net Class uses a larger Micro Via than the one defined in Setup Parameters as the Default Via.**
  - **Notice that the Through Via has been set to (None).**
    - **This is done on all Net Classes for a Micro Via board.**
    - **This will prevent to use of Through Vias so that Micro Vias can be forced through the board in a step through pattern.**

Via in Pad Considerations

- **Many times, vias are allowed to placed in the pad copper for Micro Via designs.**
- **Setup > Editor Control — Pad Entry tab.**

  - **Generally, turn off Through hole vias.**

Auto Routing Micro Vias

- **The general method is:**
  - **Fanout**
    - **Gradually fanout from the outside of the board to the inside glass core.**
  - **Route**
    - **Use No Via route passes to route on accessible layers as the fanout proceeds.**
  - **More Routing**
    - **When the glass core is accessible, use standard routing passes.**
  - **Through Vias**
    - **If the initial routes do not reach 100%, go to Net Classes and enable Through Vias, then route again.**
  - **Manufacturing Passes**

- **So what does this really look like?**

Auto Routing Example Setup

- **This example is a 10 layer board, with Micro Via Spans — 1-2 & 2-3, 8-9 &9-10.**
- **Route > Auto Route**
- **First, set passes to only do fanouts between the outer layers.**

☑	Fanout	All Nets	1	2		1, 2
☑	Fanout	All Nets	1	2		9, 10

- **Add a No Via pass for the outer layers.**

☑	Fanout	All Nets	1	2		1, 2
☑	Fanout	All Nets	1	2		9, 10
☑	No Via	All Nets	1	2		1, 10

- **Add passes to do fanouts through the second Ceramic Build Up layers.**

☑	Fanout	All Nets	1	2		1, 2
☑	Fanout	All Nets	1	2		9, 10
☑	No Via	All Nets	1	2		1, 10
☑	Fanout	All Nets	1	2		1, 2, 3
☑	Fanout	All Nets	1	2		8, 9, 10

- **Add No Via passes for the next two layers.**

☑	Fanout	All Nets	1	2		1, 2
☑	Fanout	All Nets	1	2		9, 10
☑	No Via	All Nets	1	2		1, 10
☑	Fanout	All Nets	1	2		1, 2, 3
☑	Fanout	All Nets	1	2		8, 9, 10
☑	No Via	All Nets	1	2		2, 9

Keep Going →

Auto Routing Example Setup (Cont.)

- **Add passes to do fanouts to the top of glass core.**

☑	Fanout	All Nets	1	2		1, 2
☑	Fanout	All Nets	1	2		9, 10
☑	No Via	All Nets	1	2		1, 10
☑	Fanout	All Nets	1	2		1, 2, 3
☑	Fanout	All Nets	1	2		8, 9, 10
☑	No Via	All Nets	1	2		2, 9
☑	Fanout	All Nets	1	2		1, 2, 3, 4
☑	Fanout	All Nets	1	2		7, 8, 9, 10

- **Add a No Via pass for the next two layers and then for all of the glass core layers. Finish with standard routing passes.**

☑	Fanout	All Nets	1	2		1, 2
☑	Fanout	All Nets	1	2		9, 10
☑	No Via	All Nets	1	2		1, 10
☑	Fanout	All Nets	1	2		1, 2, 3
☑	Fanout	All Nets	1	2		8, 9, 10
☑	No Via	All Nets	1	2		2, 9
☑	Fanout	All Nets	1	2		1, 2, 3, 4
☑	Fanout	All Nets	1	2		7, 8, 9, 10
☑	No Via	All Nets	1	2		3, 8
☑	No Via	All Nets	1	2		All Enabled
☑	Route	All Nets	1	2		All Enabled
☑	Route	All Nets	1	5		All Enabled

- **The good news is:**

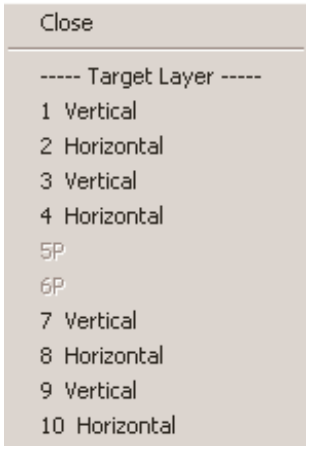
The Auto Router Fanout Pass does the Fanout stepping for you - simply enable a Fanout pass

Micro Via Strategies

- Planes on top or bottom layer of glass core.
  - Enable the Planes for routing in Editor Control.
  - Proceed as in example through the fanout that reaches the core — the surface plane layers — Pause after this pass.
  - Do not run a No Via to route on the plane layers.
  - Use Editor Control to disable routing on plane layers.
  - Continue with the rest of the example passes.
- To do Power and Ground fanout first.
  - Use the Items to route to qualify only the Power and Ground nets.
  - Just run the Fanout passes of the example.
- Signal Integrity routing.
  - Use the Items to route to qualify only the SI nets to rout, for instance all Differential Pairs.
  - Run all passes as in the example.
  - These passes would be a good candidate for a saved scheme.

Interactive Micro Vias

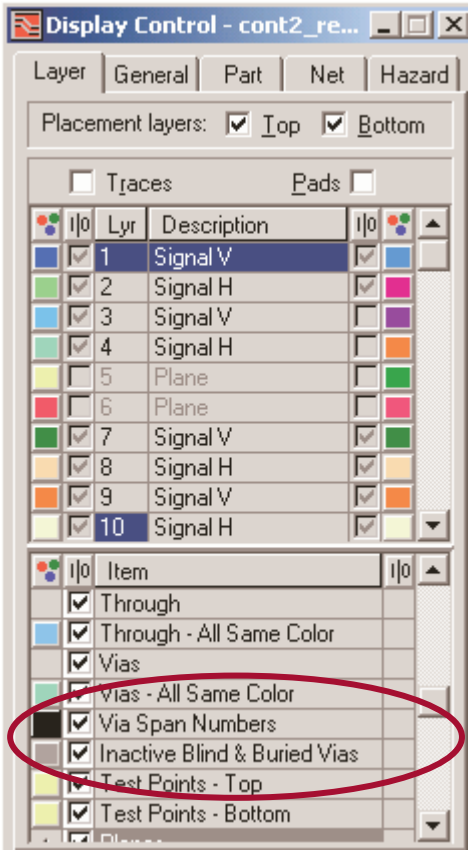
- **Routing Micro Via designs interactively is no different than other designs except:**
  - **Manually place the vias through one layer at a time.**
    - **Hold the <Shift> key.**
    - **<Right> mouse click for a menu.**



    - **Choose the layer to go to — Micro Vias will automatically be staggered through the board to the "to" layer. Click to orient the pattern, then continue routing.**

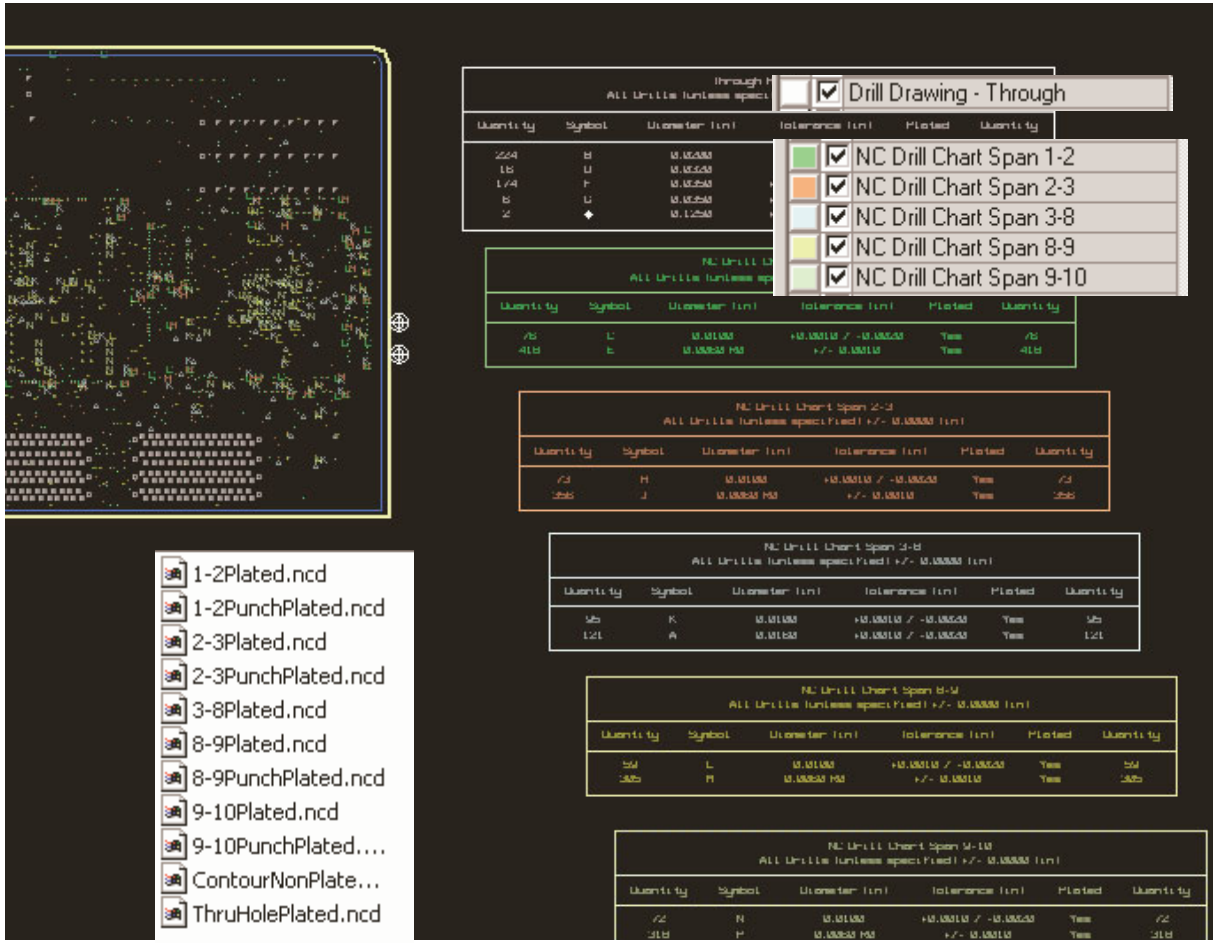
Via Span Display

- **Display Control has switches for controlling display features of Via Spans.**
  - **Via Span numbers displays the From-To span distance of the via.**
  - **Inactive Blind and Buried Vias sets a color that displays for vias that do not intersect the current active layer.**



Via Spans and NC Drill

- **On an board with Via Spans, NC Drill will:**
  - **Create a separate User defined layer for each Via Span**
  - **Create a Drill Drawing and Drill Chart on each of those User Defined layer**
  - **Output each Via Span into separate output files**



Lab Preview

- **This Module has 3 Labs.**
  - **Lab 1 — Setting Up the Database**
    - You will prepare “control2_reva” for routing as a Micro Via design.
  - **Lab 2 — Micro Via Setup**
    - You will define the Micro Via spans and parameters in the “control2_reva” database.
  - **Lab 3 — Micro Via Routing**
    - You will Interactively route some Micro Via connections. You will then AutoRoute the remainder of the design..

Advanced Expedition PCB

Appendix D

Variant Manager

Objectives

Upon completion of this lesson and lab, you will be able to:

- **Describe the Variant Manager Design Flow**
- **Create Variant Definitions**
- **Determine Part Equivalency**
- **Produce CAE Variant Output**
- **View CAE Variant Data**
- **Use Variants on Hierarchical Designs**
- **Create Variant CDBs and BOMs**
- **Create CAD Variant Data**
- **Define Variant Part and Padstack Definitions**
- **Create Report Writer Variant Data**

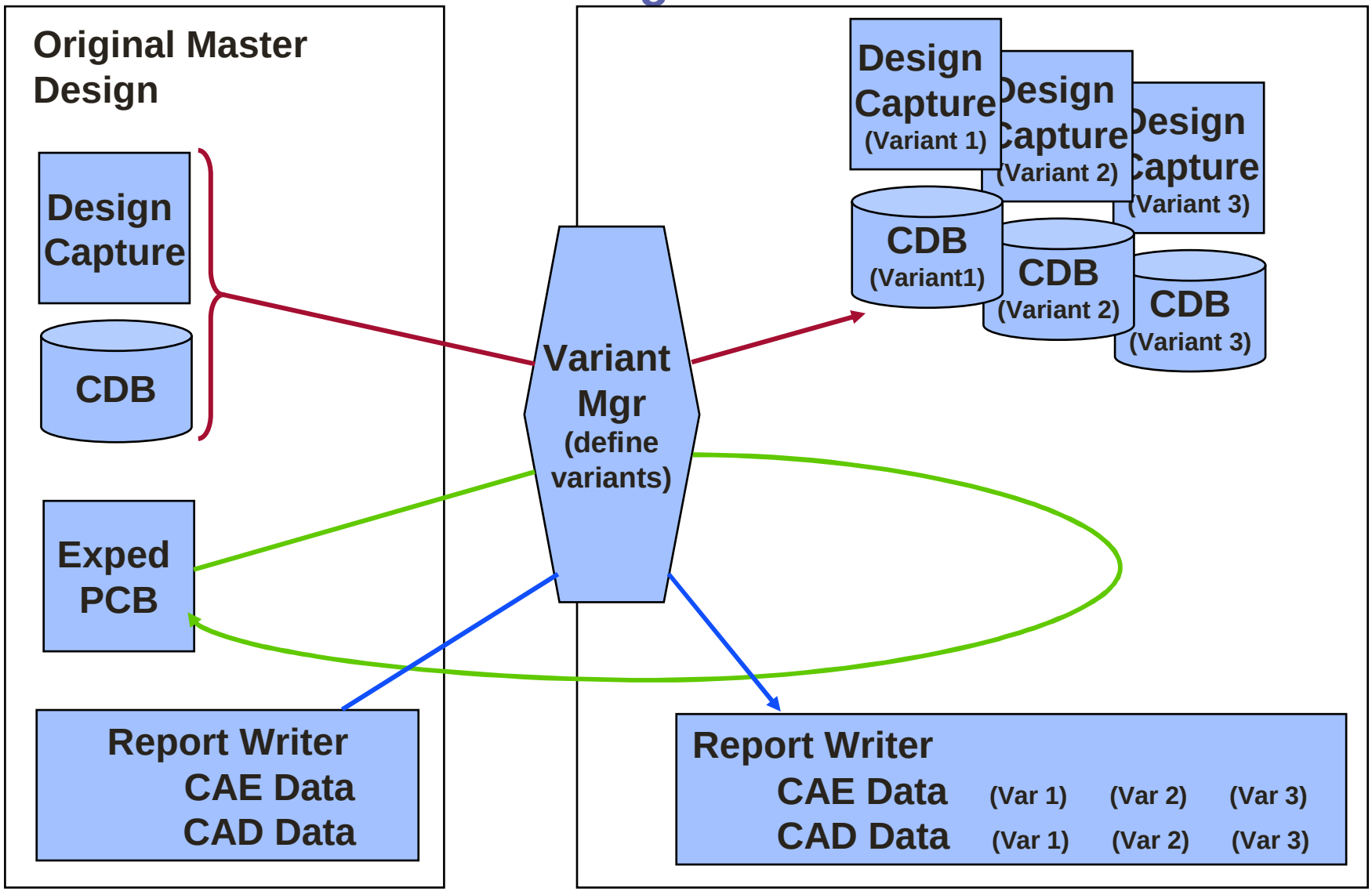
What Does Variant Manager Do?

- **Variants are designs which are subsets of an original design.**
  - **Change in Part Number of a component**
    - **Variant component has the same foot print on the PCB**
    - **Variant component has a different footprint on the PCB**
  - **Remove a component**

- **Variant Manager manages a database to store changes required for the Variants**

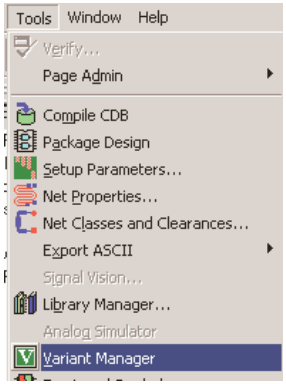
- **Variant Manager automatically modifies data to create the Variant:**
  - **CAE - Design Capture or Design View - and Utilities**
  - **CAD - Expedition PCB**
  - **Report Writer**

Variant Manager Workflow

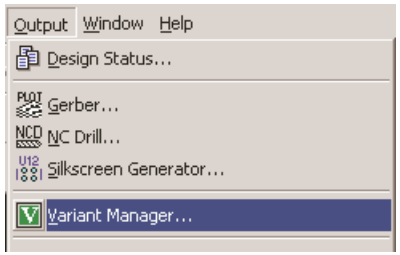


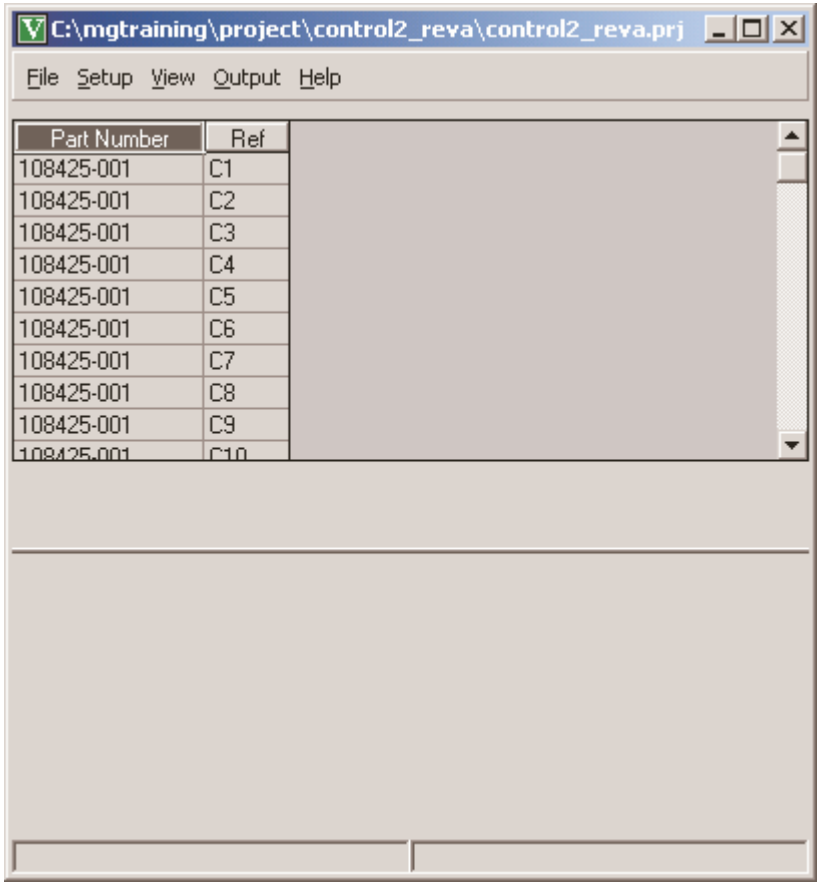
Invoking the Variant Manager

- **Start > Programs > Mentor Graphics SDD> WG2004 > Variant Manager > Variant Manager**
- **Design Capture**
  - **Tools > Variant Manager**



- **Expedition PCB**
  - **Output > Variant Manager**



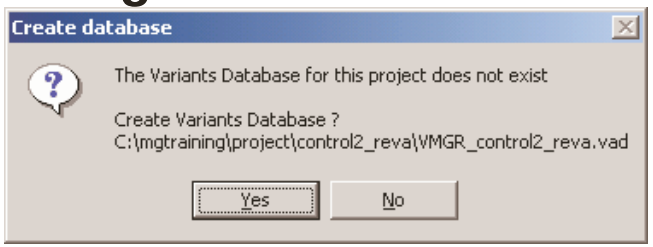


Variant Manager with Project open

Opening the Project

- **Variant Manager is a project driven tool - you must have a project open.**
  - **File > Project Open**

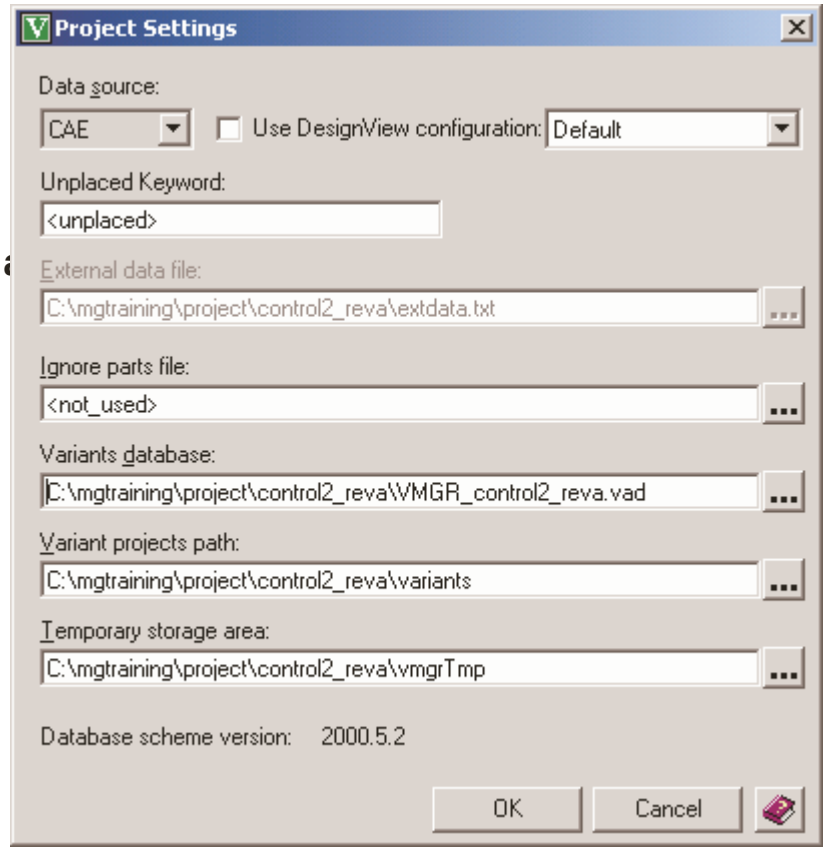
  - **Invoking from Design Capture or Expedition PCB automatically opens the current project in Variant Manager.**
- **If a project has not been opened in Variant Manager before, you will be prompted to create the Variant Manager database.**



- **The Variant Manager database is an Access format database which stores Variant information.**
  - **Stored in the Project directory**

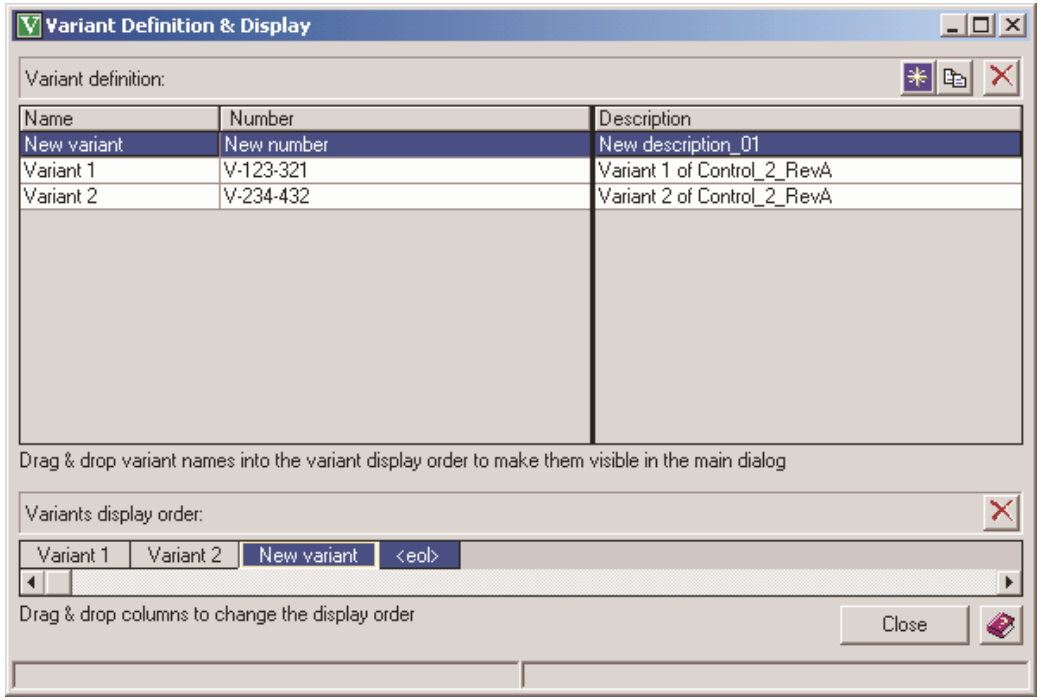
Editing the Project

- **To edit Project File settings that relate to the Variant Manager:**
  - **Setup > Project Settings**
    - **Design source - External data file**
    - **Unplaced keyword**
      - **Tag to represent unplaced Part in a Variant**
    - **Ignore parts file**
      - **ASCII file to disallow Variants on certain Part Numbers**
    - **Variants database**
      - **Location of Access Variant Manager database**
    - **Variants projects path**
      - **Location of CAE Variant projects**
    - **Temporary storage area**



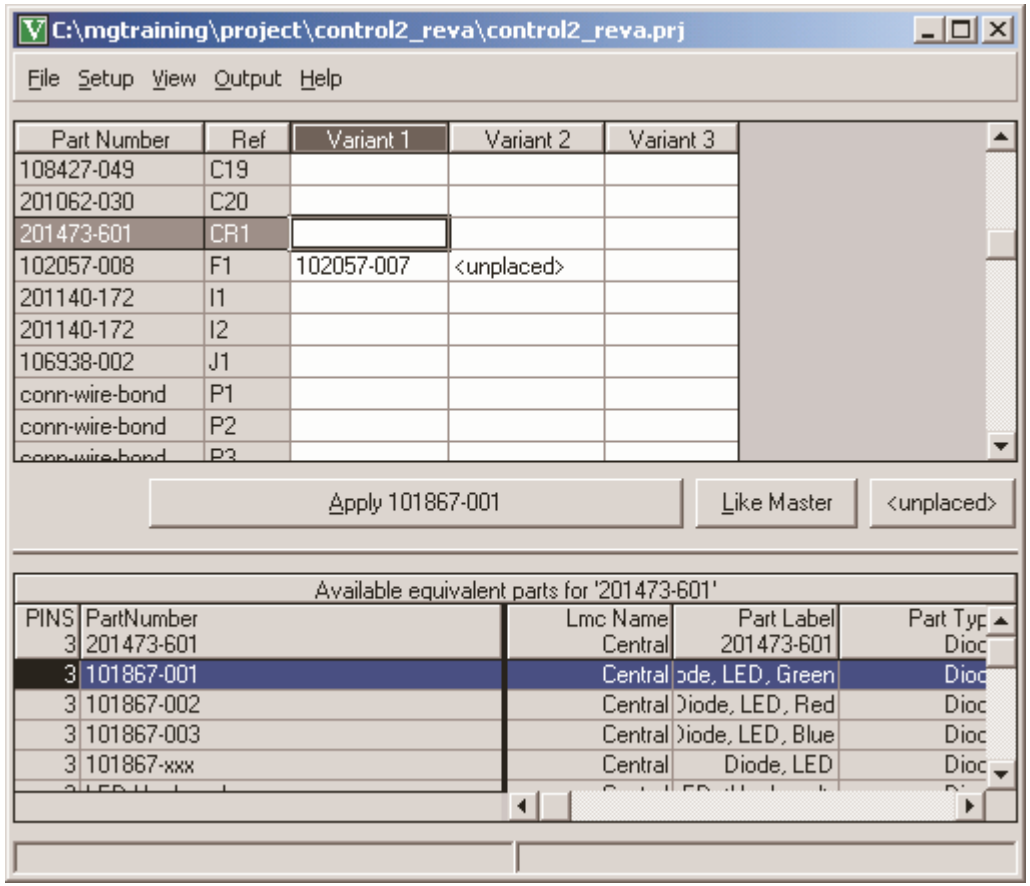
Variant Definitions

- **To Create a New Variant**
  - **Setup > Variant Definition**
    - **New or Copy icons to start a new Variant**
    - **Each Variant has a Name, Number and Description**
    - **Variant Display order**
      - **Order of Variants in other dialogs**
      - **Sets a Variant as "Active" - Delete from the list if a Variant is "Inactive"**



Variant Part Number Status

- Select the Part Number/Ref for the part to change
- Select the Variant column for the Part to change
- For a part Number Change:
  - Select the new Part Number from the Available equivalent parts table
  - Click the Apply … button
- To Remove a Part:
  - Click the <unplace> button



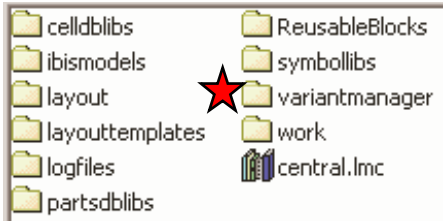
So how do parts end up on the two tables?

Which Parts Participate?

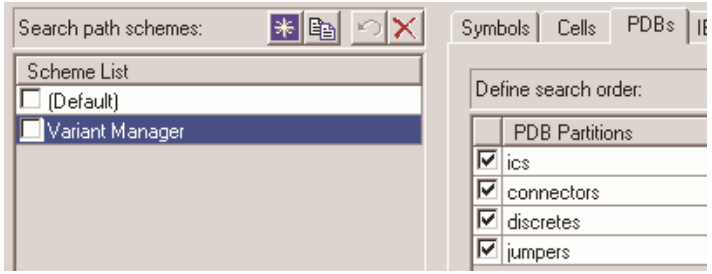
- **There are three controlling mechanisms that control part participation in Variant Manager tables:**
  - **Generate Variant Manager Central Library Data**
    - **Librarian controlled**
    - **Allows parts to appear in the Part Number table**
  - **Ignore Parts File**
    - **Designer controlled**
    - **Allows parts to be excluded from the Part Number table on a design by design basis**
  - **Setup > Equivalent Parts**
    - **Variant Manager controlled**
    - **Sets criteria for Parts to appear in the Equivalent Parts list**

Generate Variant Manager Central Library Data

- **In order for Parts to be allowed to be either a Part to be replaced, or a Part that can be used as an Equivalent, they must appear in a Central Library/Variant Manager database**
  - **Access format**
  - **Generated by the Generate Variant Manager Central Library Data command**

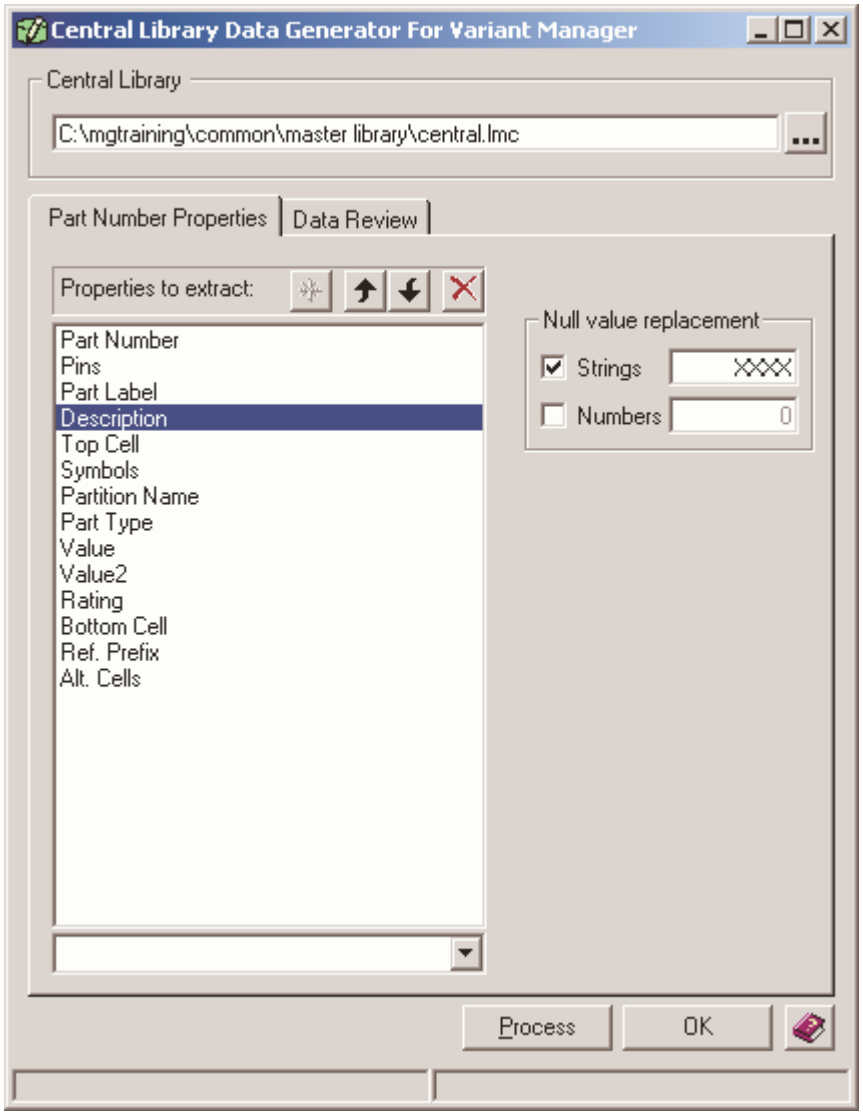


- **The GVMCLD command generates a database that lists Part Numbers and properties for all Parts in specific Part partitions**
  - **Those Partitions are listed in a special Library Manager Search Path called Variant Manager**
  - **Library Manager - Edit > Partition Search Path**
    - **Part partitions in that search path are included in the Central Library/Variant Manager database**



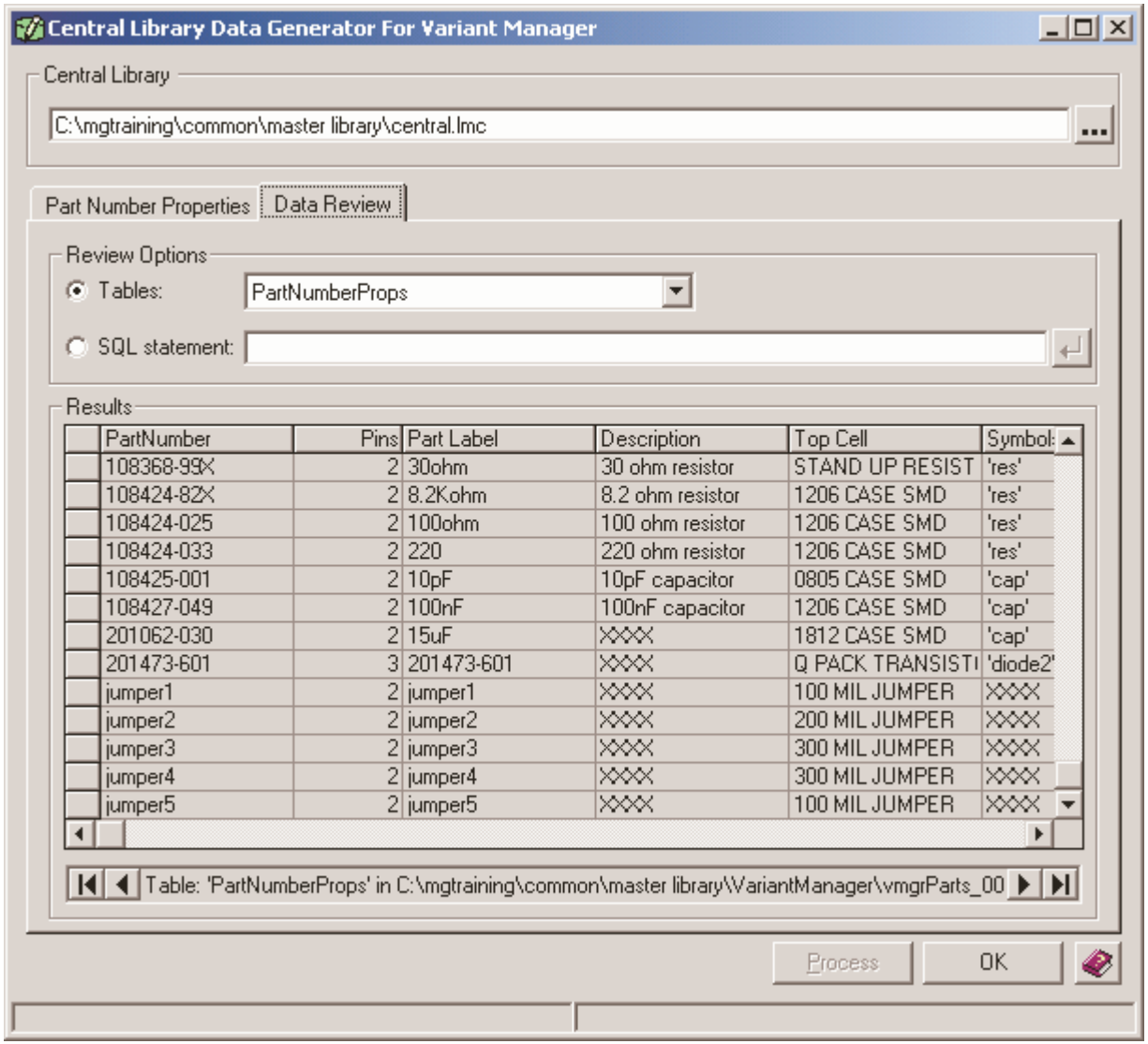
Generate Variant Manager Central Library Data (Cont.)

- **Start > Programs > Mentor Graphics SDD > WG2004 > Variant Manager > Variant Manager > Generate Variant Manager Central Library Data**
  - **Select ".lmc" file for Central Library (Browser)**
  - **Dialog - Part Number Properties tab**
    - **Set the list of Properties to include**
    - **Set default values to be put in database if there is no property value in Part**
    - **Process - builds the database**



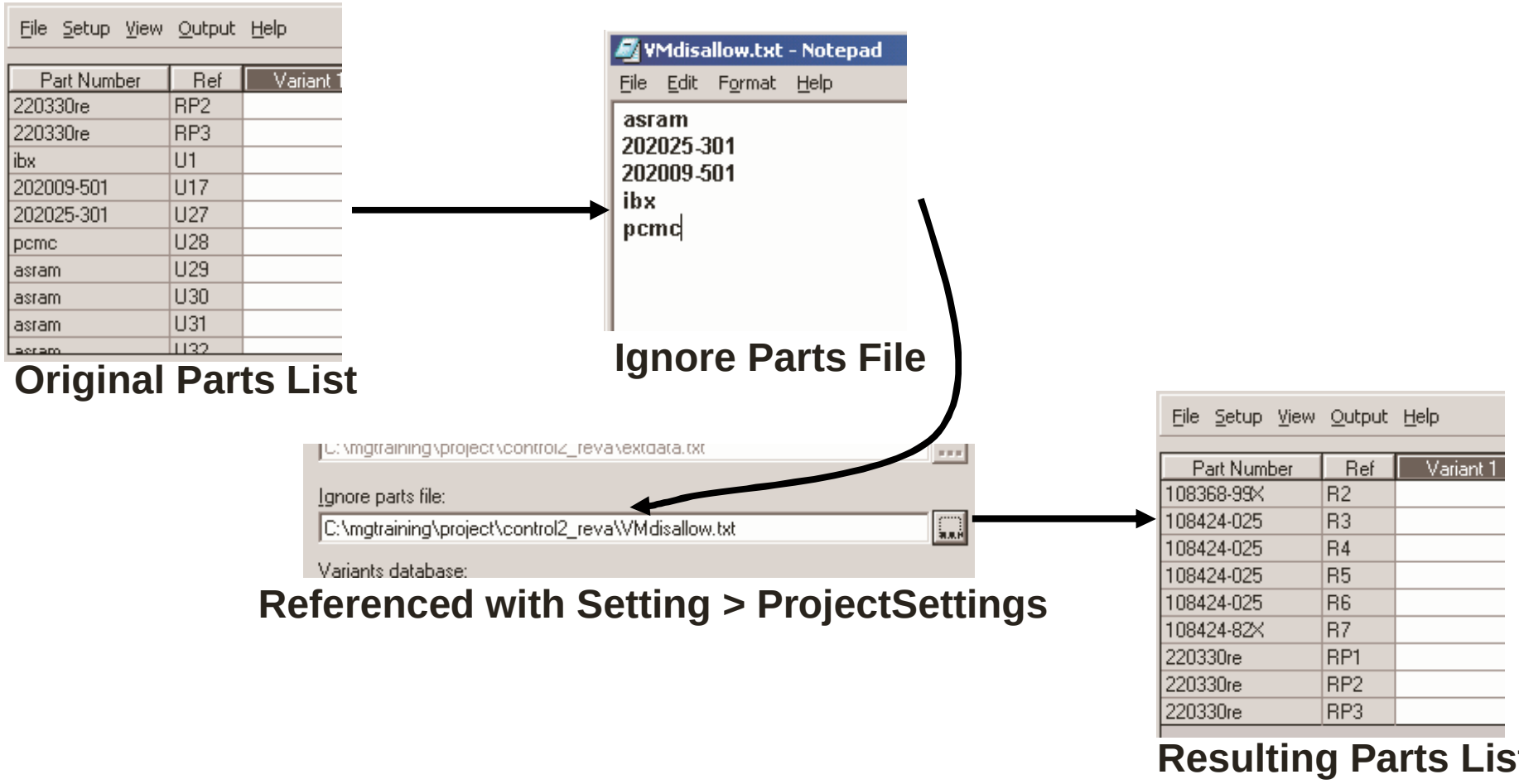
Generate Variant Manager Central Library Data (Cont.)

- **Dialog - Data Review tab**
  - **Set the Review Option**
  - **Examine the table data**



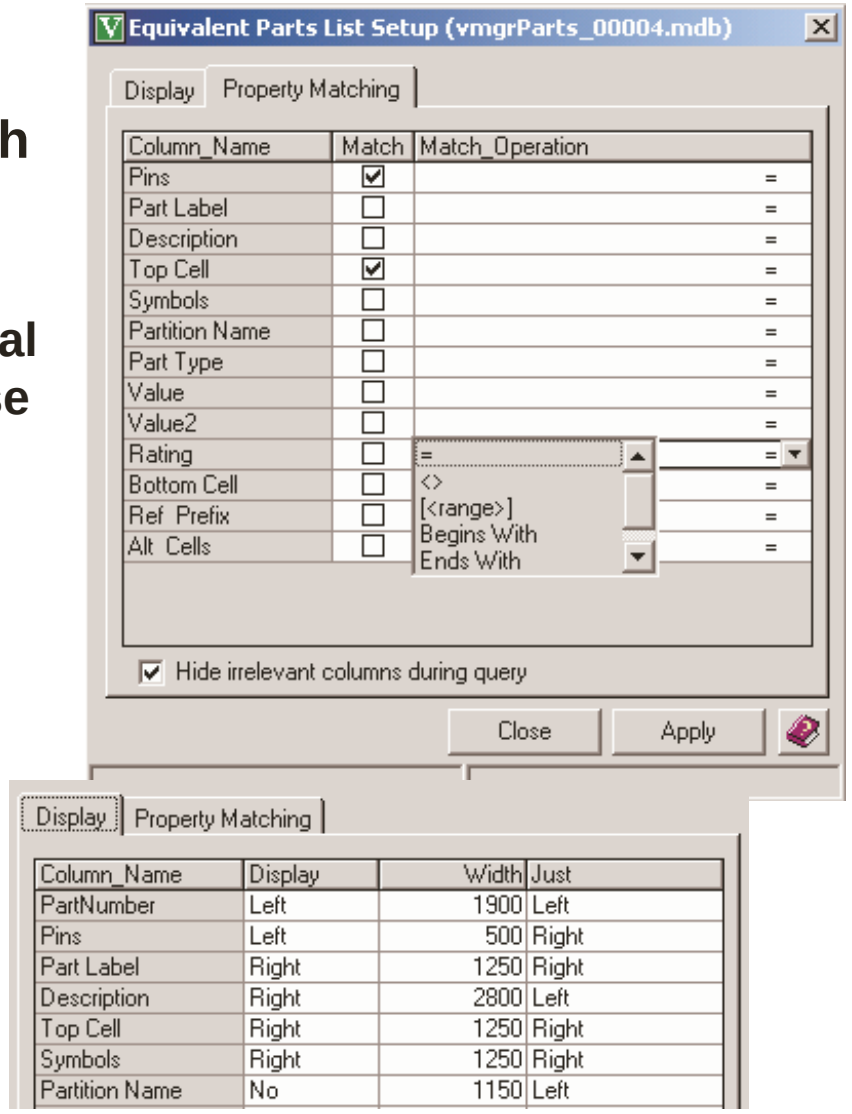
Ignore Parts File

- **An ASCII file that is a list of Parts allowed to modify in the Variants**



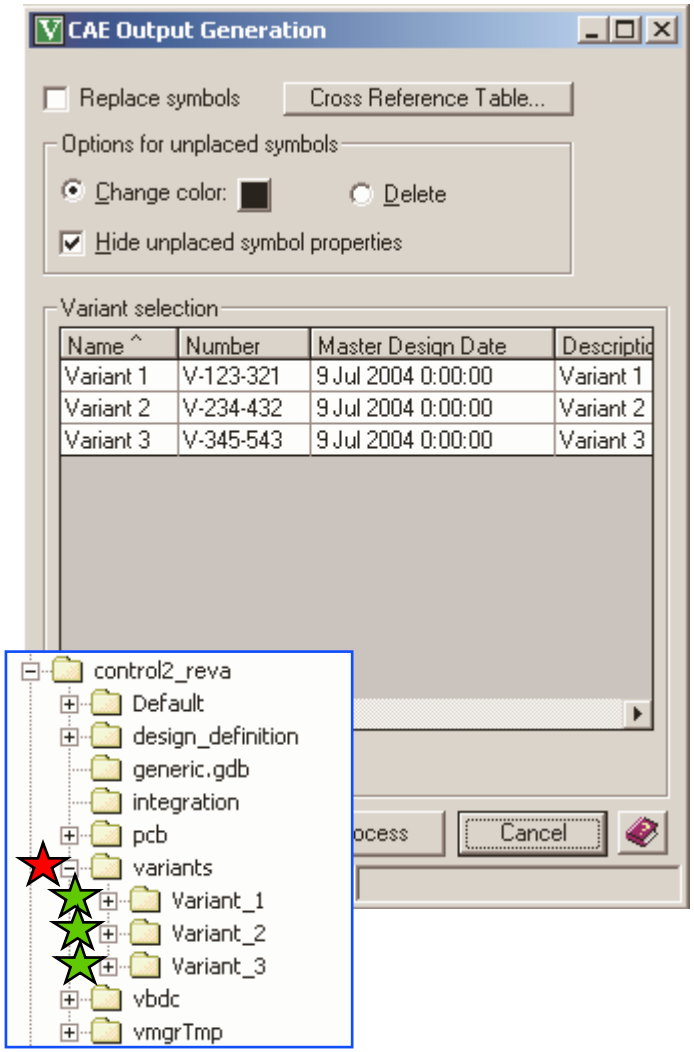
Equivalent Parts List

- **In order for Parts to be listed as Equivalent Parts they must match the qualifiers on the Setup > Equivalent Parts List command**
  - **List of all properties in the Central Library/Variant Manager database**
  - **Match - sets that property as a qualifier**
  - **Match qualifier - sets how the properties of the equivalent Part must compare to the same property in the modified Part**
  - **The Display tab sets column display characteristics on the Variant Manager table**
- **Setting can be made “on the fly”**



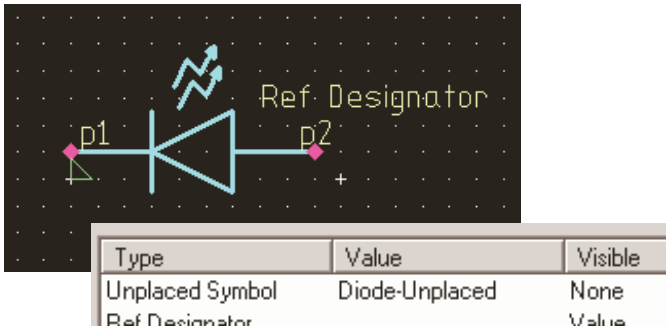
CAE Variant Output

- **To generate CAE (schematic) output for a Variant:**
  - **Output > CAE**
    - **Set Options 0 all options refer to how to handle unplaced Parts**
    - **Select Variants to Process**
      - **Only Active variants appear on the list unless you uncheck “Active variants only”**
    - **Process**
- **What it does:**
  - **Creates a Variants sub-folder in the project**
  - **Creates a new project folder for each of the variants in that sub-folder**
  - **Creates new schematics for each Variant**

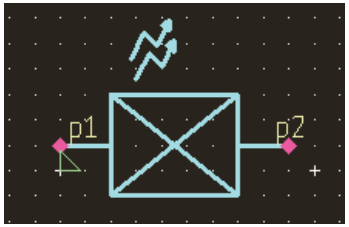


CAE Variant Output (Cont.)

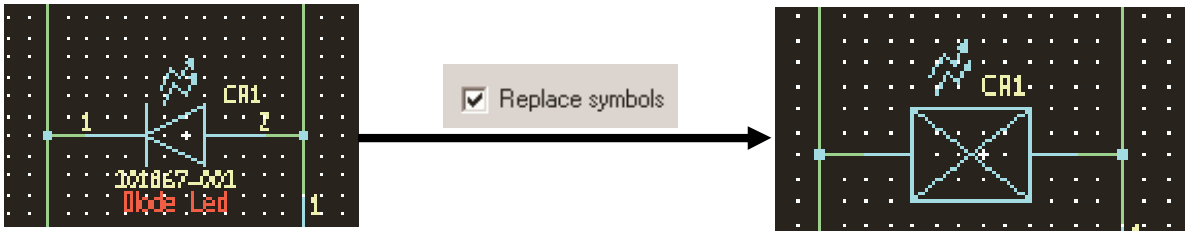
- **Replace Symbols**
  - **You can set an alternate symbol to use to replace the original symbol in a schematic if it removed in the Variant**
    - **Set the Pin locations and Pin names for the replacement Symbol to be the same as the original Symbol**
    - **Assign an Unplaced Symbol" property to the original with a value set to the name of the Unplaced_Symbol name**



Original Symbol



Replacement Symbol (Diode-Unplaced)



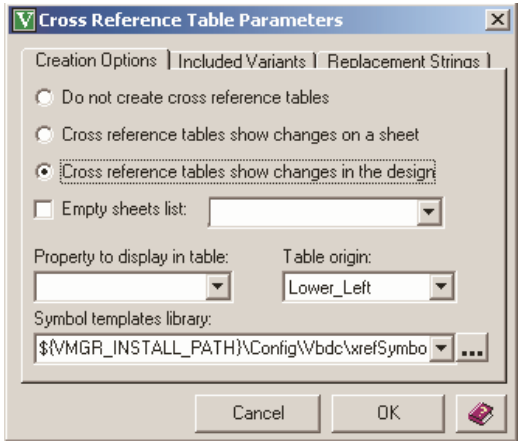
Original Schematic **Variant Schematic**

Cross Reference Table

- **A Variant table can be automatically generated for each page, showing the Variant information for that page.**
  - **Place a Cross Reference Place Holder Symbol on the page**
    - **Symbol Name must be - VMGRXREF**
    - **Symbol Type must be Pseudo Component**
    - **Any graphics is allowed - Table is placed at the Symbol origin**
  - **Edit project file settings**
    - **These setting can only be changed Using the Cross Reference Table option on the Generate CAE Output dialog**

  - **CAE Output then automatically generates the table in the Variants**

Place Holder in Master Schematic



	Variant 1	Variant 2	Variant 3
R3	108424-82X	108424-033	102057-008
R4	108424-82X	108424-033	102057-008
R5	108424-82X	108424-033	102057-008

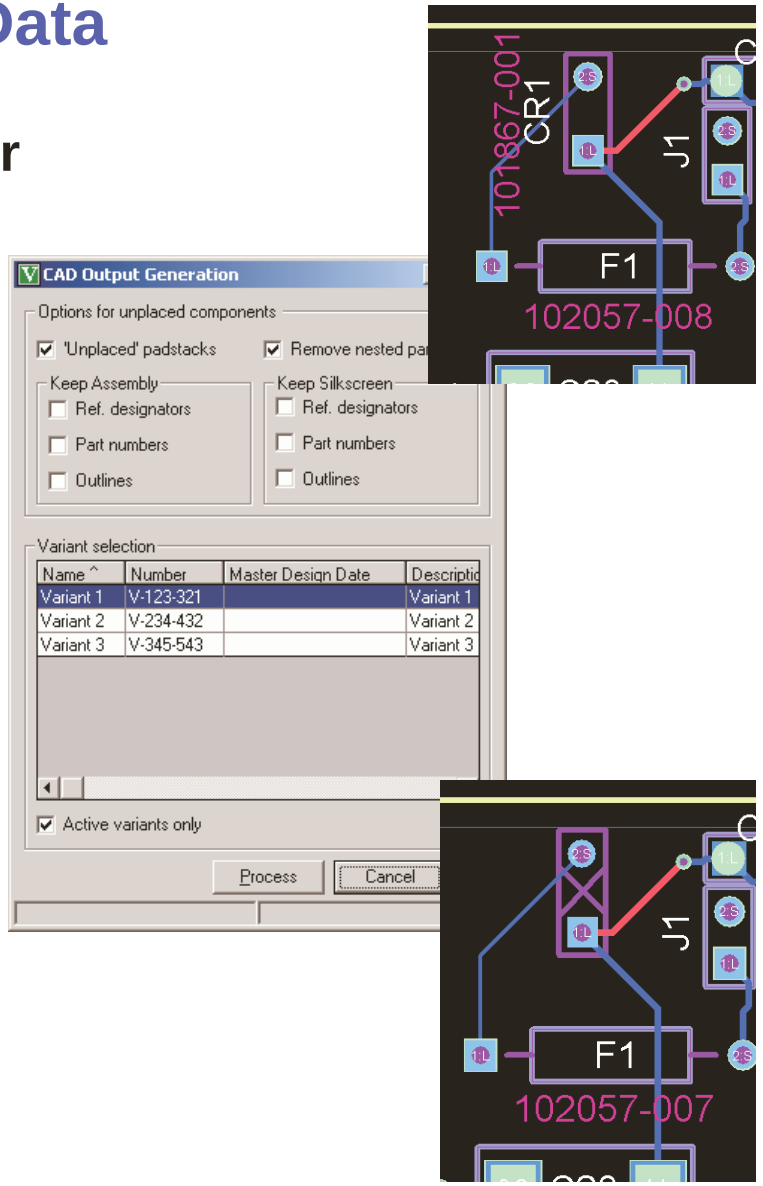
Viewing CAE Variants

- **To View the Variant Schematic, simply open the Variant project in Design Capture.**
- **If a Design has Hierarchical Blocks and there are multiple instance blocks, in the Variant, each instance of the multiple instance block will be generated separately with a unique instance name.**
- **To create a BOM from a variant:**
  - **Open the Variant project**
  - **Generate the Variant CDB**
  - **Run the “CDB to BOM” Utility using the Variant project**

CAD Variant Data

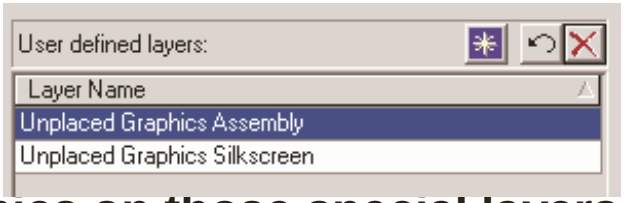
- **In order to generate the CAD data for a Variant design:**
  - **Complete the layout for the master design**
  - **Open the master design**
  - **Open Variant Manager**
    - **Output > CAD**
    - **Select Variant to Process**
    - **Set Options for removed parts**
    - **Process**
  - **Changes are made to the Expedition PCB Design**
  - **Output Gerber and NC Drill for the design**

- **DO NOT SAVE THE DESIGN**

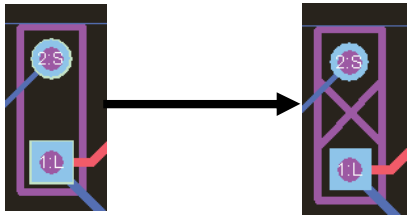


Variant Cell Data

- **When a Cell is Removed, the Assembly and Silk Screen Graphics can be replaced with “Removed Cell Graphics” that is included in the Cell.**
  - **Create the Standard Cell**
  - **In the Library Manager - Setup > Setup Parameters command, create specially named User Defined Layers - names MUST be:**
    - **Unplaced Graphics Assembly**
    - **Unplaced Graphics Silkscreen**



  - **In the Cell, draw the Unplaced Graphics on those special layers**
  - **During Output > CAD processing, the graphics from those layers are moved to the Assembly Outline and Silkscreen Outline layers for Variant output.**

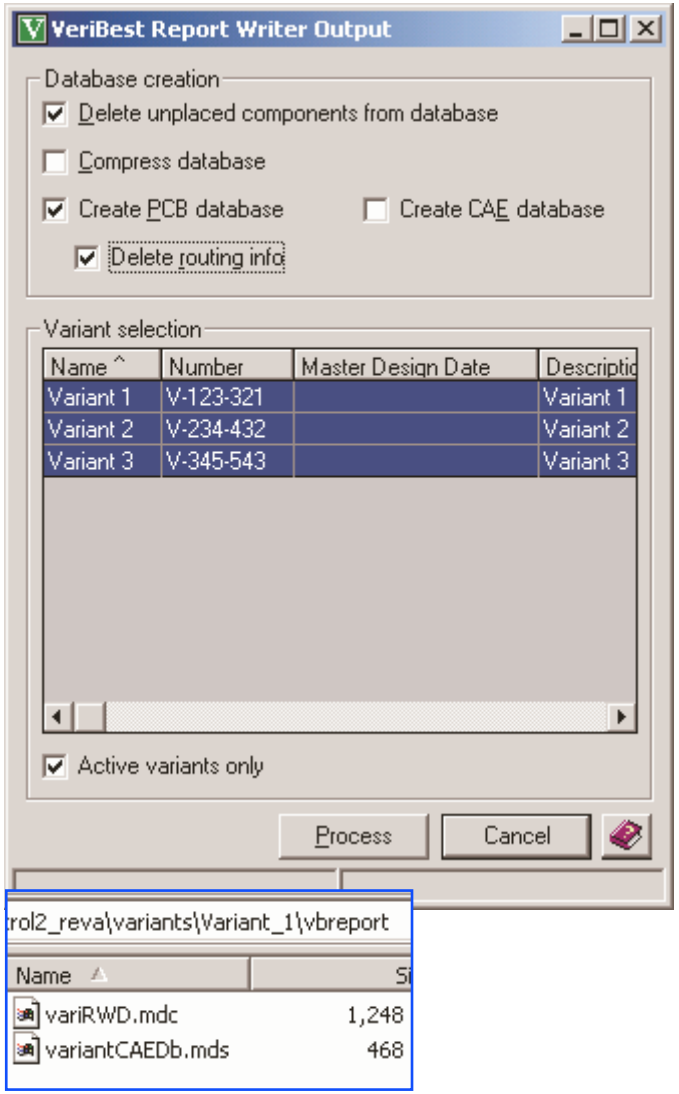


Variant Padstack Data

- **Padstacks can be replaced with a different Padstack definition during Output > CAD process.**
  - **In the Central Library - Padstack Editor, create a new Padstack with the same name as the original Padstack with a suffix on the name - "VMGR_UNPL"**
  - **Edit the new Padstack to be the Padstack in an Variant where the part is unplaced. Perhaps . .**
    - **Smaller pads**
    - **Smaller hole**
    - **Remove Solder mask, etc.**
  - **Output > CAD - Process will replace the original Padstack with the unplaced Padstack in the Variant/**

Variant Report Writer Data

- To create either CAE or CAD Report Writer data for a Variant, you must first create the CAE or CAD Report Writer databases for the master design.
  - The master design databases must not be open during the Variant process.
- In the Variant Manager
  - Output > Report Writer
  - Set data extraction options
  - Select Variants to process
  - Process
- New Report Writer databases will be generated in
  - Variant_project\vbreport



Lab Preview

- **This Module has 3 Labs.**
  - **Lab 1 — Variant Manager Configuration (Optional)**
    - In this lab you take a tour of some of the data management used by the Variant Manager. In fact you don't really do anything, so it is optional.
  - **Lab 2 — Setting Up Variants**
    - It is time to do real work. You will use the Variant Manager to create Variant Definitions for the Cont2_reva database. There will be three Variants with simple changes in each one.
  - **Lab 3 — Variant Output**
    - CAE, CAD and Report Writer output. Oh, you will be doing some experimentation with the CAE output.

Fablink XE

Appendix E

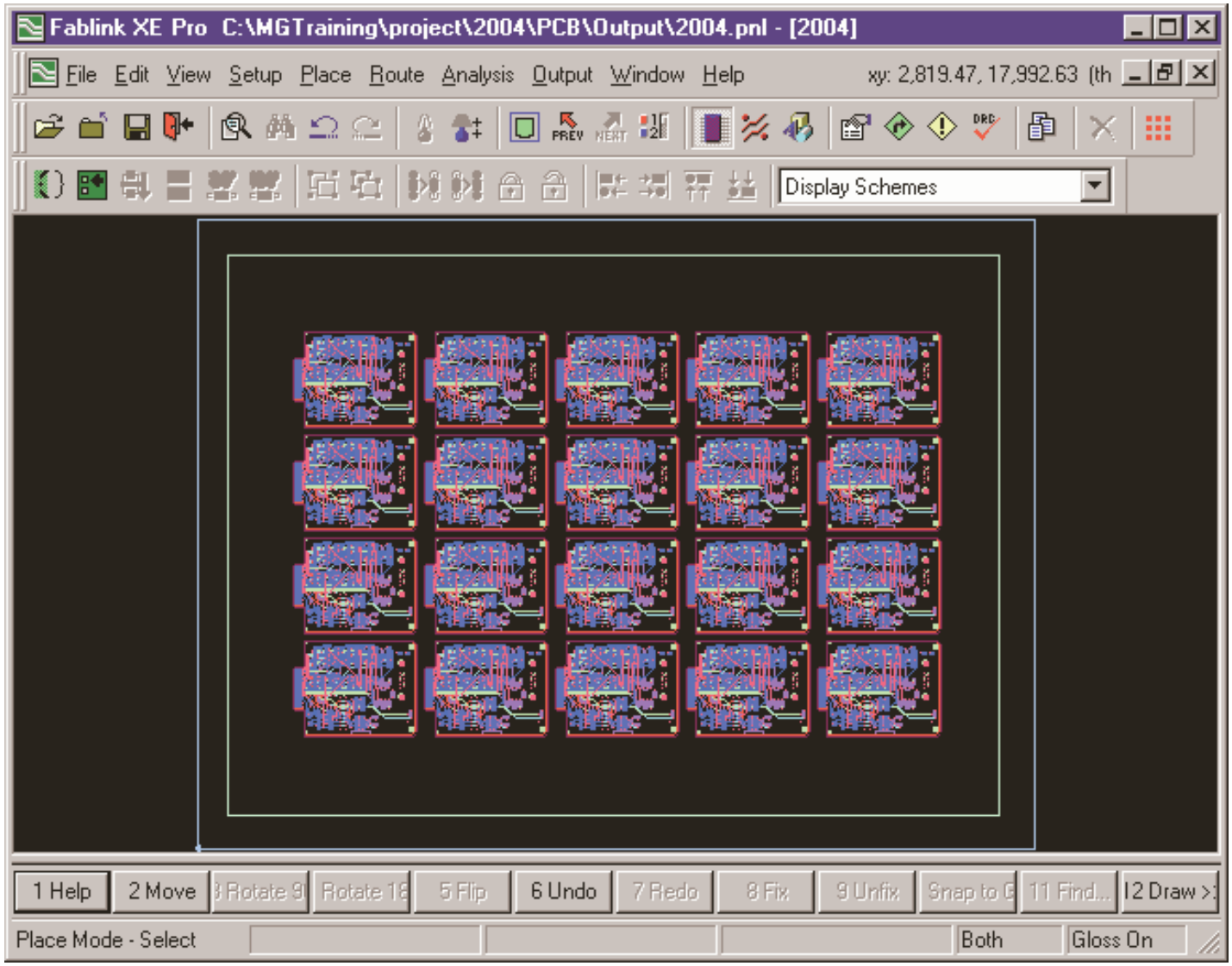
Using Fablink XE

Objectives

Upon completion of this module, you will be able to:

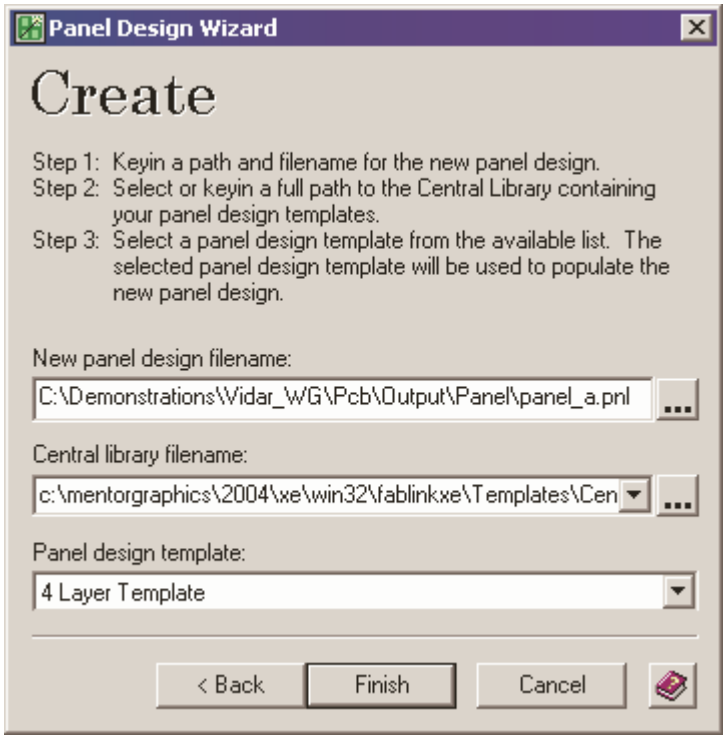
- **Create new panel templates**
- **Generate panel cells**
- **Validate a panel design**
- **Process a design for panelization**
- **Generate copper balancing**
- **Create PDF output drawings**

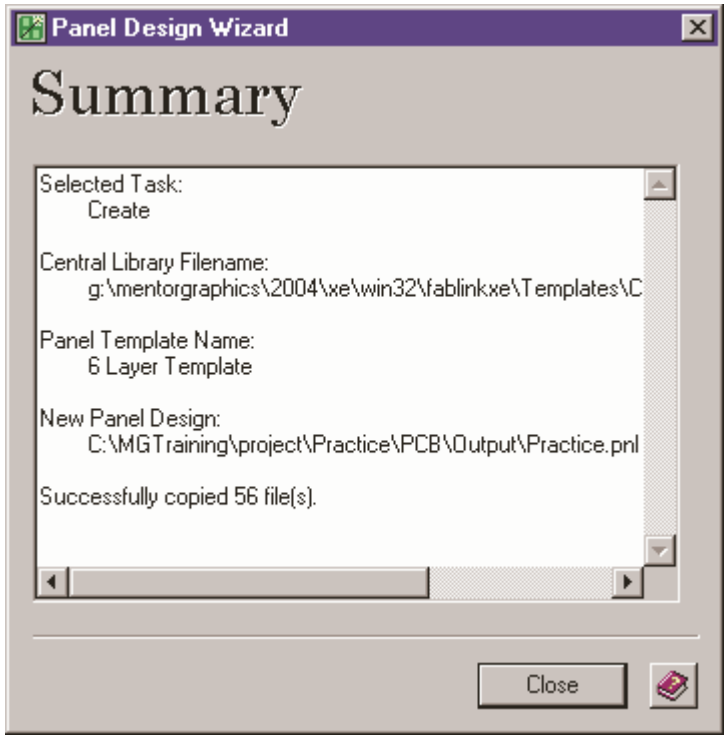
What Is Fablink XE?



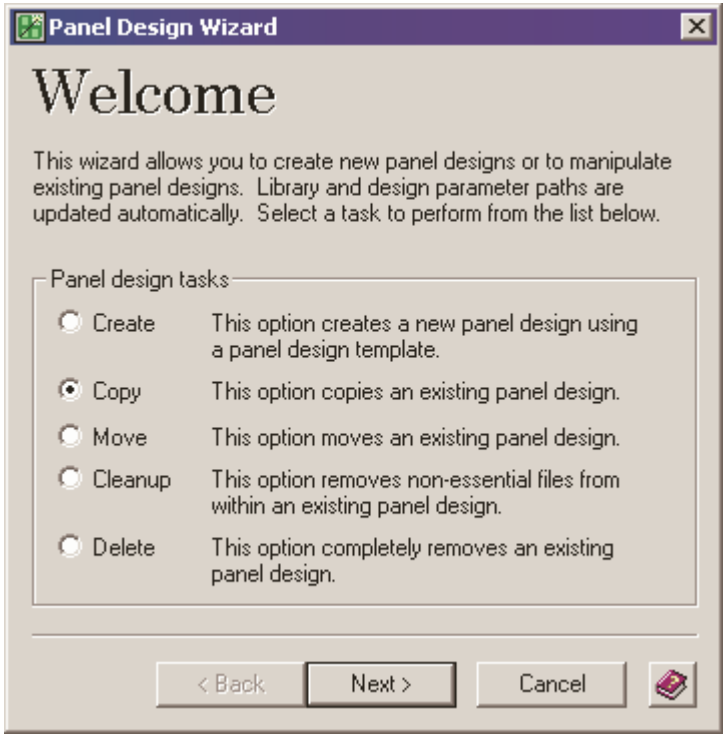
Panel Creation

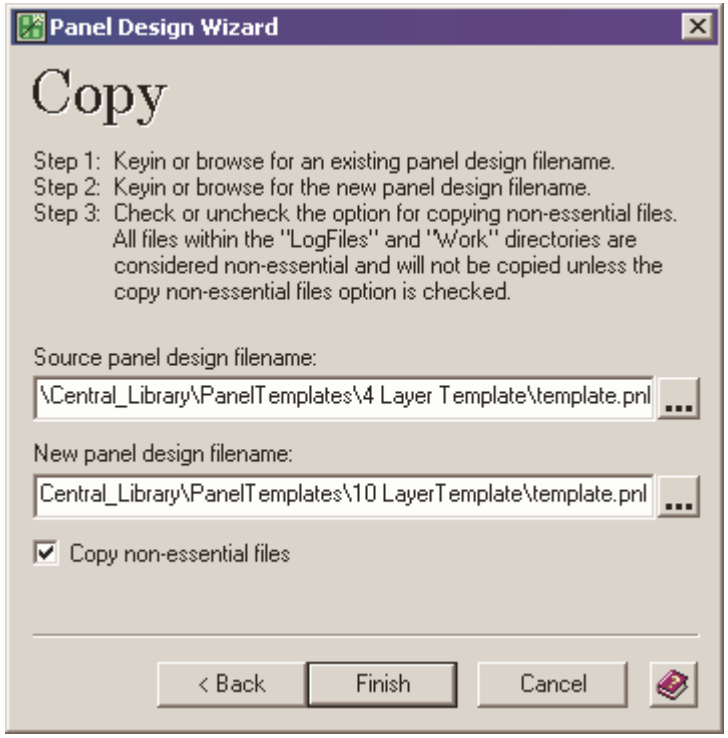
File > New





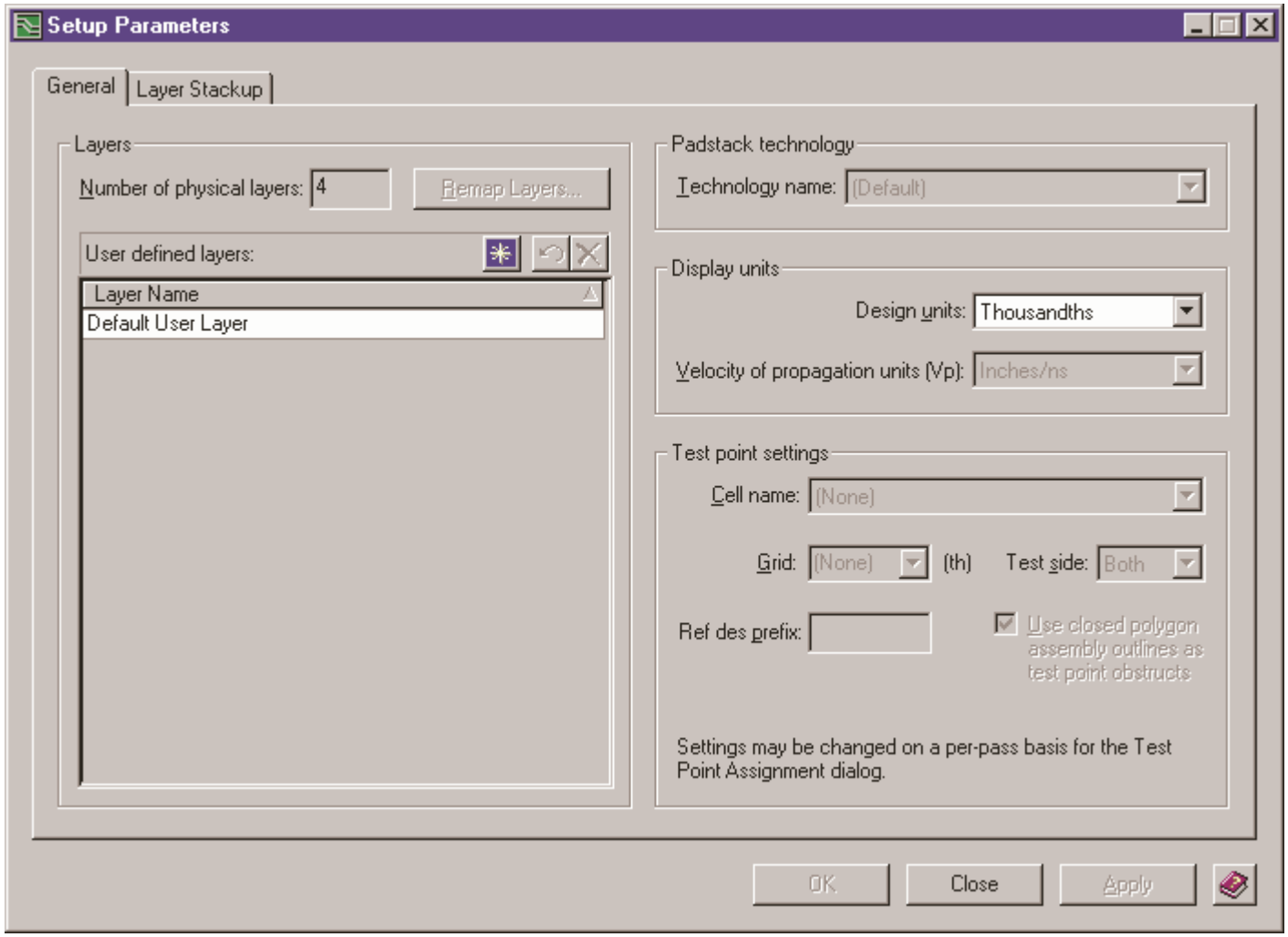
Copying Panels





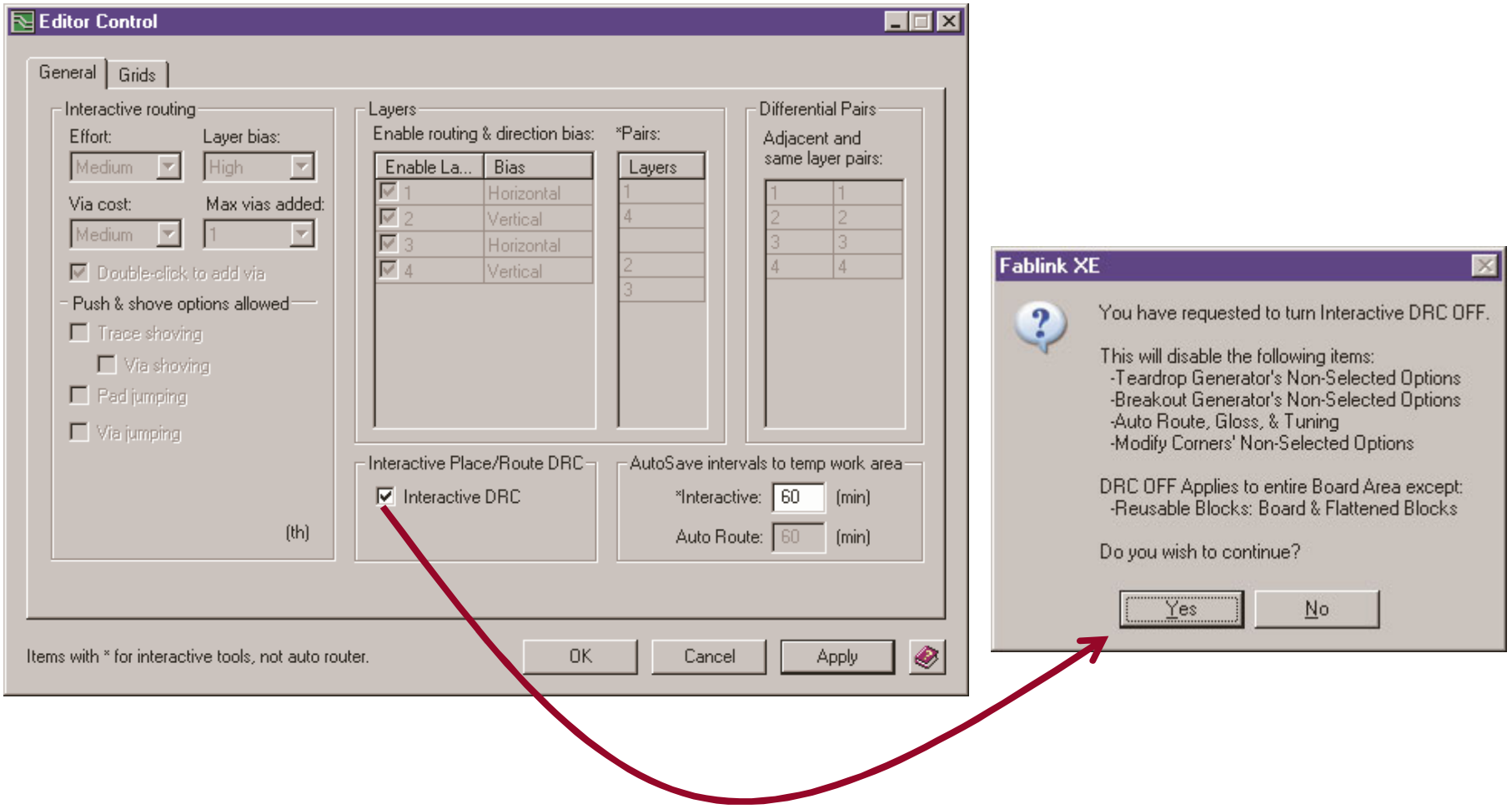
Parameter Setup

Setup > Setup Parameters



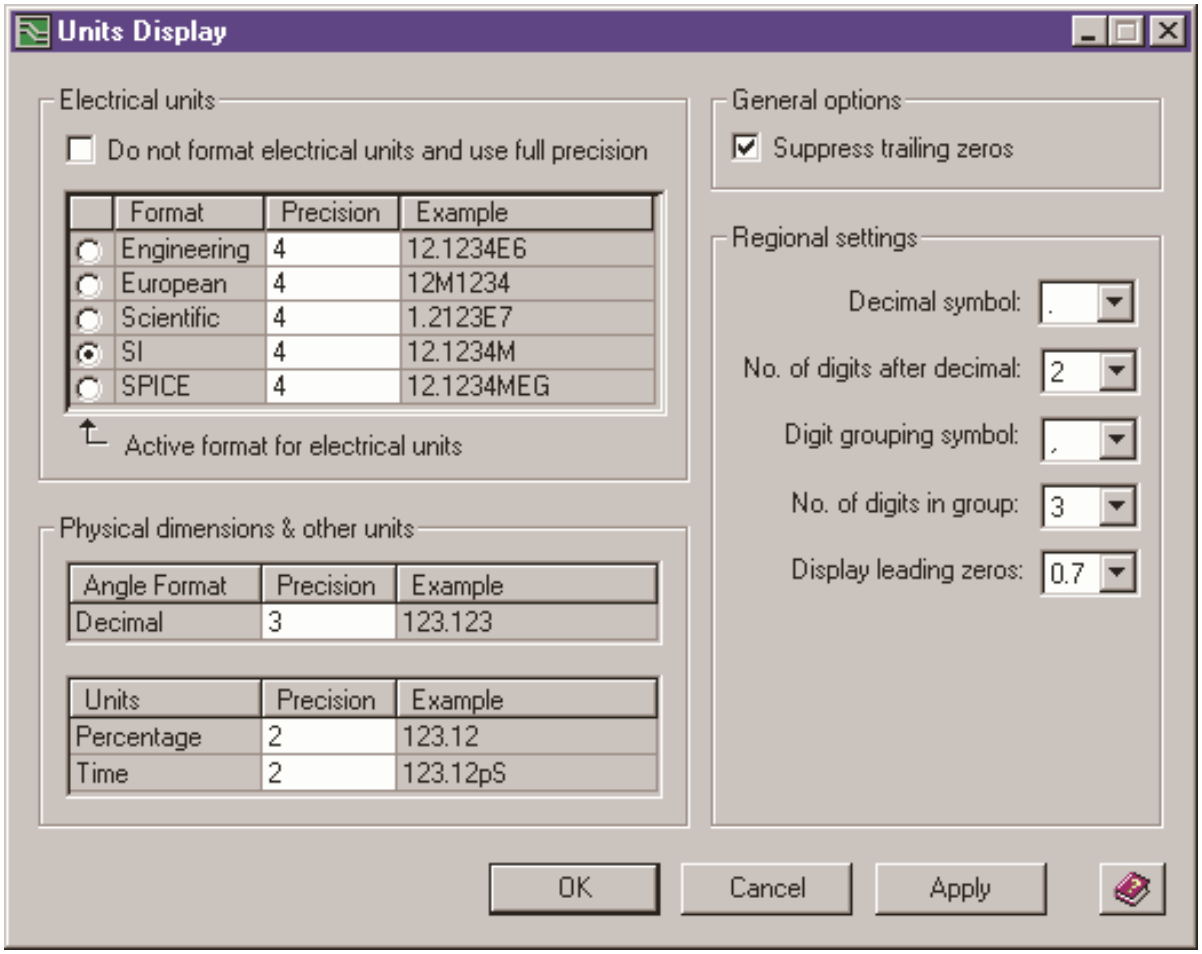
Parameter Setup (Cont.)

Setup > Editor Control



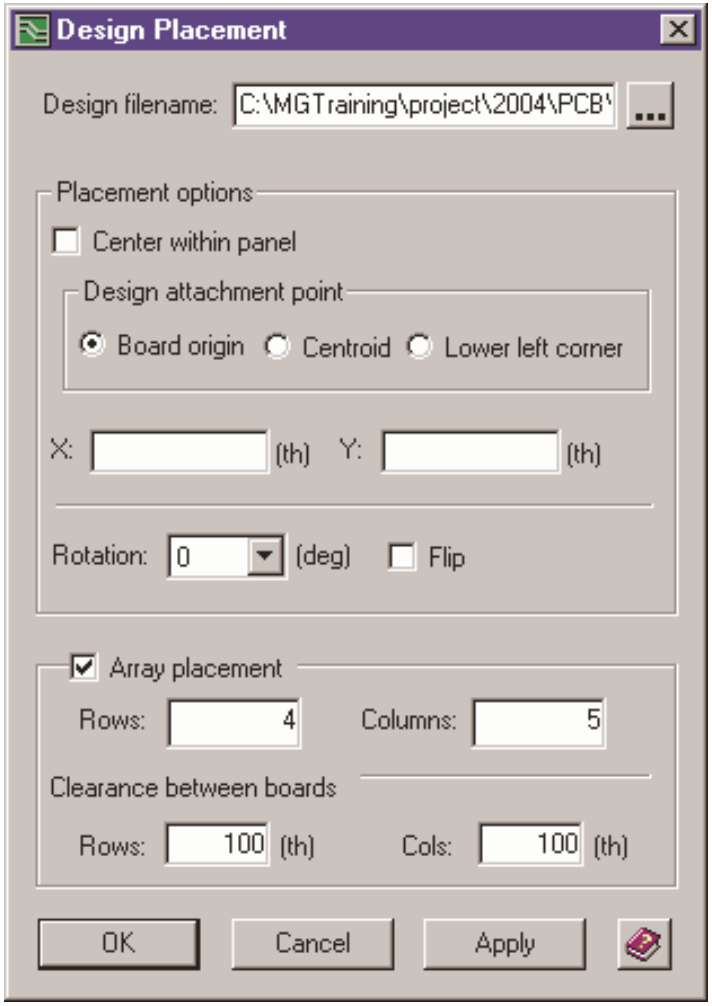
Setting Unit Precision

Setup > Units Display



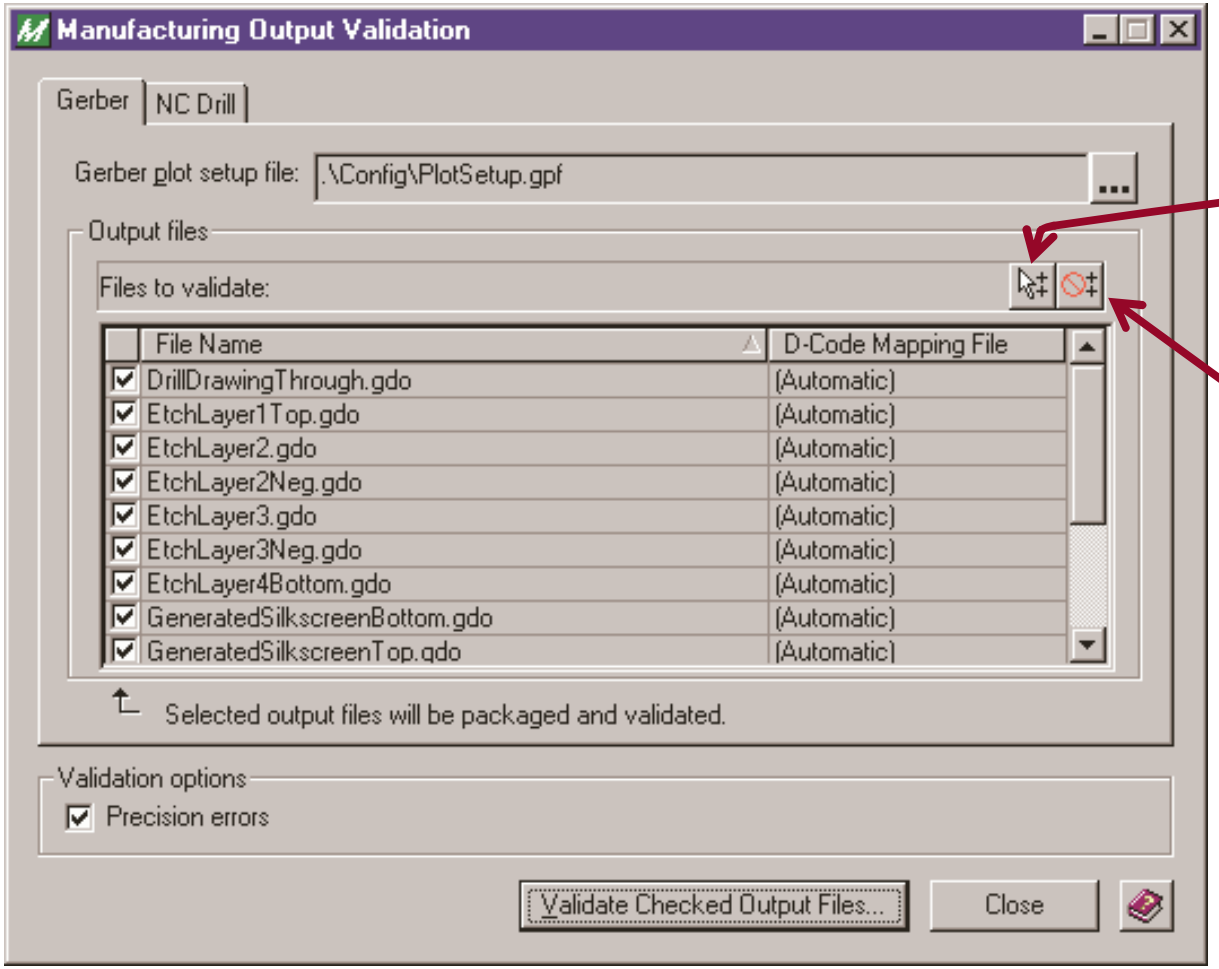
Placing the Design

Place > Design Placement



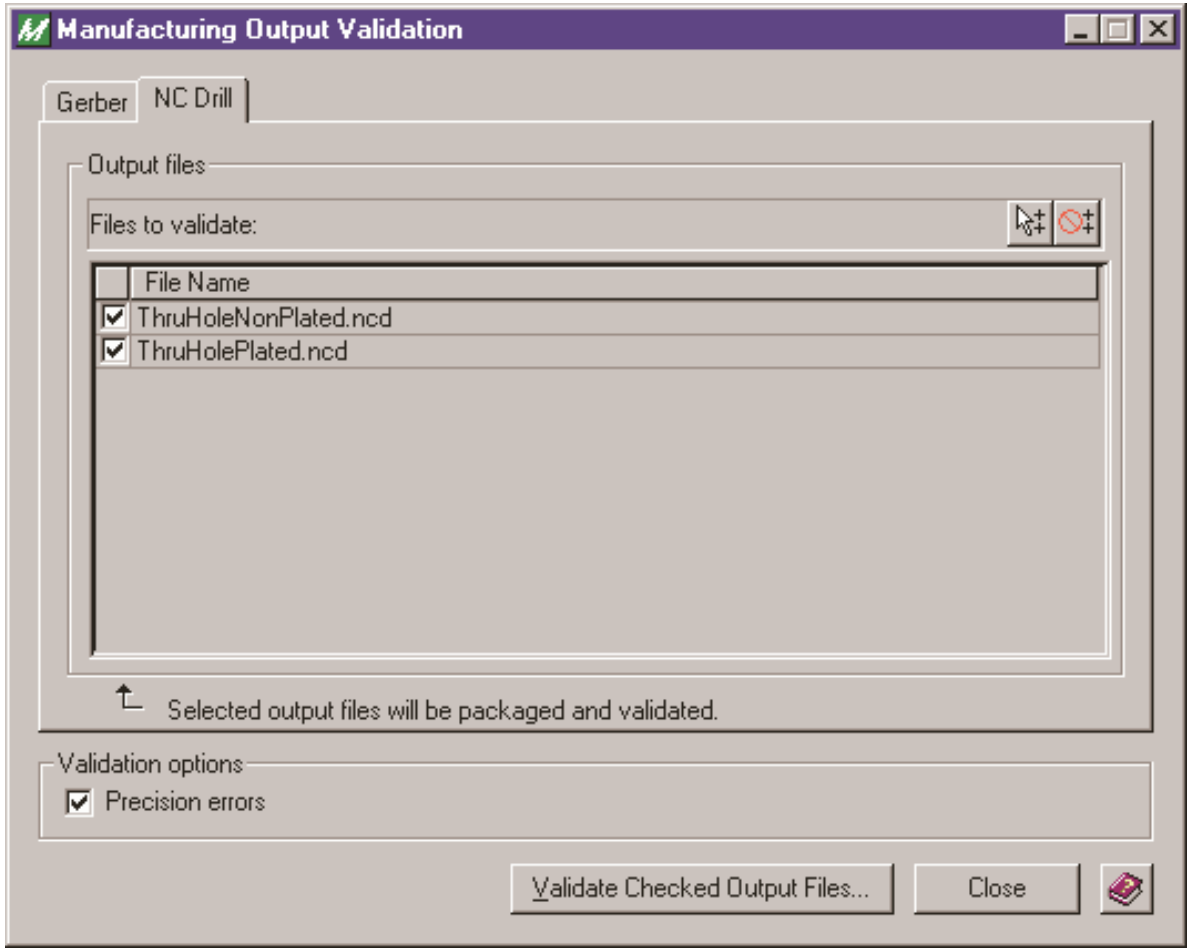
Manufacturing Output Validation

Output > Manufacturing Output Validation



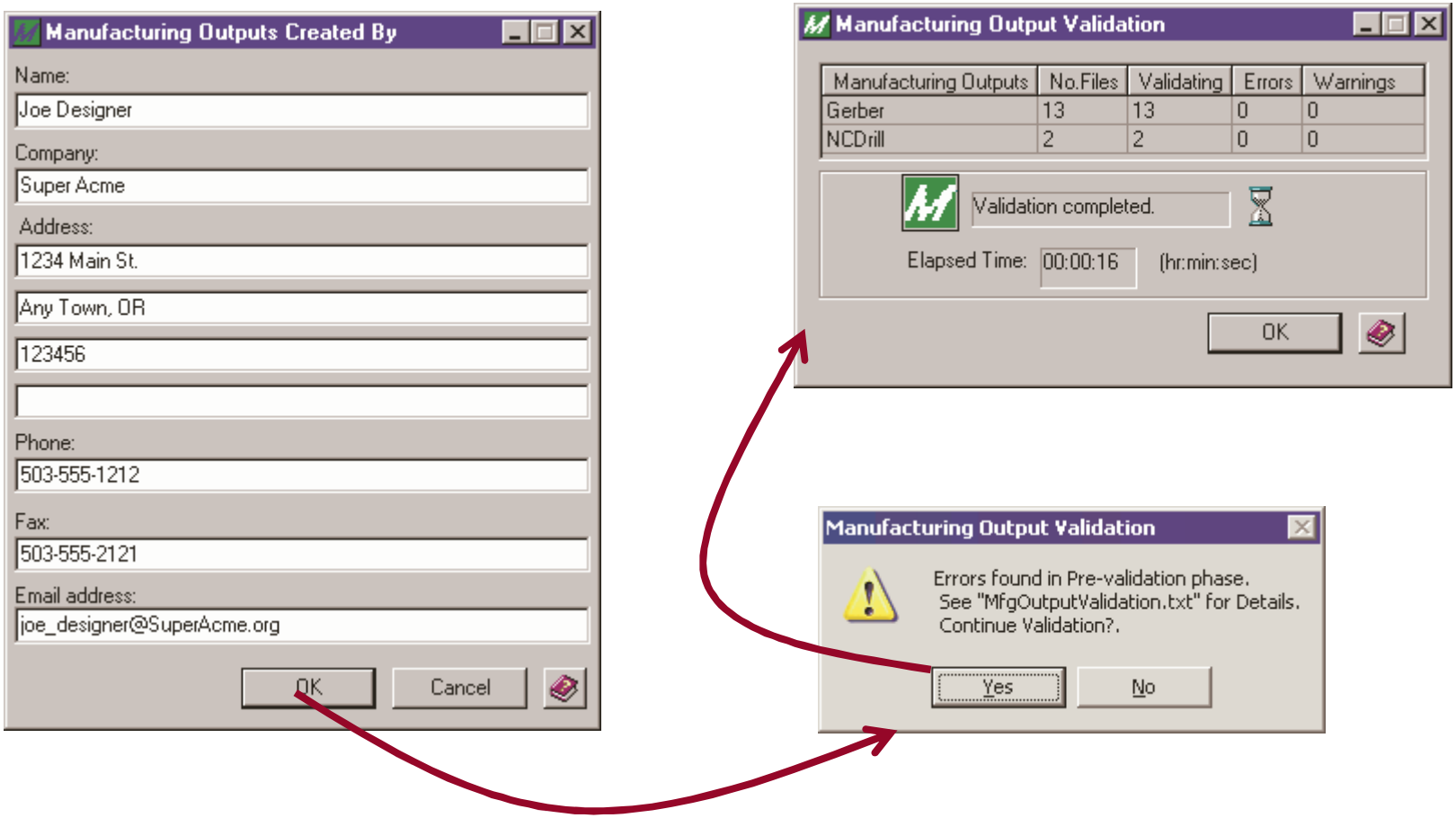
Manufacturing Output Validation (Cont.)

Output > Manufacturing Output Validation



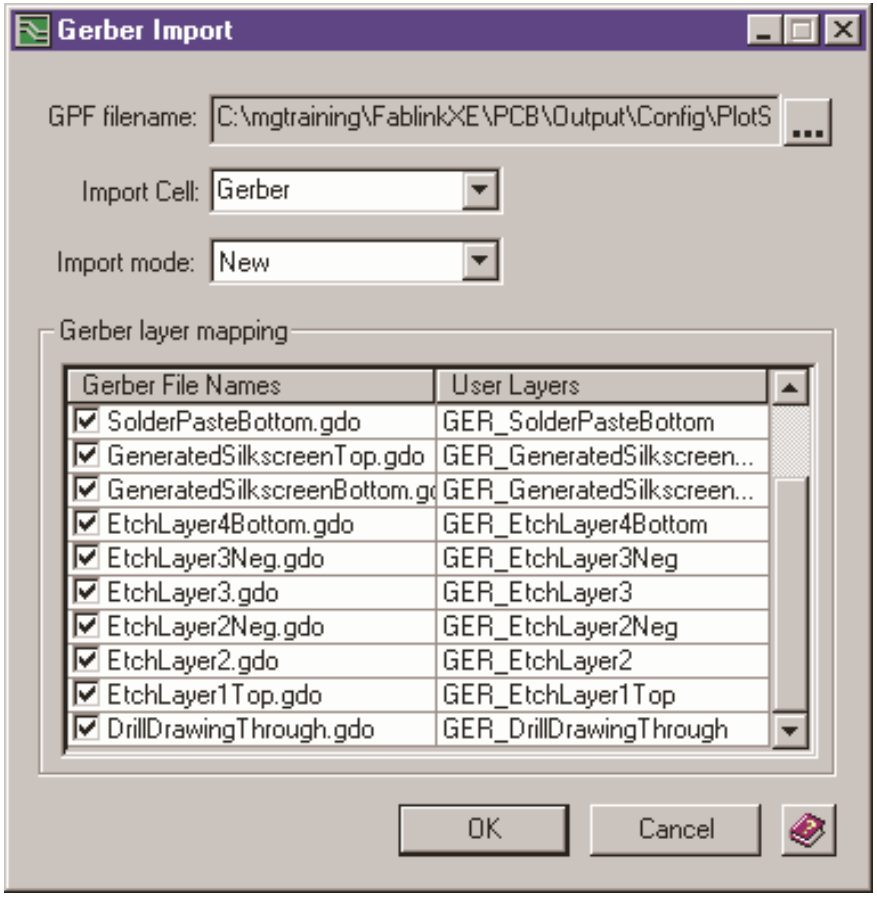
Manufacturing Output Validation (Cont.)

Output > Manufacturing Output Validation



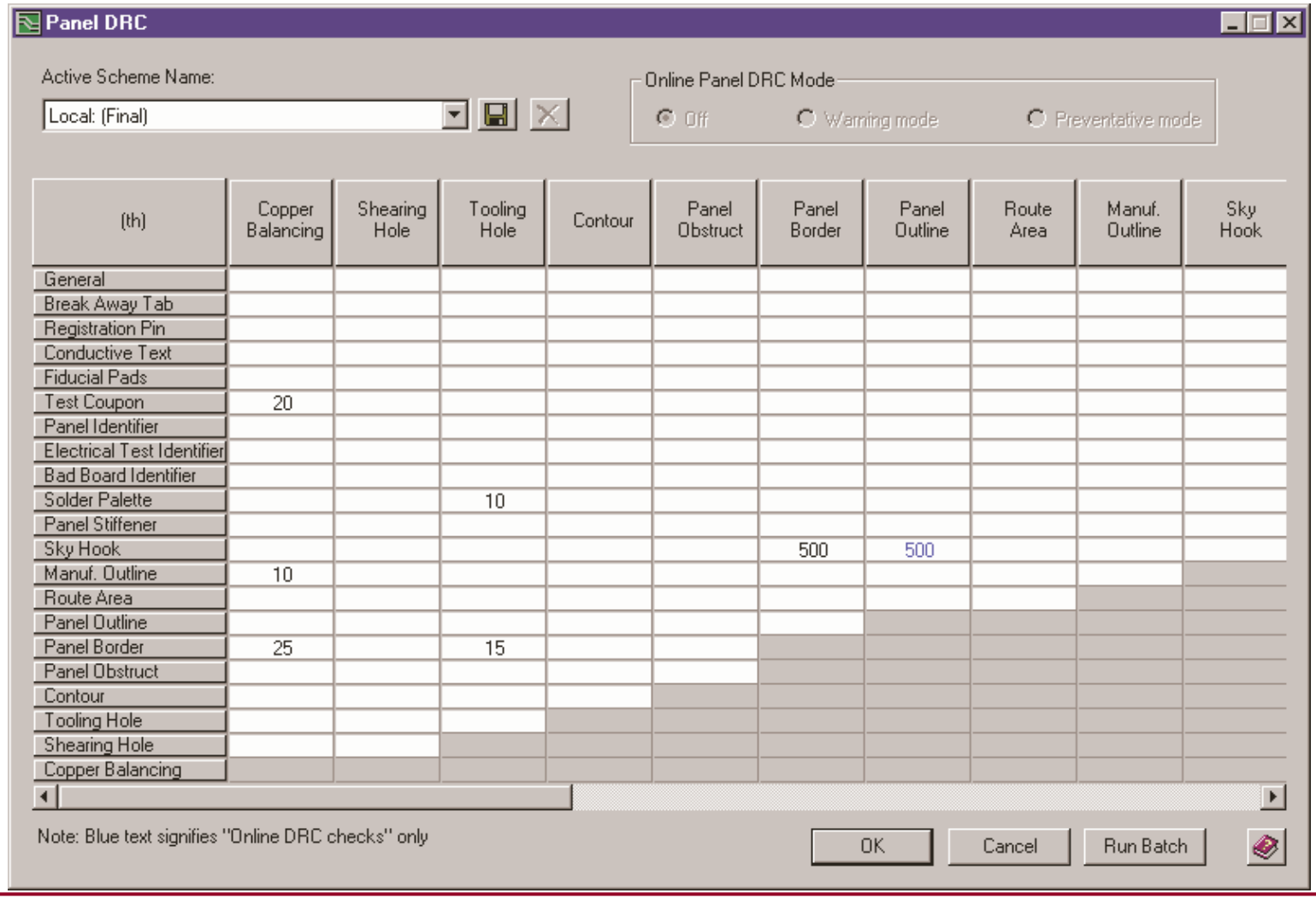
Importing Gerber Data

File > Import > Gerber



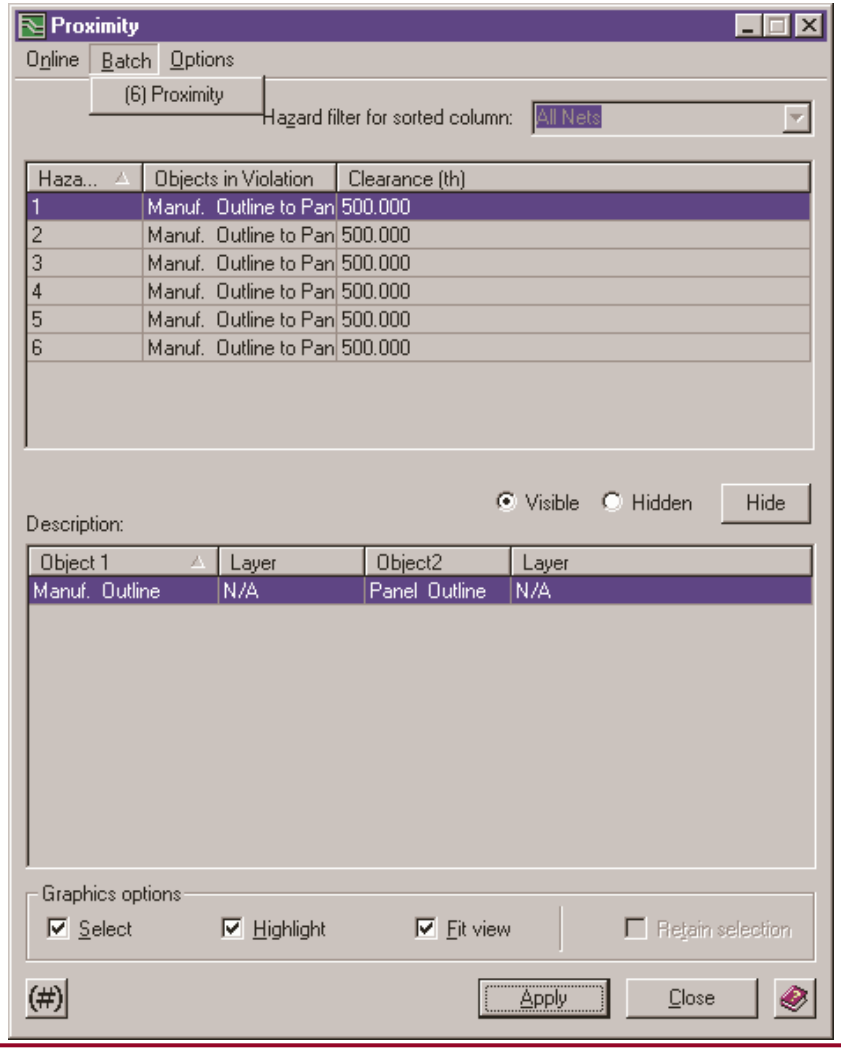
Specifying DRC Rules

Analysis > Panel DRC

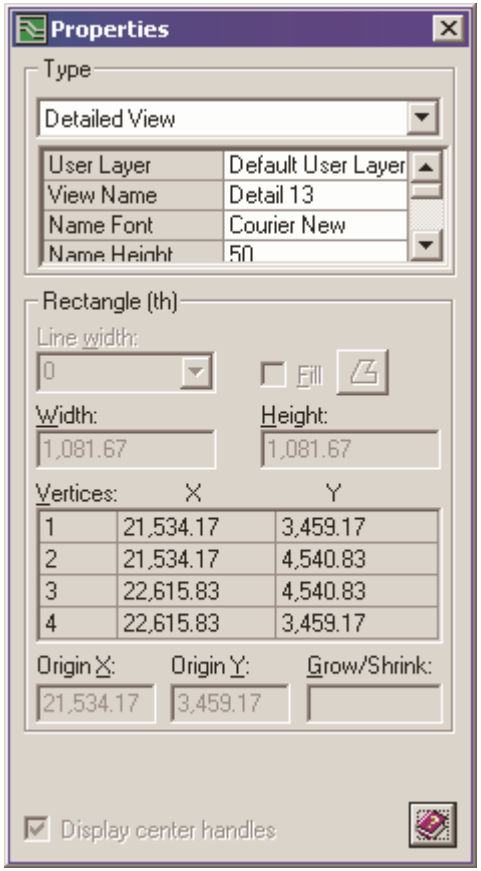


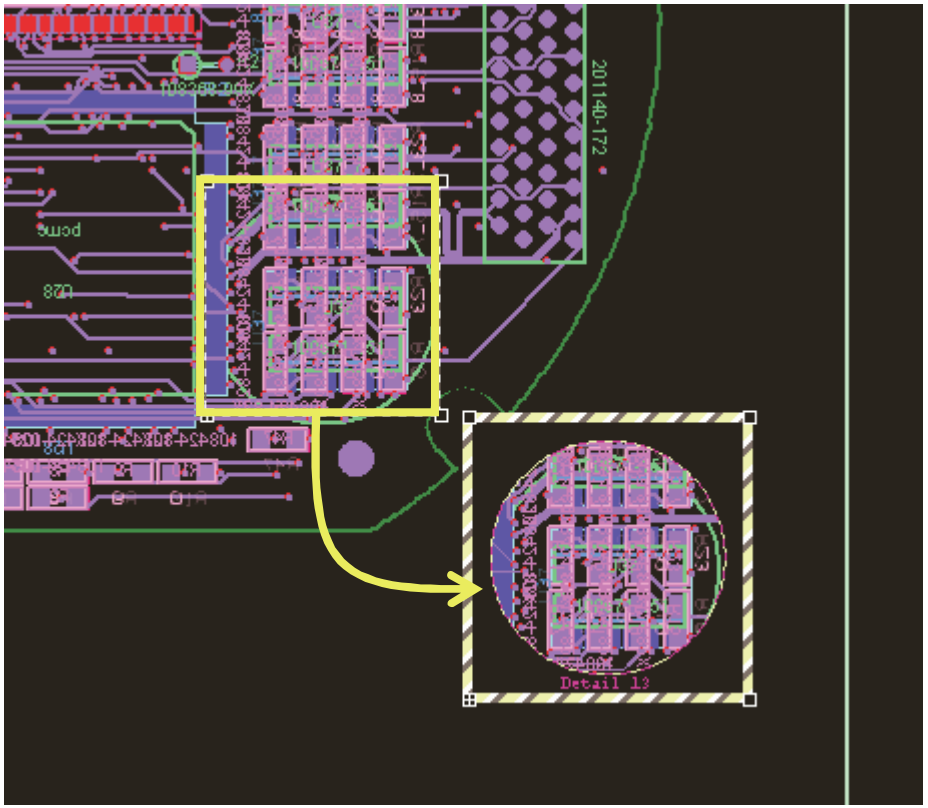
Hazard Analysis

Analysis > Review Hazards 



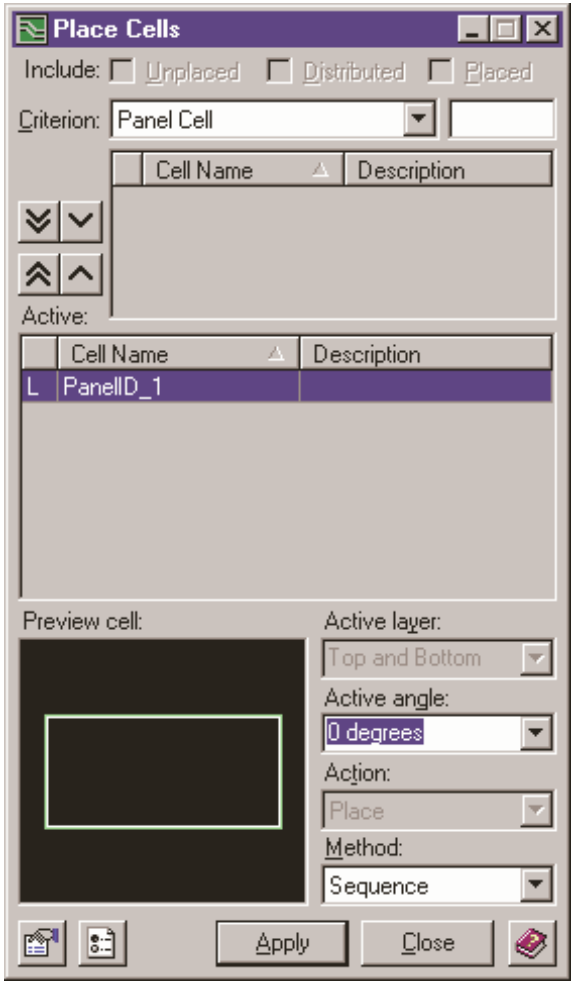
Detailed Views

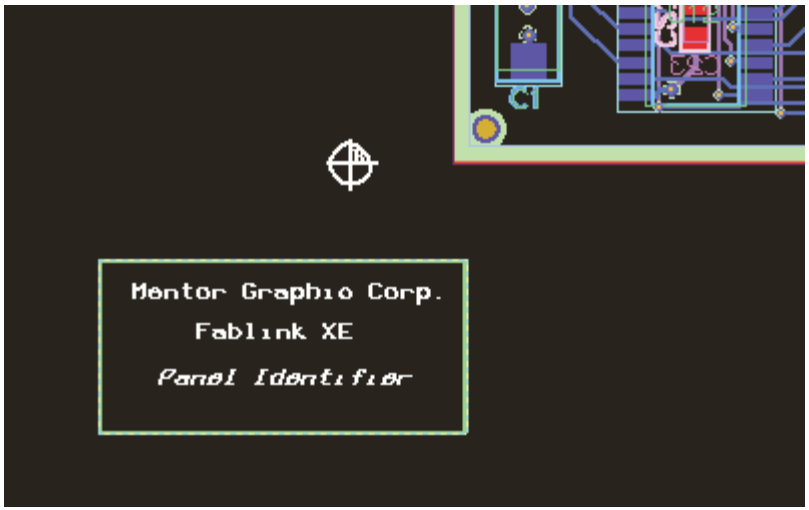




Panel Cells

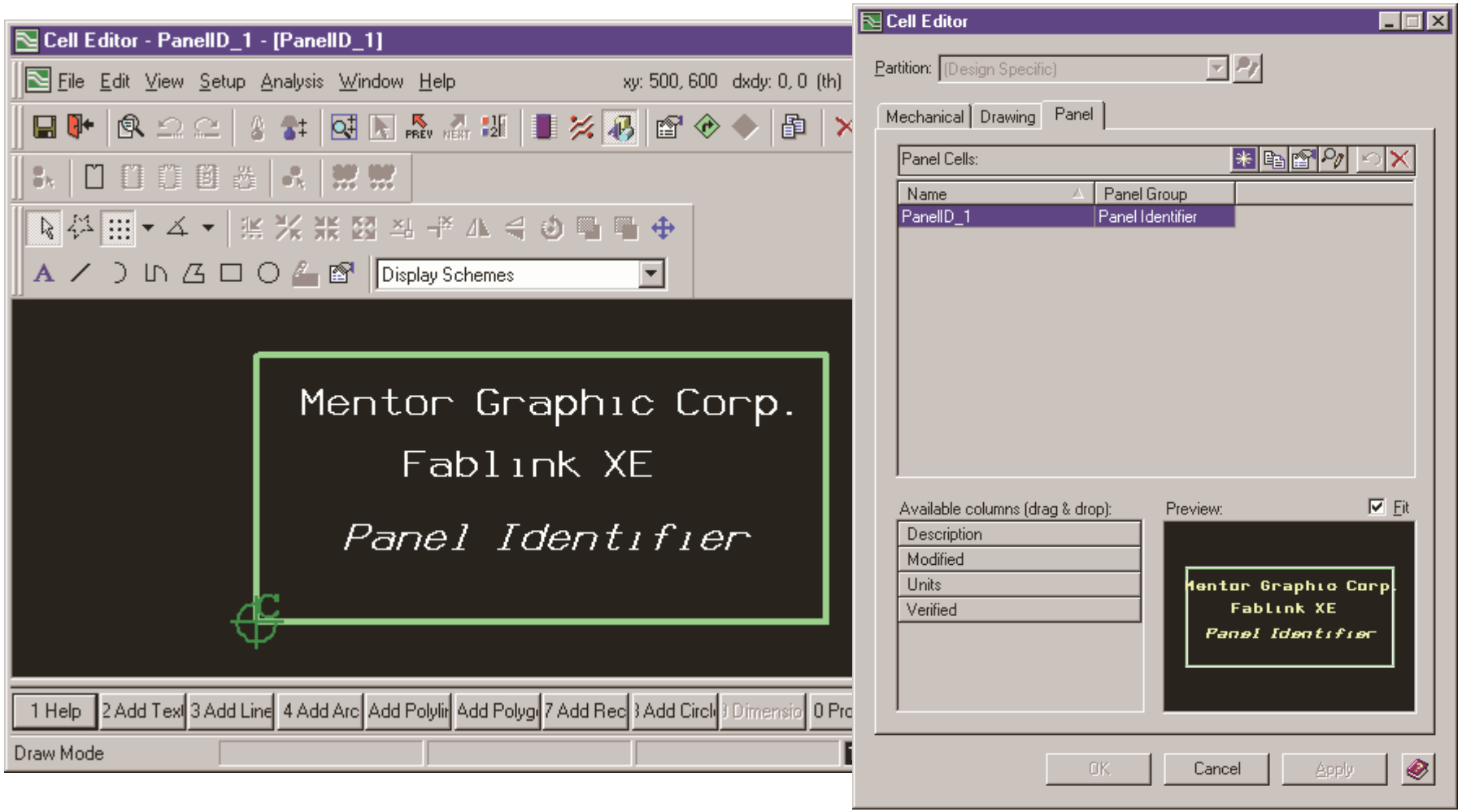
Place > Place Cells



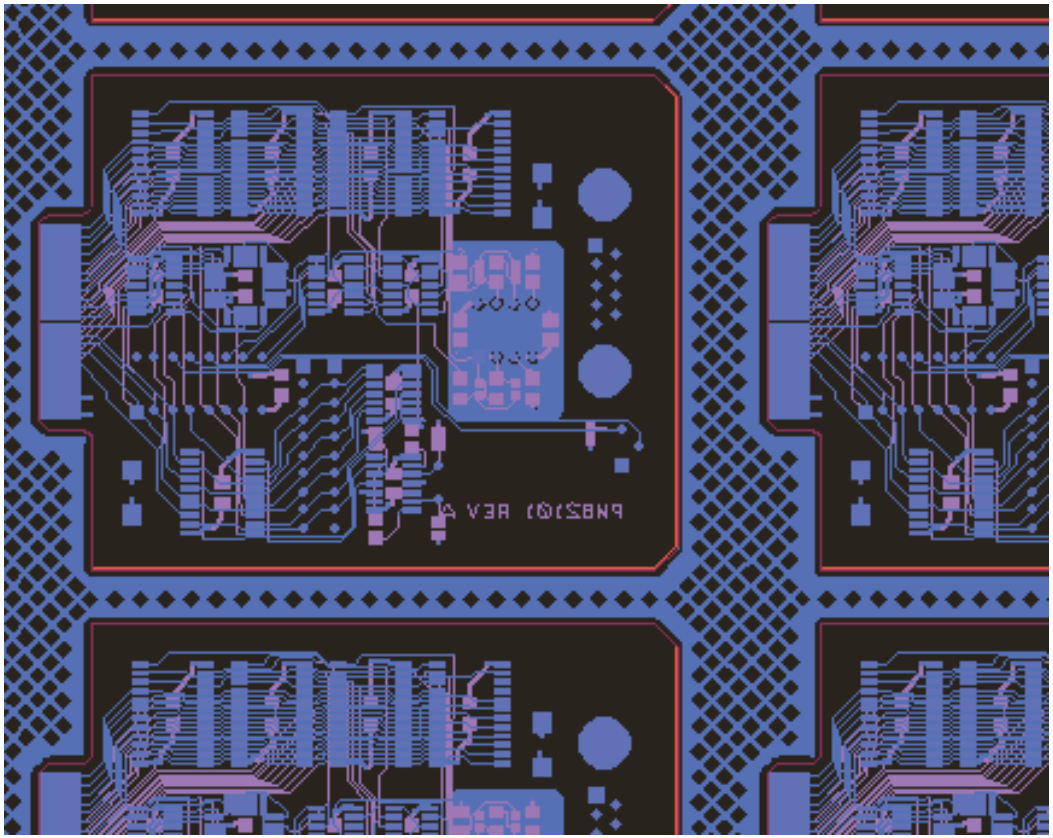


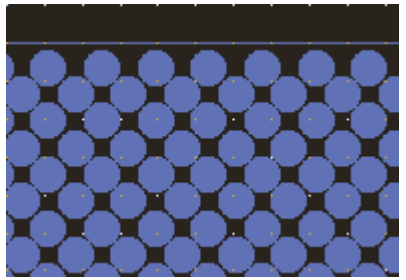
Creating Panel Cells

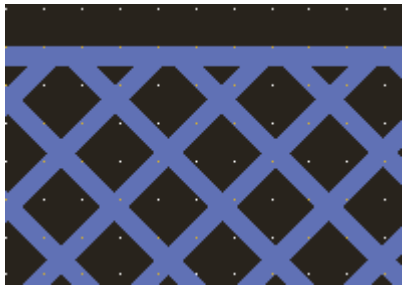
Setup > Cell Editor 



Copper Balancing

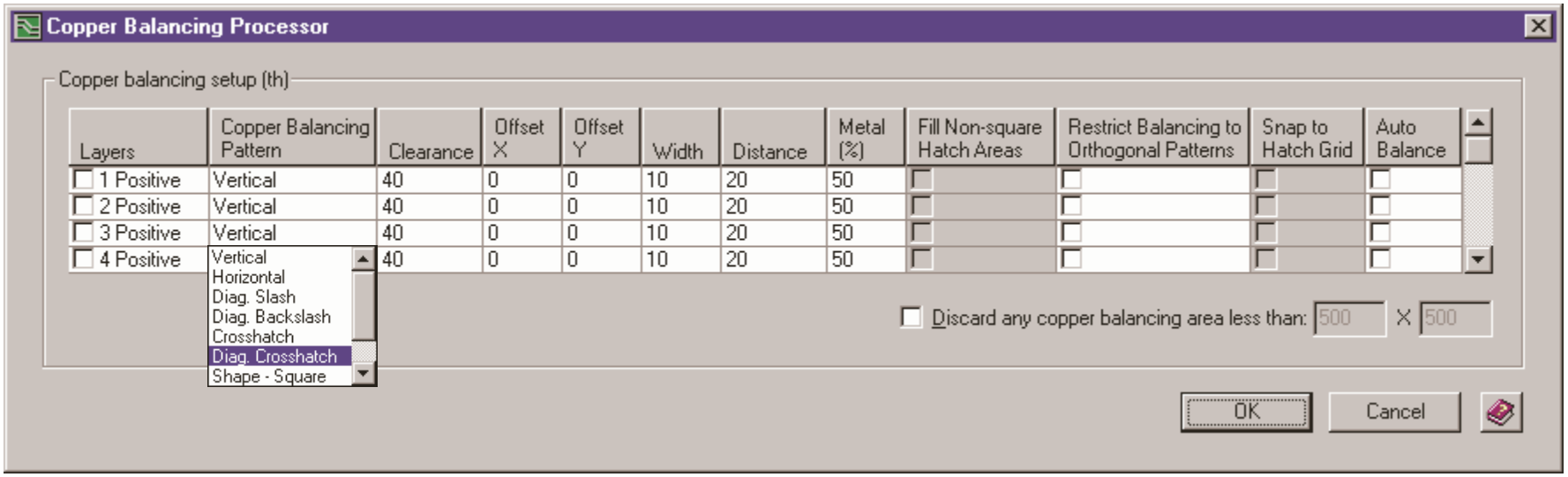




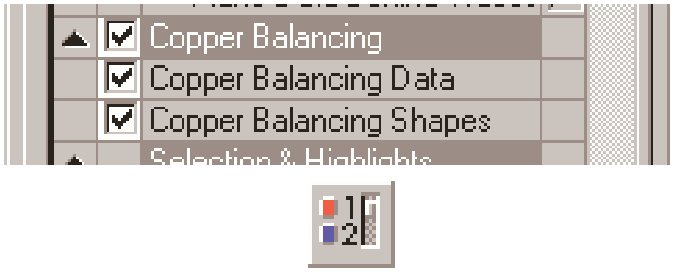


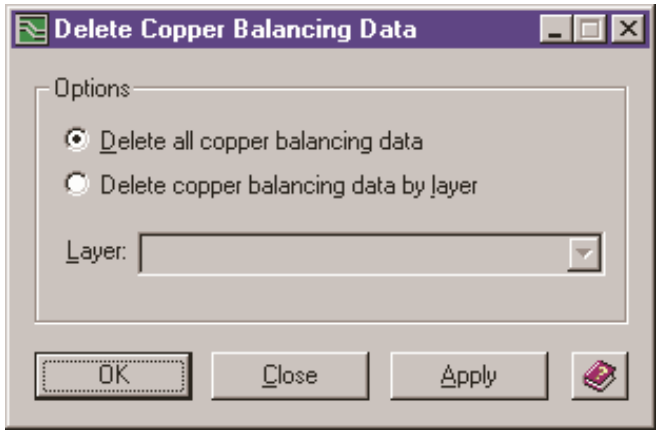
Copper Balancing (Cont.)

Route > Copper Balancing > Processor



View > Display Control > Layers





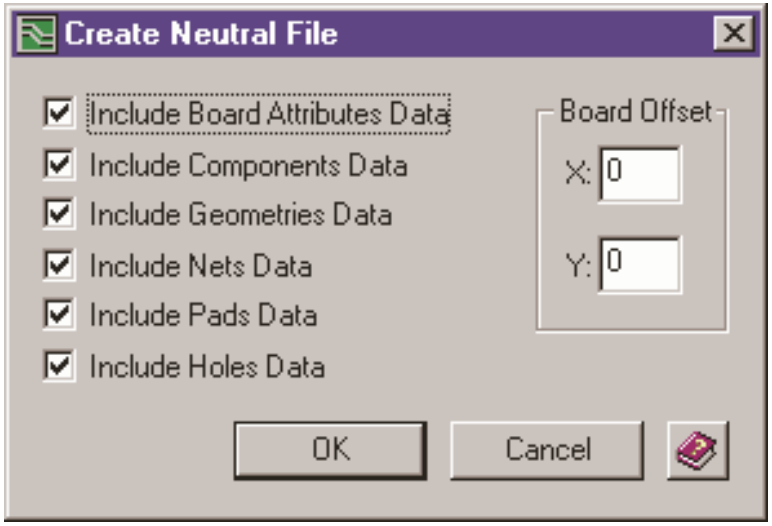
Panel Status (Partial)

Output > Panel Status 

```
NC Drill
   Through-hole Vias ..... 97
   Blind Vias ............ 0
   Buried Vias ........... 0
   Shearing Holes ........ 0
   Tooling Holes ......... 0
Panel Objects
   General ............... 0
   Panel Stiffeners ...... 0
   Bad Board Identifiers ..... 0
   Electrical Test Identifiers . 0
   Panel Identifiers ..... 0
   Test Coupons .......... 0
   Registration Pins ..... 0

Copper Balancing(Panel)
   Layer 1 ............... Yes
   Layer 2 ............... Yes
   Layer 3 ............... No
   Layer 4 ............... No
   Layer 5 ............... Yes
   Layer 6 ............... Yes

General Panel Data

Layers  ................... 6
    Layer 1 is a signal layer
    Layer 2 is a signal layer
    Layer 3 is a Negative Plane Layer with nets
        GND
```

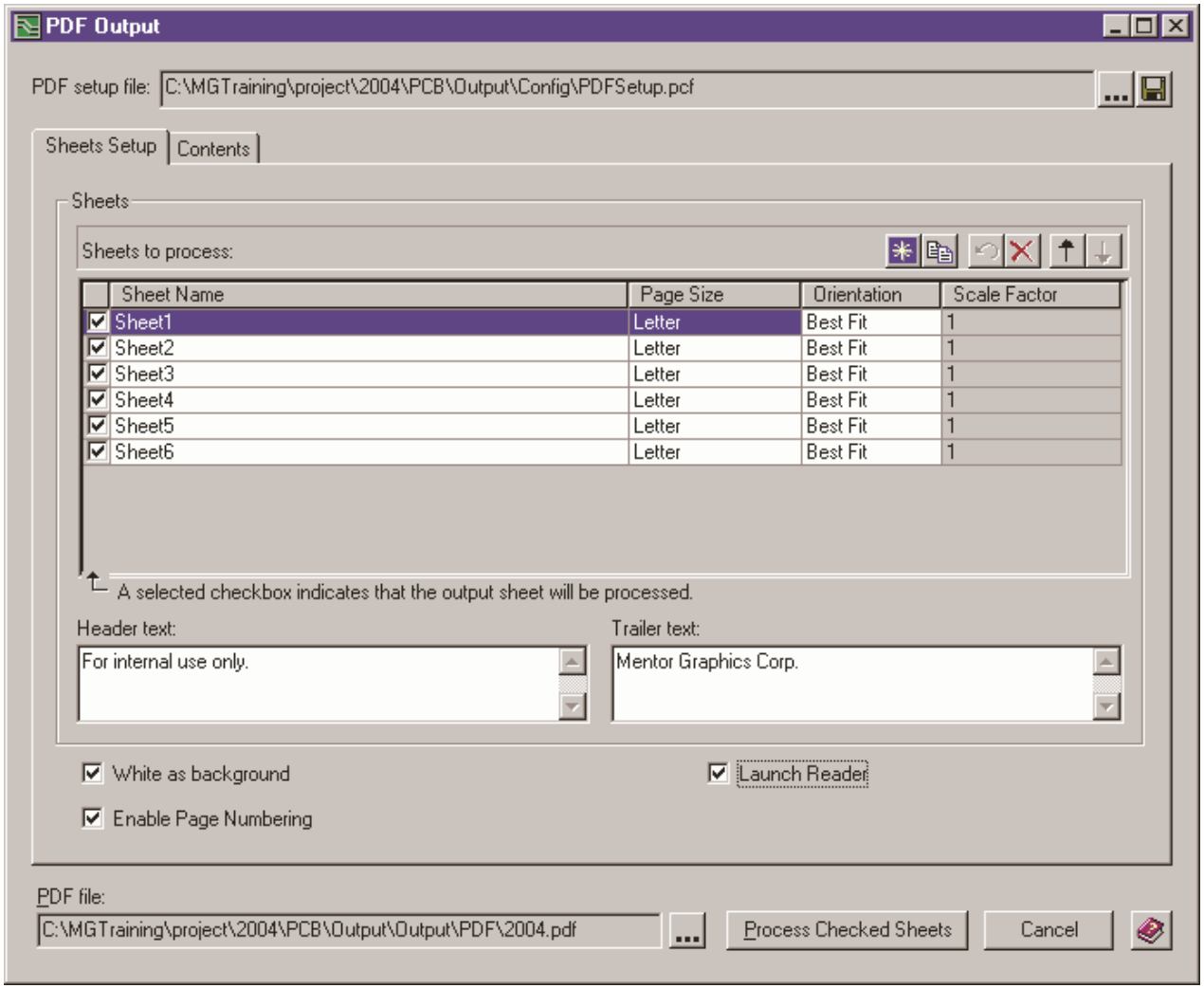
Creating Neutral Files

Output > Neutral File



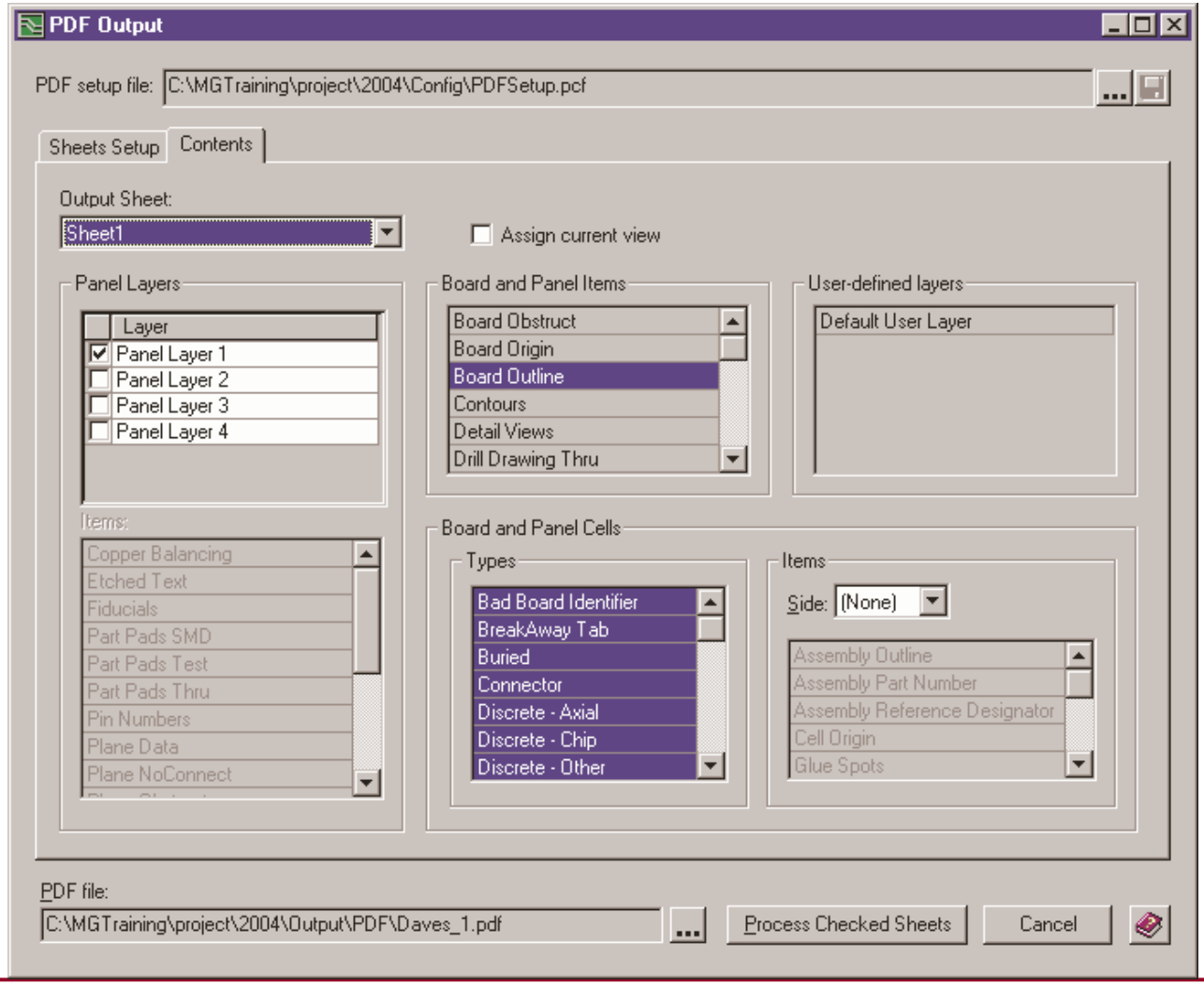
PDF Drawings

Output > PDF



PDF Drawings (Cont.)

Output > PDF



Lab Preview

- **This exercise has one lab.**
  - **Exercise 1: Creating the basic template**
  - **Exercise 2: Validating your design**
  - **Exercise 3:Placing the design**
  - **Exercise 4: Creating Detail Views**
  - **Exercise 5: Creating and placing cells**
  - **Exercise 6: Copper Balancing**
  - **Exercise 7: Creating PDF output**