Testpoint System

Related Videos

Testpoints/Testpoint Manager

Contents

Testing is an important part of the board manufacturing process. After fabrication, the board is typically tested to ensure no short or open circuits. Once fully populated with all its components, a board is often tested again to ensure signal integrity and device operation. To aide in this process, it is fundamentally beneficial to have a scheme of points on the board – testpoints – which the testing equipment can probe and perform the required tests.

The location of testpoints on a board will depend on factors including the mode of testing (including bare-board fabrication testing, in-circuit assembly testing, etc..) and the method of testing (including automated testing using flying probe and bed-of-nails fixtures, hand testing, etc..). For example, when performing bare-board fabrication testing, the board is not populated and so all pads and vias are 'fair game' when it comes to assigning testpoints. The locations used for testpoints when performing in-circuit assembly testing however, will almost always be different. As the board is populated, you may no longer have probe access to component pads and certainly no access to pads and vias under a component!

Altium Designer provides a powerful system to handle your testpoint needs and enhance the testability of your boards, allowing you to separately assign testpoints for bare-board fabrication testing and/or in-circuit assembly testing as required. Testpoints can be assigned manually or, in a more streamlined and automated fashion, using the Testpoint Manager.

Considering Your Testpoint Strategy

Before jumping into the assignation of pads and vias for use as testpoint locations, it is a good idea to step back and think about what is required. The following are just some pointers to consider when defining a strategy to incorporate testpoints into a design:

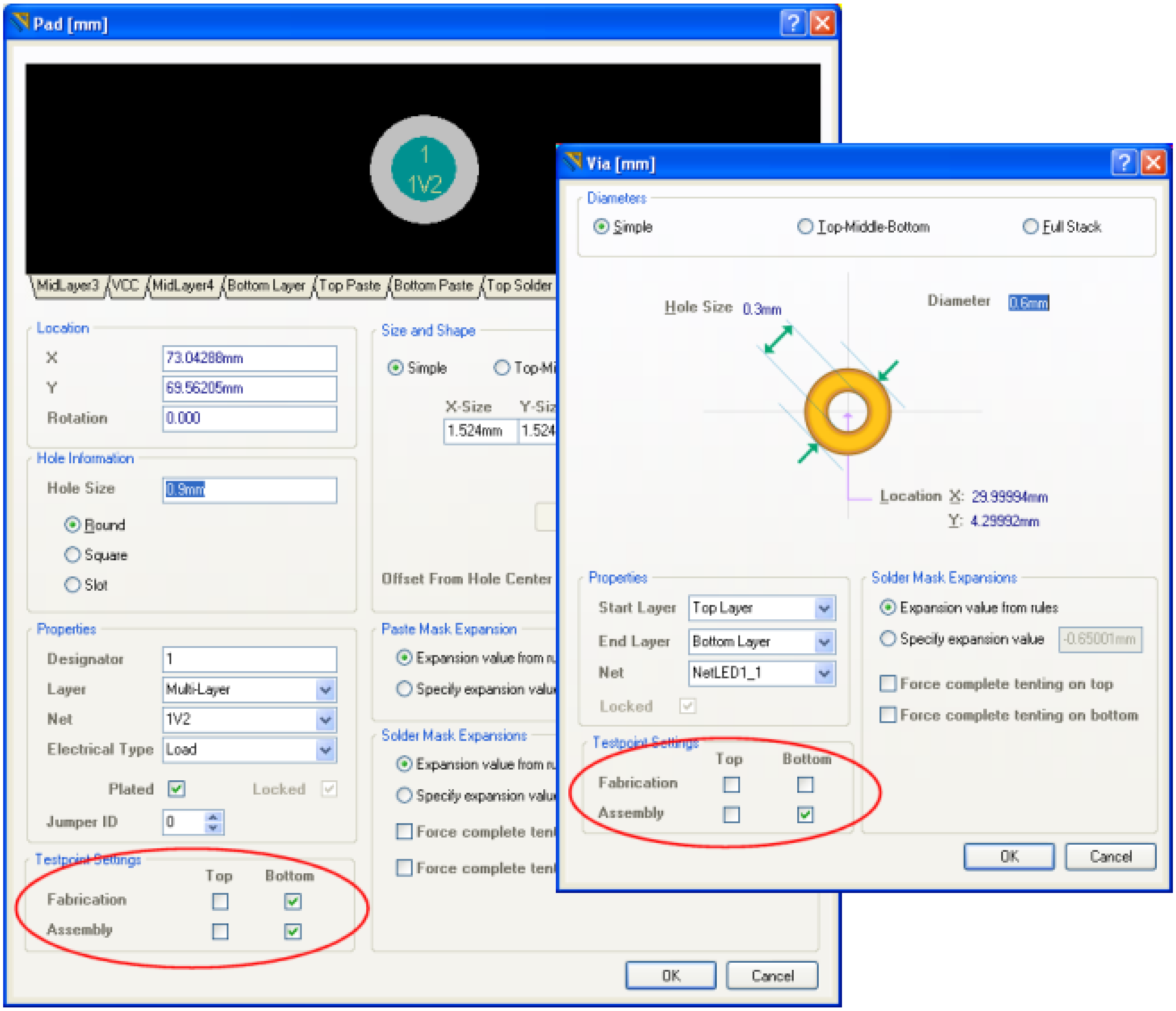
- When choosing the side of the board that testpoints will be allowed on, consideration should be given to the testing processes and associated fixtures that will be used. For example, will the board be probed from the bottom side only, the top side only, or both sides.
- A testpoint underneath a component (on the same side of the board as the component) is usually used at the bare-board testing stage. This should be taken into consideration when planning testpoint locations for assembled board testing.
- It is advisable to locate all testpoints on one side of the board only, using vias to achieve this if necessary. The reason for this lies in the fact that a dual-head test fixture incurs greater cost than a single-head test fixture.

- The more non-standard and complex your pattern of testpoints, the more costly it will be to configure a fixture with which to test the board. The best philosophy is to develop a methodology that will result in generic testability. A well-honed and adaptable testpoint policy will allow different designs to be tested efficiently and cost-effectively.
- Careful consideration should be given to any via tenting requirements of the design. Tenting a testpoint-designated via will effectively block test probe contact. Even partial tenting using a liquid photoimageable (LPI) solder mask will cause contact problems, as the mask liquid will tend to run away through the via hole. Peelable solder mask may indeed be used to provide temporary tenting of such designated vias, but this can often prove quite costly.
- Consult with your fabrication and assembly houses closely to make sure any specific design parameters are taken into account when specifying testpoints. These could include testpoint-to-testpoint clearances and testpoint-to-component clearances that may be more strict than normal placement and routing clearances.

Pad and Via Testpoint Support

Altium Designer provides full support for testpoints, allowing you to specify pads (thru-hole or SMD) and/or vias to be used as testpoint locations in fabrication and/or assembly testing. A Pad or Via is nominated for use as a testpoint by setting its relevant testpoint properties – should it be a fabrication or assembly testpoint, and on which side of the board should it be used as a testpoint. These properties can be found in the *Pad* or *Via* properties dialogs.

To streamline the process and alleviate the need for setting the testpoint properties of pads/vias manually, Altium Designer provides you with a method to automatically assign testpoints based on defined design rules and using the Testpoint Manager. This automated assignment simply sets the relevant testpoint properties for the pad/via in each case. You of course have the option to manually specify testpoints – in essence, handcrafting at the individual pad/via level – giving you full control over the testpoint scheme employed for your board.


Pad [mm]

Location
X 73.04288mm
Y 69.56205mm
Rotation 0.000

Hole Information
Hole Size 0.9mm
● Round
○ Square
○ Slot

Properties
Designator 1
Layer Multi-Layer
Net 1V2
Electrical Type Load
Plated ☑ Locked ☑
Jumper ID 0

Testpoint Settings

	Top	Bottom
Fabrication	□	☑
Assembly	□	☑

Size and Shape
● Simple ○ Top-Mi
X-Size 1.524mm Y-Siz 1.524

Offset From Hole Center

Paste Mask Expansion
● Expansion value from ru
○ Specify expansion valu

Solder Mask Expansions
● Expansion value from ru
○ Specify expansion valu
□ Force complete tent
□ Force complete tent

Via [mm]

Diameters
● Simple ○ Top-Middle-Bottom ○ Full Stack

Hole Size 0.3mm
Diameter 0.6mm
Location X: 29.99994mm
Y: 4.29992mm

Properties
Start Layer Top Layer
End Layer Bottom Layer
Net NetLED1_1
Locked ☑

Solder Mask Expansions
● Expansion value from rules
○ Specify expansion value -0.65001mm
□ Force complete tenting on top
□ Force complete tenting on bottom

Testpoint Settings

	Top	Bottom
Fabrication	□	□
Assembly	□	☑

A pad or via is specified for use as a testpoint through the relevant options in its associated properties dialog - a process that is most efficiently performed through use of the Testpoint Manager.

> When opening PCB designs created in a release of the software prior to the Summer 09 release, any enabled testpoint options will become enabled Fabrication testpoint options.

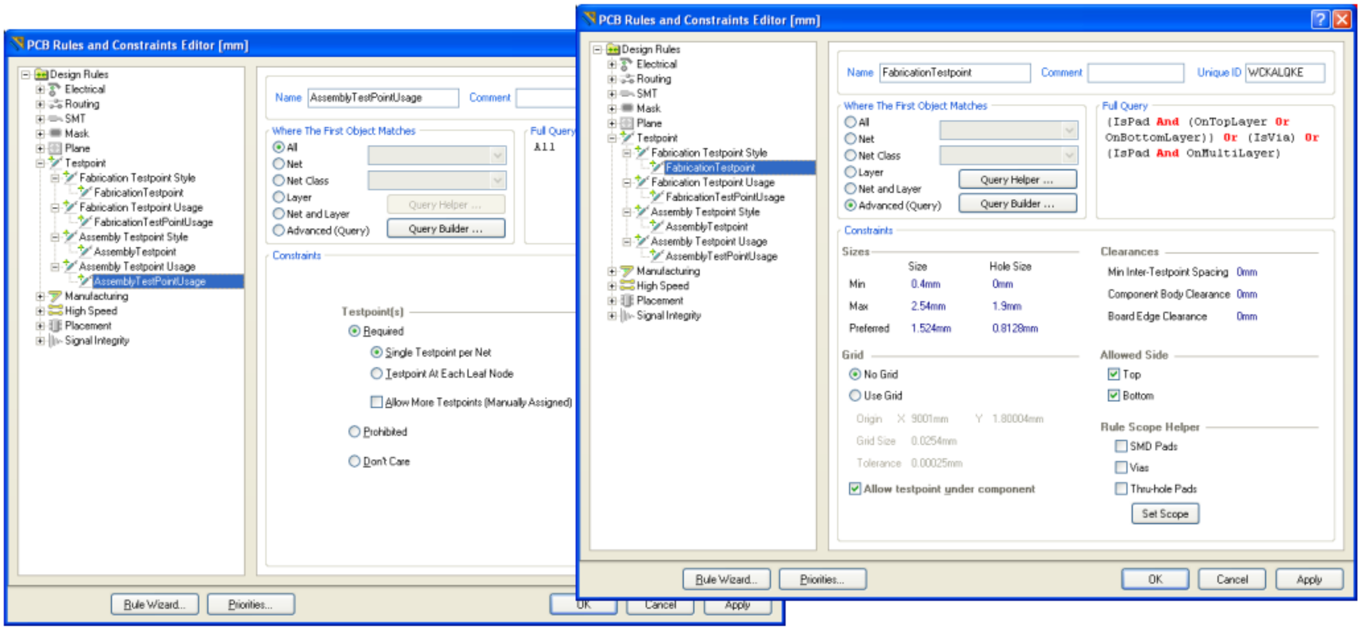
Design Rules

The constraints of a PCB design should be thought out and implemented as a well-honed set of design rules. To implement a successful testpoint scheme – where all defined testpoints can be accessed and used as part of the bare-board and/or in-circuit testing, governing constraints must be put in place. To this end, the following rule types are definable as part of the PCB Editor's Design Rules system:

- Fabrication Testpoint Style

- Fabrication Testpoint Usage
- Assembly Testpoint Style
- Assembly Testpoint Usage

Access and define rules of these types from the *PCB Rules and Constraints Editor* dialog (**Design»Design Rules**).



PCB Rules and Constraints Editor [mm]

Name: AssemblyTestPointUsage
Comment:

Where The First Object Matches: ● All ○ Net ○ Net Class ○ Layer ○ Net and Layer ○ Advanced (Query)

Full Query:

```
All
```

Constraints

Testpoint(s)
● Required
● Single Testpoint per Net
○ Testpoint At Each Leaf Node
□ Allow More Testpoints (Manually Assigned)
○ Prohibited
○ Don't Care

PCB Rules and Constraints Editor [mm]

Name: FabricationTestpoint
Comment:
Unique ID: WCKALQKE

Where The First Object Matches: ○ All ○ Net ○ Net Class ○ Layer ○ Net and Layer ● Advanced (Query)

Full Query:

```
(IsPad And (OnTopLayer Or
OnBottomLayer)) Or (IsVia) Or
(IsPad And OnMultiLayer)
```

Constraints

Sizes

	Size	Hole Size
Min	0.4mm	0mm
Max	2.54mm	1.9mm
Preferred	1.524mm	0.8128mm

Clearances
Min Inter-Testpoint Spacing: 0mm
Component Body Clearance: 0mm
Board Edge Clearance: 0mm

Grid
● No Grid
○ Use Grid
Origin X 9001mm Y 1.80004mm
Grid Size 0.0254mm
Tolerance 0.00025mm

☑ Allow testpoint under component

Allowed Side
☑ Top
☑ Bottom

Rule Scope Helper
□ SMD Pads
□ Vias
□ Thru-hole Pads

Define separate design rules to constrain which pads and/or vias in the design can be used as Fabrication testpoints and Assembly testpoints, and which nets require testpoints.

The Testpoint Style and Usage rules are identical, in terms of constraints, between the two testing modes (fabrication and assembly). The style rule essentially specifies constraints that a pad or via has to meet in order to be considered for selection as a testpoint location. The usage rule simply specifies which nets require a testpoint. When defining a style rule, the rule scope can be quickly created to target the precise pad and/or via objects for testpoint consideration, using the *Rule Scope Helper*.

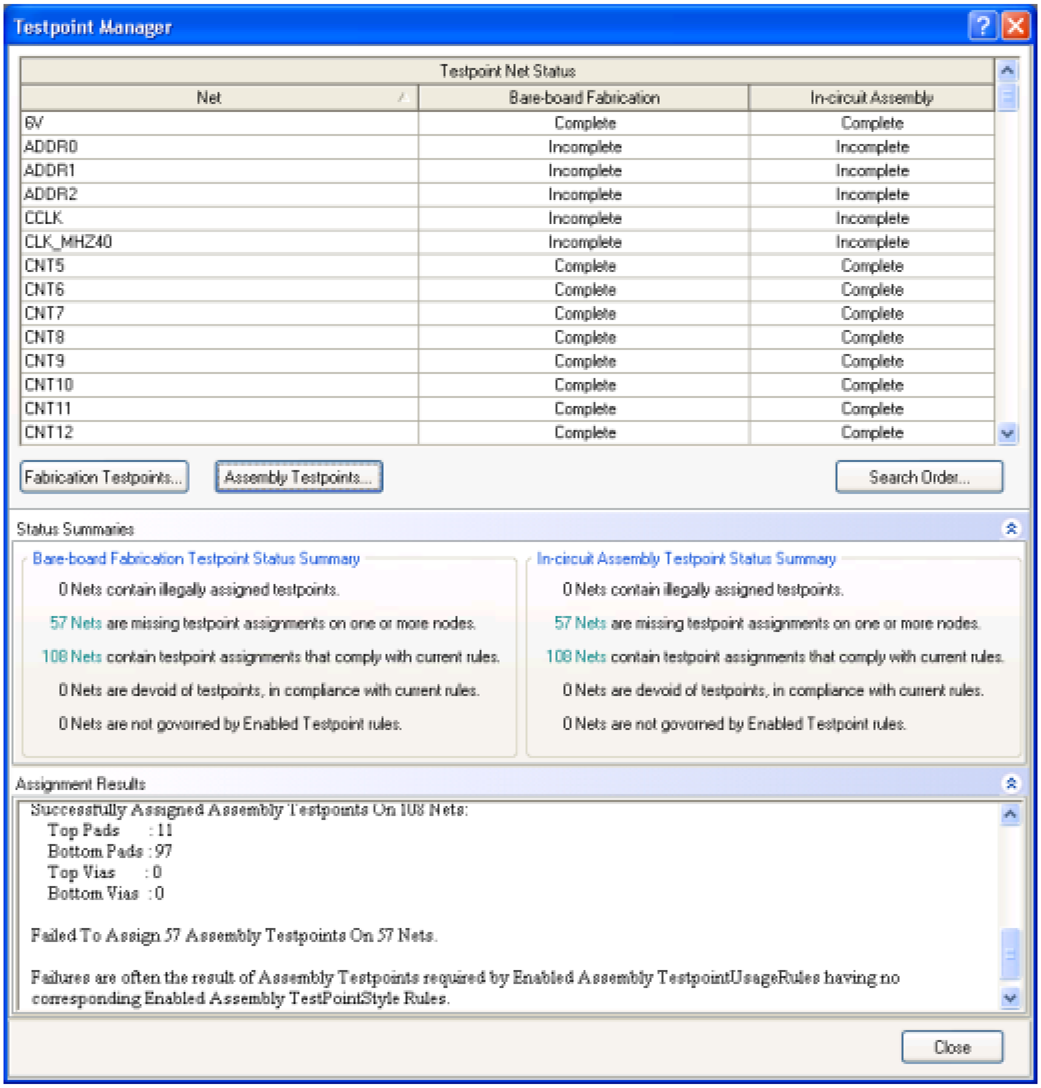
The testpoint design rules are used by the *Testpoint Manager*, the Autorouter, Online and Batch DRC processes and also during output generation.

> ⚠ Default Fabrication and Assembly Testpoint Style and Testpoint Usage rules exist. You should check whether these rules meet your board requirements and make changes as necessary. However, for the Testpoint Manager to successfully assign testpoints, there must always be at least one corresponding Style rule with a scope of `All`. If multiple rules of the same type are required, simply use the priority aspect of design rules to ensure that rules with more specific scoping are applied first (for example when running a DRC).

> When opening PCB designs or importing design rules created in a release of the software prior to the Summer 09 release, Testpoint Style rules will become Fabrication Testpoint Style rules and Testpoint Usage rules will become Fabrication Testpoint Usage rules.

Managing Testpoints

Assigning testpoints manually can be a painstaking and laborious job at the best of times. Imagine this task on a more complex board, populated with hundreds of components (possibly on both sides of the board) and the process cries out for a more automated method of testpoint assignment. To cater for streamlined management of testpoints in your board designs, Altium Designer equips the PCB Editor with a *Testpoint Manager*.



	Testpoint Net Status	
Net	Bare-board Fabrication	In-circuit Assembly
6V	Complete	Complete
ADDR0	Incomplete	Incomplete
ADDR1	Incomplete	Incomplete
ADDR2	Incomplete	Incomplete
CCLK	Incomplete	Incomplete
CLK_MHZ40	Incomplete	Incomplete
CNT5	Complete	Complete
CNT6	Complete	Complete
CNT7	Complete	Complete
CNT8	Complete	Complete
CNT9	Complete	Complete
CNT10	Complete	Complete
CNT11	Complete	Complete
CNT12	Complete	Complete

Bare-board Fabrication Testpoint Status Summary

0 Nets contain illegally assigned testpoints.
57 Nets are missing testpoint assignments on one or more nodes.
108 Nets contain testpoint assignments that comply with current rules.
0 Nets are devoid of testpoints, in compliance with current rules.
0 Nets are not governed by Enabled Testpoint rules.

In-circuit Assembly Testpoint Status Summary

0 Nets contain illegally assigned testpoints.
57 Nets are missing testpoint assignments on one or more nodes.
108 Nets contain testpoint assignments that comply with current rules.
0 Nets are devoid of testpoints, in compliance with current rules.
0 Nets are not governed by Enabled Testpoint rules.

```
Successfully Assigned Assembly Testpoints On 108 Nets:
   Top Pads      : 11
   Bottom Pads : 97
   Top Vias       : 0
   Bottom Vias  : 0

Failed To Assign 57 Assembly Testpoints On 57 Nets.

Failures are often the result of Assembly Testpoints required by Enabled Assembly TestpointUsageRules having no
corresponding Enabled Assembly TestPointStyle Rules.
```

Manage your fabrication and assembly testpoint requirements quickly and efficiently using the Testpoint Manager.

Accessed from the PCB Editor's main Tools menu (**Tools»Testpoint Manager**), the *Testpoint Manager* provides controls allowing you to automatically assign and clear testpoints from the one convenient location. A listing of all nets in the design is provided, with status to indicate testpoint coverage – either `Complete` or `Incomplete` – for both bare-board fabrication and in-circuit assembly testing.

Click the **Fabrication Testpoints** or **Assembly Testpoints** button to Assign or Clear that type of testpoint. Note that you can manually select nets in the upper region of the dialog to selectively assign testpoints.

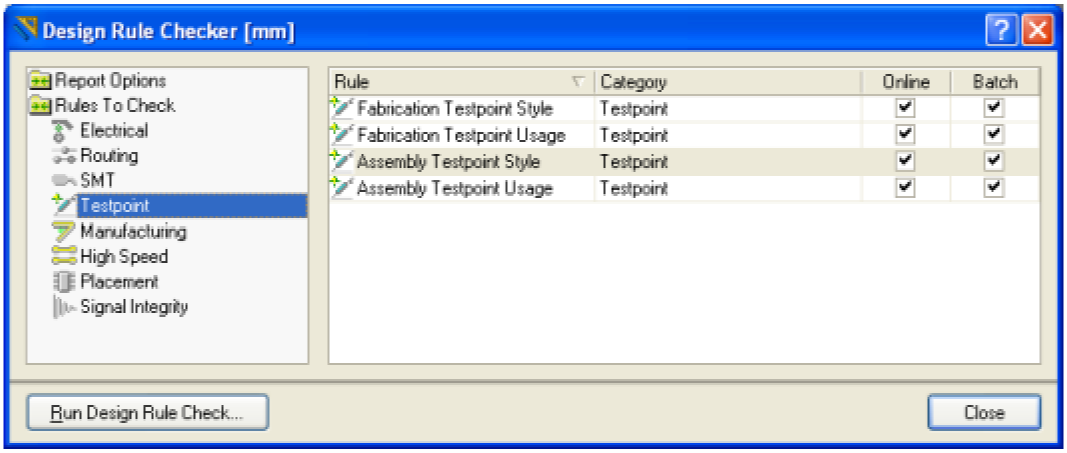
Whether assigning testpoints for some or all of the nets in a design, the *Testpoint Manager* follows the style and usage rules defined for fabrication and assembly testpoints. To see the order that valid objects are searched click the **Search Order** button. To change the order, right-click on an entry in the search order list and use the floating menu commands or the **Shift+Up Arrow** and **Shift+Down Arrow** shortcuts to move it up or down in the list.

The **Status Summaries** region provides a full summary of the testpoint status for the board, for both testing modes. This region updates with each assignment or clearance action performed. For more lower-level detail, use the **Assignment Results** region. This will give detail, for example, on the number of top/bottom pads/vias involved in an assignment/clearance.

> The *Testpoint Manager* replaces the **Tools»Find and Set Testpoints** and **Tools»Clear All Testpoints** commands found in releases of Altium Designer prior to the Summer 09 release.

Checking the Validity of Testpoints

Defined fabrication and assembly testpoint rules are followed as part of the PCB Editor's Design Rule Checking (DRC) facility. Online and/or Batch DRC checking can be enabled for the various rule types from within the *Design Rule Checker* dialog (**Tools»Design Rule Check**).



Rule	Category	Online	Batch
Fabrication Testpoint Style	Testpoint	☑	☑
Fabrication Testpoint Usage	Testpoint	☑	☑
Assembly Testpoint Style	Testpoint	☑	☑
Assembly Testpoint Usage	Testpoint	☑	☑

Include your testpoint design rules as part of the Online or Batch DRC processes.

Testpoint-related Query Fields

In support of the various fabrication and assembly testpoints that can be assigned in a design, the following testpoint-related keywords are available for use when targeting testpoints using logical query expressions. Each of the following can be found in the **PCB Functions - Fields** category, when using the *Query Helper*:

- `IsAssyTestpoint` – is an assembly testpoint
- `IsFabTestpoint` – is a fabrication testpoint
- `IsTestpoint` – is a Top or Bottom side testpoint
- `Testpoint` – is it a Top or Bottom side testpoint
- `TestpointAssy` – is it an assembly testpoint
- `TestpointAssyBottom` – is it a Bottom side assembly testpoint

- `TestpointAssyTop` – is it a Top side assembly testpoint
- `TestpointBottom` – is it a Bottom side testpoint
- `TestpointFab` – is it a fabrication testpoint
- `TestpointFabBottom` – is it a Bottom side fabrication testpoint
- `TestpointFabTop` – is it a Top side fabrication testpoint
- `TestpointTop` – is it a Top side testpoint

Create logical expressions for queries to target and return testpoints in your design as required. Some examples of logical query expressions targeting fabrication and assembly testpoint are:

`(ObjectKind = 'Pad') And (TestpointAssy = 'True')` – targets all pads that are assembly testpoints

`IsPad And (TestpointAssyTop = 'True')` – targets all pads that are Top side assembly testpoints

`(ObjectKind = 'Pad') And (TestpointFab = 'True')` – targets all pads that are fabrication testpoints

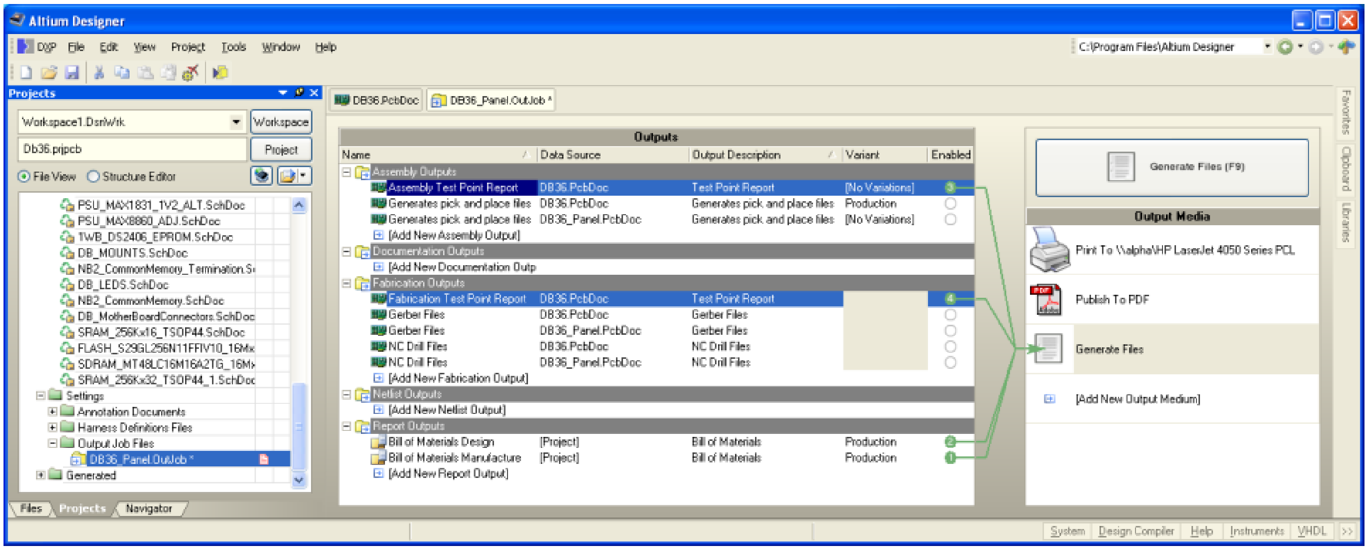
`((IsPad Or IsVia)) And (TestpointAssy = 'True')` – targets all pads and vias that are assembly testpoints

`((IsPad Or IsVia)) And IsFabTestpoint` – targets all pads and vias that are fabrication testpoints.

Generating Testpoint Reports

Altium Designer includes dedicated report generators for generation of fabrication and assembly testpoint reports respectively. These two report generators utilize the relevant testpoint properties for the pad and via primitives in a design. A fabrication testpoint report will therefore only use pad or via **Fabrication** testpoint settings. An assembly testpoint report will use only **Assembly** testpoint settings.

Reports can be generated either directly from within the PCB document (using the **File»Fabrication Outputs»Test Point Report** and **File»Assembly Outputs»Test Point Report** commands), or by using appropriately configured output generators defined in an Output Job Configuration file (`*.OutJob`). The latter is created using Altium Designer's OutputJob Editor – an invaluable resource for getting your design to manufacture.



Outputs

Name	Data Source	Output Description	Variant	Enabled
Assembly Outputs				
Assembly Test Point Report	DB36.PcbDoc	Test Point Report	[No Variations]	3
Generates pick and place files	DB36.PcbDoc	Generates pick and place files	Production	○
Generates pick and place files	DB36_Panel.PcbDoc	Generates pick and place files	[No Variations]	○
[Add New Assembly Output]				
Documentation Outputs				
[Add New Documentation Outp				
Fabrication Outputs				
Fabrication Test Point Report	DB36.PcbDoc	Test Point Report		4
Gerber Files	DB36.PcbDoc	Gerber Files		○
Gerber Files	DB36_Panel.PcbDoc	Gerber Files		○
NC Drill Files	DB36.PcbDoc	NC Drill Files		○
NC Drill Files	DB36_Panel.PcbDoc	NC Drill Files		○
[Add New Fabrication Output]				
Netlist Outputs				
[Add New Netlist Output]				
Report Outputs				
Bill of Materials Design	[Project]	Bill of Materials	Production	2
Bill of Materials Manufacture	[Project]	Bill of Materials	Production	1
[Add New Report Output]				

Generate Files (F9)

Output Media

Print To \\alpha\HP LaserJet 4050 Series PCL

Publish To PDF

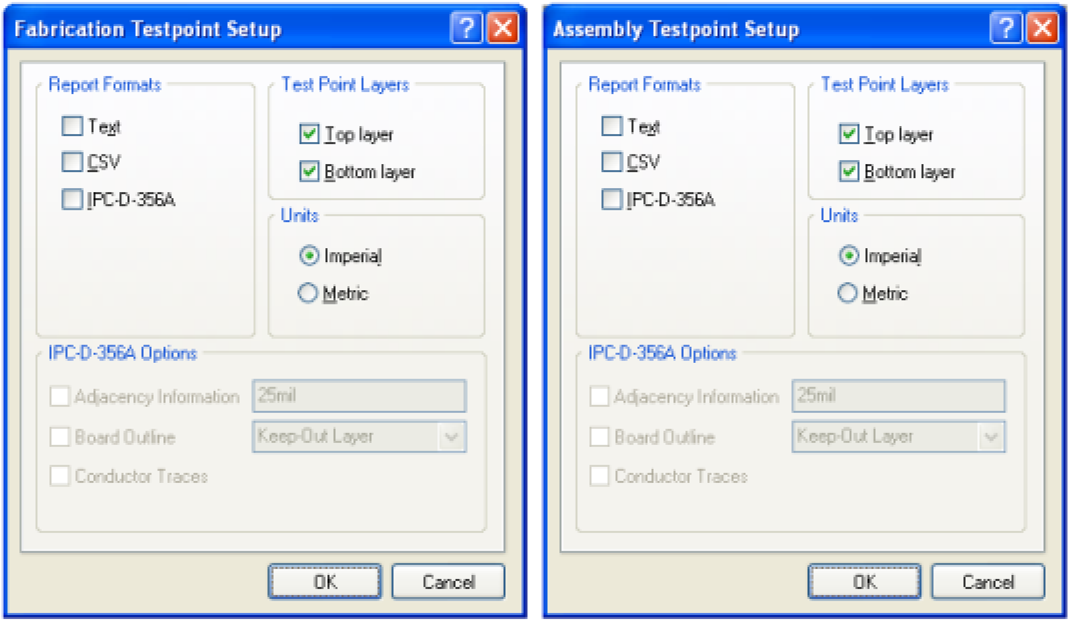
Generate Files

[Add New Output Medium]

Include and configure fabrication and assembly testpoint report output generators within a self-contained and versatile Output Job Configuration file. Once defined, obtain your reports at the touch of a button!

> The settings defined in a Testpoint Setup dialog when generating output directly from the PCB are distinct and separate to those defined for the same output type in an Output Job Configuration file. In the case of the former, the settings are stored in the project file, whereas for the latter they are stored in the Output Job Configuration file.

Regardless of the method used to generate a report, the report options themselves are defined in the same dialog. For a fabrication testpoint report, this involves the *Fabrication Testpoint Setup* dialog. For an assembly testpoint report, the *Assembly Testpoint Setup* dialog is used. Report options are identical between these dialogs.



Fabrication Testpoint Setup

Report Formats

- □ Text
- □ CSV
- □ IPC-D-356A

Test Point Layers

- ☑ Top layer
- ☑ Bottom layer

Units

- ● Imperial
- ○ Metric

IPC-D-356A Options

- □ Adjacency Information: 25mil
- □ Board Outline: Keep-Out Layer
- □ Conductor Traces

OK Cancel

Assembly Testpoint Setup

Report Formats

- □ Text
- □ CSV
- □ IPC-D-356A

Test Point Layers

- ☑ Top layer
- ☑ Bottom layer

Units

- ● Imperial
- ○ Metric

IPC-D-356A Options

- □ Adjacency Information: 25mil
- □ Board Outline: Keep-Out Layer
- □ Conductor Traces

OK Cancel

Define report options, including generated file format, using the relevant report setup dialog.

Upon generation, the output will be added to the project and appear in the Projects Panel under the `Generated` folder.

Role of the IPC-D-356A Netlist File

One of the three flavours of testpoint report output formats is an IPC-D-356A netlist file. This file is typically used to target the bare-board fabrication testing mode. The IPC file is post-processed into commands that drive a flying probe testing device.

Regardless of which features are specifically identified as test point locations in an IPC-D-356A file, board fabrication houses can generally use the file data to achieve whatever type of testing that they want although, depending on circumstances and the content of the file, it may require some manual intervention to do so.