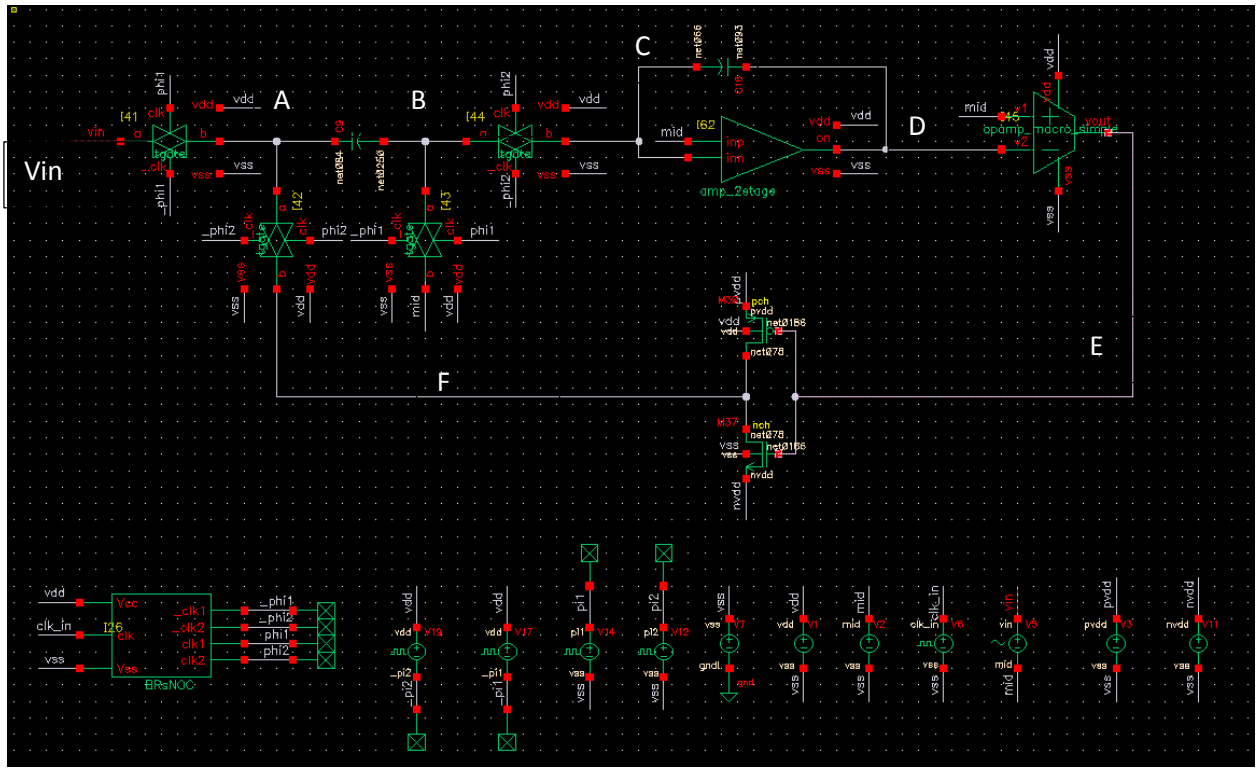
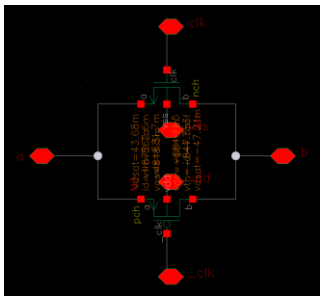
The architecture that I am using is the very simple single ended ΔΣ modulator. The modulator is supposed to work for audio band signals (20-20KHz). The clock signal that is used is a 2.56MHz pulse. Therefore OSR is 64. Switches that I used are the simple Tgate switches, a simple single stage amplifier is used for the sc-integrator. Also a simple two stage amplifier is used for the 1-bit ADC. The 1-bit DAC is realized with a simple inverter. The positive voltage of the DAC is +VREF and the negative voltage is -VREF. Capacitor sizes are equal to 1pF.

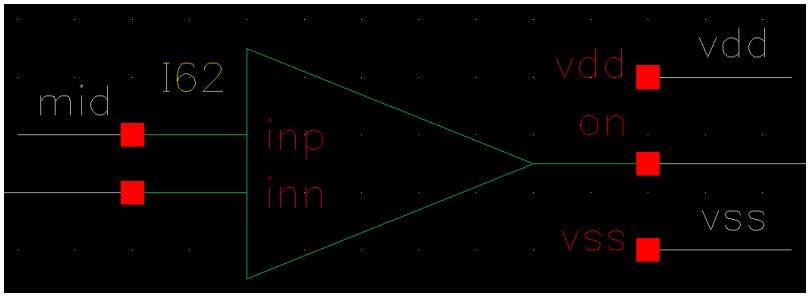
The sigma delta ADC test bench AND the name of the different nodes (Vin, A,B,C,D,E,F) I am using is:

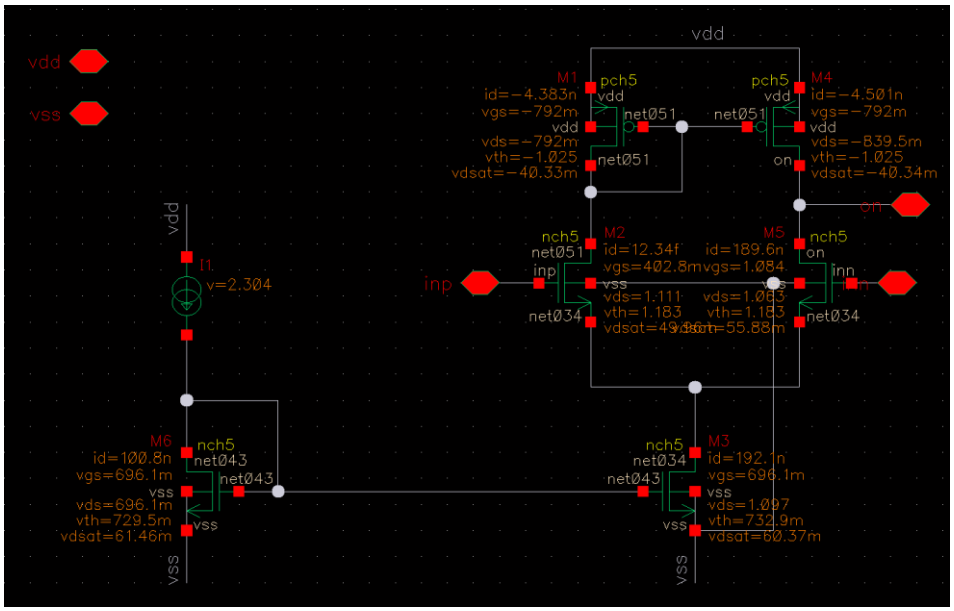


The Tgate switch:

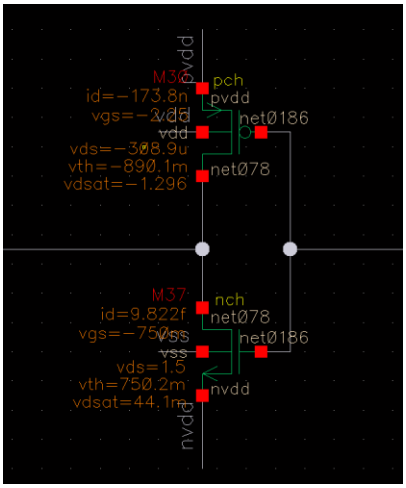


The OTA that I am using for the integrator in my design is:



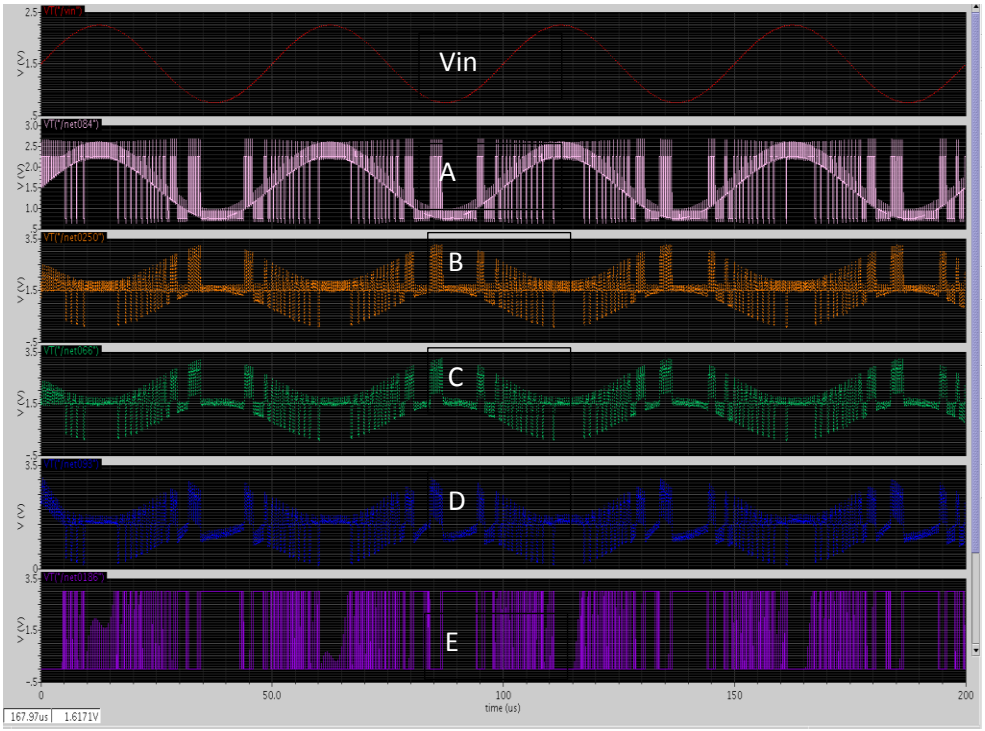


And the 1-bit DAC that is used in the loop is:



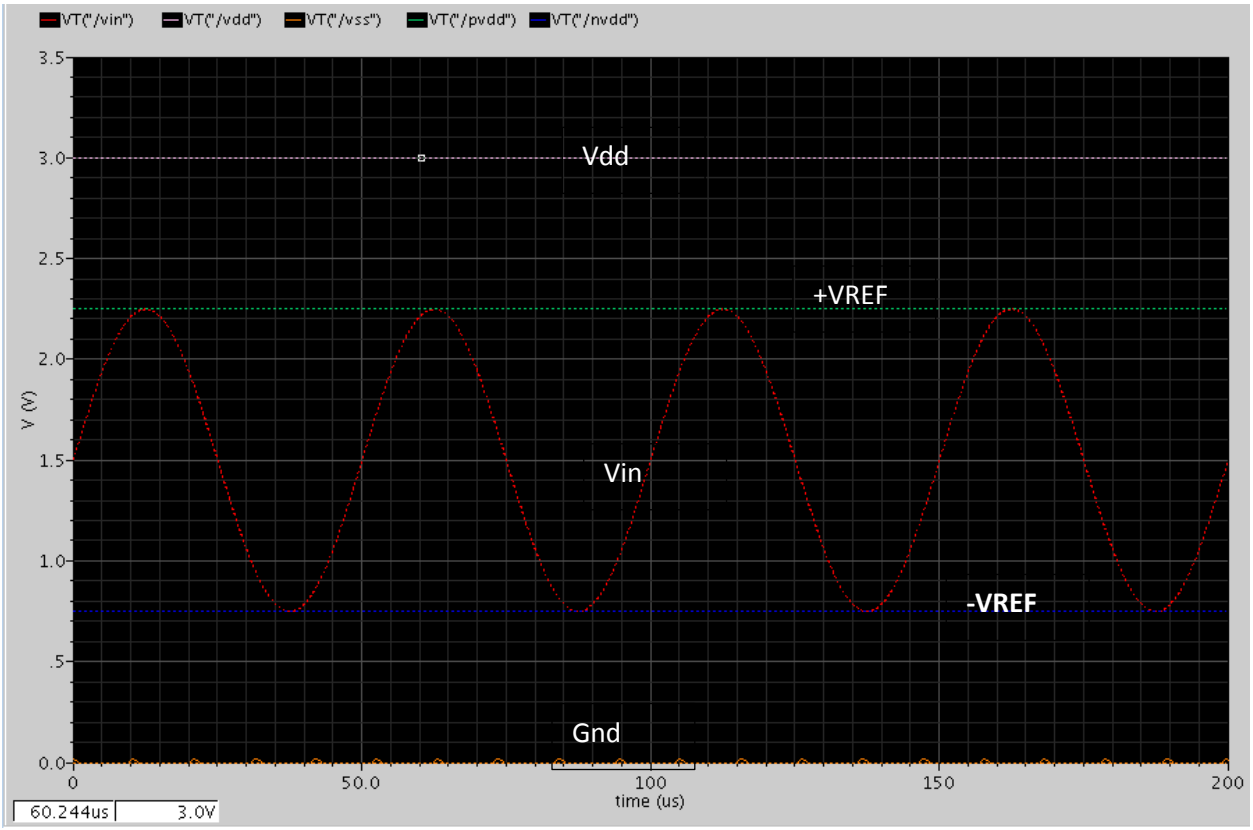
This is the simulation results for the Vin=1.5+0.75*Sin(2*pi*20K*t) and +Vref=2.25V -Vref=0.75V.

Input frequency is 20KHz / Vdd=3 / Mid=1.5V / C1=1Pf / C2=1pF

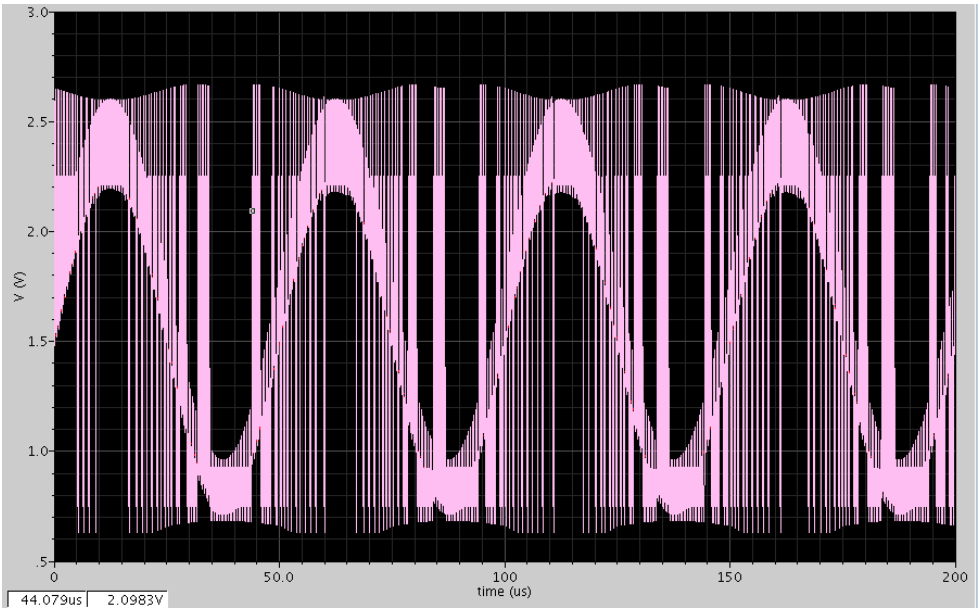


From top to bottom: Vin A B C D E

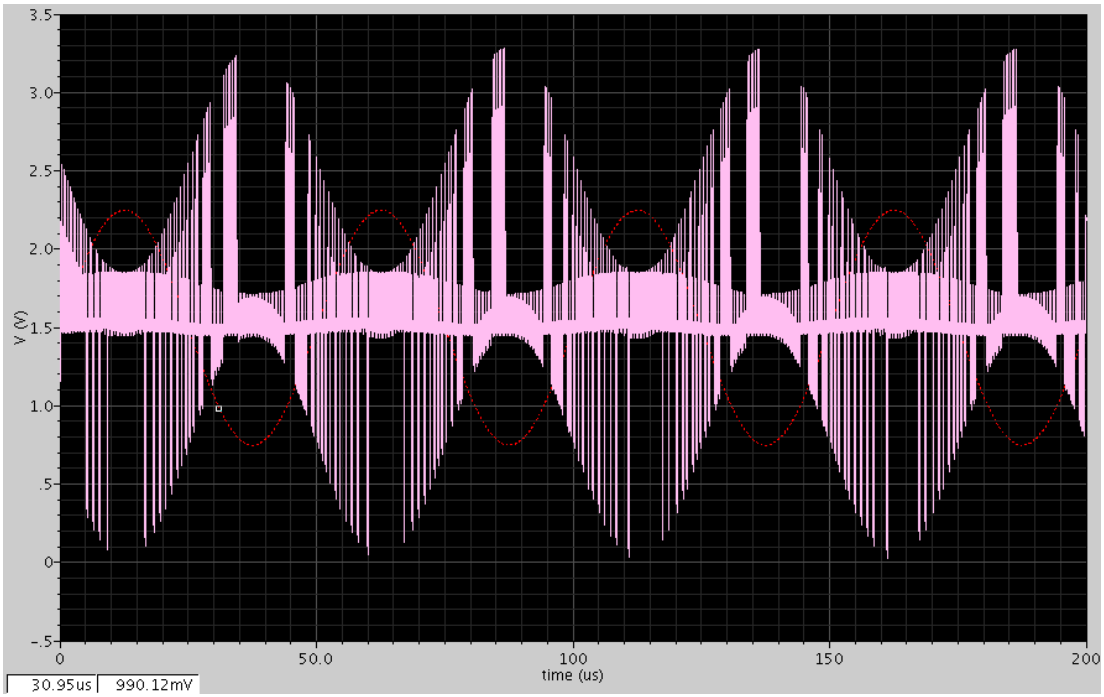
In order to see much easier, I showed the input signal versus different nodes again:



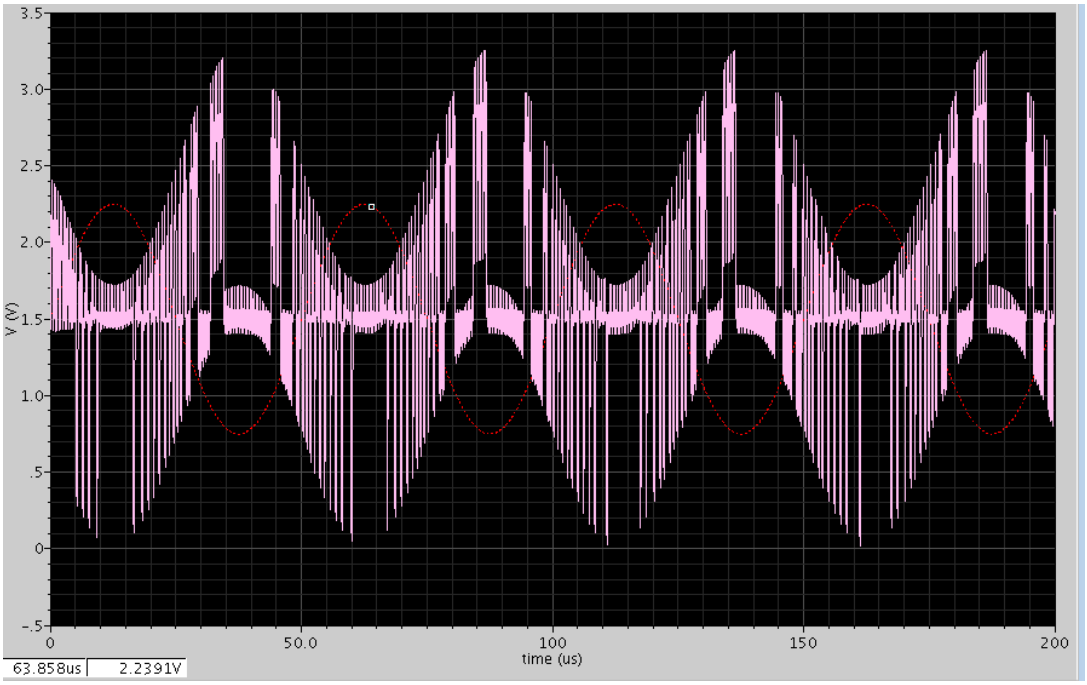
Input signal vs (A) or sampled input:



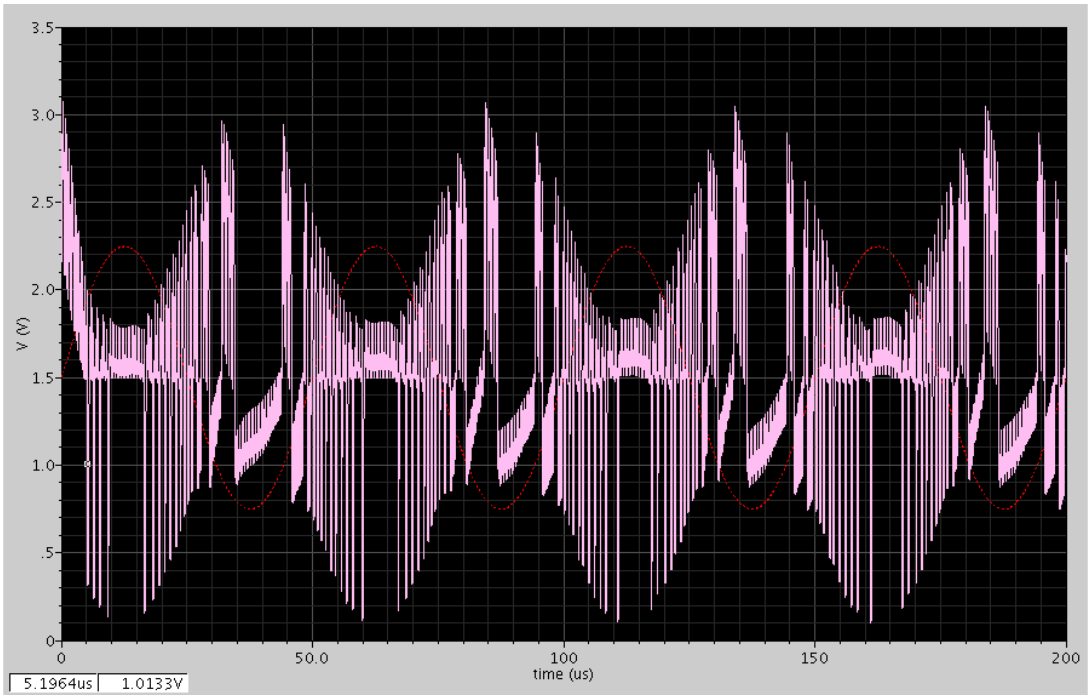
Input voltage vs (B):



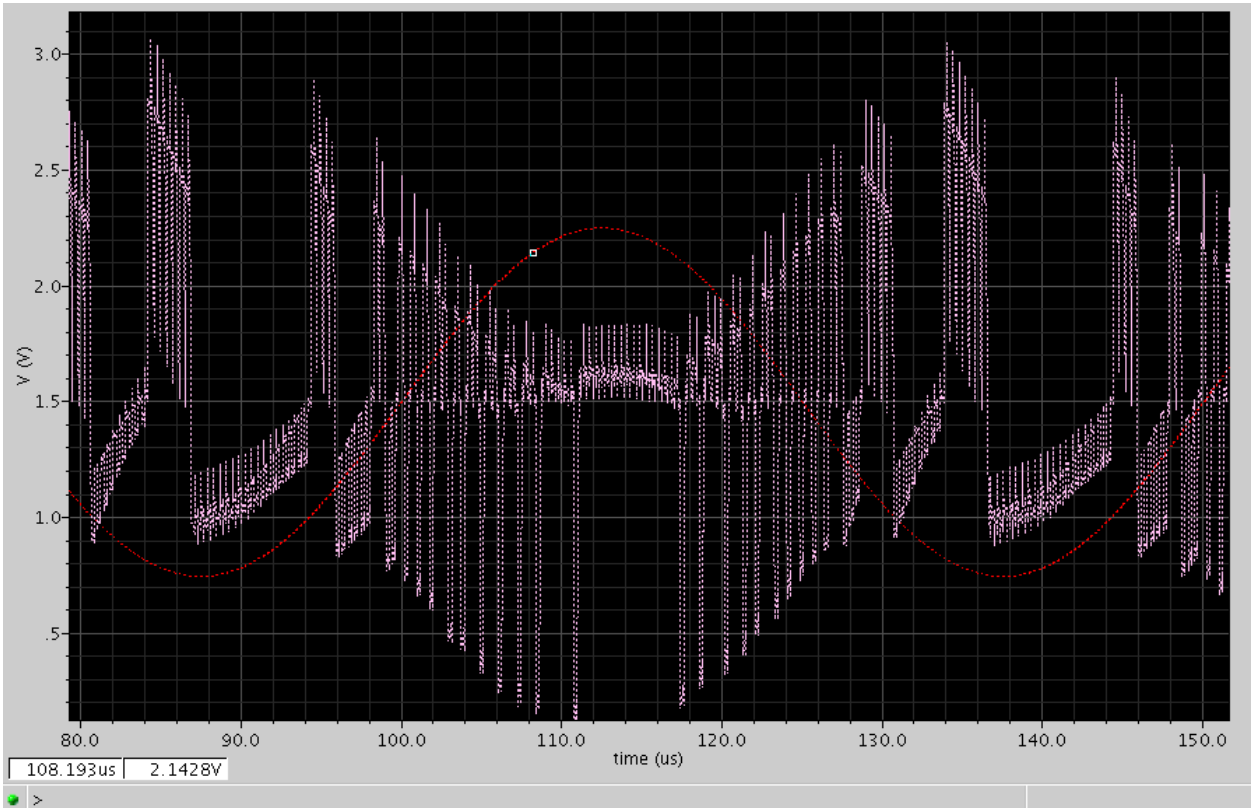
Input voltage vs (C) or OTA negative input:



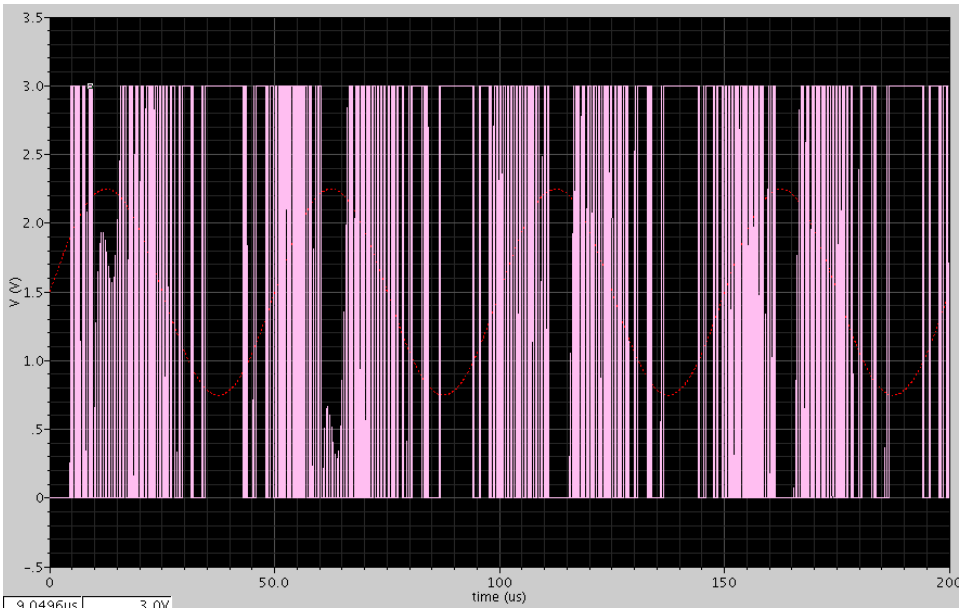
Input voltage vs (D) or integrator output:



Zoomed in (Input voltage vs (D) or integrator output):



Input voltage vs (E) or digital output:



Input voltage vs (F) or feedback signal: