ACOUSTIC NOISE REMOVAL FROM SMPS
(A NON-COMPETENT TRIAL & ERROR APPROACH)

Acoustic noise in switch mode power products can be a troublesome thing for a novice designer. However in order to remove it from a prototype, better understanding and sound knowledge of magnetic components is required. While troubleshooting such cases the reasons behind acoustic noise generation that I found in flyback and forward type topologies are as below.

At light loads the current sensing circuitry measures the low current demand and lowers the duty ratio. In real scenarios this duty ratio is so small that almost diminishing. Thus in next cycle a high primary current flows through MOSFET and current sensing circuitry. This produces more than necessary power at output and thus in next cycles the cycle is skipped or duty ratio is lowered too much. One thing to be noted that this primary current when flowing at low output power is still at peak primary current level determined and limited by current sensing circuitry. Also this current is at random cycles either because of this reason or due to false triggering of current sensing circuitry by leading edge spike. This high level of random current produces high peak flux in transformer core which causes audible noise due to magnetostriction. The solution is that we can remove acoustic noise almost if we can keep primary current level to a lower level instead of at peak cutoff level at low output power. Then if possible we can also operate this SMPS in burst mode without danger of acoustic noise.

To rectify the problem I redesigned a flyback SMPS on veroboard.

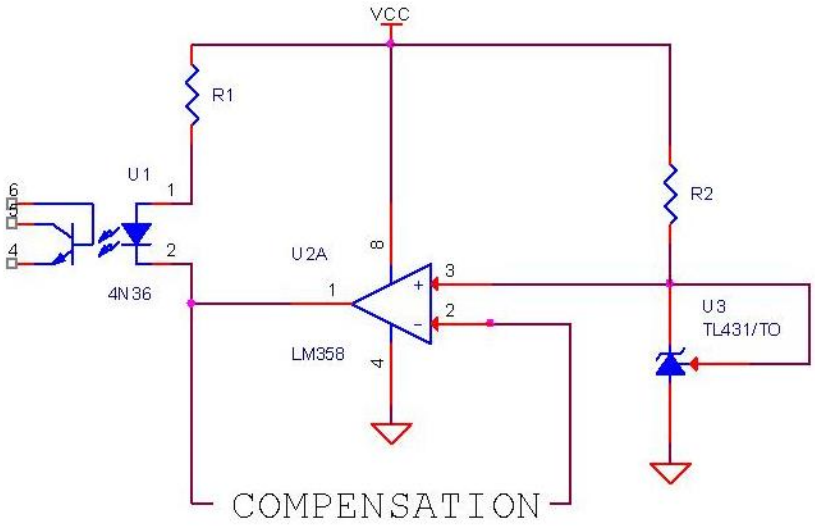

FIGURE 1

It is operating at 50 KHz but no audible noise from transformer detected at no load to full load. First of all I did as before and there was audible noise of around 1.6KHz. It was designed using UC3844, an old traditional IC. I used the same type of snubber and clamp "ceramic" capacitors as were in previous design and it was not the culprit though I don't recommend them. The things that I did to solve this problem were as below.

1) Don't use single op-amp part as feedback with opto-LED cathode side connected to its output side (and anode connected to VCC side) to save another op-amp part (Figure 1). Otherwise there might still be enough voltage differential acorss opto-LED to let it turn on at input turn off command. This issue can be seen frequently in op-amps that don't provide rail-to-rail operation. Even if used two op-amp parts so that signal level could be inverted again (Figure 2) the acoustic noise would be still loud there and next suggestions should be followed.

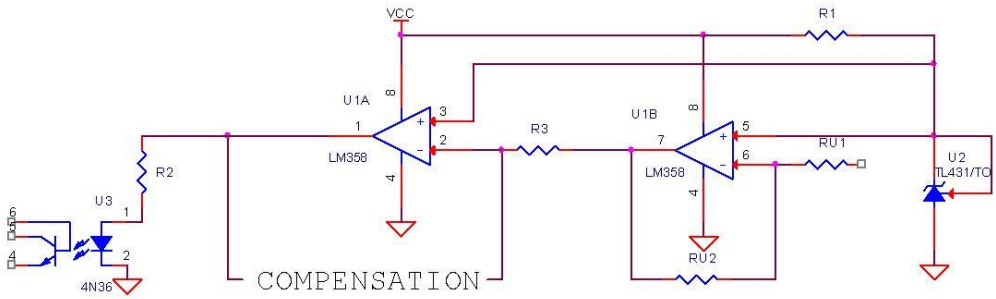

FIGURE 2

2) The feedback op-amp and connected opto-LED should be given power from much higher than 5V (Figure 3) or other intelligent methods should be used so that it could occupy and thus sweep full range of resistor limited current from this opto-LED. This will produce more shades of opto-LED light intensity instead of just on and off. This will prevent cycle skipping command.

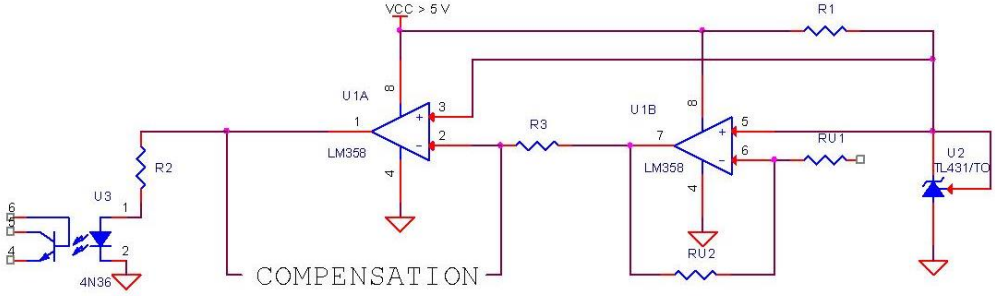

FIGURE 3

3) Correct the opto-transistor current according to current transfer ratio, CTR.

4) Add a small value non-polar capacitor in parallel with current sense resistor (Figure 4). This will further reduce the acoustic noise.

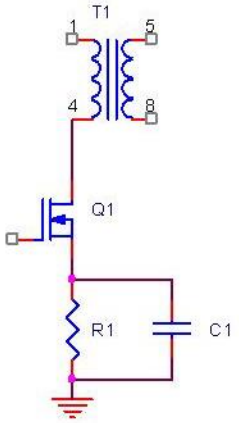

FIGURE 4

5) Add a small value high voltage capacitor above 1 KV working volts between primary and secondary ground (Figure 5).

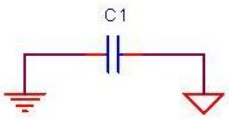

FIGURE 5

6) You may now hear light acoustic noise and that would be at no load. By pressing core parts to each other this should vanish. Use some varnish and epoxy to fasten the two core parts and problem solved.

7) If your PWM IC does not support leading edge blanking option then you can implement at current sense pin with few external parts (Figure 6). This will almost eliminate the false triggering at this pin and help reduce acoustic noise further.

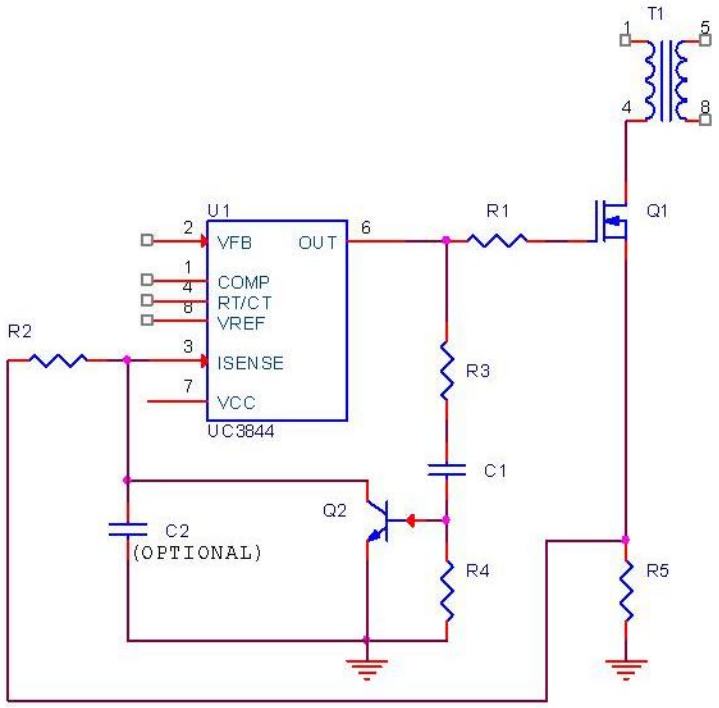

FIGURE 6

8) Operate feedback error amplifier output in current source mode by using a transistor in opto-LED path (Figure 7).

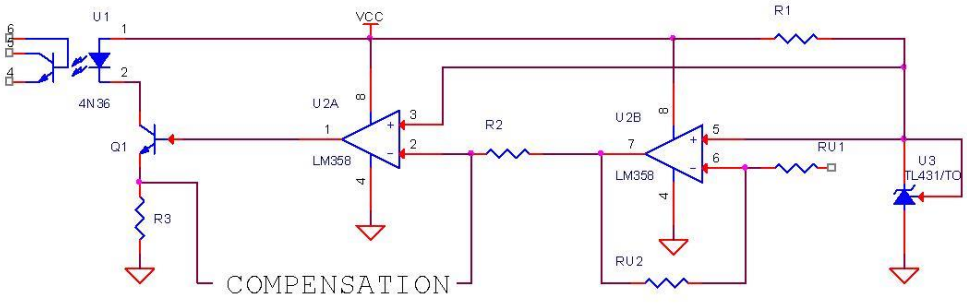

FIGURE 7

9) Another trick that works is to keep PWM chip error amplifier at unity gain on primary side after opto-transistor with compensation done on secondary side and primary error amplifier input and feedback resistor near minimum set value as shown in datasheet. As an example it is 8.8 K for UC384X series and 30 K for SG3526 type ICs (Figure 8).

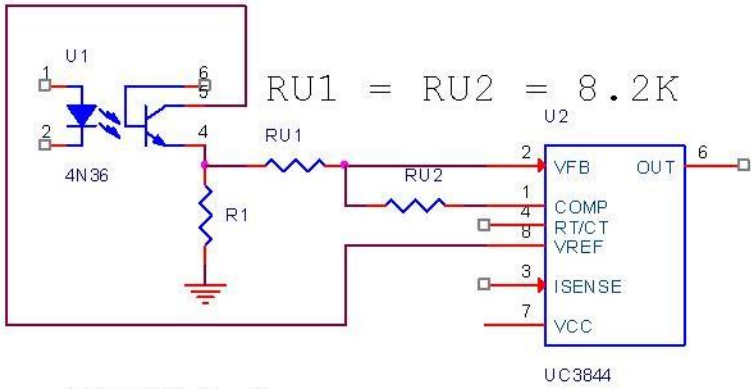

FIGURE 8

10) In order to eliminate cycle skipping and hence acoustic noise slightly lower the reference voltage used to power opto-transistor collector pin (Figure 9).

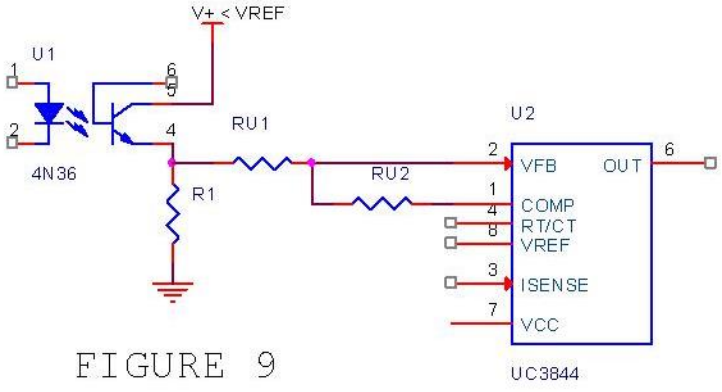

FIGURE 9

11) Sometimes connecting current sense pin ISENSE to rectified high voltage DC +HVDC via 1 Meg resistor helps (Figure 10).

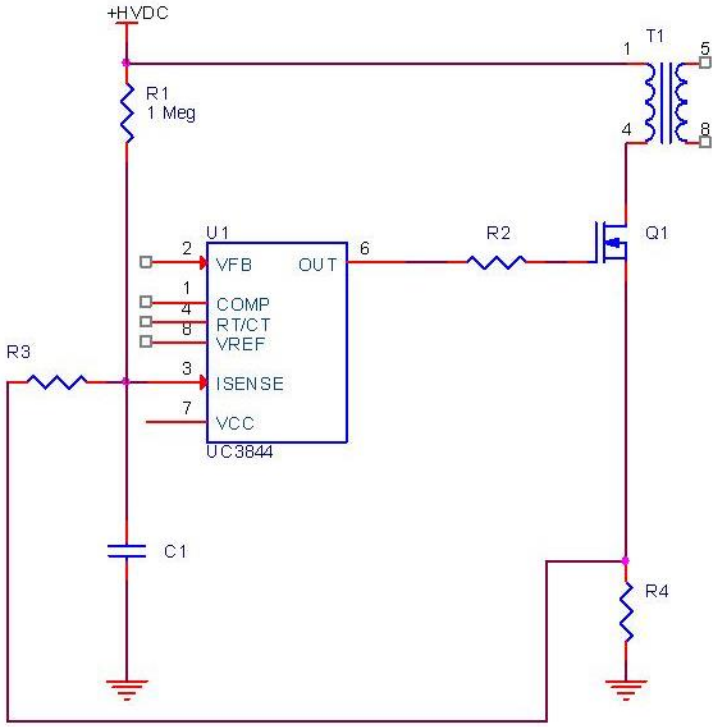

FIGURE 10

12) Another way of connecting a small value high voltage non-polar capacitor to output ground is to link it with input high voltage rectified DC +HVDC (Figure 11).

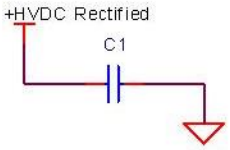

FIGURE 11

13) Some other ICs like NCP120x series have built in adjustment technique for peak level of current at current sense resistor to reduce or forbid the acoustic noise completely. They lowers the peak level of current at low power demand (Figure 12). This way peak level of flux is lowered which reduces magnetostriction effect so that no acoustic noise can be heard from transformer core. The advantage is that we can operate the power supply in burst mode at light loading without danger of acoustic noise. Burst mode operation can also be implemented with UC384X chips using few

external parts.

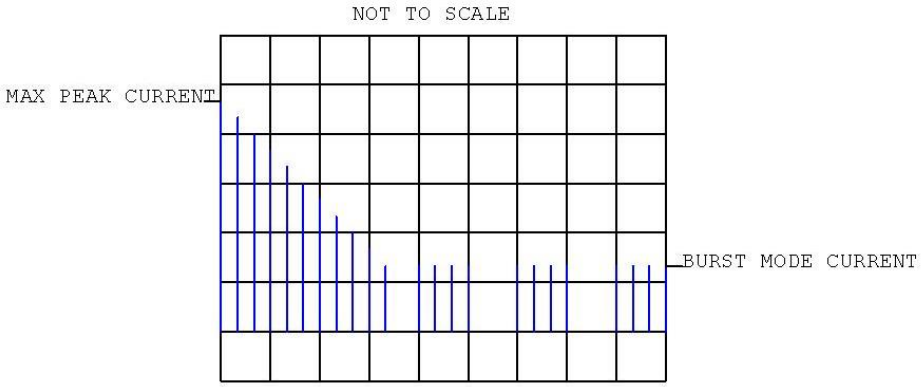

FIGURE 12