

Full-Bridge Modular Multilevel Submodule-Based High-Voltage Bipolar Pulse Generator With Low-Voltage DC, Input for Pulsed Electric Field Applications

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Abstract—High-voltage (HV) pulse generators (PGs) are the core of pulsed electric field applications. Applying HV pulses produces electrical pores in a biological cell membrane, in which if the size of the pores increases beyond a critical size, the cell will not survive. This paper proposes a new HV-PG based on the modular multilevel converter with full-bridge submodules (FB-SMs). In order to alleviate the need of complicated sensorless or sensor-based voltage balancing techniques for the FB-SM capacitors, a dedicated self-regulating charging circuit is connected across each FB-SM capacitor. The individual capacitor charging voltage level is obtained from three successive stages, namely, convert the low-voltage dc input voltage to a high-frequency square ac voltage, increase the ac voltage level via a nanocrystalline step-up transformer, and rectify the secondary transformer ac voltage via a diode FB rectifier. The HV bipolar pulses are formed across the load in a fourth stage through series connected FB-SMs. The flexibility of inserting and bypassing the FB-SM capacitors allows the proposed topology to generate different pulse-waveform shapes, including rectangular waveforms with specifically reduced dv/dt and ramp pulses. The practical results, from a scaled-down experimental rig with five FB-SMs and a 1-kV peak-to-peak pulse output, validate the proposed topology.

Index Terms—Electroporation, high-voltage bipolar pulses, modular multilevel converters (MMCs), pulsed electric field (PEF).

I. INTRODUCTION

APPLYING a pulsed electric field (PEF) across a biological cell membrane produces electrical pores

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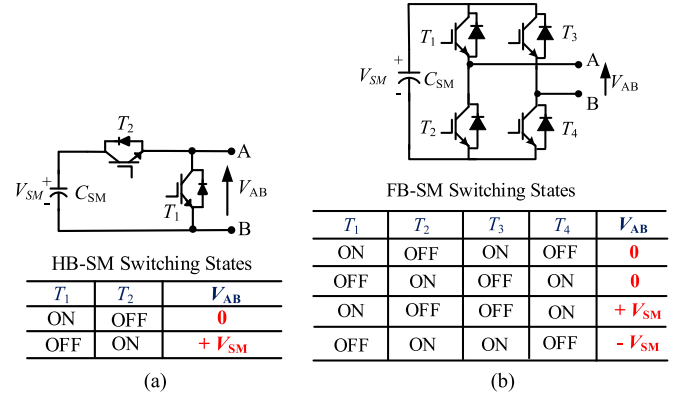


Fig. 1. MMC-SMs. (a) HB-SM. (b) FB-SM.

(or electroporation) in the cell. According to the cell type there is a critical pore size beyond which the cell will not survive, namely, it cannot reseal its pore [1]. Biofouling and protein insertion are examples of nonlethal exposure to a PEF, while water treatment and air pollution control are examples of lethal PEF applications [2], [3].

Applying a lethal or nonlethal PEF is associated with heat generation; however, in food sterilization this is an unwanted feature when preserving the nutritional value of food [4]. Generally, nonthermal plasma is utilized in water treatment and food sterilization through applying short pulse durations (tens of nanoseconds to a few hundred microseconds) of a electric field of strength 10–50 kV/cm [3]–[5].

Advances in power electronic devices, namely, their high power and high frequency ratings, have enabled semiconductor based high-voltage (HV) pulse generators (PGs) for PEF applications. The emerged topologies usually mimic the classically dominating PG converters, such as the Marx generator [6]–[8]. Creating HV pulses usually exploits the parallel charging of a group of capacitors and then their series connection to discharge across the load; achieved by means of semiconductor switches [9]–[11]. Utilizing the inherent capacitor in a modular multilevel converter (MMC) submodule (SM), to store energy and discharge across the load during pulse generation, is presented in the literature [12]–[15]. Generally, there are two main types of MMC-SM, namely, the half-bridge SM (HB-SM) and the full-bridge SM (FB-SM). Both have been extensively studied for MMC-based HVDC transmission applications, where the features of each SM type

have been revealed [16], [17]. Whereas the HB-SM has half the number of semiconductor switches, the FB-SM has the ability to generate negative voltage at its terminals, which can be used to block a HVDC dc fault current. Both SM types, along with their switch states, are shown in Fig. 1.

The voltage clamping feature of HB-SMs is employed in [15] to generate HV bipolar/unipolar rectangular pulses with a high repetition frequency while avoiding voltage sharing problems when series connecting semiconductor switches. In [12], the HB-SM capacitors are charged sequentially, and then connected in series to discharge into the load. The reduced dv/dt feature inherited in multilevel converters for HVDC transmission applications has been utilized to generate reduced dv/dt pulse waveforms to decrease the converter's electromagnetic interference (EMI) [18], [19]. In [20], with two H-bridges fed from two isolated dc input sources, a bipolar PG is proposed but providing the isolated dc sources to the H-bridges is not addressed. This possibly will impede the scalability of the PG.

Practically, classical PGs are able to generate unipolar pulses of rectangular as well as exponential waveforms [6], where these pulses impose electrical stresses on the cell membrane until electroporation is completed. Bipolar pulses prove their effectiveness in electroporation applications by subjecting the cell membrane to mechanical stresses in addition to the electrical stresses [21], [22].

In this paper, a new HV-PG topology is proposed, which is formed of four successive conversion stages. The stages start with a relatively low-voltage dc (LVDC) input and end with HV pulse generation across the load. The PG utilizes modular multilevel FB-SMs, thus can generate bipolar voltage pulses. HB-SMs produce a unipolar pulse, but with half the number of SM insulated-gate bipolar transistors (IGBTs). With both SM types, the SM capacitors are charged independently of individually connected circuitry across each SM capacitor. Thus, along with modularity and scalability, the proposed topology alleviates the need of an SM capacitor voltage balancing algorithm, as each SM capacitor is constantly charged by its individual circuit to the designed charging voltage level. Not only rectangular pulses are possible with the proposed topology, but also multilevel pulses with reduced dv/dt are possible. The utilized FB-SM capacitance is small compared with the mF capacitances in HVDC transmission applications, which reduces the topology footprint. The main contribution of the proposed HV-PG can be summarized as follows.

- 1) Generating HV pulses from an LVDC input supply.
- 2) Generation flexible pulse-waveform shapes.
- 3) Capacitor voltage balance is achieved without any voltage sensors or control algorithm.
- 4) Generation of bipolar pulses using one arm of series connected MMC FB-SMs.

The proposed converter is introduced in Section II, while its operational principle and FB-SM capacitor sizing are outlined in Section III. Experimental results are presented in Section IV. Finally, Section V summarizes the proposed topology aspects and limitations.

II. PROPOSED HV-PULSE GENERATOR TOPOLOGY

The proposed HV-PG converter topology and the four successive stages for HV pulse generation across a load are illustrated in Fig. 2. Stage-I, the H-bridge inverter, is responsible for converting the LVDC input V_s into a high-frequency square ac voltage of peak-to-peak value $2V_s$. In Fig. 2, stage-II is formed of multiple nanocrystalline core-based high-frequency step-up transformers; all with the same turns ratio $1 : n$. The nanocrystalline material is preferred (over ferrite) for high-frequency operation due to its high core permeability, hence high magnetizing inductance, high flux density, near square hysteresis loop, etc. [23]. The reduced transformer volume, due to high-frequency operation, enhances the modularity of the proposed topology. The primary of each transformer is a single turn that is located in the axial center of each transformer core. A single turn realizes the necessary HV isolation creepage and clearance. The peak of the applied high-frequency square ac voltage from stage-I, at the primary of each transformer is V_s/N , while the secondary voltage peak is nV_s/N where N is the number of transformer cores (hence FB-SMs) and n is the number of secondary turns.

The inductor L_{in} in stage-II has a small inductance, typically in the μ H range, to limit the input current (thus, creating a current source [24]–[25]). With a large number of transformers, the total leakage inductance may be sufficient to alleviate the need of L_{in} at the input. In stage-III, the high-frequency square ac voltage of each transformer secondary is rectified through a diode FB rectifier, resulting in a dc voltage of

$$V_{SM} = nV_s/N. \quad (1)$$

The final stage, stage-IV, consists of the N series connected FB-SMs across the load (usually the treatment chamber). With each FB-SM capacitor C_{SM} directly fed from the output of stage-III, the peak pulse voltage is approximately

$$V_p = nV_s. \quad (2)$$

The use of FB-SMs allows the generation of both positive and negative output voltage polarities. The antiparallel diodes across each IGBT switch in the FB-SMs can be omitted because they are not utilized to recharge the FB-SM capacitors as in HVDC transmission applications. Here, each of the N FB-SM capacitors is independently charged by one of the N external isolated sources (stage-III in Fig. 2).

III. HV-PG OPERATING PRINCIPLE AND FB-SM CAPACITOR SIZING

A. Principle of Operation

The voltage waveforms of the first three stages are illustrated in Fig. 3. Starting from an LVDC input V_s , each FB-SM capacitor is charged simultaneously and independently, to a dc voltage of nV_s/N . The FB-SM capacitors are the energy pool that delivers the required HV pulse energy (or stage IV), where with the aid of the FB-SM voltage clamping configuration, it is possible to connect the charged capacitors in series to create pulses with a peak voltage of $\pm nV_s$, if all the FB-SMs are inserted.

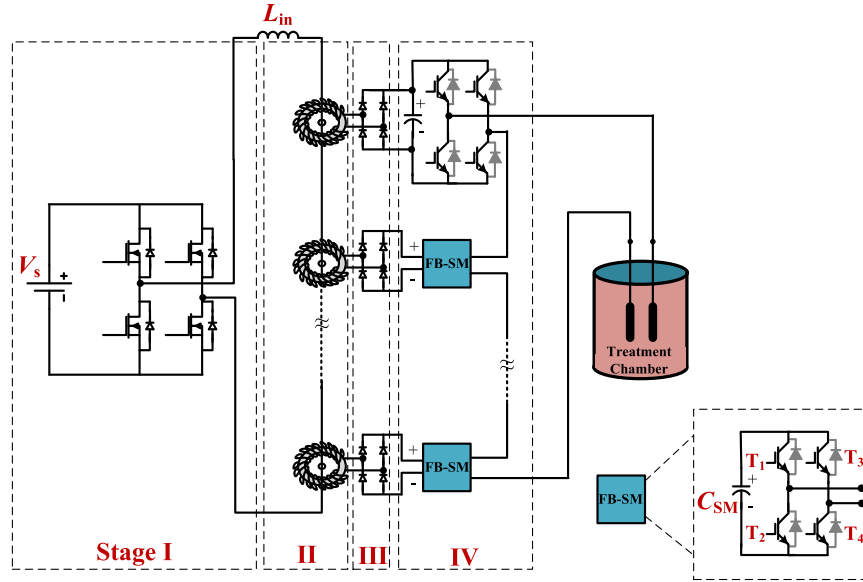


Fig. 2. Proposed pulse power topology and its four successive conversion stages for HV pulse generation.

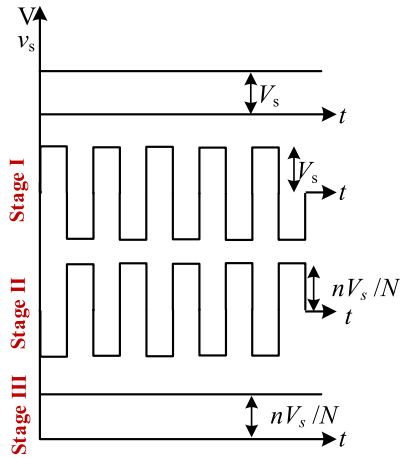


Fig. 3. Voltage variation through different stages of the proposed PG topology.

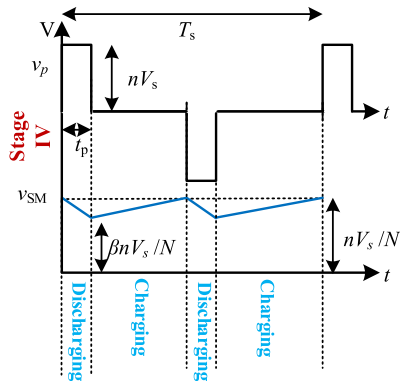


Fig. 4. Generating rectangular bipolar pulses by the proposed PG.

Fig. 4 illustrates the generation of a bipolar rectangular pulse waveform with a repetition time of T_s . At $t = 0$, all the FB-SM capacitors are inserted simultaneously to form the positive polarity voltage pulse (by turning ON T_1 and T_4 of each FB-SM), for the desired pulse time t_p , thus a peak voltage of $+nV_s$ is impressed across the load. Then, the FB-SMs are bypassed, by turning ON T_1 and T_3 (or T_2 and T_4) of each FB-SM, for $(1/2T_s - t_p)$ which nulls (zeros) the voltage

across the load. The FB-SM capacitors are inserted simultaneously to form the negative polarity voltage pulse (by turning ON T_2 and T_3 of each FB-SM), for the desired pulse time t_p . Then, again the SMs are bypassed, by turning ON T_1 and T_3 (or T_2 and T_4) of each FB-SM, for the remainder of T_s . During pulse generation, the FB-SM capacitor voltage V_{SM} decreases and droops, as a result of transferring some stored energy to the load. The remaining voltage V_o on each FB-SM capacitor is

$$V_o = \beta nV_s / N \quad (3)$$

where β is the percent remaining voltage after pulse generation. After pulse generation, the individual FB-SM capacitors are recharged to their predischarging value $V_{SM} = nV_s / N$ through stage-III (although charging occurs continuously, even during the pulse).

As the pulse voltage magnitude increases, it is desirable to reduce the PG dv/dt to reduce the EMI level. Several recent PGs utilize the MMC HB-SM for such a task [13], [14], [19]. However, generating multilevel pulse waveforms is not possible without assuring balance of the individual SM capacitor voltages. Generally, this can be achieved only by employing sensorless or sensor-based techniques. Balancing is possible with the proposed PG without the necessity of complicated algorithms for sorting the FB-SM capacitor voltages as in HVDC transmission applications. The fact that each FB-SM voltage is restored to its predischarging voltage level immediately after contributing to pulse generation, makes it possible to generate multilevel pulse waveforms, using the first-in first-out (FIFO) principle.

The FB-SM with the lowest capacitor voltage is charged first as the low-voltage H-bridge is forced to operate in a current source mode (current limit mode). Progressively, all the FB-SM capacitors are simultaneously charged in a current limiting mode until each capacitor voltage reaches V_{SM} , when the H-bridge operates in a voltage source mode. Thus, when an FB-SM is taken out of pulse generation (that is, bypassed)

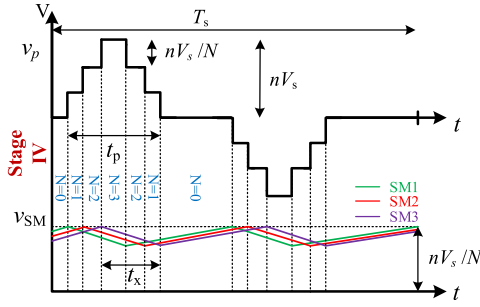


Fig. 5. Generating multilevel pulses by the proposed PG.

it is charged to the predischage voltage level while waiting for the next pulse generation. Fig. 5 illustrates the principle of generating four-level pulses with $N = 3$, rising to the pulse-peak voltage, as well as its decrease. During voltage increase (at the zero voltage level $N = 0$), for the first level ($N = 1$) only one FB-SM is inserted, SM1, for the second level ($N = 2$), SM2 is inserted, adding to SM1, and finally, SM3 is inserted, meaning all three SMs source the load, forming the pulse-peak voltage.

The transition to zero voltage is controlled by bypassing the first inserted FB-SMs first, based on the FIFO concept as illustrated in Fig. 5.

B. FB-SM Capacitance Sizing

In Figs. 4 and 5, after the FB-SM capacitor voltage droops due to transferring some of its stored energy to the load, it is charged to the predischarged voltage via the charging circuit in stage-III. Thus, if a bipolar rectangular pulse of pulse time t_p is considered (as in Fig. 4), the energy transferred to the load per pulse polarity, with a small voltage droop, can be expressed as

$$\frac{1}{2}C_{SM}(V_{SM}^2 - V_o^2)N \approx \frac{V_p^2}{R}t_p \quad (4)$$

where V_p is the peak of the of the rectangular pulse across the resistive load R . Modeling the load as a resistor is valid if the target pulses range is in microseconds and longer [2], which is the targeted range in this paper.

By neglecting semiconductor voltage drops from (1)–(3), (4) becomes

$$\frac{1}{2}C_{SM}\frac{n^2V_s^2}{N}(1-\beta^2) = \frac{n^2V_s^2}{R}t_p. \quad (5)$$

Rearranging (5), the FB-SM capacitance can be estimated as

$$C_{SM} = \frac{2Nt_p}{(1-\beta^2)R}\alpha \quad (6)$$

where $\alpha \geq 1$ is a factor to account for neglected semiconductor voltage drops and circuit parasitic resistances.

Although the estimated value in (6) is based on a rectangular pulse waveform, it can be used for a multilevel pulse waveform. At the individual FB-SM level t_p is substituted by t_x where t_x is the total insertion time for each individual FB-SM capacitor based on the discussed FIFO principle of insertion.

TABLE I
SPECIFICATIONS FOR THE SCALED-DOWN EXPERIMENTAL SETUP

Stage-I inverter frequency		16 kHz
Output peak-peak pulse voltage		1 kV
DC input voltage	V_s	25 V
Pulse repetition frequency	f_s	2 kHz
Input inductance	L_{in}	10 μ H
Transformers secondary turns	n	20
Number of FB-SMs	N	5
Load resistance	R	500 Ω
FB-SM capacitance	C_{SM}	10 μ F
Percent voltage ripple	β	0.98
Safety factor	α	1

IV. EXPERIMENTAL VALIDATION

A scaled-down experimental setup consisting of five FB-SMs is used to validate operation and the flexibility of the proposed PG. The experimental setup parameters are given in Table I, while Fig. 6 shows rig details. The stage-I H-bridge inverter is shown in Fig. 6(a), a module combining stages-II, III, and IV is depicted in Fig. 6(b), the five modules are shown in Fig. 6(c), and the complete setup is shown in Fig. 6(d). With five FB-SMs, the PG is able to generate a multilevel bipolar pulse waveform of up to six voltage levels ($N+1$) in each polarity. A six-level bipolar voltage pulse is shown in Fig. 7(a), where the FB-SM dc voltage is 100 V (hence, $nV_s/N = 100$ V) for the five FB-SMs successively inserted at 5- μ s intervals. The 500-V peak is for 20 μ s, when all the FB-SMs are inserted. With the reverse FB-SM sequencing process on the trailing edge, a pulse $t_p = 60$ μ s of 500-V peak is impressed across the load.

The voltages of three FB-SM capacitors are shown in Fig. 7(b). The capacitor voltages balance around 100 V, and immediately after contributing to a pulse-polarity generation, all started to charge. The 100-V charging level for the FB-SM capacitor is obtained from rectifying the stage-II square ac voltage of each FB-SM. Since the dc voltage input is 25 V, the output square ac voltage from stage-I inverter has a peak voltage of 25 V, as shown in Fig. 8, which also shows the typical primary current of the stage-II transformers.

By inserting the five FB-SM capacitors simultaneously in series, a rectangular pulse waveform of 20 μ s is generated from the proposed PG as shown in Fig. 9(a), while the capacitor voltages of three FB-SMs are shown in Fig. 9(b). The pulse transition time is limited not by absolute delays, but delay variation between FB-SMs and IGBT rise and fall time variations. The flexibility of inserting and bypassing the FB-SM capacitors without affecting their voltage balance allows generating pulses of combined null periods (no intervening zero period between two successive opposite polarity pulses).

Fig. 10(a) and (b) shows two six-level voltage pulses, where the null load voltage durations between the negative and positive-pulse polarities are combined, when the FB-SM capacitors are inserted at the pulse peak for 20 and 5 μ s, respectively.

Combined null load voltage durations in the case of rectangular pulses with different positive and negative dura-

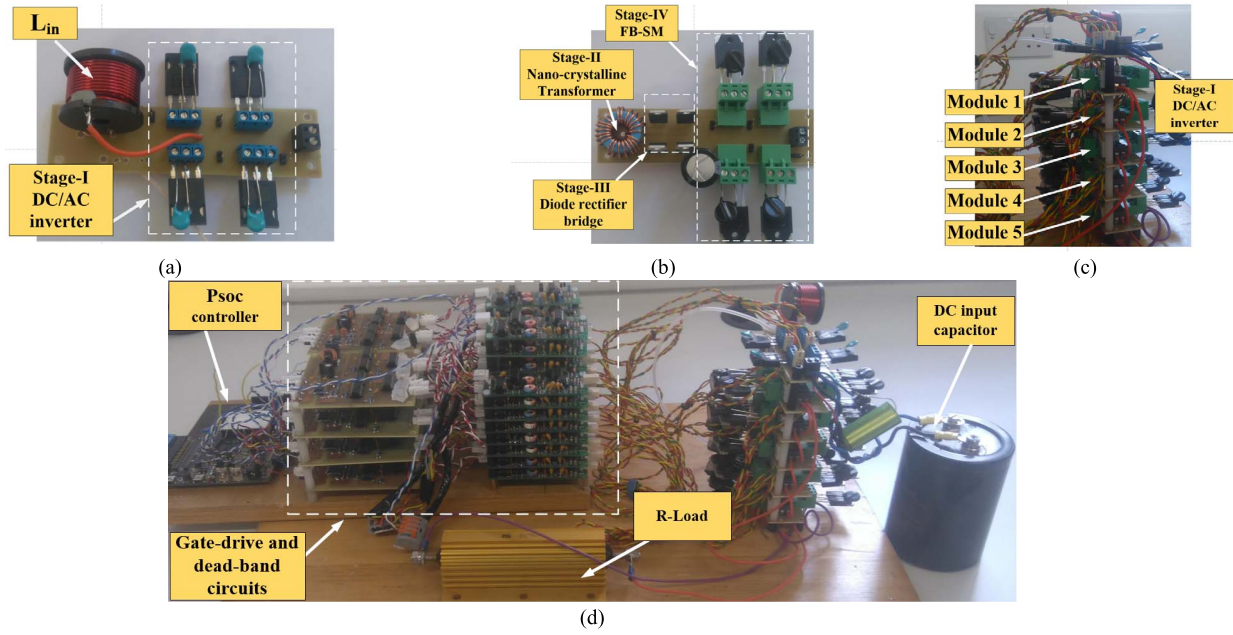


Fig. 6. Scaled-down experimental setup. (a) Stage-I H-Bridge inverter. (b) Complete module of stages-II, III, and IV. (c) Complete five modules. (d) Complete experimental test rig.

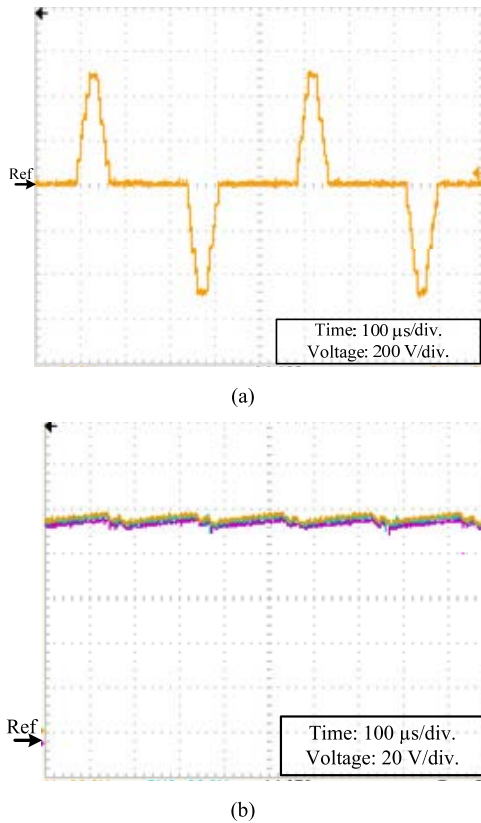


Fig. 7. Experimental results for the multilevel pulse. (a) 500-V pulse. (b) Three FB-SM capacitor voltages.

tions (30 and 10 μ s, respectively) are shown in Fig. 11(a). Not only different positive and negative pulse durations can be generated by the proposed PG, but also different magnitudes (+500 and -300 V) are possible, as shown in Fig. 11(b). In Fig. 11(b), two FB-SMs are bypassed during negative pulse-polarity generation, hence, the peak of the positive-pulse polarity is 500 V and the peak of the negative pulse polarity is 300 V, each of 10- μ s duration. Fig. 11(c)

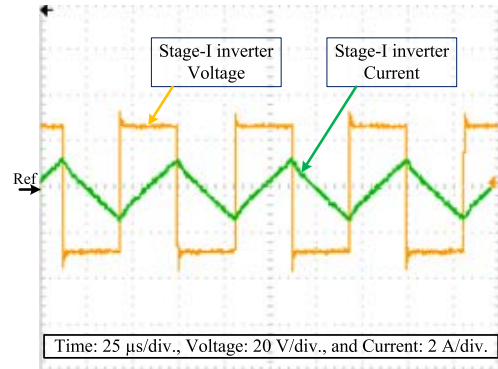


Fig. 8. Experimental results of stage-I inverter voltage and current waveforms.

shows the voltages of three FB-SM capacitors, where one is bypassed. In Fig. 11(c), the bypassed FB-SM capacitor voltage is near 100 V (as it only contributes to positive-pulse generation for 10 μ s), while the other two capacitors contribute to generating both pulse polarities.

Finally, by inserting all the FB-SM capacitors simultaneously on the rising edge then bypassing them sequentially on the falling edge, the proposed PG is able to create ramp pulse waveforms (which mimic conventional exponential pulse waveforms). The generated trailing edge ramp pulse waveform is shown in Fig. 12(a) and the capacitor voltages of three FB-SM capacitors are shown in Fig. 12(b).

V. PROPOSED TOPOLOGY ASPECTS AND LIMITATIONS

A. Transformer Series Primary Isolation Technique Aspects

A key aspect of the proposed PG, hence an attribute, is that each FB-SM is powered via a separate transformer, but with a single coupled primary source. By using a single primary turn (a common conductor passing through the core longitudinal axis as shown in Fig. 2), HV properties of isolation and low interwinding capacitance are obtained.

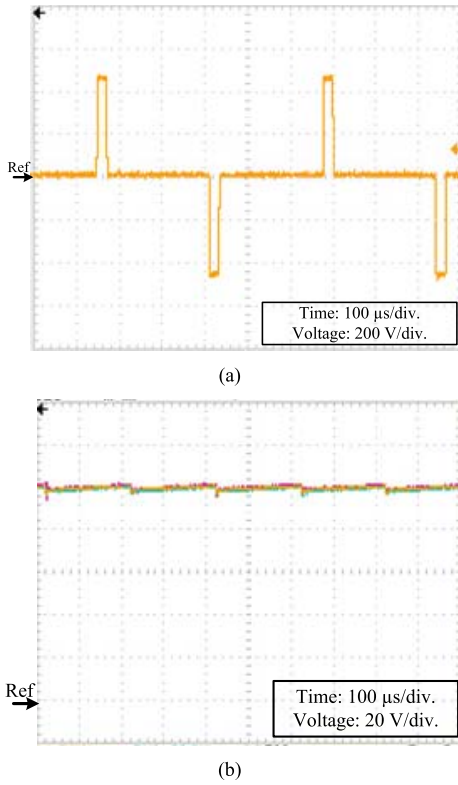


Fig. 9. Experimental results for the rectangular pulse. (a) 500-V pulse. (b) Three FB-SM capacitor voltages.

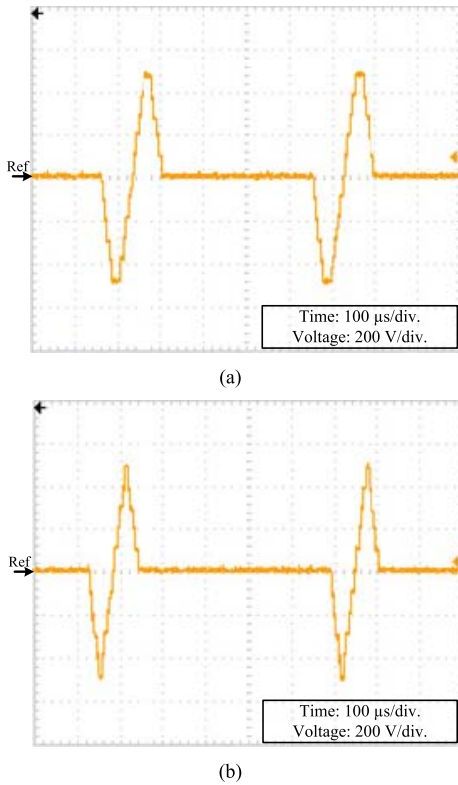


Fig. 10. Experimental results for combined null multilevel ± 500 V pulses. (a) With a 20- μ s pulse-peak duration. (b) With a 5- μ s pulse-peak duration.

For scaling to high power, the H-bridge dc to square wave ac generator should operate in two modes. The first mode is a current control mode, by utilizing inductor L_{in} (and its current as feedback) in Fig. 2 and transformer leakage, and

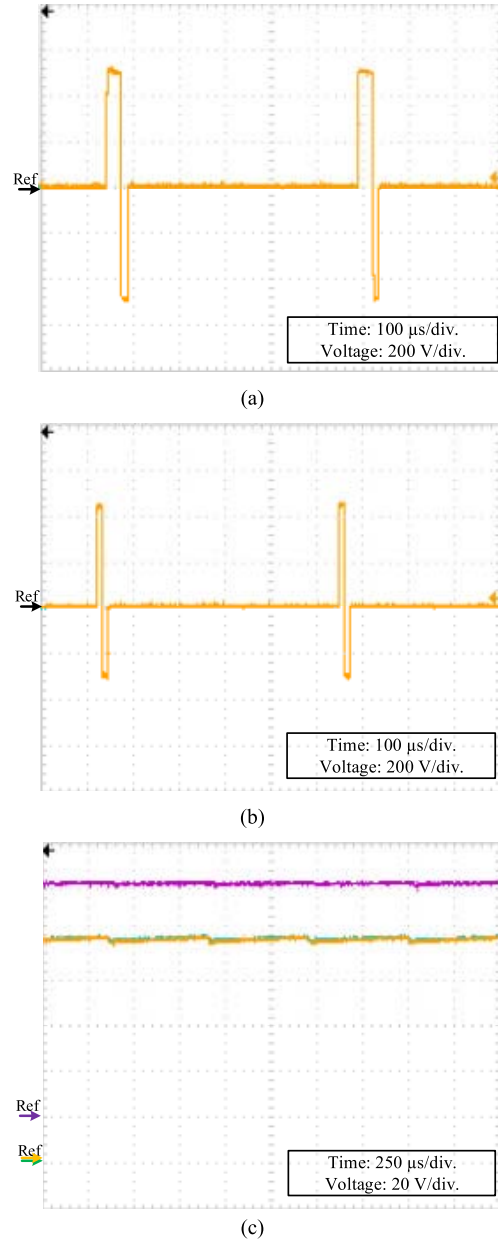


Fig. 11. Experimental results for the combined null load voltage rectangular pulses. (a) Positive and negative pulse durations of 30 and 10 μ s, respectively. (b) Positive and negative pulse-peak voltage of +500 and -300 V, respectively. (c) Three FB-SM capacitor voltages.

the second mode is as a voltage controller by decreasing the switching frequency or bypassing L_{in} .

The current control mode is used to initially charge the system capacitors from 0 V to nV_s/N . The current control mode is key to maintaining FB-SM capacitor voltage balance. In a current control mode, the transformer acts like a current transformer, where $\Sigma ni = 0$ and $V_{SM} < nV_s/N$ conditions dominate. This means all the primary energy is transferred to the FB-SM with the lowest capacitor voltage. Thus, progressively all the FB-SM capacitors charge to a level where voltage transformer conditions dominate, that is $V_{SM} = nV_s/N$ control ensures all capacitors have the same voltage, but an FB-SM with a voltage higher than nV_s/N receives no charge. Capacitor voltage balance is assured because the lowest voltage FB-SM capacitor(s) will always charge to nV_s/N , while a

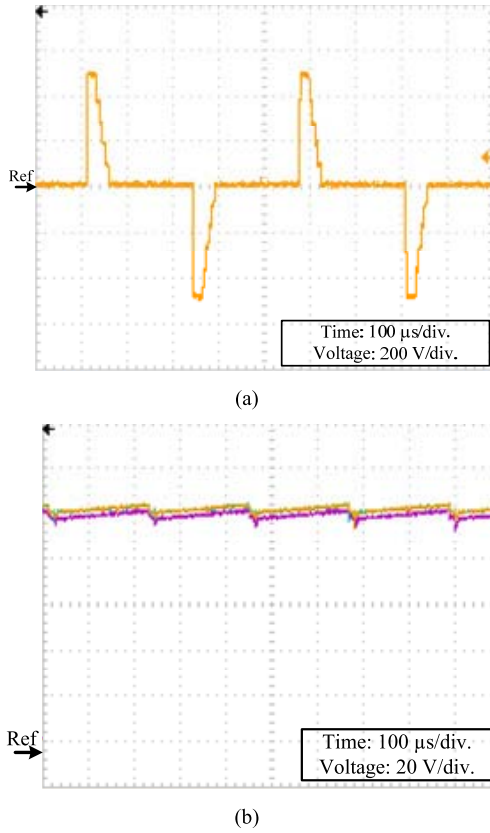


Fig. 12. Experimental results for the ramp trailing edge pulse. (a) 500-V pulse. (b) Three FB-SM capacitor voltages.

capacitor voltage(s) $V_{SM} > nV_s/N$ will not increase because the secondary output appears as an open-circuit condition.

At modest power levels, a compromise on the magnitude of L_{in} can avoid the need for two mode control of the H-bridge. Specifically, inductance is large enough to limit peak currents (particularly at system FB-SM capacitor initial charge up), but small enough to minimize the loss at the maximum output voltage (since it adds to transformer leakage inductance), at a given frequency.

B. Factors Affecting FB-SM Capacitance Sizing

Basically, HV pulse specification is determined by the application and the load requirements. The factors are mainly the pulse-peak voltage V_p , the repetition time T_s , and the pulse duration time t_p . Based on these and the load resistance R , the FB-SM capacitance can be estimated as in (6). However, two factors will affect capacitance as follows:

- 1) the capacitor voltage droop after contributing to the generated pulse;
- 2) the neglected semiconductor voltage drops and circuit parasitic resistances.

These two factors are considered in (6) by introducing two variables β and α . β is the percent remaining capacitor voltage after contributing to the pulse. The voltage across the capacitor will be restored to $V_{SM} = nV_s/N$ after contributing to the pulse (of peak voltage nV_s), then this cycle will be continued every T_s . This voltage fluctuation is the capacitor voltage ripple. A common practice allows a voltage ripple up to 0.1 pu. Consequently, the minimum remaining voltage is 0.9 pu. Thus, the suggested values of β will range from 0.9 to 1 pu.

With the selected value of β , the equivalent capacitance will control the droop. However, the neglected voltage drops and parasitic resistance may affect the designed droop adversely if not compensated. Accordingly, since all the parameters in (6) are fixed, the safety factor α is used to increase the FB-SM capacitance if the droop level is not satisfactory. Initially, the safety factor is set to $\alpha = 1$, the droop value is tested, if it is not satisfactory, α is increased.

C. Pulse Generation Limitations

The ability of the proposed HV-PG to generate the required pulse waveforms at high repetition rates depends on the following factors:

- 1) the speed of the selected controller in executing the control software instructions, such that the total software execution time is less than the required pulse repetition time;
- 2) the turn ON/OFF delay times (and mismatch) of the power semiconductor switches and their gate drives.

Rectangular as well as ramp pulses may require accurate turning ON/OFF timing of the semiconductor switches. Timing deviation may be evident in the practical generation of pulses. A solution is to precompensate the gate signal timing by software control such that actual switching OFF/ON timings are matched.

Increasing or decreasing the number of the MMC FB-SMs has no effect on the dc input supply (other than its current rating). Increasing the number of the FB-SMs will provide flexibility of pulse-waveform generation by creating N levels, and will provide redundant FB-SMs in the case of failure and will allow reducing the voltage rating of the semiconductor switches. In contrast, the minimum number of FB-SMs is ultimately dependent on the desired HVDC level as well as the voltage rating of the semiconductor switches and their turn ON/OFF speed.

VI. CONCLUSION

This paper presented a new PG topology-based separately sourced MMC FB-SMs. With a dedicated charging circuit for each FB-SM capacitor, no voltage balancing technique for the FB-SM capacitors is required. Individual capacitor charging is obtained from three successive stages, namely, conversion of a common LVDC input voltage to a high-frequency ac voltage square wave, step-up and isolation of the ac voltage level via nanocrystalline step-up transformers, and rectification of the secondary transformer ac voltage by a diode FB rectifier. HV bipolar pulses are formed across the load in the fourth stage via series connected FB-SMs. Thus, the proposed topology is modular and scalable. Not only rectangular pulse waveforms can be generated, but multilevel pulses with controlled dv/dt and ramp pulses are possible. Along with pulse generation flexibility, the FB-SM capacitance is relatively small, which reduces converter footprint. With five modules (each module is formed of a nanocrystalline transformer, a diode FB connected to the FB-SM capacitor, and an FB-SM), a scaled-down rig produced different pulse shapes at peak-to-peak pulse voltages of 1 kV. This establishes the viability of the proposed topology for PEF applications.

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The statements made herein are solely the responsibility of the authors.

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