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A sub 1V bandgap reference circuit

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A Sub 1 V Bandgap Reference Circuit

by

Ashish A Digvadekar

A Thesis submitted in Partial Fulfillment of the

Requirements for the Degree of

MASTERS OF SCIENCE

In

Electrical Engineering

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A journey is easier when you travel together. Interdependence is certainly more valuable than independence. I have worked on this thesis for more than a year. I owe the completion of this thesis to a countless number of people. It is impossible to mention all the names here but I would definitely take this opportunity to thank the following people who have guided, encouraged, motivated and helped me through the different phases of the thesis.

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ABSTRACT

This thesis proposes a novel technique for a low supply voltage temperature-independent reference voltage. With the scaling of supply voltages, the threshold voltages don't scale proportionally and thus low supply reference circuits have replaced the conventional bandgap reference circuit. The first chapter of this work discusses the conventional bandgap references (The Widlar and Brokaw references). The terminology used in the bandgap world is introduced here. The second chapter investigates the existing low supply voltage reference circuits with their advantages and the limitations. A table discussing all the investigated circuits is provided towards the end of the chapter as a summary.

Chapter Three proposes a novel technique to generate a temperature-independent voltage which does not use an operational amplifier. This chapter also provides a mathematical understanding for behavior of the circuit. Chapter Four talks about two variations of the proposed architecture. These variations are designed in order to improve the performance of the proposed circuit against power supply variations. Each one of them has its own merits and drawbacks. Finally Chapter Five discusses the effects of process variations and transient response of the proposed circuit. A digital trimming scheme using an EE-PROM is proposed to manage almost all of the process variation effects on the circuit.

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Introduction

1.1 Introduction

1.1.1 Zener Based Voltage Reference

1.1.2 Bandgap Voltage Reference

1.2 Bandgap terminology

1.3 Classical Bandgap Circuits – Widlar and Brokaw

1.3.1 Widlar Bandgap reference

1.3.2 Brokaw Bandgap reference

1.4 Bandgap reference principle

1.1 - INTRODUCTION

Voltage reference circuits are precision references which exhibit little dependence on supply voltage variations and process parameters and a well defined dependence on temperature. These references are very important for the accurate working of various circuits like data converters, PLL's, dynamic random access memories (DRAM's) and oscillators. The resolution of an A/D or D/A converter is limited by the precision of its reference voltage over the circuit's supply voltage and operating temperature ranges. Thus the precision voltage reference forms an integral part of almost all circuit designs.

Some of the desired characteristics of a voltage reference are:-

- a) Ability to be implemented in silicon.
- b) Accuracy and stability over supply voltage & time.
- c) Proper startup value.
- d) Accurate over a wide range of temperature.

The two most popular voltage references are:-

- a) Zener-based Voltage reference
- b) Bandgap Voltage reference

1.1.1 Zener-based voltage reference

The simplest and the conventional form of a voltage reference is the Zener-based voltage reference. Here the Zener diode operates in the reverse bias region and current begins to flow in it at a specific voltage (around 6 V) and thereafter the current increases rapidly with the increase in voltage. Thus, to use it as a reference a constant current is required. This is provided through a resistor from a higher supply voltage.

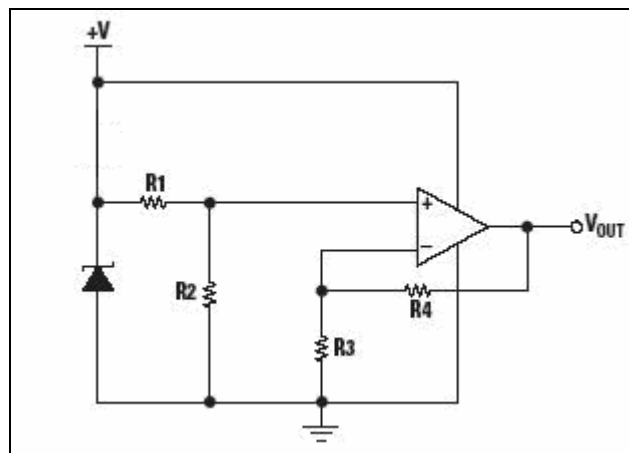


Figure 1.1 – Buried Zener reference circuit

Figure 1.1 [12] shows a buried Zener voltage reference where the diode is biased by a current source. The resistors R1 and R2 form a resistor divider network across the Zener diode. The divided voltage is applied to the non-inverting terminal of an operational amplifier whose output is the reference voltage. The gain of the amplifier is decided by the resistor values R4 and R3. The expression for the output is

$$V_{out} = \frac{R2}{R1 + R2} \left(1 + \frac{R4}{R3} \right) \times V \quad (1.1)$$

They are called buried diodes as they are fabricated beneath the surface of the chip. The ones fabricated on the surface are noisier as they can get contaminated easily. The buried diode references are more expensive than the bandgap references but are more accurate. Buried Zener diodes can be made with a range of voltages and have good low noise performance (better than bandgap references), but the ones that, in combination with their temperature compensating diodes, have a breakdown voltage just below 7 V, have the best temperature performance.

But their biggest limitation is the minimum supply voltage required. They need a supply voltage of at least 6 V. In today's technology the supply voltages are always shrinking and 6 V is just not the norm. Thus these types of references are no longer used.

1.1.2 Bandgap Voltage Reference

A Bandgap reference circuit is one where two quantities with opposite temperature coefficients are added with a proper weighing factor to result in a temperature coefficient of approximately zero. This can be explained as two quantities B_1 and B_2 having opposite temperature coefficients and choosing the coefficients c_1 and c_2 in such a way that

$$c_1 \frac{\partial B_1}{\partial T} + c_2 \frac{\partial B_2}{\partial T} = 0 \quad (1.2)$$

Thus the reference voltage $V_{out} = c_1 V_1 + c_2 V_2$ has a zero temperature coefficient.

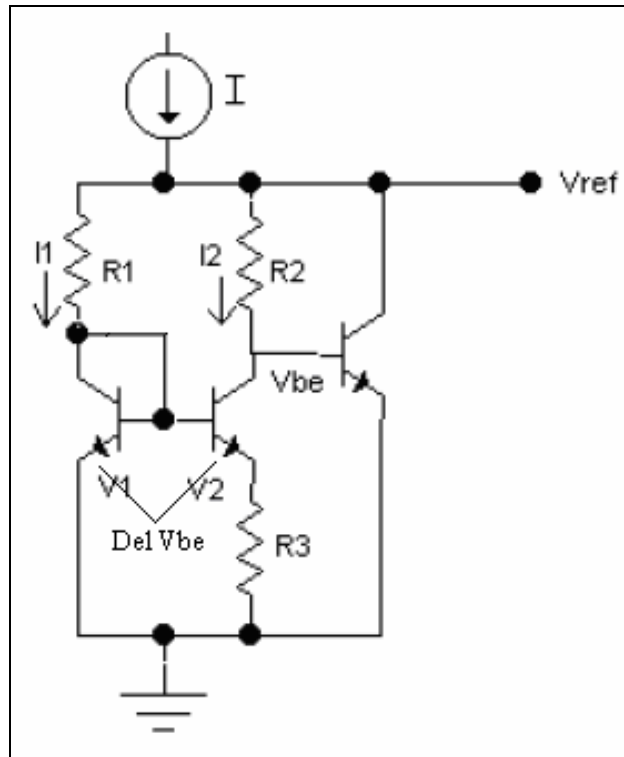


Figure 1.2 – Basic Bandgap Circuit

Figure 1.2 shows a bandgap circuit in its very basic form. Here the V_{be} , which has a negative temperature coefficient is complementary to absolute temperature and the ΔV_{be} is proportional to absolute temperature and a weighted addition of both results in the V_{ref} with a near zero temperature coefficient. All the terminology is discussed in the next section.

1.2 - BANDGAP TERMINOLOGY

a) Bandgap Voltage

Bandgap voltage of a semiconductor measured in eV refers to the potential energy difference between the valence band and the conduction band for that semiconductor. It has a nearly constant value and its variation with temperature is small. Each type of a semiconductor has a unique bandgap. Typically for silicon its value is approximately 1.17 eV.

b) PTAT Voltage

PTAT stands for proportional to absolute temperature which means that the quantity varies proportionally with absolute temperature - *i.e.*, the quantity increases with absolute temperature. Most of the bandgap reference circuits use the difference in the V_{be} 's of two transistors operating under same current densities as the PTAT voltage.

c) CTAT Voltage

CTAT stands for complementary to absolute temperature which means that the quantity varies complementary to absolute temperature - *i.e.*, the voltage decreases with absolute temperature. Most of the bandgap reference circuits because of its linearity use the V_{be} of a transistor as the CTAT voltage.

d) Bandgap Reference circuit (BGR)

A bandgap reference circuit is one which does a weighted addition on the PTAT voltage with the CTAT voltage to have an end result having a near-zero temperature coefficient. This resulting voltage is equal to the bandgap voltage of the semiconductor at the reference temperature.

e) Parts per million (PPM)

Reference-accuracy unit used commonly with precision voltage reference designs. Designers typically use this measure to specify temperature coefficients and other parameters that change little under varying conditions. For a 2.5 V reference, 1 ppm is one-millionth of 2.5 V, or 2.5 μ V. If the reference is accurate to within 10 ppm, then it is extremely good performance for any voltage reference.

f) Power Supply Rejection Ratio (PSRR)

PSRR is defined as the ability of the circuit to maintain its output voltage as its power-supply voltage is varied. The PSRR for a Bandgap reference circuit can be calculated by the equation

$$PSRR = 20 \log \left(\frac{\Delta V_{POWER-SUPPLY}}{\Delta V_{BANDGAP-OUTPUT}} \right) \text{ in dB} \quad (1.3)$$

1.3 - CLASSICAL BANDGAP CIRCUITS – WIDLAR AND BROKAW

1.3.1 Widlar Bandgap reference

The first bandgap reference was proposed by Robert Widlar in 1971 [2] as shown in Figure 1.3 below. It used conventional junction isolated bipolar technology to make a stable low voltage (1.220 V) reference. Early MOS implementations of these voltage references were based on the difference between the threshold voltages of enhancement and depletion mode MOS transistors [3]. This provides low temperature coefficient (TC); however, the drawbacks are that the output is not easy to control because of the direct dependence on the doses of ion implantation steps and, further depletion mode transistors are not available in most CMOS processes.

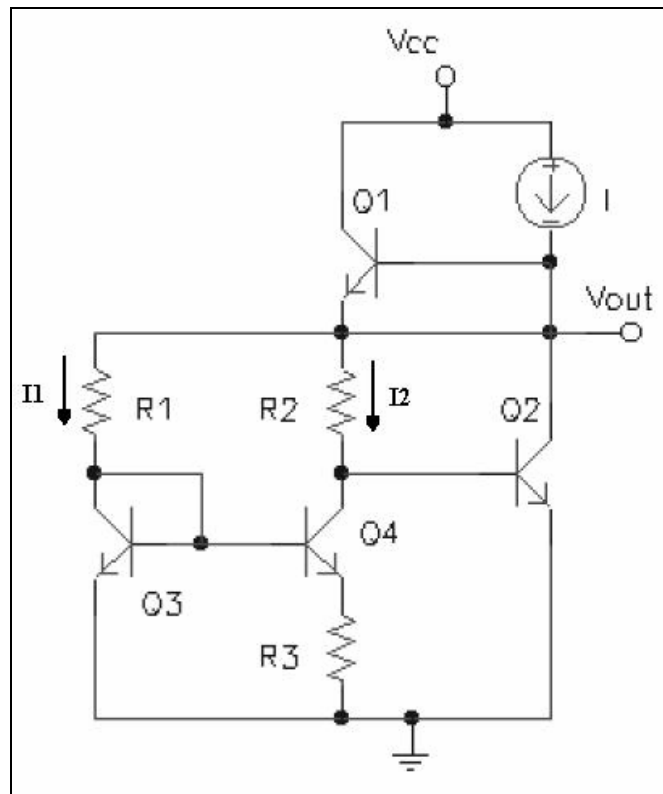


Figure 1.3 – Widlar bandgap reference[2]

The Widlar circuit shown above operates as explained with equations below:

$$V_{BE3} = V_{BE4} + I_2 R_3 \quad (1.4)$$

$$\therefore V_{BE3} - V_{BE4} = I_2 R_3 \Rightarrow \Delta V_{BE} = I_2 R_3 \quad (1.5)$$

But,

$$\Delta V_{BE} = V_{thermal} \ln\left(\frac{I_1}{I_{S1}}\right) - V_{thermal} \ln\left(\frac{I_2}{I_{S2}}\right) = V_{thermal} \ln\left(\frac{I_1 I_{S2}}{I_2 I_{S1}}\right) \quad (1.6)$$

Assuming that $V_{be3} = V_{be2}$, this implies $I_1 R_1 = I_2 R_2$

$$\therefore I_2 = \frac{\Delta V_{BE}}{R_3} = \frac{V_{thermal}}{R_3} \ln\left(\frac{I_1 I_{S2}}{I_2 I_{S1}}\right) = \frac{V_{thermal}}{R_3} \ln\left(\frac{R_2 I_{S2}}{R_1 I_{S1}}\right) \quad (1.7)$$

$$\therefore V_{OUT} = I_2 R_2 + V_{BE2} = \frac{R_2}{R_3} V_{thermal} \ln\left(\frac{R_2 I_{S2}}{R_1 I_{S1}}\right) + V_{BE2} = K V_{thermal} + V_{BE2} \quad (1.8)$$

R_1 , R_2 and R_3 can be manipulated to achieve the desired value of K .

Drawbacks of the basic four-transistor circuit include the fact that the reference output voltage cannot be changed. Also the performance of the circuit depends heavily on the current density in Q_2 which will change if the circuit is loaded.

1.3.2 Brokaw Bandgap reference

Paul Brokaw made his bandgap reference [13] by solving many of the problems in the Widlar reference. Figure 1.4 below shows the Brokaw bandgap reference circuit. The circuit has two transistors and collector current sensing to form the basic bandgap voltage. The output voltage can be expressed as

$$V_{OUT} = V_{BE1} + \text{Voltage_across_} R_1 \quad (1.9)$$

$$\therefore V_{OUT} = V_{BE1} + 2 \frac{R_1}{R_2} \left(\frac{kT}{q} \ln \left(\frac{A_1}{A_2} \right) \right) \quad (1.10)$$

Here A_1 and A_2 are the areas of Q_1 and Q_2 respectively.

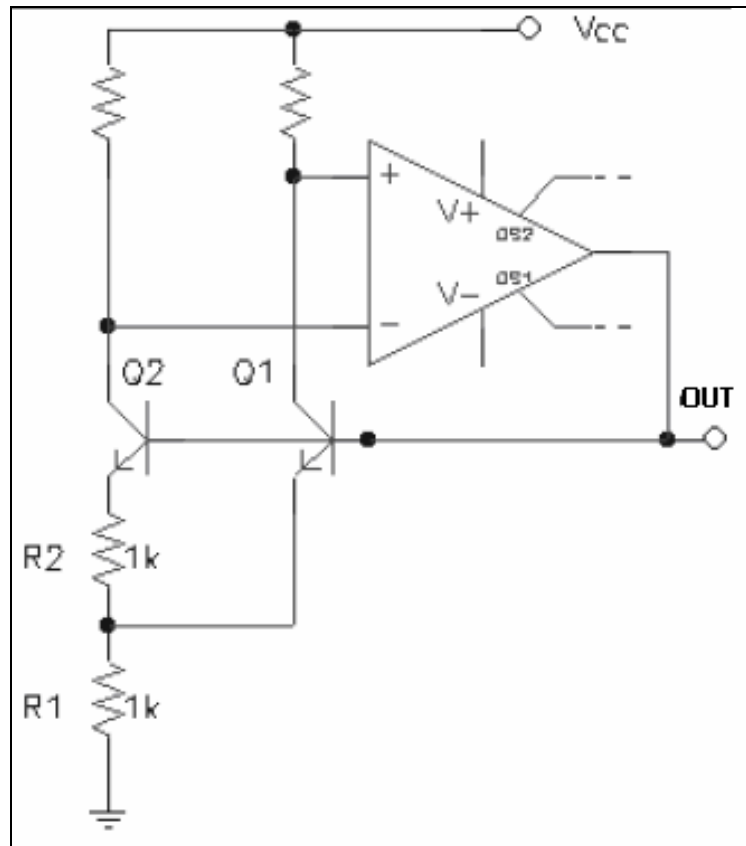


Figure 1.4 – Brokaw Bandgap reference [13]

The reason for the voltage across R_1 having a positive temperature coefficient is that the currents through both the transistors are equal, thus acts like a PTAT. The V_{be} acts as a CTAT. The proper weighted addition of both the quantities leads to a temperature invariant V_{out} which is the bandgap reference output.

1.4 - BANDGAP REFERENCE PRINCIPLE

Most of the modern bandgap reference circuits are made on the Paul Brokaw school of thought. Thus every bandgap reference will result from the weighted addition of a PTAT voltage with a CTAT voltage. For this they rely on well transistors. These are vertical bipolar transistors that use wells as their bases and substrate as their collectors. These are shown in Figure 1.5 below.

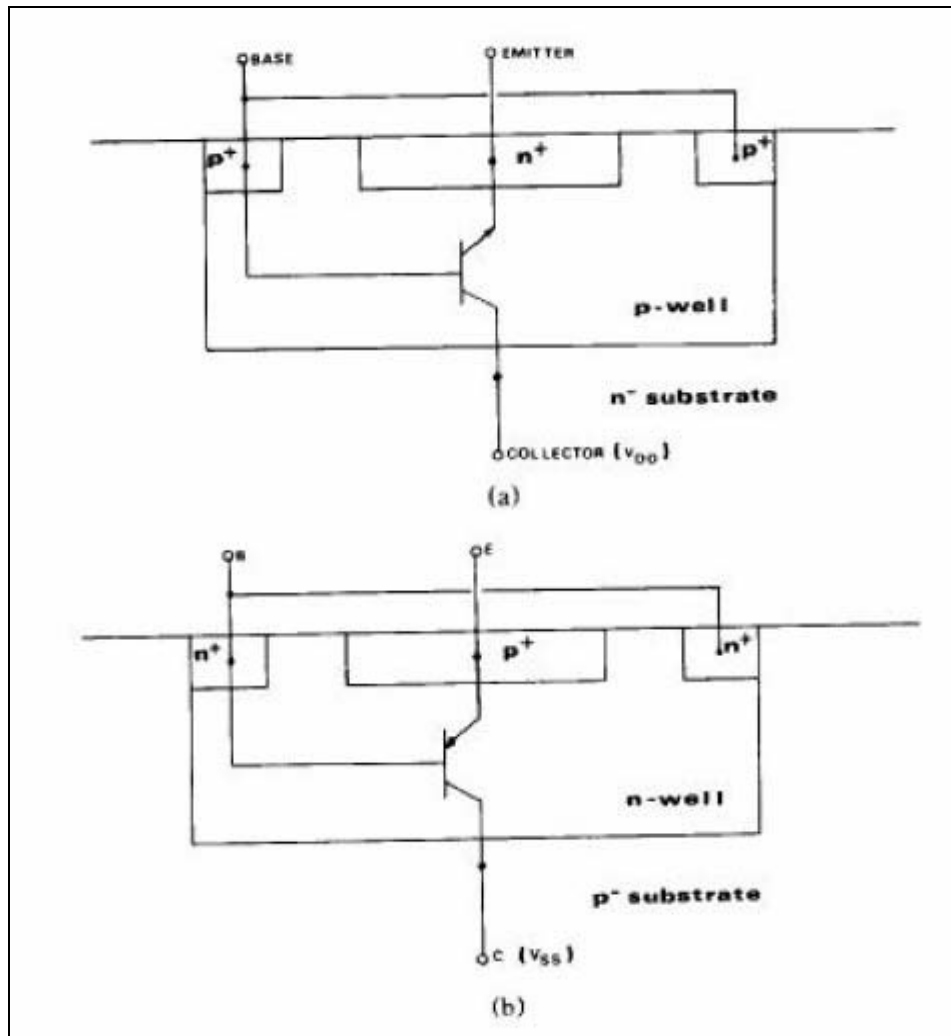


Figure 1.5 - a) Vertical NPN transistor b) Vertical PNP transistor

A conventional bandgap [4] reference circuit is shown in the Figure 1.6. The output of the circuit is given by the equation:

$$V_{OUT} = V_{BE2} + \Delta V_{BE} \frac{(R_3 + R_2)}{R_3} \quad (1.11)$$

$$\therefore V_{OUT} = V_{BE2} + V_t \ln n \left(1 + \frac{R_2}{R_3} \right) \quad (1.12)$$

Here n is the ratio of the sizes of the two bipolar junction transistors and V_t is the thermal voltage. The first term represents the CTAT voltage and the second term represents the PTAT voltage.

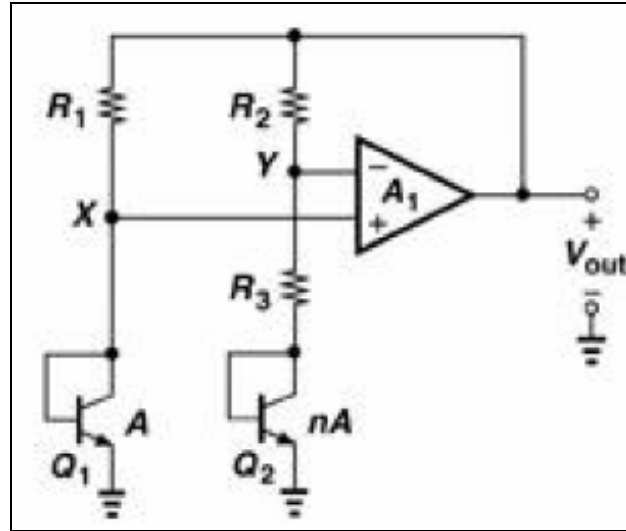


Figure 1.6 – Conventional BGR circuit [4]

The output voltage for a conventional BGR is 1.26 V. The output here is from an opamp. Even if we consider a simple two stage opamp, the minimum supply voltage is the output V_{out} plus the V_{DSsat} drop across the output stage transistor. This is around 1.4 to 1.5 V depending upon the technology.

Background of Low Supply Voltage BGR's

- 2.1 Background of Low Supply Voltage Bandgap Reference**
 - 2.2 Resistor Divider Network**
 - 2.3 Current Summing and a voltage summing Circuits**
 - 2.4 Transimpedance Amplifier**
 - 2.5 Dynamic Threshold MOS (DTMOS)**
 - 2.6 Depletion transistors**
 - 2.7 Threshold Voltage based circuit**
 - 2.8 Low Voltage BGR Comparison**
-

2.1 - BACKGROUND OF LOW SUPPLY VOLTAGE BANDGAP

REFERENCES

As the technology scales, so do the supply voltages. The supply voltages recently tend to be in the range of 0.9 V – 1.2 V. The supply voltage scales with the technology, but the threshold voltage of the transistors does not scale at the same rate. This makes it difficult to incorporate conventional designs of bandgap reference circuits to processes having supply voltage near 1 V. Here arises the need to come up with new topologies of bandgap reference to operate properly in the low supply voltages. For the low voltage bandgap reference design the following approaches have been used:

- 1) Resistive divider networks
- 2) Current summing and a voltage summing circuits
- 3) Transimpedance amplifier
- 4) Dynamic Threshold MOS (DTMOS)
- 5) Depletion transistors
- 6) Threshold voltage based circuit
- 7) Bandgap using two V_{be} sources

2.2 RESISTOR DIVIDER NETWORK

The resistive divider network proposed by Banba [5] is shown in the Figure 2.1. The concept here used was to sum two currents (instead of voltages in the conventional BGR circuits). The forward bias voltage of the diodes is defined as V_F . One of the currents is proportional to V_F , which is the CTAT here, and the other current is proportional to V_T . The circuit configuration is shown in Figure 2.1 below. Here the diodes can be replaced with PNP transistors available in the today's processes.

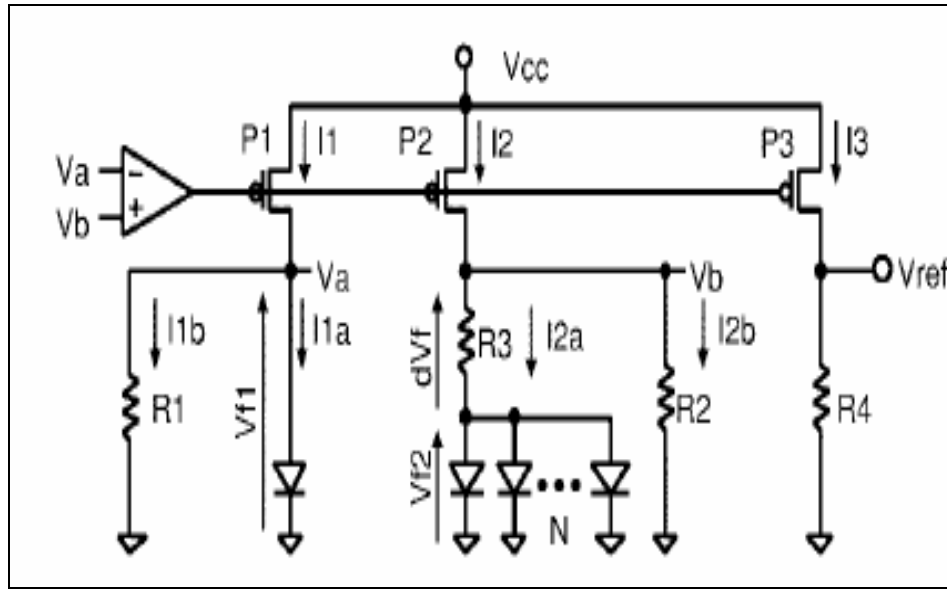


Figure 2.1 – BGR using Resistor divider network [5]

Here,

$$V_{REF} = R_4 \left(\frac{V_{F1}}{R_2} + \frac{dV_F}{R_3} \right) \quad (2.1)$$

The value of V_{REF} can be adjusted by altering the values of R_4 , R_3 and R_2 .

The circuit was designed for a reference voltage of 515 mV. V_{REF} showed a variation of 515 mV \pm 1 mV for the supply variation of 2.2 to 4 V at 27°C; and 515 mV \pm 3 mV for temperature variation from 27 to 125°C as shown in Figure 2.2 below. However the minimum supply voltage was limited to 2.1 V.

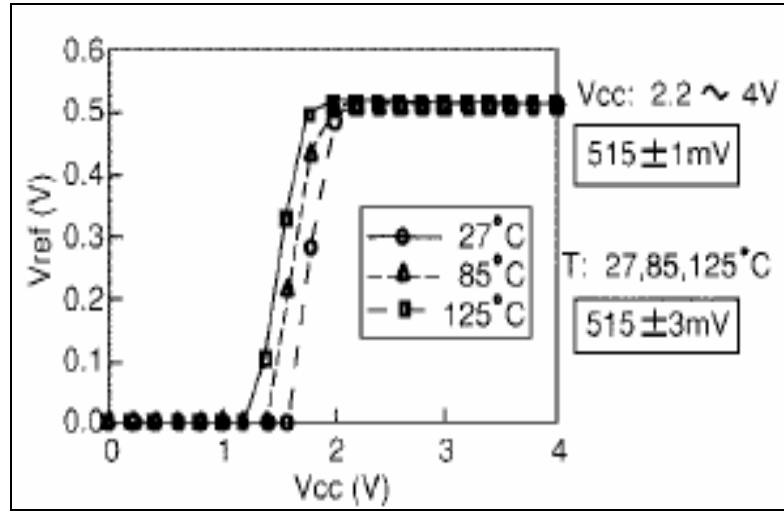


Figure – 2.2 Measured V_{REF} characteristics of the proposed BGR [5]

Several modifications were proposed to the circuit presented in [5]. In one of the modifications by Waltari [6], the sub-1 V operation is achieved by folding the circuit in Figure 2.1 at nodes Va and Vb. The problem in this circuit is that the nodes Va and Vb are at a voltage of 0.7 V and this is not suitable for a low voltage opamp. The voltage at these nodes is reduced with the help of a resistor divider network as shown below in Figure 2.3.

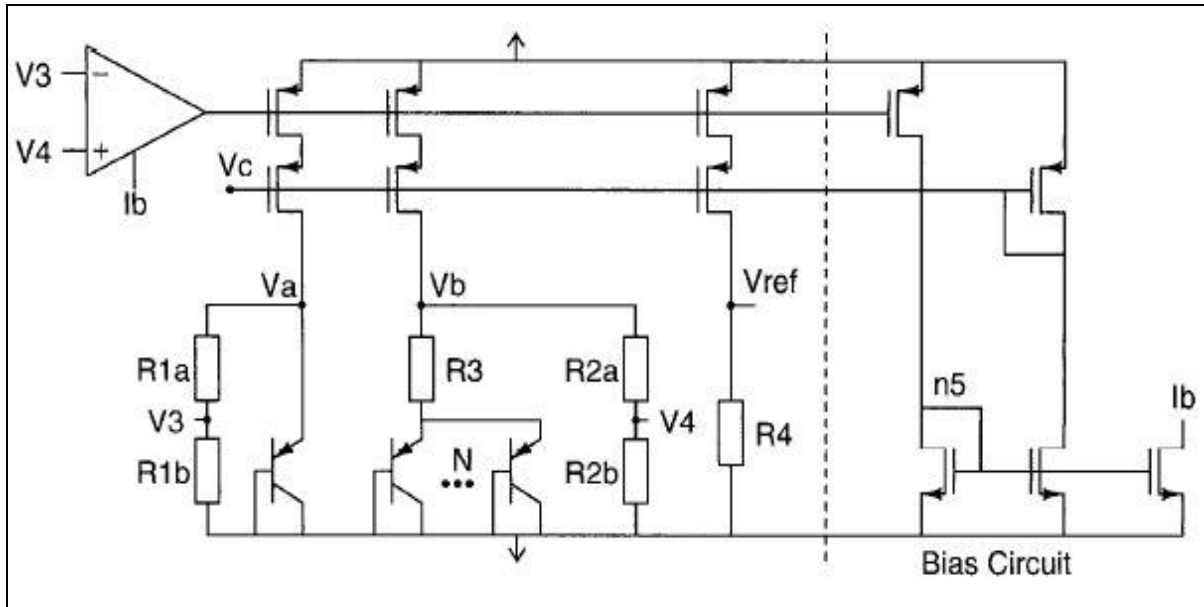


Figure 2.3 – Low Voltage BGR as presented by [6]

The voltage at the nodes V_a and V_b is now 150 mV – 200 mV due to the resistive divider network of R_{1a} , R_{1b} , R_{2a} and R_{2b} . The output impedance of the current source is improved by using cascade configuration. This also helps to maximize the PSRR of the circuit. The simulation results are shown in Figure 2.4. The TC variation was observed to be less than 0.24%.

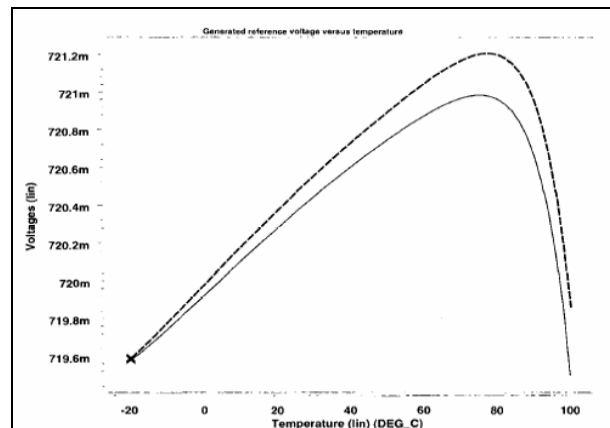


Figure 2.4 – Generated reference voltage versus temperature using a 0.95 V (solid curve) and a 1.5 V (dashed curve supply voltage) [6]

2.3 CURRENT SUMMING AND A VOLTAGE SUMMING CIRCUITS

Ripamonti [7] talks about two different configurations capable of sub-1 V supply voltage BGR circuits. The first technique operates by summing two currents with opposite temperature dependence on a resistor, and the resistor value further controls the reference voltage. The second technique sums two voltages that are first attenuated, where resistive voltage dividers are used for the determination of the attenuation factor. The circuit that sums two currents is given in Figure 2.5.

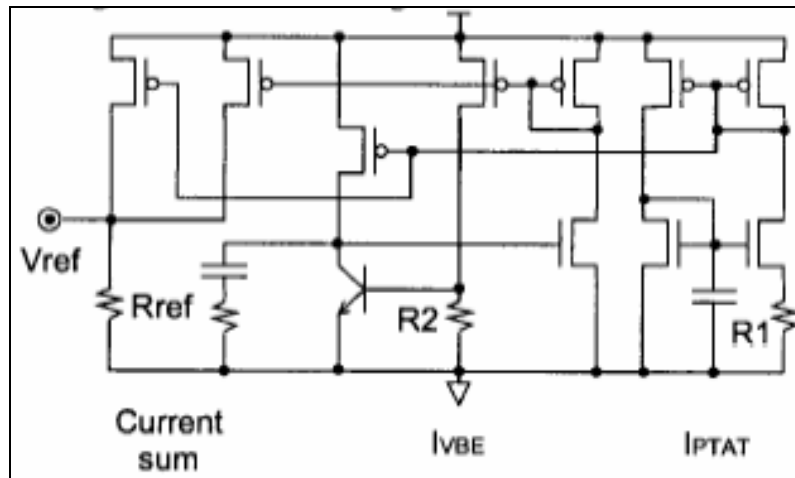


Figure 2.5 – Current Summing BGR [7]

The circuit is divided into three sub-blocks. The first generates current PTAT by using the MOS operating in the sub threshold region. The second block produces current CTAT. The third block is a resistor where both the currents are added. The major advantage of the circuit is that the supply voltage here is the addition of the drop across the forward biased diode and the V_{DS} of the transistor, which are 0.7 V and 0.2 V respectively. Thus the supply voltage can be as low as 0.9 V. A major drawback of the circuit is its extremely low PSRR. Figure 2.6 below shows the temperature dependence of the bandgap output.

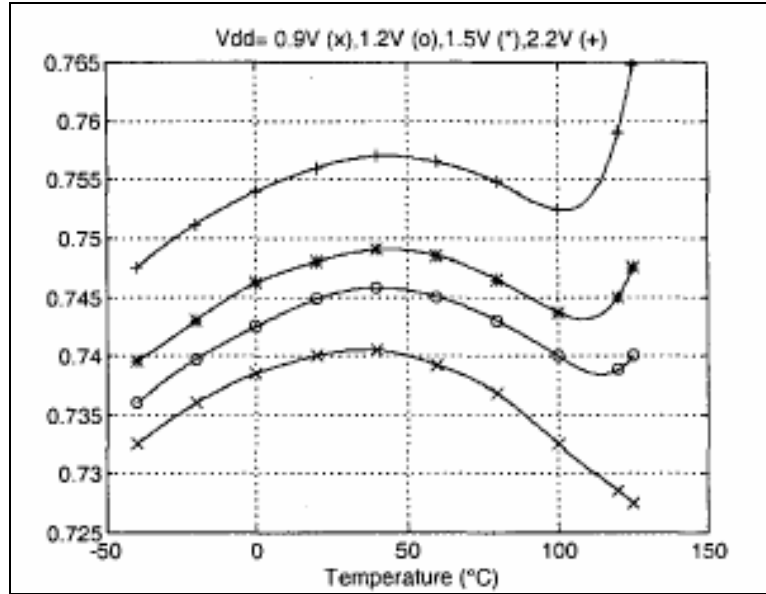


Figure 2.6 – Temperature Variation of the BGR in the current summing circuit [7]

The voltage summing BGR in Figure 2.7 is also composed of three sub circuits. The only difference between the current summing BGR and the voltage summing BGR is the third sub-circuit. The third section is composed of a differential amplifier in a non-inverting feedback loop. The offset voltage from the use of unmatched bipolar transistors generates the PTAT component. The applied diode voltage is not the full base-emitter voltage, as in a standard BGR, but a fraction. The minimum supply voltage of one path is V_T plus a V_{CEsat} , plus the source to drain voltage of the current source. The second path's minimum supply voltage is a V_{BE} plus the minimum voltage of the current source plus the output voltage of the V_{BE} generator. This value is equal to 1 V with the technology that was used in this study.

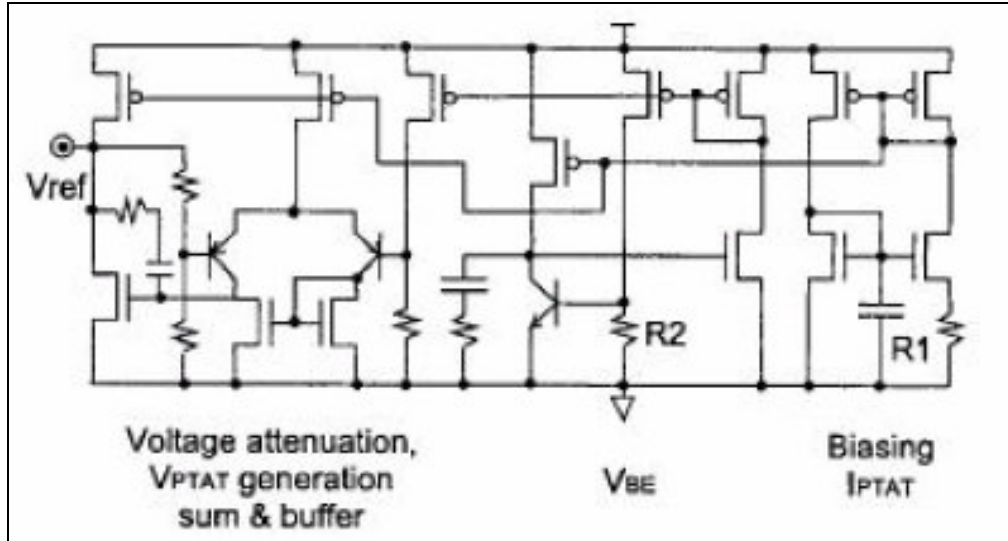


Figure 2.7 – Voltage Summing BGR [7]

Variations in reference voltage with supply voltage and temperature are plotted in Figure 2.8. The output voltage was found to vary by less than 0.5% over the 0.9 V to 2.5 V range. In the same range the temperature dependence varied by 2%.

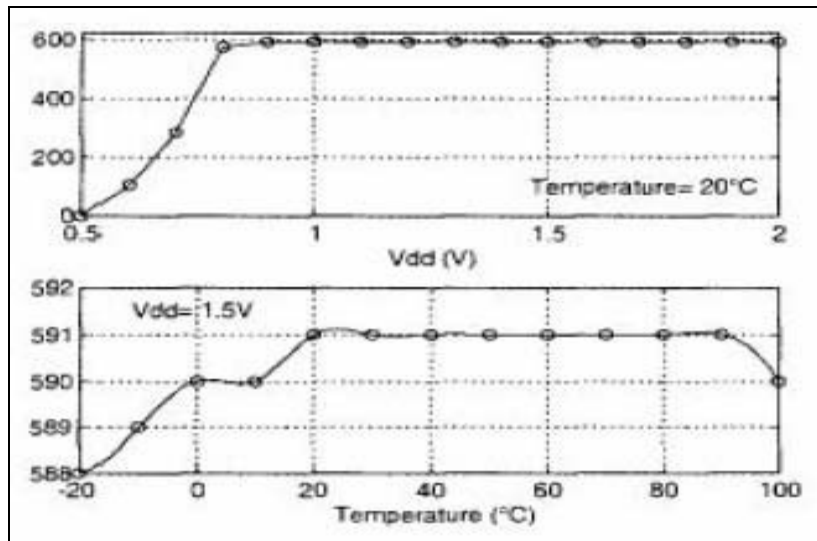


Figure 2.8 a) VREF vs. VDD b) VREF vs. Temperature [7]

2.4 TRANSIMPEDANCE AMPLIFIER

The conventional BGR circuit is limited by the input common mode range of the operational amplifier. Jiang [8] proposes another improvement to the circuit described by Banba [5], as depicted in Figure 2.9. Here resistors are used in place of input differential stage of the opamp. They are used to obtain a PTAT current by sensing the voltage difference and the current is summed with a current complementary to V_{EB} to obtain the reference voltage. This technique is based on the use of a Transimpedance amplifier.

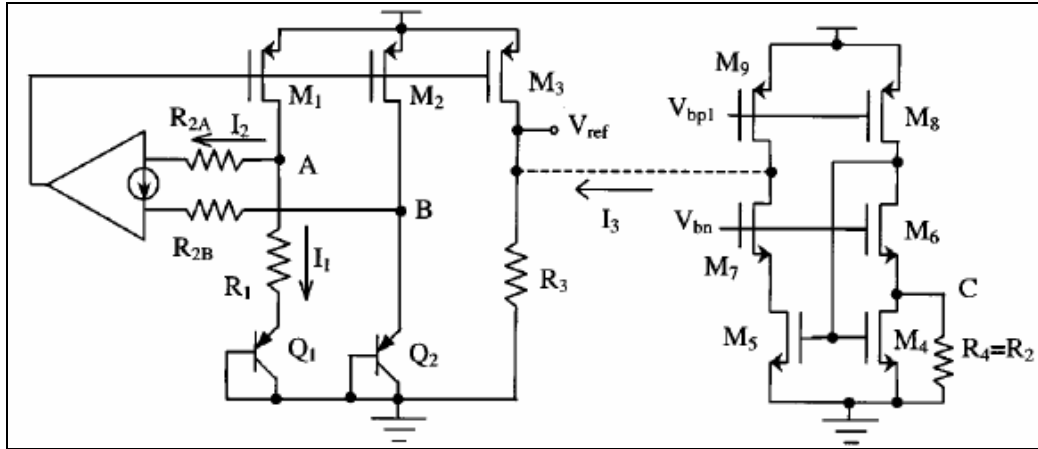


Figure 2.9 – Transimpedance Amplifier using BGR [8]

The value of V_{REF} here is given by

$$V_{REF} = R_3 \left[\frac{1}{R_1} V_T \ln \left(\frac{A_1}{A_2} \right) + \frac{V_{BE}}{R_2} - \frac{V_B}{R_2} \right] \quad (2.2)$$

Here A_1 and A_2 are the areas of transistors Q_1 and Q_2 respectively. The value of V_{ref} can be changed by choosing different values of R_1 , R_2 , and R_3 . The measured V_{REF} is shown in Figure 2.10.

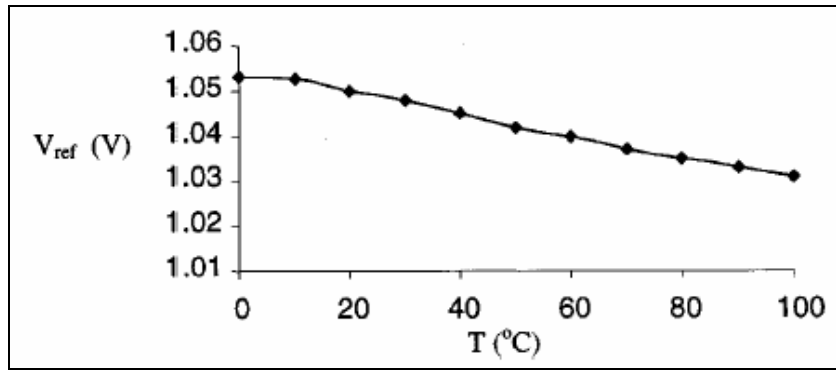


Figure 2.10- Measured VREF characteristics without trimming [8]

2.5 DYNAMIC THRESHOLD MOS (DTMOS)

Annema [9] talks about another method of low power, low voltage BGR design through the use of dynamic threshold MOS (DTMOS) devices. As we have seen, the bandgap for low power applications can be made to appear smaller through resistive subdivision, but it is at the expense of area. The bandgap can also be made to appear smaller if the junction is in the presence of an electrostatic field. The electrostatic field lowers the bandgap. This method can be implemented by replacing the normal diodes with MOS diodes that have interconnected gates and back gates. These devices are DTMOS devices; a cross-section is shown in Figure 2.11. The use of a P-DTMOS device results in a V_{G0} of 0.6 V and the temperature gradient of V_{GS} is approximately $-1 \text{ mV}/^\circ\text{K}$. These values are half the typical values of a standard BGR.

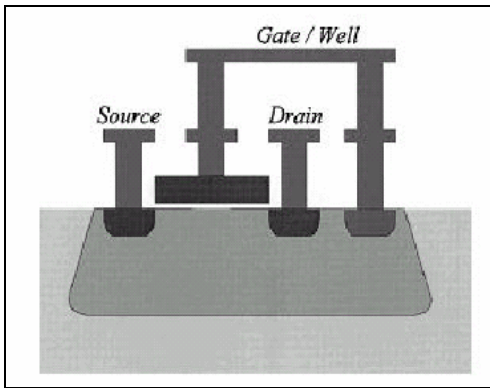


Figure 2.11 – DTMOS Cross-section [9]

A DTMOS BGR can be designed using the same topology as a standard CMOS BGR. Figure 2.12 demonstrates such a circuit. The circuit consists of a folded cascode opamp and matched resistors with unequal value. The DTMOS diodes are shown with the gate-substrate connection. The input stage also utilizes DTMOS transistors, which allows operation at low

supply voltages. The opamp's output stage, shaded, uses a low voltage current mirror. Correct operation of this opamp was verified for supply voltages down to 0.7 V.

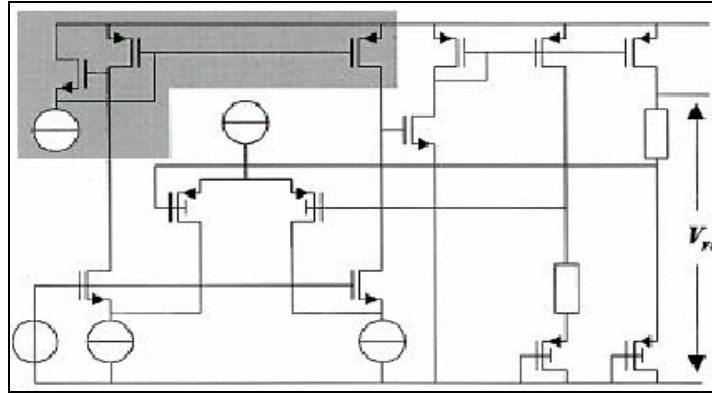


Figure 2.12 – Low Voltage DTMOS BGR [9]

The circuit's temperature dependence is shown in Figure 2.13. The variation over the range, -20°C to 100°C, is just 4.5 mV.

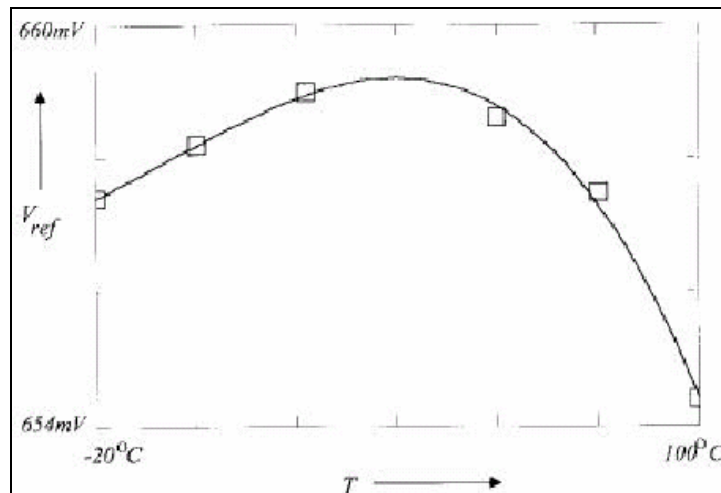


Figure 2.13 – VREF v/s temperature [9]

2.6 DEPLETION TRANSISTORS

Pierazzi [10] made opamp that used PMOS in the depletion mode in order to cope with the supply voltage reduction. Thus the circuit cannot be fabricated in regular low cost CMOS technologies that usually do not have these special devices. This opamp uses PMOS in the weak inversion and is shown in Figure 2.14. A diode-connected PMOS transistor loads the second gain stage. Thus, the biasing of the opamp is derived from the output voltage and thus this maximizes the PSRR of the whole opamp but at the cost of low voltage gain.

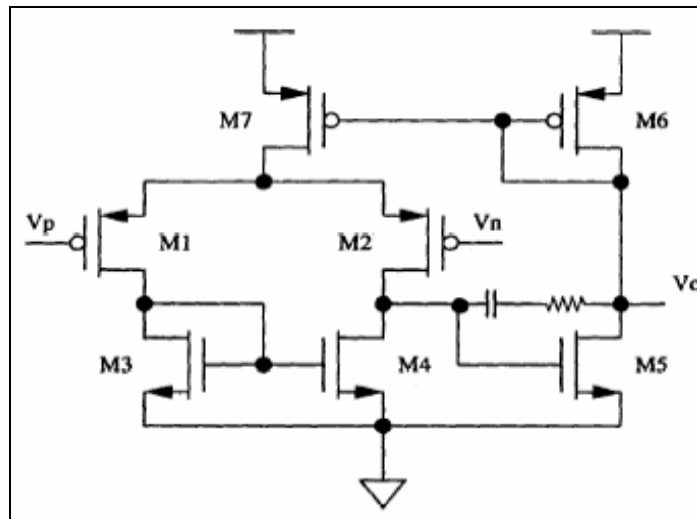


Figure 2.14 – OpAmp using transistors in depletion mode [10]

The input transistors work in strong inversion at a supply voltage of around 1.4 V. Below this voltage the transistors drop into a weak inversion. The bias current is reduced to a few nanoamps at a supply voltage of 1 V. As seen from Figure 2.15 below the supply voltage of 0.9 V there is no longer enough loop gain to keep the BGR at correct bias point.

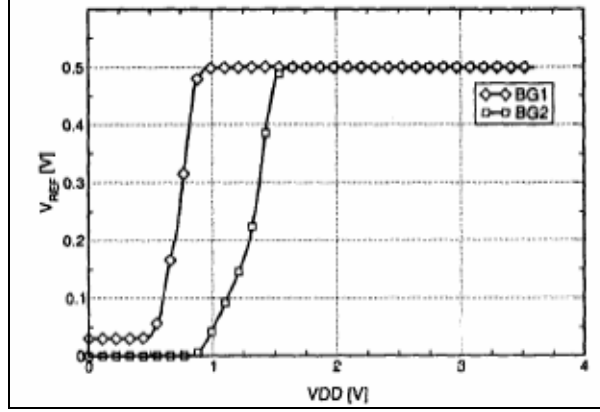


Figure 2.15 - Simulated output voltages at 27°C at different supply voltages. BG1 is the curve of our interest. [10]

The BGR was implemented in 0.35 μm CMOS technology. The measured V_{REF} vs supply voltage for various temperatures is shown in Figure 2.16. The measurements suggest a minimum supply voltage of 0.9 V.

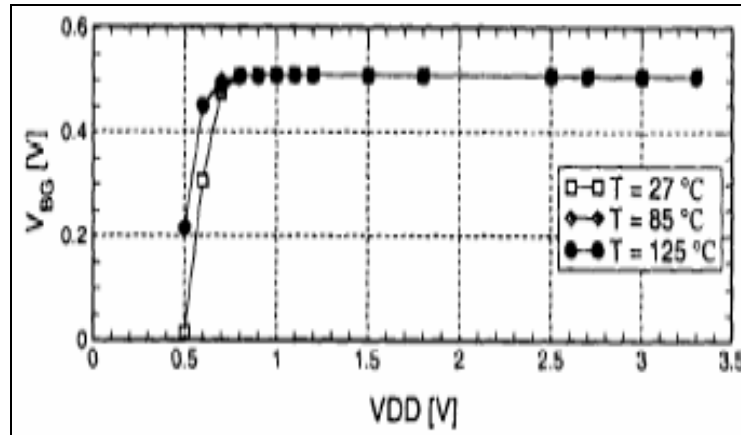


Figure 2.16 - Measured V_{REF} vs supply voltage for various temperatures [10]

2.7 THRESHOLD VOLTAGE BASED CIRCUIT

Ytterdal [11] introduces the new concept of threshold voltage based voltage references. The basic idea here is to compensate the temperature dependency of the threshold voltage of a PMOS transistor with that of an NMOS transistor, both having a CTAT dependency. This concept is pictorially shown in Figure 2.17. The performance of the proposed BGR is shown to be comparable to bandgap circuits, but at the cost of more area and complexity.

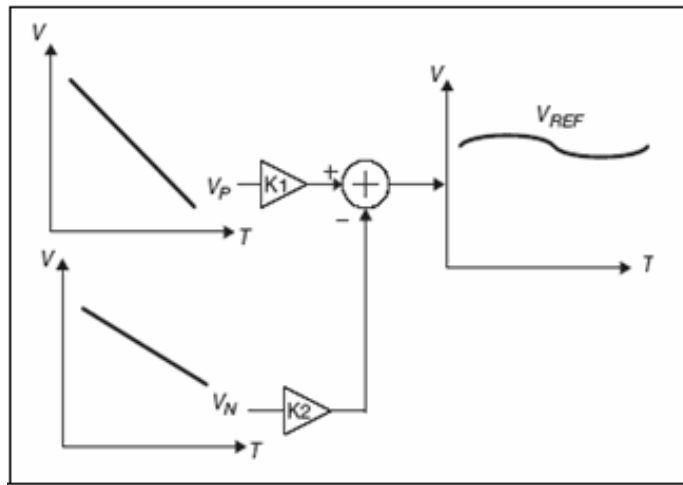


Figure – 2.17 Threshold Voltage BGR Concept [11]

The simulation results for the circuit made with this technique are shown in Figure 2.18.

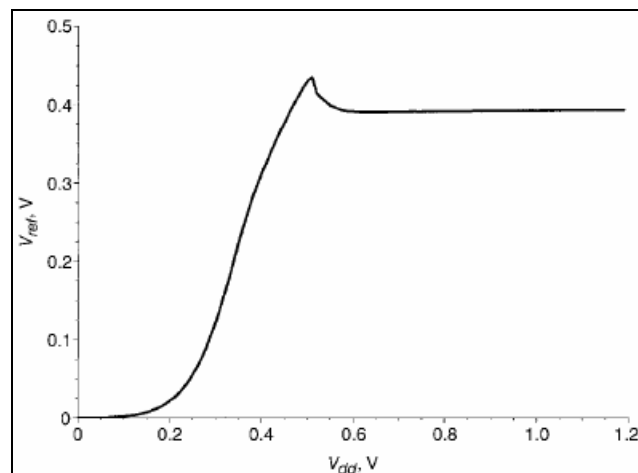


Figure 2.18 – Simulated BGR Output [11]

2.8 BANDGAP USING TWO VBE SOURCES

The work by Washburn [17] was driven by the motivation of developing a low voltage bandgap reference circuit having low power consumption, no dependence on TC of resistors, minimum number of critical components that need to be matched and usage of resistor arrays that are a multiple of a single resistance value.

The work in [17] exhibits a series of attainable circuit behaviors as discussed below:

- The ability to multiply PTAT voltage to get it to be almost equal to the CTAT voltage near the center of the desired operating temperature range.
- The voltage source like behavior of the multiplied PTAT voltage when dropped across a resistor having a impedance equal to that of the resistor value.
- If CTAT and PTAT voltages are connected as shown in Figure 2.19 then the value of the resistor on the CTAT side can be chosen in a way to have near zero TC at the junction of the two resistors.

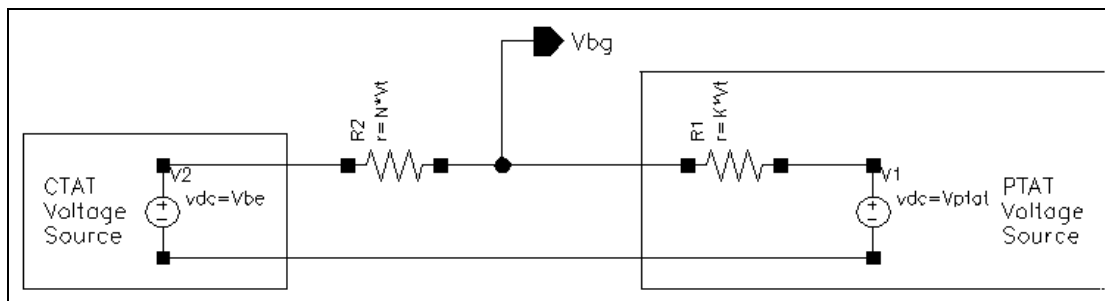


Figure 2.19 - Zero TC point [17]

- The using of two equal resistors meeting at V_{bg} to generate a stiff V_{be} voltage source as shown in Figure 2.20. This is conceptually explained in Figure 2.21.

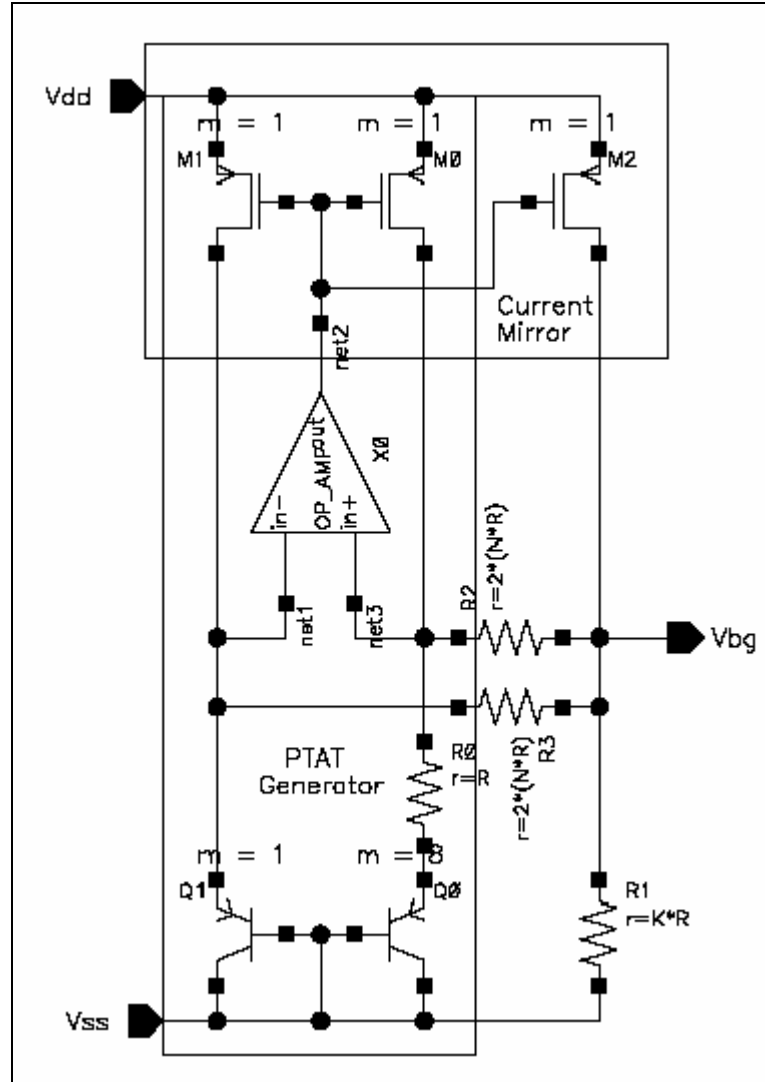


Figure 2.20 – Low voltage bandgap using two V_{be} sources [17]

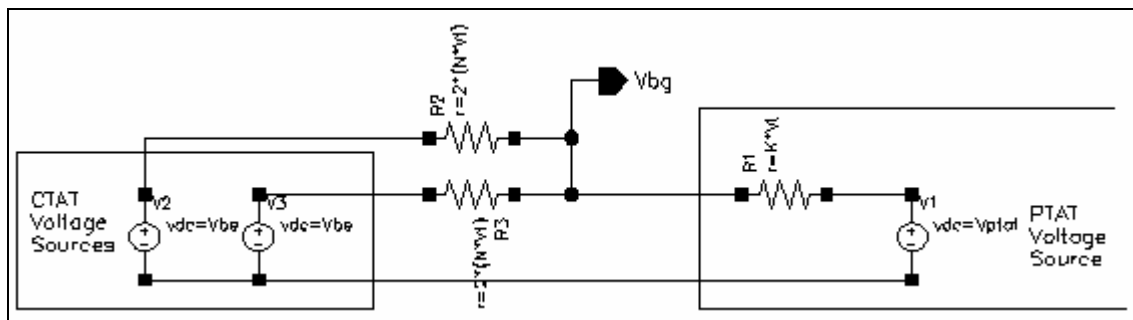


Figure 2.21 - Zero TC with two V_{be} sources [17]

The resulting output voltage is $V_{bg} = 0.6$ to 0.7 V depending upon the point of cancellation. The V_{be} (CTAT voltage) does not impose a limit on the voltage headroom. The headroom is limited by the mirrors. So according to [17] the minimum supply voltage depends upon the headroom needed for the mirrors to operate which is around 0.1 V in 90 nm technologies. So the supply voltage required is just above the output voltage V_{bg} .

[17] proposes a new resistor scheme where the resistors will be in the form of series and parallel stripes of a single resistor as shown conceptually in Figure 2.22 below.

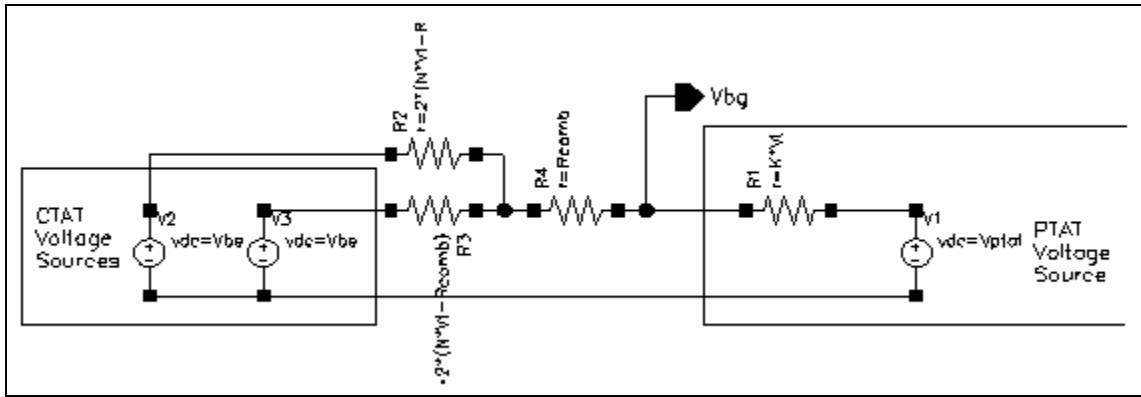


Figure 2.22 - Combining Vbe Resistors [17]

The proposed architecture removes the additional current path present in conventional BGR. The output voltage is almost independent of the resistor TC's and absolute value tolerances.

2.9 LOW VOLTAGE BGR COMPARISON

The work done on low supply voltage bandgap references was discussed in this chapter. All of them have their own advantages and drawbacks. Table 1 below compares the results from all the discussed works. This gives an overall idea on the performance of the individual circuit compared to the others in areas like technology used, minimum supply voltage, output voltage, ppm accuracy and the PSRR in dB.

Circuit type	Technology	Min. Supply Voltage (V)	Output Voltage (V)	Accuracy (ppm/°C)	PSRR (dB)
Resistor Divider (Banba)	0.4 μm CMOS	2.1 V	515 mV	± 59 ppm/°C	Not Mentioned
Resistor Divider (Waltari)	0.6 μm CMOS	0.95 V	720 mV	.24%. Not mentioned in ppm.	44dB at 10KHz
Current Summing (Ripamonti)	Not Mentioned	0.9V	521mv	2.4%. Not Mentioned in ppm.	Low
Transimpedance Amplifier (Jiang)	1.2 μm CMOS	1.2 V	1000 mV	+/- 100 ppm/°C	20dB at 1KHZ
DTMOS (Annema)	0.35 μm CMOS	0.85 V	650 mV	57 ppm/°C	Not Mentioned

Depletion Transistors (Peirazzi)	0.35 μ m CMOS	0.9 V	510 mV	Not Mentioned	Not Mentioned
Threshold Voltage Based (Ytterdal)	0.13 μ m Digital CMOS	0.55 V	400 mV	93 ppm/ $^{\circ}$ C	Not Mentioned

Table 1 – Comparison of Low Voltage bandgap references

Proposed Low Supply BGR Circuit

- 3.1 Proposed Low supply Bandgap Reference circuit**
 - 3.2 Operation**
 - 3.2.1 PTAT Current Generation**
 - 3.2.2 CTAT Current Generation**
 - 3.3 CTAT Voltage Generation at the base of current mirror transistors**
 - 3.4 Bandgap output Voltage**
-

3.1 PROPOSED LOW SUPPLY BANDGAP REFERENCE CIRCUIT

The proposed bandgap reference architecture is motivated by the requirement of a low supply voltage bandgap reference. The circuit can be represented in simplest form as shown below in Figure 3.1.

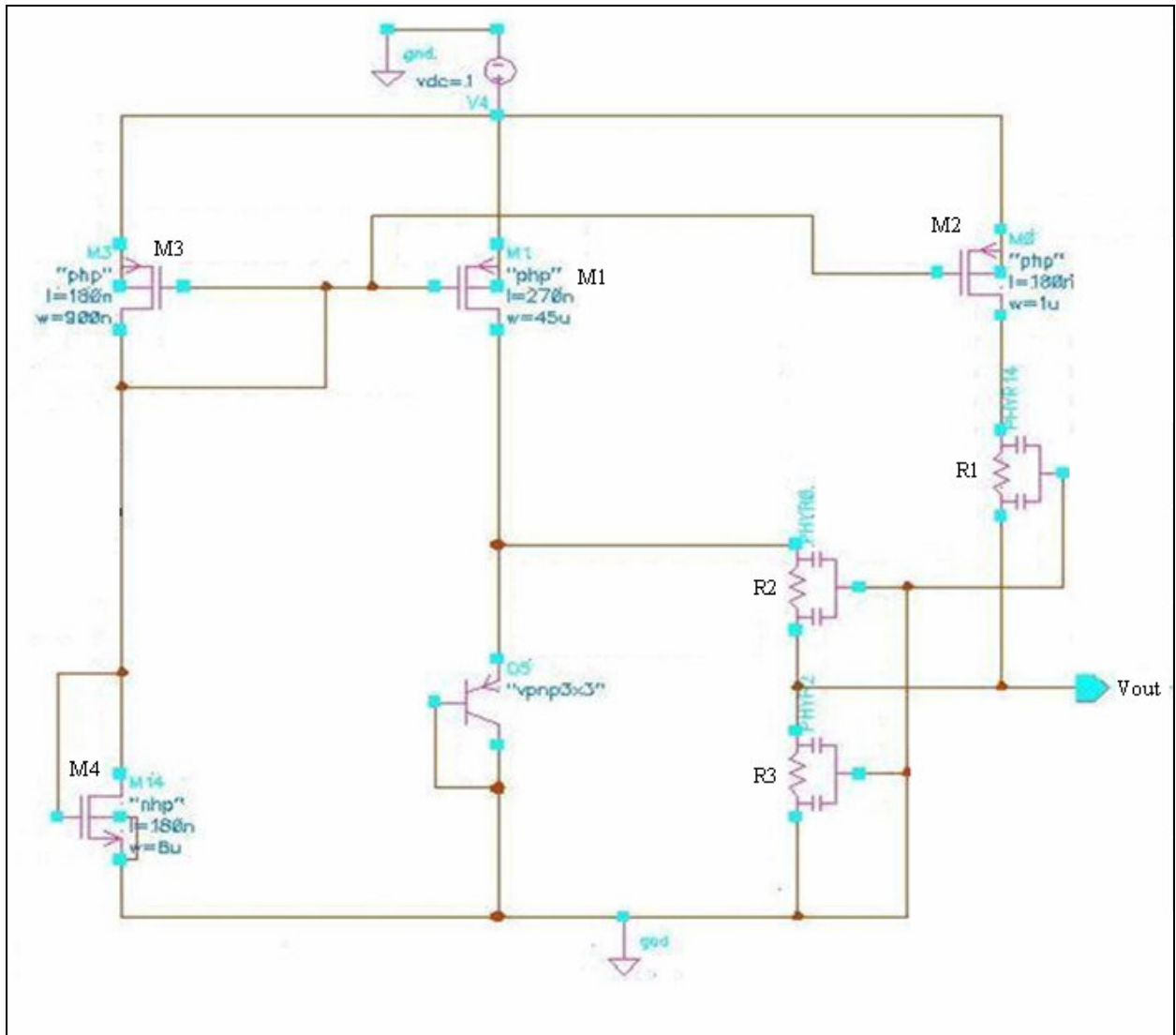


Figure 3.1 - Proposed bandgap reference in the simplest form

Briefly, the working of the circuit can be explained as the summation of two currents (one PTAT and the other CTAT) across the resistor R_3 . The diode-connected BJT makes a conventional CTAT current flow through the resistor combination R_2 and R_3 . The two diode connected transistors M_3 and M_4 are used for biasing. The voltage at the gate of the transistors in the current mirror is of CTAT type. This voltage at the gate of M_2 and the combination of the PMOS with a P+ poly resistor R_1 produces a PTAT current flowing through the combination R_1 and R_3 .

The circuit is designed using the LSI Logic 0.18 micron CMOS process. The parametric values of the various components used in the circuit are mentioned in Table 2 below. Here the resistors used are all different from each other. R_1 is P+ Poly resistor with a negative temperature coefficient. R_2 is a P+ Poly Silicided resistor with a positive temperature coefficient and R_3 is a Metal 1 resistor with a positive temperature coefficient.

Sr. #	Part #	Type	Value
1	M_1	PMOS	$W = 45 \mu\text{m}, L = 270 \text{ nm}$
2	M_2	PMOS	$W = 1 \mu\text{m}, L = 180 \text{ nm}$
3	M_3	PMOS	$W = 900 \text{ nm}, L = 180 \text{ nm}$
4	M_4	NMOS	$W = 8 \mu\text{m}, L = 180 \text{ nm}$
5	R_1	P+ Poly Resistor	29.4 K Ω
6	R_2	P+ Ploy Silicided resistor	16.92 K Ω
7	R_3	Metal 1 Resistor	7.46 K Ω

Table 2 – Component parameters of the proposed circuit

3.2 OPERATION

The operation of the circuit will be studied by dividing it into three simpler parts. The first part will explain the generation of the PTAT current and the second will explain the generation of the CTAT current. The third will explain the PTAT nature of the gate voltage of the current mirror transistors M_1 & M_2 .

3.2.1 PTAT Current Generation

The most conventional way of making the PTAT quantity is using the difference in the V_{be} 's of two PN junctions having different current densities. But this technique needs an operational amplifier to magnify the slope of the delta V_{be} . Here, a new technique is used to get the PTAT current.

Figure 3.2 below shows the circuit that generates the PTAT current.

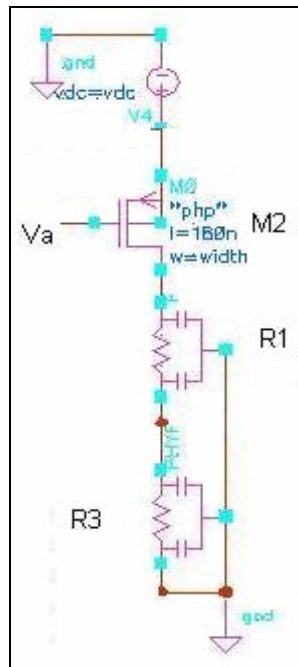


Figure 3.2 – Circuit for PTAT current generation

In the figure above the current in the resistors is given by the square law equation

$$I_D = \frac{1}{2} K_p' \left(\frac{W}{L} \right) (V_{GS} - V_T)^2 \quad (3.1)$$

where $K_p = \mu_0 C_{OX}$ for the transistor M_2 & V_T is the threshold voltage of the transistor.

$$\therefore I_D = \frac{1}{2} K_p \left(\frac{W}{L} \right) (V_{GS}^2 + V_T^2 - 2V_{GS}V_T) \quad (3.2)$$

$$\therefore \frac{\partial I_D}{\partial T} = \frac{1}{2} \left(\frac{W}{L} \right) C_{OX} \left[\left(\left(\frac{\partial \mu_0}{\partial T} \right) (V_{GS}^2 + V_T^2 - 2V_{GS}V_T) \right) + \mu_0 \frac{\partial}{\partial T} (V_{GS}^2 + V_T^2 - 2V_{GS}V_T) \right] \quad (3.3)$$

$$\therefore \frac{\partial I_D}{\partial T} = \frac{1}{2} \left(\frac{W}{L} \right) C_{OX} \left[\left(\frac{\partial \mu_0}{\partial T} \right) (V_{GS}^2 + V_T^2 - 2V_{GS}V_T) + 2\mu_0 (V_{GS} - V_T) \left(\frac{\partial V_{GS}}{\partial T} - \frac{\partial V_T}{\partial T} \right) \right] \quad (3.4)$$

In the above equation (4), there are three parameters that will decide the nature of the current

versus temperature. They are $\frac{\partial \mu_0}{\partial T}$, $\frac{\partial V_{GS}}{\partial T}$ & $\frac{\partial V_T}{\partial T}$.

μ_0 is the mobility of the carriers. Temperature appears explicitly in the value of surface mobility for the MOSFET model. The temperature dependence for the mobility as explained in [14] is determined by:

$$\mu_0(T) = \frac{\mu_0(T_0)}{\left(\frac{T}{T_0} \right)^{1.5}} \quad (3.5)$$

Thus the mobility decreases with the increase in temperature.

$\frac{\partial V_{GS}}{\partial T}$ has a slope of around $393.09 \mu\text{V}/^\circ\text{C}$. This would be derived in a later section.

$\frac{\partial V_T}{\partial T}$ here has a slope of about $-65 \mu\text{V}/^\circ\text{C}$ as seen from simulation results for this specific

transistor size and similar biasing. Thus the value of $\left(\frac{\partial V_{GS}}{\partial T} - \frac{\partial V_T}{\partial T}\right)$ is around $460 \mu\text{V}/^\circ\text{C}$ and

has a PTAT nature.

The variation of mobility with temperature is much smaller when compared to that of $(V_{GS} - V_T)$ and thus the current has a PTAT nature. The variation of the current and output PTAT voltage across temperature is shown in Figures 3.3 and 3.4 below.

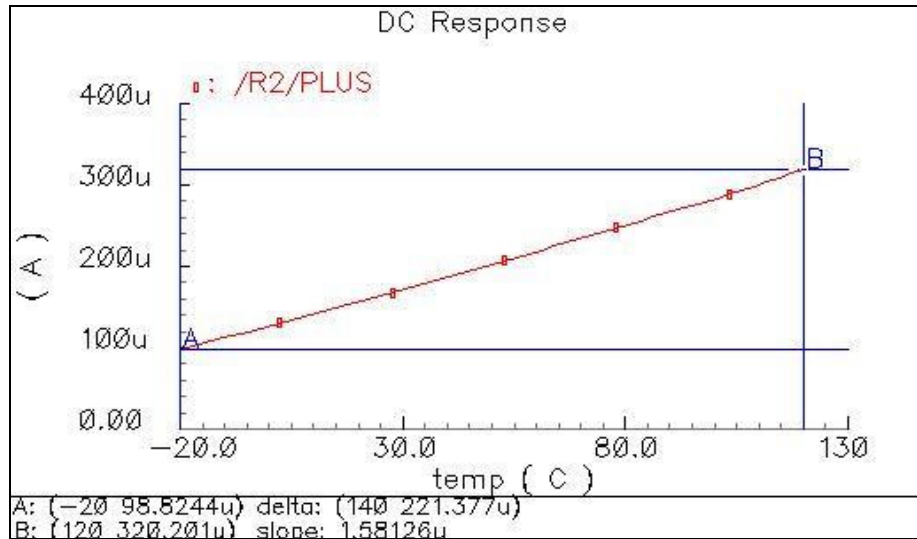


Figure 3.3 – PTAT current

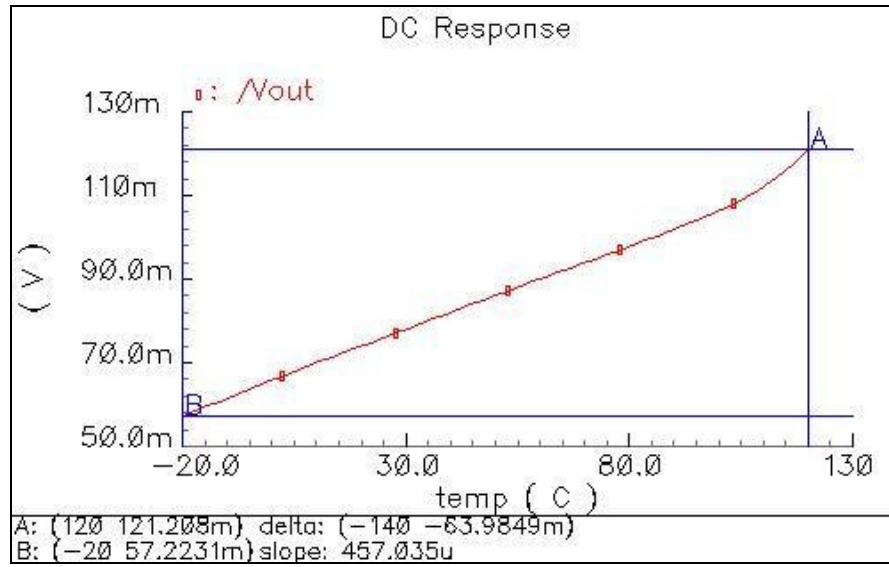


Figure 3. 4 – PTAT voltage drop across the output resistor

3.2.2 CTAT Current Generation

The most conventional technique for generating the CTAT (voltage/current) is through the use of V_{be} of the BJT.

Here the V_{be} of the vertical PNP that is present in the technology is used. The variation of the V_{be} of the VPNP BJT with respect to temperature is shown in Figure 3.5 below. As seen from the Figure 3.5, the voltage varies about 253.625 mV for the temperature range of -20°C to 120°C at a slope of $-1.812 \text{ mV}/^{\circ}\text{C}$.

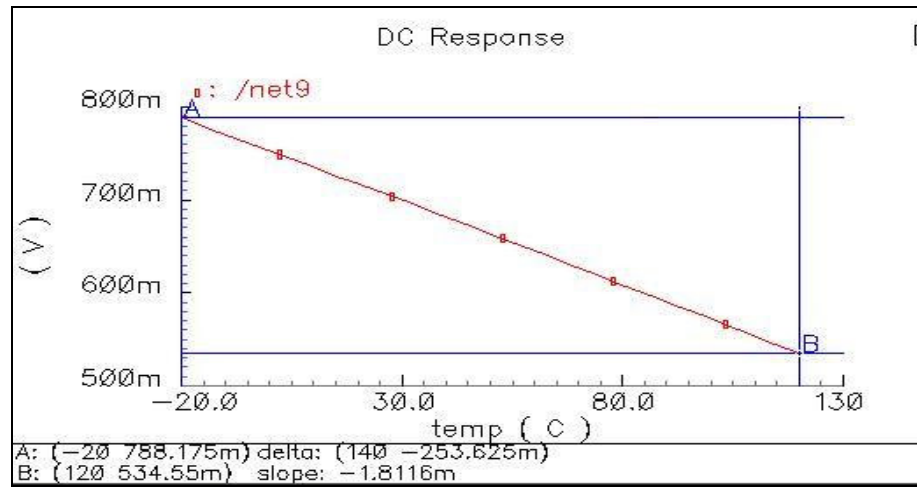


Figure 3.5 – Variation of PN junction voltage with temperature

This variation is too large compared to that of the PTAT current across the output resistor R_3 . This is reduced in its value by allowing a PTAT V_{GS} for the current mirror transistor M_1 . This reduces the slope of the V_{be} temperature dependence and thus the voltage is a little less CTAT than before. Additionally, the resistor divider network of R_2 and R_3 helps in reducing the slope of the CTAT voltage across R_3 more.

The circuit generating the CTAT quantity is shown in Figure 3.6 below.

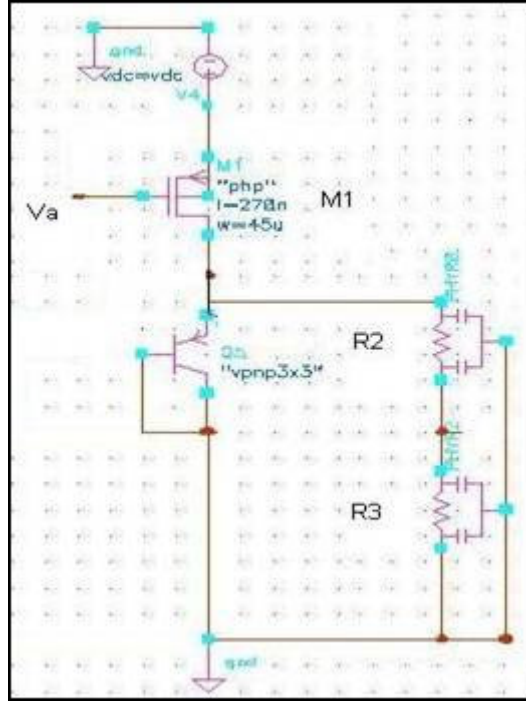


Figure 3.6 – Circuit generating CTAT quantity

Neglecting the base current for the BJT we have,

$$V_{BE} = V_{thermal} \ln \left(\frac{I_{BJT}}{I_S} \right) \quad (3.6)$$

where $V_{thermal}$ is the thermal voltage and I_S is the saturation current which can be related to the device structure by

$$I_S = \frac{qAn_i^2 D_n}{Q_B} = Bn_i^2 D_n = B'n_i^2 T\mu_n \quad (3.7)$$

Here n_i is the intrinsic minority carrier concentration, Q_B is the total base doping per unit area, μ_n is the average electron mobility in the base, A is the emitter base junction area and T is the temperature. Here, the constants B and B' involve only temperature-independent quantities.

The quantities that are temperature dependent are given by

$$\begin{aligned}\mu_n &= CT^{-n} \\ n_i^2 &= DT^3 \exp\left(-\frac{V_{G0}}{V_{thermal}}\right)\end{aligned}\quad (3.8)$$

Here V_{G0} is the bandgap voltage of silicon extrapolated to 0°K and the value of n is approximately 1.5 as shown in equation (3.5).

C and D are temperature-independent quantities. Combining the above four equations yields

$$V_{BE} = V_{thermal} \ln\left(I_{BJT} T^{-\gamma} E \exp\left(\frac{V_{G0}}{V_{thermal}}\right)\right) \quad (3.9)$$

E is another temperature independent constant and $\gamma = 4 - n \approx 2.5$.

For our circuit, the current I_{BJT} varies with temperature. We assume for the time being that the temperature variation is known and that it can be written in the form

$$I_{BJT} = GT^\alpha \quad (3.10)$$

Here G is another temperature-independent constant.

$$V_{BE} = V_{G0} - V_{thermal} [(\gamma - \alpha) \ln T - \ln(EG)] \quad (3.11)$$

In the above equation V_{G0} , E & G are temperature independent quantities.

$$\begin{aligned}\frac{\partial V_{BE}}{\partial T} &= \frac{\partial}{\partial T} [V_{thermal} (\alpha - \gamma) \ln T + V_{thermal} \ln(EG)] \\ \therefore \frac{\partial V_{BE}}{\partial T} &= \frac{\partial V_{thermal}}{\partial T} (\alpha - \gamma) \ln T + \frac{(\alpha - \gamma) V_{thermal}}{T} + \frac{\partial V_{thermal}}{\partial T} \ln(EG)\end{aligned}\quad (3.12)$$

$(\alpha - \gamma)$ has a value of approximately -2.

$\frac{\partial V_{thermal}}{\partial T}$ can be calculated as shown below.

$$V_{thermal} = \frac{kT}{q} \quad (3.13)$$

Here k is Boltzmann's constant, T is absolute temperature and q is electronic charge. Thus we have,

$$\frac{\partial V_{thermal}}{\partial T} = \frac{\partial}{\partial T} \left(\frac{kT}{q} \right) = \frac{k}{q} = 8.62 \times 10^{-5} \text{ V/}^\circ\text{K}. \quad (3.14)$$

Thus the resulting value of $\frac{\partial V_{BE}}{\partial T}$ is CTAT in nature. The value of the V_{be} drop across the output resistor R_3 across temperature is shown in Figure 3.7 below. This slope of V_{be} is exactly enough to cancel the PTAT-natured slope of the current produced by the transistor M_2 across the same output resistor.

Figure 3.7 below shows the current through the resistor network

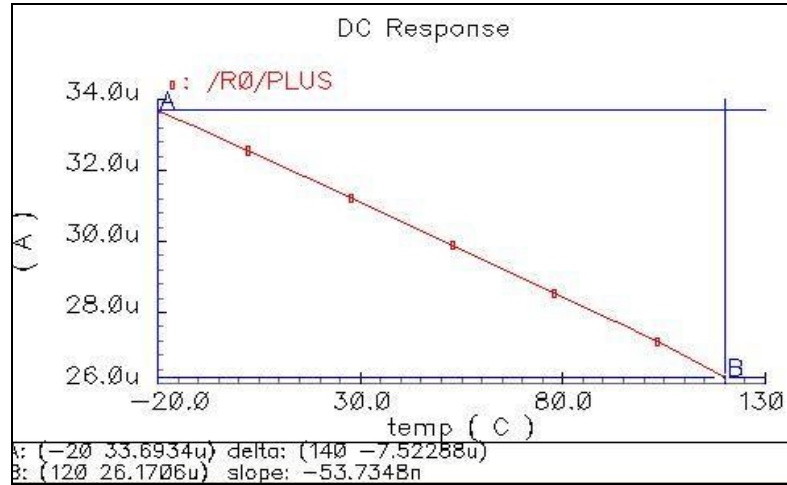


Figure 3.7 – Current through the resistor network

Figure 3.8 below shows the voltage drop across the output resistor caused by the CTAT generation circuit.

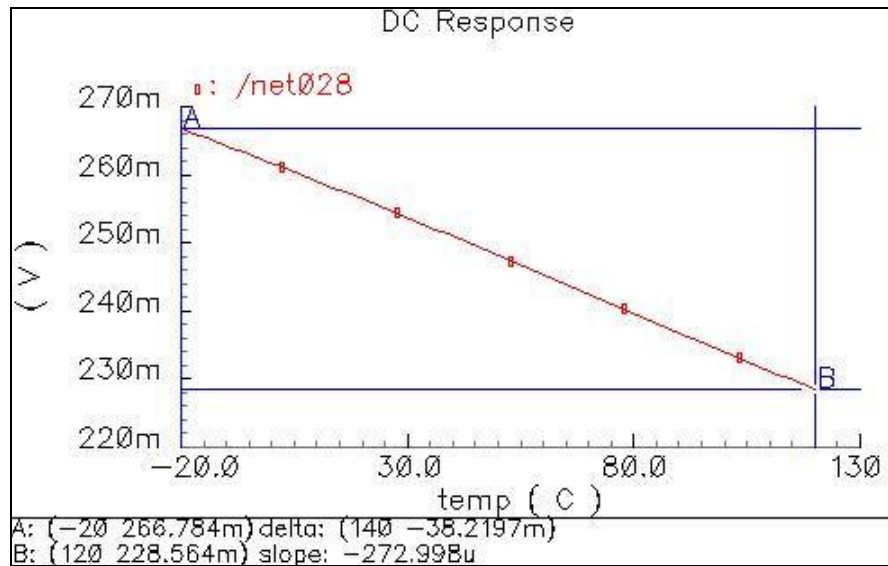


Figure 3.8 – Voltage drop across output resistor due to the CTAT generation circuit

3.3 CTAT VOLTAGE GENERATION AT THE BASE OF CURRENT

MIRROR TRANSISTORS

The CTAT voltage (i.e., the PTAT V_{gs} for PMOS) is generated by the biasing circuit which consists of two diode-connected transistors M_3 and M_4 . The biasing circuit is shown in Figure 3.9 below.

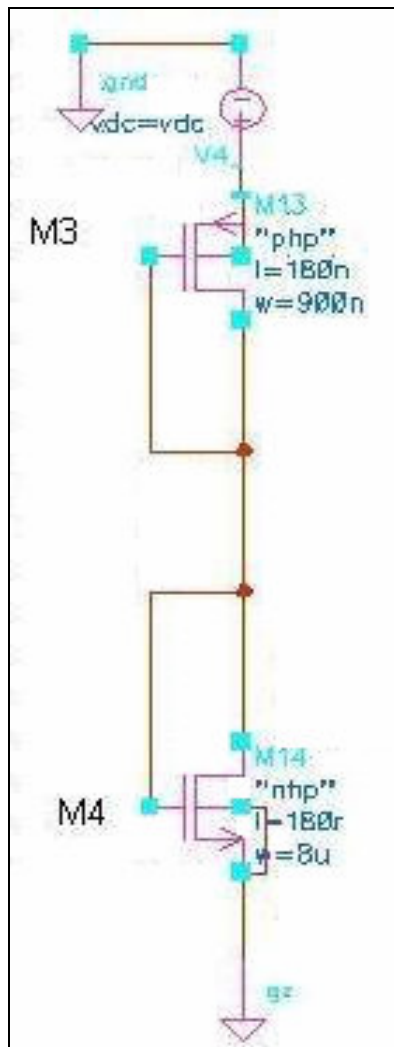


Figure 3.9 – Biasing Circuit

The output here can be given as

$$V_{OUT} = \frac{V_{DD}}{\frac{1}{g_{mn}} + \frac{1}{g_{mp}}} \times \frac{1}{g_{mn}} \quad (3.15)$$

where g_{mp} and g_{mn} are tranconductances of the PMOS and the NMOS transistors respectively.

$$\therefore V_{OUT} = \frac{V_{DD} \cdot g_{mp}}{g_{mp} + g_{mn}} \quad (3.16)$$

$$\therefore \frac{\partial V_{OUT}}{\partial T} = V_{DD} \left[\left(\frac{\partial g_{mp}}{\partial T} \times \frac{1}{g_{mp} + g_{mn}} \right) - \left(\frac{g_{mp}}{(g_{mp} + g_{mn})^2} \times \left(\frac{\partial g_{mp}}{\partial T} + \frac{\partial g_{mn}}{\partial T} \right) \right) \right] \quad (3.17)$$

For the sake of derivation we will assume that $\left(\frac{\partial g_{mp}}{\partial T} \right) = \left(\frac{\partial g_{mn}}{\partial T} \right) = \left(\frac{\partial g_m}{\partial T} \right)$.

$$\therefore \frac{\partial V_{OUT}}{\partial T} = \frac{V_{DD}}{(g_{mp} + g_{mn})^2} \times \frac{\partial g_m}{\partial T} \times (g_{mn} - g_{mp}) \quad (3.18)$$

In the above equation the two terms that will decide the nature of the output are

$$\frac{\partial g_m}{\partial T} \text{ and } (g_{mp} - g_{mn}).$$

Here, $g_{mn} > g_{mp}$ as the transconductance for NMOS is greater than PMOS if they are similarly sized. Here, since NMOS is much larger than PMOS we surely have $g_{mn} > g_{mp}$.

The transconductance can be calculated as

$$g_m = \frac{\partial I_D}{\partial V_{GS}}. \quad (3.19)$$

Temperature dependency of g_m can be defined as

$$g_m(T) = k(T) \times (V_{GS} - V_T(T)). \quad (3.20)$$

As discussed earlier both V_{th} and k decrease with the rise in temperature. But the effect of $k(T)$ is more than that of $V_{th}(T)$. Thus the overall value of g_m reduces with the increase in temperature. This change in g_m is more than that of $(g_{mn} - g_{mp})$, and thus the output is of CTAT in nature.

The variation of the output with respect to temperature is shown in Figure 3.10 below

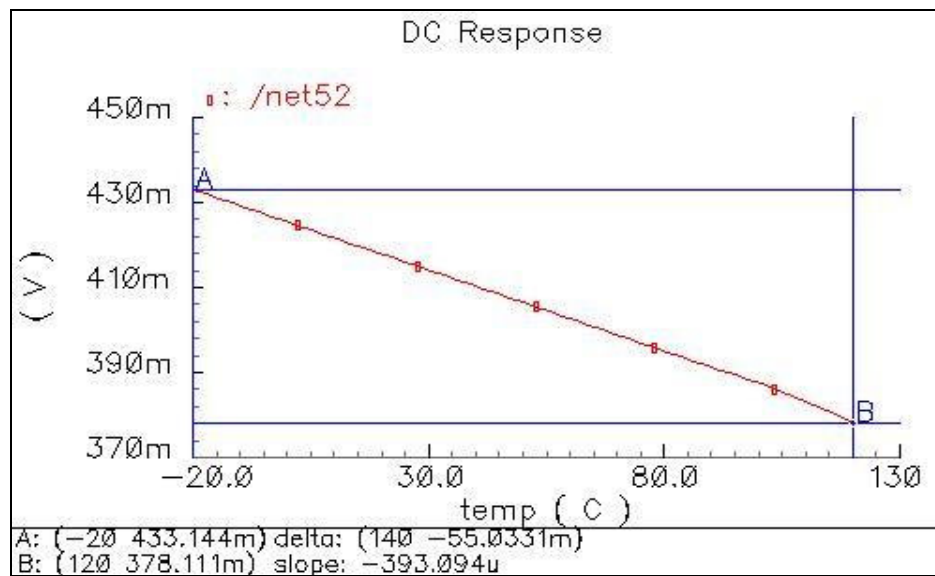


Figure 3.10 – Output from the biasing circuit

3.4 BANDGAP OUTPUT

The output of the circuit can be calculated by using the current in the two branches. If we assume the currents in the two branches to be I_1 and I_2 then the voltage V_{out} can be defined as

$$V_{OUT} = (I_1 + I_2)R_3 \quad (3.21)$$

$$\therefore V_{OUT} = \left(\frac{V_{BE}}{R_1 + R_2} + I_2 \right) R_3 \quad (3.22)$$

Using the above relation a desired value for V_{out} can be obtained by iterating the values of R_1 , R_2 and R_3 . The output of a particular configuration of the resistors is shown in the Figure 3.11 below.

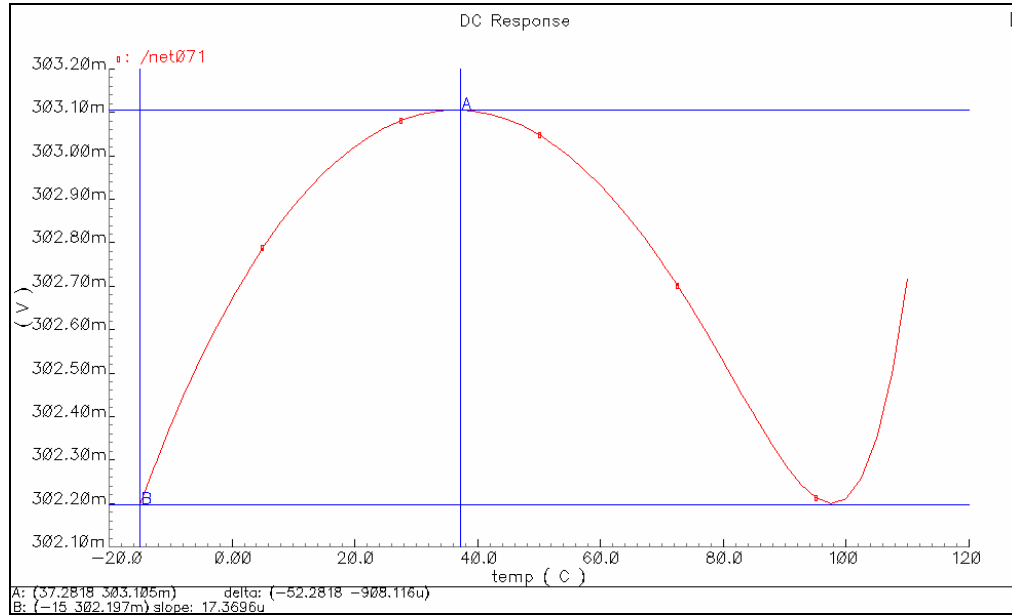


Figure 3.11 - Bandgap output for a particular combination of resistors

Depending on the need of the application the value of the bandgap output voltage can be changed using different combination of resistors. The current consumption in this case was 96μA. The BJT was using 60 μA of the total current consumed. 5 μA of current was unaccounted for in the simulation and is assumed to be the leakage current of the BJT.

Versions of the Bandgap Reference

- 4.1 Versions of the Bandgap Reference**
 - 4.2 Circuit Variation # 1**
 - 4.3 Circuit Variation # 2**
 - 4.4 Comparison Chart**
-

4.1 VERSIONS OF THE BANDGAP REFERENCE

This section will discuss two different architectures of the bandgap reference circuit explained in the previous section. The bandgap reference circuit explained in the previous section varies only $900\text{ }\mu\text{V}$ over a temperature variation from -20°C to 120°C . The circuit exhibits a very low PSRR. The Figure 4.1 below shows bandgap voltage variation over the supply voltage variation from 950 mV to 1050 mV .

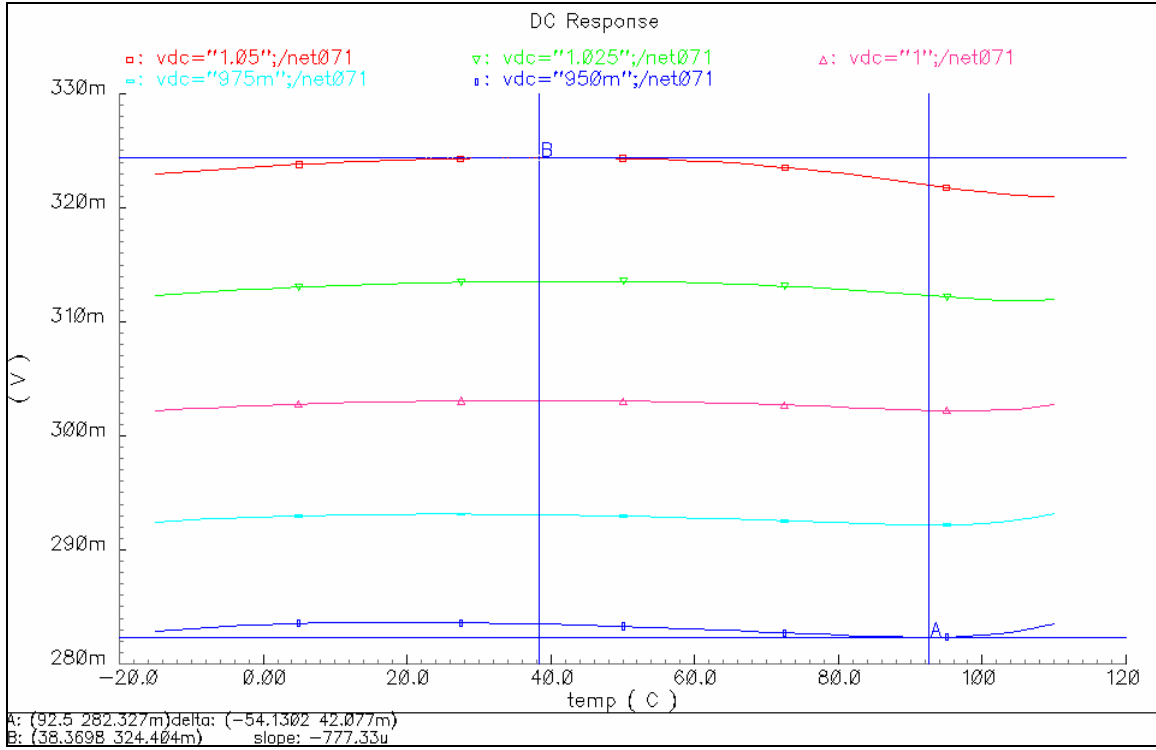


Figure 4.1 – Voltage supply variation of the basic BGR circuit

The PSRR of the circuit can be calculated by the equation

$$PSRR = 20 \log \left(\frac{\Delta V_{POWER-SUPPLY}}{\Delta V_{BANDGAP-OUTPUT}} \right) \text{ in dB} \quad (4.1)$$

$$PSRR = 20 \log \left(\frac{100mV}{42.077mV} \right) = 7.5191db \quad (4.2)$$

This circuit as shown in the figure above has a PSRR of about 7.5 dB. This is very small as generally a good bandgap reference circuit should have a PSRR of about 20 dB. The advantage of this configuration is that it has an accuracy of 21 ppm/°C.

Two variants of the basic bandgap reference circuit will be discussed in this section. Both of the circuits have a better PSRR than the present circuit. The first one supports a wider range on the bandgap voltage reference with an improved PSRR. The other circuit supports only a very low (up to 200 mV) bandgap reference output voltage but has a very good PSRR as compared to the other two circuits.

4.2 - CIRCUIT VARIATION # 1

This circuit as shown in Figure 4.2 keeps the most of the configuration of the original circuit. The basic PSRR issue in the original circuit was the fact that the PTAT generating PMOS transistor is directly connected to the power supply. So any variation in the power supply directly affects the output of the circuit. Whereas the CTAT generating BJT is shielded from the power supply through the current mirror transistor. In this variation of the circuit the PTAT generating MOS is connected to a less variable voltage as generated by the bias circuit.

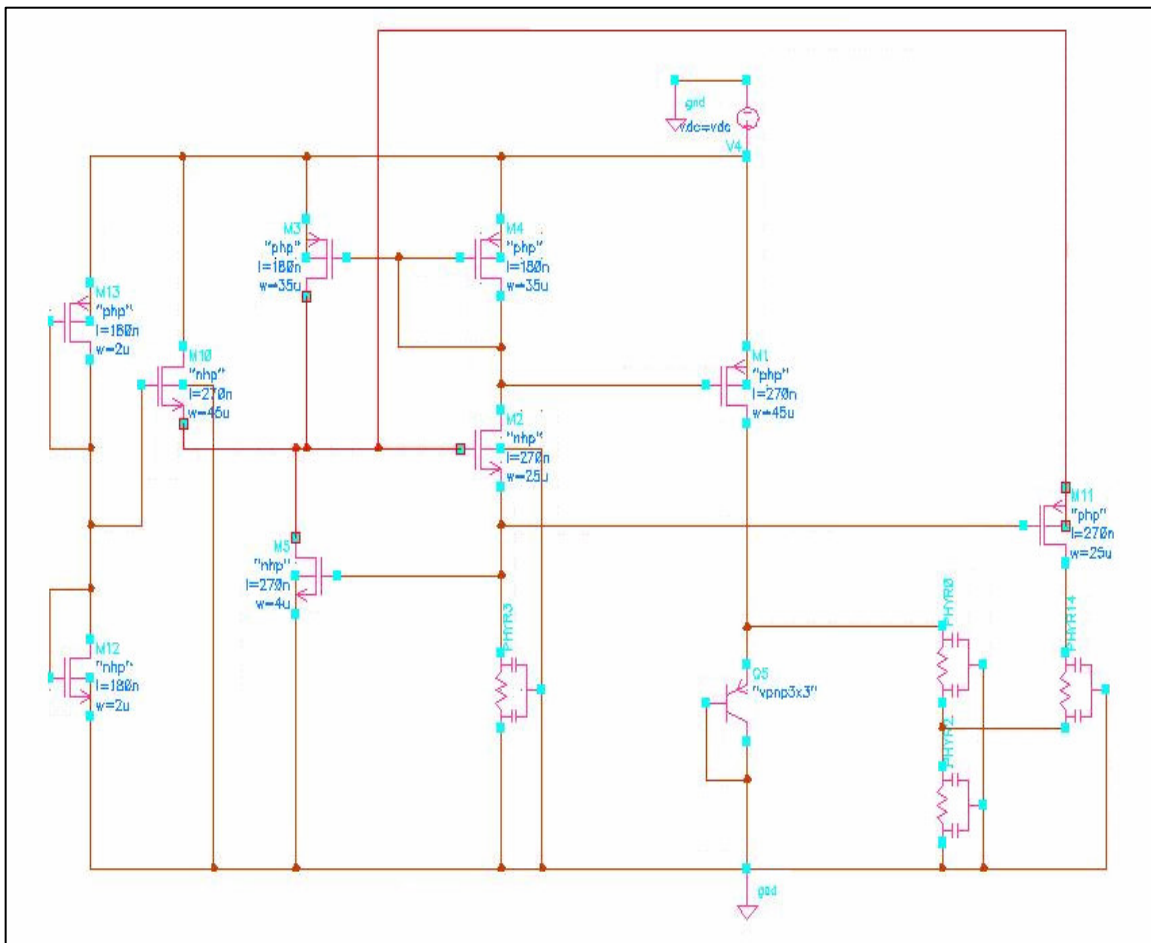


Figure 4.2 – Circuit Variation # 1

The biasing method used here as shown in Figure 4.3 is known as threshold voltage self biasing. The idea here is to get the current in the transistor M5 to be almost independent of supply voltage variations. This would make the voltage drop across the resistor R4 to be independent of supply voltage and will thus depend only on temperature.

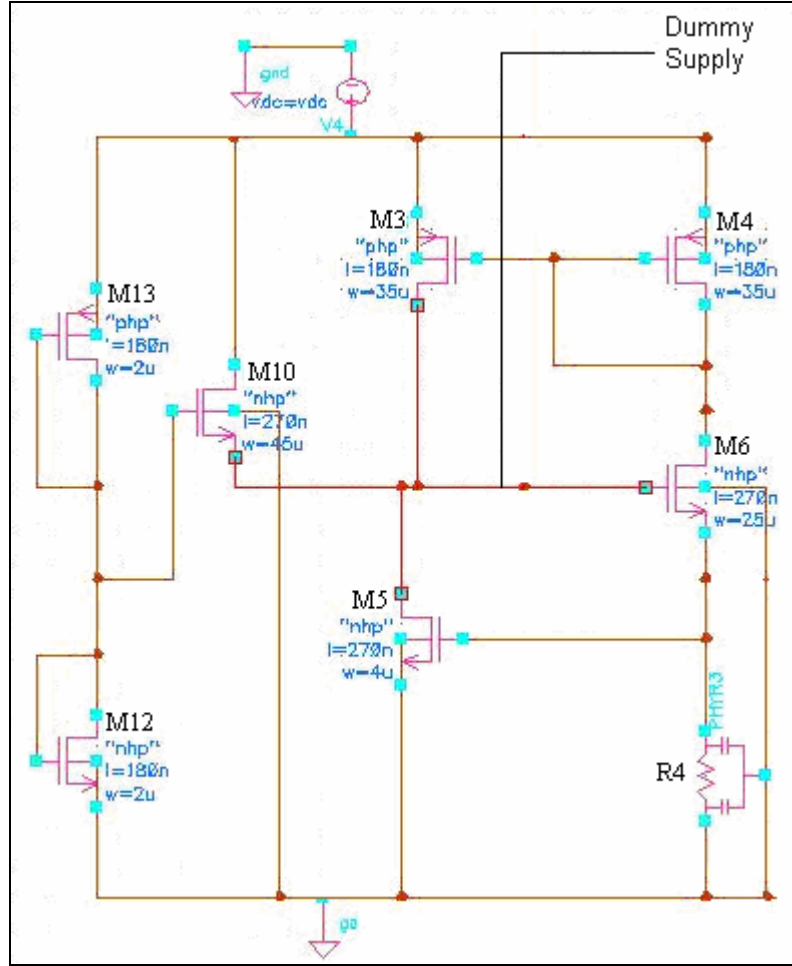


Figure 4.3 – Threshold voltage self biasing

If we neglect the body effects and the channel length modulation effects then we can define the drop across the resistor as

$$V_{R4} = V_{GS8} = V_{THN} + \sqrt{\frac{2I_{R4}}{(W/L)_5 C_{OX}}} \Rightarrow I_{R4} = \frac{V_{GS8}^2}{R} \approx \frac{V_{THN}^2}{R} \quad (\text{If } (W/L)_5 C_{OX} \text{ is large}) \quad (4.3)$$

This result implies that current I_{R4} will be independent of supply voltage. In practice, this is not true due to the finite output resistance of the MOSFET's.

The accuracy of current I_{R4} is determined by the threshold voltage accuracy and the resistor accuracy, which could vary 20%. Note also that threshold voltage's TC and the resistor's TC determine the circuit's temperature dependency. The temperature coefficient of the resistor is positive while that of the threshold voltage is negative.

Consequently, the threshold voltage self-biasing technique provides a current with a large negative temperature coefficient. This in the original circuit was done by the two diode connected transistors making up the biasing circuit. The CTAT nature of this voltage is very important to the functionality of the circuit as explained in the previous section.

The startup of the bias circuit is taken care of by the transistor M9 to avoid the zero current initial condition. The PTAT generating PMOS is provided with a power supply by a point on the bias circuit shown as the "Dummy Supply". The characteristic needed in the supply is that it should vary very little with temperature and with actual supply voltage variation. But in this case the supply voltage has a PTAT nature as shown in Figure 4.4 below.

The biasing for the start-up circuit is provided by two diode-connected transistors as shown in the figure. The circuit will not be affected by the PVT variations involving this two transistor biasing circuit.

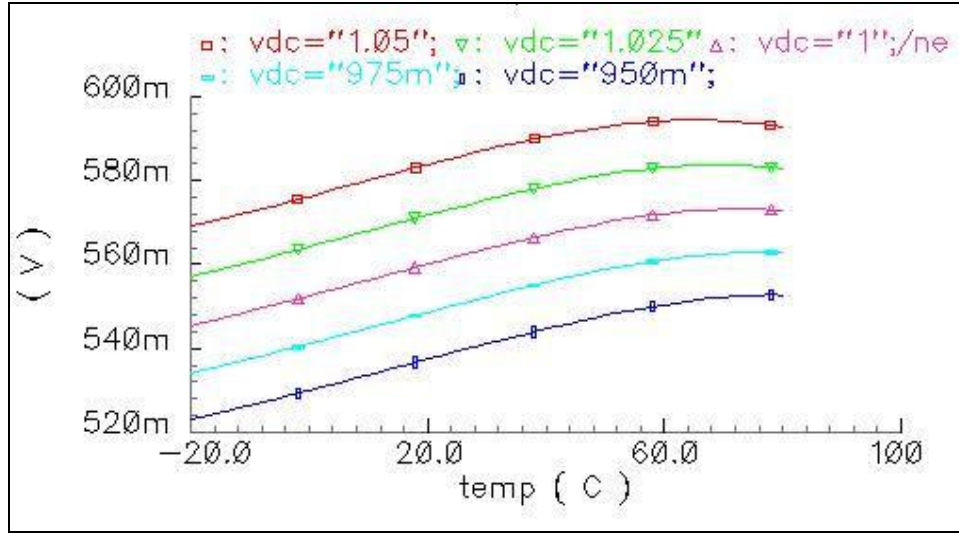


Figure 4.4 – Supply Voltage for the PTAT generating part of the circuit

This PTAT nature of the supply voltage results in a PTAT V_{GS} for the transistor. This PTAT V_{GS} generates a PTAT current as explained in the previous chapter. The variation of this voltage over 100 mV supply voltage variation is about 50 mV and thus the circuit exhibits a better PSRR compared to the original circuit.

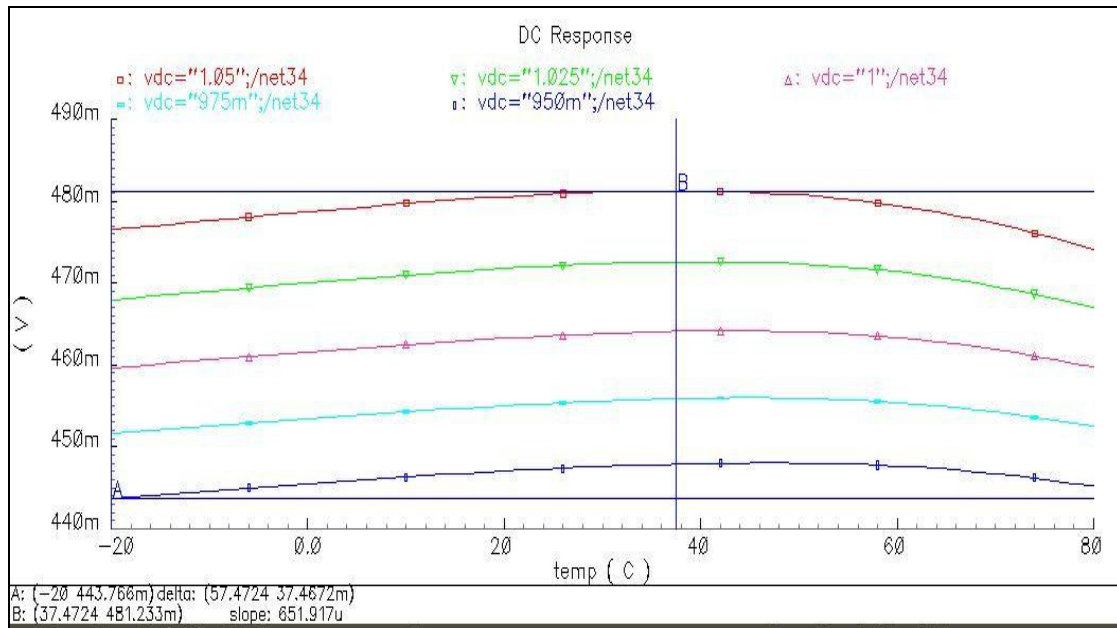


Figure 4.5 – Variation of Output voltage with 100 mV supply voltage variation

The PSRR of the circuit can be calculated by the equation

$$PSRR = 20 \log \left(\frac{\Delta V_{POWER-SUPPLY}}{\Delta V_{BANDGAP-OUTPUT}} \right) \text{ in dB} \quad (4.4)$$

$$PSRR = 20 \log \left(\frac{100mV}{37.4672mV} \right) = 8.5269db \quad (4.5)$$

The improvement in the PSRR comes only at the cost of bandgap voltage range and accuracy over temperature. The accuracy of the circuit as shown in Figure 4.6 below is about 96 ppm/°C which is low as compared to the original circuit. The dummy supply voltage used here reduces the bandgap voltage range considerably. The cancellation of the PTAT and the CTAT quantities is also affected. This causes a reduction in accuracy over the temperature range. In the original circuit the output varies only about 900 μ V over a temperature range of -20 °C to 120 °C. The variation for this version is around 5 mV over the temperature range of -20 °C to 80 °C as shown in Figure 4.6 below. The current consumed by this configuration was 114 μ A.

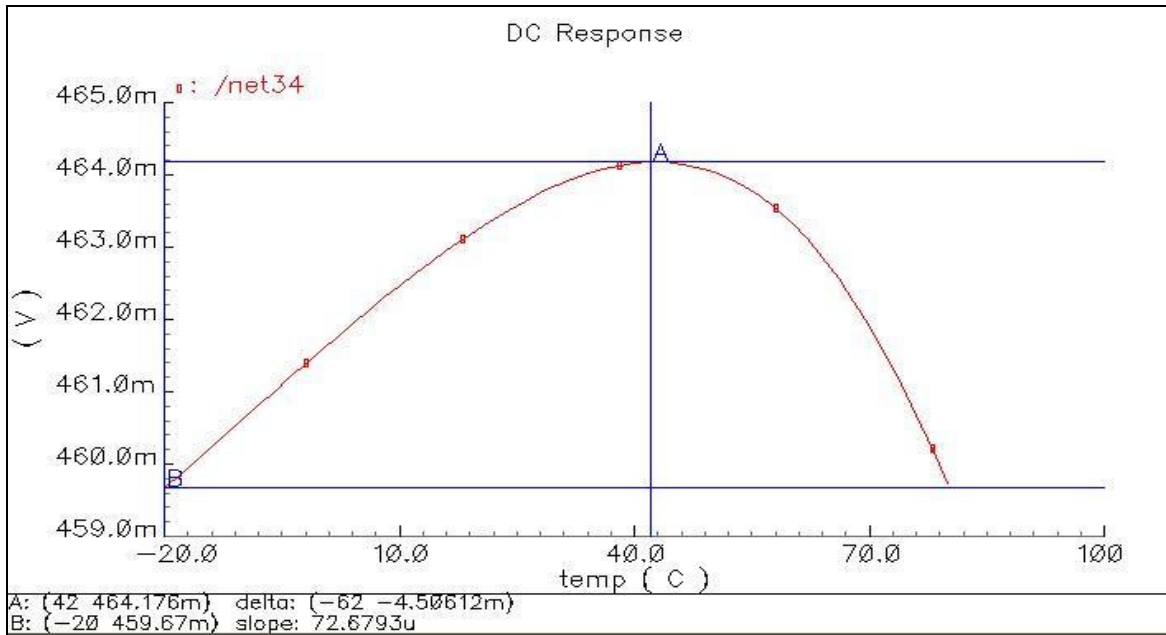


Figure 4.6 – Performance over temperature

4.3 - CIRCUIT VARIATION # 2

This variation of the circuit offers a significantly improved PSRR compared to the other two variations. This improvement in PSRR comes at the cost of lack of range in the output for the bandgap reference circuit. The circuit configuration is shown in Figure 4.7 below.

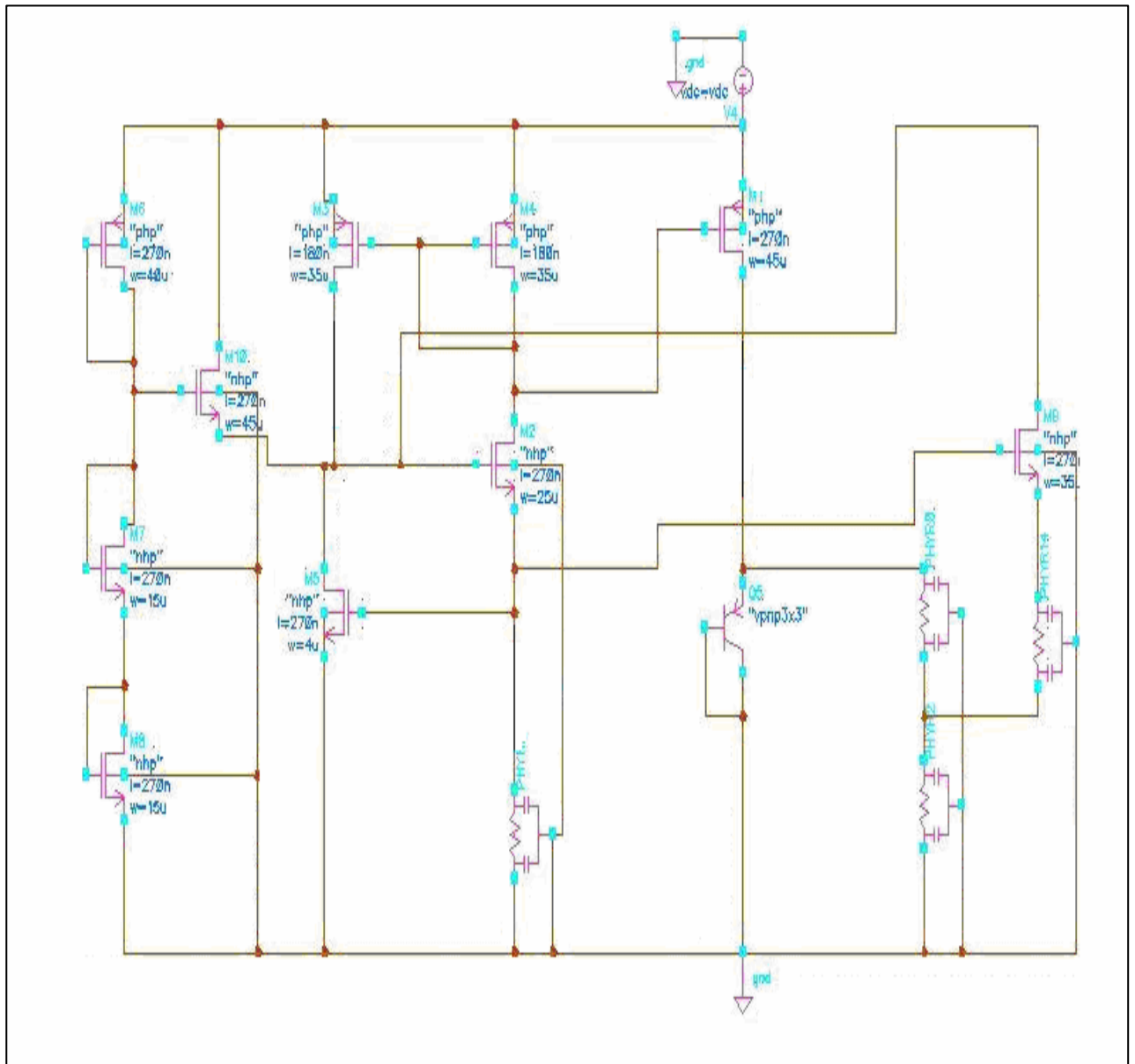


Figure 4.7 – Circuit variation # 2

This variation of the original circuit is essentially the same as the first one. The only difference is that the PTAT generation circuit here uses a NMOS transistor in the source follower configuration. The advantage of this circuit is that the PSRR is very good but the major disadvantage of this configuration is the range of the output voltage. It is only usable up to 250 mV.

Figure 4.8 below shows the output voltage over supply voltage variation of 100 mV.

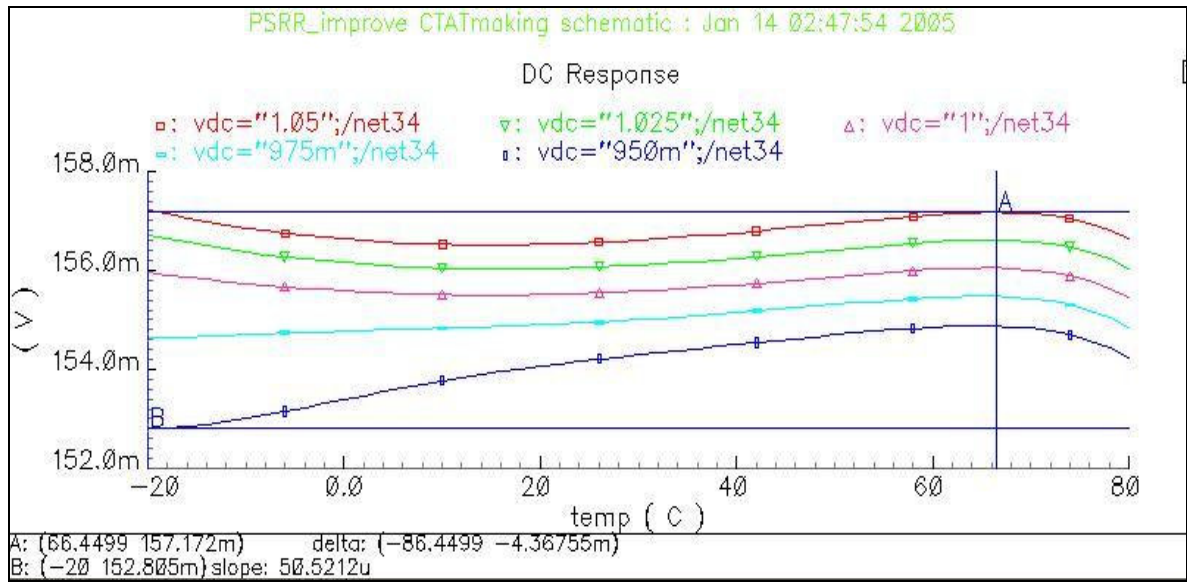


Figure 4.8 - PSRR of Circuit Variation # 2

The PSRR of the circuit can be calculated by the equation

$$PSRR = 20 \log \left(\frac{\Delta V_{POWER-SUPPLY}}{\Delta V_{BANDGAP-OUTPUT}} \right) \text{ in dB} \quad (4.6)$$

$$PSRR = 20 \log \left(\frac{100mV}{4.3675mV} \right) = 27.2db \quad (4.7)$$

The PSRR of 27.2 dB is very good for a bandgap reference circuit. The other advantage of the circuit is the accuracy over temperature of about 38 ppm/°C. The TC cancellation for this configuration is better than that in circuit variation #1. The variation of the bandgap output voltage over the temperature range of -20 °C to 80 °C is shown in Figure 4.9 below. The current consumed by this configuration was 110 μ A.

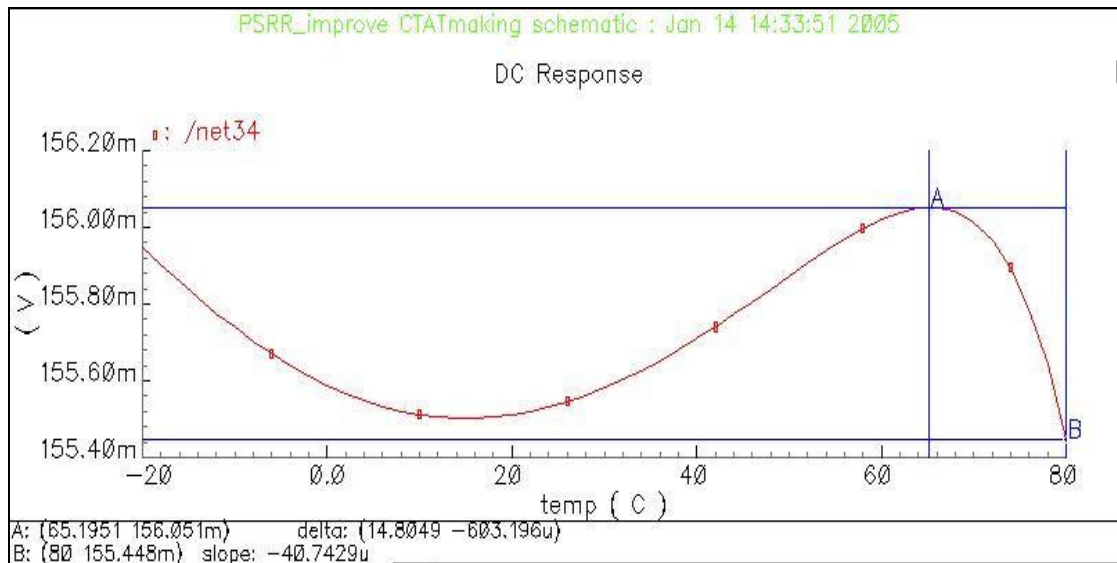


Figure 4.9 – Bandgap output voltage

4.4 - COMPARISON CHART

Table 3 below shows a parametric comparison between the three variations of the bandgap circuit to a good bandgap reference circuit. The good bandgap reference circuit considered here is the one by Banba [5]. As seen from the table every configuration has its own advantages and disadvantages when compared to each other or to the good bandgap reference circuit.

Parameter	Proposed Circuit	Circuit Variation –I	Circuit Variation - II	Popular BGR Circuit
Bandgap Output Voltage	302 mV	460 mV	155 mV	515 mV
Output Voltage Range	200 mV to 600 mV	200 mV to 500 mV	100 mV to 250 mV	N/A
Precision (ppm/°C)	21 ppm/°C	96 ppm/°C	38 ppm/°C	±59 ppm/°C
PSRR (dB)	7.5 dB	8.5269 dB	27.2 dB	N/A

Table – 3 Comparison between the three variations

Process Variations and Transient Response

5.1 Process Variations and Transient Response

5.1.1 Process Variations

5.1.2 Transient Analysis

5.1 PROCESS VARIATIONS AND TRANSIENT RESPONSE

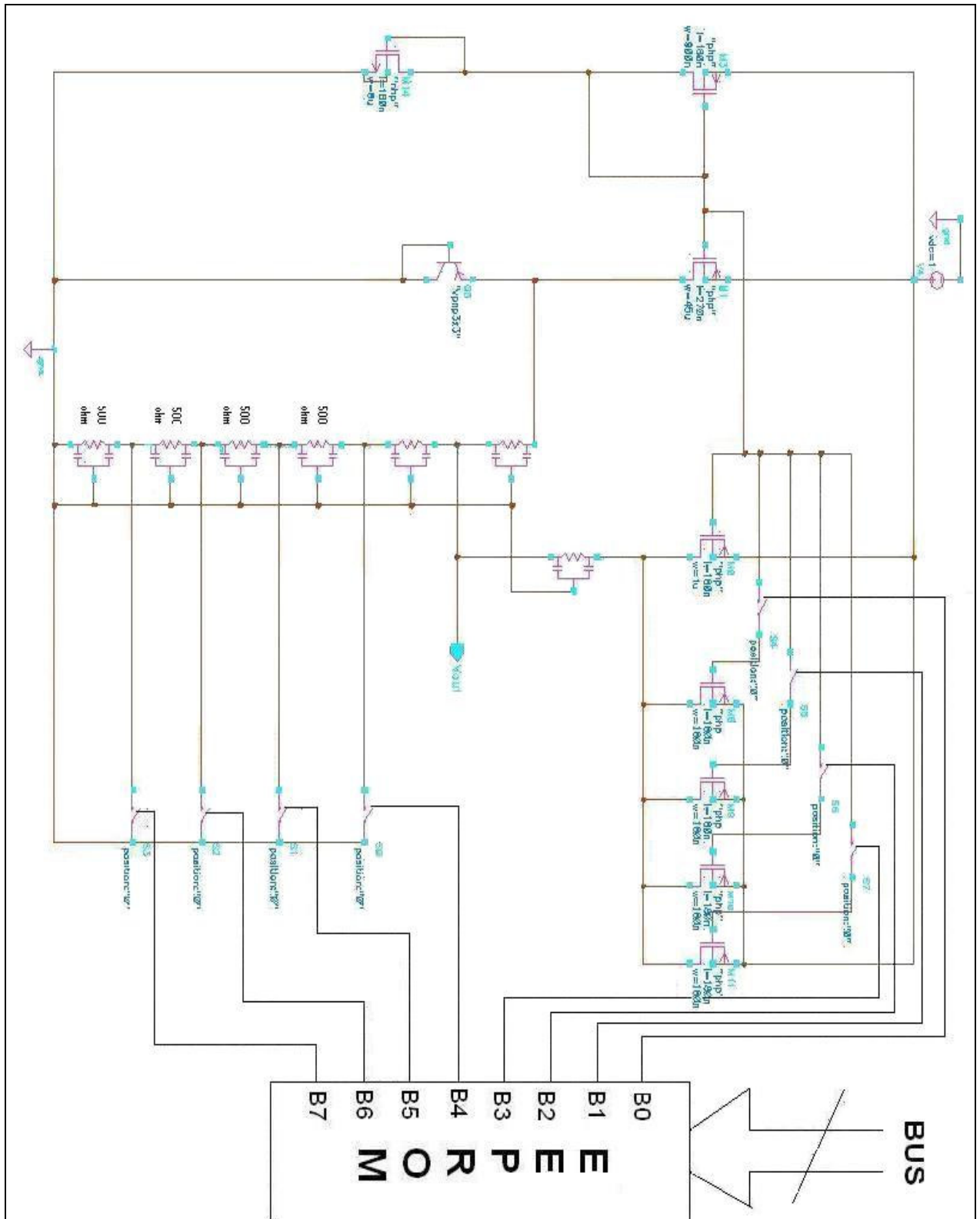
This section will discuss about techniques to protect the circuit from resistor and transistor process variations and the response of the circuit versus time. The process variation remedies are explained for the original circuit. Similar remedies can also be applied to the circuit variations as well.

5.1.1 Process Variations

The variations in the resistors and the transistors affect the circuit in this case. The process variations in the size of the current mirror transistors can result in the alteration of the current that they mirror and thus affect the output voltage of the circuit. The variation in the absolute value of the resistors also affects the circuit as the output voltage relies heavily on the ratio of

the resistors. A digital trim [16] as shown in Figure 5.1 is used here to get the exact resistor and transistor value required.

The limitation of this technique is that the technology should support Electrically Erasable Programmable Read Only Memory (EEPROM). For this circuit 8 trim bits have been used. The current in the output branch is monitored and accordingly the switches on the transistors are controlled. If the current is too low then all the switches are closed and if it is perfect then none are closed. The first four bits $B_0 - B_3$ stored in the EEPROM are devoted for transistor trim. The EEPROM is written with the appropriate bits through a digital bus.



Bits $B_4 - B_7$ are devoted for the resistor trim. The value of the resistor is monitored by external tests and the value is trimmed with the help of the resistor trim bits. Series resistance of $2\text{ K}\Omega$ can be added in series to the output resistance.

As seen from the above discussion, extra width for transistor and extra series resistance can be added to trim them to the exact value. But if the final value of the resistor is more than what is needed then the resistance cannot be removed to come to the exact value. Thus here care is taken that the resistor always comes out either exactly the same or less than the desired value. The same care is taken for the transistors as well.

5.1.2 Transient Analysis

The original circuit does not have any startup circuit. The transient analysis of the circuit shows that it does not need any startup circuit. This makes sense as if we look at the circuit: there is no initial condition requirement and it is safe to assume that the BJT and the PMOS's will start in saturation region. The transient response of the original circuit is shown in Figure 5.2 below.

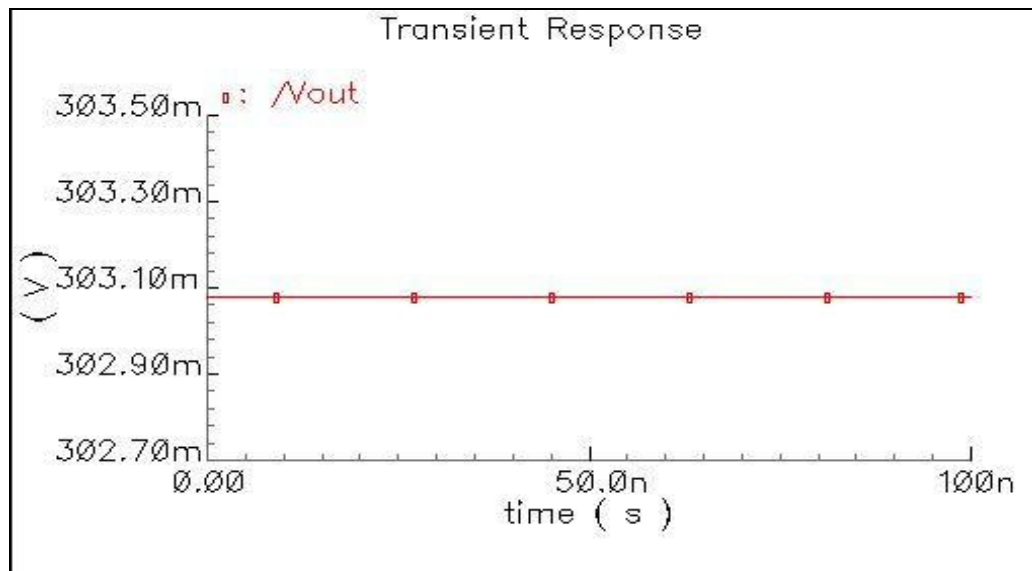


Figure 5.2 – Transient response of the original circuit

The two variations of the circuits are provided with startup circuits as explained in the previous section. These startup circuits insure that the additional circuitry added to the original circuit starts up as we want it to. The transient response of circuit variation # 1 which uses PMOS in the output branch which is powered not by the power supply but by a point in the additional circuitry added is shown in Figure 5.3 below.

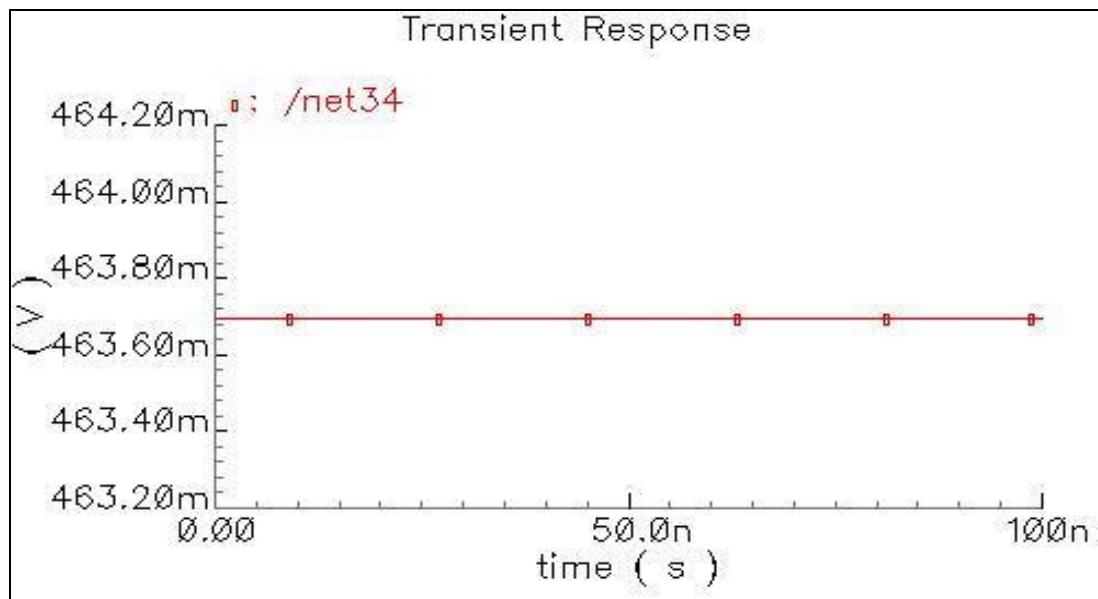


Figure 5.3 – Transient response for Circuit Variation # 1

The circuit variation # 2 also has a start up circuit as mentioned in the previous section. This variation uses an NMOS connected in the source follower configuration in the output branch. The transient response of the circuit is shown in Figure 5.4 below.

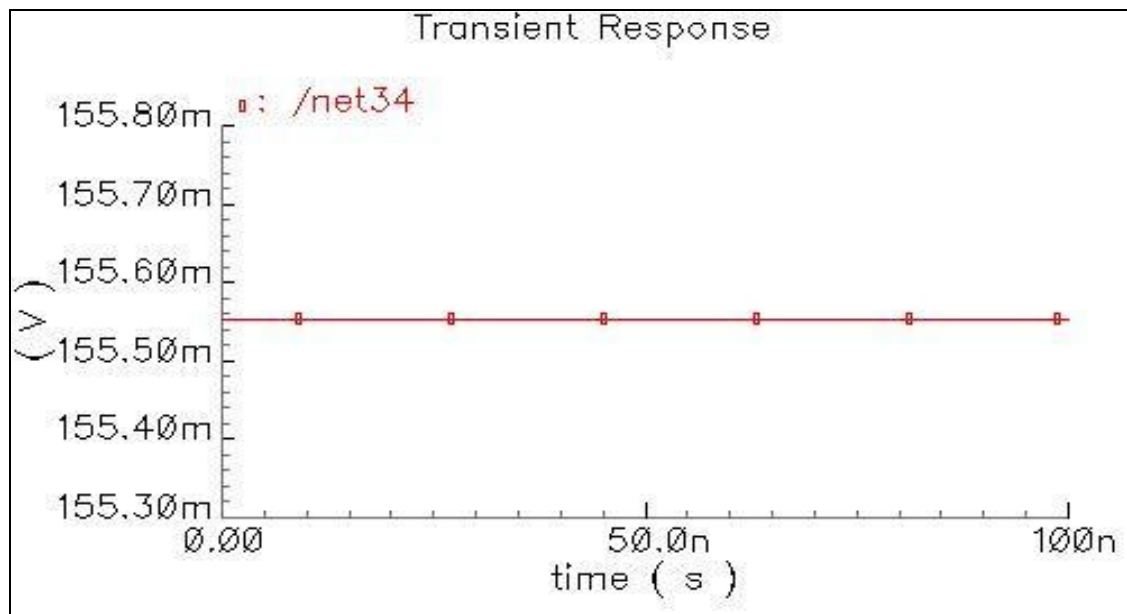


Figure 5.4 – Transient response for Circuit Variation # 2

CONCLUSION AND FUTURE WORK

The goal of this work was to develop a new sub-1 V bandgap reference topology without the use of any special devices. In this work effort is made to understand various topologies of the existing bandgap reference circuits and identify the limitations which make these circuits difficult to use with current processes, mainly with sub-1V technologies. A new topology for bandgap reference was developed which did not use an operational amplifier as used in the conventional circuits.

This new architecture used the current of a BJT to make the conventional CTAT. The PTAT was generated with a PMOS (having PTAT V_{GS} as its gate) and a P+ Poly resistor. Both the currents were summed across a resistor to make a near-zero temperature coefficient voltage reference. The simulation results show a bandgap output voltage of 302 mV with and accuracy of 21 ppm/°C. Two variations of this circuit were introduced to improve on the poor PSRR (7.5 dB) of the proposed circuit. These variations have output voltage of 460 mV and 155 mV with and accuracy of 96 ppm/°C and 38 ppm/°C respectively. They have PSRR's of 8.53 dB and 27.2 dB respectively.

A digital trimming scheme using EE-PROM was proposed to cope with the process variations in the resistors and transistors.

Future Work

The future work will include developing a master circuit which will have all the advantages of the three variations of the circuit proposed in this work. This master circuit will have a good output voltage range, good precision and a very high PSRR.

The EE-PROM based digital trimming may not be feasible in all the technologies. Alternative approaches not using an EE-PROM need to be developed.

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